Integrated Circuit Layout Design Methodology
For
Deep Sub-Wavelength Processes

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Dedication

To my wife Caro

For her boundless love that inspires me to become a better man,

For her unwavering support of my work on this thesis,

For being my emotional rock in times of doubt.

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I want to thank my family and family-in-law for their example, good wishes and words of encouragement.

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One of the critical aspects of semiconductor fabrication is the patterning of multiple design layers onto silicon wafers. Since 180nm processes came online, the semiconductor industry has operated under conditions in which the critical features are smaller than the wavelength of light used during the patterning process. Such sub-wavelength conditions present many challenges because topology, rather than feature width and space, defines the yield characteristics of the devices.

Pattern variability can contribute as much as 80% of the total timing margins defined by traditional SPICE corner models. Because feature variability is undesirable from electrical considerations, this work proposes a physical design verification methodology that emphasizes pattern robustness to process variations. This new method is based on a framework composed of manufacturability objects, operators and guidelines, which permits the definition of a scoring system ranking the manufacturing process and the manufacturability of the designs.

This framework is intended to alleviate circuit design and verification challenges and it based on three new concepts: the first relates to compact process model requirements. The second involves the definition of a new design object, called *pv-Band*, which reflects layout sensitivity to process variations. The third is the specification of two manufacturability metrics that, when optimized, can improve yield by accounting layout sensitivities across multiple design levels (e.g., Active, polysilicon, contact, metal 1, etc.).

By integrating these new concepts (process models, pv-Bands and manufacturability metrics) with existing knowledge, this work moves forward the state-of-the-art of physical design and verification of integrated circuits subject to sub-wavelength effects.

1 Introduction

1.1 Semiconductor Industry Challenges

During the design stage of integrated circuits (ICs), electronic designers have relied on functional and physical verification. The objective of functional verification is to determine the electrical correctness of the design; physical verification assures that an IC design will yield sufficient quantities to make the IC product commercially viable.

As we approach volume production of 90nm devices, risk production of 65nm and active research for 45nm and 32nm processes, there is one clear trend: the interdependence of manufacturing and design processes necessary to build integrated circuits has reached the point where an insufficient description of the process in physical verification design rules seriously jeopardizes the successful production of advanced microelectronic devices.

Existing physical verification design rules are primarily geometric in nature (e.g., spacing, enclosure, width, connectivity and area checks). These geometrical rules are empirical approximations of complex manufacturing behavior that includes optical, chemical and electrical phenomena. Unfortunately, the process and design communities have acknowledged that the current process information being transferred to the designer is no longer sufficient. Evidence of this lack of relevant process information during the design stage has been quantified in the form of historical yield learning curves and maximum attainable yield information. The study of such data indicates a decline in yield for the past process generations[1] from a half micron to 180nm.

To comprehend why newer process generations seem to produce lower maximum attainable yields (as shown in Figure 1), it is important to understand the mechanisms that produce yield-loss. Yield-loss mechanisms can be classified in two groups: random and systematic. The random classification includes particle contamination, scratches, solvent drips, residues, dose or focus drift and vibrations, and can be minimized only during the manufacture of a product. The second classification refers to predictable and reproducible phenomena that in principle can be pre-corrected. For example, by introducing optical proximity corrections it is possible to prevent lithography-induced, iso-dense biases. Similarly, dummy fill insertion is routinely used to minimize the feature degradation that arises from chemical metal polish (CMP) or optical flare induced by heterogeneous density environments.

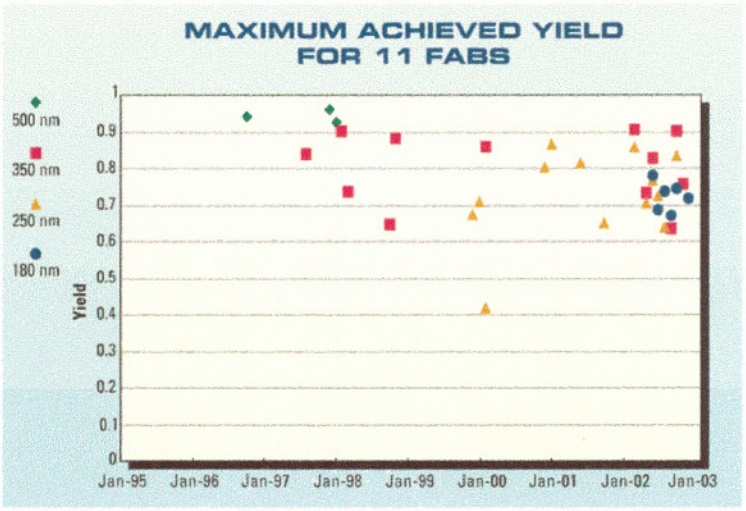


Figure 1. Maximum attainable yield for 500nm, 350nm, 250nm and 180nm processes.[1]

Traditionally, there has been a strong drive to minimize the random components of yield-loss, and special emphasis has been placed on reducing the concentration of particles that can land on the surface of a device. For that reason, there has been an ongoing and successful effort in reducing particle density and particle size distribution. However, as feature sizes continue to shrink (180nm and below), the maximum attainable yield has decreased (Figure 1). The main reason of such decline is the increased relative contribution of systematic induced yield-loss mechanisms. The semiconductor industry has a long history of dealing with random (particle) defects, but this increased contribution of largely process-parameter-dependent yield loss has increased the importance of understanding and managing the systematic contributors to yield-loss.

Prior to 1995, the wavelength of light was equal to or smaller than the target feature to be printed by the lithography process. Figure 2A shows a well publicized graph[2] that ties target feature dimensions to the wavelength used by the lithography process. Although resolution depends on many other variables in addition to wavelength, this graph provides a good qualitative description of the effects that yield analysis tools need to address in order to process features smaller than a quarter micron.

Figure 2B presents the maximum attainable yield per feature size and the yield learning curve for each process for a large variety of products and process implementations.[1] The arrows connecting insets A and B attempt to qualitatively correlate the sudden jump in yield-loss to the size of the sub-wavelength gap. Interestingly, 180nm processes were the first to introduce rudimentary forms of optical proximity corrections that are now used extensively and in more advanced forms for all processes with target features smaller than 130nm.

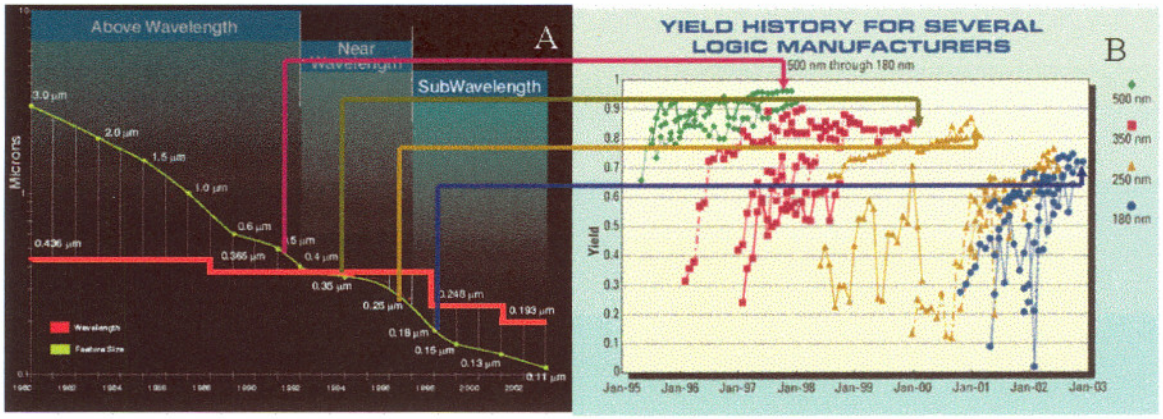


Figure 2. Sub-wavelength gap[2] and its correlation to maximum attainable yield.[1]

At this point, it would be sensible to assume these new resolution enhancement technologies (RET) could fill the sub-wavelength gap, as they have successfully done until now, but this is merely wishful thinking. Although certain RET methods can in theory fill the sub-wavelength gap,[3] they do so only for specific patterns or geometric topologies.

This means that for any sub-wavelength process, there will be specific design restrictions that, unless implemented, will cause the resolution to remain limited by the more traditional optical limits of numerical aperture, partial coherence and wavelength.

It is now possible to extend the classification of yield-loss mechanisms by including explicitly process variations. This is necessary because a complete elimination of the systematic yield-loss components would require an absolute and perfect control of the defining process variables. Since such precise control does not exist for any real processes, all yield-loss mechanisms have in essence a random origin. However, the impact these random variations will have on the design depends on the systematic sensitivity of a given element to the type and magnitude of the process variation.

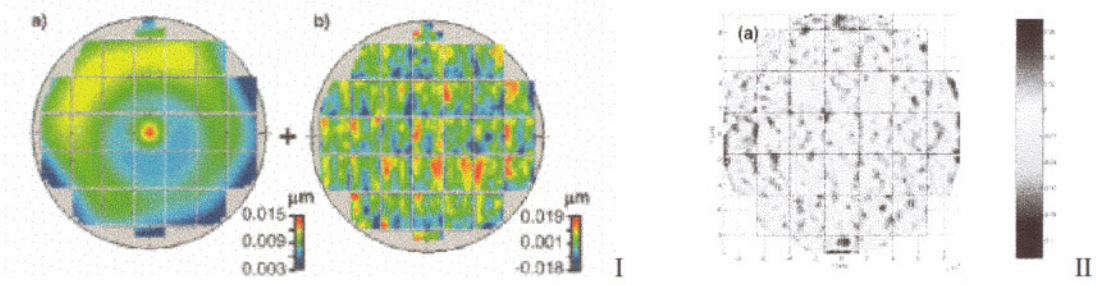


Figure 3. Mean defocus: Wafer component[4] (Ia), field-by-field defocus residuals (removing systematic wafer component)[4] (Ib) and field-by-field residuals (II)[5].

For example, variations in the resist thickness translate into different defocus conditions between dies or wafers. Recent studies[4,5] place the intrinsic process control within a wafer at about 20nm for one standard deviation. Since processes should typically be controlled within six standard deviations, the intrinsic requirement for depth of focus (DOF) is about 240nm.

How much a process fluctuation affects the final yield depends on the magnitude and systematic sensitivity of the design to such variation. By following a statistical process fluctuation approach, Bowman[6] determined that the impact of these random process fluctuations could mean a loss in performance equivalent to a process generation (Figure 4).

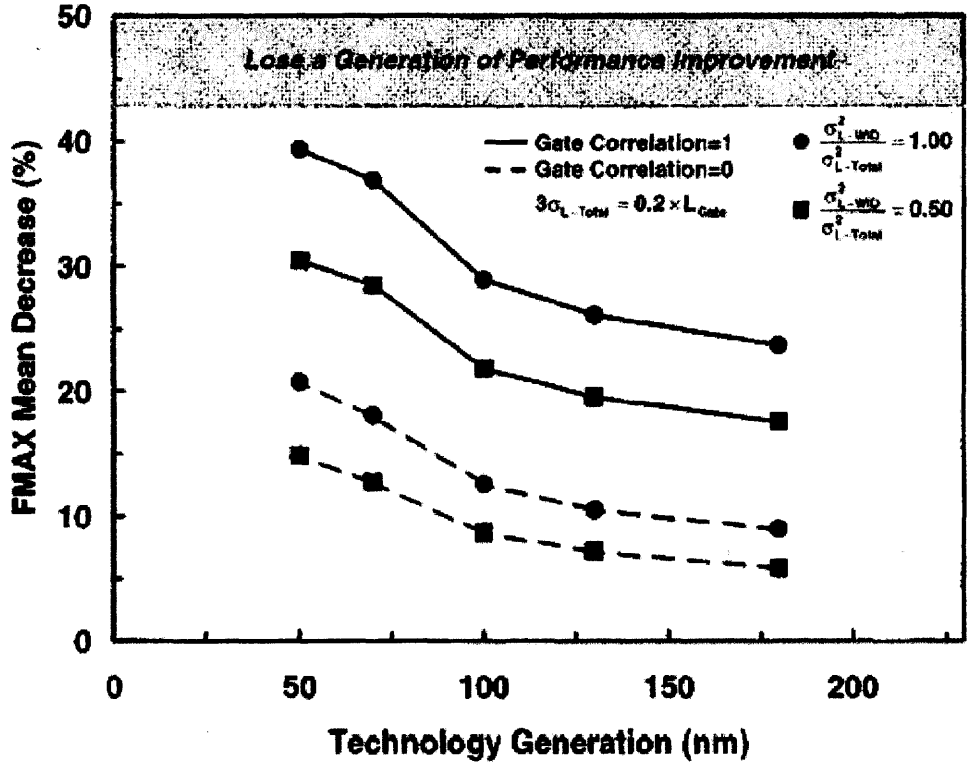


Figure 4. Reduction in maximum frequency resulting from within-die parameter fluctuations versus technology generation. [6]

What Bowman's work does not consider is that the process fluctuations do not affect all features in the design equally. Thus, even if the process variation itself cannot be completely eliminated, it is possible to minimize the design sensitivity to this variation by modifying the layout.

Process variations can be observed at the topological or the electrical level. The topological level refers to the shape and physical attributes of the devices, including critical dimension (CD), minimum pitch and pattern density. Depending on the topological change, the electrical behavior can be affected if the variations occur in electrically sensitive areas of the design (e.g., polysilicon gate width differences

between a pair of matched transistors, or narrowing of long metal lines that subsequently increase resistance). At the same time, topological changes induced by some types of dummy fill, short interconnect paths or non-critical corners of diffusion layers will not present any observable differences in the electrical behavior of the devices.

Until now, only shape-centric parameters such as fidelity (achieved by aggressive RET) and pattern robustness (achieved by manufacturing-aware design) have been considered in the manufacturability of designs. However, other processing effects that are less dependent on shape or structure can also contribute to the final operation of the electronic devices. For example, even when poly gate widths are perfectly matched and robustly built, processing steps such as ion implantation, diffusion or material selection can make an otherwise correct design fail.

With the former paragraph in mind, the scope of this work is to apply relevant DFM principles to the topological or shape aspects of manufacturing in order to bring yield to its historical value. This work does not include the material science or electrical characterization aspects necessary for a complete description of the manufacture of integrated circuits. Instead, it quantifies some electrical variables that shape and topology have on the electrical behavior of devices.

When the non-shape-related effects (such as lack of adequate processing materials or quantum tunneling) become the limiting factors, or the restrictions imposed by this methodology become economically infeasible, it might be necessary to proceed with completely novel manufacturing approaches.

1.2 Toward an IC-DFM Methodology

At present, there are widely known DFM principles,[7] many of which are directly applicable to IC manufacturing, as described by D. M. Anderson (2004):

- Understand manufacturing problems: Issues of current/past products.
- Design for easy fabrication, processing and assembly.
- Adhere to specific process design guidelines.
- Minimize tooling complexity by concurrently designing tooling.
- Specify optimal tolerances for a Robust Design.
- Understand tolerance step functions and specify tolerances wisely.[7]

DFM concepts have already been demonstrated in other manufacturing fields (e.g., automotive and consumer products) and provide clear competitive advantages applicable to any manufacturing business.

- Product design establishes the feature set, how well the features work, hence the marketability of the product.
- The product development process determines how quickly a new product can be introduced into the marketplace.
- The product design determines how easily the product is manufactured and how easy it will be to introduce manufacturing improvements.[7]

The value associated with these concepts has propelled a strong interest in the semiconductor industry. Unfortunately, while there is no shortage of ideas about the objective of DFM,[8,9,10,11,12] there is no general agreement on the specifics. In other words, there is agreement on the outcome of DFM, but there is no consensus on how to achieve it. Considering all the requirements expressed by many authors, perhaps Liebmann has laid out the best general requirements of a successful DFM system:

- ***Improve manufacturability at extremely aggressive patterning resolution*:** A layout that does not rely on tight control of 2-d detail will function even within the limitations of two-beam imaging lithography.
- ***Ensure migrateablility of designs into future technology nodes*:** The resource and time investment in a new layout make it necessary to use a given chip design for multiple technology generations with minimal redesign effort.
- ***Allow for density- and performance-competitive chip designs*:** Constraints that optimize lithography but erase any benefit of moving to the next technology node do not make sense.
- ***Address a broad spectrum of customer objectives with a single design and process solution*:** To leverage the cost of mask and wafer manufacturing, different customers' needs have to be addressed with a common process solution.[13]

Before proposing and presenting existing new approaches to DFM, it is important to know about existing IC-design flows. These are extremely varied and evolving constantly. Figure 5 depicts a typical IC design flow in very general terms by grouping the design and production activities into three main categories: logic, virtual product and physical product.

This organization is based on the evolution of the product, which means that during the logic design, the objective is to capture the functional requirements established by the product concept. At this point the product has incorporated very little information about its final implementation and remains at a conceptual

or architectural stage. As the different operations progress, the product starts to take a virtual form in which macros, cells and libraries are first generated. More information is needed about the final implementation of the product, and continuing verification steps are needed.

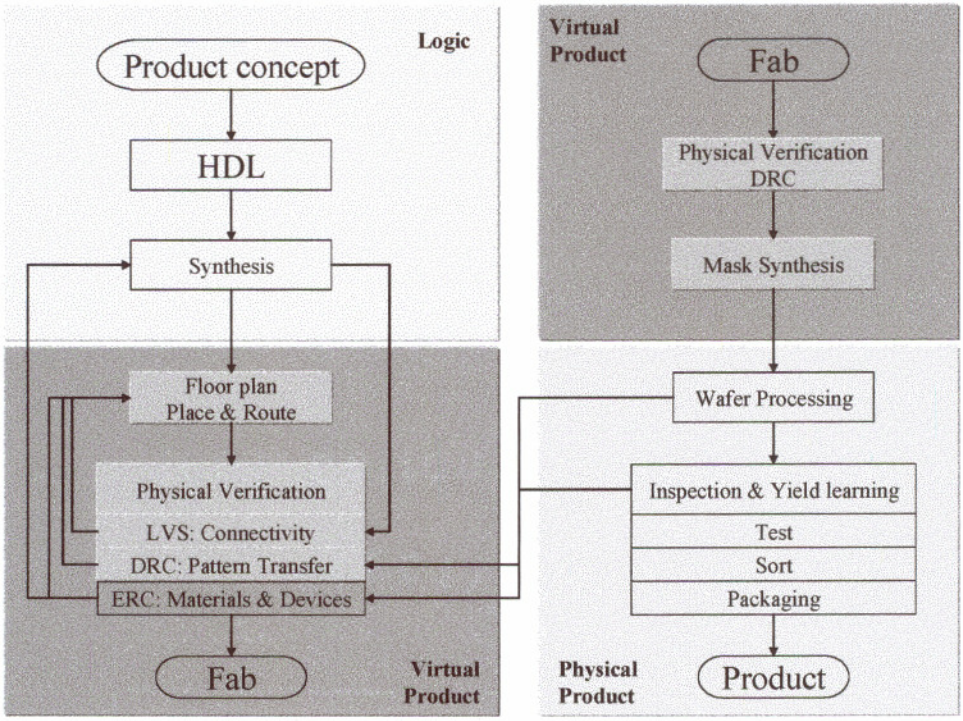


Figure 5. Typical IC-design flow.

The first step involves a layout Vs schematic (LVS) check in which primarily connectivity and consistency between the logic and the physical objects are compared. A second verification, commonly known as Design Rule Check (DRC), is used mainly to address pattern transfer and pattern integration issues during manufacturing. Finally, an Electrical Rule Check (ERC) evaluates the electrical behavior of devices in the context of the product by performing a thorough characterization of the process. Especially important are effects such as resistance, capacitance and inductance, which are specific to the final topology and material selection.

The product remains in a virtual state while transferred from the design teams to the fabrication facilities (Fab). After the information arrives at the Fab, it is checked again for pattern transfer-related issues. Mask synthesis operations are used to further modify the layout to make it more manufacturable by using Resolution Enhancement Technologies (RET), fill for planarization and data fracturing for mask production. The mask synthesis must be done for each level in the virtual product.

When there are no further modifications to the virtual product, actual manufacturing can proceed. It is at this point that the product takes its final physical form, so it can be inspected, tested, sorted and packaged

for distribution. It is also at this stage that the process groups can learn about the problematic topologies or configurations that present a challenge for manufacture, and learn more about the actual performance of the materials being used. Newly acquired data is gathered, and ERC and DRC rules are constantly updated to represent the present state of the process.

As of today, multiple companies have tools to efficiently perform a typical design flow. If this is the case, why is there a sudden need to talk about DFM? In 1999, Weiler[14] and Schellenberg[15] expressed the need to integrate existing design and manufacturing tools into a single flow that could provide the basis for a DFM system, but five years later little has been done in the realm of DFM.

The main impediments to DFM progress in the industry were the advent and subsequent success of RET. RET operations started to gain momentum in 1999 and were widely used, allowing the current infrastructure to remain almost unaltered. Only the mask synthesis operation had to undergo a fundamental transformation. Although prior to sub-wavelength, simple Boolean operations, rotations and fracturing were required to manufacture a successful mask, a complete series of more radical modifications was necessary to guarantee an adequate pattern fidelity. The success of RET and the difficulty of achieving continuous and seamless communication between production and design teams have encouraged IC and EDA companies to focus their resources on RET activities while accomplishing little in the area of DFM. When performed properly, DFM refers to the action of making modifications to the "target" design; by contrast, RET makes modifications to the design so that it can meet the given "target".

Now that the effectiveness of the RET is diminishing with each successive process node, it is clear that true DFM activities need to be studied and evaluated. The hardware used for production is reaching its resolution limits, and layout sensitivities to process variations account for a large (although not yet well defined) contribution to yield-loss.

One of the challenges for a successful implementation of DFM is the lack of a framework to guide it. The large number of experiments needed to quantify the manufacturability of a design, by using simple extensions to traditional verification and correction methods, makes such an approach impractical. The point of having a framework is to provide a predefined set of guidelines for integrating the available knowledge into a consistent and compact formulation that can be used to compensate for manufacturing variations. This means that the framework has to provide a mechanism to detect and rank manufacturability problems in a design, and also to guide the correction process. In addition, such a framework must alter the existing design flow as little as possible to qualify for widespread adoption, which is one of the main reasons RET has become ubiquitous.

At present, there are groups who believe that it will be possible to improve process corner modeling of devices by massive electrical characterizations, thus achieving a more robust design[16] at logic synthesis. Although these methods have clear applications in interconnect delays and timing closure, they fail to

provide information about forbidden topologies that cannot be characterized adequately due to their high sensitivity to process variations. By approaching DFM from the standpoint of pattern robustness, and by making the layout less sensitive to process variations, these methods can be relevant when trying to explain the material aspects and electrical behavior of devices without having to explain pattern transfer effects that cannot be captured effectively in traditional electrical models. For this reason, such approaches are considered complementary to this pattern transfer-centric proposal for DFM rather than competing.

The following sections evaluate the advantages and challenges for each of the leading techniques being explored to improve pattern manufacturability. Although many of these techniques are currently being evaluated for post-RET verification, in principle they could be used within a design environment to allow the designer to dictate the topology changes required to make the design more manufacturable.

1.2.1 Critical Area Analysis

Because random (particle-induced) defects were the dominant yield-loss mechanism for most mature process above 180nm, a method that could allow yield predictions in the presence of particles had to be developed. Critical Area Analysis combines empirically determined defect distributions with target layout geometries. Such an approach has been so successful that is routinely used in the semiconductor industry, and it continues to be an open area of investigation.[17] However, Critical Area Analysis alone is not sufficient to produce an adequate yield estimate in the sub-wavelength regime.

In 2004, Asami[18] and co-authors presented a methodology on how critical area can be used successfully to predict yield-loss for an 180nm process under a wide variety of product conditions.

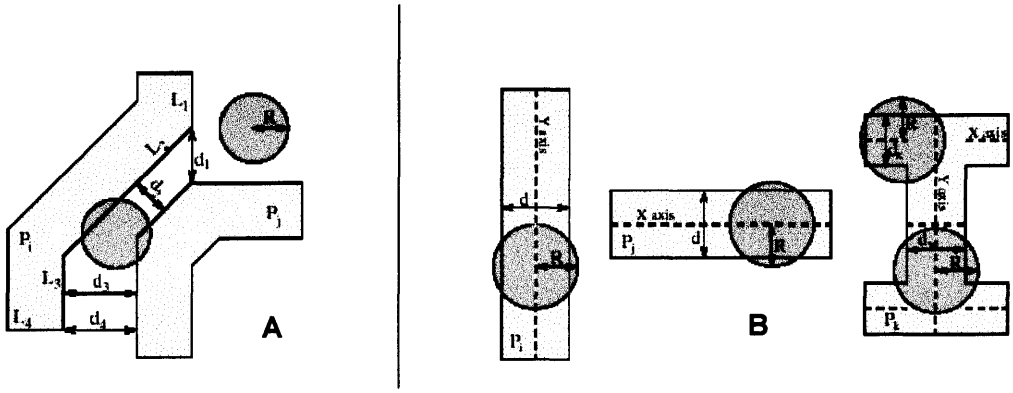


Figure 6. Critical area calculation depicting short (A) and open (B) defects.[17]

Critical area (A_c) is a function defined for a particle defect size of equivalent radius (r), as equation 1 suggests:

$$F(R) = \sum_{layers} \sum_{r=0}^{R} P_d(r) \cdot A_c(r) \qquad 1$$

Critical area along a defect density function typically defines a failure factor F(R), which as expected depends on the equivalent radius of defect particle size. The continued success of critical area methods is based on the extension of the "particle" concept to formulate failure rates originated by random defects independent of their physical origin. These formulae are constantly being used to explain non-particle (as in "non-physical particle", such as dust) failure mechanisms (e.g., resist collapse, resist bridging or pinching and metal stress). The use of critical area formulae is possible when clear failure mechanisms and their respective failure rates can be clearly characterized by continuous sampling during manufacturing.

However, critical area analysis has two main drawbacks. It is incapable of early yield assessment for new processes, and it lacks the mathematical machinery to incorporate systematic defects. Although critical area can, on average, provide a good estimate of the expected yield of a product, the analysis can be performed only after enough data has been gathered during manufacturing. Critical area alone cannot predict the yield of an IC product before going into a new process. Only by using massive amounts of historical information can this method predict expected yields.

The second limitation results from the use of empirical models, which depend on short-range effects. For supra-wavelength processes, it is possible to use only space and width measurements to define critical area. As the resolution of the systems approaches the domain of deep sub-wavelength (below 1/2 wavelength), however, larger regions of layout context are needed to adequately capture high-sensitivity regions.

While Critical Area Analysis alone cannot be used to produce accurate yield estimations in the sub-wavelength regime, it may be possible to combine it with systematic and parametric yield-loss estimators in order to arrive to a more comprehensive and accurate yield prediction.

1.2.2 Improve Contrast Method

Because lithography is one of the most critical drivers for systematic yield-loss due to the sub-wavelength gap (Figure 2A), and image contrast has long been used as a criterion for image robustness,[19] it is not surprising that many DFM groups have tried to use contrast as a metric for evaluating the robustness of a given layout.[20,21,22]

Among the advantages of improving image contrast is the control of line-end roughness[23] and traditional lithographic process windows (larger depth of focus and exposure latitude). However, because image contrast remains an optical quantity (albeit with known positive effects in resist- and mask-induced errors), it cannot be extended to incorporate other process effects such as etch, chemical metal polish or overlay.

In addition, as Figure 7 suggests, it is not trivial to maximize image contrast for multiple layers concurrently. The authors of this figure restricted their analysis to the polysilicon layer, and offered little explanation for the effect that such changes had on the manufacturability of other layers present in the design.

Another consideration is that an image contrast can capture only major sensitivities in the design and does not directly translate into actual CD control because most chemically amplified resists perform in a non-linear fashion. Knowing the impact or variations in CD is one of the critical challenges that analog design faces[24] and that cannot be reliably addressed with this method.

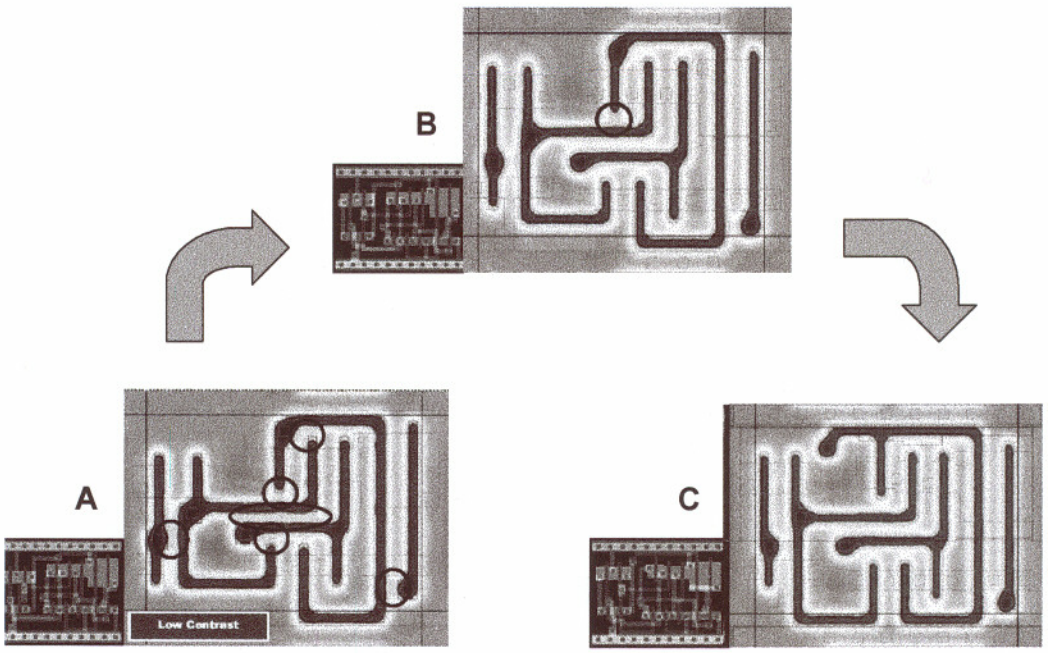


Figure 7. Example of contrast-based driven DFM optimization for a 130nm standard cell.[22] Original layout (A), intermediate layout (B) and optimal layout (C).

Based on this discussion, we can identify immediately the range of applications for these methods: primarily digital design and single-layer applications. This is one of the fastest model-based methods, since it might require single optical simulations to produce a good estimate of the image quality across process window conditions. This is a very desirable characteristic of any model-based DFM method, as will be highlighted later in this work.

1.2.3 Reduce Mask Error Enhancement Factor (MEEF)

One of the first metrics that relies on sensitivity of the layout is MEEF (Mask Error Enhancement Factor). MEEF is defined as the change in the width of a feature (CD_{wafer}) from the change in the width of the feature in the mask (CD_{mask}), divided by the image reduction factor (M), which typically is 4X. MEEF is expressed in equation 2.

$$MEEF = \frac{\partial\left(CD_{wafer}\right)}{\partial\left(\frac{CD_{mask}}{M}\right)} \qquad 2$$

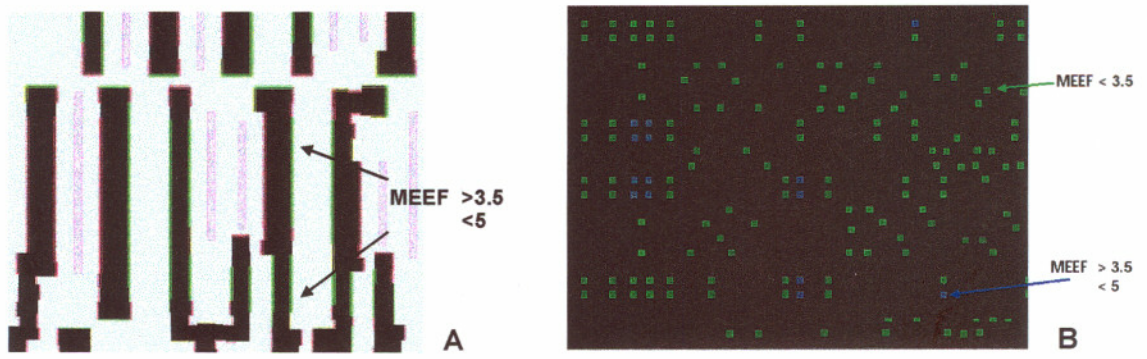


Figure 8. High-sensitivity feature detection:[25] typical poly layer (A) and typical contact array (B).

While critical area and image contrast methods rely on a single-pass calculation, MEEF is a perturbation quantity. To be adequately calculated, the features on the mask need to be biased prior to measuring the induced CD on the wafer in order to make it possible to obtain the corresponding MEEF value. Even with this apparent limitation, this metric is now proposed for use as a post-RET verification.[25]

MEEF is well suited for post-RET verification because the RET objective is to bring all features as close as possible to the target design. But there is an assumption that the mask can be perfectly manufactured. By using MEEF as an additional metric, it is possible to highlight locations in the mask that will be more susceptible to CD error induced by imperfect masks.

Although this metric incorporates a relative measure of a process-induced CD variation (the process of making the mask), it also remains primarily optical in nature. In addition, MEEF remains a fairly one-dimensional metric because CD is not well defined in corners and in low-aspect-ratio features in general. Especially for sub-wavelength features, in which high-frequency objects (such as corners or dense structures) are not well captured by the optical system and other pattern transfer effects start to become important, it is necessary to adopt a more general definition for CD variation and control. It is also interesting to note that, aside from critical area analysis, all the present proposals for a pattern transfer DFM system have been developed by RET and lithography groups trying, in one way or another, to detect the locations most likely to fail in a layer.

1.2.4 Critical Failure Optical Rule Check (CFORC)

A recent methodology to detect probable failure points in the design also depends on optical image quantities. This technique, called Critical Failure Optical Rule Check (CFORC),[26] maps out the failure and

non-failure regions across the process window. Figure 9 shows a process envelope (or boundary) separating process regions that will print reliably from those that will not.

This failure model is calibrated by empirical binary data in which a feature either does or does not print. This is different from traditional process model calibrations, in which many CD values are captured for any given feature, and locations that cannot be measured reliably are removed during calibration.

This model relies on an empirical mapping between image parameters (such as minimum and maximum intensities and a two-dimensional image parameter, shown as **Factor** in Figure 9) and the printability or non-printability of the design. Therefore, it offers the advantage that a single optical simulation is able to detect regions most likely to fail across process window conditions. However, the speed of the calculation is improved by trading a physical model for an empirical model that lacks predictive power outside the domain used for calibration, making this method very sensitive to process space sampling resulting from the test features included for calibration.

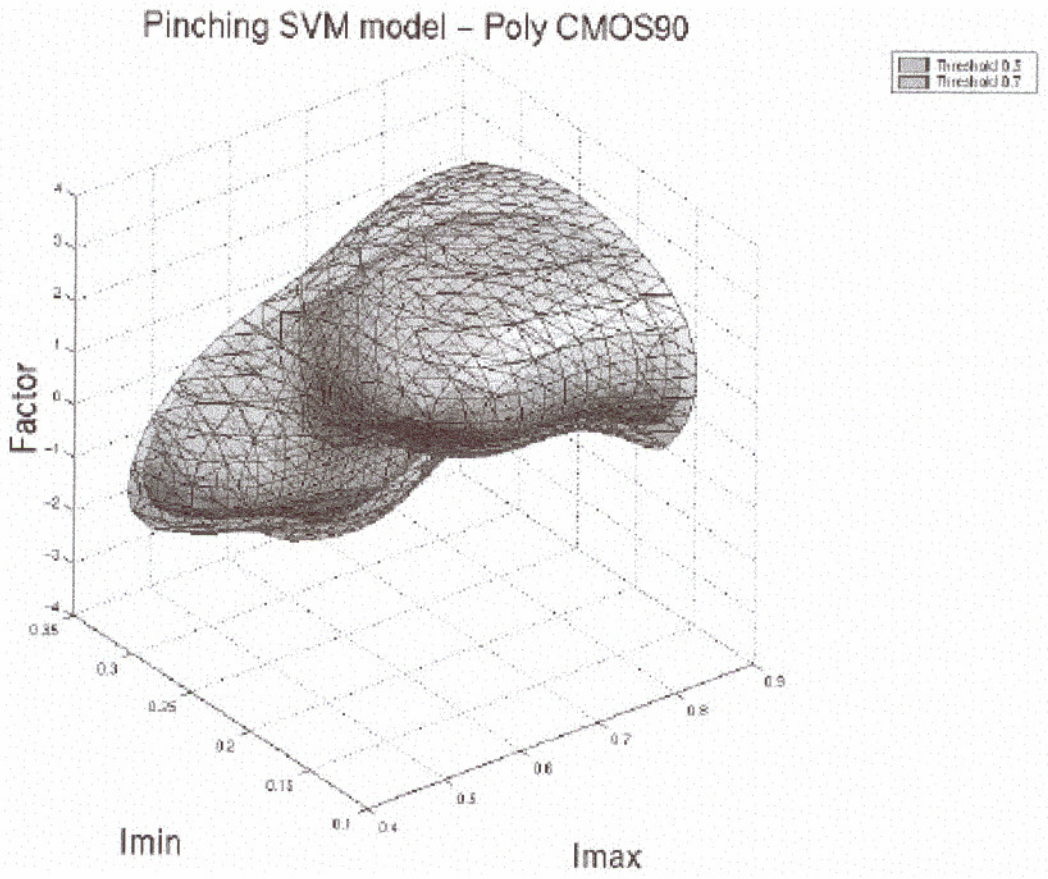


Figure 9. Pinch-failure model for a 90nm process.[26] The surface indicates the boundary between failure and robust printing.

1.2.5 Restrictive Design Rules (RDR)

Although all the previous techniques can detect and highlight regions in the layout that will most likely create problems during manufacturing, they do not directly address or forbid specific layout topologies. One approach widely supported by lithography groups is the use of restricted design rules (RDR).[27,28,29] This approach is guided by the general principle that homogenous structures with well defined frequencies can be manufactured more easily than objects that are highly bi-dimensional.

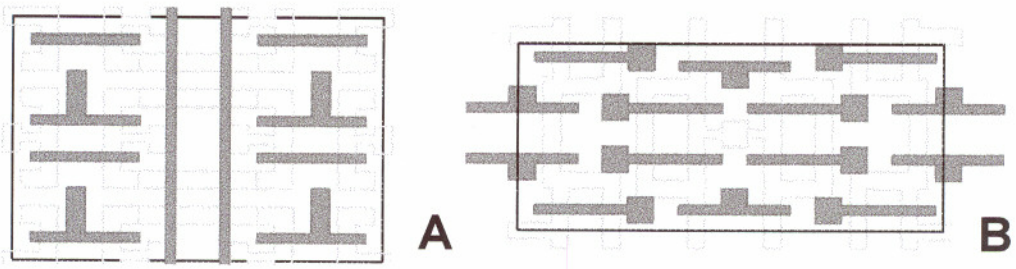


Figure 10. Example of restricted design rules.[27] Polysilicon layer for a typical (A) and a more manufacturable (B) SRAM cell.

Liebman (2003) establishes the following principles for a more manufacturable layout:

- Limited number of narrow line widths....
- Single orientation of narrow features....
- Narrow features placed on uniform and coarse pitch....
- Uniform proximity environment for all critical gates....
- Limited number of pitches for critical gates.[27]

Traditionally, designers do not receive such restrictive rules well because they appear to require much larger design areas. Since area, timing and power are the three main quantities for which designers are responsible, having restricted design rules affecting any of these three criteria results in an unwelcoming response. However, a multitude of investigations suggests that the area penalty incurred by aggressive design rules is not as large as expected[20,29] when the designer and the lithography groups work together toward a solution that includes pattern transfer manufacturability as a new target metric.

Unfortunately, the use of restrictive design rules has not been adopted widely because there is no systematic method in which the layout can be analyzed and ranked according to manufacturability. All other design objectives have clear procedures and figures of merit: timing (maximum clock frequency, which defines the performance of the devices), power (wattage, which with mobile applications improves

battery life) and area (square microns that translate into more product per wafer, thus reducing price). But until now, there has been no metric that relates early enough in the process to product yield or reliability.

Although most RDR guidelines are adequate in general, they still require the layout designer to have a good understanding of the process being used for manufacture, or at the very least a strong interaction between the layout designer and RET experts who are able to determine what a "uniform proximity environment" really means.

As is apparent by now, different groups along the IC production chain use various approaches for improving their methods to better and more economically produce aggressive designs. The objective of this framework is to build on the strengths and bypass the weaknesses inherent in all current pattern transfer DFM proposals. While many of the individual building blocks used in this proposal already exist, it is the integration of these tools into a formal and logical pattern transfer DFM framework that is lacking.

The following sections describe this framework and test the details of its implementation to achieve designs less sensitive to process variations. Although the primary objective of the framework is the development of more robust layouts, the last section of this work also evaluates the impact that more robust structures have on the electrical behavior of the devices.

2 Proposal for an IC-DFM Framework

This work presents a proposal for a software framework aimed at improving the manufacturability of a given layout. The framework is not restricted to problems that occur during lithography, but rather to the availability of an adequate compact model. The framework is illustrated by using a lithography process as an example because accurate and compact process models exist for lithographic processes. The framework comprises three main components:

- **Objects:** Elements that capture design intent and process conditions. The two main objects are the original layout, which depicts the physical representation of the circuit, and the process variability bands (pv-Band), which reflect the sensitivity to the manufacturing process.
- **Operators:** Operations that can be performed on the objects to select or extract quantitative information. While the original layout and the pv-Bands are passive components of the framework, the operators are active components that exploit the properties of the pv-Bands and the layout. These operators, not unlike traditional Boolean, distance and area modifiers, allow the expression of manufacturing violations or marginalities and a scoring system.
- **Guidelines:** Recommendations for integrating the objects and operators consistently. By combining a scoring system with a method of detecting local errors, two different manufacturing indices can be defined: one that describes the process and another that describes the design. The combination of the scoring method and the error detection has multiple applications: RET selection, litho-friendly design and model-based design checks. In this work, such applications are not specifically described, but the general concepts of error detection (Section 2.3.1) and design scoring (Section 2.3.2) are explained in depth.

As with any new proposal, this DFM method is open to extensions and enhancements as more information about the interactions between process and design is identified. To maintain its consistency and usefulness, however, only the addition of elements that fall into one of the three previously defined categories is desirable.

This proposal is based on the assumption that fast manufacturing models are available. Although pattern transfer depends on the interaction of lithography, etch and planarization, this work uses compact lithography models[30,31] to illustrate the proposed methodology. The reasoning is that fast process window lithography models have been previously calibrated[32,33] and shown to reproduce lithography effects with an accuracy level comparable to that of experimental metrology.

Although only lithography effects are explored in the following pages, it must be clear that as new process models are made available for other pattern transfer effects, they can be incorporated into the proposed formulation. This can be achieved because the manufacturability object described in the following section is nothing more than the pattern variability response to a process variable.

The nature of the process variation is relevant only with respect to the actual calculation of the manufacturability object. The number and type of process variations affect the framework only by requiring additional computing time during the calculation of the manufacturability object. The analysis methods described by the framework remain constant and applicable.

2.1 Framework Objects: Layout and pv-Bands

Any proposal for a DFM methodology must incorporate design and manufacturing components, or objects that describe the interactions between design and manufacturing. For that reason, this work proposes two objects: one that describes the design and another that describes the process/design interactions.

- **Design object:** This is the physical layout residing in the design environment. This condition is necessary for two reasons: the final layout is the only object that has enough information about the intended topology, and any correction to the layout topology must be re-evaluated electrically. Otherwise, it might be possible to achieve a highly manufacturable grid structure with zero functional contribution.
- **Manufacturing object:** This work proposes the concept of process variability bands (pv-Bands). A pv-Band is defined as the physical representation of the layout sensitivity to process variations, and it is represented as an additional design layer in the design database.

One way to calculate a pv-Band is to compute the pattern transfer at multiple process conditions, and then perform a series of Boolean operations to extract the maximum and minimum edge displacement, as indicated in Figure 11. pv-Bands can be easily expressed as additional polygon layers in layout formats such as GL1, GDSII or OASIS.

Although existing layout formats can describe wafer plane structures well, these formats require extensions to support information related to the feature thickness. However, this is a limitation of the current layout formats, because a pv-Band can be defined in the vertical direction, in which the band represents the thickness variation rather than width variations.

It is clear that an intelligent sampling method of all possible process conditions should be considered, as well as an adequate description of the processes under study (for example, the choice of RET in lithography, or the statistical variation in etch biases due to wafer processing).

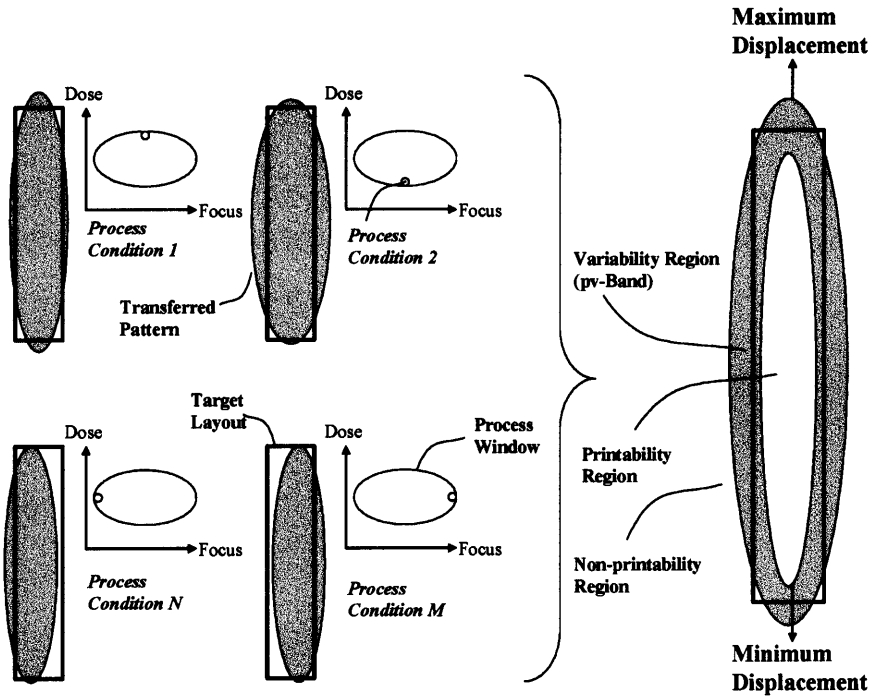


Figure 11. pv-Band calculation. At every point within the process window, a pattern transfer image is calculated. The region inside the pv-Band corresponds to the constantly printing region, and the band itself (gray) corresponds to the variability region that indicates probable locations of the boundary between printing and non-printing.

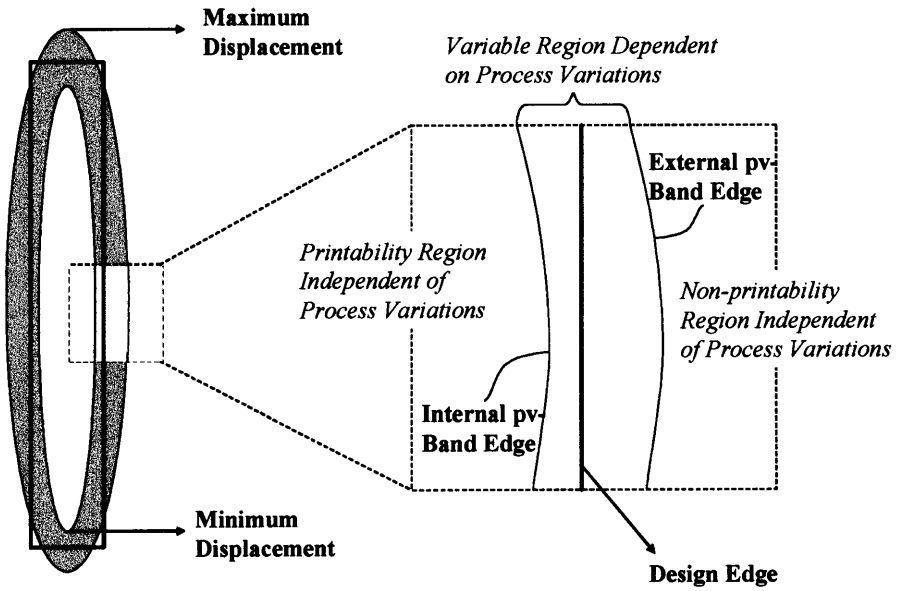


Figure 12. pv-Band elements. The internal pv-Band edge is the boundary between the printability and variable regions. The external pv-Band edge is the boundary between the variable and non-probability regions.

As Figure 12 suggests, the pv-Band is an uncertainty region between areas that will always print and areas that will never print, thus providing a mechanism to assess the likelihood of a particular topology transfer. In other words, the smaller the pv-Band, the higher the probability of correct pattern transfer. Although Figure 12 shows energy dose and image defocus (typical lithographic process control variables), any process variation can be incorporated because it will introduce its own printability signature as long as a well calibrated, physical model is available.

These simple objects have intrinsic properties that provide the basis of this framework. The pv-Bands can be made small in one of the following ways: very good process control, a more advanced process or a more robust design. In addition, pv-Bands can be calculated for any layer or process and, when combined, account for inter-layer variations. For example, when a landing pad and contact variability bands overlap, the likelihood of an improper connection increases; when polysilicon and diffusion layer variability bands overlap, the likelihood of a short circuit increases.

Each effect can be weighed according to its importance. A variability that produces a short or bridge should account for a larger contribution than the same variability in another region that does not cause a fatal defect. And because these highly process-sensitive regions are local in nature, they provide intra-die variation information.

Because process variability can be reduced over time, the same formulation can be used for processes under development (when the uncertainty is higher) and for mature processes (when the uncertainty is well controlled but not completely eliminated), thus providing a consistent evolutionary path. Although all these are qualitative benefits of using a pv-Band formulation, the framework also provides a mechanism for ranking designs and manufacture processes in a quantitative way.

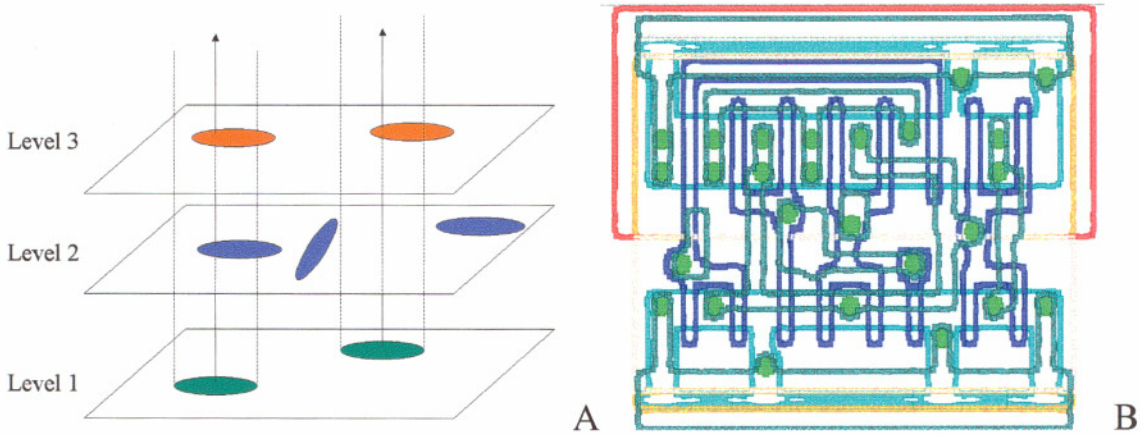


Figure 13. This design comprises several layers, and the final composite sensitivity is a weighted combination of all individual sensitivities along the connectivity line-of-sight and the unconnected line-of-sight. A shows the concept, and B shows the actual implementation in a 130nm cell.

Another novelty of this approach is that sensitivities are calculated across multiple layers because the manufacturability of the design depends on the interaction of the pv-Bands. A composite map can be created to account for all the manufacturability sensitivities and highlight regions that have worse or better pattern robustness for a certain process, as indicated in Figure 13. The information contained in the pv-Bands can be efficiently displayed and processed during design, thanks to advances in layout data representation/compression.[34]

2.2 Operators

Having an object to work with is only the first step. At this point, it is necessary to define a series of operators that act on the objects. These operators are software functions and procedures. Some of the proposed operators are already available in most physical verification commercial tools (such as Calibre, Hercules and Dracula) and they include Boolean OR, AND and NOT operations. However, there are also new operations because they depend on the properties of a pv-Band (e.g., E2I, E2E and I2I). Table 1 lists and describes each operator in what is believed to be the complete set required for the proposed framework.

Operator	**Description**
PVBAND(*Layer*)	Calculates the process variability band of *Layer* and creates a *pvBand* object.
E2I($pvBand_i$, $pvBand_j$)	Measures the distance between the external $pvBand_i$ edge and the internal $pvBand_j$ edge and creates a marker layer that completely encloses the selected region.
E2E($pvBand_i$, $pvBand_j$)	Measures the distance between the external $pvBand_i$ edge and the external $pvBand_j$ edge and creates a marker layer that completely encloses the selected region.
I2I($pvBand_i$, $pvBand_j$)	Measures the distance between the internal $pvBand_i$ edge and the internal $pvBand_j$ edge and creates a marker layer that completely encloses the selected region.
OR($Object_i$... $Object_j$)	Boolean operation that adds all the contents of $Object_i$ through $Object_j$ to create a derived layer. *Object* can be an original or derived *Layer* or *pvBand*.
AND($Object_i$... $Object_j$)	Boolean operation that adds the common contents of $Object_i$ through $Object_j$ to create a derived layer. *Object* can be an original or derived *Layer* or *pvBand*.

NOT(*Object*$_i$, *Object*$_j$)	Boolean operation that discounts the common contents of *Object*$_i$ and *Object*$_j$ from *Object*$_i$ to create a derived layer. *Object* can be an original or derived *Layer* or *pvBand*.
AREA(*Object*)	Calculates the area of the *Object*. *Object* can be an original or derived *Layer* or *pvBand*.

Table 1. Description of framework operators.

2.3 Guidelines

After manufacturability objects and operators are defined, the framework requires a series of guidelines on integrating and using them effectively. These guidelines comprise the best practices for exploiting the properties of the pv-Bands to improve the robustness of process variations of the design layout. But before describing the guidelines, it is necessary to describe the system itself.

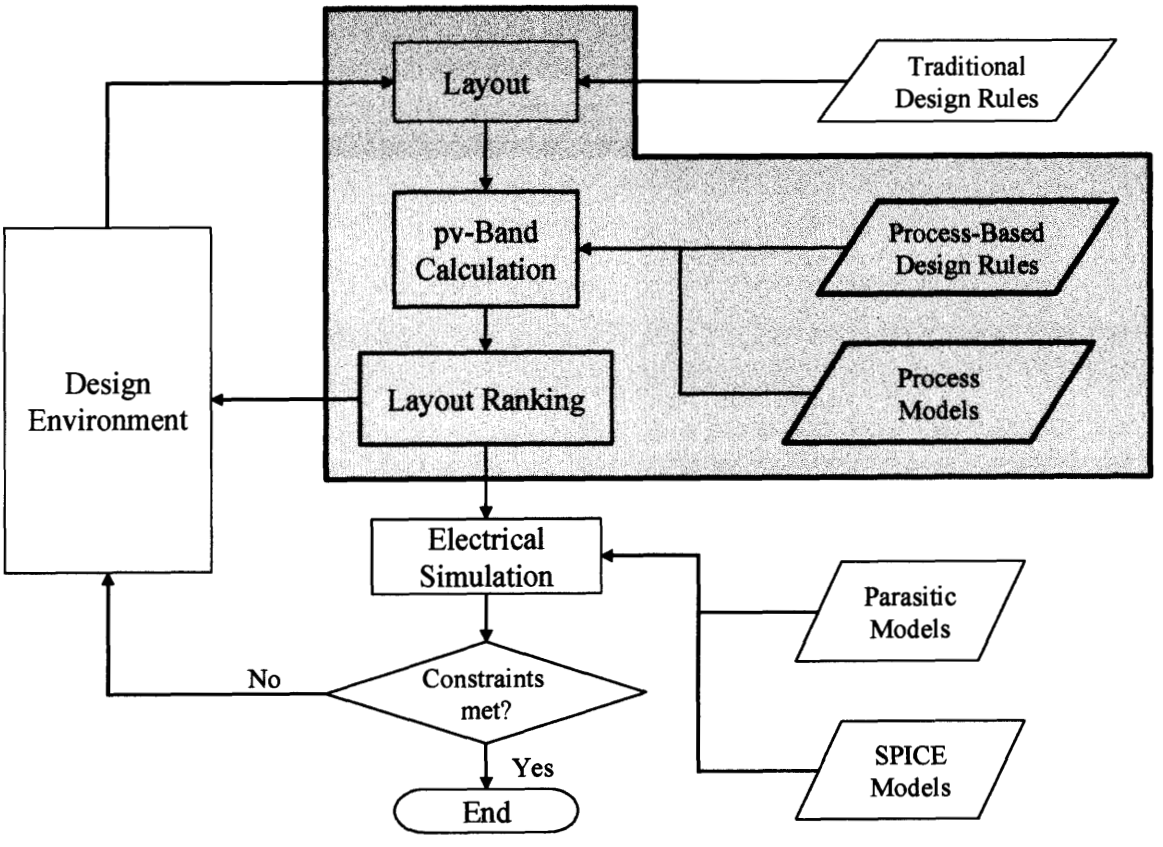


Figure 14. Enhanced design flow using the methodology proposed in this work.

Figure 14 shows (in gray) how the new design components can be incorporated into a traditional design flow with minimal impact on existing design methodologies, thus defining the natural insertion points of this methodology within the existing IC design process.

Because this method determines whether the layout is likely to fail, it should primarily be used prior to electrical simulations, as shown in Figure 14. Only after the layout can be reliably manufactured does it make sense to proceed with its electrical analysis.

Each of the new or modified operations needs to comply with new requirements.

1. **Layout:** The layout should be large enough to address the areas of influence imposed by the process, since pattern transfer effects are highly dependent on the surrounding topology.

2. **Process models:** These models should reliably identify the maximum and minimum pattern responses within the process variations. In the absence of a single model that can explain all process variations, they should limit prediction to specific and well defined effects.[33] In this way, a composite pv-Band can be used to identify regions that present maximum variability across many process effects and retain information on the largest contributor to the pattern variation.

3. **Process-based design rules:** These rules define the design violations and help to identify regions that are most sensitive. The results are used to flag regions of maximum variability and extract a quantitative metric to manufacturability.

4. **pv-Band calculation:** This calculation uses the process models in conjunction with the process-based design rules.

5. **Layout ranking:** Before proceeding with electrical simulations, this layout-ranking metric serves as a design manufacturability target. Even when the process-based design rules do not return errors, it is possible to look at a continuous metric that provides additional opportunities for improvement.

6. **Correction (inside the design environment):** The correction resides in the design environment and requires a different interpretation of the results provided by the process-based design rules. While typical design-rule violations can be fixed by topological changes (e.g., compacting features) or morphological changes (e.g., clipping corners), these rules will generally require a topological change.

After such a system has been put in place, it depends on the specific application and the actual mode of operation. However, in all cases the following guidelines will apply.

- **Manufacturing checks:** Provide a mechanism for filtering regions where the variability creates a problem from regions where the variability does not affect the function of the device. These can be intra or inter layer, and in general are expressed as inequalities.
- **Ranking system:** Provides a metric to score the manufacturability of the layout and indicate the likelihood of attaining high yields. Two indices result from the basis of the scoring system: a Process Manufacturability Index and a Design Manufacturability Index.
- **Area of influence:** Describes the minimum area needed to obtain reasonable results.
- **Simulation requirements:** Since the framework is based on process simulations, there are special requirements for the models to be used in this framework.

2.3.1 Manufacturing Rule Checks

RDR makes a design more manufacturable by aggressively restricting the types of topologies allowed in a design,[35,36] but it relies heavily on past experience and on the assumption of the existence of a geometric representation of the restricted rule. One possible way to enhance RDR is by using process-based design rules,[37] which are derived from the actual simulation of the layout.

This method derives process-based design rules from pv-Bands rather than from nominal distortions and shape analysis.[37] A pattern manufacturability rule is constructed by performing Boolean and spacing checks of the pv-Bands. In this fashion, a typical set of design rules[38,39] can be translated into new design rules based on pv-Bands.

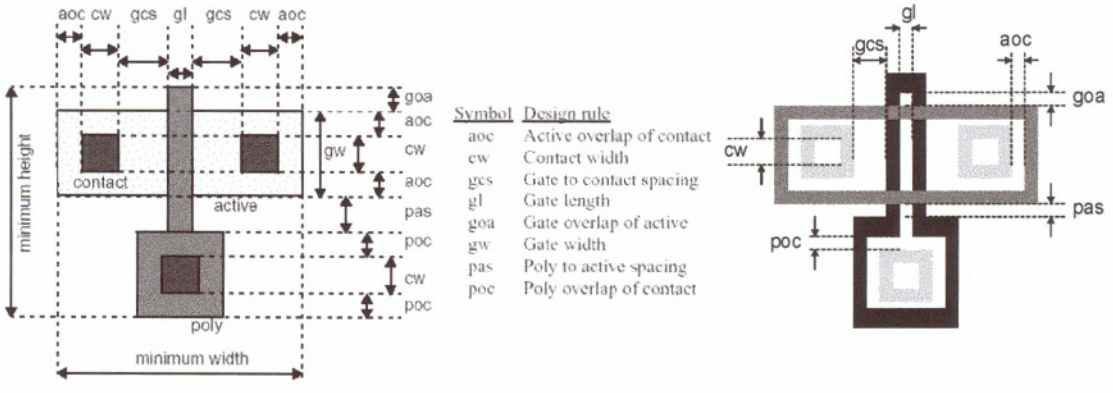


Figure 15. Typical design rules[38] (left) versus pv-Band-based design rules (right).

Figure 15 shows a simple example of target geometry (left) and a schematic representation of the pv-Bands (right) for three layers: poly, active and contact. For a perfectly modeled process, the rules can be as simple as identifying the respective pv-Band overlaps. However, a more general description specifies rule tolerances that serve as an additional safety margin or depend on electrical rules.

The rules depicted in Figure 15 can now be formally expressed as a collection of equations that use the previously defined operators and objects, and each of the traditional pattern-related design rules can be tied to its original intention. Not all design rules are included in this formulation. For example, all the electrical design rules are not incorporated because they depend on the material aspects of manufacture.

$$aoc_{Violation} = OR\begin{pmatrix} AND((pvBand(contact), pvBand(active))), \\ E2I(pvBand(contact), pvBand(active)) \le aoc_{\min} \end{pmatrix} \quad 3$$

$$cw_{Violation} = OR\begin{pmatrix} AND(pvBand(contact)), \\ I2I(pvBand(contact)) \le cw_{\min} \end{pmatrix} \quad 4$$

$$gcs_{Violation} = OR\begin{pmatrix} AND((pvBand(poly), pvBand(contact))), \\ E2E(pvBand(poly), pvBand(contact)) \le gcs_{\min} \end{pmatrix} \quad 5$$

$$goa_{Violation} = OR\begin{pmatrix} AND((pvBand(poly), pvBand(contact)), endCap), \\ E2I(pvBand(active), pvBand(poly)) \le goa_{\min} \end{pmatrix} \quad 6$$

$$gw_{Violation} = OR\begin{pmatrix} AND(pvBand(poly)), \\ I2I(pvBand(poly)) \le gw_{\min} \end{pmatrix} \quad 7$$

$$pas_{Violation} = OR\begin{pmatrix} AND((pvBand(active), pvBand(poly))), \\ E2E(pvBand(active), pvBand(poly)) \le pas_{\min} \end{pmatrix} \quad 8$$

$$poc_{Violation} = OR\begin{pmatrix} AND((pvBand(contact), pvBand(poly))), \\ E2I(pvBand(contact), pvBand(poly)) \le poc_{\min} \end{pmatrix} \quad 9$$

2.3.1.1 Critical Area Identification: Intra Layer

The AND operator can be applied to single layers since each of the pv-Bands are generated per edge. The AND operation can also serve as an explicit pv-Band overlap detection. This simplifies the rule writing and avoids the unnecessary definition of positive or negative distances. The second part of the equations relates to inequalities used to defined margins that incorporate limitations of the process model, or electrically-justified design rules.

One of the main advantages of this work is the ability to describe multiple types of violations. Other methods, such as CFORC, can account only for the catastrophic events that happen within a single layer, such as bridging and pinching. Notice how such situations are accounted for in this work by simple space and width checks.

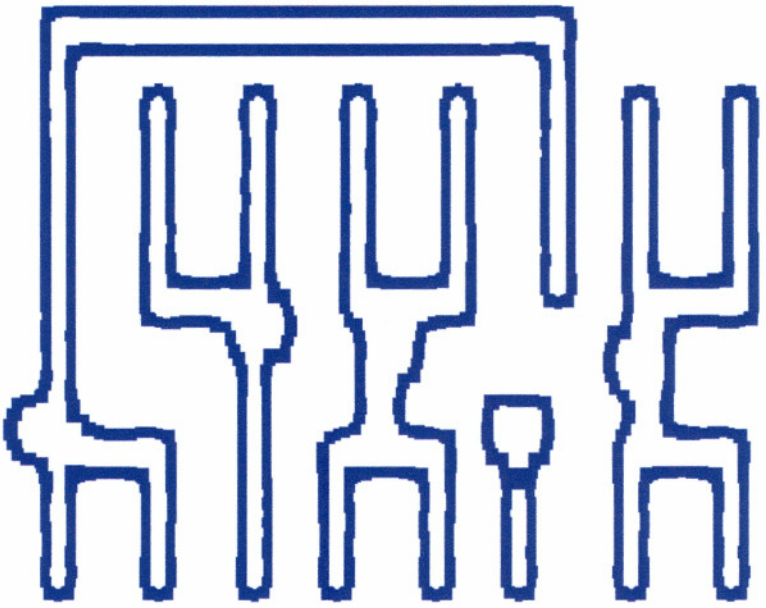


Figure 16. Single-layer pv-Band interaction. The internal and external distances of the pv-Bands determine the pass-fail criterion.

2.3.1.2 Critical Area Identification: Inter Layer

By using the operators described in Table 1, it is possible to identify a particular type of failure mechanism. This is the case of the *goa* design rule (equation **6**), in which an *endCap* failure is detected by the overlap of polysilicon (poly) and active pv-Bands, as depicted in Figure 17.

The support region includes the drawn line-end, plus the area defined by the boundaries of the external edges of the polysilicon pv-Band. While support regions are useful in single layer, they become essential for most inter-layer design rules.

One of the advantages of using models to detect critical regions is highlighted with the following example. When line-ends fail (Figure 17A) due to pv-Band overlap, a typical correction extends the line-end (Figure 17B). But as Figure 18 suggests, there might be other configurations in which a line-end extension is not required (Figure 18A), and forcing such an extension can result in another type of violation, such as a polysilicon bridge (Figure 18B)

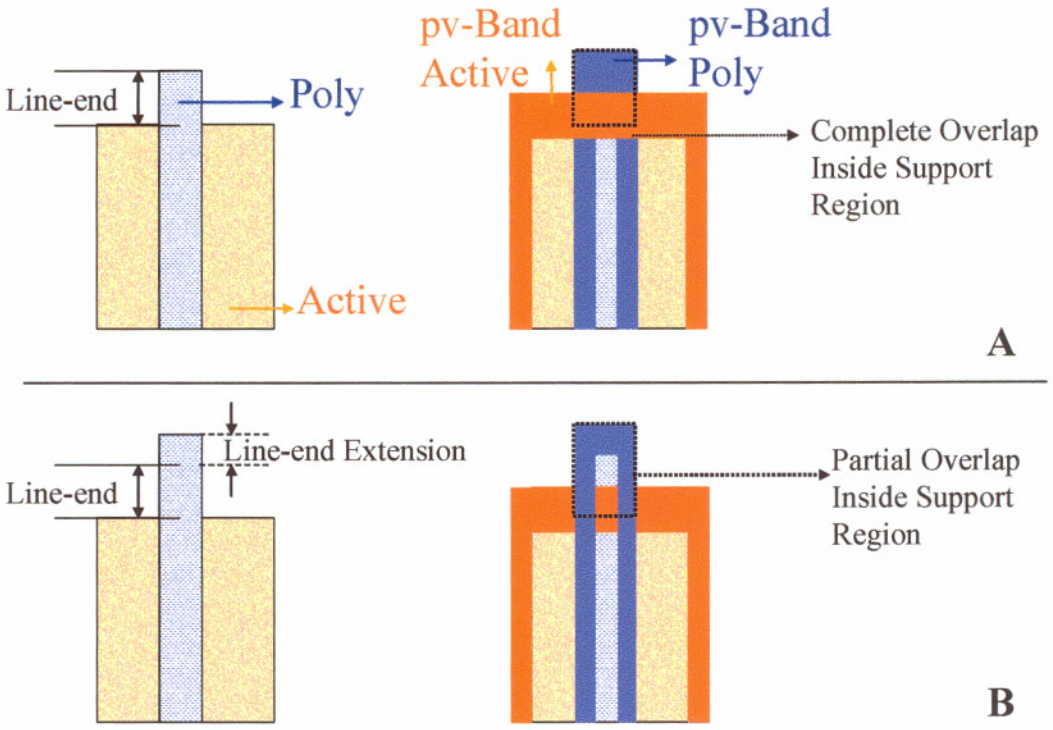


Figure 17. Two-layer pv-Band interaction. The enclosure rules are determined by incomplete overlap existence.

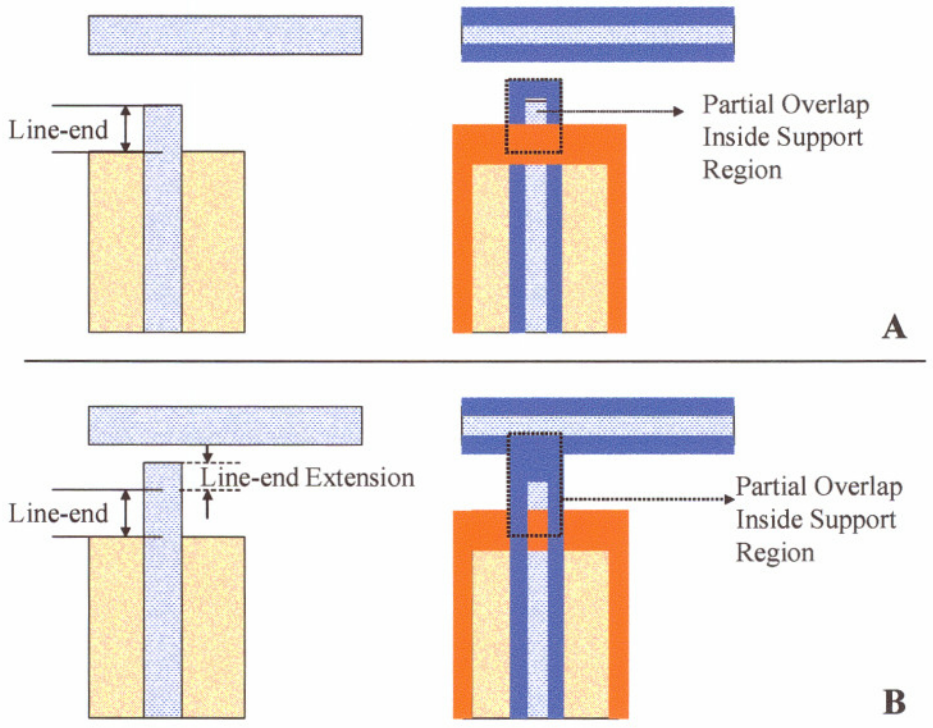


Figure 18. Two-layer pv-Band interaction. Different topology environment.

2.3.2 Ranking System: Manufacturability Indices

Although manufacturing checks are useful for highlighting regions prone to failure in the design, thus far there is no mechanism to assess the viability of the layout from the manufacturing point of view.

Introducing manufacturability indices, by defining a process manufacturability index and a design manufacturability index, solves the problem that results when two layouts with clean design rules return different pattern manufacturability behavior.

The process manufacturability index (PMI) is related to the average difficulty of image transfer for a given design. The design manufacturability index (DMI) is related to the number of locations in a layout that are sensitive to a given process.

By definition, PMI is a global metric and does not provide specific information about the failure locations in the design. However, this apparent shortcoming makes it ideal for qualifying the process capabilities or the global behavior of a complete layer. In its simplest form, the PMI can be expressed as follows:

$$PMI = \sum_{layer} \frac{AREA(pvBand(layer))}{AREA(layer)} + \sum_{layer_i, layer_j} \frac{AREA(AND(pvBand(layer_i), pvBand(layer_j)))}{AREA(AND(layer_i, layer_j))} \quad \mathbf{10}$$

In addition, we can define DMI that primarily serve to highlight the regions most likely to fail in the design. The desirable number in this case is zero.

$$DMI = \sum \frac{AREA(DesignRule\ Violations)}{AREA(SupportLayer)} \quad \mathbf{11}$$

In equation **11**, design rule violations result from the manufacturing checks, and the support layer is used to normalize the errors with respect to the area of interest.

The design rule violation concept can be enhanced by including only defects that occur in non-redundant regions of the design. For the present discussion, however, the formulation is limited to non-redundant logic.

Immediately we can identify four conditions:

Regime I. Desirable: The process is stable and the design is manufacturable

$PMI \rightarrow 0$

$DMI = 0$

Regime II. Design limited: The process is stable and the design is not manufacturable

$PMI \rightarrow 0$

$DMI > 0$

Regime III. Process limited: The process is unstable but the design is manufacturable

$PMI >> 0$

$DMI = 0$

Regime IV. Undesirable: The process is unstable and the design is not manufacturable

$PMI >> 0$

$DMI > 0$

DMI can have a value of zero because it depends on user-definable tolerances and it is in a discontinuous function. However, PMI is a continuous function that has a fundamental limit (PMI_{min}). Therefore, a more realistic definition of the manufacturability regimes is as follows:

Regime I. Desirable: The process is stable and the design is manufacturable

$PMI \rightarrow PMI_{min}$

$DMI = 0$

Regime II. Design limited: The process is stable and the design is not manufacturable

$PMI \rightarrow PMI_{min}$

$DMI > 0$

Regime III. Process limited: The process is unstable but the design is manufacturable

$PMI >> PMI_{min}$

$DMI = 0$

Regime IV. Undesirable: The process is unstable and the design is not manufacturable

$PMI >> PMI_{min}$

$DMI > 0$

Both indices are process specific; they depend on the number of design rules used as well as the existing process margins. However, after the definitions of the indices and their arguments are fixed, the indices have the potential to permit a quantitative comparison between evolving processes and design styles.

2.3.3 Areas of Influence: Necessary Design Domain

As new processes push toward smaller and denser features, the areas that can be pre-corrected are geometrically shrinking. For that reason, the simulation area should be commensurate with the target technology and process effect.

Layout design is classified in two categories. The first is custom layout, typically used for microprocessor, memory cell and FPGA design. The second and most common category is based on automated layout generation that uses library-driven digital place and route, in which pre-existing cells (functionality units) are placed and routed to compose the desired electrical system.

Because the placement-independent area of standard cells is disappearing (as Figure 19 indicates), larger blocks must be analyzed to adequately capture the sensitivities of the design. This is one of the main challenges facing library-driven digital place and route; traditionally, place and route tools have dealt only with cell placement impacted by routing and consequent timing closure effects.

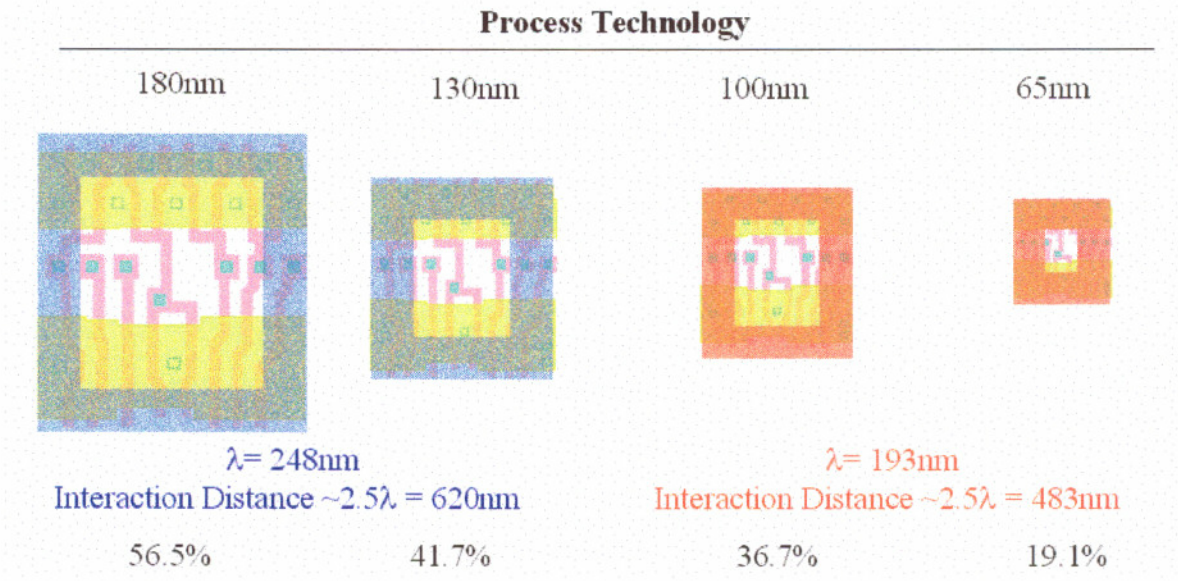


Figure 19. Placement-independent areas for multiple process nodes.

This suggests that IP providers will have to verify their libraries are laid out in a way that is not subject to strong process sensitivities during any of the pattern transfer processes such as lithography, etch or planarization. Otherwise, the same library elements run the risk of performing as designed in some areas and differently in others, which complicates the verification of such electronic systems and creates unnecessary complexity.

On the other hand, custom layout applications can arbitrarily choose the area of interest and simplify the layout verification. This is possible because larger blocks are typically used in such applications, the surrounding layout context is known and no additional assumptions are necessary.

Although having accurate models for each of these processes provides the basis for further improvements in process technology, it is now perceived that blanket process corrections during mask synthesis will result in unacceptable turnaround times and extensive computing requirements (i.e., hundreds of CPUs). But it should be clear that, although such corrections are needed to achieve maximum accuracy during the pattern transfer, this framework suggests simply improving the robustness of the constituents of the final layout, which is based on the relative sensitivity of the layout to process variations.

The challenge of informing design teams which areas are adequate to undergo simulation and analysis can be minimized by the existing hierarchical composition of the layout. This means that for supra-wavelength techniques, cells remain the placement-independent building blocks.

For sub-wavelength technologies, placement-independent blocks can still be achieved, but require a larger number of devices. In other words, while the functional building blocks shrink with process technology, the real chip areas needed to analyze manufacturability will remain fairly constant. In the past, that was not the case, because the wavelengths that the exposure systems used were always ahead of (smaller than) the minimum features present in the design.

For the foreseeable future, the main resolution parameters (i.e., numerical aperture and wavelength) will remain almost constant. Therefore, cells are no longer the manufacturability and functional objects, and the areas needed for manufacturability analysis will need to be calculated by the existing process effects involved in pattern transfer.

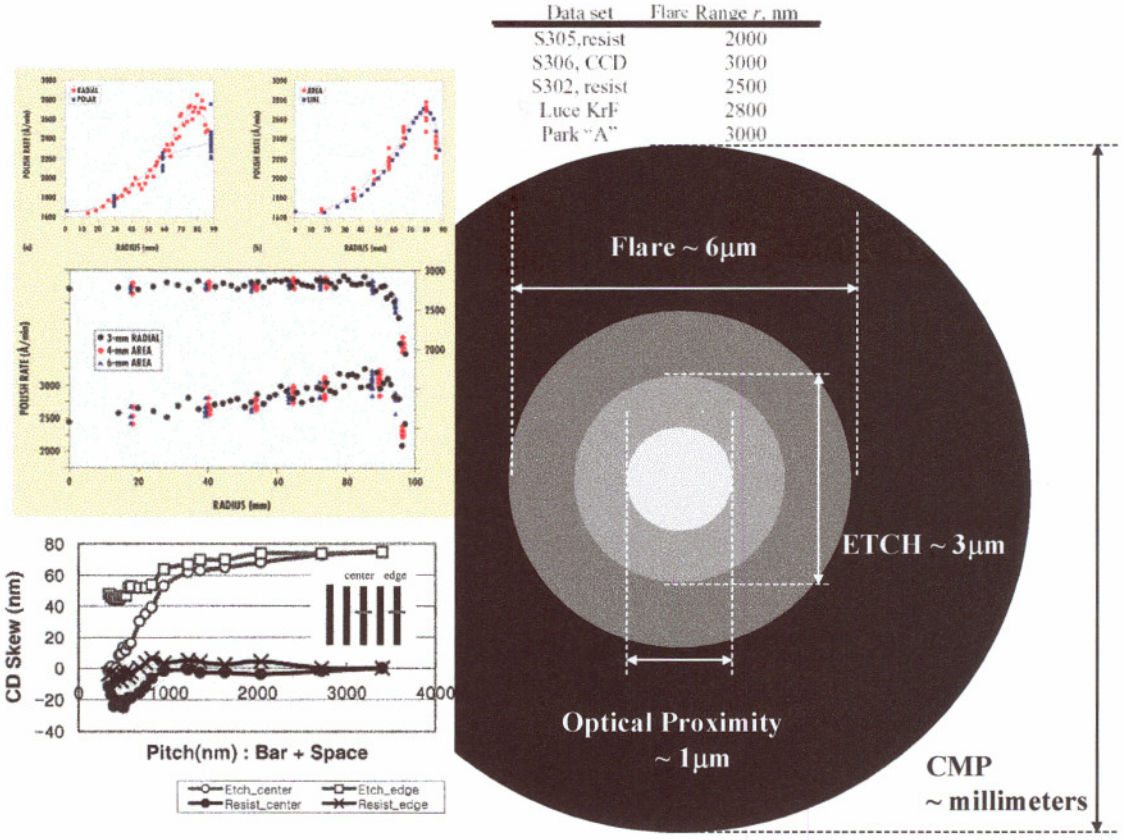


Figure 20. Typical ranges for four mechanisms involved during pattern transfer: chemical metal polish (CMP),[40] optical flare,[42] etch[41] and optical proximity.[41]

Figure 20 depicts typical ranges of influence for four different mechanisms known to degrade the final pattern transfer process: chemical metal polish (CMP), flare, etch and optical proximity. Because of their range of influence, different methods have been adopted to minimize their impact. In the case of CMP, dummy metal fill is inserted to homogenize the pattern density and maintain polishing rates constant throughout the wafer.

Long- and short-range flare mechanisms[42] are minimized by wafer edge exposure, mask blades and redesign of the exposure systems. Etch effects (also predominantly pattern-density dependent[43]) are corrected by small feature biases during mask synthesis. And finally, optical proximity has become the main culprit of pattern degradation and is currently addressed by RET and OPC techniques.

The block boundaries (placement-dependent areas) need to be calculated at the very end by a full-chip-capable tool. By proper management of the boundaries, it is possible to reuse prior analysis data while recalculating only the placement-dependent areas. It is important to note that at every stage of a hierarchical composition, larger placement-independent areas start to populate the entirety of the design, to the point where the process is effectively carried out in parallel. This minimizes the risk of running into bottlenecks during the DFM analysis. However, the only real information that can be carried during layout construction is robustness; an accurate correction imposed by RET or dummy fill is not possible due to the placement-dependent effects previously discussed.

To stress the distinction between accurate and robust designs, the accuracy of a design can be achieved only by providing the complete and final physical representation of the design. By contrast, the robustness of the design can be achieved even with partial information about the final physical implementation by following a hierarchical design construction. In other words, design robustness must be achieved by modifying the structure of the layout during the design stage, and design accuracy should and can be corrected only prior to final mask manufacture.

2.3.4 Simulation Requirements

As indicated in Figure 21A, the formulation of the DFM model should include most systematic and quantifiable sources of error during each processing step. Process development groups can use very early DFM models to select the best process for a set of technology requirements. However, design teams should only use specific DFM models after the process has been partially selected (OPC/RET recipe, initial process window and overlay margins).

This highlights an undesirable effect of DFM in which the only foreseeable opportunity for very early physical design is by designing to multiple process candidates. This is not a limitation of the present framework, but rather a limitation of the DFM concept itself: it is impossible to design for manufacturability when the manufacturing process remains undefined.

Assuming DFM models are available, such models should predict the variability of any element in the design with respect to a given process margin. After this model has been defined, it can be incorporated easily by means of device recognition in traditional timing analysis processes when coupled with the corresponding test vectors, as shown in Figure 21B.

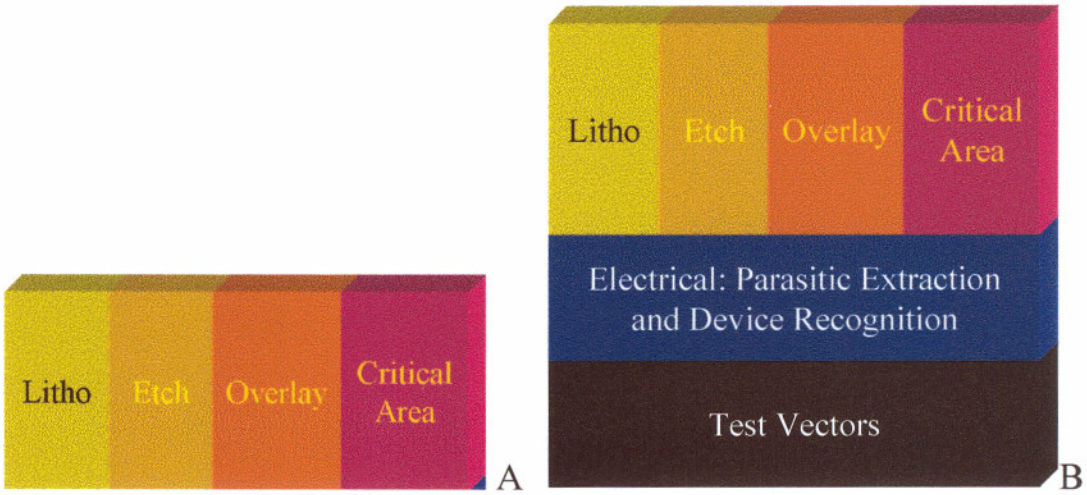


Figure 21. DFM model proposal for analysis and correction (A); coupling the manufacturing information with electrical information to determine the functionality of a device for analysis purposes (B).

New computing platforms have been proposed to deal with the more subtle effects in the deep sub-wavelength regime.[44] Although accurate, these approaches cannot be used for a DFM analysis due to extensive turnaround times. Therefore, the first step is to verify that accurate compact models are available.

Because the range at which CMP operates (on the order of millimeters) is commeasurable to the overall size of the chips to be manufactured, there is no need for extensive modeling at the cell and block levels. The only recommendation is to achieve a density-homogenous pattern to minimize the impact of different polishing rates. Such a density pattern will also be achieved indirectly by improving flare and etch control, because these two effects depend mostly on pattern density.[42,43]

As mentioned before, the models are semi-empirical, especially the resist and etch models. These models are typically based on image intensity quantities. The difference between single- and multiple-process condition models is that, in this case, the model for single-process conditions should be able to predict the CD at one process condition. But a process window model should be able to predict the rates at which the CD changes with respect to a given process variation. In other words, traditional models require the following:

$$\min \sum_{Locations} \left(CD_{simulated} - CD_{experimental} \right) \quad \textbf{12}$$

However, if we generically define a lithography model as follows:

$$CD = CD(P_i) \quad \textbf{13}$$

Where,

P_i can be any number (N) of model parameters

A lithographic process-aware model is also subject to at least two additional constraints:

$$\frac{\partial CD}{\partial Focus} = \sum_{i=1}^{N} \frac{\partial CD}{\partial P_i} \frac{\partial P_i}{\partial Focus} \quad \textbf{14}$$

$$\frac{\partial CD}{\partial Exposure_{Dose}} = \sum_{i=1}^{N} \frac{\partial CD}{\partial P_i} \frac{\partial P_i}{\partial Exposure_{Dose}} \quad \textbf{15}$$

These constraints impose further restrictions to the model, but when met they guarantee the applicability of the model for the purpose of process variability prediction.

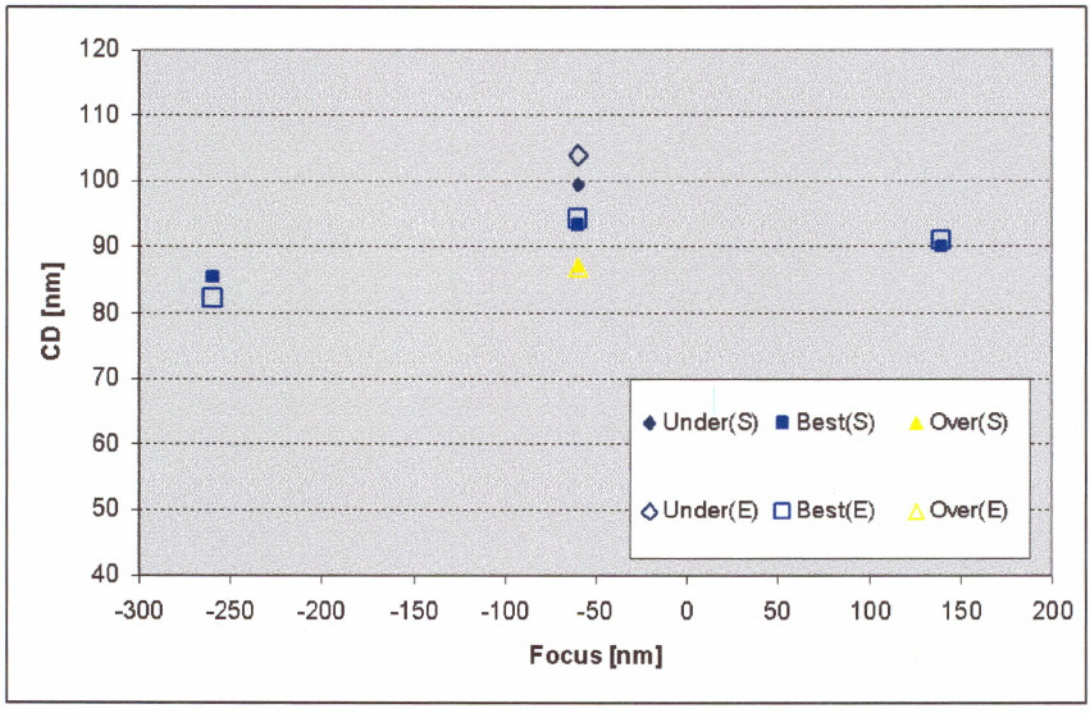


Figure 22. 90nm isolated feature with SRAF at five points of the process window.[32]

This work uses an optical vector model and variable threshold resist model combination to explain lithographic effects. These models have a demonstrated level of accuracy when compared to experimental data (as shown in Figure 22). With these models we can calculate the sensitivity of the design to a particular process variation, and detect failure regions by fully understanding the process signature (Figure 9).

Although this work emphasizes and uses lithography models, the model requirements are applicable for any type of process, as long as the accuracy of the model remains within the metrology and acceptable model error for nominal and process range conditions. What "acceptable model error" means for a particular technology remains to be defined by process integration and circuit design teams.

3 Robust Pattern Design: A Test Case

As an initial test to this methodology, the PMI and DMI were calculated for 130nm and 90nm versions of the same layout by using a 90nm process. This was done to verify the qualitative behavior of the metrics in which a smaller CD design should be more challenging than a larger CD design. Only a subset of single-layer violations was considered:

$$pinch_{Violation} = OR\begin{pmatrix} AND(pvBand(layer)), \\ I2I(pvBand(layer)) \le pinch_{\min} \end{pmatrix} \quad 16$$

$$bridge_{Violation} = OR\begin{pmatrix} AND(pvBand(layer)), \\ E2E(pvBand(layer)) \le bridge_{\min} \end{pmatrix} \quad 17$$

Where,

$pinch_{min}$ = 45nm, $bridge_{min}$ = 45nm

The support region needed to calculate DMI was the layer itself. The process variations were limited to dose and defocus lithographic effects. The dose margins were varied from +/- 5% to +/- 20%, and the defocus variations were modified from +/-50nm to +/-150nm. Polysilicon, thin-oxide, diffusion, n and p implant, metal 1, contacts and nwell were calculated, but only the results for n-implant, polysilicon and contacts are included for discussion purposes.

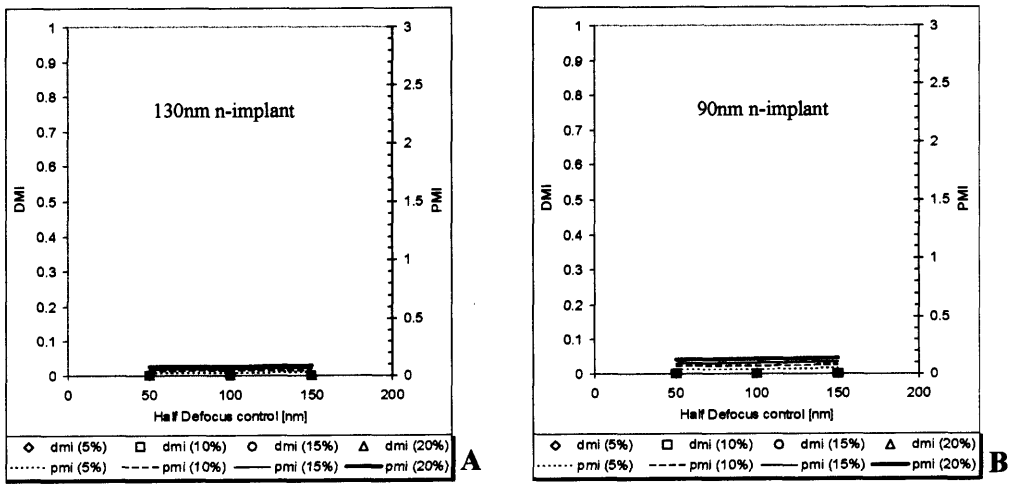


Figure 23. Process and design manufacturability indices for an n-implant layer: 130nm process (A) and 90nm process (B). n-implant layers are typically composed of large features.

As expected, both the DMI (markers) and PMI (lines) are low, showing little sensitivity to process variations. On the other hand, contacts present a contrasting view. Although the DMI remains low, it is now possible to see a slight sensitivity to focus and dose margins. Because DMI is tied to local regions in the layout, it presents the opportunity to improve regions that produce most of the problem. By contrast, PMI shows the sensitivity that focus and dose variations impose on the layout, and that there is a much higher sensitivity for 90nm contacts than for 130nm contacts. This sudden jump in DMI (as Figure 24 indicates) is a characteristic response of a layout close to the limits of the process. However, depending on the process margins, none, some or all the contacts fail, providing the opportunity to identify topologies that are robust to process variations and replicate them for more sensitive contact arrangements.

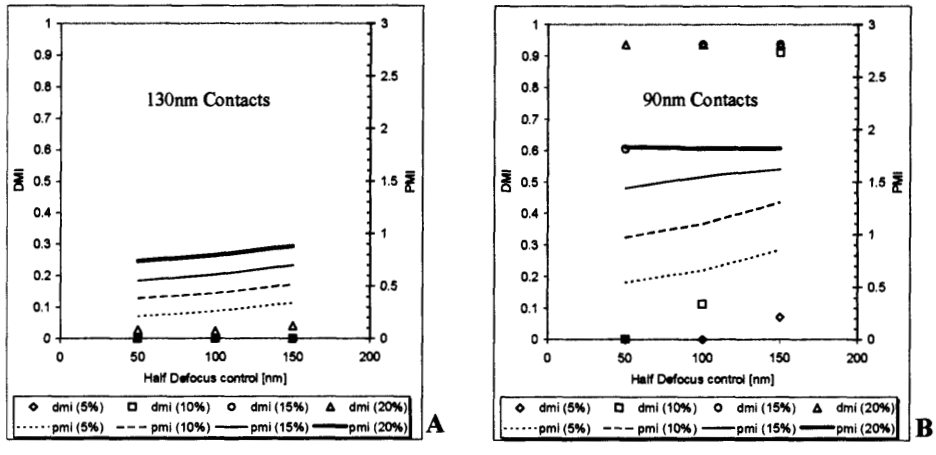


Figure 24. Process and design manufacturability indices for a contact layer: 130nm process (A) and 90nm process (B).

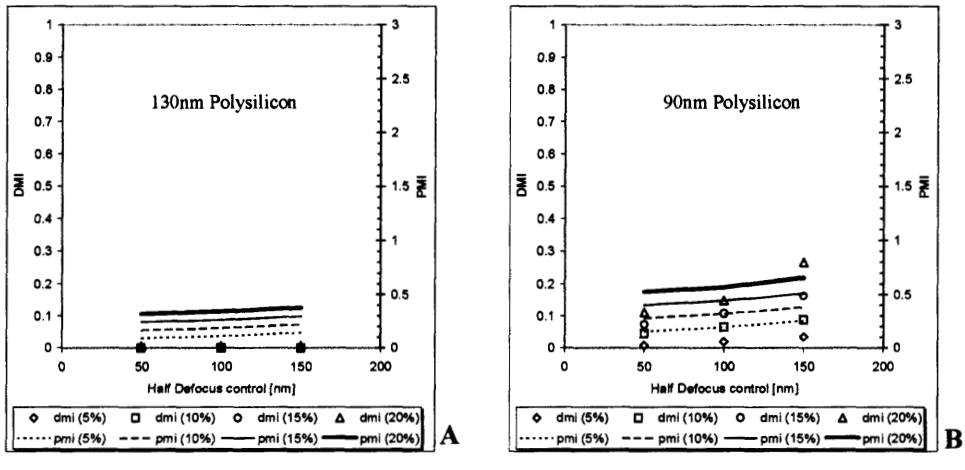


Figure 25. Process and design manufacturability indices for a polysilicon layer: 130nm process (A) and 90nm process (B).

Figure 25 shows the DMI and PMI for the polysilicon layer. Unlike a contact layer, in which a contact either opens or closes, this layer does not completely fail. Instead, the manufacturability is more continuous, with some regions failing while others image well.

This way of identifying regions that fail and comparing them to those that do not fail makes it possible to determine quantitatively the improvement in manufacturability after the changes have been made. At this point, it is also possible to assess changes in one layer and determine how the modifications affect other layers by calculating the complete DMI and PMI for all layers of interest. In this manner, even if manufacturability is gained in one layer, the negative effects in others can be quantified, and a more informed decision about the changes can be made.

3.1 Design Optimization

The example that follows integrates design and manufacturing information and uses the proposed framework to improve the manufacturability of a small library cell. The schematic and layout understudy are shown in Figure 26.

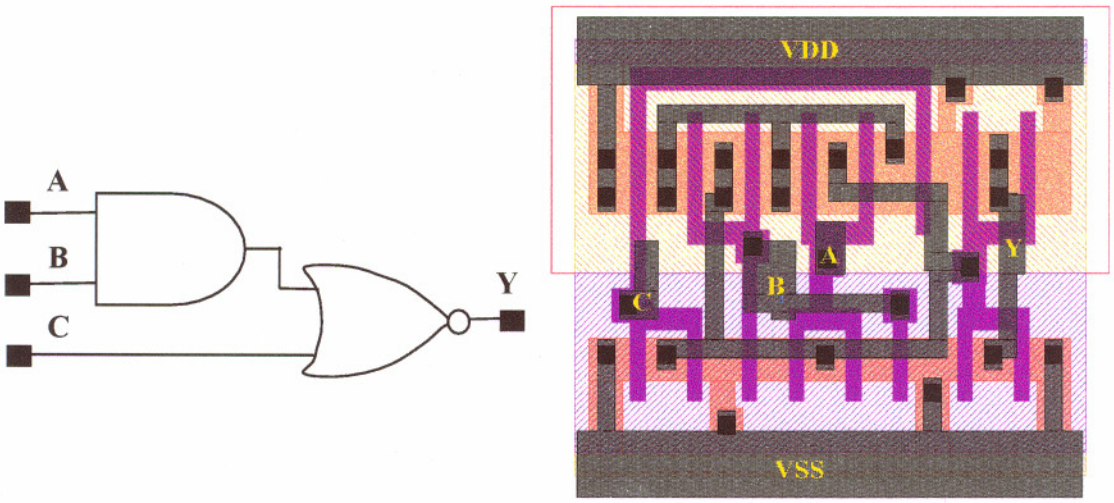


Figure 26. Schematic and initial physical implementation.

This DRC clean cell was obtained initially by an automated compaction tool. The subsequent operations maintained the DRC clean condition while seeking a different, more manufacturable topology.

The modifications were subject to traditional multi-layer constraints (e.g., poly landing pads were aligned with contact and metal layers). The complete truth table was tested for static functionality. The dynamic functionality was defined by 13 events that correspond to the number of times the output signal (Y) changes during the truth table test.

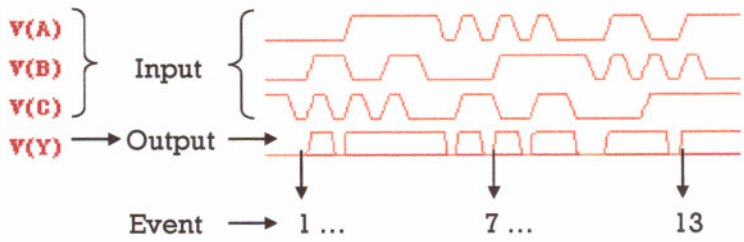


Figure 27. Event definition. Thirteen events were sampled for every litho-process condition.

For two reasons, a 90nm-capable manufacturing process was used to simulate the 130nm cells. First, it tested the sensitivity of the design optimization method since a 90nm process should have no problems in manufacturing 130nm designs rules. The second reason was that complete SPICE models were lacking. Because of their tabular nature, using a 90nm process model provided access to smaller feature sizes relative to the 130nm nominal features.

The simulations for each process condition used existing parasitic and SPICE models. To simulate timing, the 130nm cells were modeled by using an existing 90nm process. In this way, the SPICE model tables were able to interpolate the smaller geometries from the process-induced topological changes.

The layout optimization was carried out by minimizing DMI and PMI, and then modifying the layout manually by following RDR principles such as arraying contact holes in regular clusters, ordering the elements of the poly layer in a regular grid, modifying the landing pads placement to make use of existing low aspect-ratio regions and increasing metal width when possible.

The layout optimization method was as follows:

1. Calculate DMI by using two process conditions: one at 200nm depth of focus (DOF) and 10% exposure latitude (EL), and another at 400nm depth of focus and 40% exposure latitude.

2. Identify layout sensitivities and follow RDR recommendations to improve the layout.

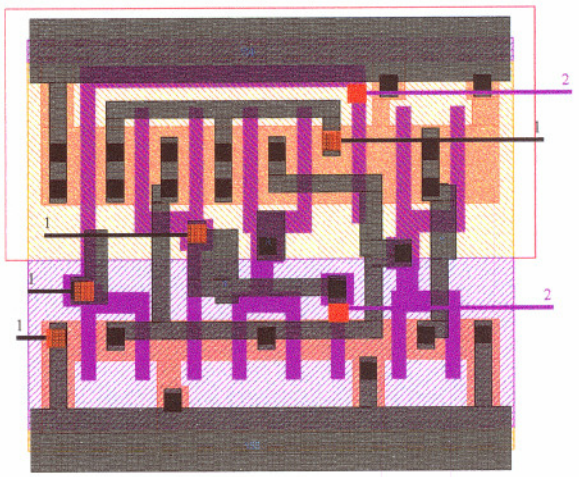
The objective of the optimization was to make DMI zero at the less aggressive process requirements (200nm DOF, 10% EL), and to improve or maintain the DMI at the more aggressive process requirements (400nm DOF, 40% EL).

The initial manufacturing analysis of the cell is presented in Figure 28. This figure indicates that there are four weak contact locations and two likely pinch-points in the polysilicon layer when assuming the less aggressive process variations. It also shows that the DMI for the contacts is much larger relative to the other two layers of interest when subjected to large process variations. For that reason, contacts are modified more extensively than other layers due to the relative DMI values.

Errors calculated @ DOF = 200nm, EL = 10%, Simple OPC.

1) Non resolving contacts

2) Poly silicon pinching



Layer	DMI
POLY	0.008
CONTACT	0.294
METAL1	0.004

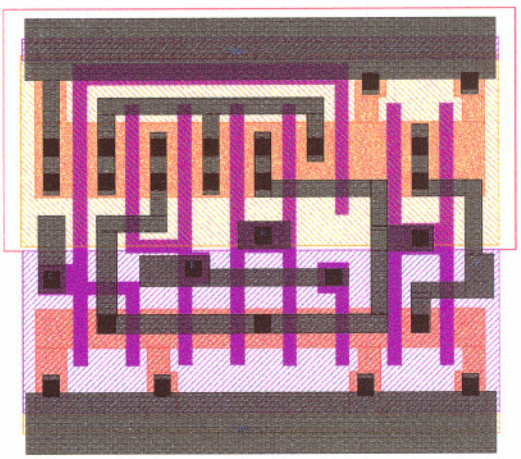
Table calculated at @ DOF = 400nm, EL = 40%, Simple OPC.

Figure 28. Initial layout analysis and detection of sensitive areas.

Figure 29 illustrates that, after performing modifications to the contact and polysilicon layers and minor adjustments to the other layers, the errors detected for contacts and polysilicon have disappeared for the small process variations. At the same time, the DMI for contacts and polysilicon has also improved (since a smaller value is preferred) with respect to the original layout. Unfortunately, the modifications adversely affected the metal layer, in which the DMI increased from 0.004 to 0.005. While this change is small and can be detected only at the larger process variation conditions, new modifications to the layout are explored to try to return the DMI to its original value.

Errors calculated @ DOF = 200nm, EL = 10%, Simple OPC.

0) None



Place contacts on grid and modify metal and poly

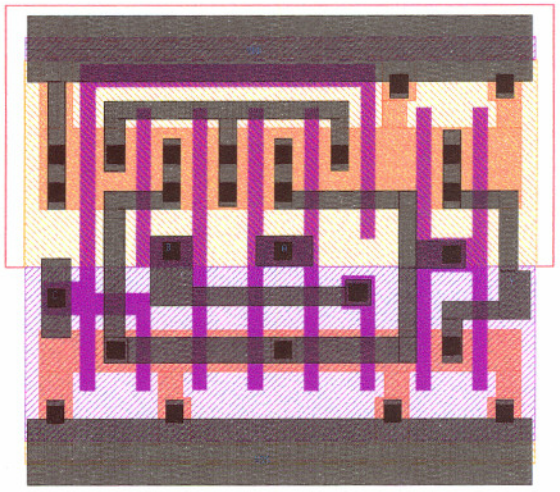
Layer	DMI
POLY	0.007
CONTACT	0.000
METAL1	0.005

Table calculated at @ DOF = 400nm, EL = 40%, Simple OPC.

Figure 29. Analysis after layout modification using RDR principles and detected errors.

Errors calculated @ DOF = 200nm, EL = 10%, Simple OPC.

0) None



Widen metal and change poly and contacts accordingly

Layer	DMI
POLY	0.007
CONTACT	0.000
METAL1	0.004

Table calculated at @ DOF = 400nm, EL = 40%, Simple OPC.

Figure 30. Analysis of the final layout.

Figure 30 shows the final variation, in which the metal is widened in order to restore the original DMI value without affecting the other layers. The most manufacturable cell along with the companion pv-Bands are depicted in Figure 31.

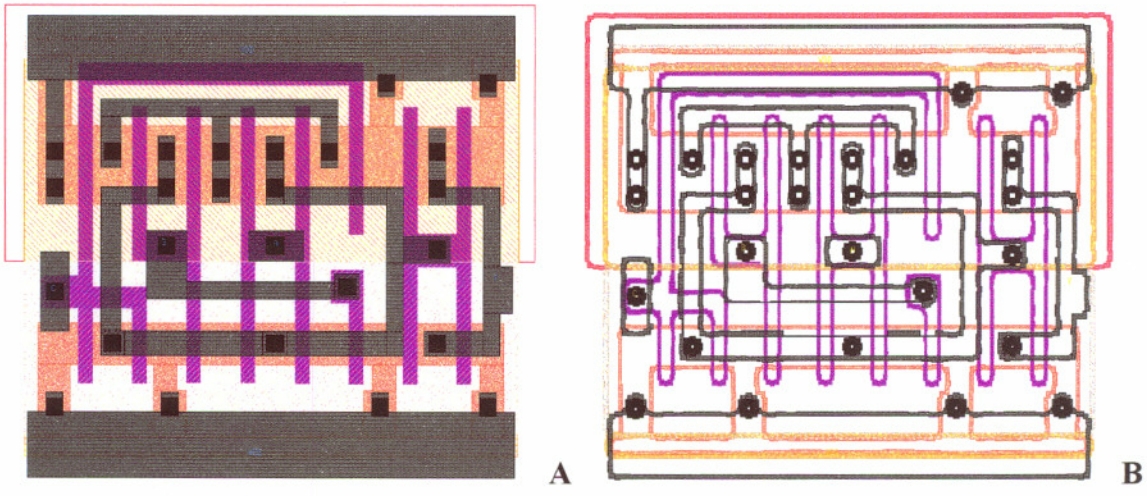


Figure 31. Optimal 130nm physical implementation of the test cell (A) and respective pv-Bands for all layers (B).

Notice how the cell implementations (Figure 26 versus Figure 31) differ in topological aspects; the optimized cell takes on a more manufacturable grid-like aspect as proposed by RDR. The area of the

original and the optimized cells is the same, and both operate as designed at nominal conditions. However, a stricter comparison involves the cell characterization at other processing conditions.

The DMI and the PMI were calculated at +/-5, 10, 15 and 20% dose control and +/- 50, 100, 150, 200 and 250nm defocus control. Due to the definition of DMI and PMI, a smaller value is desirable, indicating that the pattern transfer variability is small with respect to the area of relevance. This effectively converts the layout optimization problem to a cost-function minimization problem and introduces the possibility for automatic corrections.

Unfortunately, existing compactor tools do not easily support configuration changes, especially those needed to define symmetry and array properties, because they are based primarily on space and width measurements. Nevertheless, automatic correction methods seem within reach by improving existing compaction methods and adding pv-Bands capabilities.

Because of the lack of such automatic tools, the correction method was performed manually as previously described by using a layout editor and a pv-Band calculator environment.

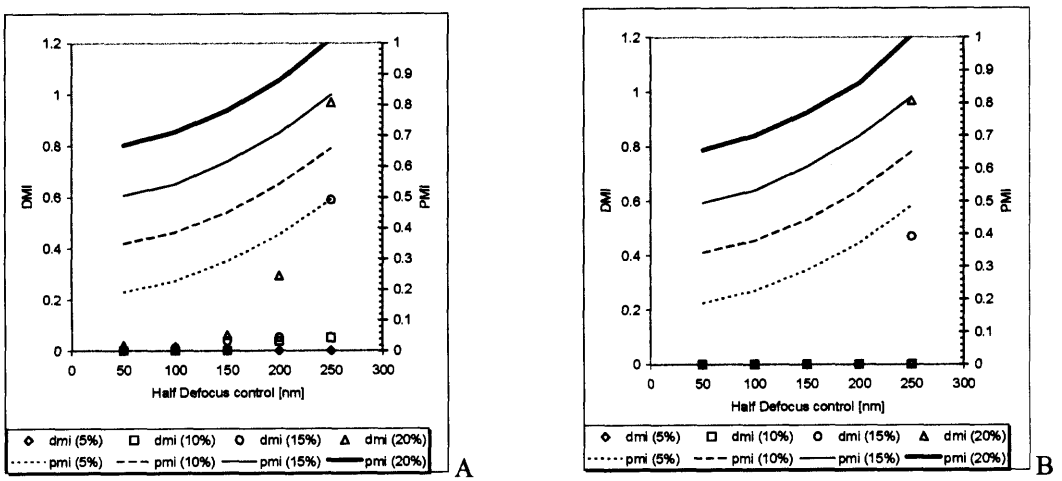


Figure 32. Manufacturability indices for contacts (130nm technology): original cell (A) and optimized cell (B).

Figure 32A shows how contacts drastically fail (i.e., isolated contacts do not open and dense contacts merge) at the larger defocus conditions (+/-200 and +/-250nm) and more extreme dose margins (+/- 15 and +/-20%), but it also indicates that there are a few errors at even tighter process control. By contrast, Figure 32B shows large failures at the largest process margins, but high process insensitivity at any other process condition.

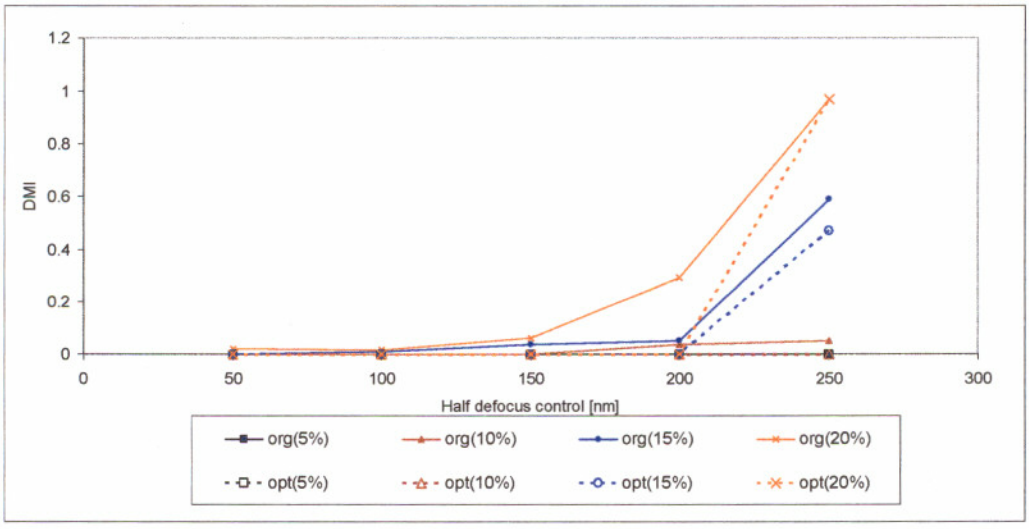


Figure 33. Contact DMI results for the original and the optimum cells.

For layout optimization purposes, DMI is the main figure of merit. Figure 33 compares side-by-side the DMI across multiple process margins. Notice how the optimal cell (opt) consistently has a lower DMI when compared to the original (org) cell.

One of the main problems with making a layer insensitive is that improving the manufacturability of one layer can adversely affect another. To assess this concern, Figure 34 shows the results for the polysilicon layer and how improvements can also be made to this layer. The improvements are much less dramatic (notice the different DMI scale), but nevertheless they are present.

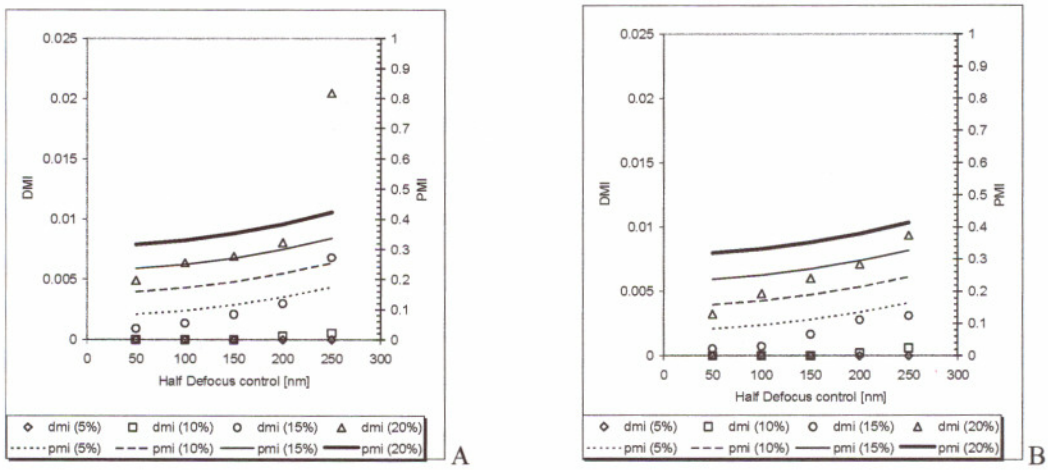


Figure 34. Manufacturability for polysilicon (130nm technology): original cell (A) and optimized cell (B).

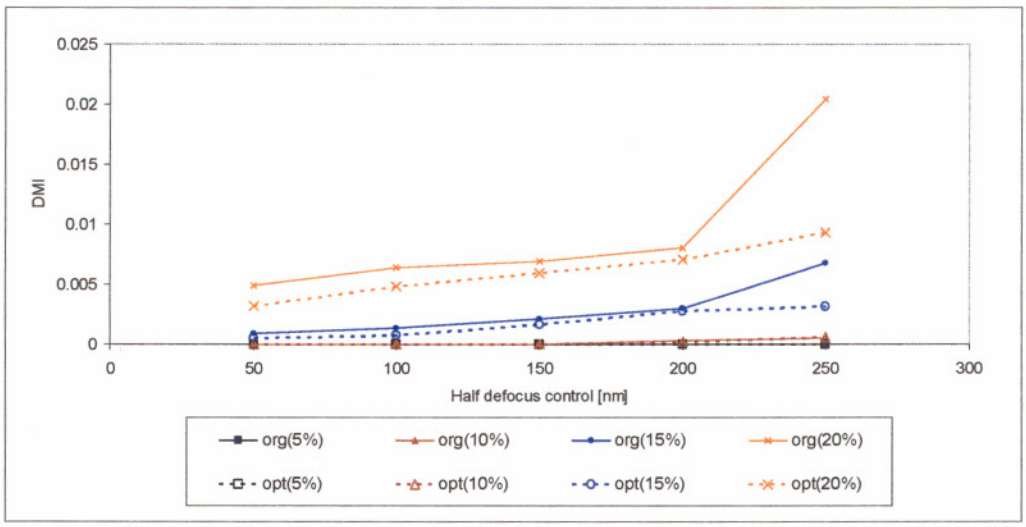


Figure 35. Polysilicon DMI results for the original and the optimum cells.

To better assess the improvements in DMI for the polysilicon layer, we compare the original and optimum cells. As Figure 35 indicates, the DMI is consistently better for the optimum cell (dashed lines and open markers) when compared to the original (solid lines with solid markers).

Finally, the same analysis is performed for the metal 1 layer. Figure 36 and Figure 37 show how the metal 1 DMI is similar between the original and optimized cells. Because the DMI for metal 1 is already extremely low (compared to that of the polysilicon and contact layers), it is fair to say that the DMI has been marginally improved. This indicates that this method is not only useful to improve topologies that will very likely fail (such as contacts), but it can also provide a very fine metric to distinguish more robust configurations.

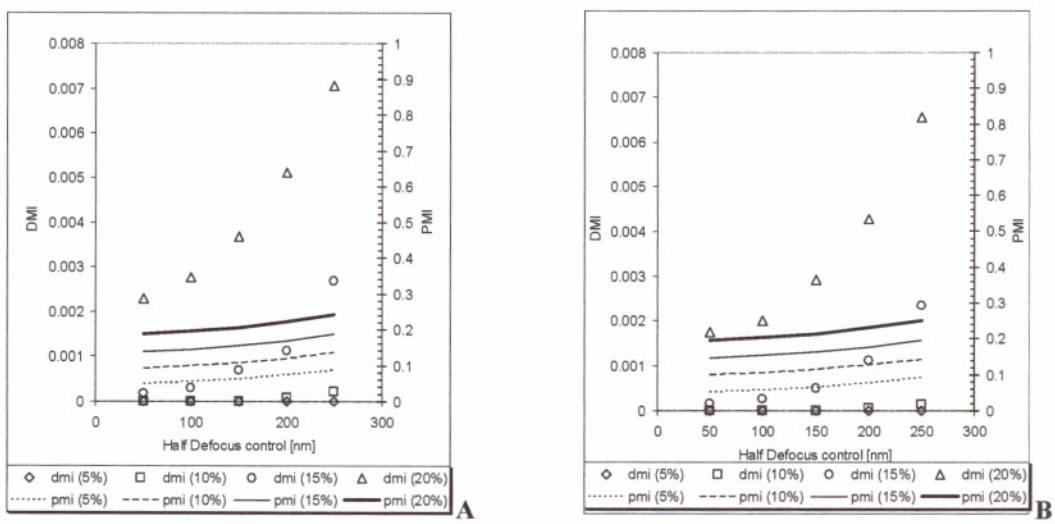


Figure 36. Manufacturability for metal 1 (130nm technology): original cell (A) and optimized cell (B).

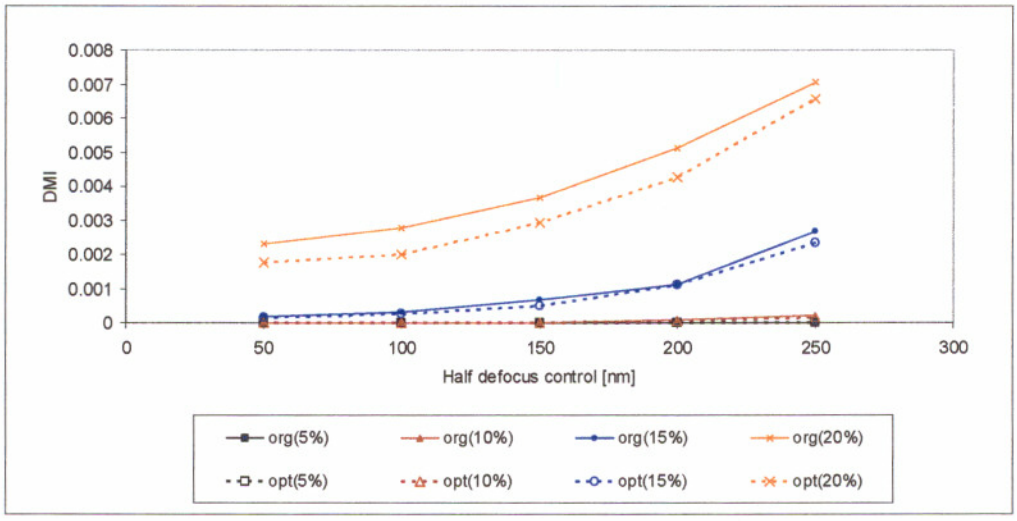


Figure 37. Metal 1 DMI results for the original and the optimum cell.

The same analysis could be done to all layers, but since n and p implant, oxide and diffusion layers remained unchanged there is no difference between the PMI and DMI. These layers were not optimized because they did not exhibit any failure points within the process margins of interest, and they did not have to be modified to accommodate any changes imposed to the poly, contact and metal 1 levels.

It is of interest to investigate whether the modifications performed on the 130nm design provide a more manufacturable design across multiple technology nodes. To achieve the evaluation, the 130nm cell was directly shrunk to 90nm. Since there were no 90nm DRC rules available, both cells might not have been DRC clean; however, it is important to assess the validity of this typical design migration method that has been in use until today.

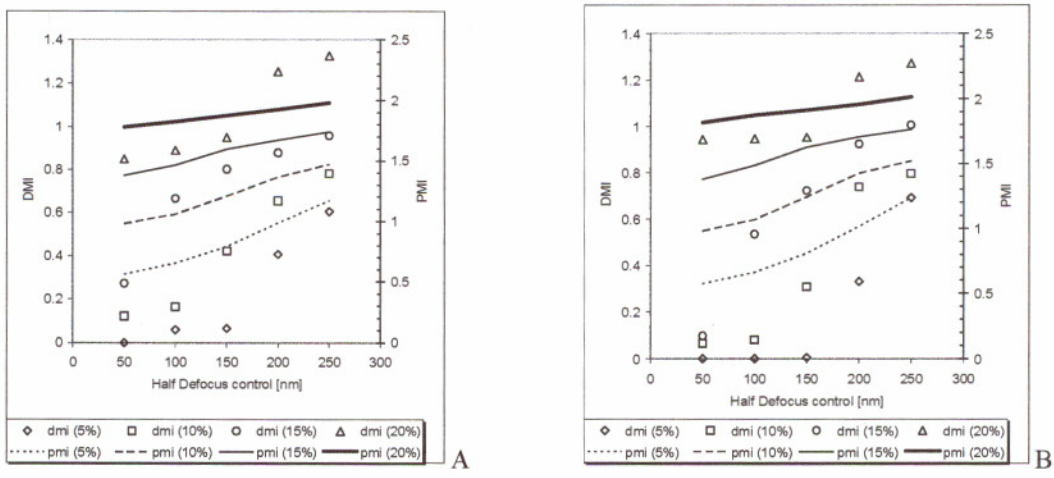


Figure 38. Manufacturability indices for contacts (90nm technology): original 130nm cell shrunk to 90nm (A) and optimized 130nm cell shrunk to 90nm (B).

To evaluate the validity of design migration, only the most challenging layer (contact) was analyzed. As Figure 38 and Figure 39 indicate, at 90nm the sensitivity to process variations is much more evident. The previously calculated optimal contact layer, now shrunk by a factor of 70%, is only slightly better than the original, which is shrunk by the same rate.

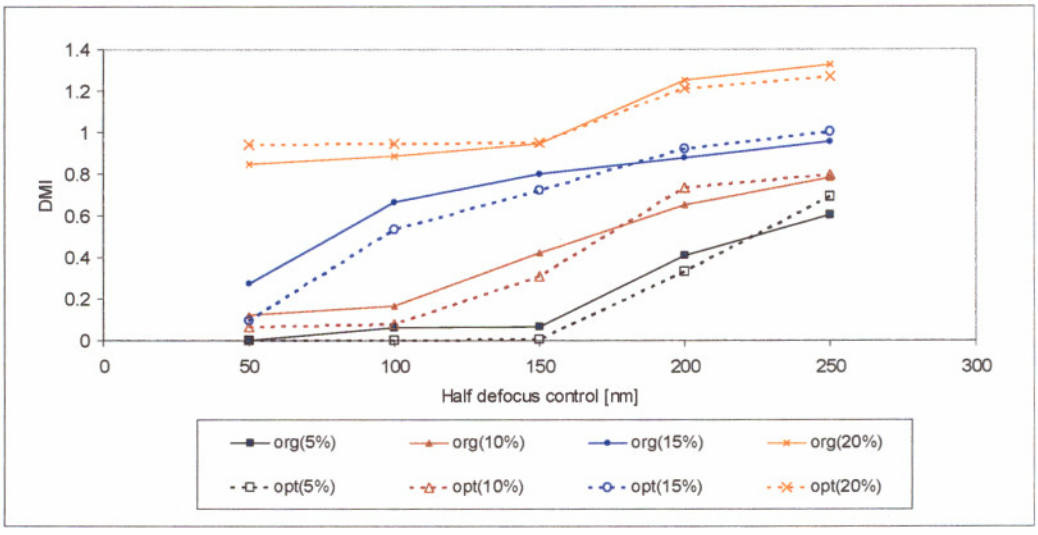


Figure 39. DMI results for the original and the optimum cell, both shrunk from 130nm to 90nm.

This data highlights an undesirable side effect of DFM: optimal topologies can be tied to a particular process technology in a way that makes it difficult to generate a solution that returns maximum manufacturability for a group of available processes.

In principle, this limitation can be addressed by considering the bounds of multiple processes instead of one. This, of course, adds to the computational requirements, but it remains feasible. The downside is that, unlike a solution targeted for a specific process, this solution can be suboptimal for the final process. This is when the availability of a manufacturability index helps guide the design tradeoffs by quantitatively measuring how much more manufacturable a design would be for any given processes.

3.2 Pattern Robustness Analysis: Critical Dimension Stability

Pattern robustness is typically assessed by focus-exposure data in which a given feature is being sampled. Figure 40 shows feature changes that affect gate length for the original (**org**) and the optimized (**opt**) cell.

Under the worst process margins (+/- 250nm defocus and +/- 20% dose change), the total CD range for the original cell is about 63nm, and for the optimized cell is 53nm. This is how lithographers typically report feature behavior with process variations.

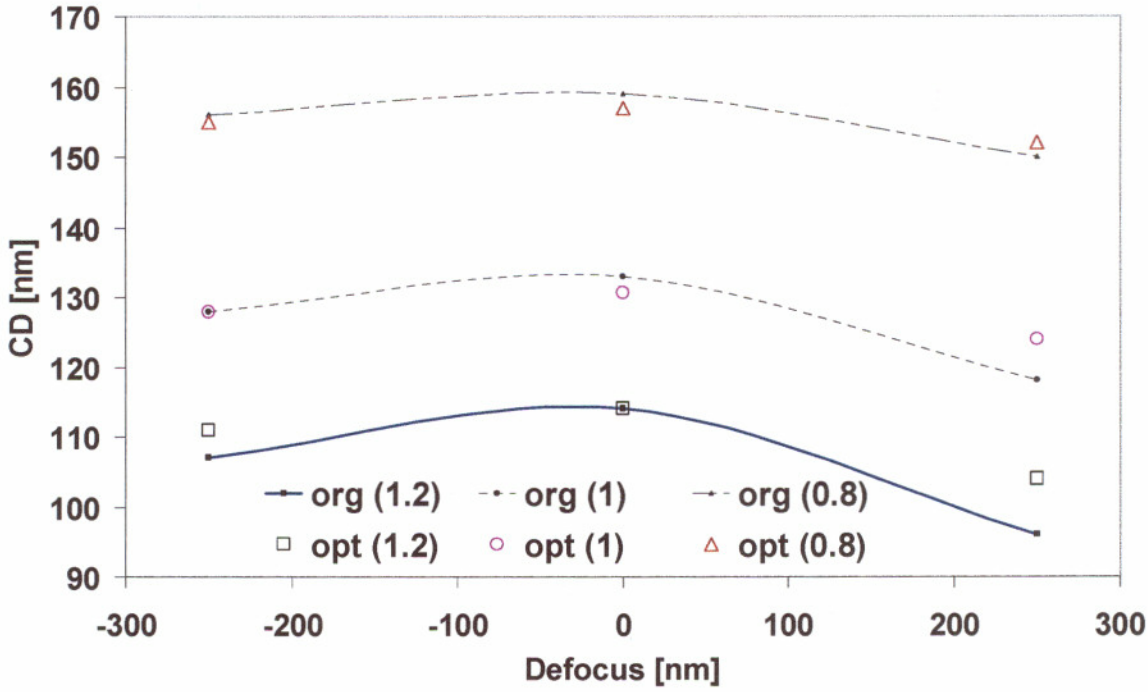


Figure 40. Focus-exposure "Bossung" graph showing the CD behavior across focus and energy dose for the same transistor.

The problem with this type of analysis is that not all features behave in the same manner. Although there are regions that can be made more robust, others regions are very sensitive to process variations. How much these feature variations affect the electrical behavior of the cells has been a popular topic of investigation[12,45] that will be addressed in the following section.

3.3 Electrical Analysis: Timing Process Windows

After the manufacturability index of the region is optimized, the electrical impact can be correlated to the functional (timing) information to determine whether the manufacturability margins are adequate. Using the experimentally calibrated process window models, we can recalculate the effect in the timing process window for two different devices: one timed element and one untimed element. In this case, only the polysilicon layer was allowed to fluctuate to illustrate the method, but in principle this can be done for any number of layers.

The limitation then becomes the amount of computing power needed to correctly characterize the electrical variations. For this reason, it is preferable to make the design less sensitive to process variations, or at least equivalently sensitive, so that this electrical analysis can be performed in the traditional fashion.

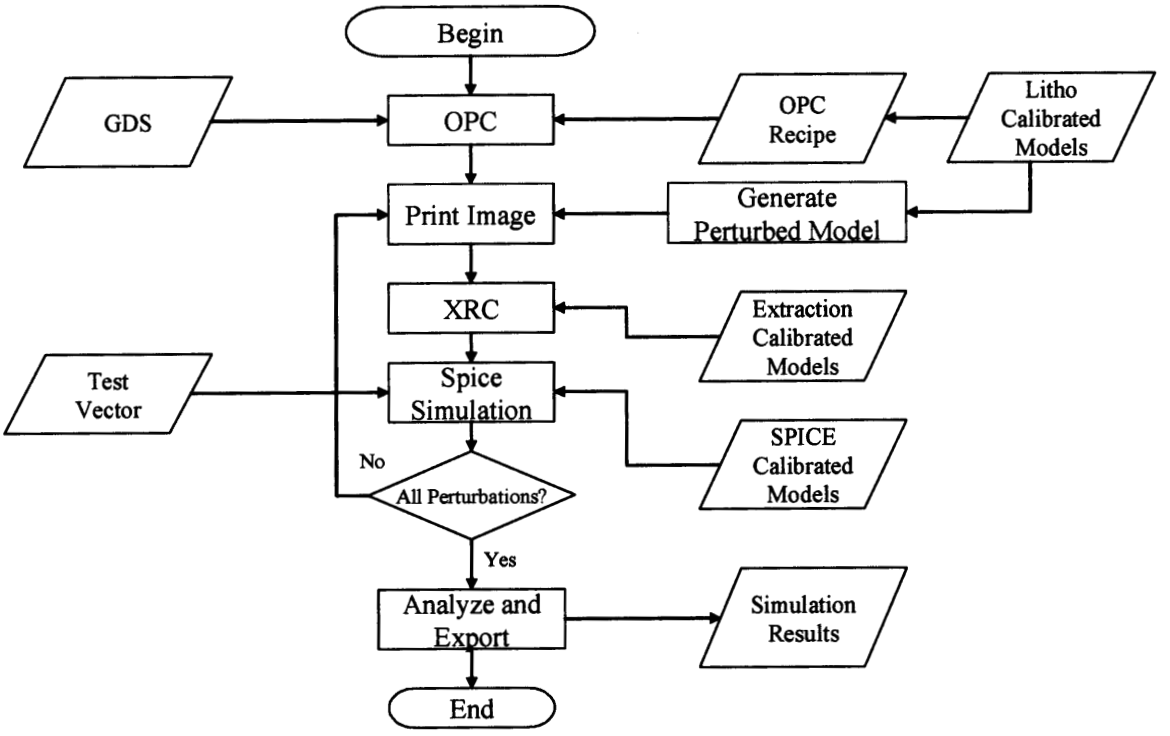


Figure 41. Electrical analysis for designs subject to process fluctuations during manufacturing.

To assess the improvements that a more robust pattern provides to the parametric behavior of a design, the flow depicted in Figure 41 was implemented in a program called EDOCEO. (Translated from Latin, EDOCEO means "to instruct thoroughly, to inform fully".)

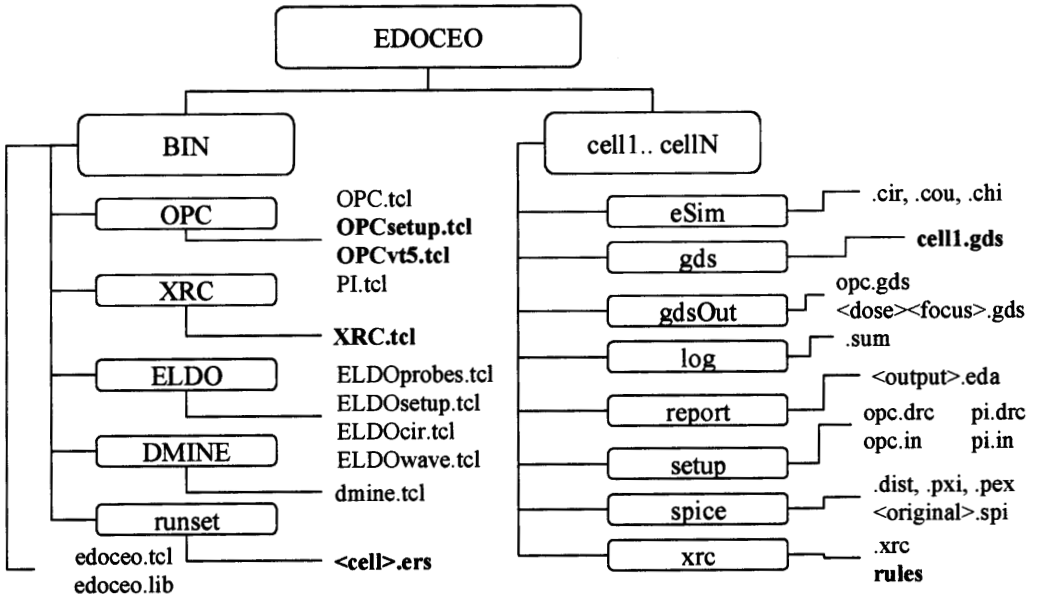


Figure 42. EDOCEO components.

The organization of the program along its major components is depicted in Figure 42. The program consisted of interfacing existing EDA tools from Mentor Graphics using the tcl/tk scripting language. The tools used were Calibre® DRC, LVS, XRC and RET for the computation of the silicon image and extraction of the new electrical system, and ELDO for the timing simulation. The analysis and reformatting were accomplished by developing tcl/tk programs.

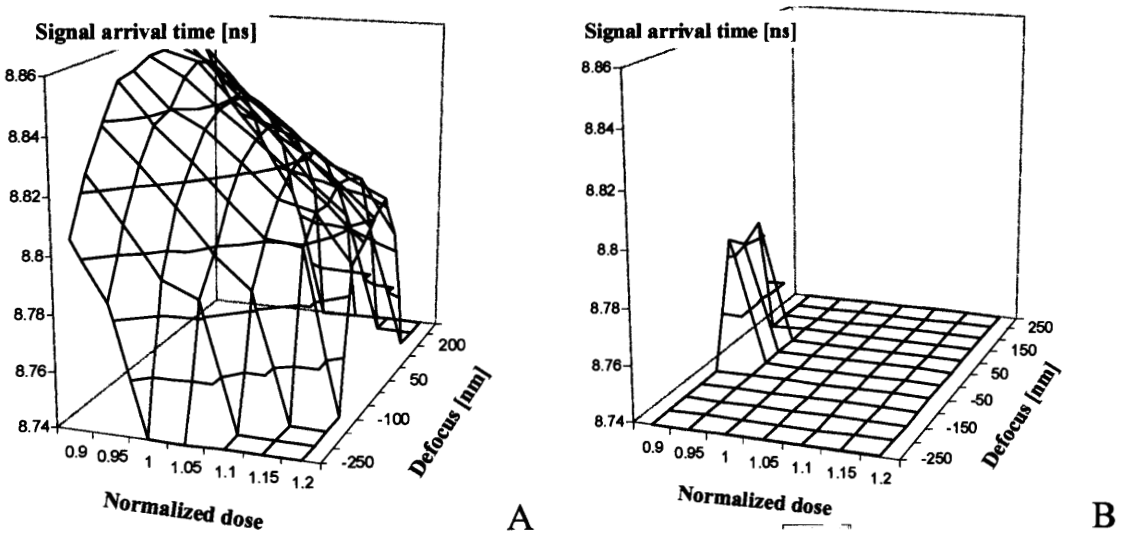


Figure 43. Clocked elements: dose (front horizontal axis), focus (perpendicular to the page plane axis) and signal arrival time (vertical axis), with OPC (A) and without OPC (B).

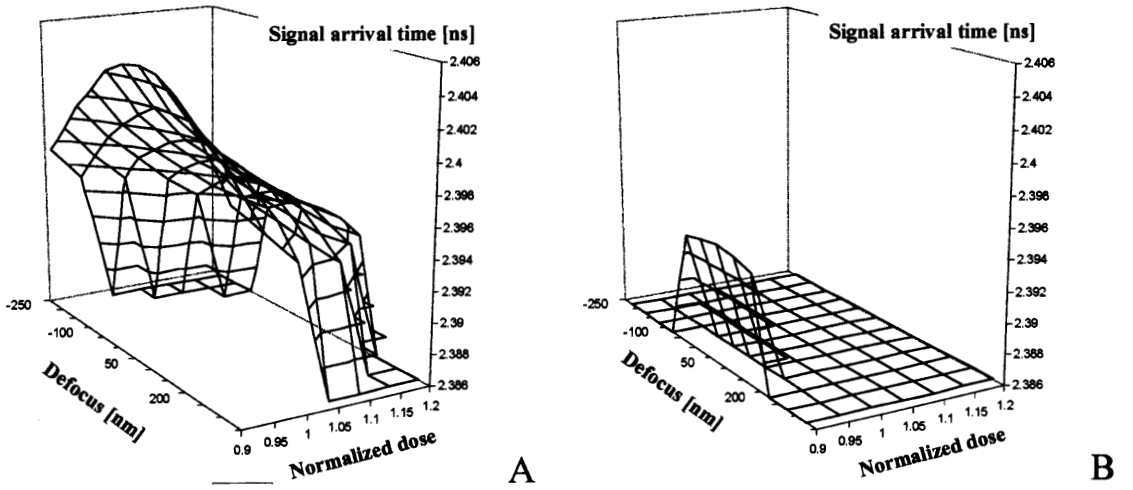


Figure 44. Unclocked elements: dose (front horizontal axis), focus (perpendicular to the page plane axis) and signal arrival time (vertical axis), with OPC (A) and without OPC (B).

As an example of the results that such a program can generate, Figure 43 and Figure 44 correspond to two timing test vectors for different process window conditions applied to a 130nm polysilicon layer. Only the polysilicon layer was replaced during the analysis; therefore, the contributions to timing from the "imperfection" of other layers were assumed to be zero.

As these figures show, the use of OPC is mandatory for sub-wavelength processes. For that reason, the process characterization step should include the nature of the RET being used because it will introduce its own sensitivity signature.

Traditionally, manufacturing facilities provide five types of SPICE models: TT (nominal), FF, FS, SF and SS, referring to the fast (F) and slow (S) conditions for the n and p transistors. By the nature of their calibration, SPICE models incorporate all processing effects, including lithography, from a statistical analysis of the process corners.

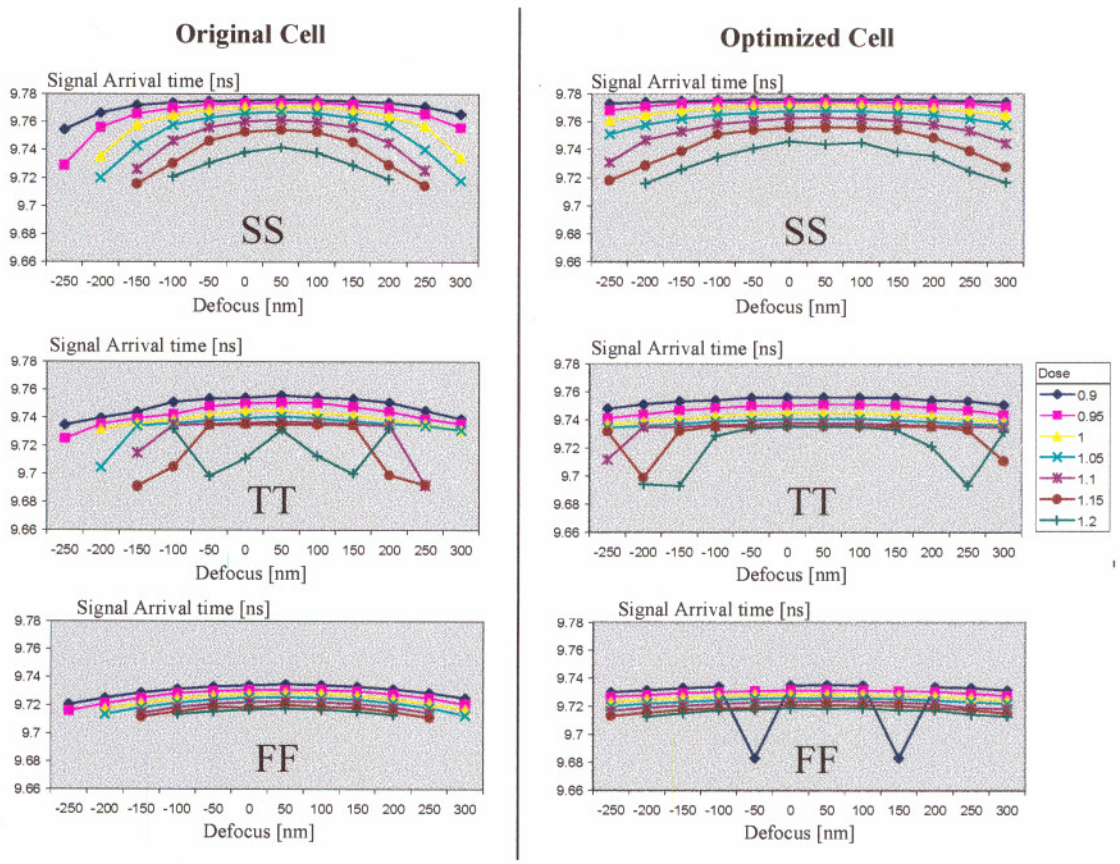


Figure 45. Original and optimal cell timing: signal arrival times using fast (FF), slow (SS) and nominal (TT) SPICE models.

The inclusion of multiple effects complicates the analysis of individual contributors. However, by explicitly calculating one manufacturing effect across all available electrical models, it is possible to determine the

raw sensitivity of the design to the manufacturing effect. For simplicity, this analysis assumes that all layers are built perfectly as drawn, and only the polysilicon layer has been replaced by the real silicon image.

This is a conservative approximation of the impact that lithography has on the electrical performance of devices. The simulations are done by using all five available SPICE models in order to assess the relative contribution of lithography to the complete processing behavior. Although the timing margins established by the non-nominal models (FF, SS, SF and FS) are able to enclose the polysilicon process variations at nominal conditions (TT), it is clear that the process-induced pattern variations contribute greatly to the total design margin.

Figure 45 (nominal, fast and slow SPICE models) and Figure 46 (nominal and mixed-mode SPICE models) show how the optimal cell continues to function under an even a wider set of process conditions. When the cell ceases to operate, the data series are truncated, thus indicating that a fatal failure has occurred.

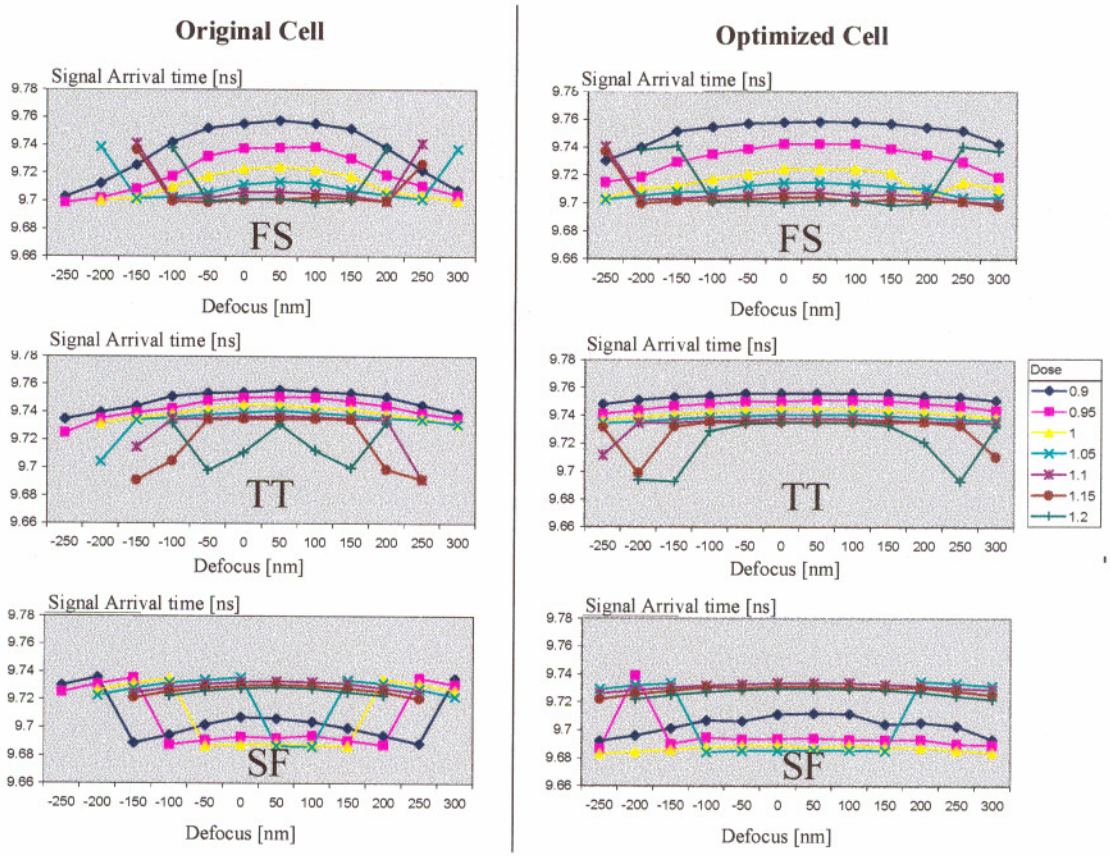


Figure 46. Original and optimal cell timing: signal arrival times using mixed-mode (SF and FS) and nominal (TT) SPICE models.

Figure 47 shows event 3 under a variety of process conditions and RET treatments. It is no surprise that the optimal cell shows the smallest delay sensitivity under most of the tested process conditions.

The same analysis was performed on the original cell with and without RET. The very different behavior in the three cases suggests that, to correctly predict the electrical behavior of a layout, it may be necessary to incorporate RET and process information during the electrical simulations, particularly when trying to determine the margins of operation.

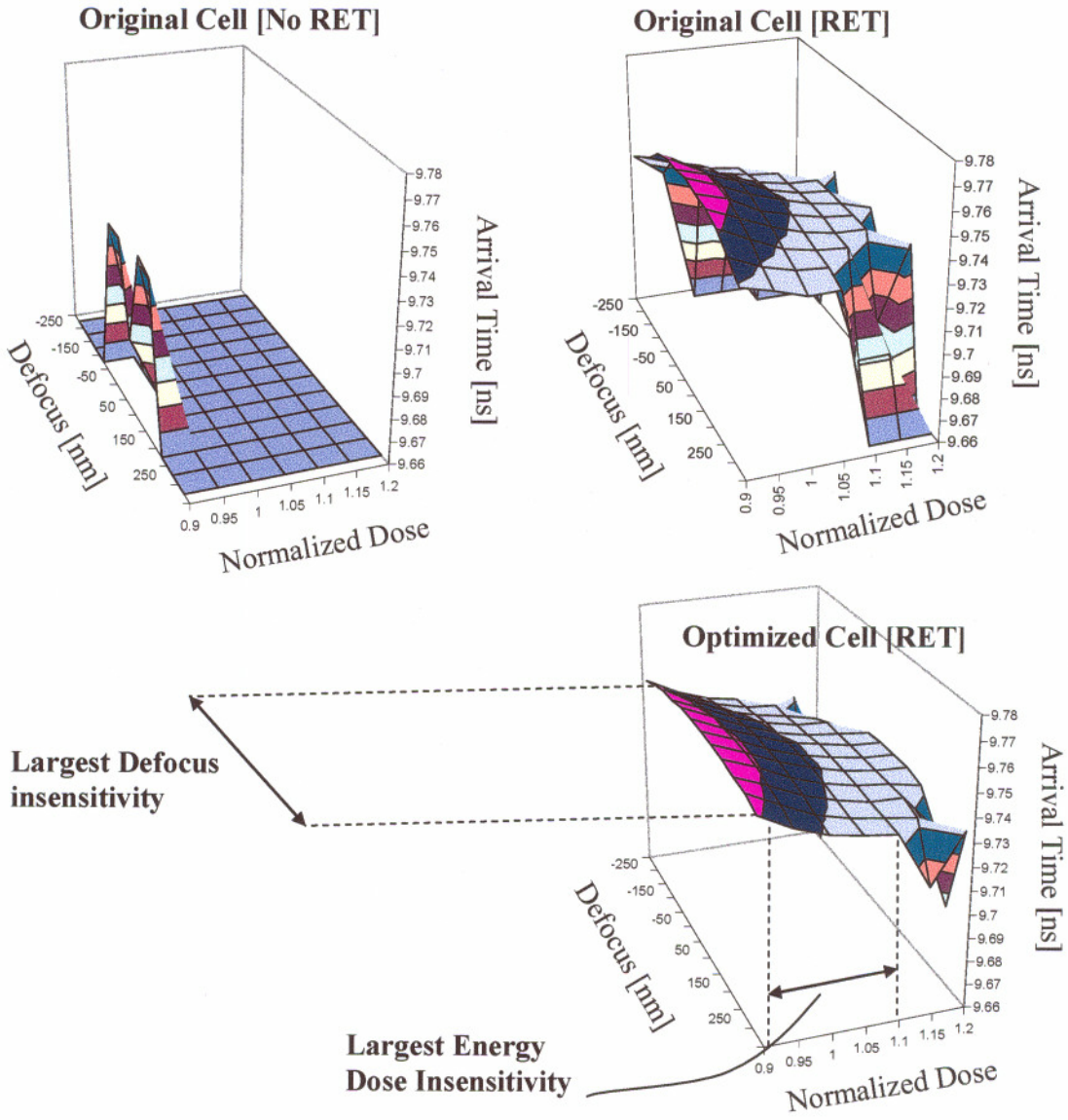


Figure 47. Pattern robustness translates into more consistent timing. (Nominal SPICE model shown.)

These figures show an important aspect of the proposed framework: as the process control improves, the need for more robust designs diminishes. Conversely, as the process margins worsen with respect to the

target geometries (as is likely with smaller and smaller sub-wavelength processes), the need to qualify the sensitivities of the design in a consistent and standardized fashion increases. These plots also suggest the need to better account for these pattern transfer sensitivities in a more complete fashion in existing electrical models.

In practice, such timing analysis is excessive and does not provide any clear guidance for improving the design. However, employing this type of refined analysis is useful for characterizing the benefit that different design-for-manufacturing techniques provide. In addition, as Figure 47 suggests, the proposed framework results in a direct and beneficial impact on the parametric response and does not require additional electrical simulation of the system.

3.4 Considerations with Respect to Existing Methods

As mentioned in the introduction, multiple approaches are currently proposed to improve the manufacturability of design layouts. This section describes why this work is a superset of some methods and a complement to others.

3.4.1 Critical Area Analysis

While it has already been discussed why a critical area analysis is insufficient to explain all observed yield-loss for subwavelength pattern imaging (Section 1.2.1), critical area is complementary to this work when critical area is used solely to study random defects. Since this work is based on modeling systematic components of yield-loss, critical area analysis complements this method by addressing problems that are random in nature and, therefore, are not captured by this proposal.

3.4.2 Improve Contrast Method

By improving pv-Bands that consider dose variations, image contrast is automatically improved. Image contrast is defined as the rate at which the image intensity (I) changes with respect to a distance parallel to the wafer surface (x). For that reason, contrast has been found to be a good indicator of healthy image formation.

$$Contrast = \frac{\Delta I}{\Delta x} \qquad \textbf{18}$$

Since the proposed framework is based on reducing the width of the pv-Band, and the width of the pv-Band is determined by different intensity (dose) levels, we can immediately see that by keeping ΔI constant and minimizing Δx, the contrast of the image increases, thus improving the quality of the pattern transfer.

3.4.3 Reduce Mask Error Enhancement Factor (MEEF)

While it was not presented as an example of this work, the pv-Band concept accepts a number of process variations in addition to defocus and dose. One of the additional variables to be considered is mask bias. Once mask bias is incorporated into the calculation of the pv-Band, one of the MEEF components (equation 2) is fixed. Therefore, by minimizing ΔCD_{wafer} produced by a fixed ΔCD_{mask} the MEEF value of the layout is minimized. In other words, the layout sensitivity to mask bias variation is reduced.

3.4.4 Critical Failure Optical Rule Check (CFORC)

Critical failure models have the capability to pinpoint regions of the layout that are most likely to fail, but they are limited to single-layer interactions and only two types of failure mechanisms (pinch and bridge). The present method can describe many more types of errors (as indicated in Figure 15) within one layer, but especially between multiple layers.

While CFORC provides an interesting opportunity to reduce the number of simulations needed to detect pinching and bridging problems, it cannot be extended to encompass multiple layers. Because of its empirical nature, it can provide only predictive behavior for processes that are fully qualified and where a CFORC model is available.

3.4.5 Restrictive Design Rules (RDRs)

RDRs provide the directives on how to achieve more manufacturable designs. Such concepts were used during the layout optimization presented in Section 3.1. However, as explained in the introduction of this work, RDRs do not possess any mechanism to grade the design or to identify regions that should be improved.

For that reason RDRs and this method are extremely complementary. The first provides guidance for correcting a problem, while this work provides the detection and scoring infrastructure to identify and sort the problems and their relative impact in the overall manufacturability of the design.

4 Conclusions and Open Areas for Investigation

This work proposes a framework for improving layout manufacturability, and ultimately product yield, by defining a method comprising Objects (which define design intent and process characteristics), Operators (which are functions to extract and combine design intent with process characteristics) and Guidelines (which are the set of best practices and considerations for improving the manufacturability of the layouts).

To develop and prove the validity of this method, three new concepts were developed:

1. Full chip compact model requirements exemplified by a lithography model: Before this work there were two types of process models: fast and accurate compact models that were limited to the prediction of a single-process condition, and physical models that predicted multiple-process conditions but lacked the speed requirements to be used at full chip.

2. Definition of a process variability band (pv-Band): Early attempts at silicon verification used traditional design rules to check for pattern robustness, but they involved design checks for each of the process corners. A pv-Band reduces the number of design rule checks by rendering all relevant information in a single object.

3. Definition of two manufacturability indices: Before this work there was no single metric that was able to relate layout configurations to yield based on inter-layer and intra-layer interactions. These metrics also provide a mechanism to optimize yield during the design stage rather than waiting for marginal improvements after traditional tape-out.

The results indicate that an adequate implementation of the framework has the potential to improve the yield of the designs by increasing their robustness to process variations. In addition, there is a clear link between pattern robustness and parametric behavior. This link can be the object of a different study, but the results presented here indicate the possibility of a unified manufacturability framework that includes electrical and pattern transfer effects.

This framework also frees the layout design team from the need to be proficient in all details of the manufacturing process. Since the models encapsulate the process being used, the output and the way the designer interacts with the process data are independent of the process itself.

Due to its generic nature, this framework can automatically yield designs that are aware of any manufacturing process. The only limitation that prevents extending this framework to other process effects is the availability of compact process models that can capture the main variables of process variability in a fast and reliable compact model.

Plenty of challenges remain for the semiconductor industry. For example, there is a need to characterize and engineer new materials and processes that can surpass heat-dissipation and gate leakage, and to develop new architectures that minimize the impact of interconnect delay or power requirements.

However, as long as the materials and processing techniques rely on production methods similar to those existing today (e.g., lithography, etch and planarization), this proposal should enable design teams to create robust designs capable of withstanding the unavoidable and persistent process fluctuations.

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