

Growth and Characterization of High Permittivity Thin Film Nanolaminates
Fabricated by Atomic Layer Epitaxy

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
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To
my parents
&
my husband

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ABSTRACT

Growth and Characterization of High Permittivity Thin Film Nanolaminates Fabricated by Atomic Layer Epitaxy

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This thesis considers three issues regarding high permittivity thin films and their nanolaminates. Atomic layer epitaxy, the process technique used to deposit thin films of Ta_2O_5 , HfO_2 , ZrO_2 and their nanolaminates will be discussed first. Material properties of these films are presented next. Finally, the electrical properties and dielectric characteristics are investigated.

Atomic layer epitaxy was used to grow binary oxides (Ta_2O_5 , HfO_2 , and ZrO_2) and their nanolaminates (Ta_2O_5 - HfO_2 , Ta_2O_5 - ZrO_2 , HfO_2 - ZrO_2) on silicon substrates. Metallic chlorides and water vapor were used as source materials. The as-deposited Ta_2O_5 , HfO_2 and ZrO_2 thin films grown at 300°C were amorphous. The crystallization temperatures of these films were 800°C , 800°C and 700°C , respectively.

Transmission electron microscope (TEM) showed that silicon surface oxidation occurred during the high permittivity film growth due to the use of water vapor. A thin layer of silicon nitride was grown by rapid thermal nitridation as a barrier layer prior to the deposition of high permittivity films.

Capacitors made with these binary oxides and their nanolaminates were characterized by capacitance – voltage (C-V) and current – voltage (I-V) measurements. Dielectric constants, flatband voltage and interface fixed charges were calculated based on C-V data. Leakage current of nanolaminates was dramatically reduced compared to

that of binary oxides. It was found that Schottky emission and Poole-Frenkel conduction were the major leakage mechanisms. Crystallization of amorphous films had two effects on the dielectric properties. First, it increased the dielectric constant, which was desirable. Secondly, it created grain boundaries that facilitate the current leakage in the dielectric films. As the thicknesses of high permittivity films decreased, the dielectric constants dropped. This reduction in dielectric constant has been shown to depend on the number of atomic monolayers and the atomic polarizability of the film. The investigation of these high permittivity nanolaminates suggested that they could be useful for future gate dielectric material.

Chapter 1

Introduction

The metal-oxide-semiconductor or MOS structure is, without a doubt, the core structure in modern-day microelectronics. Although a quasi-MOS device was first proposed in the 1920s, the metal-oxide-semiconductor fields effect transistor (MOSFET) achieved practical status in 1960, mainly attributed to D. Kahng and M. M. Atalla who filed patents on the Si-SiO₂ based FET [1]. Over the last four decades, the integrated circuit (IC) market has increased dramatically. In 1960s the IC market was broadly based on the bipolar transistors. Since 1970s, however, digital MOS ICs has prevailed. MOSFET and related integrated circuits now constitute about 90% of the semiconductor device market.

Throughout the MOS development history, the quality of the gate SiO₂ and its interface to Si has always been playing an essential role, in both MOS and Dynamic Random Access Memory (DRAMs) [2]. There were strong efforts to obtain a dielectric film superior to the thermally grown SiO₂. They include SiO₂ formed using plasma [3], laser [4], and CVD (Chemical Vapor Deposition) technique [5], Si₃N₄ [6], and ferroelectrics [7]. Such films having other interfaces than thermal SiO₂ to Si, however, suffered from inferior dielectric quality, especially with respect to the defect charge density, and so have not been implemented as gate dielectrics.

Continued Ultra-Large Scale Integration (ULSI: more than 10⁷ transistors on a chip) has been achieved mainly by decreasing the size of an individual transistor as well

as by increasing the chip size and circuit complexity, as typically seen for DRAM whose memory size grows at a rate of approximately four times every three years. The feature size (L) of an individual device continues to decrease to two thirds or a little bit less than that of a prior generation. For example, L was on the order of several micrometers in the 1970s, the decade of Large-Scale Integration (LSI: $10^3 \sim 10^4$ transistors on a chip), while that for the ULSL is now scaled down to $0.25\mu\text{m}$ or less. Accordingly, the thickness of the gate oxides has been reduced from $\sim 100\text{nm}$ in the LSI technology to $\sim 10\text{nm}$ or less for ULSI. As described in the National Technology Roadmap for Semiconductors (Table 1-1), the device dimension will shrink from $0.25\mu\text{m}$ in 1997 to $0.10\mu\text{m}$ in 2005.

Table 1-1 The International Technology Roadmap [8]

Year	1999	2000	2001	2002	2003	2004	2005
Technology Node	180nm			130nm			100nm
DRAM $\frac{1}{2}$ Pitch (nm)	180	165	150	130	120	110	100
MPU Gate Length (nm)	140	120	100	85-90	80	70	65
MPU/ASIC $\frac{1}{2}$ Pitch (nm)	230	210	180	160	145	130	115
ASIC Gate Length (nm)	180	165	150	130	120	110	100

The scaling trends discussed above lead to several limitations and issues of the MOS technology, mainly to (a) small-geometry effects, (b) limited performance under high electrical field, (c) hot-carrier-induced device degradation, (d) gate-induced drain leakage, and (e) gate-dielectric reliability [9]. The limitations (b, c, e) are closely related to the quality of the gate dielectric and its interface to silicon, while the limitations (a, b, d) are more dependent on the gate dielectric thickness. In either case, almost all the limitations become more critical as the gate dielectric thickness is scaled down to

nanometer scale. Generally, increasing internal electric fields will enhance the circuit performance while it degrades reliability. Therefore, trade-off between performance and reliability has become one of the most important device design issues in ULSI technology.

With the continuous shrinkage of the silicon dioxide thickness, direct tunneling current through the dielectric will be a very serious concern. A major limiting factor in transistor scaling beyond the current 0.18- μm design rules has been the difficulty to grow high quality, ultra-thin oxides as the tunneling limit of 2.5nm for SiO_2 is approached and gate currents exceed 1 A/cm^2 . Furthermore, SiO_2 is not a good diffusion barrier for gate electrode dopants, such as boron. Even with nitrogen incorporation [10, 11], it is difficult to utilize ultra-thin nitrided oxides for sub-0.25 μm technologies due to high tunneling current and rough Si- SiO_2 interface. Therefore, a high dielectric constant (k) material of equivalent electrical dielectric thickness is a possible alternative to thermally grown SiO_2 . High k materials [12-14] have been studied for storage capacitors but successful demonstrations for MOSFET are rare [15]. The biggest challenge in DRAM technology is to shrink the size of the memory cell, while maintaining enough capacitance to store a bit. With the traditional SiO_2 as the dielectric, special topologies have to be used to achieve high capacitance and high density. This results in planarization problem and process complexity. Therefore, it is very desirable to replace the current SiO_2 with high permittivity materials.

As a relatively high permittivity material, silicon nitride film has been studied extensively as a gate or capacitor dielectric. It is not used alone but in combination with SiO_2 to form silicon oxynitride [16] or nitride/oxide stack [17]. However, the dielectric constant (7.5~7.8) of silicon nitride is not high enough for future 0.10 μm ULSI devices. According to the National Technology Road Map for semiconductors (1997), gate dielectric scaling down to 2nm is desired from 2006 onward. When the SiO_2 thickness is reduced below 2 nm, alternative high permittivity dielectrics such as Ta_2O_5 , TiO_2 , HfO_2 and ZrO_2 must be considered. Ta_2O_5 has been studied for applications as the capacitor

dielectric in gigabit DRAMs [18-20]. Ta_2O_5 has also been proposed as MOSFET gate dielectric for high-speed circuit in simulation study [21]. Recently MOSFET devices have also been fabricated using high k thin films such as Ta_2O_5 , HfO_2 and ZrO_2 . Some of these results were reported in references [22-25]. One major obstacle in using high k materials is that a solid material with higher permittivity tends to have narrower bandgap. This is deduced from a reduced cohesive force according to the quantum-mechanical consideration [26], thereby suffering from a larger leakage current.

The purpose of this research was to study the deposition of Ta_2O_5 , HfO_2 and ZrO_2 films and their nanolaminates (Ta_2O_5 - HfO_2 , Ta_2O_5 - ZrO_2 and HfO_2 - ZrO_2) using atomic layer epitaxy (ALE) technique and to characterize the material and electrical properties of MOS capacitors made with these films.

This thesis contains 6 chapters including this introduction. In chapter 2, dielectric properties of materials are discussed and the relationship between dielectric constant and bandgap is presented. This chapter also includes basic theory of MOS system and the ULSI device scaling. The ALE technique and its application are described in chapter 3. In chapter 4, the experimental results of the Ta_2O_5 , HfO_2 , ZrO_2 and their nanolaminates by ALE technique are presented. The fabrication sequence and material characteristics are also included in this chapter. Chapter 5 presents material and electrical properties of MOS capacitors built with these high k thin films. C-V characteristics at high frequency were investigated and dielectric constants were extracted from C-V measurement. I-V characteristics were studied to determine the leakage mechanisms and reliability. Argon and oxygen annealing effects on leakage current are described. Summary and conclusions were presented in chapter 6.

References

- [1] M. M. Atalla, E. Tannenbaum, and E. J. Scheibner, "Stabilization of silicon surfaces by thermally grown oxides," *Bell Syst. Tech. J.* **38**, 1959, pp. 749-754.
- [2] P. Singer, "Directions in dielectrics in CMOS and DRAMs," *Semiconductor International* **17**, 1994, pp. 56-59.
- [3] V. K. Bhat, K. N. Bhat, and A. Subrahmanyam, "Electrical characterization of Ultrathin oxides of silicon grown by N_2O plasma assisted oxidation," *J. Electronic Materials* **20**, 2000, pp. 399-404.
- [4] I. W. Boyd, "Incorporation of carbon dioxide laser-grown oxide layers into conventional metal-oxide-silicon devices," *J. Appl. Phys.* **54**, 1983, pp. 3561-3565.
- [5] L. G. Meiners, "Indirect plasma deposition of silicon dioxide," *J. Vac. Sci. Technol.* **21**, 1982, pp. 655-658.
- [6] Y. Kuo, "PECVD silicon nitride as gate dielectric for amorphous silicon thin film transistor," *J. Electrochem. Soc.* **142**, 1995, pp. 186-190.
- [7] J. R. Pfister, *Performance limit of CMOS very large scale integration*, Ph.D. Thesis, Elect. Eng. Dept., Stanford University, Technology Report, No. G541-1 (1984).
- [8] The International Technology Road Map for Semiconductors, Semiconductor Industry Association, San Jose, CA, 1999.
- [9] T. Hori, *Gate Dielectrics and MOS ULSIs*, Springer-Verlag Berlin Heidelberg, 1997, p. 110.
- [10] Y. Yamamoto, T. Ogura, Y. Saito, K. Uwasawa, T. Tatsumi, and T. Mogami, "An advanced 2.5nm oxidized nitride gate dielectric for highly reliable 0.25 μ m MOSFET," *Symp. on VLSI Technology Digest of Technical Papers*, 1997, pp. 45-46.
- [11] X. Guo and T. P. Ma, "Tunneling Leakage current in oxynitride: dependence on oxygen/nitrogen content," *IEEE Electron Device Letters* **19**, June 1998, pp. 207-209.
- [12] M. Hao, K. Lai, W. M. Chen, and J. C. Lee, "Surface cleaning effect on dielectric integrity for Ultrathin oxynitride grown in N_2O ," *Appl. Phys. Lett.* **65**, 1994, pp. 1133-1135.

- [13] Y. Matsui, K. Torri, M. Hirayama, Y. Fujisaki, S. Iijima, and Y. Ohji, "Reduction of current leakage in chemical vapor deposited Ta_2O_5 thin films by oxygen radical annealing," *IEEE Electron Device Letters* **17**, 1996, pp. 431-433.
- [14] S.C. Sun and T. F. Chen, "Leakage current reduction in chemical-vapor deposited Ta_2O_5 films by rapid thermal annealing in N_2O ," *IEEE Electron Device Letters* **17**, 1996, pp. 355-357.
- [15] M. Matsui, H. Hagayoshi, G. Muto, S. Tanimoo, K. Kuroiwa, and Y. Tarui, "Amorphous silicon thin film transistors employing photoprocessed tantalum oxide films as gate insulators," *Jpn. J. Appl. Phys.* **29**, 1990, pp. 62 -66.
- [16] B. Maiti, P. J. Tobin, V. Misra, R. I. Hedge, K. G. Reid, and C. Gelatos, " High performance 20 Å NO oxynitride for gate dielectric in deep sub quarter micron CMOS technology," *IEEE IEDM*, Washington, DC, Dec. 7-10, 1997, pp. 651-654.
- [17] B. Y. Kim, H. F. Luan, and D. L. Kwong, "Ultra thin (<3nm) high quality nitride /oxide stack gate dielectrics fabricated by in-situ rapid thermal processing," *IEEE IEDM*, Washington, DC, Dec. 7-10, 1997, pp. 463-466.
- [18] K. A. Mckinley and N. P. Sandler, "Tantalum pentoxide for advanced DRAM applications," *Thin Solid Films* **290-291**, 1996, pp. 440-446.
- [19] M. B. Lee, H.D. Lee, B.L. Park, U.I.Chung, Y.B. Koh, and M.Y. Lee, "Electrical characterization of CVD TiN upper electrode for Ta_2O_5 capacitor," *IEEE IEDM*, San Francisco, CA, Dec. 8-11, 1996, pp. 683-686.
- [20] S. C. Sun and T. F. Chen, "A new post-deposition annealing method using furnace N_2O for the reduction of leakage current of CVD Ta_2O_5 storage capacitors," *IEEE IEDM*, San Francisco, CA, Dec. 8-11, 1996, pp. 687-690.
- [21] H. Shimada and T. Ohmi, "Current drive enhancement by using high-permittivity gate insulator in SOI MOSFET's and its limitation," *IEEE Trans. Electron Devices* **43**, 1996, pp. 431-435.
- [22] J. L. Autran, R.Devine, C. Chanelieve, and B. Balland, "Fabrication and characterization of Si-MOSFET's with PECVD amorphous Ta_2O_5 gate insulator," *IEEE Electron Device Letters* **18**, 1997, pp. 447-449.
- [23] D. Park, Y. King, Q. Lu, T. King, C. Hu, A. Kalnisky, S. Tay, and C. C. Cheng, "Transistor characteristics with Ta_2O_5 gate dielectric," *IEEE Electron Device Letters* **19**, Nov. 1998, pp. 441-443.

- [24] B. H. Lee, L. Kang, W-J Qi, R. Nieh, Y. Joen, K. Onishi, and J. C. Lee, "Ultrathin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application," IEEE IEDM, Washington, DC, Dec.5-8, 1999, pp. 133-136.
- [25] W. J. Qi, R. Nieh, B. H. Lee, L. Kang, Y. Jeon, K. Onishi, T. Ngai, S. Banerjee, and J. C. Lee, "MOSCAP and MOSFET characteristics using ZrO_2 gate dielectric deposited directly on Si," IEEE IEDM, Washington, DC, Dec.5-8, 1999, pp. 145-148.
- [26] K. W. Boer, Survey of Semiconductor Physics, Van Nostrand Reinhold, 1990, p. 26.

Chapter 2

MOS System and High Permittivity Materials

In this chapter, the history and fundamentals of the metal-oxide-semiconductor structure are reviewed. Basic device physics and device characterization techniques are discussed. Device scaling and demand for high permittivity materials as gate dielectrics are presented as well. This chapter also includes the discussion of dielectric properties of high permittivity materials and their application in ULSI devices.

2.1 MOS system

An MOS structure shown in Fig. 2.1 consists of a top electrode called a gate generally made by vacuum deposition of a metal or by chemical deposition of polysilicon, an oxide layer usually thermally grown, and an ohmic contact to the silicon substrate. An MOS capacitor has only two terminals, and is the simplest and most useful device in the study of semiconductor surfaces and gate dielectrics [1]. A second metallic layer present on the bottom side of the semiconductor provides an electrical contact to the silicon substrate.

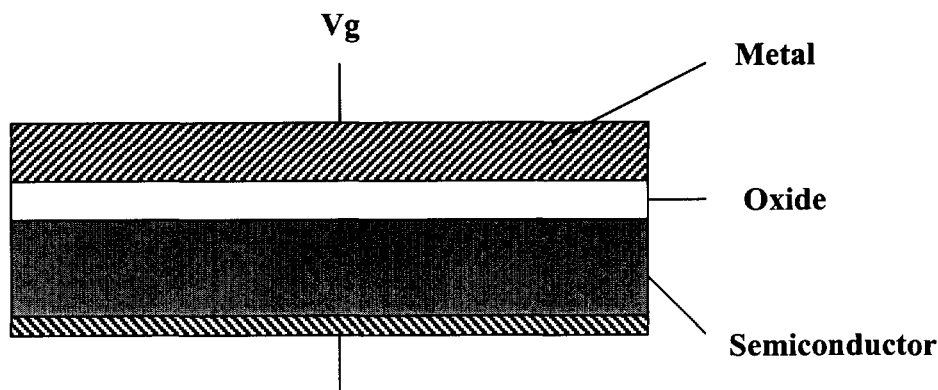


Fig. 2.1 MOS Structure

An ideal MOS structure has the following explicit properties: (1) the metallic gate is sufficiently thick so that it can be considered an equipotential region under ac as well as dc biasing conditions; (2) the oxide is a perfect insulator with zero current flowing through the oxide layer under all static biasing conditions; (3) there are no charge centers located in the oxide or at the oxide-semiconductor interface; (4) the semiconductor is uniformly doped; (5) the semiconductor is sufficiently thick so that, regardless of the applied gate potential, a field-free region (so called Si “bulk”) is encountered before reaching the back contact [2]. With the scaling down of device size, the idealization (2) and (3) have been challenged.

The energy band diagram is an indispensable aid in visualizing the internal status of the MOS structure under static biasing conditions. As schematically illustrated in Fig. 2.2, when an ideal MOS capacitor with a p-type substrate is biased with V_g not equal to zero, basically three situations may arise at the semiconductor surface.

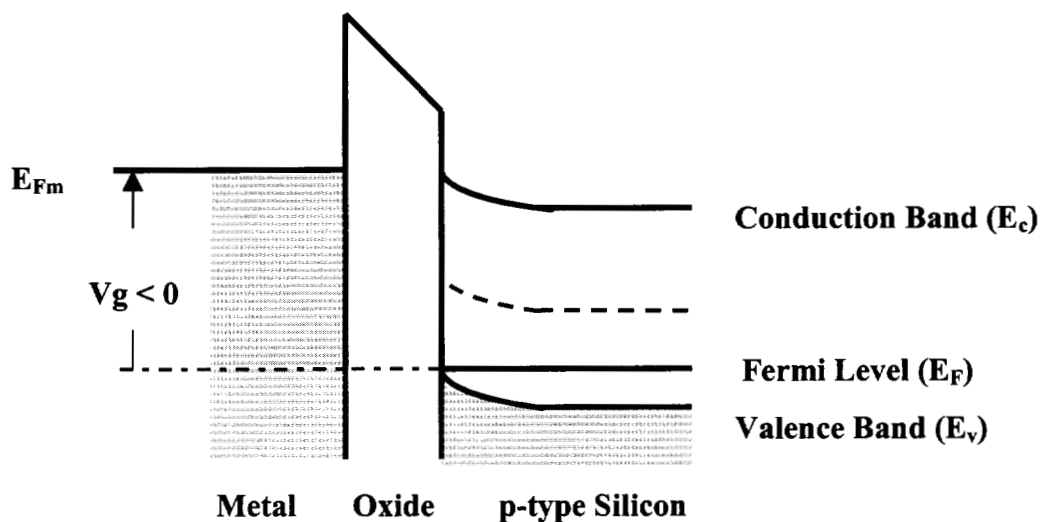


Fig. 2.2a Accumulation region of MOS capacitor

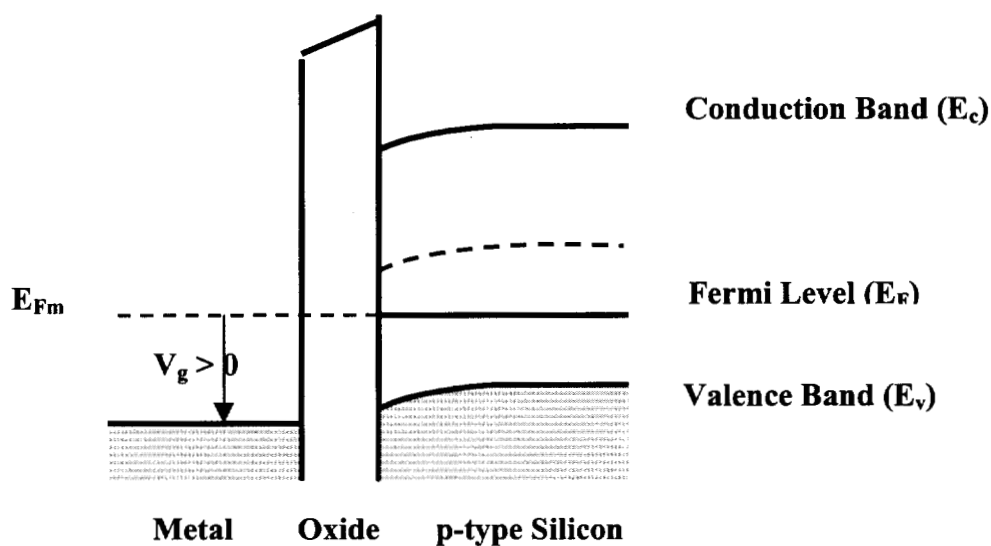


Fig. 2.2b Depletion region of MOS capacitor

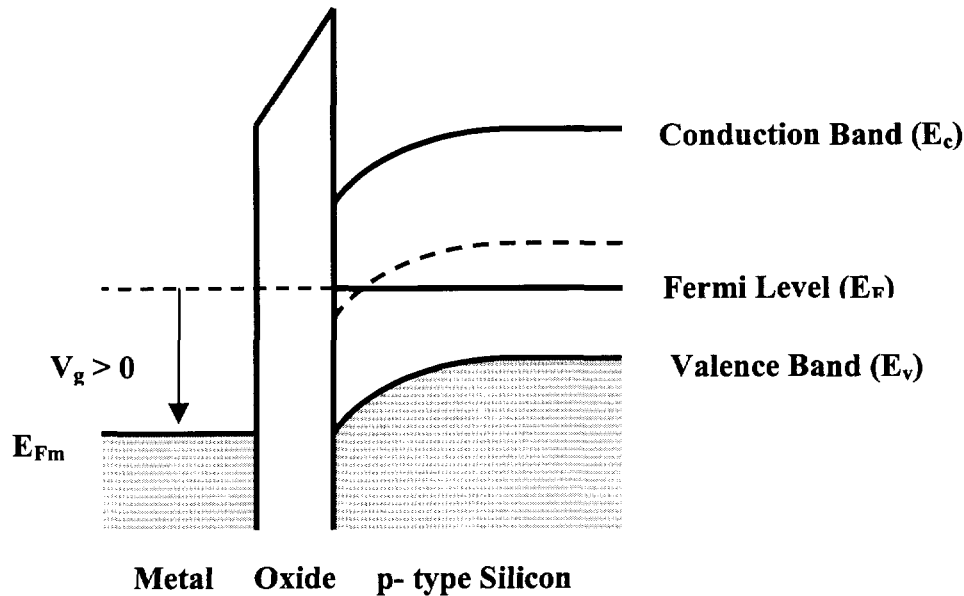


Fig. 2.2c Inversion region of MOS capacitor

Regardless of the gate potential V_g , the Fermi level E_F remains constant throughout the semiconductor since no current flows in the semiconductor. When $V_g < 0$, the negative gate potential attracts positive charges under the interface in the semiconductor (holes in the p-type Si in the case of Fig. 2.2a). This results in an enhanced concentration of majority carriers (holes for p-type substrate), called accumulation, at the interface of oxide and semiconductor. When a positive gate voltage is applied, negative charges are introduced near the semiconductor and oxide interface. This, at first, is due to the holes being pushed away from the semiconductor surface, leaving behind a depletion region consisting of uncompensated acceptor ions as illustrated in Fig. 2.2b. As the positive gate potential increases, the surface depletion region is widened. Accordingly, the total electrostatic potential variation, as represented by the energy band bending, increases so that the midgap energy E_i crosses over the quasi-Fermi level E_F of the semiconductor. Beyond this point, the concentration of

minority carriers (electrons in this case) is larger than that of the majority carriers (holes) near the semiconductor and oxide interface. Therefore, the surface is rich in minority carriers, so called under inversion condition, as shown in Fig. 2.2c. Similar results can be obtained for n-type semiconductors when the gate bias is reversed.

To derive the capacitance – voltage (C-V) characteristics of the MOS structure, we need to develop a relation for the charge in the semiconductor to the surface band bending potential ψ_s . A p-type semiconductor is used to illustrate the C-V characteristics as show in Fig. 2.3. An arrow pointing down represents a positive potential. Band bending potential (ψ) is measured with respect to midgap energy (E_i) as a function of the distance x from the interface of oxide and semiconductor. It is defined to be zero in the bulk of the semiconductor, which indicated that gate voltage drop was only applied across the oxide and the semiconductor surface. The surface potential ϕ is defined as the potential difference between E_i and E_F , and therefore $\psi(x)$ can be expressed as $\phi(x) + \phi_F$. The n and p are given as functions of either $\psi(x)$ or $\phi(x)$ by the following equations:

$$n(x) = N_D \exp (\psi(x) / \phi_t) = n_i \exp (\phi(x)/ \phi_t) \quad (2.1a)$$

$$p(x) = N_A \exp (-\psi(x) / \phi_t) = n_i \exp (-\phi(x)/ \phi_t) \quad (2.1b)$$

where n_i is the intrinsic carrier concentration, $\phi_t = kT/q$ is the thermal voltage (~ 26 mV at room temperature), N_D (N_A) is the donor (acceptor) concentration.

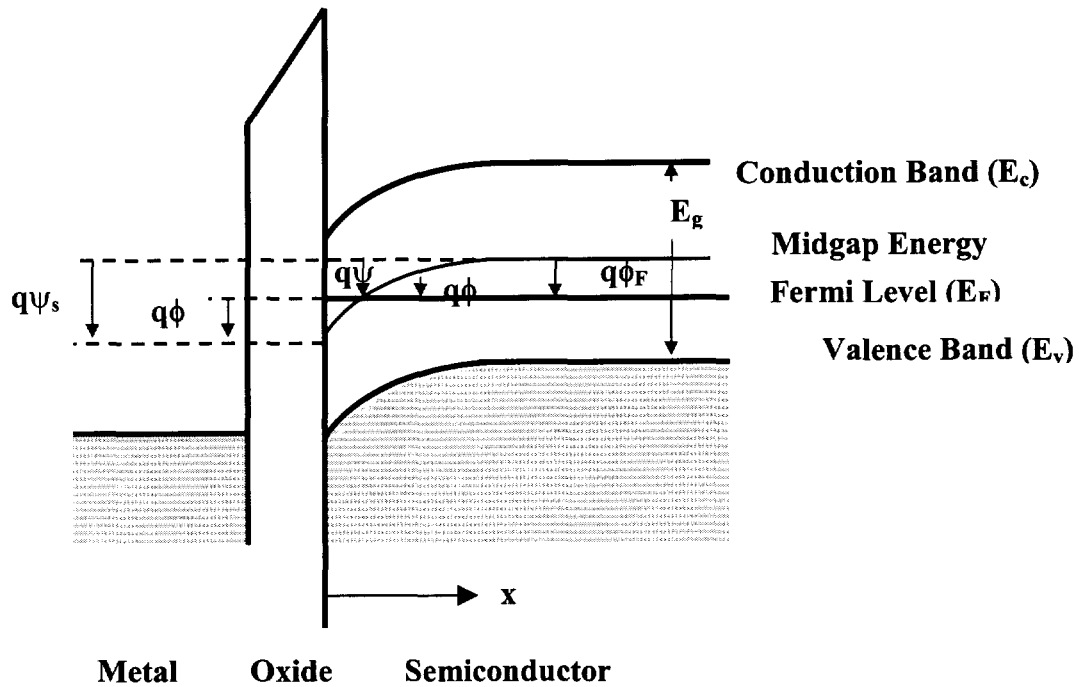


Fig. 2.3 Energy band diagram at the surface of a p-type semiconductor. An arrow pointing down (up) denotes positive (negative) potential. Surface potential ϕ_s is measured with respect to the Fermi level E_F at the interface. Surface band bending ψ_s is measured with respect to the intrinsic Fermi level E_i at the interface.

From the above discussion together with Eqn. 2.1, The following regions of surface band bending potential can be distinguished [3]:

$\psi_s < 0$	Accumulation of holes (bands bending upward)
$\psi_s = 0$	Flat-band condition ($n < p$)
$\phi_F > \psi_s > 0$	Depletion of holes (bands bend downward)
$\psi_s = \phi_F$	Intrinsic condition at surface ($n = p = n_i$)
$2\phi_F > \psi_s > \phi_F$	Weak inversion ($N_A > n > p$)
$\psi_s > 2\phi_F$	Strong inversion ($n > N_A$)

The potential distribution in the semiconductor is described by one-dimensional Poisson equation:

$$\frac{d^2\psi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_s} = -\frac{q}{\epsilon_s} [p(x) - n(x) + N_D - N_A] \quad (2.2)$$

where $p(x)$ and $n(x)$ is the hole and electron concentration in silicon respectively, N_D and N_A are the density of ionized donors and acceptors respectively, ϵ_s is the permittivity of the semiconductor, $\rho(x)$ is the total space-charge density. Integrating Eqn. 2.1 in conduction with Eqn. 2.2 from the bulk toward the surface [4]

$$\int_0^{\psi_s/\phi_t} \frac{\partial \psi}{\partial x} d \left[\frac{\partial \psi}{\partial x} \right] = -\frac{q}{\epsilon_s} \int_0^{\psi_s} [N_A (e^{-\psi/\phi_t} - 1) - N_D (e^{\psi/\phi_t} - 1)] d\psi \quad (2.3)$$

gives the relation between potential ψ and the electric field E :

$$E = -\frac{\partial \psi}{\partial x} = \pm \sqrt{2} \frac{\phi_t}{L_D} F(\psi, N_A) \quad (2.4)$$

with the positive sign for $\psi > 0$ and the negative sign for $\psi < 0$. The extrinsic Debye length L_D which is a characteristic length of semiconductors, and $F(\psi, N_A)$ are defined as

$$L_D = \sqrt{\frac{\epsilon_s \phi_t}{q N_A}} \quad (2.5a)$$

$$F(\psi, N_A) = \sqrt{e^{-\psi/\phi_t} + \psi/\phi_t - 1 + (n_i/N_A)^2 (e^{\psi/\phi_t} - \psi/\phi_t - 1)} \quad (2.5b)$$

At thermal equilibrium the depletion layer width of abrupt junction is about $8L_D$ for Si. The surface electric field E_s is given by substituting ψ_s for ψ into Eqn. 2.4. By

Gauss's law, the total charge Q_s per unit area in the semiconductor required to produce the field E_s is:

$$Q_s \equiv -\epsilon_s E_s = \mp \sqrt{2} \frac{\epsilon_s \phi_t}{L_D} F(\psi_s, N_A) \quad (2.6)$$

The differential capacitance of the semiconductor is given by:

$$C_s \equiv \frac{\partial Q_s}{\partial \psi_s} = \frac{\epsilon_s}{\sqrt{2} L_D} \frac{|1 - e^{-\psi_s/\phi_t} + (n_i/N_A)^2 (e^{\psi_s/\phi_t} - 1)|}{F(\psi_s, N_A)} \quad (2.7)$$

The total capacitance C of a MOS system is a series combination of insulator capacitance C_i and the semiconductor capacitance C_s :

$$C = \frac{1}{1/C_i + 1/C_s} \quad (2.8)$$

C_i is the oxide capacitance per unit area:

$$C_i = \frac{\epsilon_i}{t_i} \quad (2.9)$$

where ϵ_i is the permittivity of the insulator (oxide in most cases) and t_i is the thickness of the insulator. When a gate voltage is applied to the MOS structure, the ideal MOS capacitance – voltage (C-V) characteristics for a p-type semiconductor can be described by the C-V curves at high- and low-frequency conditions as shown in Fig. 2.4.

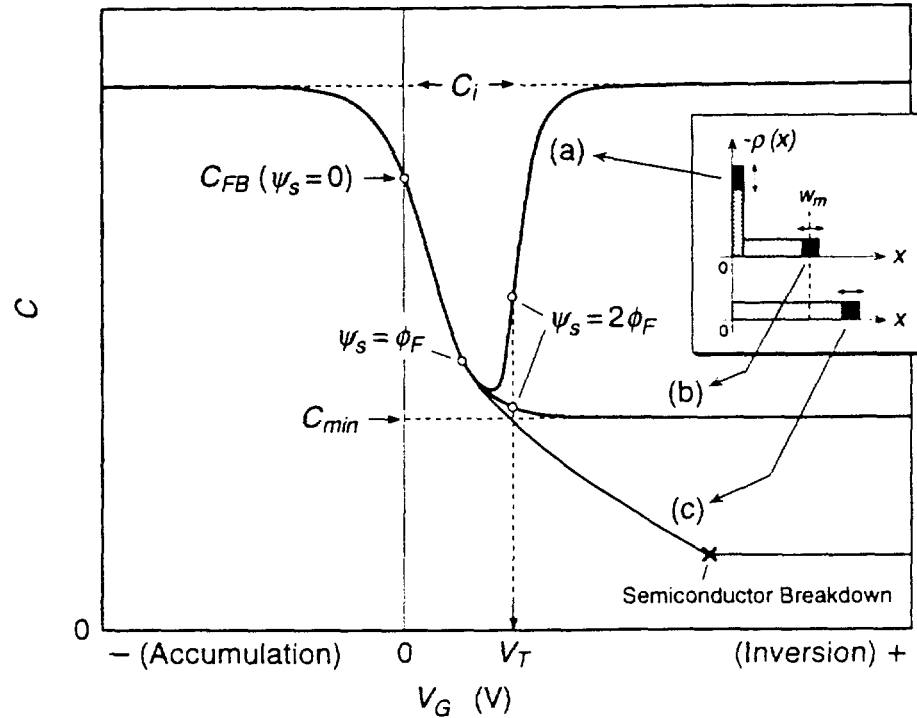


Fig. 2.4 MOS capacitance-voltage characteristics under (a) low frequency, (b) high-frequency, and (c) deep-depletion conditions
[5]

For the low frequency C-V curve (a) in Fig. 2.4, accumulation of holes occurs with a negative gate bias ($V_g < 0$) and Q_s (hole charge in this case) dominates. Therefore the differential capacitance of the semiconductor C_s is much larger than the capacitance of the insulator C_i . As a result, the total C of the MOS is close to its maximum C_i . As V_g is increased to be slightly positive, a depletion layer, which may act as a dielectric layer of thickness w in series with the insulator, forms and widens near the semiconductor surface. Therefore the total capacitance C decreases substantially according to

$$C = \frac{1}{t_i / \epsilon_i + w / \epsilon_s} \quad (2.10)$$

As V_g is further increased to exceed the so called threshold voltage V_t at which strong inversion occurs ($\psi_s \approx 2\phi_F$), total capacitance C increases again after showing a minimum and then approaching the maximum C_i , since the charges Q_s in the inversion layer of semiconductor increases dramatically by a slight increase of the surface band bending potential ψ_s . Once strong inversion occurs, w reaches its maximum w_m . Simplifying F in Eqn. 2.5b by expressing it only through the second term and equating Q_s at $\psi_s \approx 2\phi_F$ with Eqn. 2.6 to $Q_D = qN_A w_m$, w_m is given by:

$$w_m \approx \sqrt{\frac{2\epsilon_s 2\phi_F}{qN_A}} = 2\sqrt{\frac{\phi_F}{\phi_t}} L_D \quad (2.11)$$

To measure the differential capacitance, the AC signal of small amplitude δV with the angular frequency ω ($\omega = 2\pi f$, f being frequency) is superimposed onto the DC voltage V_g . Comparing the curves a and b in Fig. 2.4, it should be noticed that the increase of capacitance in inversion region occurs at low frequencies where the recombination-generation rates of minority carriers can keep up with the small signal variation and lead to charge exchange with the inversion layer. These minority carriers will contribute an additional capacitance C_{it} to the measured low frequency C-V curve. At low frequencies, the C-V characteristics are represented by the equivalent circuit in Fig. 2.5. The total capacitance can be calculated using Eqn. (2.12).

$$\frac{1}{C_{LF}} = \frac{1}{C_i} + \frac{1}{C_s + C_{it}} \quad (2.12)$$

At higher frequencies, interface traps lag behind the small-signal AC change with the minority-carrier response time. The capacitance at high frequency can be given by:

$$C_{HF} = \frac{C_i C_s}{C_i + C_s} \quad (2.13)$$

This capacitance corresponds to the equivalent circuit shown in Fig. 2.6.

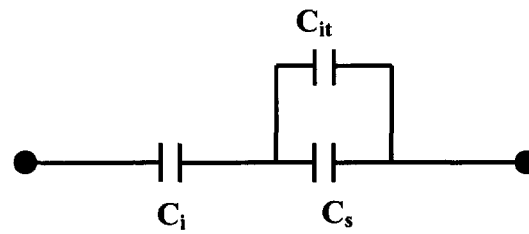


Fig. 2.5 Low frequency equivalent circuit of the MOS

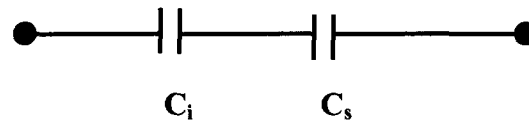


Fig. 2.6 High frequency equivalent circuit of the MOS capacitor

An experimental set of low frequency C-V data is shown in Fig. 2.7. It is obvious that for this Si-SiO₂ system the onset of low frequency curves occurs at $f \leq 100$ Hz.

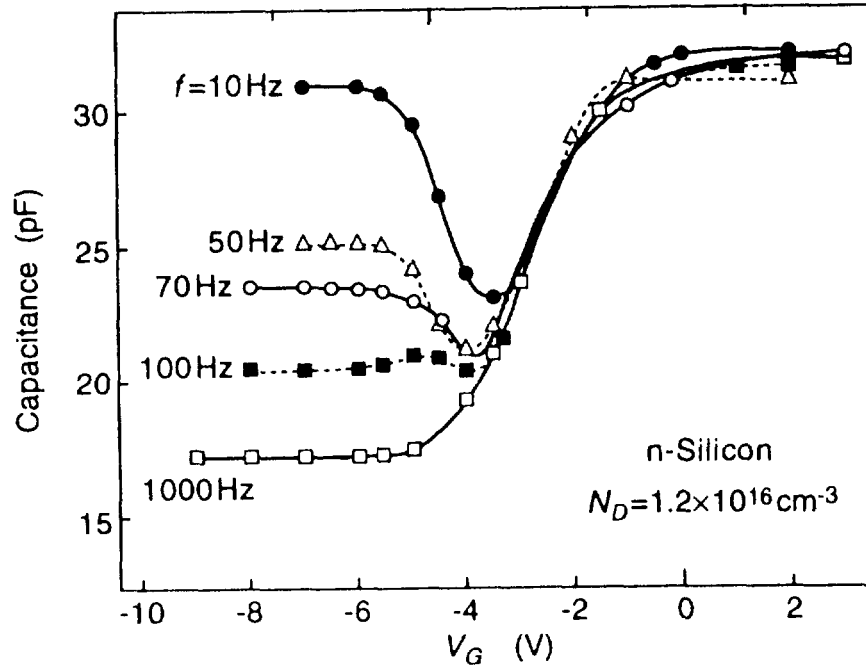


Fig. 2.7 MOS C-V curves measured at room temperature with frequency as a parameter . The substrate is n-type.
[6]

The capacitance-voltage characteristics of an ideal MOS structure vary not only with the frequency but also the thickness of the oxide layer and the doping concentration of the substrate. As the thickness d is made thinner or the substrate doping is made lighter, a large variation of capacitance is observed, as illustrated in Fig. 2.8. In these figures, the dielectric constant k ($= \epsilon_i / \epsilon_0$) of SiO_2 is approximately three times smaller than that of silicon (~ 11.8), ϵ_0 being the permittivity of vacuum. In order to replace another insulator for SiO_2 , simply replace its physical thickness t with an electrically equivalent thickness of SiO_2 , $t_{eq,ox}$ defined as

$$t_{eq,ox} = \frac{\epsilon_{ox}}{\epsilon_i} t = \frac{3.9}{\epsilon_i / \epsilon_0} t \quad (2.14)$$

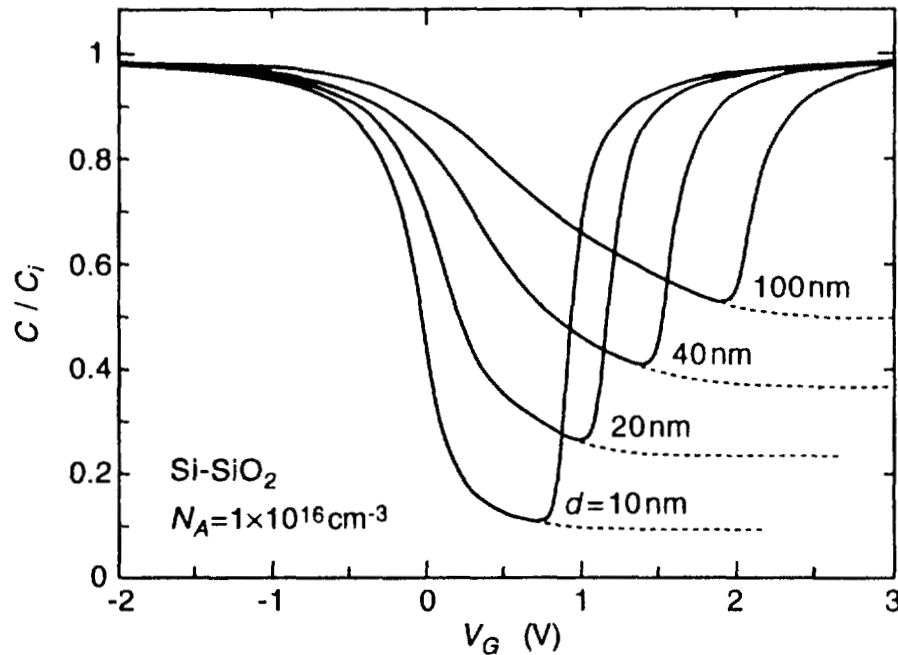


Fig. 2.8 MOS C-V characteristics as a function of the oxide thickness. Solid lines correspond to low frequency and dashed lines represent high frequency. The substrate is p-type silicon.

[7]

2.2 Charges in a MOS system

An ideal MOS capacitor does not contain any defect charges. However, for a real MOS capacitor there exist different defect charges especially near the Si-SiO₂ interface where the chemical composition is considered not to be stoichiometric (SiO_x: $x < 2$) unlike in the bulk. As shown in Fig. 2.9, there are four distinct types of charges in the Si-SiO₂ system: Q_f the fixed charges, located very near the interface but can not exchange charges with the semiconductor; Q_{it} the interface –state charges, located very close to the

interface and have energy states close to the Fermi level (E_F) within the forbidden bandgap as to be able to exchange charges with the semiconductor; Q_{ot} oxide trapped charges, the trap sites are distributed throughout the bulk of the oxide; Q_m mobile ionic charges, results from alkali-metal ions (mainly sodium) that are easy to be absorbed in the oxide under bias-temperature aging conditions. Among the four kinds of charges, Q_f causes the parallel shift ΔV along the V axis in a C-V curve, i.e.

$$\Delta V = -\frac{Q_f}{C_i} = -\frac{Q_f t_i}{\epsilon_i} \quad (2.15)$$

where t_i is the thickness of insulator (oxide) and ϵ_i is the permittivity of the insulator.

The effects of Q_{it} on C-V curve are more complicated. Q_{it} will not simply shift the C-V curve in parallel but stretch them out, because the interface states occupancy varies with the gate bias. Since the interface state levels are distributed across the energy band gap, the interface state density is described as $D_{it} \equiv \partial N_{it} / \partial E$ in units of cm^{-2}/eV . There are two types of interface states, acceptor type and donor type. Acceptor -like interface states are negative when filled with electrons and neutral when empty, whereas donor-like ones are neutral when filled and positive when empty. It is generally considered that interface states above the midgap energy are acceptor type while those below midgap are donor type. An interface state can interact with the silicon conduction band by capturing or emitting an electron and with the silicon valence band by capturing or emitting a hole.

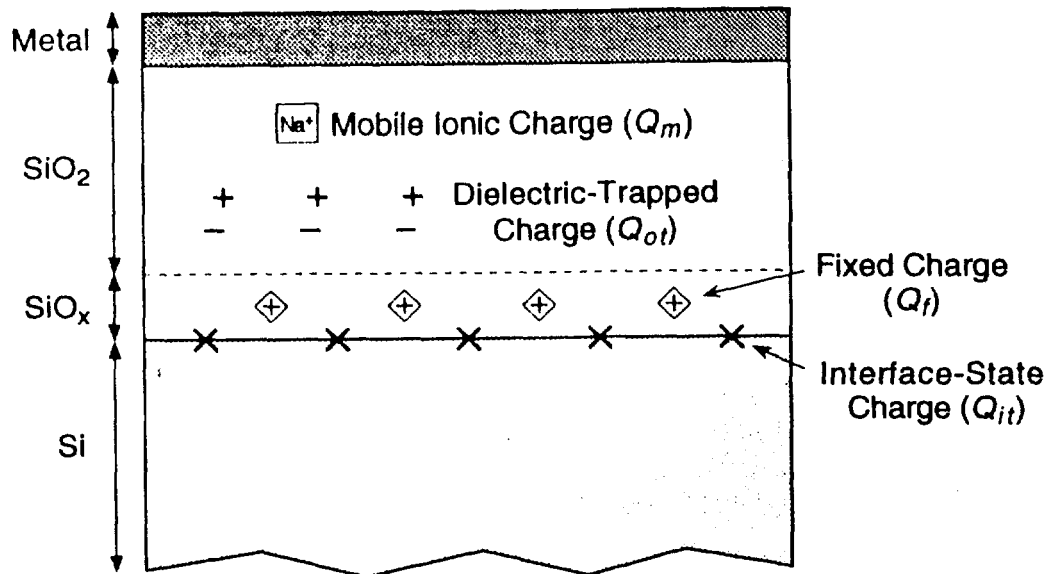


Fig. 2.9 Four categories of oxide charges in the MOS system.
[8]

Interface states can be extracted from capacitance, conductance and sub-threshold measurements. Terman used the theoretical and measured high frequency C-V data to extract the interface state density [9]. The interface state density can also be obtained from the low frequency C-V measurement, a technique developed by Berglund [10]. The difference of the theoretical and measured low frequency C-V curve is due to the interaction of interface states with the silicon substrate. Castagne and Vapaille proposed a method to calculate interface state density using both high frequency and low frequency C-V data [11]. The conductance method, proposed by Nicollian and Goetzberger in 1967, is considered the most sensitive approach to determine D_{it} [12]. It is based on the measurement of the equivalent parallel conductance G_p of a MOS capacitor as a function of bias and frequency. The charge pumping method, originally proposed by Brugler in 1969 [13], is suitable for interface states measurement on small geometry MOSFET's

states distribution from the charge pumping effects [14]. The advantage of charge pumping method is the direct measurement of the current that is proportional to D_{it} and the fact it can be used to measure regular MOSFET devices without preparing extra test structures.

2.3 Carrier transport in dielectric films

The conductance of an insulating thin film is assumed to be zero in an ideal MOS structure. Real insulators, however, show carrier conductance when the electric field or temperature is sufficiently high. An estimation of the relationship between electric field and the permittivity can be obtained from

$$E_i \epsilon_i = E_s \epsilon_s \quad (2.16)$$

where E_i and E_s are electric fields in insulator and semiconductor, respectively, and ϵ_i and ϵ_s are the corresponding permittivities. For the Si-SiO₂ system, the field for silicon at avalanche breakdown is about 3×10^5 V/cm, the corresponding field in oxide is about three time larger ($\epsilon_{Si}/\epsilon_{SiO_2} = 11.9/3.9$), that is, about 10^6 V/cm. Under such an electric field, the conduction of electron and hole in the oxide film is negligible even at elevated temperatures. However, when sufficiently high electric fields E (V/cm), are applied to dielectric films, the response is passage of a current density j (A/cm²). If E is small, the response is linear or ohmic, and the conductivity (σ), given by j/E , is independent of E . For larger applied fields the j - E relationships defining charge transport through dielectric films are more complex. Depending on the mechanism, the conduction process is described in Table 2-1 [15]. In most cases the magnitude of j is strongly temperature-dependent according to Maxwell-Boltzmann relationship.

Table 2-1 Conduction processes in dielectric films

Process	j-E relationships	Voltage(V), Temperature(T) dependence
1.Schottky emission	$j = A^* T^2 \exp \left[\frac{-q(\Phi_B - (qE/(4\pi\epsilon_i))^{1/2})}{kT} \right]$	$\approx T^2 \exp \left[\frac{+aV^{1/2} - b}{T} \right]$
2. Frenkel-Poole emission	$j = B \exp \left[\frac{-q(\Phi_B - (qE/(\pi\epsilon_i))^{1/2})}{kT} \right]$	$\approx V \exp \left[\frac{+a'V^{1/2} - b}{T} \right]$
3. Tunneling	$j = \frac{CE^2}{\Phi_B} \exp \left[-\frac{8\pi(2m)^{1/2}(q\Phi_B)^{3/2}}{3hqE} \right]$	$\approx V^2 \exp(-\frac{c}{V})$
4.Space-charge- limited	$j = \frac{4\epsilon_0(2q/m)^{1/2}}{9} \frac{E^{3/2}}{t^{1/2}}$	$\approx V^{3/2}$
5.Ohmic (intrinsic)	$j = ET^{3/2} \exp \left[-\frac{E_g}{2kT} \right]$	$\approx VT^{3/2} \exp \left[-\frac{eE_g}{T} \right]$
6.Ionic conduction (low field)	$j \approx \frac{E \exp[-E_a/kT]}{T}$	$\approx \frac{V \exp(-E_a/T)}{T}$
7.Ionic conduction (high field)	$j \approx \sinh[qaE/kT] \exp[-E_a/kT]$	$\approx \sinh(gV/T) \exp(-hE_a/T)$

A^* = Richardson constant, Φ_B = barrier height, E = electric field, ϵ_i = insulator dielectric constant, ϵ_0 = permittivity of free space, m = effective electron mass, t = insulator thickness, h = Planck's constant, E_g = insulator energy gap, E_a = activation energy for ion creation and motion. Constants B , C , a , a' , b , c , e , and f are independent of V .

The Schottky emission process is similar to the current transport in the metal-semiconductor contacts that is mainly due to (1) majority carriers transport from the metal over the potential barrier into the semiconductor at moderate temperatures (e.g., 300K). The other contributions to carrier transport from thermionic emission across the metal-insulator interface or the insulator-semiconductor interface are (2) quantum-mechanical tunneling of electrons through the barrier, (3) recombination in the space-charge region and (4) electron injection from the metal to the semiconductor under negative gate bias. Fig. 2.10 shows the transport processes in the Schottky emission under forward bias. A plot of $\ln(J)$ versus \sqrt{E} yields a straight line where E is the electric field and J is the current density. Meanwhile, a plot of $\ln(J/T^2)$ versus $1/T$ would also show a straight line where T denotes the temperature.

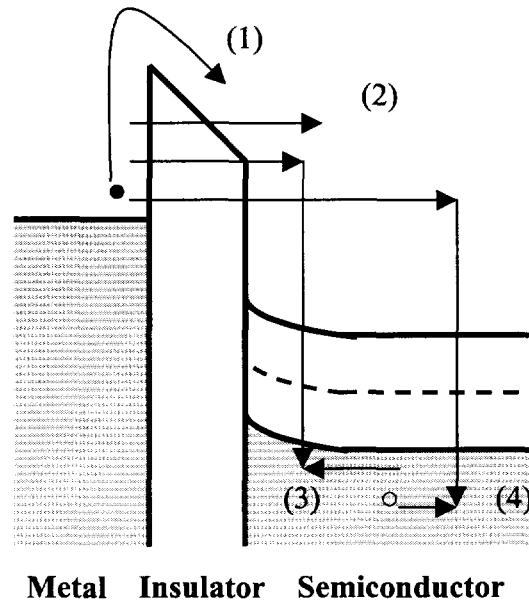


Fig. 2.10 Four basic transport processes in Schottky emission.
[16]

The Frenkel-Poole emission, shown in Fig. 2.11, is due to the field-enhanced thermal excitation of trapped electrons into the conduction band. For trap states with coulomb potentials, the expression is virtually identical to that of the Schottky emission. The barrier height is the depth of the trap potential well. The tunneling is caused by the field-assisted electron emission into the conduction band or by electrons tunneling from metal Fermi level into the insulator conduction band. The tunneling process is substantially

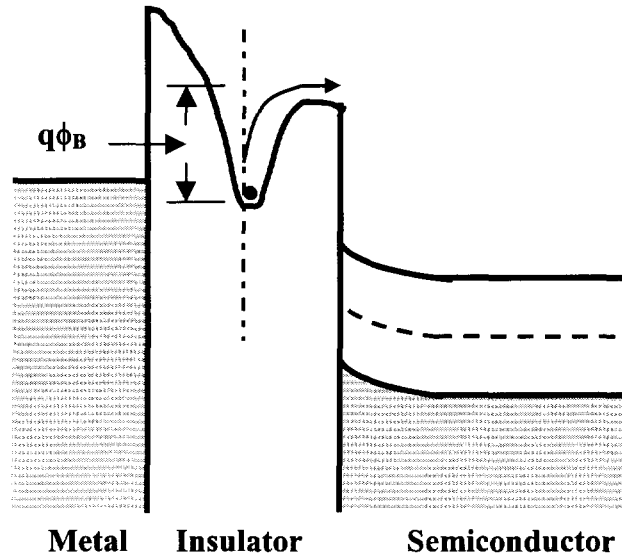


Fig. 2.11 Illustration of Frenkel-Poole emission. ϕ_B is the barrier height.
[17]

dependent on the applied voltage and independent of the temperature. Fowler-Nordheim tunneling occurs at a large electric field above 6-7 MV/cm. If electric field E_i is further increased beyond 10~12 MV/cm, depending on the dielectric film thickness, dielectric breakdown occurs. When the thickness of dielectric films is reduced to 4~5nm, direct

tunneling becomes dominant. The tunneling processes are shown in Fig. 2.12. A simple criterion that direct tunneling occurs is that:

$$V_i \equiv E_i t < \Phi_B \quad (2.17)$$

which means that electrons go into the conduction band of silicon rather than of SiO_2 . V_i is the potential across the oxide layer of thickness t . Φ_B is the barrier potential from metal to oxide. Substituting $\Phi_B = 3.2$ V and $E_i = 7$ MV/cm for the onset of F-N tunneling into Eqn. 2.17, for example, we approximately find for the Si- SiO_2 system that direct tunneling is dominant when the dielectric thickness is less than 4.5 nm. This agrees with the experimental observations. Due to the mechanism of direct tunneling, it has much smaller dependence on the gate voltage V_g compared to the F-N tunneling. Therefore, the current in such a low- V_g range at which MOSFET's are operated in practice is undesirably increased, setting a fundamental constraint on MOS technology.

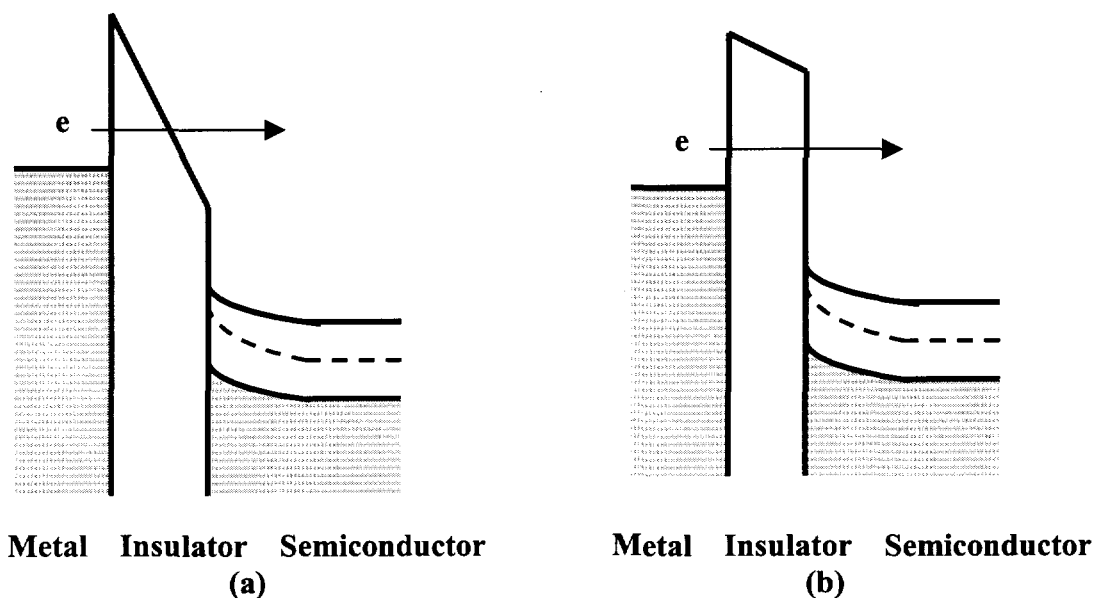


Fig. 2.12 Diagram of tunneling processes in insulating films. (a) Direct Tunneling (b) Fowler-Nordheim Tunneling

The space-charge-limited current is due to the carriers injected into the insulator, where no compensating charge is present. At low voltage and high temperature, conduction current is formed by thermally excited electrons hopping from one isolated state to the next, this leads to an ohmic characteristic exponential dependence on temperature. The ionic conduction is similar to diffusion processes. The dc ionic conduction is not obvious during the time the voltage is initially applied since ions can not be readily injected or extracted from the insulator. After the initial current flow, positive and negative space charges will build up at the metal-insulator and insulator-semiconductor interfaces, causing a distortion of the potential distribution. As the voltage is removed, large internal fields remain which cause some ions to flow back to their equilibrium position.

Intrinsic tunneling and leaky paths due to neutral trapping centers created by plasma exposure are the major leakage mechanisms in MOS devices with untrathin oxide [18]. Thin gate oxides are subjected to plasma process induced charging damage since so many plasma steps are used and plasma damage is cumulative. Plasma charging may cause electrical stress of the gate oxide that can result in reduced device yield. When charging stress is milder, interface traps are generated and the characteristics of MOS devices may exhibit a higher range of variability. Reliability of devices is also degraded. The nature of the oxide degradation under plasma charging relies on the Fowler-Nordheim (F-N) current being forced through the thin oxide layer under electrical stress. Degradation of the gate oxide leakage depends on bias polarity, temperature, and gate material such as boron or phosphor doped poly silicon gates. The Stress-Induced-Leakage-Current (SILC) in gate oxide has been studied extensively since it may impose constraints on dielectric thickness scaling. It was reported that for stress voltage below 5 V and for gate oxide thickness less than 3.5 nm, SILC is caused by tunneling via interfacial traps, rather than through bulk oxide traps [19].

2.4 MOSFET Transistor

MOSFET transistor is a four-terminal structure including gate, substrate, source and drain, as shown in Fig. 2.13. There are two types of transistors based on the carriers in the channel: n-type (n-channel) and p-type (p-channel). In this section, operation theory and equations of n-channel on p-type substrate are discussed. Similar results can also be applied to p-channel device with corresponding polarity modifications.

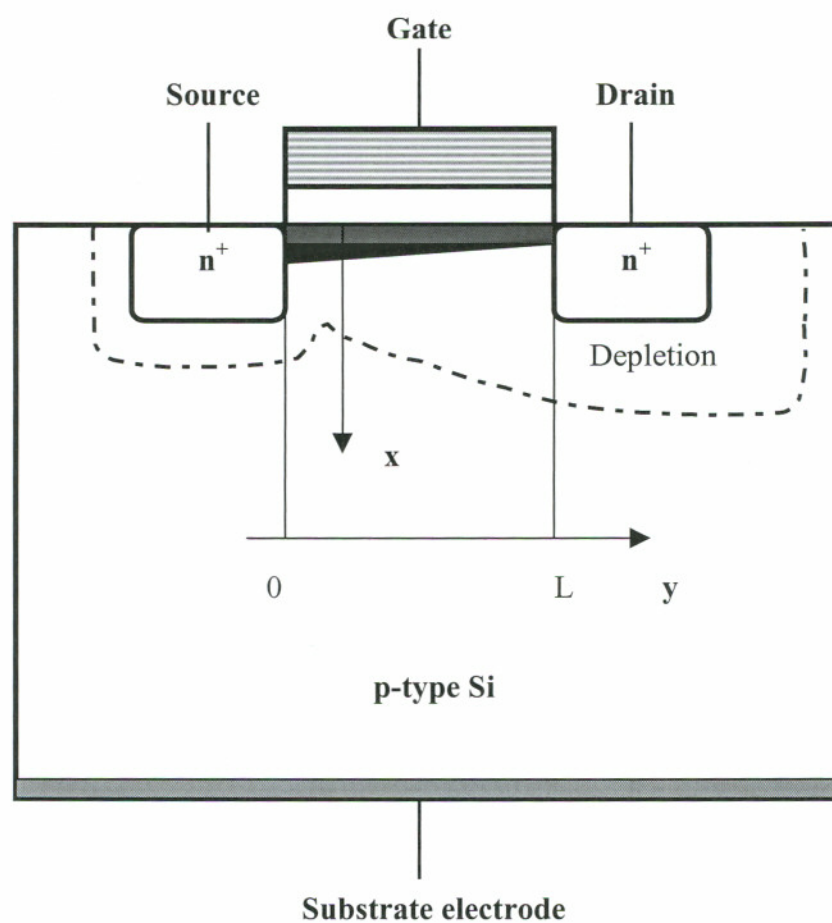


Fig. 2.13 Cross section of a MOSFET

When the gate voltage V_g is larger than the threshold voltage V_{th} , electrons in the substrate will be attracted to the semiconductor surface, forming so called n-channel underneath the gate oxide. The potential difference between source and drain will cause electrons in the n-channel to drift from source to drain therefore current flows through the channel. The threshold voltage is an important parameter for the MOSFET device. It is the minimum gate voltage needed to turn on the transistor. The threshold voltage for large-geometry devices on uniformly doped substrates with no short- or narrow-channel effects is given by

$$V_{th} = V_{FB} + 2\phi_F + \frac{\sqrt{2q\epsilon_{Si}N_A(2\phi_F)}}{C_i} \quad (2.18)$$

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \quad (2.19)$$

where V_{FB} is the flat band voltage, substrate and source are both grounded. The threshold voltage for non-uniformly doped, ion-implanted devices depends on the implant dose as well. C_i is the gate dielectric capacitance, which increases with the reduction of gate dielectric thickness. Additional corrections are needed for short- or narrow-channel devices. The charges that exist at interface of semiconductor and oxide will also cause a shift of the threshold voltage. In this case, the threshold voltage can be expressed as

$$V_{th} = V_{FB} + 2\phi_F + \frac{\sqrt{2q\epsilon_{Si}N_A(2\phi_F)}}{C_i} + \frac{Q_{it} + Q_{ot}}{C_i} \quad (2.20)$$

where Q_{it} are the interface charges and Q_{ot} are the oxide trapped charges. The scaling of oxide thickness results in an increase of oxide capacitance. Therefore, the threshold voltage could be reduced.

As a large enough gate voltage is applied to the MOSFET device, an n-type inversion layer will be formed and electrons in this n-channel will flow from source to drain with $V_D > 0$. There are two cases of small and large V_D to be considered. For a small V_D , inversion layer charges are uniformly distributed under the gate oxide and current flows through the conducting channel. The channel acts as a resistor in this case so that the drain current increases proportionally to V_D . This is called linear region. As V_D is further increased, electrons in the inversion layer close to the drain end will be attracted to the drain and this region will be depleted of mobile electrons. Therefore the channel resistance will be increased until eventually the inversion layer charge becomes zero (called pinchoff) at the drain end. V_D at which saturation occurs is denoted by the saturation drain voltage V_{Dsat} . Once V_D exceeds the saturation voltage, the pinchoff point will move towards the source end leaving a depletion region behind at the surface. The drain current will eventually remain constant I_D because it depends on the voltage drop (fixed at V_{Dsat}) inside the channel. This region is called saturation.

To derive the I_D - V_D characteristics, only drift current is considered for simplicity. The mobility is assumed to be constant throughout the channel. Integrating the equation for current density J (v_d : drift velocity of the electrons) [3]

$$J = -qn(x)v_d \quad (2.21)$$

from the surface towards the point $x = x_1$ at which the intrinsic Fermi level E_i intersects E_{Fn} gives

$$I_D = WQ_I\mu_n E_{\parallel} = -WQ_I\mu_n \partial V / \partial y \quad (2.22)$$

where $E_{\parallel} \equiv -\partial V / \partial y$, W is the width of the channel, and Q_I is the inversion charge per unit area defined by

$$Q_I = - \int_0^{x_I} qn(x)dx \quad (2.23)$$

There are several methods to calculate the Q_I in Eqn. 2.23. Some approaches are very complicated and time-consuming. Usually a gradual-channel approximation is used ($V_D \ll 2\phi_F$, in this case) and a simple drain current calculation yields

$$I_D = \frac{W}{L} \mu_n C_i (V_g - V_{th} - V_D / 2) V_D \quad (2.24)$$

where the threshold voltage V_{th} is given by

$$V_{th} = 2\phi_F + \frac{1}{C_i} \sqrt{2\varepsilon_s q N_A \cdot 2\phi_F} = 2\phi_F + K \sqrt{\phi_i \cdot 2\phi_F} \quad (2.25)$$

K is a characteristic ratio of semiconductor capacitance to the gate dielectric capacitance C_i defined by

$$K = \frac{\sqrt{2\varepsilon_s}}{C_i} \frac{1}{L_D} = \frac{\sqrt{2\varepsilon_s q N_A / \phi_i}}{C_i} \quad (2.26)$$

which includes the Debye length L_D as described in Chapter 2.1. Eqn. 2.24 reflects the drain current in the so-called linear region. In this region, for a given gate voltage V_g , I_D first increases linearly with V_D , then gradually levels off, and reaches its maximum I_{Dsat} at V_{Dsat} . Solving $\partial I_D / \partial V_D = 0$ with Eqn. 2.24 produces

$$V_{Dsat} = V_g - V_{th} \quad (2.27)$$

I_{Dsat} is then obtained by substituting Eqn. 2.27 into Eqn. 2.24,

$$I_{Dsat} = \frac{W}{L} \mu_n C_i \frac{(V_g - V_{th})^2}{2} \quad (2.28)$$

which is used to describe I_D with $V_D > V_{Dsat}$. A typical $I_D - V_D$ curve is shown in Fig. 2.14.

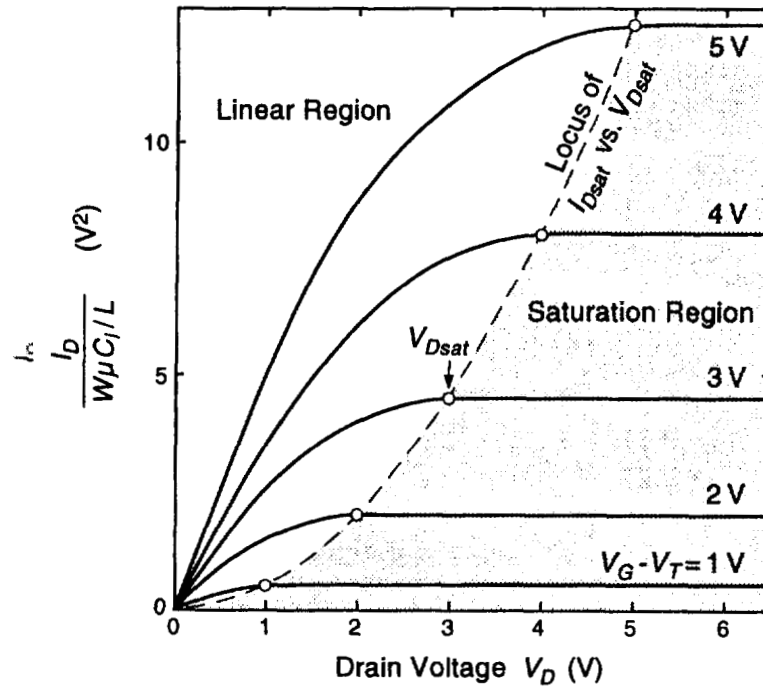


Fig. 2.14 Idealized saturation characteristics (I_D vs. V_D) of an n-channel MOSFET. The dashed line indicates the locus of I_{Dsat} vs. V_{Dsat} .

[3]

According to the drain current expression in the linear region, I_D should be zero for $V_g < V_{th}$. This is because when the drain current was explored, only drift current was considered. In reality, there will be a current flow in the channel even gate voltage is

smaller than the threshold voltage. Unlike the drift current in the strong inversion, the subthreshold current I_D in weak inversion is dominated by diffusion due to the difference between the electron density at the source and drain. This current is especially important for low-voltage, low-power applications such as CMOS logic and DRAM memory devices.

2.5 Scaling issues and limitations

Scaling down or shrinking of the device size has been extensively used to improve device and circuit performance. This enhanced performance includes a faster switching speed, low power dissipation, smaller device and circuit areas and high capacity of integration. The initial scaling concept, the constant – field scaling law, was proposed by IBM researchers [20] in mid 1970s to keep the internal electric fields constant by reducing all geometry factors and voltage by the single scaling factor λ as shown in Table 2-2. The geometric factors include the channel length L , channel width W , source/drain junction depth x_j , and the gate dielectric thickness d . The doping density N_B is increased by λ so that the depletion layer depth is reduced by λ , under the biases reduced by λ . Therefore, undesirable two-dimensional effects such as short channel effects remain under control. The scaling reduces the drain current drive I_D by λ , the switching delay by λ , and the power dissipation by λ^2 . This theory was confirmed by the successful fabrication of 1- μm channel MOSFET showing the proper characteristics as expected with respect to traditional 5- μm technology.

Since then, the constant –field scaling law has acted as a concise guide for device shrinking. However, as devices continue to be scaled down to deep-submicrometer, the constant-field scaling law can not hold any more. In particular, the voltage for the above 1- μm MOSFET device was already reduced to 1 V. Therefore, in the mid 1980s, the IBM researchers modified their theory [21] to the generalized scaling law that reduces the

voltage by a factor κ generally smaller than the factor λ . By resetting the starting voltage to 2.5V for the 1- μm channel FET, it was demonstrated that a 1/4- μm channel FET with $d = 5 \text{ nm}$ ($\lambda = 4$) operates well under a reduced bias ($\kappa = 2.5$) of 1 V. The generalized design does not require major modifications of the state-of-art MOS technology since $\kappa < \lambda$, but it requires an evolution toward much thinner gate dielectrics and the proportionally reduced fabrication tolerance since thickness of gate dielectric d is reduced by the same factor λ .

In practice, several limitation factors restrict the voltage to be scaled as much as the device dimensions. The temperature deviation of V_{th} leads to large threshold fluctuation if extended operation temperatures would be used, i.e. from -55°C to $+135^\circ\text{C}$ [22]. The subthreshold characteristics are nonscalable. The above two issues prevent V_{th} from being scaled proportionally with the device dimensions down to less than roughly 0.4~0.5V[23]. Otherwise the subthreshold current and power dissipation will be undesirably increased. There are other concerns such as the non-scalability of junction built-in potential and the transition region, where the inversion charge Q_{I} is nonlinearly increased with V_{g} . In addition to the above fundamental limits associated with the physical parameters of ϕ_{t} , ϕ_{F} , and E_{g} , there are other practical limiting factors for scaling. The circuit requirement on functional capability with appropriate noise immunity prevents the power supply voltage from being less than about $4V_{\text{th}}$ [23, 24]. In fact the power supply voltage is kept constant as long as possible, which is called constant-voltage scaling. The nonscalability of the interconnection line length as well as the parasitic capacitance lead to slower response time with progress of scaling. The major delay for a circuit comes from the interconnection delay, which can not be solved by scaling the transistor size. Historically designers tried to expand circuits to reduce the interconnection length.

Table 2-2 Scaling factors associated with important device parameters for the constant-field scaling law, generalized one and the practical constant-voltage scaling law.

Parameter		Expression	Scaling Law		
			Constant E	Generalized	Constant V
Dimension		W, L, d, x_j	$1 / \lambda$		
Voltage		V_{DD}, V_T	$1 / \lambda$	$1 / \kappa$	1
Electric Field		$E_i, E_{ }$	1	λ / κ	λ
Doping Density		N_B	λ	λ^2 / κ	λ^2
Circuit	Capacitance	$C_G = A \epsilon_i / d$	$1 / \lambda$		
	Current	I_D	$1 / \lambda$	λ / κ^2	λ
	Gate Delay Time	$t_{pd} = C_G V_{DD} / I_D$	$1 / \lambda$	κ / λ^2	$1 / \lambda^2$
	Power Dissipation	$I_D V_{DD}$	$1 / \lambda^2$	$1 / \lambda \kappa$	$1 / \lambda$
Interconnection	Line Resistance	$R_L = \rho l / A_L$	λ		
	Time Constant	$R_L C_L$	1		
	Current Density	I_D / A_L	λ	λ^3 / κ^2	λ^3

All the fundamental and practical limiting factors call for supply voltage and threshold voltage to be reduced less than the traditional constant-field scaling would require. For modern sub-micron devices, the constant-voltage scaling law has become a practical guide for device shrinking. Therefore, the lateral and normal electric fields in a sub-micron MOSFET have been considerably increased. As the power supply voltage was maintained at 5V for over five generations from 3- μm to 0.6- μm design rules, the gate dielectric field has already been close to its highest allowable value of $\sim 3 \text{ MV/cm}$. Due to the increased electric fields, various concerns on device and circuit performance and reliability have caught attention in semiconductor field.

As recent development of ULSIs have required further scaling of MOSFETs down to deep sub-micron, the gate oxides are thinned to nanometers or even angstroms, and requirements on the quality and reliability become more severe. There are two alternative ways to resolve this problem, one is to keep the gate oxide unchanged and scale other device parameters such as operating voltage, and the other method is to replace the current gate oxide SiO_2 with a high dielectric constant insulator to achieve very thin equivalent SiO_2 . With the continuous scaling of device, operation voltage can not remain at the current value for 0.13 μm and smaller MOSFETs. Searching for high dielectric constant (k) material provides a resolution for future IC fabrication.

2.6 High Dielectric Constant Materials

Dielectric materials, also called insulators are very important in IC fabrication. They are used for insulation between conducting layers, for diffusion and ion implantation masks, for diffusion from doped oxides, for capping doped films to prevent the loss of dopants, for gettering impurities, and for passivation to protect devices from impurities, moisture, and scratches [25]. The general characteristics of dielectric usually comprise strong ionic or directed covalent bonds, brittle mechanical behavior at ordinary

temperatures, very high resistivity and transparent to visible and infrared light. A dielectric is polarized in the presence of an electric field. Dipole moments are produced as an external electric field is applied to the dielectric. There are several parameters used to describe this phenomenon such as electric field E , electric displacement D , the polarization P together with the electric susceptibility κ , and the dielectric constant ϵ or k . The relationships of above factors are

$$D = \epsilon^* E = \epsilon_0 E + P \quad (2.29)$$

$$P = \kappa \epsilon_0 E \quad (2.30)$$

$$\epsilon = 1 + \kappa \quad (2.31)$$

where ϵ_0 is the permittivity of vacuum, ϵ^* is the permittivity of the material and the relative dielectric constant is

$$\epsilon = \frac{\epsilon^*}{\epsilon_0} \quad (2.32)$$

For a dielectric material containing different kinds of atoms with concentration N_i and polarizability α_i , and assuming that different kinds of atoms act independently of one another, the relationship between the macroscopic quantity ϵ and the atomic quantity α_i is given by [26]

$$\sum_i N_i \alpha_i = 3 \frac{\epsilon - 1}{\epsilon + 2} \quad (2.33)$$

This is known as the Clausius-Mossotti formula. To relate the dielectric properties to the optical properties and consider time-dependent fields, we have

$$\epsilon = N^2 \quad (2.34)$$

where N is the refractive index. Substituting Eqn. 2.34 into Eqn. 2.33,

$$\sum_i N_i \alpha_i = 3 \frac{N^2 - 1}{N^2 + 2} \quad (2.35)$$

which is known as the Lorentz-Lorentz formula.

If the dielectric material possesses only electronic polarizability, it is non-polar and the dielectric constant will not change with frequency because electrons in atoms readily respond to optical frequencies. At X-ray frequencies, however, the dielectric constant is eventually unity and there is no agreement between the static and the X-ray dielectric constants. Materials that possess permanent molecular dipole moments have very different low- and high- frequency behavior, so that Eqn. 2.33 and Eqn. 2.35 can not be expected to give the same polarizabilities.

The frequency dependence of dielectric constant is related to the different mechanisms of polarization. There are four types of polarizations: electronic polarization, ionic polarization, dipolar polarization, and interfacial polarization. Electronic polarization is due to the separation of the centers of gravity of the electronic and nuclear charges in the applied electric field. This occurs up to very high frequency (10^{16} Hz). The application of an electric field to a polar substance causes a relative displacement of the ions leading to a lattice polarization described by an ionic polarization. Ions are heavy particles and more sluggish in their motion than electrons. As the frequency of applied electric field increases, there comes a time when the field changes so rapidly that the ions

can no longer follow its variation. Then there is no contribution to the total polarization from the ionic polarization. Therefore, ionic polarization only occurs in a relatively low frequency range $10^{10} - 10^{13}$ Hz. Dipole polarization is caused by the perturbation of the thermal motion of ionic or molecular dipoles, introducing a dipolar orientation in the direction of applied field. Interfacial polarization involves mobile charges in the dielectrics.

For simple elemental materials or binary compounds, Duffy has established an empirical relationship between energy band gap E_g and the dielectric constant ϵ : [27]

$$E_g = 20 \left[\frac{3}{\epsilon + 2} \right]^2 \quad (2.36)$$

This equation indicates that a material having large dielectric constant tends to have smaller band gap. An oxide of a single metal, such as Ta_2O_5 or ZrO_2 , usually has a relatively high dielectric constant. In general, with increasing the atomic number of the metal, the atomic (or ionic) radius increases and so the cohesive force decreases, leading to a higher dielectric constant but a narrower band gap [28]. Table 2-3 summarized the dielectric constants of various semiconductors and insulators. The comparison of the data in Table 2-3 and the calculated data from Eqn. 2.36 was shown in Fig. 2.15.

Table 2-3 The energy band gaps and dielectric constants of various dielectric materials.

	ϵ (low frequency)	E_g (eV)
Diamond (C)	5.7	5.4
Si	11.9	1.17
Ge	16	0.7
α -Sn	23.8	~ 0
SiO ₂	3.9	1.12
Si ₃ N ₄	7.5	5
Ta ₂ O ₅	15 -25	4.2
HfO ₂	16	5.68
Al ₂ O ₃	8 - 12	-
TiO ₂	20 – 170	3.0-3.2
ZrO ₂	20	5.16-7.8

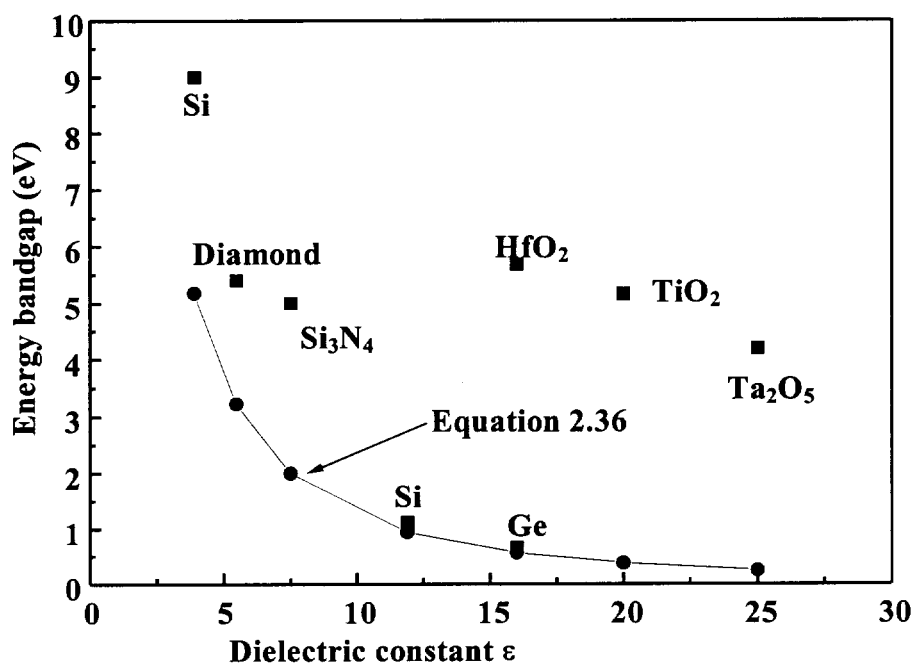


Fig.2.15 Energy bandgap vs. the dielectric constant of various semiconductor and dielectric materials.

Duffy's equation can not describe dielectric thin films accurately as seen from Fig. 2.15. However, it does show the trend that energy bandgap decreases with the increase of dielectric constant.

As the device size keeps shrinking, there is a great need to replace the gate oxide with some high dielectric constant material. However, the leakage current through high dielectric materials is a serious concern when these materials are to be integrated into low power IC fabrication.

Among these high dielectric metal oxides, Ta_2O_5 , HfO_2 , Al_2O_3 , and ZrO_2 have relatively large band gaps. Especially Ta_2O_5 has been extensively studied for high-density DRAM applications. Recently Ta_2O_5 has also been investigated as one of the promising candidates to replace SiO_2 as the gate dielectrics in MOSFETs. To relieve the high leakage current in Ta_2O_5 especially polycrystalline Ta_2O_5 , stacked structure of Ta_2O_5 with other insulators, such as SiO_2 [29,30], Al_2O_3 [31], are fabricated. The unique thin film deposition technique called atomic layer epitaxy allows growing of layered structures with nanometer range constituent layer. Using this method, Ta_2O_5 - HfO_2 nanolaminates have been studied to improve the leakage characteristics of Ta_2O_5 [32,33]. There are other nanolaminates such as Ta_2O_5 - ZrO_2 and HfO_2 - ZrO_2 that show improved leakage current characteristics while retaining high dielectric constant. In this thesis, the details of different nanolaminates for gate dielectrics have been investigated and will be presented in chapters 4 and 5.

References

- [1] E. H. Nicollian and J. R. Brews, MOS Physics and Technology, John Wiley & Sons, 1982, p. 208.
- [2] R. F. Pierret, Field Effect Devices, Addison-Wesley, 1990, p. 30.
- [3] S. M. Sze, Physics of Semiconductor Devices, John Wiley & Sons, 1981, p. 367.
- [4] C. G. B. Garrett and W. H. Brattain, "Physical theory of semiconductor surfaces," Phys. Rev. **99**, 1955, pp. 376-382.
- [5] A. S. Grove, B. E. Deal, E. H. Snow, and C. T. Sah, "Investigation of thermally oxidized silicon surface using metal-oxide-semiconductor structures," Solid State Electronics **8**, 1965, pp. 145-153.
- [6] A. Goetzberger and E. H. Nicollian, "Temperature dependence of inversion layer frequency response in silicon," Bell Syst. Tech. J. **46**, 1967, pp. 513-518.
- [7] A. Goetzberger, "Ideal MOS curves for silicon," Bell Syst. Tech. J. **45**, 1966, pp. 1097-1103.
- [8] B. E. Deal, "Standardized terminology for oxide charges associated with thermally oxidized silicon," IEEE Trans. Electron Devices **27**, 1980, pp. 606-612.
- [9] L. M. Terman, "An investigation of surface states at silicon/silicon dioxide interface employing metal-oxide-silicon diodes," Solid State Electronics **5**, 1962, pp. 285-290.
- [10] C. N. Berglund, "Surface states at steam-grown silicon-silicon dioxide interface," IEEE Trans. Electron Devices **13**, 1966, pp. 701-705.
- [11] R. Castagne, P. Hesto, and A. Vapaille, "Very low frequency response of inversion layer in MIS structure," Surface Science **268**, 1969, pp. 1578-1581.
- [12] E. H. Nicollian and A. Goetzberger, "The Si-SiO₂ interface electrical properties as determined by the MIS conductance technique," Bell Syst. Tech. J. **46**, 1967, pp. 1055-1061.
- [13] J. S. Brugler and P. G. A. Jespers, "Charge Pumping in MOS Devices," IEEE Trans. Electron Devices **16**, 1969, pp. 297-302.

- [14] F. Hofmann and W. H. Krautschneider, "A simple technique for determining the interface-trap distribution of submicron metal-oxide-semiconductor transistors by the charge pump method," *J. Appl. Phys.* **65**, 1989, pp. 1358-1360.
- [15] M. Ohring, *Reliability and Failure of Electronic Materials and Devices*, Academic Press, 1998, p. 305.
- [16] S. M. Sze, *Physics of Semiconductor Physics*, John Wiley & Sons, 1981, p. 254.
- [17] S. M. Sze, *Physics of Semiconductor Physics*, John Wiley & Sons, 1981, p. 403.
- [18] A. Balasinski, C. Petti, H. Bamnolker, K. Kamkumar, and A. Chung, "Characterization of plasma induced damage using transient current measurements," 3rd International Symposium on Plasma Process-Induced Damage, June 4-5, 1998, Honolulu, HI, pp. 26-29.
- [19] P. E. Nicollian, M. Rodder, D. T. Grider, P. Chen, R. M. Wallace, and S. V. Hattangady, "Low leakage stress-induced-leakage-current in ultrathin gate oxides," 37th Annual International Reliability Physics Symposium, San Diego, CA, 1999, pp. 400-404.
- [20] R. H. Dennard, F. H. Gaensslen, H. -N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid State Circuits* **9**, 1974, pp. 256-268.
- [21] G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to $\frac{1}{4}$ micrometer MOSFET design," *IEEE Trans. Electron Devices* **31**, 1984, pp. 452-462.
- [22] J. T. Tzou, C. C. Yao, R. Cheung, and H. Han, "The temperature dependence of threshold voltages in submicrometer CMOS," *IEEE Electron Device Letters* **6**, 1985, pp. 250-252.
- [23] J. R. Pfister, J. D. Shott, and J. D. Meindl, "Performance limits of CMOS ULSI," *IEEE Trans. Electron Devices* **32**, 1985, pp. 333-343.
- [24] B. Hoefflinger and G. Zimmer, "New CMOS technologies," *Solid State Devices* **57**, 1980, pp. 85-139.
- [25] S. M. Sze, *VLSI Technology*, John Wiley & Sons, 1988, p. 234.
- [26] H. P. Myers, *Introductory Solid State Physics*, Taylor & Francis, 1997, p. 391.

- [27] J. A. Duffy, *Bonding Energy Levels and Bands in Inorganic Solids*, John Wiley & Sons, 1990, p. 108.
- [28] K. W. Boer, *Survey of Semiconductor Physics*, Van Nostrand Reinhold, 1990, p. 26.
- [29] Y. Momiuama, H. Minakata, and T. Sugii, "Ultrathin Ta₂O₅/SiO₂ gate insulator with TiN gate technology for 0.1μm MOSFETs," 1997 Symp. on VLSI Technology Digest of Technical Papers, pp. 135-136.
- [30] I. C. Kizilyalli, R. Y. S. Huang, and P. K. Roy, "MOS transistor with stacked SiO₂-Ta₂O₅-SiO₂ gate dielectrics for giga-scale integration of CMOS technologies," *IEEE Electron Device Letters* **19**, 1998, pp. 423-425.
- [31] R. J. Cava, W. F. Peck, Jr. J. J. Krajewski, G. L. Roberts, B. P. Barber, H. M. O'Bryan, and P. L. Gammel, "Improvement of the dielectric properties of Ta₂O₅ through substitution with Al₂O₃," *Appl. Phys. Lett.* **70**, 1997, pp. 1396-1398.
- [32] K. Kukli, J. Ihakko, M. Ritala, and M. Leskela, "Tailoring the dielectric properties of HfO₂-Ta₂O₅ nanolaminates," *Appl. Phys. Lett.* **68**, 1996, pp. 3737-3739.
- [33] K. Kukli, J. Ihakko, M. Ritala, and M. Leskela, "Properties of Ta₂O₅-based dielectric nanolaminates deposited by atomic layer epitaxy," *J. Electrochem. Soc.* **144**, 1997, pp. 300-306.

Chapter 3

Atomic Layer Epitaxy

This chapter is a review of the fundamentals of Atomic Layer Epitaxy (ALE), its development history, the operation mechanism and the application of this technique. The actual application ALE on high dielectric constant thin film deposition will be addressed in details in next chapter.

3.1 Background of ALE

Atomic layer epitaxy (ALE) is a method for producing thin films and layers of crystalline or amorphous films one atomic layer at a time utilizing a self-controlled surface reaction. It was originally developed to meet the needs of ZnS thin films and dielectric thin films for electroluminescent (EL) thin film display devices [1-3]. The ALE technique was first established by Suntola and Anston based on a modified vacuum evaporator in 1974. Although the name “atomic layer epitaxy” was originally given by Suntola, it is now a generic term for this method of film deposition and the deposited film can be either crystalline or amorphous. The first US patent on ALE was submitted by the Lohja Corporation from Finland in 1975 and granted in 1977 [1]. Since then ALE has been used mostly to grow thin films in display industry. Current commercial grade ALE reactors manufactured by ASM Microchemistry can handle 8-inch wafers. The ALE technique has also been extended for semiconductor and IC fabrication. The high

permittivity insulators, such as metal oxides processed by ALE have recently attracted more interest from the semiconductor industry [4-5].

3.2 The mechanism of ALE process

The basic idea of ALE is the sequential surface reactions resulting in a saturating monolayer growth during each step. In a typical ALE process, the substrate is exposed to alternate vapor sources. The substrate surface is initially saturated with the first reactant in vapor phase. This step is followed by a purging cycle by an inert gas such as N_2 to remove the excess reactants. Due to the energy difference between chemical adsorption and physical adsorption, only one atomic layer will be left adhering to reaction surface. Then the substrate is subject to the second component vapor for a binary compound. After the reaction of the first and the second reactants, an atomic layer of desired binary compound is deposited on the substrate surface after one cycle. The gas phase by-products and excess vapors of reactants are carried out of the reactor by the purge gas pulse. By repeating the reaction cycles, thin films can be deposited monolayer-by-monolayer.

The successful growth via ALE is based on the energy difference between chemical adsorption and physical absorption of reactants on the surface of a substrate. Chemical adsorption describes the chemical bonding between two atoms, while physical adsorption is due to the van der Waal's forces between charges. When a flux of reactant reaches the substrate surface, the first layer interacts with the substrate and is chemically adsorbed onto the substrate, forming chemical bond at an appropriate temperature. This is called chemical adsorption. The subsequent layers are bonded much more weakly and the bonds are very easy to break, hence called physical adsorption. The energy diagram of these two kinds of adsorption mechanism is illustrated in Fig. 3.1, where E_c and E_p are the activation energies of chemical adsorption and physical adsorption, respectively [6].

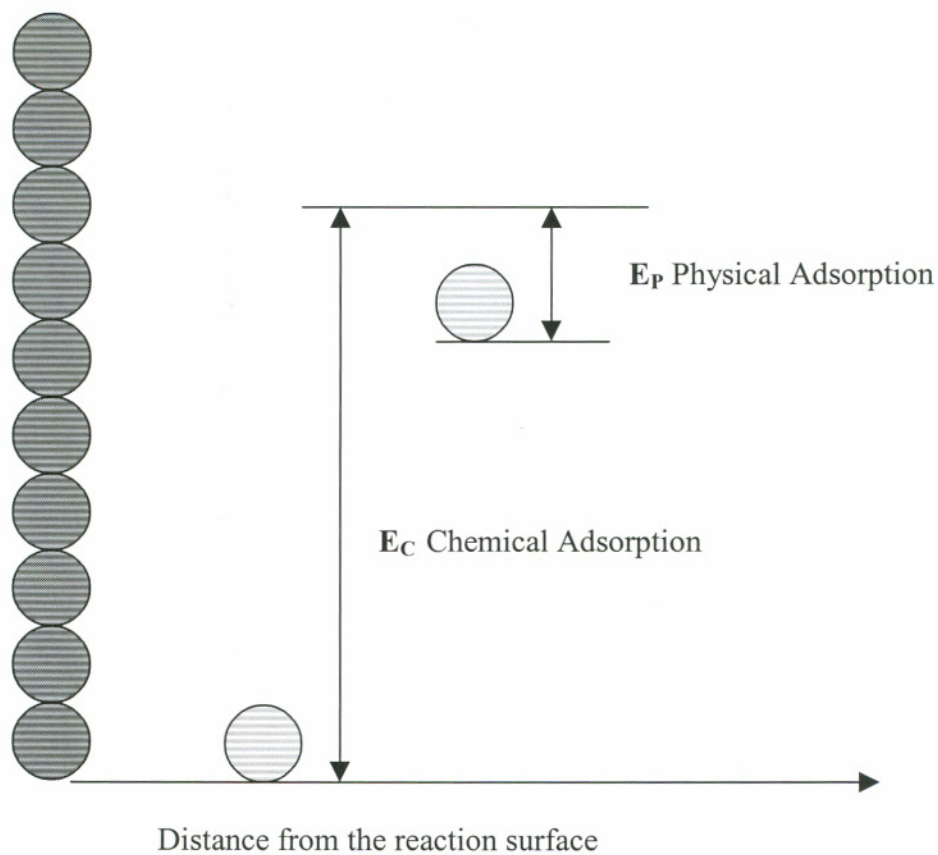


Fig. 3.1 Energy diagram of chemical and physical adsorption

When selecting the source materials for an ALE process, a discrimination factor η is defined as:

$$\eta = \exp\left(\frac{E_C}{E_P}\right) \quad (3.1)$$

It is desirable to find the source materials with large discrimination factors when they are introduced to the substrate. This allows us to have larger ALE process

temperature windows. Generally the substrate temperature should satisfy $E_p < kT \ll E_c$, where k is the Boltzmann constant and kT is the thermal energy of the substrate. The appropriate temperature range for a successful ALE growth, the so-called ALE temperature window has been studied by Suntola [7]. In this temperature range the film growth will produce one monolayer per cycle and the growth rate remains constant regardless of the temperature changes within the allowed range, as illustrated in Fig. 3.2.

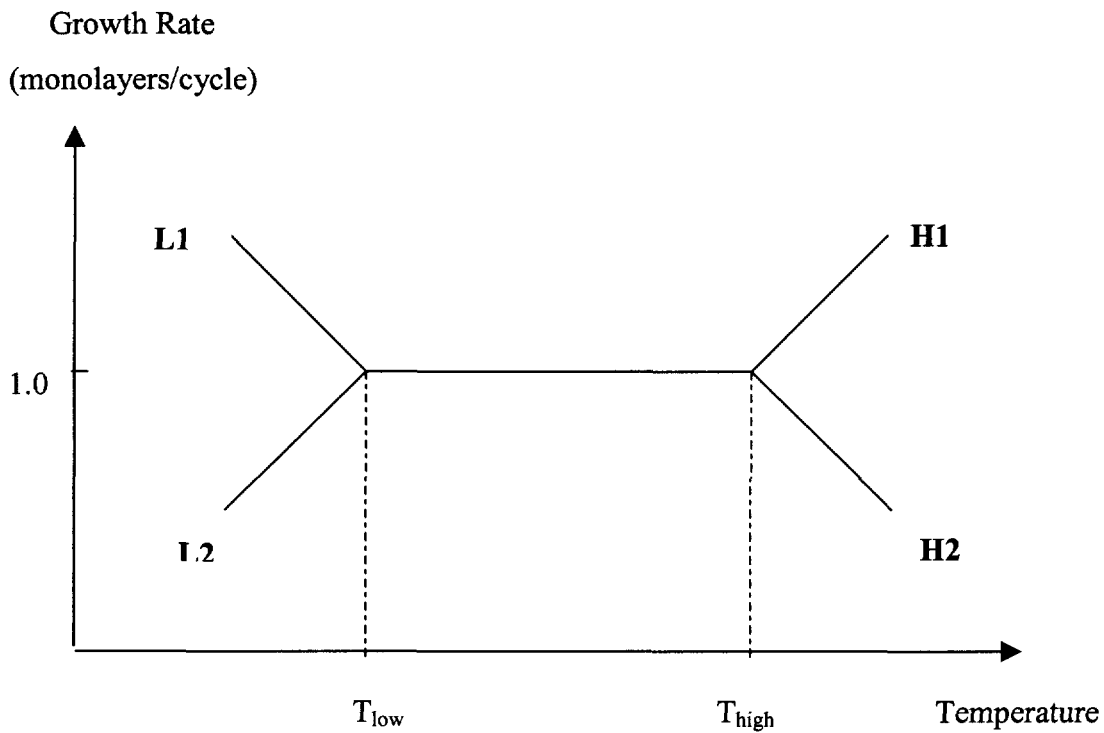


Fig. 3.2 An ALE processing temperature window.

The temperature dependence of the growth rate in monolayer units per cycle gives a first indication of the limiting mechanisms of ALE process. When the operation temperature is between T_{low} and T_{high} , monolayer ALE growth occurs.

At the operating temperature below the lower limit of the window temperature, the following problems will take place:

(L1) Condensation of reactants and their by-products generally with elemental sources. This may cause higher growth rate but this rate will vary with temperature. Therefore, this is an uncontrollable process.

(L2) Incomplete surface reactions mostly with molecular sources. In this case, there is activation energy to be exceeded. Extra energy will be needed to form the chemical adsorption.

At operating temperature above the higher limit of the window temperature, other problems can occur:

(H1) The undesirable decomposition of molecular reactants will result in fast film growth. This is typical when large molecular metal organic compounds are used as precursors.

(H2) Re-evaporation of a formed monolayers.

The temperature limits depend on the time and flux density of the reactants used for each sequence. In a typical ALE process, there are several process parameters that need to be optimized to achieve an ideal monolayer growth. First of all, the substrate temperature is obviously critical as seen from the ALE temperature window. Meanwhile, the substrate has to be saturated with the source material in vapor phase, which means the flux of source vapor must be able to cover the entire substrate. Therefore, reactor pressure and the source material temperature must be carefully adjusted. Furthermore, the vapor source should have high mobility across the substrate to achieve uniform growth. This is a matter of choosing source material and defines the flow rate of inert purge gas, as well as setting pulse time for each sequence. Reactor cleaning is also critical to prevent cross contamination from run to run.

There is some literature reporting surface chemistry of ALE growth of metal oxides on porous silica. The surface coverage of metal species achievable at a certain temperature on an oxide is determined by the number of specific reactive sites for the

precursors [8]. Silica surfaces are terminated by isolated H-bonded OH groups and siloxanes (oxygen bridges), which serve as bonding sites. The heat treatment of silica controls the number of OH groups on the surface, which in turn determines the surface density of a precursor bonding to the OH groups. Although these studies only concentrated on silica, they can be applied on other oxides since all oxide surfaces are more or less terminated with OH groups and oxygen bridges. However, each precursor/oxide pair would need a separate study.

Atomic layer epitaxy is primarily used in epitaxial growth of III-V and II-VI compounds, especially layered structures, such as superlattices and superalloys. It has great advantage in thin film deposition from multiple source materials at relatively low temperatures. Since ALE is a fairly new technique, the growth technique is still not well understood. However, this does not influence the application of ALE on high quality thin film deposition. Most thin film deposition techniques involve material transfer from a solid source via vapor phase in high vacuum systems or at high temperature, such as evaporation, sputtering, or chemical vapor deposition (CVD). Compared to these technologies, ALE produces epitaxial layers at relatively lower temperatures and does not require ultra-high vacuum reactors. It is a self-controlled process, which results in an accuracy of a single atomic layer because of saturated surface reactions. ALE has been proved to be suitable for growing uniform layers over large areas, even on non-planar surfaces. Using this method, it is possible to investigate the chemical reactions associated with thin film growth in more details compared to other technologies. In current ultra thin film (in nanometer scale) processing, ALE excels over other traditional approaches due to its precise control of the thickness and composition of thin films across a large area. Therefore, ALE is finding more applications in modern high-tech industries.

References

- [1] T. Suntola and M. J. Anston, "Method for producing compound thin films," U. S. Patent No. 4,058,430 (1977).
- [2] T. Suntola, A. Pakkala, and S. Lindfors, "Method for performing growth of compound thin films," U. S. Patent No. 4,413,022 (1983).
- [3] T. Suntola, "Performance of atomic layer epitaxy devices," Digest of Technical Papers on SID International Symposium (Society for Information Display), New York, NY, 1981, pp. 20-21.
- [4] L. Niinisto, M. Ritala, and M. Leskela, "Synthesis of oxide thin films and overlayers by atomic layer epitaxy for advanced applications," *Materials Science and Engineering B* **41**, 1996, pp. 23-29.
- [5] H. Kattelus, M. Yliammi, J. Saarilahti, J. Antson, and S. Lindfors, "Layered tantalum-aluminum oxide films deposited by atomic layer epitaxy," *Thin Solid Films* **225**, 1993, pp. 296-298.
- [6] T. Suntola, "Atomic layer epitaxy," *Acta Polytechnica Scandinavica, Electrical Engineering Series* **64**, 1989, pp. 242-270.
- [7] T. Suntola, "Atomic layer epitaxy," *Materials Science Report* **4**, 1989, pp. 261-312.
- [8] S. Haukka, E-L Lakomaa, and T. Suntola, "Surface coverage of ALE precursors on oxides," *Applied Surface Science* **82/83**, 1994, pp. 548-552.

Chapter 4

ALE growth of Ta₂O₅, HfO₂, ZrO₂ and their nanolaminates

In this chapter, the growth of high dielectric constant thin films Ta₂O₅, HfO₂ and ZrO₂ by atomic layer deposition will be described. The process conditions for growing these films on bare silicon substrate and silicon nitride passivated silicon substrates are presented. X-ray diffraction and transmission electron microscope (TEM) were employed to characterize material properties.

4.1 Introduction of the F-120 ALE reactor

ALE F-120 reactor was manufactured by the Finnish company Microchemistry Ltd. It was designed for research purposes, for high flexibility and for easy operation. The design of the gas flow dynamics in F-120 has been made in parallel with that in production size reactors. Therefore processes developed with F-120 reactor are scalable to industrial scale in a straightforward way.

The schematic diagram of the F-120 is shown in Fig. 4.1[1]. There are six precursor sources available, four of which (#1, #2, #4, #5) are for solid source materials (mostly powders or pre-melted powders), the other two (#3 and #6) are for gases (such as H₂S and H₂) and liquid (such as H₂O) sources. Each port is sealed with an O-ring and has a thermocouple probe. Solid source materials are usually held in glass boats that are attached to the thermocouples for temperature control. The solid source temperatures

need to be high enough for the precursor to be vaporized and low enough to prevent the precursor from being depleted before a deposition run finishes. The tubing and valving system of the F-120 reactor are fairly complicated as shown in Fig. 4.1. There is one inner tube and one outer tube for each source port. When the vapor is not needed in the reaction chamber, valve A is closed and only N_2 can flow in the outer tube. The vapor is split at the substrate end, going to the substrate and along the BDE to carry the undesired vapor (excess source precursor and by-products) to the exhaust tube. On the other hand, when the vapor is needed, valve A opens, and N_2 will be divided to flow in both inner and outer tubes but mostly through the inner tube. Source vapor flows in direction DBC to the substrate holder.

Heating coils control the temperatures of eight temperature zones, and temperature increases in the direction toward the substrate holder. The advantage of this temperature distribution is that gases flowing toward the substrate travel through regions of increasing temperatures, reducing or eliminating the possibility of condensation on the tube wall. The temperature setting of each temperature zone will be affected by its neighboring heaters because the thermal insulation of adjacent temperature zones is not perfect. It is necessary to set small temperature increments for adjacent heaters when we set up a run. However, this weakness limits our choices of precursors.

The schematic side view of the substrate holder (also called "satellite") in the F-120 is shown in Fig. 4.2. Fig. 4.3 shows the rear view. Two 50 mm x 50 mm substrates are held back-to-back and sit vertically in the substrate holder. A glass spacer could be used between the two substrates depending on the actual width of the trench on the glass substrate boat used to hold the substrates in the "satellite".

The ALE process is controlled by a Compaq 386-PC computer that allows the user to program the source temperatures, growth temperature, gas flow rate and pulsing sequence. Programming can conveniently control multiple layer growth and doping levels.

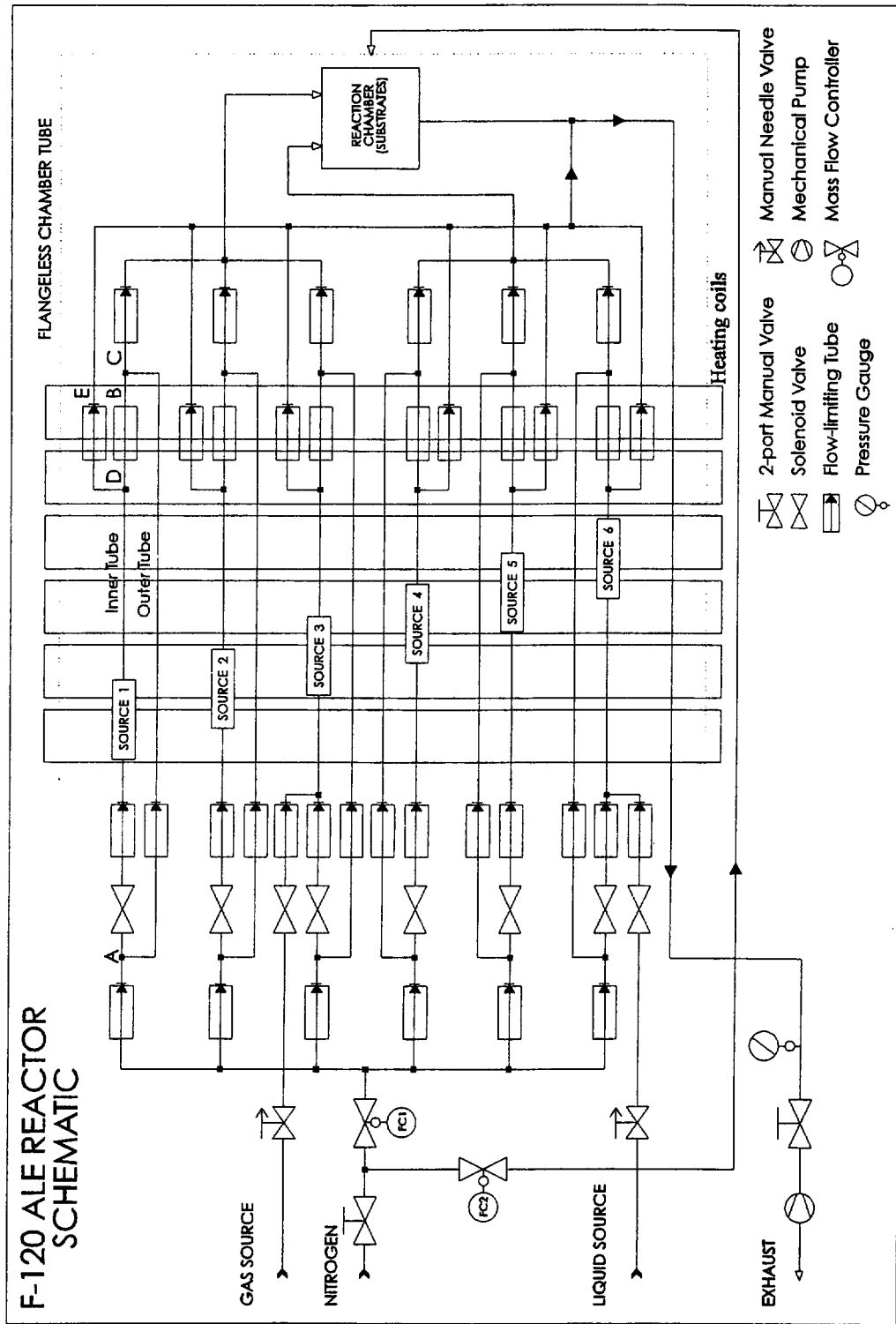


Fig. 4.1 ALE F-120 reactor system schematic.
[1]

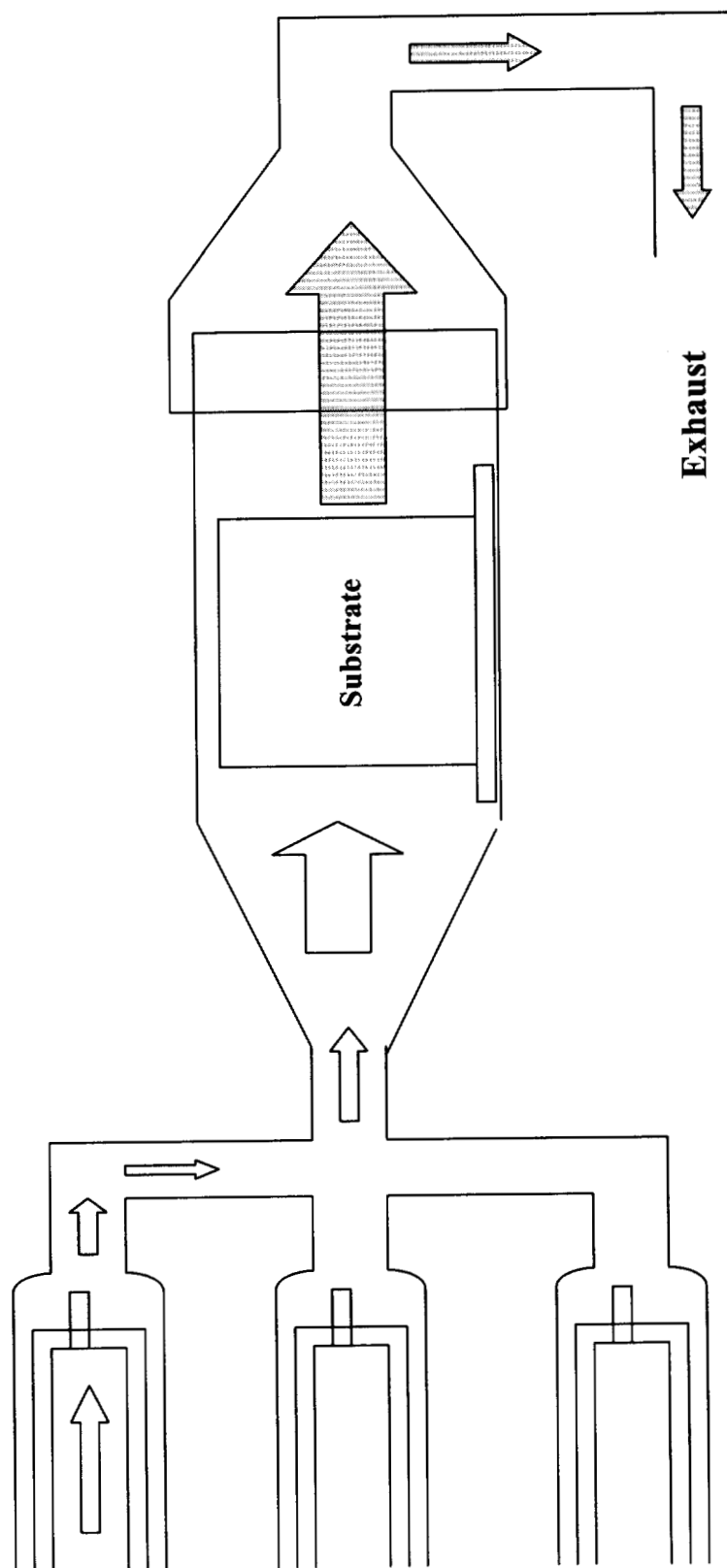


Fig. 4.2 Schematic diagram of the F-120 substrate holder (side view)

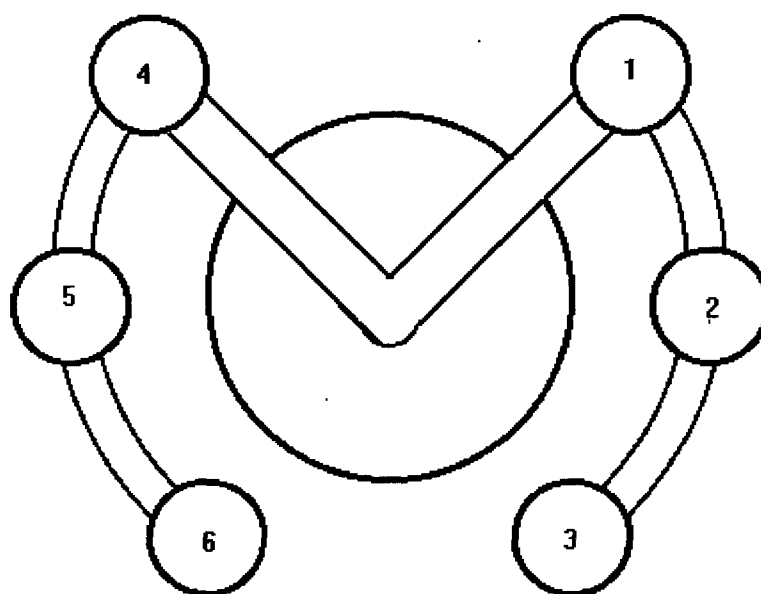


Fig. 4.3 The rear view of F-120 substrate holder. There are six precursor ports.

4.2 Growth and Initial Characterization of Ta_2O_5

Tantalum oxide (Ta_2O_5) thin film has attracted much interest due to its promising application as a storage capacitor material for gigabit dynamic random access memories (DRAM) [2-5]. Ta_2O_5 has many outstanding characteristics, including high dielectric constant and high capacitor density [6]. Having a dielectric constant of around 25, Ta_2O_5 has also been proposed as MOSFET gate insulator for high-speed circuits [7]. Ta_2O_5 thin films grown by ALE at 300°C are usually amorphous and turn to polycrystalline after rapid thermal annealing at temperatures above 800°C . When growing via ALE, tantalum chloride (TaCl_5) and water (H_2O) vapor have been used as source materials. TaCl_5 is the metallic precursor while H_2O is used as the oxidant source. The TaCl_5 used is in form of

very fine powder and has fairly high vapor pressure when heated up to around 100°C. H_2O source was kept at room temperature. In the growth cycle of Ta_2O_5 , TaCl_5 and H_2O vapor were pulsed alternatively as shown in Fig. 4.4. Nitrogen (N_2) is used as the carrier gas for both precursors. A 2 s N_2 purging gas is inserted between TaCl_5 and H_2O pulses. The effect of N_2 purge is to transport source material to substrates and clean the reaction surface so that excess gas molecules and by-products are carried away. The overall chemistry on the substrate surface will lead to formation of Ta_2O_5 and HCl . The HCl is volatile and will be pumped out while Ta_2O_5 will stay on the substrate. When Ta_2O_5 is grown on Si substrates, the substrates are pre-cleaned and dipped into HF prior to loading into the ALE reactor. The oxide thickness and their refractive indices were initially determined with a Gaertner ellipsometer (at wavelength of 632.8 nm) and then more detailed analysis was done using a spectroscopic ellipsometer (SOPRA ES4G). The crystalline properties were determined using a grazing incidence X-ray diffractometer (XRD) and cross-sectional transmission electron microscopy (TEM).

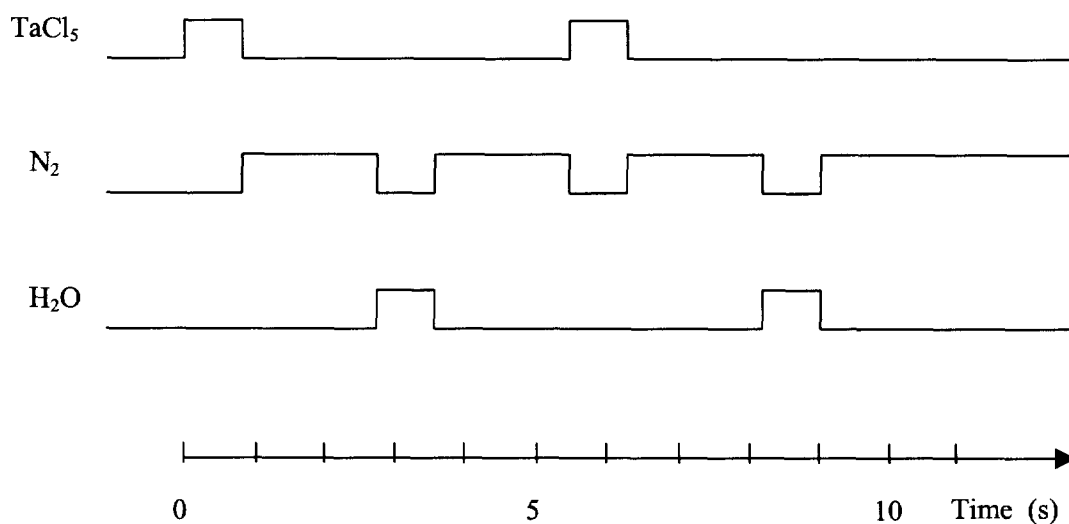


Fig. 4.4 Gas pulse sequence in Ta_2O_5 growth by ALE process

During growth of Ta_2O_5 , a very thin layer of SiO_2 is formed on top of Si as shown in Fig.4.5. This is due to the oxidation of silicon by the H_2O pulse at the growth temperature. This thin layer of SiO_2 dramatically reduced the total capacitance of the SiO_2 - Ta_2O_5 stack due to the low dielectric constant of SiO_2 . Some Ta_2O_5 depositions were performed on Indium-Titanium-Oxide (ITO) substrate, and the capacitance of this ITO- Ta_2O_5 stack was much higher than that of Ta_2O_5 - SiO_2 stack. To prevent Si surface from oxidizing, a layer of Si_3N_4 of thickness 2.76 nm was formed on Si substrate by rapid thermal process in NH_3 ambient at 1000°C for 15~30 seconds. Subsequent Ta_2O_5 deposition was on Si_3N_4 coated Si substrates.

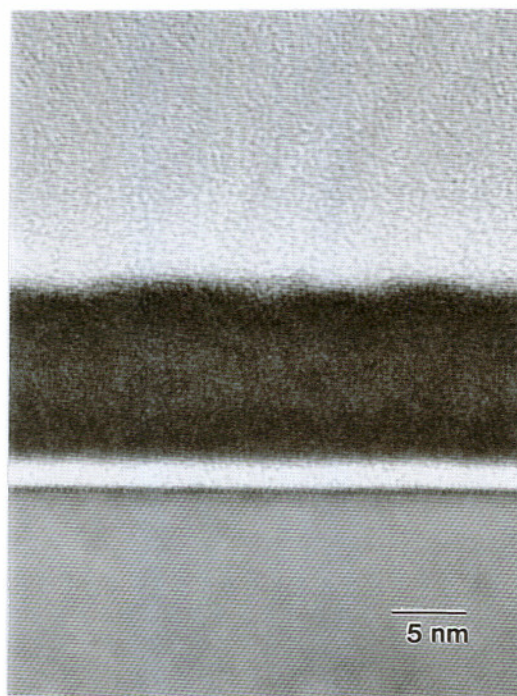


Fig. 4.5 High resolution TEM lattice image of Ta_2O_5 film with an ellipsometrically measured thickness of 11.6 nm grown on silicon substrate. A layer of 1.5 nm SiO_2 is formed at the interface.

A wide range of growth temperatures was studied. Ta_2O_5 thin films were deposited at reactor temperatures of 100, 200, 300, 400 and 500°C. As shown in Fig. 4.6, the growth rate decreases with an increase of film growth temperature. At temperatures of 100 and 200°C, condensation of reactants occurs on the substrates so that the growth rates were fairly high. Extreme low growth rates were observed at 400 and 500°C, which was due to re-evaporation of a formed monolayer. Therefore, the proper growth temperature window is around 300°C. Rapid thermal anneal (RTA) at 1000°C in argon ambient did not change the film thickness except for the film grown at 100°C, where Ta_2O_5 film thickness decreased after RTA as shown in Fig. 4.7. This could be due to the densification of the film grown at 100°C. It is also necessary to optimize the amount of water in the process. With the growth temperature set at 300°C, Ta_2O_5 was grown with water needle valve opened at 2, 4, 6 and 7.5 turns. Film thickness increased with the increase of water. The best uniformity was obtained with water opened at four turns. No obvious variation of film thickness was observed before and after RTP as shown in Fig. 4.8. Ellipsometry study revealed that the refractive index of annealed film was 2.183 at 632.8 nm, the same as the as-deposited films. XRD analysis indicated that as-deposited Ta_2O_5 thin film to be amorphous. However, these films crystallized after annealing in a RTP chamber at 800°C in either argon or oxygen ambient as shown in Fig. 4.9 and had the hexagonal crystal structure. Argon was used to avoid oxidation of the Si substrates during anneal. There could be oxygen vacancies in the deposited films, which can cause the increase of leakage current as has been reported. O_2 anneal helps to reduce the oxygen vacancies if there are any. Secondary ion mass spectroscopy (SIMS) characterization showed the films to be stoichiometric, with the concentration of chlorine below the detection limit.

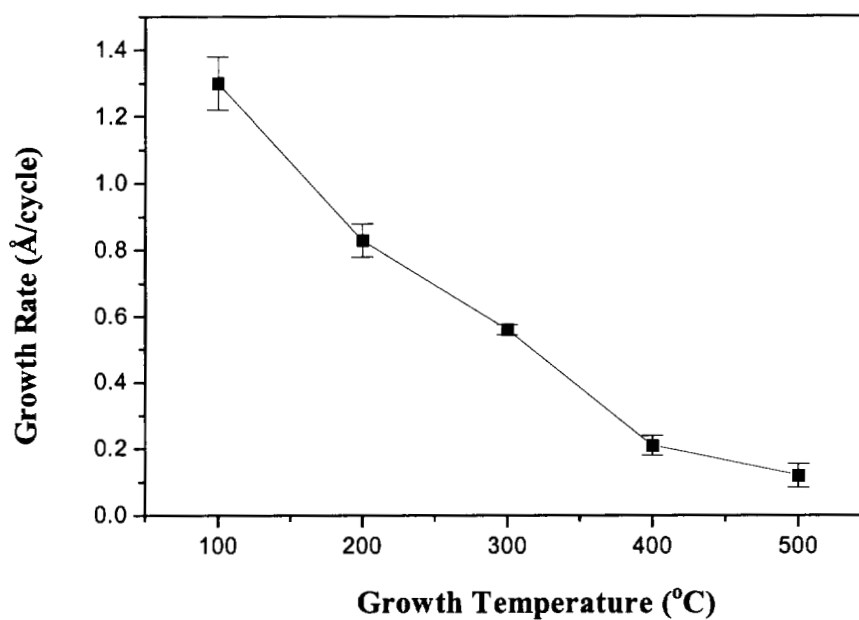


Fig.4.6 Growth rate vs. growth temperature of Ta_2O_5 ALE thin films grown on Si substrate using TaCl_5 and H_2O .

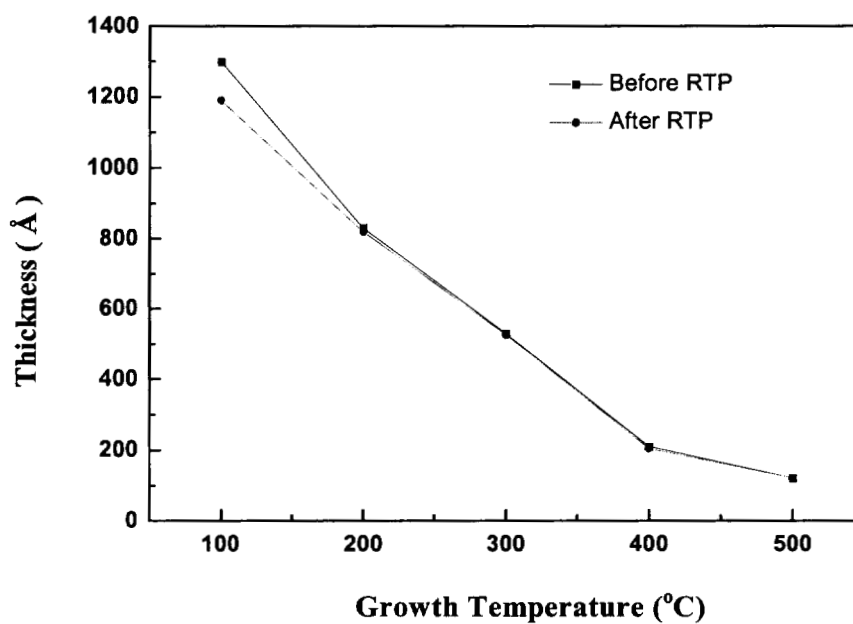


Fig. 4.7 The effect of RTP on Ta_2O_5 film thickness at growth temperatures of 100, 200, 300, 400 and 500°C. The number of water turn is 4 and water is kept at 20°C.

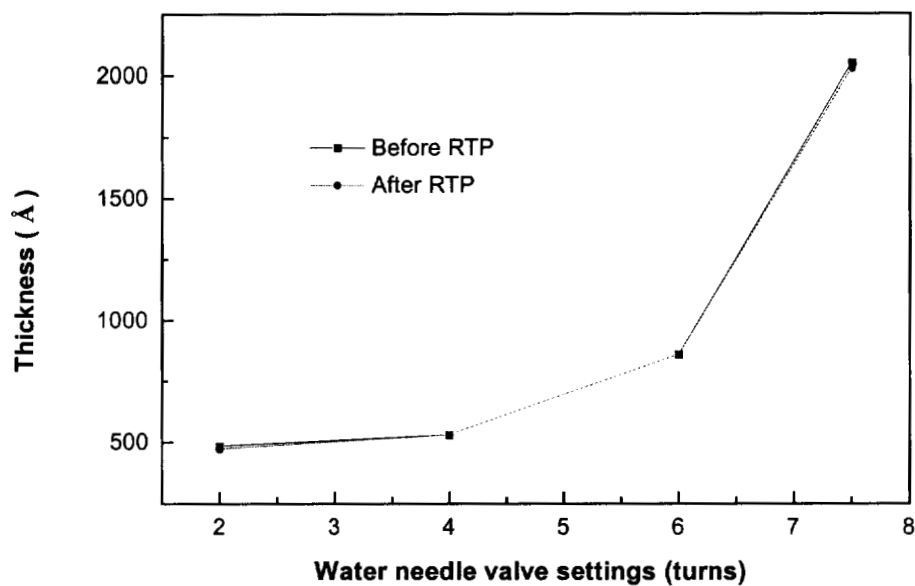


Fig. 4.8 The effect of water on Ta₂O₅ film thickness at growth temperature of 300°C.

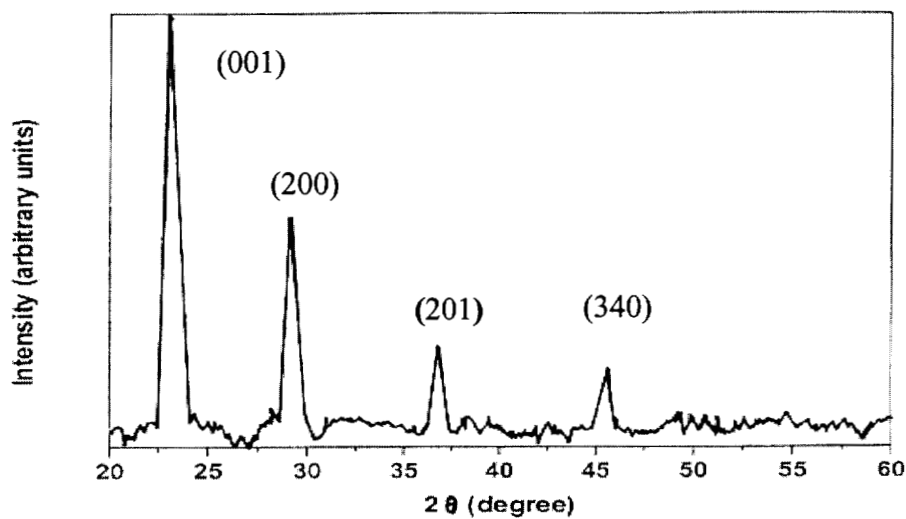


Fig. 4.9 X-ray diffraction pattern of rapid thermal annealed Ta₂O₅ film at 800°C for 30 s in Ar.

4.3 Growth and initial characterization of HfO₂

Hafnium oxide (HfO₂) is another insulating material with a much higher permittivity than silicon dioxide (SiO₂). The reported dielectric constants of bulk HfO₂ are 13-16 [8], which is lower than that of Ta₂O₅. However, the leakage current of HfO₂ is much lower than that of Ta₂O₅ for films of the same thickness. Quite promising results have been reported for sputtered HfO₂ films used in MOS capacitors [9]. It has also been used as an effective etch-stop layer when etching SiO₂ overcoats [10].

The source materials for growing HfO₂ were HfCl₄ powder and water vapor. The optimized source temperature was 140°C for HfCl₄, whereas H₂O was again kept at 20°C. The deposition of HfO₂ by ALE was conducted between 250 – 500°C. The growth rate decreased from 1.9 Å/cycle at 250°C to 0.32 Å/cycle at 500°C. The growth rate of HfO₂ is 1.1 Å/cycle at 300°C. To keep the growth temperature same as that for Ta₂O₅, a film deposited at 300°C was analyzed using SIMS technique giving a result that the chlorine concentration is less than detection limit. When HfO₂ was grown on a Si substrate, the film uniformity was very poor. Similar to the growth of Ta₂O₅ on bare Si substrates, an interfacial layer of SiO₂ was observed when growing HfO₂ directly on Si. However, the uniformity of HfO₂ film was significantly improved when HfO₂ was deposited on a nitrided Si substrate. This is due to the improved adhesion of HfO₂ to Si₃N₄. HfO₂ deposited on a Si substrate and Indium- Titanium- Oxide (ITO) coated glass by ALE at 300°C had a dielectric constant of 16 for a 28 nm thick film. Although there was a thin layer of SiO₂ appeared at the HfO₂-Si interface, the reduction of capacitance due to the existence of SiO₂ is negligible when the thickness of HfO₂ is greater than 20 nm. It is obvious that the capacitance of the HfO₂ will dominate when its thickness is large enough. The as-deposited HfO₂ by ALE was also amorphous. It is evident from XRD analysis that HfO₂ thin films crystallize after annealing in the RTA chamber at 800°C for 30 s in Ar or O₂ ambient, as shown in Fig. 4.10. The monoclinic structure is believed to be stable with lattice constants $a = 5.285 \text{ \AA}$, $b = 5.182 \text{ \AA}$, $c = 5.116 \text{ \AA}$, a preferred orientation in the (1, 1, 1) plane. A TEM cross-section photograph showed the oxidation of Si during the

growth of HfO_2 on bare Si wafer in Fig. 4.11. This thin interfacial layer of SiO_2 will reduce the effective k value of $\text{HfO}_2/\text{SiO}_2$ stack because of the low dielectric constant of SiO_2 . Therefore, a nitrided silicon substrate was used in the future HfO_2 growth, as for the Ta_2O_5 thin film.

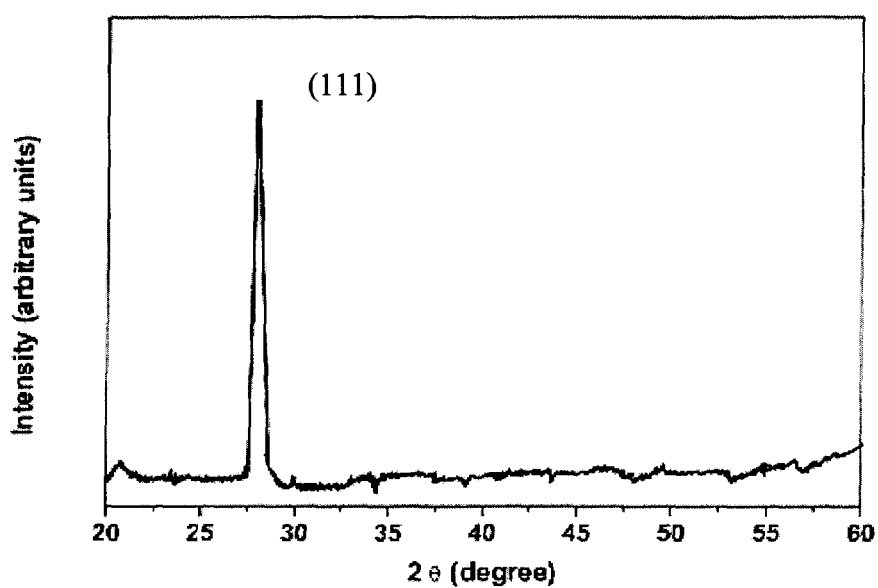


Fig. 4.10 X-ray diffraction pattern of HfO_2 annealed in RTA chamber at 800 °C for 30 s in Ar.

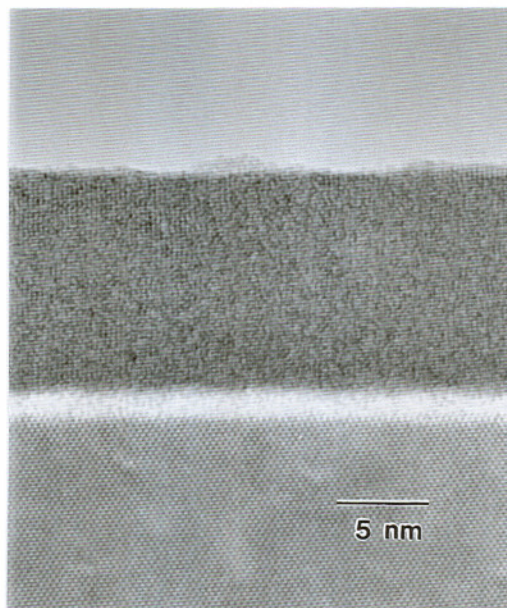


Fig. 4.11 High resolution TEM lattice image of HfO_2 film with an ellipsometry thickness of 15 nm grown on Si. SiO_2 layer of 2 nm is formed at the interface.

4.4 Growth and initial characterization of ZrO_2

Zirconium oxide (ZrO_2) is characterized by extreme thermal, chemical and mechanical stability which together with its optical and electrical properties gives rise to a wide range of technical applications for its thin films and coatings, especially in optics, electronics, and as protective layers. The fairly high permittivity (20 for bulk material) and low leakage current with a wide band gap of 5.1~7.8 eV make ZrO_2 an attractive material for future high capacitance MOS capacitor. Besides numerous physical vapor deposition techniques, like plasma spraying [11] and sputtering [12], chemical vapor deposition (CVD) has also been used to deposit ZrO_2 thin films [13,14]. The use of ZrCl_4 , the most readily available volatile zirconium precursor, is complicated due to its hygroscopic properties and the oxidation results in premature powder formation. The

characteristic feature of ALE can avoid the gas-phase reactions when exploiting ZrCl_4 and H_2O as the source materials [15].

In a typical ALE process, ZrCl_4 (99.5% purity; Strem) was evaporated from an open boat at 150°C onto the substrate. An external water reservoir held at 20°C was connected to the cold end of the reactor through a capillary and a needle valve. Water was introduced into the reactor by its own pressure without any bubbling systems. Total pressure of the reactor was in the order of 10 mbar. ZrO_2 films were deposited at 300°C , 400°C and 500°C , respectively. Lower growth rates were observed at 400°C and 500°C . In order to grow nanolaminates, ZrO_2 grown at 300°C was studied in detail. Compared to deposition of Ta_2O_5 and HfO_2 , rather long pulse and purge times were needed to realize the self-controlled process for the ZrO_2 growth. The growth of ZrO_2 highly depended on ZrCl_4 and the water pulse durations at substrate temperature of 300°C . Fig. 4.12 shows the dependence of film thickness on ZrCl_4 pulse duration. The effect of the purge time was studied with a 2 s pulse durations as indicated in Fig. 4.13. The thicknesses shown were measured at the center of the substrates. When the ZrCl_4 pulse time was longer than 1.5 s and water purge duration exceeded 2 s, saturation is reached and film conformity was independent of the above parameters. It was observed that the ZrCl_4 pulse was critical with respect to the surface saturation, while short water pulse had no effect on film thickness. On the other hand, water purge time was essential to achieve good thickness uniformity. The optimized growth condition of ZrO_2 produced a growth rate of 1.2 Å/cycle.

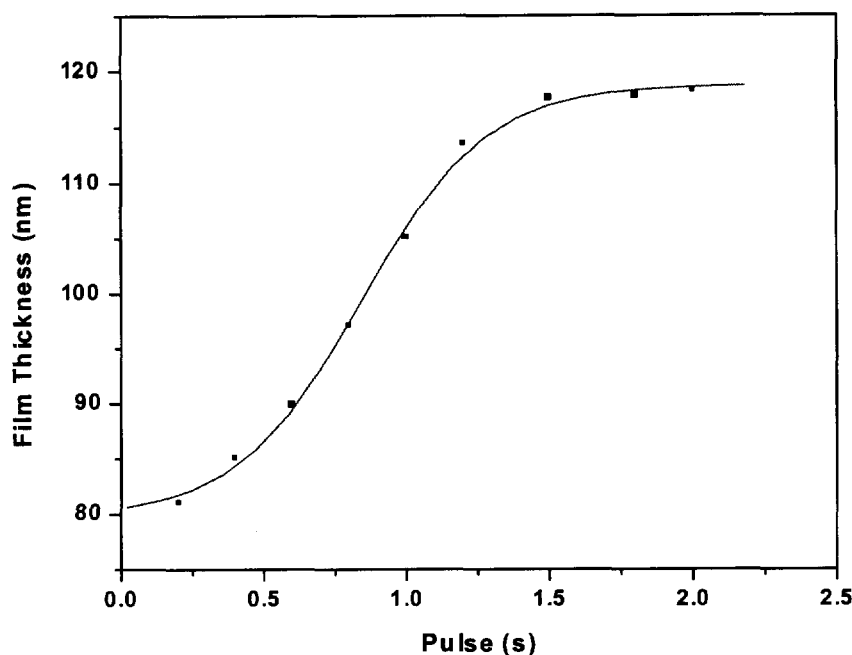


Fig. 4.12 The dependence of film thickness on the ZrCl_4 pulse duration for ZrO_2 film deposited at 300°C for 1000 reaction cycles. The ZrCl_4 purge time used was 2.0 s except for 2.0 s pulse time where 4.0 s purge duration was employed.

The as-deposited ZrO_2 was nearly amorphous and was partially crystallized after RTP at 700°C for 30 s, as shown in Fig. 4.14. The film showed strong (002) peak of tetragonal ZrO_2 and relatively weak (111) peak of monoclinic ZrO_2 . This means the polycrystalline ZrO_2 film was composed of mainly tetragonal ZrO_2 with a small amount of monoclinic ZrO_2 . Again SIMS analysis did not detect any trace of chloride in the ZrO_2 thin film. The ellipsometry measurement indicated a refractive index of 2.1 at wavelength 632.8 nm.

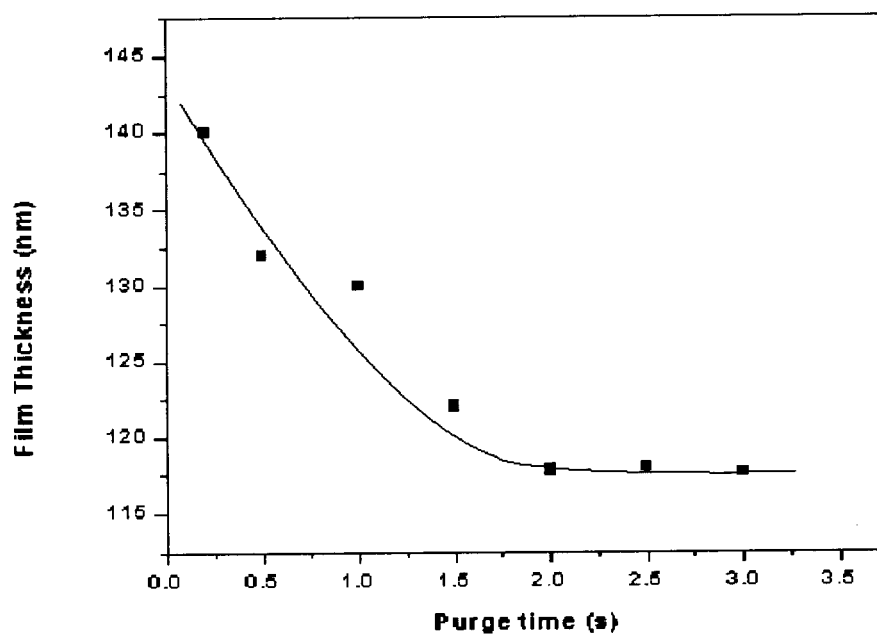


Fig. 4.13 The film thickness as a function of the water purge durations. The data were measured at the center of the film grown by 1000 cycles at 300°C using 2.0 s ZrCl_4 pulses.

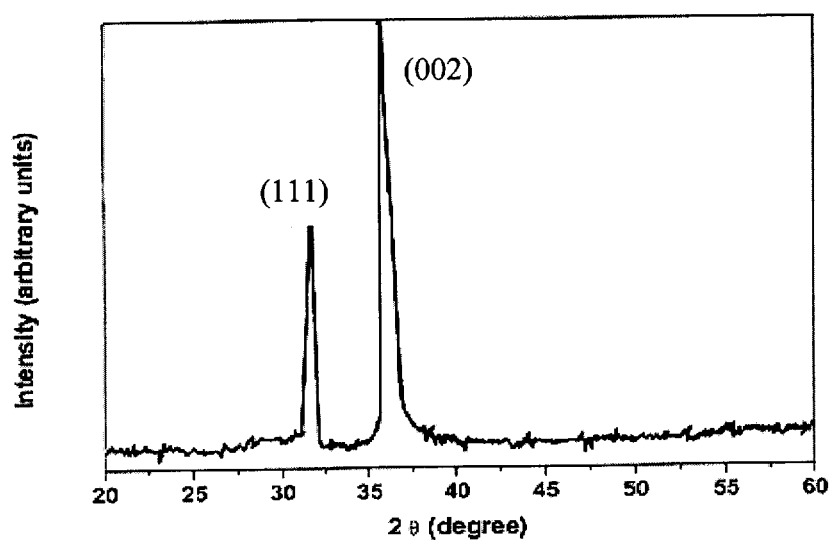


Fig. 4.14 X-ray diffraction pattern of ZrO_2 annealed at 700°C for 30 s in Ar.

4.5 Growth and initial characterization of nanolaminates

Nanolaminates consist of thin layers of alternating metal oxides. These oxides may be crystalline or amorphous by themselves. Since the amorphous layers interrupt the continuous growth of the polycrystalline material, the continuous grain boundaries were inherently eliminated [16]. To obtain the optimum dielectric properties, the constituent oxides should be of high permittivity and sufficiently thin.

As the layer thickness was reduced, the size of the crystallites after anneal was reduced, which in turn decreased the leakage current of the nanolaminates. An increased amount of electron trapping centers at the interlayer boundaries could also be the cause of leakage current reduction. The leakage current reduction in nanolaminates can also be due to electron trapping at the interfaces states at the end of leakage channels extending through single sublayers, thereby causing a decrease of the injecting electric field in the vicinity of these channels.

4.5.1 Growth of Ta_2O_5 – HfO_2 nanolaminates

Since both Ta_2O_5 and HfO_2 thin films on Si substrate were successfully fabricated by ALE, it is straightforward to grow Ta_2O_5 – HfO_2 nanolaminates by alternating the sequence of source materials. All the Ta_2O_5 – HfO_2 nanolaminates were deposited on nitrided silicon substrate at 300°C. A cross sectional view of the multilayer structure is shown in Fig. 4.15. By varying the number of cycles for each oxide constituent layer, one can determine the thickness of each intermediate layer and the total thickness of the stack.

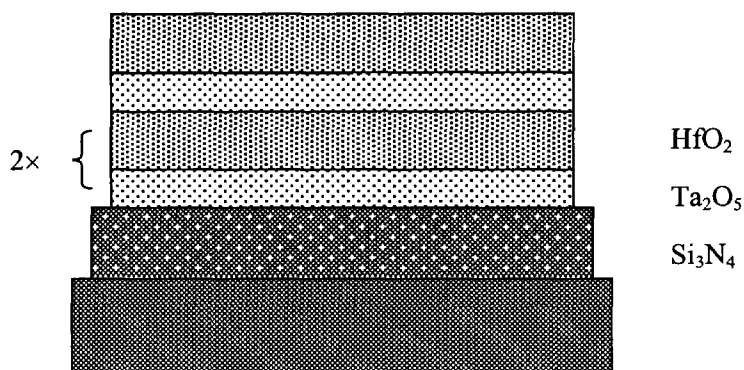


Fig. 4.15 Schematic cross-section view of a Ta_2O_5 – HfO_2 nanolaminates structure of $2 \times (\text{Ta}_2\text{O}_5 + \text{HfO}_2)$. The thickness of each constituent layer can be varied by number of reaction cycles. The silicon nitride layer is 2.76 nm thick.

For nanolaminates deposition, the pulses of source materials and N_2 purge time were increased to ensure a smooth interface between the different oxide constituent layers. For ultra thin nanolaminates a Ta_2O_5 seeding layer (5~10 cycles) was deposited before the sublayer was grown. The spectroscopic ellipsometer measured thickness was consistent with the thickness calculated from growth rate and number of reaction cycles. Our examination focused on very thin nanolaminates. The as-deposited Ta_2O_5 – HfO_2 nanolaminates were amorphous but crystallized after being annealed in a RTA furnace at 800°C for 30 s in either O_2 or Ar ambient. The strongest diffraction peaks appeared in the XRD patterns corresponded to the monoclinic phase of HfO_2 , while the Ta_2O_5 showed only very weak crystallization. The determination of film composition was not possible even with Rutherford Backscattering Spectrometry (RBS) technique because the atomic weights of Ta and Hf are too close to each other, and the mass resolution of RBS is limited for heavy elements. The refractive index of the nanolaminate was 2.1 at a wavelength of 632.8 nm. The dielectric properties of Ta_2O_5 – HfO_2 nanolaminates with varied thickness were studied and the detailed discussion will be presented in Chapter 5.

4.5.2 Growth of $\text{Ta}_2\text{O}_5 - \text{ZrO}_2$ nanolaminates

Similar to the process of $\text{Ta}_2\text{O}_5 - \text{HfO}_2$, $\text{Ta}_2\text{O}_5 - \text{ZrO}_2$ nanolaminates were deposited on silicon or nitrided silicon substrates at 300°C . The schematic side-view of the multi-layer structure is the same as Fig. 4.15 except the HfO_2 layer should be replaced by ZrO_2 film. Since both Ta_2O_5 and ZrO_2 stick very well on bare Si substrate and nitrided Si substrate (a thin layer of SiO_2 is formed at the interface again), it does not matter which oxide should be grown first. Only very thin $\text{Ta}_2\text{O}_5 - \text{ZrO}_2$ nanolaminates (10 nm or less) were grown on nitrided silicon substrates. The as-deposited $\text{Ta}_2\text{O}_5 - \text{ZrO}_2$ nanolaminates were also amorphous and was crystallized partially after 700°C annealing for 30 s in Ar or O_2 . It is evident that a strong reflection peak of metastable t- ZrO_2 and two weak peaks of crystalline Ta_2O_5 appeared, indicating the existence of nano-size crystallite phases. For nanolaminates with extremely thin constituent layer, for example, less than 5 nm, no obvious crystal sites would be detected by the X-ray diffractometer. This is due to the less chance for crystal growth for each oxide layer during the short exposure time of each precursor or X-ray could not detect the microcrystalline structure. The optical properties were characterized by spectroscopic ellipsometer. The refractive index was 2.0 and extinction coefficient was zero throughout the visible and near infrared region, which indicates that this film was optically transparent.

4.5.3 Growth of $\text{ZrO}_2 - \text{HfO}_2$ nanolaminates

The procedure for growing $\text{ZrO}_2 - \text{HfO}_2$ nanolaminates is very much similar to that of the above two kinds of nanolaminates. More attention has been paid to sequence of binary oxide deposition on pure Si due to the unstable film formation when HfO_2 was first deposited on Si. Therefore, during all the $\text{ZrO}_2 - \text{HfO}_2$ nanolaminates deposition, ZrO_2 was grown first in contact with the Si/ SiO_2 interface. Even this order does not have to be kept in the case of nitrided Si substrate, most nanolaminates of $\text{ZrO}_2 - \text{HfO}_2$ on nitrided Si were grown in the same order since no difference in thickness from these two

orders was observed. The crystallization temperature of $\text{ZrO}_2 - \text{HfO}_2$ nanolaminates is higher than that of $\text{Ta}_2\text{O}_5\text{-ZrO}_2$. It required 800°C to achieve partial crystallization for relatively thick $\text{ZrO}_2 - \text{HfO}_2$ nanolaminates. It should be noted that only film with thickness less than 20 nm were investigated in details and the thickness of each constituent layer was less than 5 nm. There could be micro-crystallite structure with sub-nanometer scale, thus the XRD examination did not show any strong crystallization peaks.

So far in this chapter, the depositions of the binary oxides and nanolaminates have been described. Each film requires independent study related to the process parameters such as source temperatures, pulse times, purge duration and anneal temperature. The initial characterizations of these films were focused on crystalline structure and uniformity. The electrical and dielectric properties will be presented in Chapter 5.

References

- [1] W. Kong, "Growth and characterization of thin film electroluminescent devices fabricated using atomic layer epitaxy," Ph.D. Dissertation, Oregon Graduate Institute, 1996, p. 31.
- [2] H. Shinriki and M. Nakata, "UV-O₃ and Dry-O₂: Two-step annealed chemical vapor deposited Ta₂O₅ films for storage dielectrics of 64-Mb DRAM's," IEEE Trans. Electron Devices **38**, 1991, pp. 455-462.
- [3] S. Kamiyama, P. Y. Lesaicherre, H. Suzuki, A. Sakai, I. Nishiyama, and A. Ishitani, "Ultrathin tantalum oxide capacitor dielectric layers fabricated using rapid thermal nitridation prior to low temperature chemical vapor deposition," J. Electrochem. Soc. **140**, 1993, pp. 1617-1624.
- [4] Y. Takaishi, M. Sakao, S. Kamiyama, H. Suzuki, and H. Watanabe, "Low temperature integrated process below 500°C for thin Ta₂O₅ capacitor for giga-bit DRAMs," IEEE IEDM, San Francisco, CA, Dec. 11-14, 1994, p. 839-840.
- [5] K. F. Schuegraf, "Reliability of thin SiO₂ at direct-tunneling voltages," IEEE IEDM, San Francisco, CA, Dec. 11-14, 1994, p. 609-612.
- [6] G. S. Orhrlein, "Oxidation temperature dependence of the dc electrical conduction characteristics and dielectric strength of thin Ta₂O₅ films on silicon," J. Appl. Phys. **59**, 1986, pp. 1587-1595.
- [7] S. O. Kim and H. J. Kim, "Fabrication of n-metal-oxide semiconductor field effect transistor with Ta₂O₅ gate oxide prepared by plasma enhanced metal organic chemical vapor deposition," J. Vac. Sci. Technol. **B12**, 1994, pp. 3006-3009.
- [8] M. Ritala, M. Leskela, L. Niinisto, T. Prohaska, G. Friedbacher, and M. Grasserbauer, "Surface roughness reduction in atomic layer epitaxy growth of titanium dioxide thin films," Thin Solid Films **250**, 1994, pp. 155-162.
- [9] C. T. Kuo, R. Kwor, and K. M. Jones, "Study of sputtered HfO₂ thin films on silicon," Thin Solid Films **213**, 1991, pp. 257-264.
- [10] J. A. Britten, H. T. Nguyen, S. F. Falabella, B. W. Shore, M. D. Perry, and D. H. Raguin, "Etch-stop characteristics of Sc₂O₃ and HfO₂ films for multiplayer dielectric grating applications," J. Vac. Sci. Technol. **A14**, 1996, pp. 2793-2795.

- [11] G. Johner and K. K. Schweitzer, "Thermal barrier coatings for jet engine improvement," *Thin Solid Films* **119**, 1984, pp. 301-315.
- [12] Y. Ma, Y. Ono, L. Stecker, D. R. Evans, and S. T. Hsu, "Zirconium oxide based gate dielectrics with equivalent oxide thickness of less than 1.0nm and performance of submicron MOSFET using a nitride gate replacement process," *Applied Surface Science*, **75**, 1994, pp. 333-340.
- [13] C. S. Hwang and H. J. Kim, "Deposition and characterization of ZrO_2 thin film on silicon substrate by MOCVD," *J. Mater. Research* **8**, 1993, pp. 1361-1367.
- [14] J. Si, S. B. Desu, and C-Y Tsai, "Metal-organic chemical vapor deposition of ZrO_2 films using $\text{Zr}(\text{thd})_4$ as precursors," *J. Mater. Research* **9**, 1994, pp. 1721-1727.
- [15] M. Ritala and M. Leskela, "Zirconium dioxide thin films deposited by ALE using zirconium tetrachloride as precursor," *Applied Surface Science* **75**, 1994, pp. 333-340.
- [16] K. Kukli, M. Ritala, and M. Leskela, "Dielectric oxide nanolaminates deposited by atomic layer epitaxy," *Electrochem. Soc. Proc.* **25**, 1997, pp. 1137-1144.

Chapter 5

Characterization of MOS Structures with High k Insulators

Dielectric properties of binary oxides and nanolaminates are presented in this chapter. Material properties were characterized using variety of techniques. Film surface roughness was analyzed by an atomic force microscope (AFM). Chemical analysis was performed using FTIR. Composition profiles of different films were obtained from secondary ion mass spectroscope (SIMS). The electrical and optical properties were evaluated of thin films with different thicknesses. Dielectric constant was extracted from capacitance-voltage measurement. The dielectric constant decrease with film thickness is discussed. Gate leakage current mechanisms are presented for as-deposited and annealed thin films. The capacitance-voltage characteristics were measured with an HP4275 LCR meter. The current-voltage characteristics were analyzed using HP4145B parameter analyzer. The average thickness of binary oxides and nanolaminates were measured with an ellipsometer. Some thicknesses were verified by transmission electron microscope and SIMS profiles.

5.1 Nitrided silicon substrate

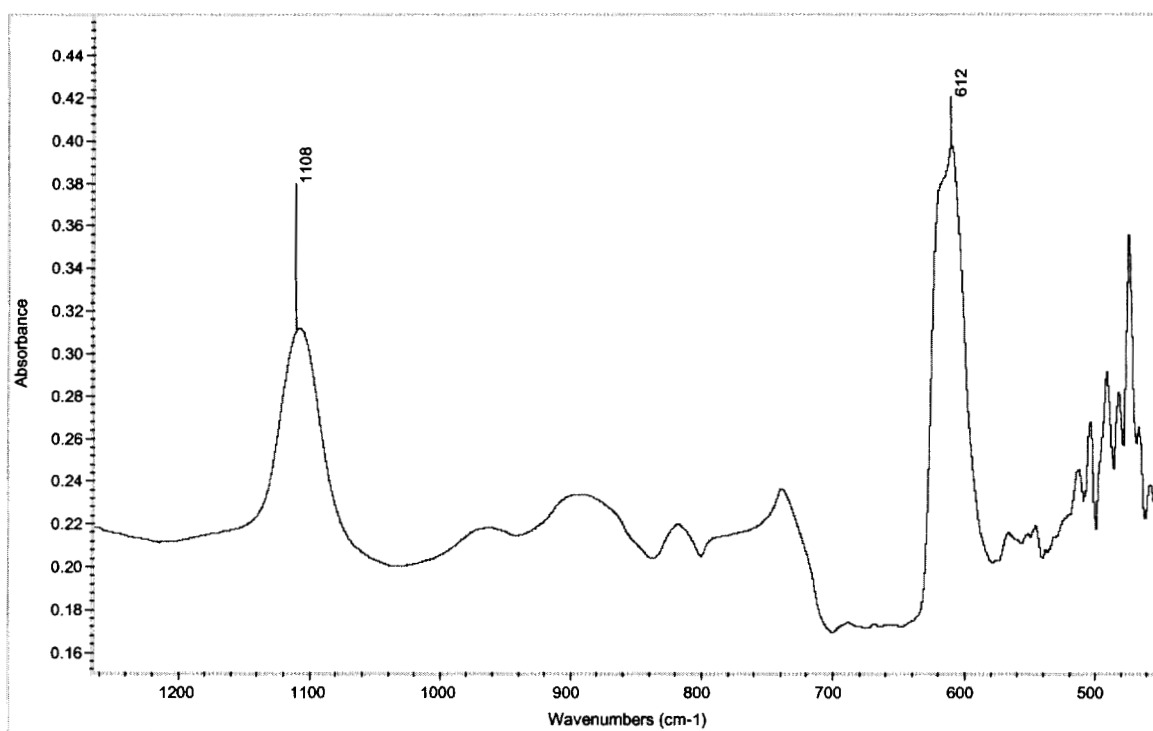
As we discussed in chap 4, silicon nitride was grown by RTP to act as a buffer layer to prevent the oxidation of silicon substrate during the high dielectric constant film growth. Our wafer came with the nitride layer. To reveal the doping concentration of the

Si substrate, the nitride layer was etched off by boiling in 75% phosphoric acid at 180°C. An aluminum dot was deposited on the exposed Si surface. C-V method was used to explore the doping level of the substrate according to the following equation [1]

$$N_A = \frac{2}{qk_s \epsilon_0 A^2 [d(1/C^2)/dV]} \quad (5.1)$$

where ϵ_0 is permittivity of free space, k_s is the dielectric constant of the substrate, A is the area of the aluminum dot. The calculated doping concentration was about $1.0 \times 10^{15} \text{ cm}^{-3}$. The FTIR spectrum of the nitrated substrate also indicated that the substrate was not heavily doped as shown in Fig. 5.1. The IR peak at 1108 cm^{-1} indicated interstitial oxygen atoms in Si lattice, and the peak at 612 cm^{-1} is due to substitutional carbon impurities in Si lattice. All other peaks are the phonon modes from the Si substrate. The nitride layer is fully transparent to the IR, so we were able to extract some information of the substrate underneath.

The surface roughness measurement of the silicon nitride layer was done using an atomic force microscope (AFM) as shown in Fig. 5.2. It was interesting to examine the roughness of the high dielectric film and compare it to the underlying nitride.



**Fig. 5.1 FTIR spectrum of the nitrided Si substrate.
The thickness of the nitride layer is 2.76nm.**

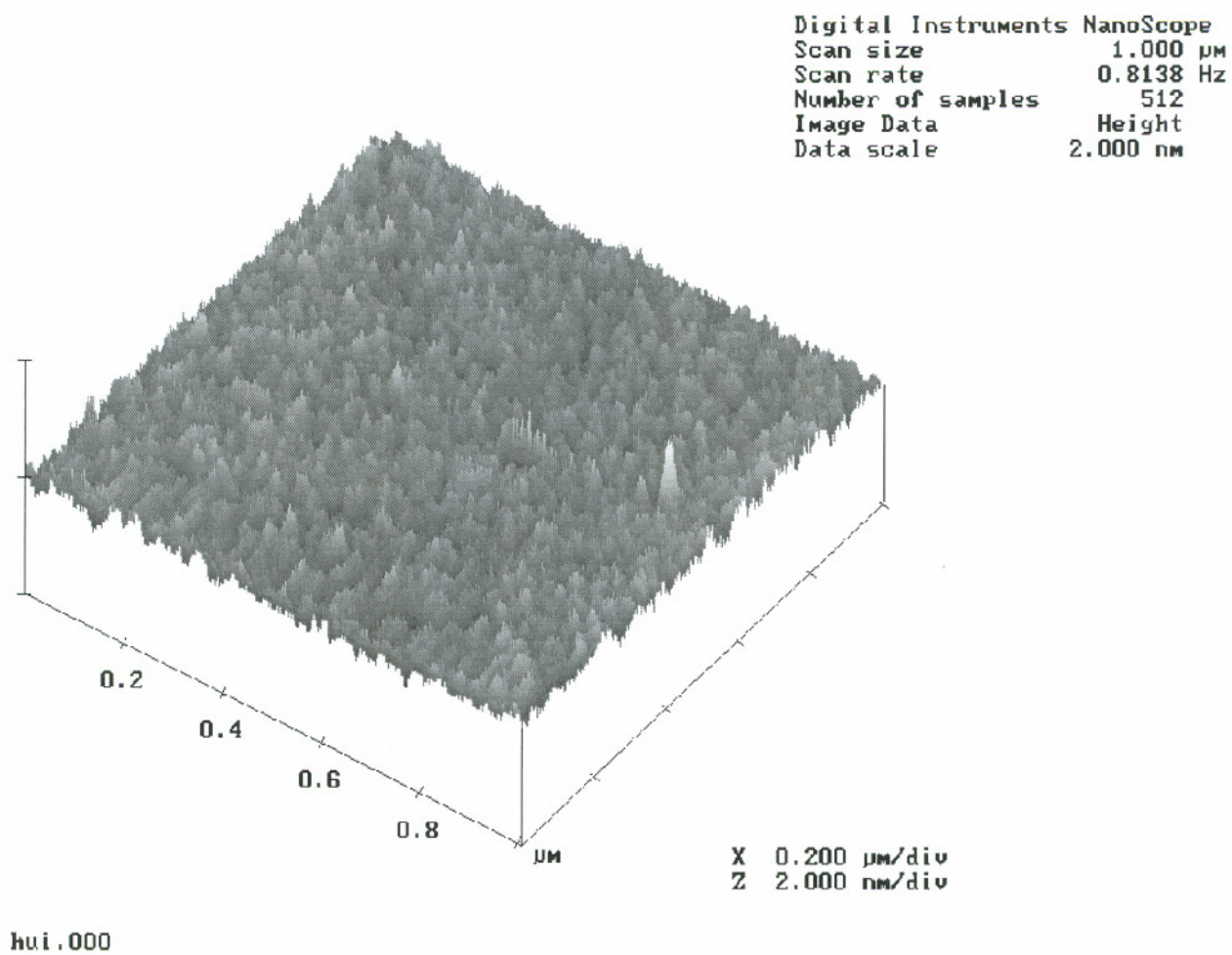


Fig. 5.2 AFM image of the silicon nitride layer of 2.76 nm, grown by rapid thermal annealing at 1000°C in ammonium for 30 s.

5.2. Material and electrical characterization of binary oxides

Al - Oxide - Si MOS structures were fabricated to determine the dielectric properties of binary oxide thin films. The Al dots of 0.4 ~ 0.6 mm diameter were evaporated on the top of the ALE grown oxides to define the MOS structures. The backsides of all these substrates were also aluminized to ensure a good back contact.

5.2.1. Ta₂O₅ thin films

The dielectric constant of an insulator can be calculated by the capacitance-voltage measurement of a MOS capacitor in deep accumulation region. Bulk Ta₂O₅ grown by ALE has a relatively high dielectric constant ($k = 27$). In our investigation, Ta₂O₅ was initially deposited on bare silicon substrates that were pre-cleaned and dipped in HF prior to loading into the reactor. The time between the HF dip and loading the sample into the ALE reactor was kept below 30 s to reduce any chances of oxidation. XRD analysis indicated these Ta₂O₅ films to be amorphous as described in chapter 4. Secondary ion mass spectroscopy (SIMS) characterization showed the films to be stoichiometric, with no trace of chlorine. Two Ta₂O₅ films were made for AFM study. Both samples were grown on nitrided Si at 300°C. In Fig. 5.3, Sample #322b1-2 was grown for 1000 cycles, which led to a thickness of about 55 nm; Sample 351b1-1 was grown for 80 cycles, which led to a thickness of about 4.4 nm. Both films were amorphous but the roughness of the thicker film is obviously more severe than that of the thinner film. This phenomenon has been reported by other authors [2,3]. It is interesting to see that the thinner Ta₂O₅ film showed a smoother surface compared to the underlying Si₃N₄. Spectroscopic ellipsometry analysis showed that the as-deposited film of 75 nm had a refractive index of around 2.18 at 632.8 nm as shown in Fig. 5.4.

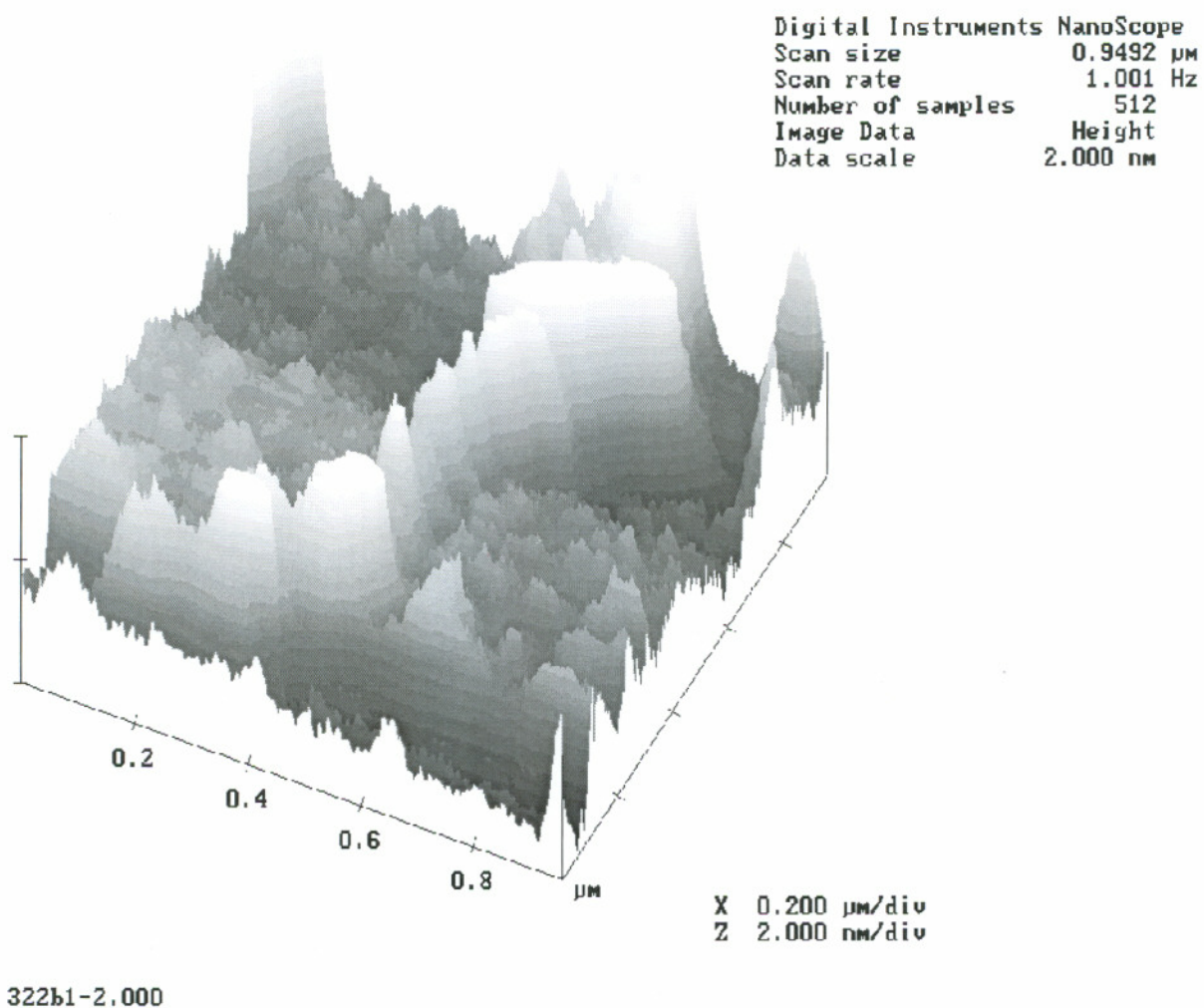


Fig. 5.3a AFM image of sample #322b1-2 on Si at 300°C for 1000 cycles
(thickness \approx 55nm)

We observed a significant difference in the dielectric properties for thick and thin films. For example, the k value of the 11.6 nm films was only 10 and a corresponding leakage current density was 6×10^{-6} A/cm² at 1 MV/cm. The values of k are significantly smaller than 27 which we had obtained from 75 nm thick Ta₂O₅ grown on Si. These results are summarized in Table 5-1. As suspected, TEM cross-sectional profile of the thin Ta₂O₅ film of 11.6 nm on bare Si showed a 1.5 nm thick layer of SiO₂ at the Si substrate/Ta₂O₅ film interface, as showed in chapter 4. Apparently the silicon surface is getting oxidized during the initial growth phase of Ta₂O₅ due to the presence of water vapor. Hence, the measured k value is that of the Ta₂O₅ and SiO₂ capacitors in series. Dielectric constant of Ta₂O₅ in this stack can be calculated according to Eqn. 5.2 and Eqn. 5.3. If we subtracted the effect of the 1.5 nm SiO₂ and assuming k of SiO₂ is 3.9, then the k value of the tantalum oxide film is 13.

$$\frac{1}{C_{meas(accum)}} = \frac{t_{SiO_2}}{\epsilon_{SiO_2}} + \frac{t_{Ta_2O_5}}{\epsilon_{Ta_2O_5}} \quad (5.2)$$

where $C_{meas(accum)}$ is the capacitance per unit area of the MOS structure in the accumulation region.

The effective dielectric constant of the Ta₂O₅ can then be derived from Eqn. 5.2,

$$\epsilon_{Ta_2O_5} = \frac{C_{meas(accum)} \epsilon_{SiO_2} t_{Ta_2O_5}}{\epsilon_{SiO_2} - C_{meas(accum)} t_{SiO_2}} \quad (5.3)$$

This equation can also be used for other interfacial layers instead of silicon oxide layer. For different stacks, it is hard to find the thickness of SiO₂ since its thickness varies with the thickness of the grown high k layer. Therefore, we will only consider the effective dielectric constant of the whole stack in most cases since we can not get a TEM picture for each film stack.

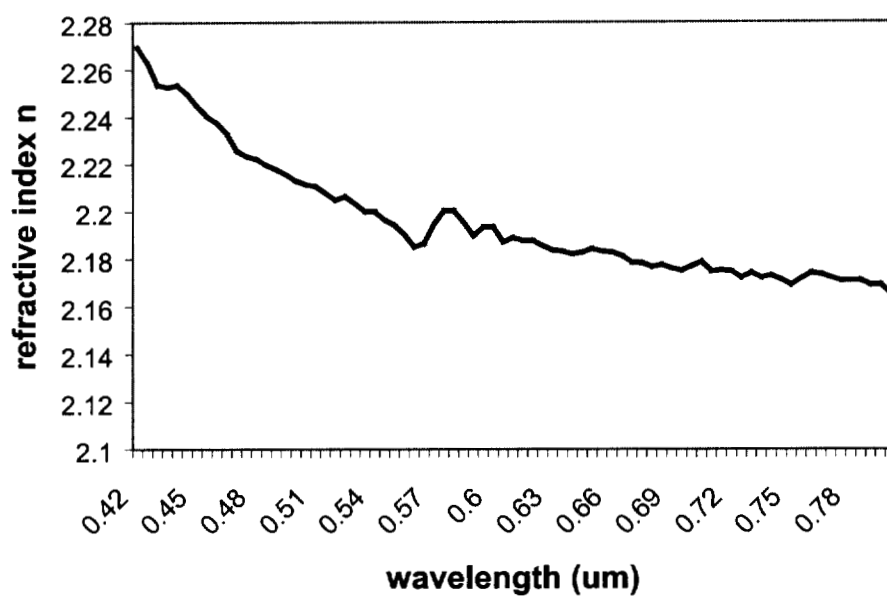


Fig. 5.4 Refractive index of as-deposited Ta_2O_5 film of 75 nm in the visible region.

Table 5-1 Electrical properties of Ta_2O_5 thin film grown on p-type Si substrate, where a thin layer of SiO_2 exists at the interface due to the Si oxidation.

Total Thickness (nm)	Dielectric constant	Leakage current density (A/cm^2)(at -1 V)
75	27	5.0×10^{-11}
36	15	1.0×10^{-11}
12.1	10	6.0×10^{-6}

In order to eliminate the native oxide growth, subsequent silicon substrates used were passivated with a 2 nm thick aluminum or a layer of silicon nitride of 2.76 nm or 2.12 nm thick. The idea of using Al as a passivation layer on Si was considered because Al has the heat of formation was reported to be higher than that of SiO_2 , thus it would form aluminum oxide readily when exposed to water on the Si substrate. Al_2O_3 films have a dielectric constant of 8.7 ~ 12.3 depending on the growth techniques. The Al_2O_3 film grown by ALE has the k of 12.3. The Al_2O_3 layer would also act as a barrier layer for further Si oxidation.

In this study, the Al was evaporated on Si at room temperature. Dielectric properties of Ta_2O_5 films grown on Al passivated Si is summarized in Table 5-2. It is obvious that for thicker films, the dielectric properties are very close to bulk value for both as-deposited film and annealed film. Annealing caused the film to crystallize. Crystallization had more effect in increasing the dielectric constant for thinner film, and it also caused an increase in the leakage current due to the existence of grain boundaries that act as conductance channels. Using Al as a passivation layer is not an ideal method if we think about the low melting point of Al ($\sim 660^\circ\text{C}$) and the diffusion between Al-Si at about 400°C . For any Al not fully oxidized during the deposition of Ta_2O_5 film, chances of melting Al and diffusion between Al-Si will introduce a complicated interface. In addition, TEM cross-sectional view indicated that the Al is not a good barrier layer for water vapor diffusion, a layer of SiO_2 was found at the interface of Si and Al_2O_3 layer. Furthermore, the interface of the high k layer and the Al_2O_3 layer was fairly rough and the thickness of Al_2O_3 layer was hard to control. Therefore, we decided to replace Al_2O_3 with silicon nitride as the passivation layer despite its relatively low dielectric constant compared to that of Al_2O_3 .

Table 5-2 Ta₂O₅ films grown on Al passivated Si. The thickness of Al layer is 2 nm.

Thickness (nm)	RTP	Refractive index	Dielectric constant	Leakage current (A/cm ²) at -1 V
75	-	2.194	26	3.3×10^{-12}
75	1000°C in Ar for 10 s	2.195	27	5.0×10^{-11}
38	-	2.123	16	1.0×10^{-11}
38	1000°C in Ar for 10 s	2.228	19	6.2×10^{-11}

Silicon nitride has been used as a passivation layer for a long time. It behaves as a nearly impervious barrier to diffusion especially for moisture and sodium. It also has a relatively high dielectric constant (~ 7.8), which makes it attractive as a gate dielectric material. The nitride layer in this research was deposited by rapid thermal nitridation in ammonia ambient at 1000°C for 30 s or less. Ta₂O₅ films grown on nitrated silicon substrates showed no indication of an oxide layer at the interface. XRD analysis again showed amorphous films and ellipsometer measurements yielded refractive index (n) of 2.1 for films of 10 nm thick on silicon nitride.

The leakage current of as deposited Ta₂O₅ is generally quite large and is attributed to oxygen vacancies and impurities in the film. Several post deposition treatments in oxidizing environments have been proposed to alleviate these defects [4-6]. We have examined the effect of post deposition thermal treatment using rapid thermal anneal (RTA) of our samples in both argon and oxygen ambients. The purpose of using both gases was to investigate if the leakage of the ALE grown films was due to oxygen vacancies. Results of two of these samples annealed (for 60 s) in these environments at 700°C and 800°C are compared in Table 5-3. After the 700°C anneal for 60 s, the k values in both cases increase and the leakage currents increased, most likely due to partial

crystallization of the films. However, following the 800°C anneal, leakage current increased even more in the case of Ar ambient and decreased in the O₂ ambient. XRD scans showed presence of the polycrystalline phase in both cases.

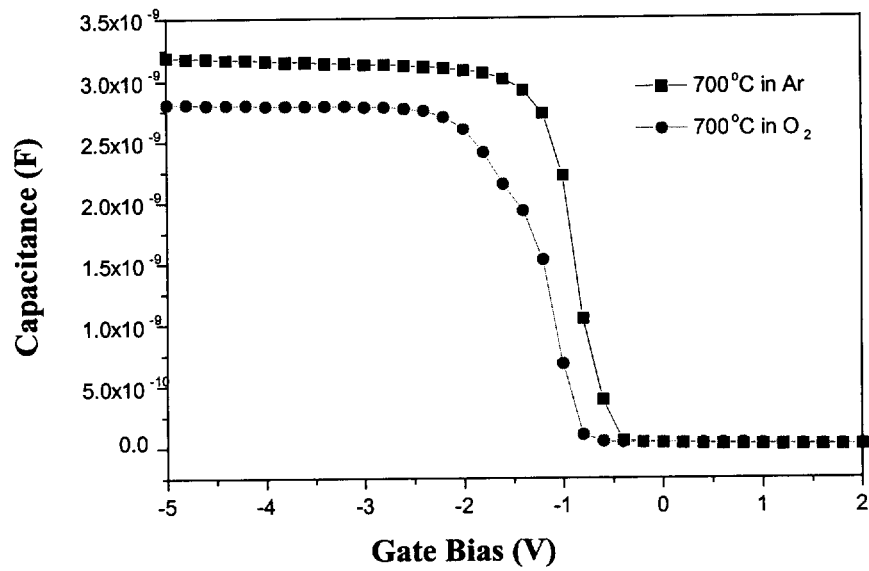
Table 5-3 Electrical properties of Ta₂O₅ / Si₃N₄ after RTA in argon and oxygen ambients.

Thickness(nm)	RTA for 60 s	Refractive index	Dielectric Constant	J (A/cm ²) at 1 MV/cm
17	None	2.2	15	2.5×10 ⁻⁹
16	700°C in Ar	2.24	21	5.6×10 ⁻⁸
16	700°C in O ₂	2.25	19	3.3×10 ⁻⁷
17	800°C in Ar	2.25	21	2.0×10 ⁻⁶
17	800°C in O ₂	2.24	21	1.9×10 ⁻⁸

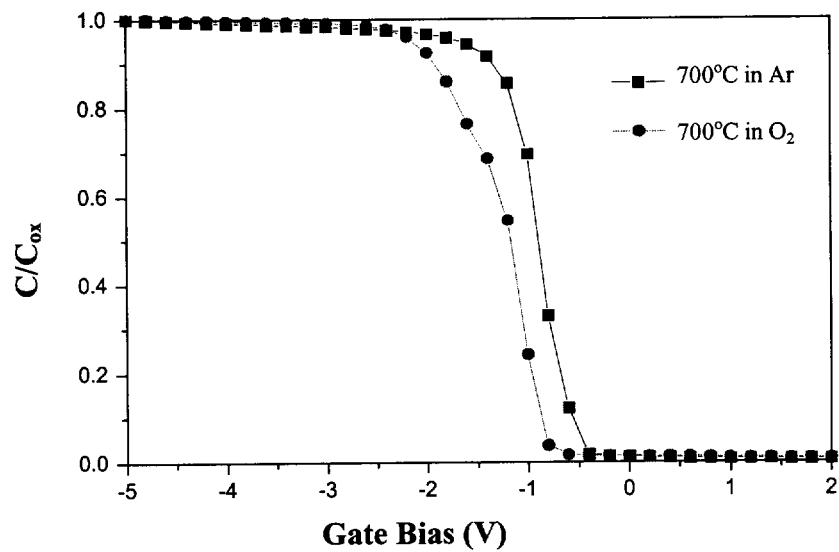
Fig. 5.5 shows the C-V curves of a 16 nm thick Ta₂O₅ film annealed at 700°C in Ar and O₂ for 60 s. The capacitance in accumulation region showed a slight difference. The dielectric constant varied from 21 for Ar annealing to 19 for oxygen annealing. A lateral shift of about 0.4 V was also seen between the two curves in (b), the normalized C-V curves. Assuming that this lateral shift is due to difference of fixed charge located near the interface, its charge density can be calculated from

$$N = \frac{C_{ox} \Delta V}{q} \quad (5.4)$$

which is approximately 10¹⁰ cm⁻².



(a)



(b)

Fig. 5.5 High frequency C-V curves for 16 nm thick of Ta_2O_5 annealed at 700°C for 60 s in Ar and O_2 . (a) C-V curve, (b) Normalized C-V curve.

The C-V characteristics of Ta_2O_5 films annealed at 800°C is shown in Fig. 5.6. It is apparent from the C-V traces that annealing in oxygen reduces the interface state charge although no attempt was made to measure the D_{it} quantitatively at this point. The stretch-out in the C-V curve was due to the interface state charges [7]. The stretch-out for the O_2 annealed thin film is much less severe than that observed in the Ar annealed sample, this also indicated a thermal silicon oxide layer could be formed at the Si surface that reduced the interface charge density significantly. As the Si surface oxidized, the thin layer of SiO_2 will adversely affect the dielectric constant due to the low dielectric constant of SiO_2 .

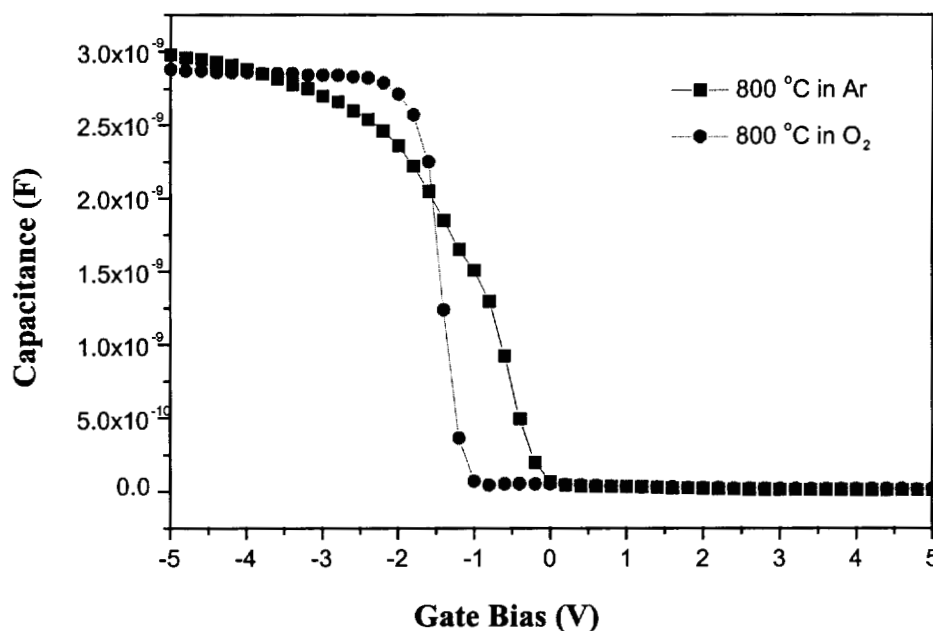


Fig. 5.6 High frequency C-V curves for 17 nm thick of Ta_2O_5 annealed at 800°C for 60 s in Ar and O_2 .

The leakage current also indicated a small discrepancy at 700°C for the two annealing ambients as shown in Fig. 5.7. It is surprising that the film annealed in O₂ is slightly more leaky than that annealed in Ar. However the difference is within an order of magnitude and we think it is within allowed margin of error. This indicated that the leakage current in ALE grown dielectric thin films is not due to the oxygen vacancies. There is a significant difference in the leakage current density for the films annealed at 800°C in Ar and O₂. In the case of O₂ anneal, very low current was obtained at gate voltage lower than 2 V, then the leakage current increased as the gate voltage increased. We believe the onset of the increase in current is due to the tunneling current through the extremely thin silicon oxide layer (~ 1-2 nm) formed at the surface at high electric field. Here the crystallization of thin film and the existence of the thin silicon oxide layer play competitive roles in determination of the leakage current. The partial crystallization contributed to higher leakage current while silicon oxide layer reduced the leakage current dramatically. It is not surprising to note that the leakage current of 800°C-annealed film in Ar is two orders higher than the same thick film annealed in oxygen. We believe it is the presence of grain boundaries that facilitates the leakage current flow. There was no significant difference in dielectric constants of the films annealed in Ar and O₂, therefore the dielectric films grown by ALE do not seem to have high density of oxygen vacancies.

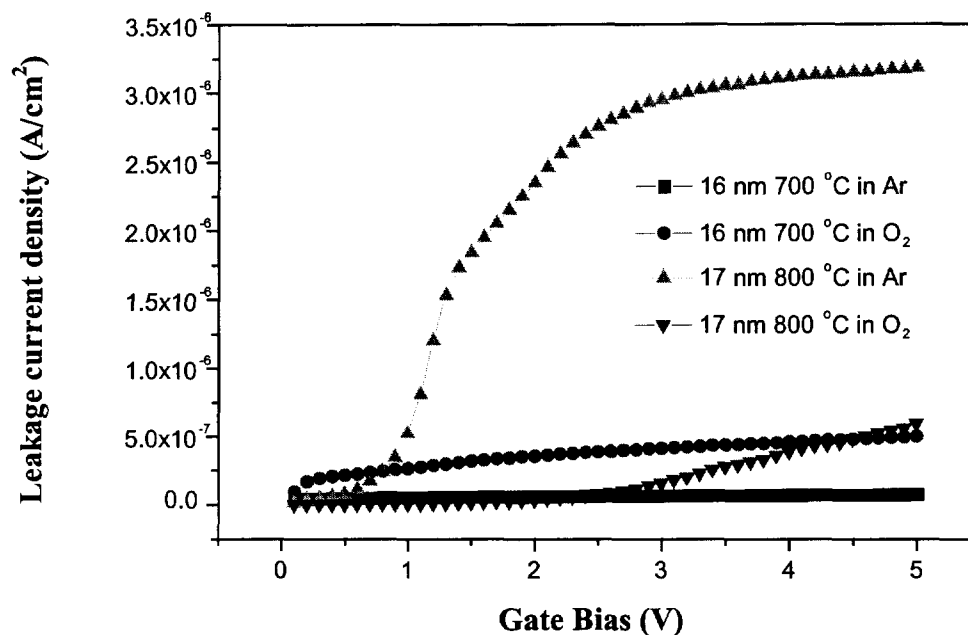


Fig. 5.7 The leakage current density of MOS capacitors with 16 nm and 17 nm thick Ta₂O₅ gate dielectric layers and under different annealing conditions.

The temperature dependence of leakage current was studied by measuring the I-V characteristics of thin films on a heated chuck. Fig. 5.8 shows the representative DC current-temperature plots at a bias of +2.0 volts for the as-deposited Ta₂O₅ film and Ar annealed film, as a function of substrate temperature. Anneal in Ar ambient will introduce crystallization thereby increase the leakage current. J/T^2 is found to follow standard Arrhenius behavior.

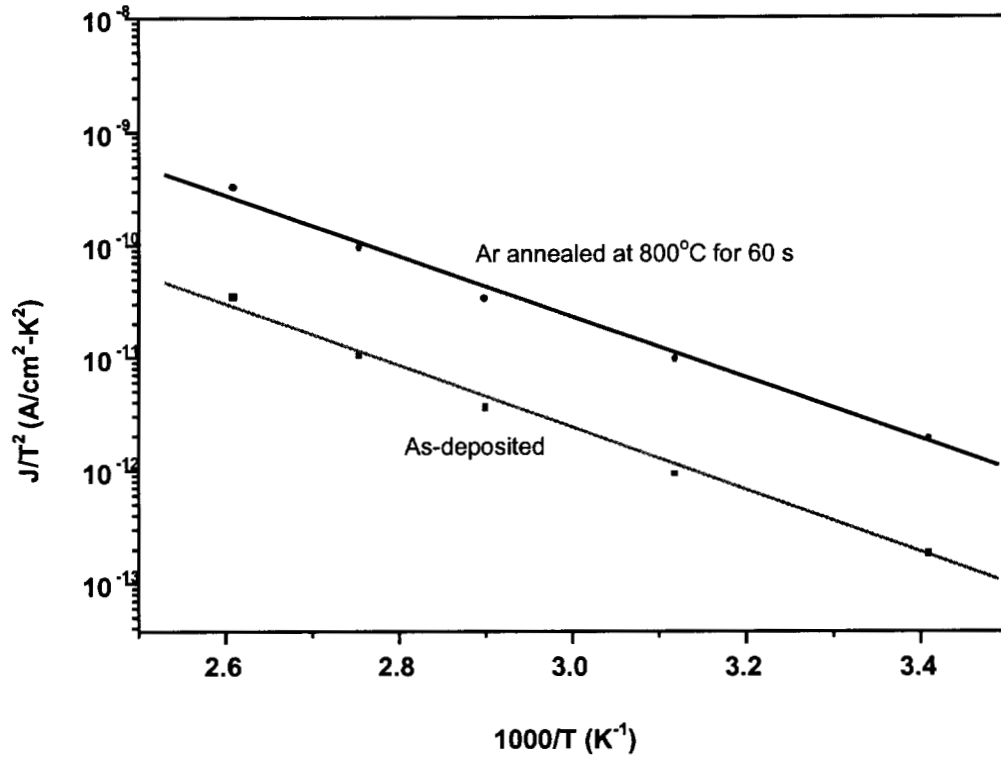


Fig. 5.8 J/T^2 plots of gate leakage current under positive gate bias +2.0 volts for as-deposited and Ar annealed Ta_2O_5 film of 17 nm.

From Eqn. 5.5 of thermionic emission current,

$$J_{th} = \frac{4\pi m^* q}{h^3} k^2 T^2 \exp\left(-\frac{q[\Phi_B - \sqrt{qE/4\pi\epsilon_{ox}}]}{kT}\right) \quad (5.5)$$

we have

$$\ln \frac{J_{th}}{T^2} = -\frac{q[\Phi_B - \sqrt{qE/4\pi\epsilon_{ox}}]}{kT} + \ln \frac{4\pi m^* q k^2}{h^3} \quad (5.6)$$

the barrier height can then be extracted from the slope of the above equation

$$\Phi_B = -k \cdot \text{slope} + \sqrt{\frac{qE}{4\pi\epsilon_{ox}}} \quad (5.7)$$

The calculated barrier height was approximately 0.68 eV for the as-deposited Ta₂O₅ film, whereas the Ar annealed film had a barrier height of 0.64 eV. It should be noticed that the permittivities of the two films were different. After anneal, the permittivity increased from 15 to 21. This slight decrease in barrier height with Ar anneal may be due to the crystallization of the film or it may represent a change in the band structure or a change in the charge state or strain at the Ta₂O₅/Si₃N₄ interface.

When the films were made thinner, although the value of refractive index kept increasing slightly, the k value kept dropping as shown in Table 5-2. We do not believe that the drop in k value with the film thickness was due to the inferior property of the film. The little change in the refractive indices of the thinner films indicated that the quality of the thinner films was as good as that of thicker film or even better. Actually for the thinner film, the film density did not decrease, and the surface roughness was less severe compared to thicker films. It is more likely that reduction in k of thinner films (< 10 nm) was due to fewer bulk dipole moments between the two surfaces. In other words, the two surfaces of the ultra-thin film experience more of the outside world than the bulk between them, as discussed in ref. [8]. In our investigation, we found a significant drop in k values for films below 10 nm thick. Dielectric films with high k values are expected to be more affected by reduction of their thickness than low k materials.

5.2.2. HfO₂ and ZrO₂

Zirconium and hafnium oxides grown by ALE have bulk k values of 21 and 16, respectively. Hf forms the most stable oxide with the highest heat of formation ($\Delta H_f = 271$ Kcal/mol) among the elements in group IVA of the periodic table (Ti, Zr, Hf). HfO₂ film is very resistive to impurity diffusion and intermixing at the interface because of its high density (9.68 g/cm³). In addition, HfO₂ is compatible with n⁺ polysilicon gate without any barrier materials. ZrO₂ is also one of the most promising candidates for high k material. It has a large energy bandgap from 5.16 to 7.8 eV [9,10], low leakage current, and can be etched in HF solution. In this study, both of these oxides were initially deposited on bare Si substrates, and subsequently on silicon nitride passivated Si as for the tantalum oxide. SIMS analysis showed both these films to be stoichiometric with no detectable chlorine. Refractive indices of HfO₂ and ZrO₂ were 2.1 and 2.15, respectively. The trends described above in the k values and leakage currents as the film thickness was reduced were again seen with these oxides.

For HfO₂ films grown on Si, the k value dropped from 16 for 27.6 nm thick films to 10 for 15 nm thick film on silicon. For the oxide films deposited on nitrated wafer, the dielectric constant of films with different thicknesses are tabulated in Table 5-4. The C-V characteristics are presented in Fig. 5.9.

Table 5-4 Electrical properties of HfO₂/ Si₃N₄ with the thickness of Si₃N₄ about 2.76nm or 2.12nm.

Thickness (nm) HfO ₂ / Si ₃ N ₄	Dielectric constant	Leakage current (A/cm ²)
24.8/2.76	16	1.4×10^{-8}
9.84/2.76	11	5.2×10^{-8}
11/2.12	10	4.7×10^{-8}
5.7/2.12	8	9.0×10^{-8}

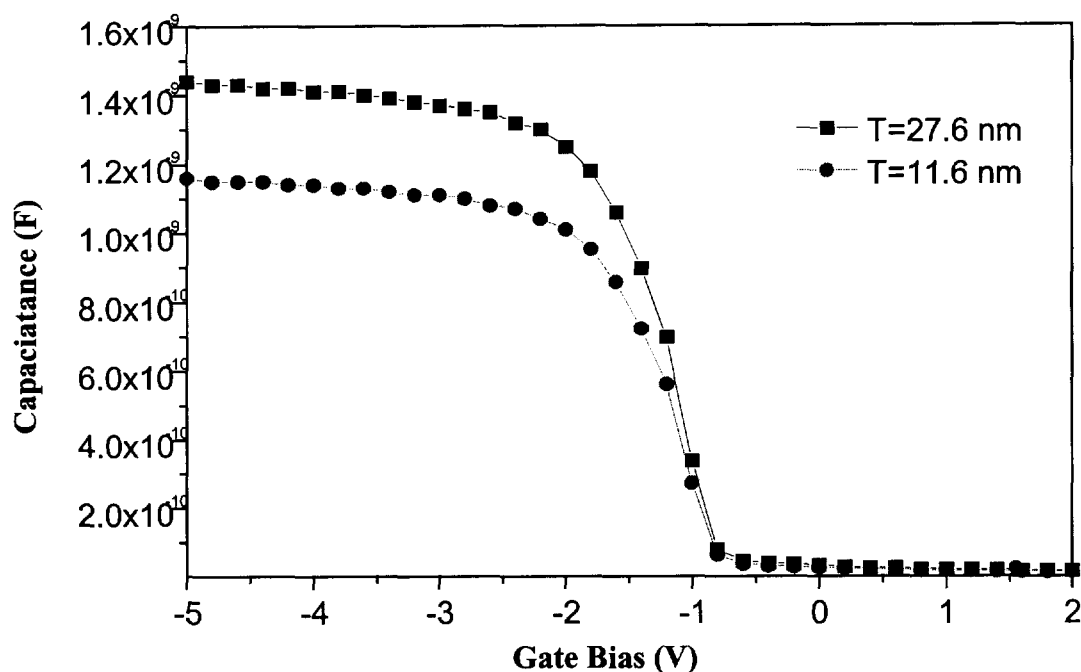


Fig. 5.9 C-V characteristics of the HfO₂ thin films with thicknesses 27.6 nm and 11.6 nm respectively. The thicknesses include 2.76 nm of nitride. The area of the capacitor is 0.0028 cm².

In the case of ZrO₂ deposited on bare Si substrates, k value was 21 for 23 nm thick film and dropped to 16 for 17.8 nm thick film. A series of thinner films were grown on nitrated substrates as presented in Table 5-5.

Table 5-5 Electrical properties of ZrO₂/ Si₃N₄ with the thickness of Si₃N₄ about 2.76nm/2.12nm.

Thickness (nm) ZrO ₂ / Si ₃ N ₄	Dielectric constant	Leakage current (A/cm ²)
6.5/2.76	10	9.4×10 ⁻⁸
18.4/2.12	21	1.7×10 ⁻⁸
8.7/2.12	10	9.0×10 ⁻⁸

It was interesting to note that HfO₂ films had the lowest leakage current of the three oxides examined. Also, the adhesion of HfO₂ films was significantly better on

nitrided Si than on bare Si surfaces. The surface chemistry of the HfO_2 films growth on Si by ALE is not well understood, but it does not affect the use of HfO_2 films to improve the dielectric properties of Ta_2O_5 when a nitride layer is used as a passivation layer.

5.3 Material and electrical characterization of nanolaminates

It has been shown that thin alternating layers (or nanolaminates) of insulators can be grown to produce a composite film whose insulating properties can be adjusted. The materials used for improving the dielectric properties of Ta_2O_5 have been HfO_2 , ZrO_2 and Al_2O_3 . We have examined Ta_2O_5 - HfO_2 , ZrO_2 - HfO_2 , and Ta_2O_5 - ZrO_2 nanolaminates that were grown on aluminum or nitride passivated silicon substrates.

5.3.1 Ta_2O_5 - HfO_2 nanolaminates

As we did for the Ta_2O_5 film, our initial work on Ta_2O_5 - HfO_2 nanolaminates was performed on Al coated Si substrates. Two sets of nanolaminates were grown by ALE. Sample #1, #2, #3 and #4 were deposited at the same condition. Sample #1 and #2 were from the same run and so were #3 and #4. Small variations in thickness were observed from run to run. For as-deposited films, the ellipsometry measured thickness of as-deposited film matched well (deviation less than 5%) with the calculated thickness based on the growth rate of each constituent film. However, the thickness of annealed film measured by an ellipsometer showed obvious difference from what the TEM picture indicated. For example, samples #1 showed a thickness of 17 nm from ellipsometry but TEM presented a total thickness of 21 nm, including the high k layer (14.2 nm) and $\text{Al}_2\text{O}_3/\text{SiO}_2$ (6.8 nm). Several issues need to be considered here. First, Al was proved not to be an ideal barrier for the water vapor as we pointed out earlier in this chapter. It was clear that a layer of SiO_2 was formed at the Si surface. Annealing process helped in increasing the thickness of SiO_2 by extracting oxygen from Ta_2O_5 and Al_2O_3 . Therefore we obtained a lower dielectric constant and lower leakage current for the annealed

samples due to the existence of the $\text{Al}_2\text{O}_3/\text{SiO}_2$ stack. The dielectric characteristic dependence on annealing is summarized in Table 5-6.

Secondly, it is interesting to note that there was no appreciable difference in dielectric constant for the two different stacks of nanolaminates with the same total thickness if the thickness ratio of each binary oxide is kept the same in both stacks. We chose the number of Ta_2O_5 growth cycles to be twice as that of HfO_2 layer because the growth rate of Ta_2O_5 is about half of that of HfO_2 . To get the nanolaminates containing the same thickness of Ta_2O_5 and HfO_2 , the growth cycles of each constituent layer must be optimized accordingly. In fact, we would like to introduce less HfO_2 to keep the dielectric constant high and also achieve lower leakage current. However, we used the same number of growth cycles for the subsequent very thin multilayer films because it was hard to get uniform deposition as the number of growth cycle decreases.

A dramatic increase of dielectric constant was achieved after the high temperature rapid thermal annealing treatment. RTA caused the crystallization of nanolaminates and therefore increased the leakage current as well.

Table 5-6 The Ta₂O₅- HfO₂ nanolaminates grown on Al coated Si substrates with and without rapid thermal annealing.

Sample	Film stack	Thickness (nm)	RTP (950°C, in Ar,10 s)	Thickness after RTP (nm)	Dielectric constant	Leakage current (A/cm ²) at 1 MV/cm
#1	2(50 Ta ₂ O ₅ +25 HfO ₂)	15.2	Yes	21.0	11	5.1×10 ⁻⁸
#2	2(50 Ta ₂ O ₅ +25 HfO ₂)	15.4	No	-	19	3.5×10 ⁻⁷
#3	4(25 Ta ₂ O ₅ +12 HfO ₂)	14.1	Yes	-	11	4.7×10 ⁻⁸
#4	2(25 Ta ₂ O ₅ +12 HfO ₂)	14.2	No	-	18	5.8×10 ⁻⁷

Due to the unpredictable surface reaction of aluminum with water vapor on silicon substrate before and after annealing, a better diffusion barrier layer such as silicon nitride was used to replace the aluminum passivation layer for the subsequent nanolaminates deposition. A series of Ta_2O_5 - HfO_2 nanolaminates were grown on the 2.76 nm or 2.12 nm silicon nitride and characterized by C-V and I-V measurements. Results from these films were summarized in Table 5-7. We have analyzed Ta_2O_5 - HfO_2 nanolaminates of thickness less than 10 nm. When these ultra-thin nanolaminates were deposited on silicon nitride coated Si substrates, the first few cycles were used for growing a thin Ta_2O_5 film that acted as a seed layer. For this step, extended pulse time for TaCl_5 and N_2 purge were used. This was an effort to resolve the problem that the first few cycles of an ALE growth were not very uniform due to island growth. This problem would be more obvious for nanolaminates growth since alternate precursors were switched frequently. It was reported that the ALE film roughening has its origin in agglomeration, which was most intense during the very first few deposition cycles. Substrate surface cleanliness may also be an issue for the island growth for the first few cycles. For our nitrided substrates, no special cleaning was performed besides blowing with dry N_2 . However, once the grown film fully covered the substrate, the surface of subsequent film becomes smoother. An AFM image showed very uniform and flat surface as presented in Fig. 5.10.

Table 5-7 The Ta₂O₅- HfO₂ nanolaminates growth on nitrided Si substrates. The thickness of Si₃N₄ is 2.76 nm.

Sample	Film stack	Total Thickness (nm)	Dielectric constant	SiO ₂ equivalent thickness (nm)	Leakage current density (A/cm ²) at 1 MV/cm
#1	10 Ta ₂ O ₅ + 2(25 Ta ₂ O ₅ +25 HfO ₂)	10	12	3.25	2.0×10 ⁻⁷
#2	10 Ta ₂ O ₅ + 2(20 Ta ₂ O ₅ +20 HfO ₂)	9.6	10	3.74	1.7×10 ⁻⁷
#3	10 Ta ₂ O ₅ + 2(10 Ta ₂ O ₅ +10 HfO ₂)	8.0	10	3.12	3.8×10 ⁻⁸
#4	5 Ta ₂ O ₅ + 2(5 Ta ₂ O ₅ +5 HfO ₂)	6.8	10	2.65	1.2×10 ⁻⁸

Ultra thin Ta_2O_5 - HfO_2 nanolaminates ($5 \text{ Ta}_2\text{O}_5 + 2 \times (10 \text{ Ta}_2\text{O}_5 + 10 \text{ HfO}_2)$) were also studied by FTIR to determine if there was any oxidation occurring at the silicon surface during the ALE process. If silicon oxide is formed at the interface, this IR spectrum will show peaks for Si-O bonding. To check for the presence of the Si-O bond due to the interstitial oxygen in Si matrix, which exists before the nanolaminates process, the FTIR spectrum of nitrided substrate was also examined. A subtraction of these two IR spectra indicated that there was no Si-O bond forming due to the process, as shown in Fig. 5.11.

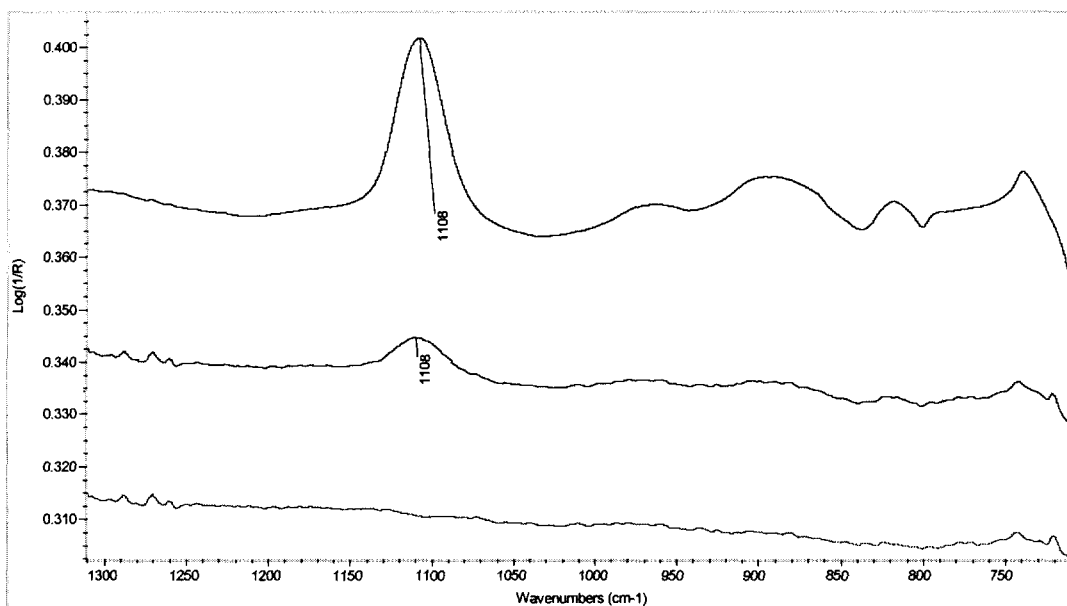


Fig. 5.11 FTIR spectra of $\text{Ta}_2\text{O}_5/\text{HfO}_2$ nanolaminates/ $\text{Si}_3\text{N}_4/\text{Si}$ and $\text{Si}_3\text{N}_4/\text{Si}$. The top curve is the spectrum of the nanolaminates, the middle one is nitrided silicon substrate, the bottom one is the subtraction of two curves showing that there is no SiO_2 forming at the interface.

X-ray reflectivity (XRR) was used to verify the total thickness and film density for nanolaminates on Si and on $\text{Si}_3\text{N}_4/\text{Si}$. Glancing angle θ - 2θ measurements were done using the Siemens D5000 XRD. It is evident that the thickness measured by spectroscopic ellipsometer was consistent with the XRR thickness (variation less than 3%). But the thickness from the single wavelength ellipsometer was 10-15% larger than that measured by the other two methods. XRR also measured the film density of 0.87-0.88 relative to bulk HfO_2 . No interfacial silicon dioxide was detected for the film grown on nitride. It proved that silicon nitride is an effective barrier layer against water vapor in this process.

Again the dielectric constants of nanolaminates were extracted from the C-V measurements. Fig. 5.12 is a typical high frequency C-V curve of as-deposited Ta_2O_5 - HfO_2 nanolaminates of 7.3 nm grown on 2.76 nm silicon nitride coated substrate, from which a dielectric constant of 12 was determined with the gate area of 0.0028 cm^2 . Hence this stack is electrically equivalent to 3.25 nm of SiO_2 . The leakage current at 1MV/cm was $2.0 \times 10^{-7} \text{ A/cm}^2$.

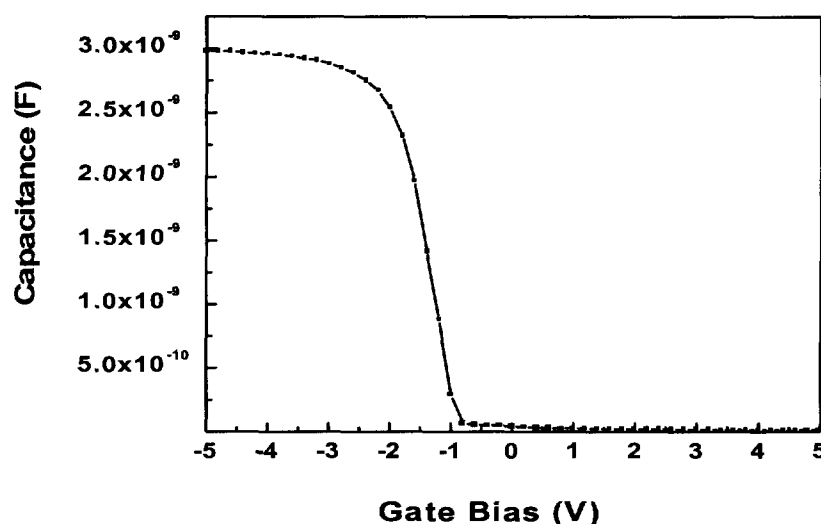


Fig. 5.12 C-V curve of the as-deposited Al- $\text{Ta}_2\text{O}_5/\text{HfO}_2$ - Si_3N_4 -Si (MIS) capacitor. The $\text{Ta}_2\text{O}_5/\text{HfO}_2$ nanolaminates contains $10\text{Ta}_2\text{O}_5+2(25 \text{Ta}_2\text{O}_5+25 \text{HfO}_2)$. The area of the capacitor is $2.8 \times 10^{-3} \text{ cm}^2$.

The flatband voltage is defined as the gate bias at which the transition from an accumulation to depletion in the surface of a MOS system occurs. It can be experimentally determined from C-V curve by plotting the $1/(C_{HF}/C_{OX})^2$ versus V_g . The lower knee of this curve occurs at $V_g=V_{FB}$. Such a transition is sometimes difficult to determine unambiguously. Differentiating this curve and finding the maximum slope of the left flank of this differentiated curve again results in a sharply peaked curve where the VFB is the gate bias corresponding to the peak position [11]. Fig. 5.13 indicated that for this Ta₂O₅-HfO₂ nanolaminates the flatband voltage (V_{FB}) is about -1.1 V.

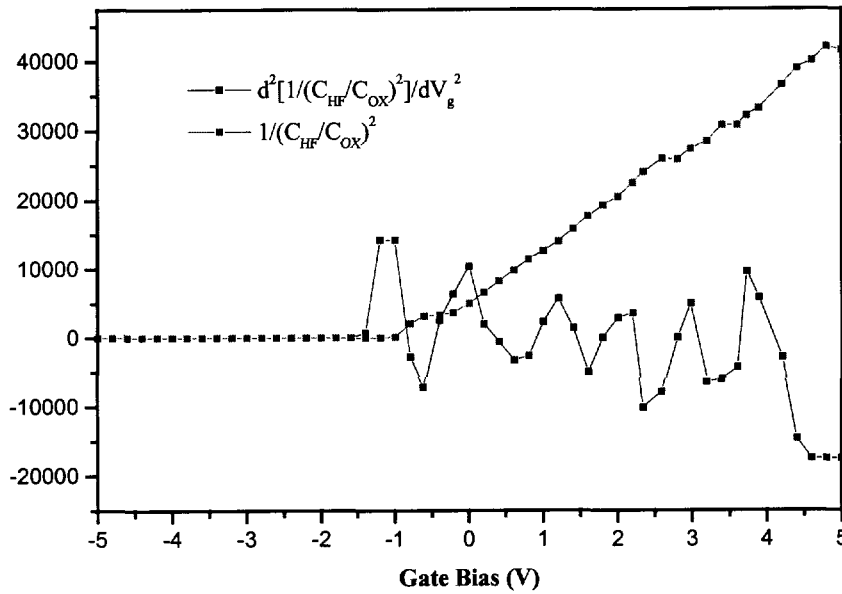


Fig. 5.13 Calculation of the flatband voltage from a C-V measurement. The gate voltage corresponds to the peak of $\frac{d^2}{dV_g^2} \left[\frac{1}{(C_{HF}/C_{ox})^2} \right]$ was the flatband voltage.

The fixed charge Q_f is related to the flatband voltage and gate-semiconductor work function difference by equation

$$Q_f = (\phi_{MS} - V_{FB})C_{ox} \quad (5.8)$$

$$N_f = \frac{Q_f}{qA} \quad (5.9)$$

where A is the capacitor area in cm^2 , ϕ_{MS} was calculated based on the doping concentration of the substrate assuming it was uniformly doped. The calculated fixed charge density was $8.3 \times 10^{10} \text{ cm}^{-2}$.

Fig. 5.14 showed that the amount of hysteresis is about 45mV for a voltage sweep from -4.0V to 2.0V , which is believed to be due to charge trapping and detrapping. The small hysteresis indicated the Ta_2O_5 - HfO_2 nanolaminates with the Si_3N_4 as the barrier layer has good film quality.

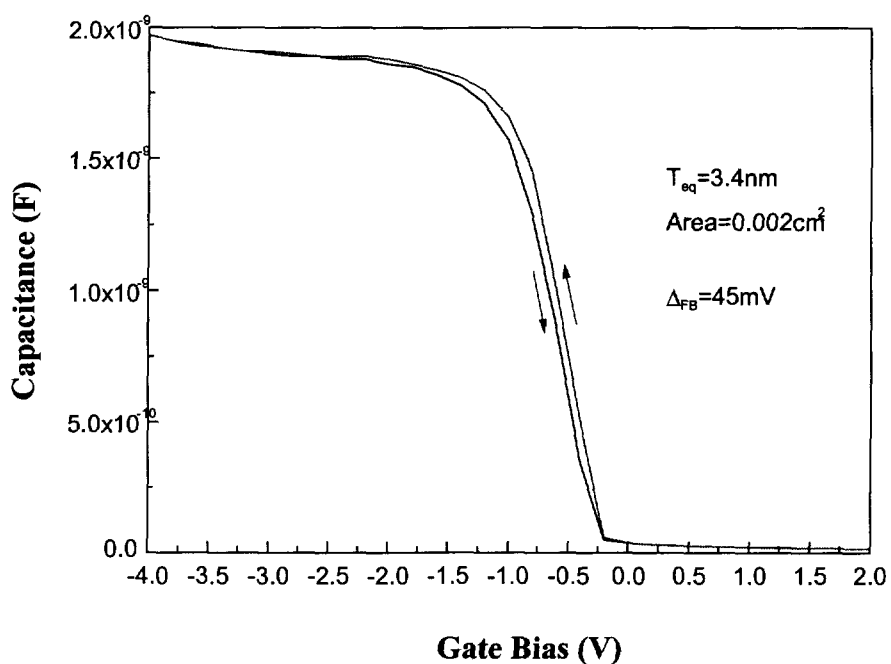


Fig. 5.14 Hysteresis characteristic of Ta_2O_5 - HfO_2 / Si_3N_4 nanolaminates, the Ta_2O_5 - HfO_2 is $5 \text{ Ta}_2\text{O}_5 + 10(8 \times \text{Ta}_2\text{O}_5 + 8 \times \text{HfO}_2)$ and Si_3N_4 is 2.12 nm.

There was no significant frequency dependence of capacitance ($<1\%$ /decade) for most process conditions as shown in Fig. 5.15. However, the capacitance measured at 20kHz was significantly higher than other higher frequencies. This frequency dependence was possibly due to the presence of fast interface state charges. All C-V measurements used to determine the dielectric constant were performed at 200 kHz, therefore the effect of interface charges could be eliminated.

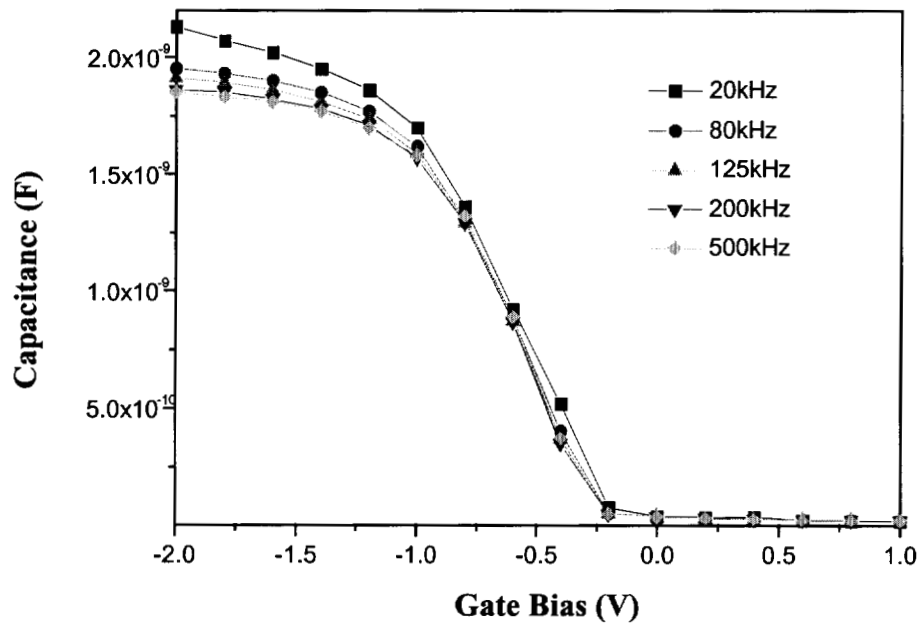


Fig. 5.15 Frequency dependency of C-V curve of Ta₂O₅-HfO₂/Si₃N₄ nanolaminates, the Ta₂O₅-HfO₂ is 5 Ta₂O₅ + 10(8×Ta₂O₅+8×HfO₂) and Si₃N₄ is 2.12 nm.

Leakage current is an issue of critical concern in gate dielectrics. Many investigations have used elaborate processes such as N₂O annealing [12], plasma O₂ annealing [13,14], and two-step annealing [15,16] to improve the leakage current levels of Ta₂O₅ capacitors. Results in this study demonstrate the leakage current of amorphous nanolaminate structure is lower than that of pure binary oxides.

In dielectric films, there are several possible mechanisms responsible for the leakage current. These mechanisms include Schottky emission, Poole-Frenkel emission, Fowler-Nordheim tunneling, direct tunneling and a space charge limited current. A detailed discussion was presented in Chapter 2. Considering our bias conditions and film thickness, Schottky and Poole-Frenkel emissions would be the dominant leakage mechanisms for these samples. The Schottky emission can be expressed as follows,

$$J \propto T^2 \exp \left[\frac{q(-\phi_B) + \sqrt{qE/4\pi k\epsilon_0}}{k_B T} \right] \quad (5.10)$$

and the Poole-Frenkel emission can be described as:

$$J \propto E \exp \left[\frac{q(-\phi_B) + \sqrt{qE/\pi k\epsilon_0}}{k_B T} \right] \quad (5.11)$$

where J represents leakage current density, T is absolute temperature, k_B is Boltzmann constant, q represents electronic charge, E is electric field, ϕ_B represents barrier height and k denotes the dielectric constant of the investigated insulator material.

The I-V characteristic of $\text{Ta}_2\text{O}_5 - \text{HfO}_2$ nanolaminate annealed at 1000°C in Ar for 10 s was displayed in Fig. 5.16. In order to determine the leakage mechanisms in the ultra-thin nanolaminates, the logarithm of the current density was plotted against the electric field. For example, in Fig. 5.17 the logarithmic current density is plotted as a function of the square root of electric field $[\ln(J) \text{ vs. } E^{1/2}]$ for $\text{Ta}_2\text{O}_5 - \text{HfO}_2$ nanolaminate stack. A straight line was obtained at low electric fields ($<0.4 \text{ MV/cm}$) implying Schottky emission [17]. At higher electric field conduction is governed by a different mechanism. In Fig. 5.18 the logarithmic current density divided by the electric field was plotted as a function of the square root of the electric field $[\ln(J/E) \text{ vs. } E^{1/2}]$. A

straight line was obtained at a high electric field (> 0.4 MV/cm), suggesting that the leakage current at high electric field is due to the Poole-Frenkel conduction mechanism [18,19].

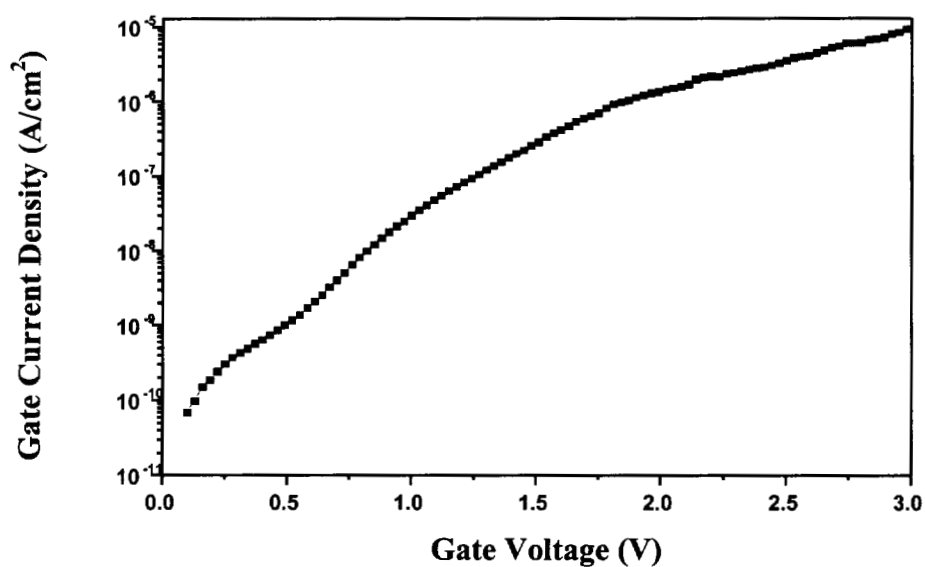


Fig. 5.16 The leakage current density vs applied voltage for the Al-Ta₂O₅/HfO₂-Si₃N₄-Si capacitor. The thickness of the nanolaminates was 7.4 nm. The area of the capacitor is 0.0028 cm².

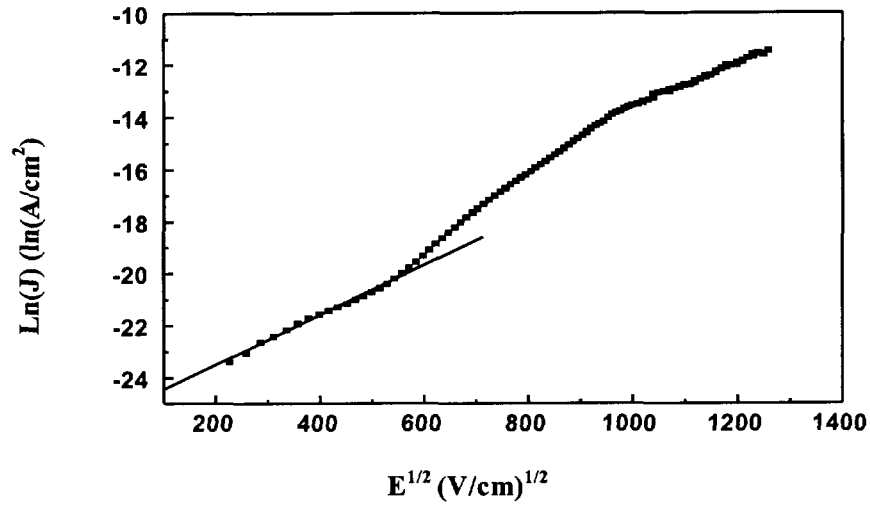


Fig. 5.17 The $\ln(J)$ vs $E^{1/2}$ is plotted for the $\text{Al-Ta}_2\text{O}_5/\text{HfO}_2\text{-Si}_3\text{N}_4\text{-Si}$ (MIS) capacitor. The straight line characteristic at low electric field (< 0.4 MV/cm) indicates Schottky emission.

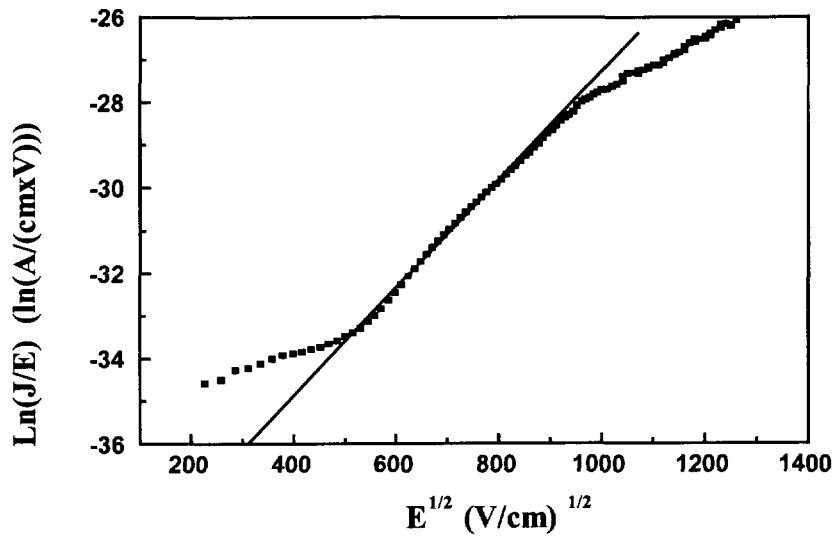


Fig. 5.18 The $\ln(J/E)$ vs $E^{1/2}$ is plotted for the $\text{Al-Ta}_2\text{O}_5/\text{HfO}_2\text{-Si}_3\text{N}_4\text{-Si}$ (MIS) capacitor. The straight-line characteristic at relative high electric field (> 0.4 MV/cm) indicates Poole-Frenkel conduction.

5.3.2 Ta₂O₅-ZrO₂ nanolaminates

Pure ZrO₂ films have showed high permittivity (21) and lower leakage current compared to pure Ta₂O₅ thin film. Therefore, ZrO₂ is a good candidate to be incorporated with Ta₂O₅ thin films. Because the refractive index of bulk ZrO₂ is comparable with that of Ta₂O₅ film, the nanolaminates have shown a fairly high refractive index of 2.1.

A series of Ta₂O₅-ZrO₂ nanolaminates were grown on bare Si and Si₃N₄ coated substrate. For nanolaminates grown on bare Si wafer, a layer of SiO₂ was expected at the Si/nanolaminates interface due to the silicon oxidation and it was confirmed by a TEM image. Ta₂O₅-ZrO₂ nanolaminates deposited on Si substrates were also analyzed by C-V and I-V measurements, as summarized in Table 5-8. For these samples, the thickness ratio of Ta₂O₅ to ZrO₂ equals to 12%: 88%. Highest permittivity was reported for Ta₂O₅-ZrO₂ nanolaminates at this ratio [20]. As seen from some TEM images, the thickness of the interfacial SiO₂ layer varies with the grown nanolaminates, which made it difficult to calculate the effective dielectric constant of the nanolaminates. Therefore the k values listed in Table 5-8 are the effective dielectric constant of the Ta₂O₅-ZrO₂ nanolaminates/SiO₂ stack. Leakage current was measured at (V_t +1) volt. T_{eq,ox} is the electrical equivalent thickness of SiO₂.

**Table 5-8 Ta₂O₅-ZrO₂ nanolaminates deposited on Si substrates.
The thickness ratio of Ta₂O₅: ZrO₂ is 12% : 88%.**

Thickness (nm)	k	T _{eq,ox} (nm)	Leakage current (A/cm ²)
82	21	15.2	8.4×10 ⁻⁹
48	16	11.7	8.4×10 ⁻⁹
37	16	9.0	4.2×10 ⁻⁹
15	11	5.3	3.4×10 ⁻⁷
10.2	10	3.9	3.7×10 ⁻⁶

To avoid the reduction of permittivity due to the Si oxidation during exposure to water vapor, another set of samples were deposited on the nitrided silicon wafer. This time our investigation was focused on thinner Ta₂O₅-ZrO₂ nanolaminates. As in the case of Ta₂O₅-HfO₂ nanolaminates, we used the same number of cycles for both Ta₂O₅ and ZrO₂ constituent layers. Rapid thermal anneal was performed on these thinner films and the dielectric properties were tabulated in Table 5-9. For the as-deposited film of 9.86 nm (including the 2.76 nm silicon nitride layer), we obtained a dielectric constant of 13 and the SiO₂ equivalent thickness is 3 nm. Once the thickness dropped below 10 nm, the decrease of the dielectric constant slowed down. The dielectric constant of 8.46 nm nanolaminates still showed a k value of 11.5. This was partially due to the existence of Si₃N₄ layer, which has a k value of 7.8. For the annealed samples, we observed the k values to vary with the annealing temperature and annealing ambient. When annealed at 700°C, k increased to 12. We believe this was due to the partial crystallization of the nanolaminates. At 800°C, k value dropped. This drop could be caused by the silicon oxidation at the Si/Si₃N₄ interface. This SiO₂ layer contributes to the reduction in dielectric constant. At higher annealing temperature such as 900°C, the crystallization and Si oxidation have competitive role in determining the dielectric constant. Fig. 5.19 showed the leakage current property of Ta₂O₅-ZrO₂ thin film nanolaminates annealed at 600 – 900°C in O₂ for 60 s. The leakage current property of nanolaminates could be improved at the expenses of the dielectric constant decrease due to the interfacial layer growth. At the same time, crystallized structure in the thin film nanolaminates would introduce higher leakage current. The sample annealed at 1000°C in Ar showed the highest dielectric constant due to the crystallization but relatively high leakage current due to the oxide-free interface.

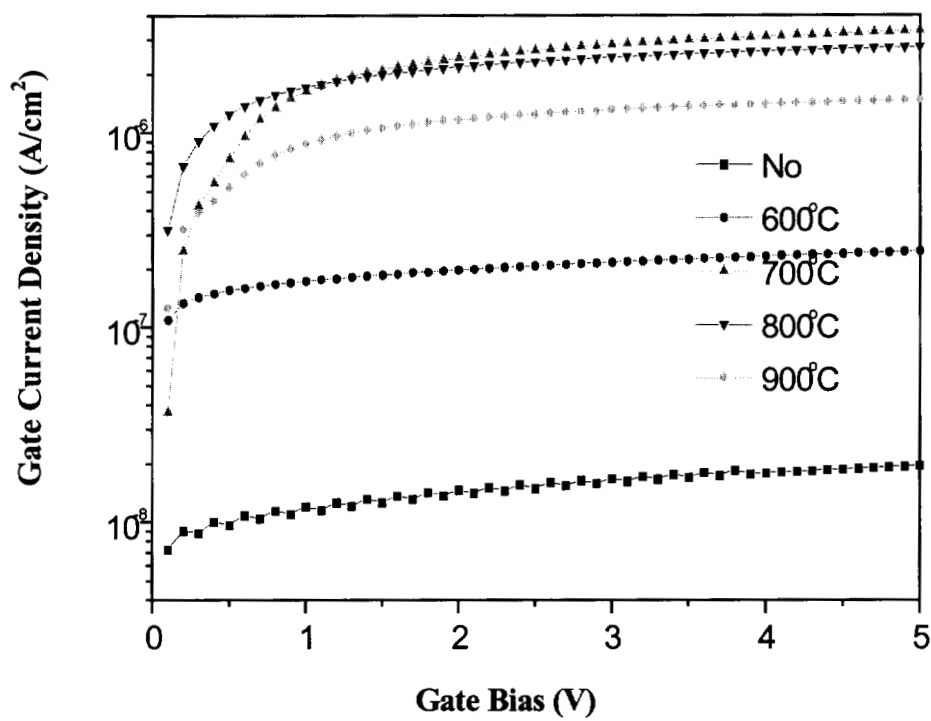


Fig. 5.19 Gate current density of as-deposited and RTA treated Ta_2O_5 - ZrO_2 nanolaminates grown on nitrated Si substrates. The thickness of the nanolaminates is about 3.7 nm and the nitride thickness is 2.76 nm.

Table 5-9 Ta₂O₅- ZrO₂ nanolaminates grown on nitrided Si substrates. The thickness of Si₃N₄ is 2.76 nm.

Film stack	RTA	Total Thickness (nm)	Dielectric constant	SiO ₂ equivalent thickness (nm)	Leakage current density (A/cm ²) at +1V.
10 Ta ₂ O ₅ + 2(20 Ta ₂ O ₅ +20 ZrO ₂)	No	9.86	13	3	3.5×10 ⁻⁸
5 Ta ₂ O ₅ + 2(8 Ta ₂ O ₅ +8 ZrO ₂)	No	5.96	8	2.9	1.2×10 ⁻⁸
5 Ta ₂ O ₅ + 2(8Ta ₂ O ₅ +8 ZrO ₂)	600°C in O ₂ for 60 s	5.96	9	2.6	1.7×10 ⁻⁷
5 Ta ₂ O ₅ + 2(8 Ta ₂ O ₅ +8 ZrO ₂)	700°C in O ₂ for 60 s	6.36	12	2.1	1.6×10 ⁻⁶
5 Ta ₂ O ₅ + 2(8 Ta ₂ O ₅ +8 ZrO ₂)	800°C in O ₂ for 60 s	6.36	9	2.8	1.7×10 ⁻⁶
5 Ta ₂ O ₅ + 2(8 Ta ₂ O ₅ +8 ZrO ₂)	900°C in O ₂ for 60 s	6.46	11	2.3	8.8×10 ⁻⁷
5 Ta ₂ O ₅ + 2(8 Ta ₂ O ₅ +8 ZrO ₂)	1000°C in Ar for 10 s	6.46	15	1.7	1.4×10 ⁻⁶

5.3.3 ZrO₂-HfO₂ nanolaminates

Besides the Ta₂O₅ based thin film nanolaminates, work has been done to combine ZrO₂ and HfO₂ thin films. We expected even lower leakage current compared to previous two thin film nanolaminates because the individual binary oxides are both less leaky than pure Ta₂O₅. Although the dielectric constant of bulk ZrO₂ is slightly lower than that of bulk Ta₂O₅, with the decrease of the film thickness, the dielectric constant was expected to drop dramatically from its bulk value. For thin film of thickness about 10 nm, the dielectric constants of both ZrO₂ and HfO₂ binary oxides are close to 10. In this study, all thin film nanolaminates were grown directly on nitrided Si substrates. X-ray diffraction pattern indicated that the ZrO₂ - HfO₂ nanolaminates crystallized at 800°C.

Again crystallization contributed to the increase of dielectric constant and the leakage current. The electrical properties of as-deposited and RTA annealed ZrO₂ - HfO₂ nanolaminates are summarized in Table 5-10. It is noticed that the leakage current variation trend with film thickness of ZrO₂ - HfO₂ nanolaminates was very similar to that of the Ta₂O₅ - ZrO₂ nanolaminates, except the leakage current of ZrO₂ - HfO₂ nanolaminates was lower than that of Ta₂O₅ - ZrO₂ nanolaminates. Again the Si oxidation at the Si/Si₃N₄ interface during annealing in oxygen would reduce the leakage current by forming a thin layer of SiO₂. Rapid thermal annealing at temperature above 800°C caused the amorphous thin film to crystallize and thus increased the dielectric constant. The I-V characteristic of these nanolaminates was shown in Fig. 5.20.

Table 5-10 ZrO₂-HfO₂ nanolaminates growth on nitrated Si substrates. The thickness of Si₃N₄ is 2.76 nm.

Film stack	RTA	Total Thickness (nm)	Dielectric constant	SiO ₂ equivalent thickness (nm)	Leakage current density (A/cm ²) at +1V
10 ZrO ₂ + 2(20 ZrO ₂ +20 HfO ₂)	No	11.6	14	3.2	2.3×10^{-8}
5 ZrO ₂ + 2(10 ZrO ₂ +10 HfO ₂)	No	8.0	12	2.5	3.6×10^{-8}
5 ZrO ₂ + 2(5 ZrO ₂ +5 HfO ₂)	No	7.6	11	2.3	7.3×10^{-8}
5 ZrO ₂ + 2(5 ZrO ₂ +5 HfO ₂)	700°C in O ₂ for 60 s	5.96	9	2.6	3.7×10^{-7}
5 ZrO ₂ + 2(5 ZrO ₂ +5 HfO ₂)	800°C in O ₂ for 60 s	5.96	12	1.8	2.8×10^{-7}
5 ZrO ₂ + 2(5 ZrO ₂ +5 HfO ₂)	900°C in O ₂ for 60 s	6.16	10	2.2	2.9×10^{-7}
5 ZrO ₂ + 2(5 ZrO ₂ +5 HfO ₂)	1000°C in Ar for 10 s	6.16	9	1.7	2.4×10^{-7}

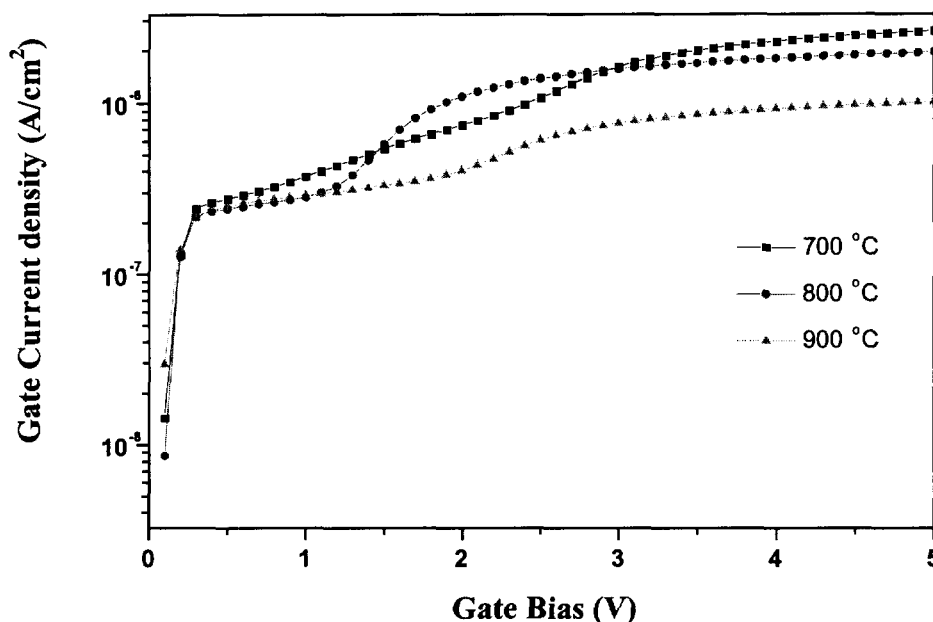


Fig. 5.20 Gate current density of as-deposited and O₂ RTA treated ZrO₂- HfO₂ nanolaminates grown on nitrated Si substrates. The thickness of the nanolaminates is about 3.4 nm and the nitride thickness is 2.76 nm.

5.4. Electrical properties of SiON and High k films

It is well known that as the thickness approaches 2~3 nm, SiO₂ would suffer from very large leakage current. Silicon oxynitride (SiON) films are more resistant to current leakage compared to SiO₂. We obtained a SiON thin film of 3.2 nm deposited on Si and measured the current –voltage characteristic. Fig. 5.21 indicated that the leakage current of SiON thin film was three orders higher than that of the high k nanolaminates with lower equivalent SiO₂ thickness when the gate bias is larger than +1 V. Among the three kinds of nanolaminates we investigated, ZrO₂ - HfO₂ nanolaminates showed the lowest leakage current, which was not surprising because each constituent binary oxide is less leaky than Ta₂O₅. For the same thickness Ta₂O₅ - HfO₂ and Ta₂O₅ - ZrO₂ nanolaminates,

the former was more leakage resistant. This was consistent with HfO_2 being less leaky than ZrO_2 .

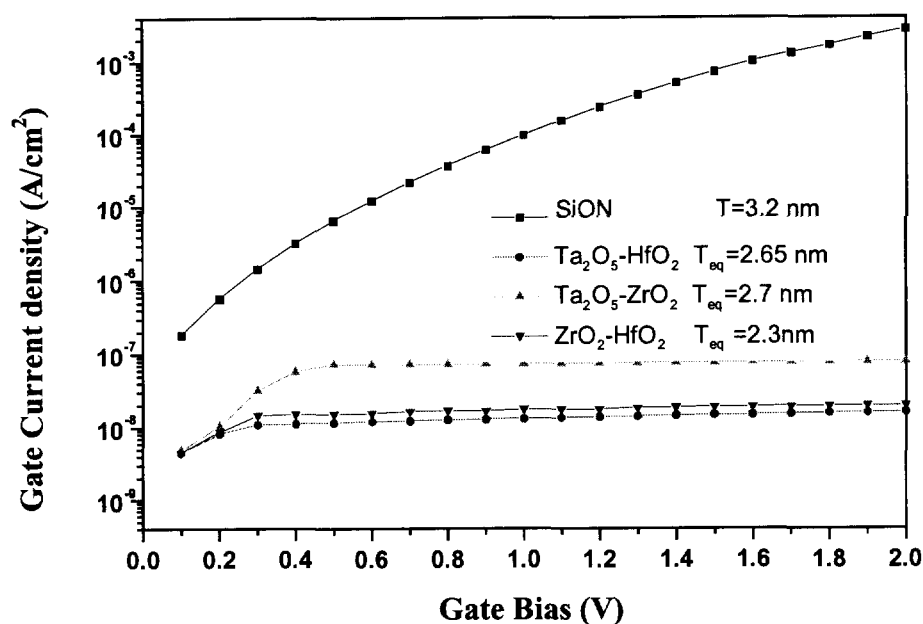


Fig. 5.21 Gate leakage current of SiON, Ta₂O₅ - HfO₂ nanolaminates/Si₃N₄, Ta₂O₅ - ZrO₂ nanolaminates/Si₃N₄, and ZrO₂ - HfO₂ nanolaminates/Si₃N₄. The thickness of Si₃N₄ is 2.76 nm for all three nanolaminates.

Fig. 5.22 shows the breakdown characteristics of as-deposited thin films of Ta₂O₅, HfO₂ and ZrO₂ on Si substrate pre-coated with 2.1 nm Si₃N₄ at room temperature. The thickness of all three films is about 8 nm. Negative biases were used in order to keep the capacitors in accumulation region and therefore minimize the voltage drop in the substrate. The current is seen to increase slowly with bias until an abrupt irreversible breakdown occurs at applied field of about 11.5 MV/cm. This may be due to the existence of the Si₃N₄ layer that has been reported to have high dielectric strength.

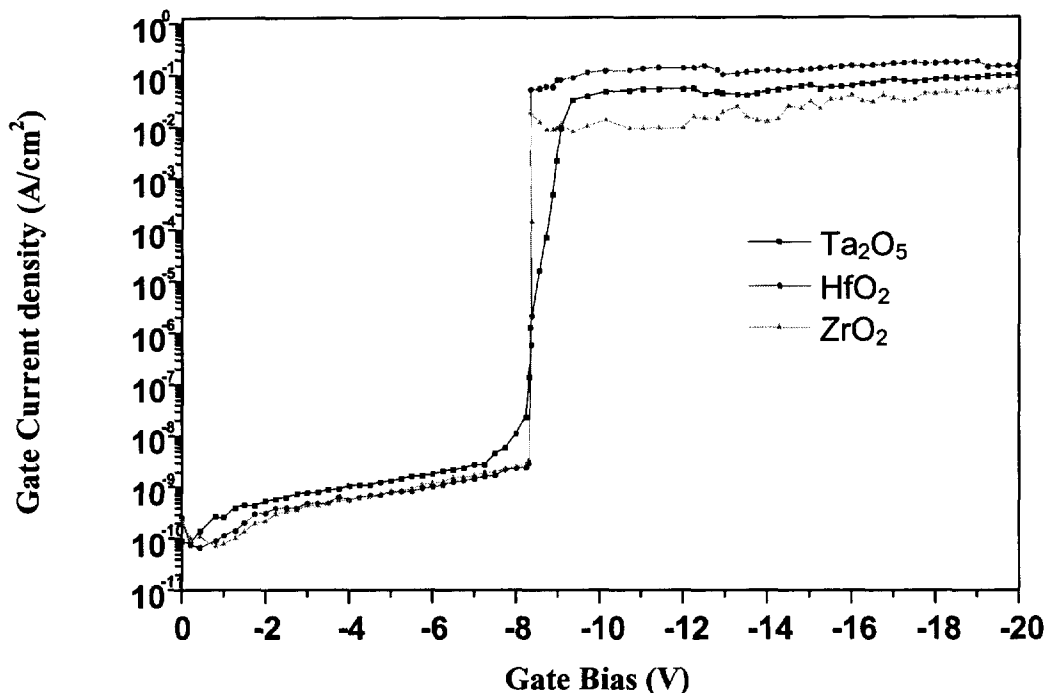


Fig. 5.22 Ramped I-V characteristic of MIS capacitors with binary high k films driven to breakdown in the accumulation mode. All films are of 8 nm thick.

A similar study on the I-V properties was performed on nanolaminates of Ta₂O₅ - HfO₂, Ta₂O₅ - ZrO₂ and ZrO₂ - HfO₂ on 2.1 nm Si₃N₄. It is surprising to see that the ZrO₂ - HfO₂ has extremely high dielectric strength compared to the other two nanolaminates and constituent binary oxides, as illustrated in Fig. 5.23. Before irreversible breakdown occurs, the leakage current for all three nanolaminates was less than 5×10^{-7} A/cm². The dielectric strengths of Ta₂O₅ - HfO₂ nanolaminates and Ta₂O₅ - ZrO₂ were 9.6 MV/cm and 9 MV/cm, respectively. However, the breakdown field for the ZrO₂ - HfO₂ was as high as 25 MV/cm.

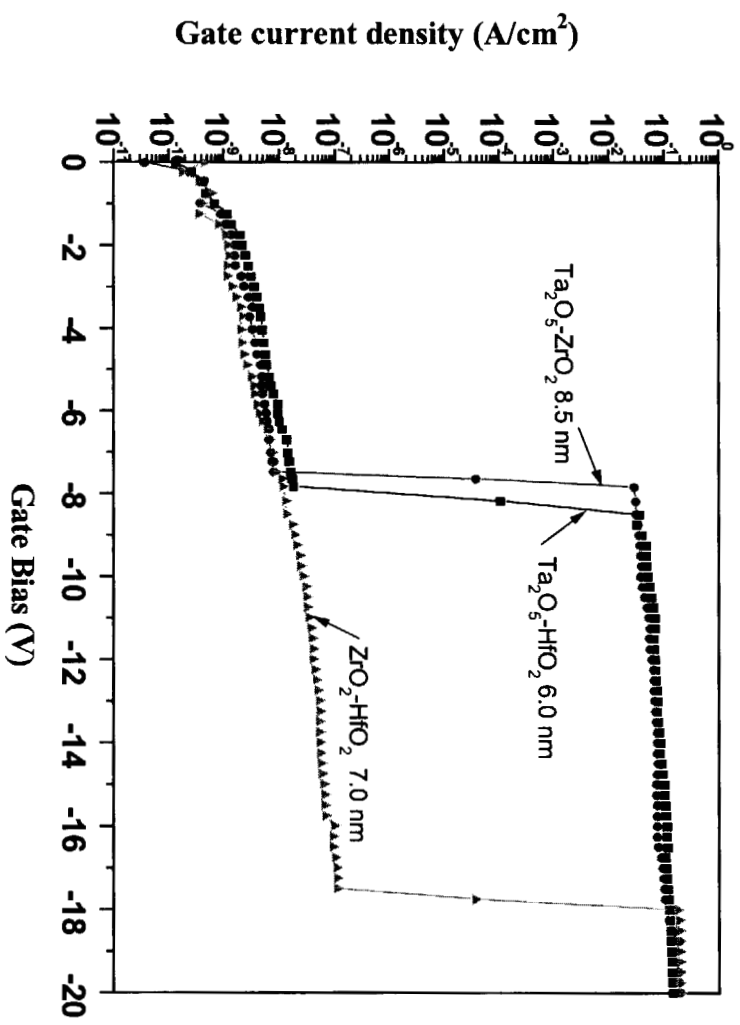


Fig. 5.23 I-V characteristics of MIS capacitors of Ta_2O_5 - HfO_2 , Ta_2O_5 - ZrO_2 and ZrO_2 - HfO_2 nanolaminates in the accumulation region.

In this chapter, material and electrical properties of binary oxides Ta_2O_5 , HfO_2 , ZrO_2 and their nanolaminates were investigated. Surface roughness of silicon nitride coated substrate and as-grown films with different thickness was studied using AFM. TEM indicated that a thin layer of SiO_2 formed when high k films were deposited directly on Si substrate, and C-V measurement showed that this layer would reduce the effective dielectric constant of the high k film/ SiO_2 stack. Al and Si_3N_4 were deposited as barrier layer of the Si oxidation separately. It was shown that the nitride was a better passivation film as to prevent Si surface oxidation by water vapor. C-V method had been used to calculate the dielectric constant, extract flatband voltage and characterize the interface charges. The leakage mechanisms of Ta_2O_5 - HfO_2 nanolaminates were examined based on I-V measurement. Dielectric breakdown of these high k films and their nanolaminates were studied as well. As we shrink the thickness of these high k materials, the extracted dielectric constant would reduce which set a limitation on application of these materials. However, they are still promising candidates for replacing SiO_2 as the future gate dielectric materials.

References

- [1] D. K. Schroder, *Semiconductor Material and Device Characterization*, John Wiley & Sons, 1990, p. 46.
- [2] C. Goodman and M. Pessa, "Atomic Layer epitaxy," *J. Appl. Phys.* **60**, 1986, R65-R81.
- [3] M. Oikkonen, M. Blomberg, T. Tuomi, and M. Tammenmaa, "X-ray diffraction study of microstructure in ZnS thin films grown from zinc acetate by atomic layer epitaxy," *Thin Solid Films* **124**, 1985, pp. 317-321.
- [4] H. Kimura, J. Mizuki, S. Kamiyama, and H. Suzuki, "Extended absorption fine line structure analysis of the difference in local structure of tantalum oxide capacitor films produced by various annealing method," *Appl. Phys. Lett.* **66**, 1995, pp. 2209-2211.
- [5] L. K. Han, G. W. Yoon, D. L. Kwong, V. K. Mathews, and P.C. Fazan, "Effects of post-deposition annealing on the electrical properties and reliability of ultrathin chemical vapor deposited Ta₂O₅ films," *IEEE Electron Device Letters*, **15**, 1994, pp. 280-282.
- [6] G. B. Alers, R.M. Fleming, Y.H. Wong, B. Dennis, A. Pinczuk, G. Redinbo, R. Urdahl, E. Ong, and Z. Hasan, "Nitrogen plasma annealing for low temperature Ta₂O₅ films," *Appl. Phys. Lett.* **72**, 1998, pp. 1308-1310.
- [7] T. Hori, *Gate Dielectrics and MOS ULSIs*, Springer, 1997, p. 42.
- [8] K. Natori, D. Otami, and N. Sano, "Thickness dependence of the effective dielectric constant in a thin film capacitor," *Appl. Phys. Lett.* **73**, 1998, pp. 632-634.
- [9] M. Balog, M. Schieber, M. Michman, and S. Patai, "The chemical vapor deposition and characterization of ZrO₂ films from organometallic compounds," *Thin Solid Films* **41**, 1977, pp. 247-250.
- [10] B. Kralik, E. K. Chang, and S. G. Louie, "Structural properties and quasiparticle band structure of ziconia," *Physical Review B* **57**, 1998, pp. 7027-7032.
- [11] R. J. Hillard, J. M. Heddleson, D. A. Zier, P. Rai-Choudhury, and D. K. Schroder "Direct and rapid method for determining flatband voltage from non-equilibrium capacitance voltage data" in *Diagnostic Techniques for Semiconductor Materials and Devices* (J. L. Benton, G. N. Maracas, and P. Rai-Choudhury, eds). Electrochem. Soc., Pennington, NJ, 1992, pp. 261-274.

- [12] S. C. Sun and T. F. Chen, "A novel approach for leakage current reduction of LPCVD Ta₂O₅ and TiO₂ films by rapid thermal N₂O annealing," IEEE IEDM, San Francisco, CA, Dec. 11-14, 1994, pp. 333-336.
- [13] S. Kamiyama, H. Suzuki, H. Watanabe, A. Sakai, M. Oshida, T. Tatsumi, T. Tanigawa, N. Kasai, and A. Ishitani, "A comparative study of hot-carrier induced light emission and degradation in bulk and SOI MOSFETs," IEEE IEDM, Washington, DC, Dec. 10-13, 1995, pp. 49-52.
- [14] S. Kamiyama, H. Suzuki, H. Watanabe, A. Sakai, H. Kimura, and J. Mizuki, "Ultrathin tantalum oxide capacitor process using oxygen-plasma annealing," J. Electrochem. Soc. **141**, 1994, pp. 1246-1251.
- [15] H. Shinriki and M. Nakata, "UV-O₃ and Dry-O₂: Two-step annealed chemical-vapor-deposited Ta₂O₅ films for storage dielectrics of 64-Mb DRAM's," IEEE Trans. Electron Devices **38**, 1991, pp. 445-464.
- [16] H. Shinriki, M. Nakata, Y. Nishioka, and K. Mukai, "Two-step annealing technique for leakage current reduction in chemical-vapor-deposited Ta₂O₅ film," IEEE Electron Devices Letters **10**, 1989, pp. 514-516.
- [17] H. Matsushashi and S. Nishikawa, "Optimum electrode materials for Ta₂O₅ capacitors for high- and low- temperature processes," Jpn. J. Appl. Phys. **133**, 1994, pp. 1293-1297.
- [18] C. Isobe and M. Saitoh, "Effect of ozone annealing on the dielectric properties of tantalum oxide thin films grown by chemical vapor deposition," Appl. Phys. Lett. **56**, 1990, pp. 907-909.
- [19] F. Chiu, J. Wang, J. Lee, and S. Wu, "Leakage currents in amorphous Ta₂O₅ thin films," J. Appl. Phys. **81**, 1997, pp. 6911-6915.
- [20] K. Kukli, J. Ihanus, M. Ritala, and M. Leskela, "Properties of Ta₂O₅-based dielectric nanolaminates deposited by atomic layer epitaxy," J. Electrochem. Soc. **144**, 1997, pp. 300-306.

Chapter 6

Summary and Conclusions

Thin films of binary oxides Ta_2O_5 , HfO_2 and ZrO_2 and their nanolaminates $\text{Ta}_2\text{O}_5\text{-HfO}_2$, $\text{Ta}_2\text{O}_5\text{-ZrO}_2$ and $\text{ZrO}_2\text{-HfO}_2$ were grown on Si substrates by atomic layer epitaxy. The F-120 ALE reactor used in this study is a research level reactor that can handle 2" \times 2" substrates. Process parameters, such as source material temperatures, substrate temperature, reactant gas flow rate, reactants pulse time and purging duration have to be optimized to get uniform deposition.

During the growth of Ta_2O_5 , it was found that the best film uniformity was achieved at 300 °C and the film was identified as amorphous by X-ray diffraction pattern. Rapid thermal anneal (RTA) above 800°C introduced crystallization. However, film thickness did not change before and after RTA, which indicated the as-deposited film was already fairly dense when the growth temperature is higher than 200 °C. Spectroscopic ellipsometry confirmed the densities of as deposited and annealed films were the same. Secondary ion mass spectroscopy characterization indicated the Ta_2O_5 film to be stoichiometric, with the concentration of chloride below the detection limit. Atomic force microscopy revealed that thicker film had a rougher surface. For Ta_2O_5 film deposited directly on bare Si (with the native oxide being removed), a thin layer of SiO_2 was

identified by Transmission Electron Microscope (TEM). This layer was formed during the Ta_2O_5 film growth as the water vapor was used as oxygen source.

For HfO_2 film, a more complicated surface reaction was observed. The uniformity of HfO_2 was very poor and island growth existed in most cases. This film showed better adhesion to Si_3N_4 coated substrate. Si_3N_4 was also served as a barrier layer against Si oxidation. The as-deposited film was either amorphous or partially crystallized with very weak peak intensity. A preferred orientation in the (1,1,1) plane with very high intensity was detected by XRD after annealing at 800°C .

ZrO_2 growth requires longer pulse and purge time to realize the self-controlled process compared to the previous two oxides. It is found that ZrCl_4 pulse was critical with respect to the thickness saturation, while short water pulse had no effect on the film thickness. Water purge time was essential to improve the film uniformity. ALE growth at 300°C produced nearly amorphous film and it crystallized upon 700°C RTA.

No process parameters needed to be optimized in the growth of nanolaminates due to the characteristics of ALE technique. We incorporated two binary oxides into a nanolaminate structure and the thickness was determined by the number of cycles of each constituent oxide layers. Since we focused on very thin nanolaminates (less than 10 nm), the dependence of dielectric properties on thickness ratio of two constituent oxides were not studied when we were already approaching the lower limit of allowable number of cycles.

For Ta_2O_5 - HfO_2 , aluminum evaporated on Si as the water barrier layer was studied. A more complicated interface layer consisting of $\text{Al}_2\text{O}_3/\text{SiO}_2$ after deposition of high k films was showed by TEM image, which indicated Al was not an effective coating for preventing Si surface oxidation. When Si_3N_4 coated substrates were used, several techniques, such as SIMS, FT-IR spectrum and X-ray reflectivity analysis were used to determine that no SiO_2 formed underneath the nitride layer after the high k films were deposited.

Dielectric properties of binary oxides and nanolaminates were characterized by various techniques, including C-V measurement, I-V measurement and ellipsometry. The relative dielectric constant (k) was calculated from C-V curve. The C-V measurements on the films from same process but with different thicknesses showed a decreased dielectric constant versus the k value of bulk material as the film thickness was reduced. A significant drop of k value was observed for films less than 10 nm thick. This reduction in k has been shown to depend on the number of atomic monolayers and the atomic polarizability of the film. In other words, there were fewer dipole moments between two surfaces, the polarizability of the ultra thin film can be dramatically affected by its interfaces as opposed to the diminishing bulk properties.

Rapid thermal annealing (RTA) was performed in different ambients, including argon (Ar) and oxygen (O_2). It showed a positive effect on the dielectric constant due to the crystallization of the film. However, annealing in Ar increased the leakage current because the crystallization facilitated the leakage path through the grain boundaries. The reduction of gate current in O_2 RTA could be due to the formation of thin SiO_2 layer. This very thin SiO_2 layer had little effect on k for high k film of 16 nm thick. However, a negative effect on k was expected for thinner film with this very thin SiO_2 layer although no experiments were performed. We have to compensate between the increased k value and increased leakage current after RTA process.

Among the three binary oxides, HfO_2 showed the lowest leakage current while Ta_2O_5 was the most leaky film due to the small bandgap. Therefore ZrO_2 - HfO_2 demonstrated the best leakage resistant characteristic among the three nanolaminates while all three nanolaminates showed lower leakage compared to SiO_2 of same thickness. The leakage mechanism was studied on Ta_2O_5 - HfO_2 nanolaminates. It revealed that Schottky emission was responsible for the leakage at low electric field and Poole-Frenkel conduction dominated at high field. The dielectric strength of Ta_2O_5 , HfO_2 and ZrO_2 was very close with the breakdown occurred at applied field of about 11.5 MV/cm. It was surprising that the dielectric strength of ZrO_2 - HfO_2 was much higher than that of the

Ta₂O₅-HfO₂ and Ta₂O₅-ZrO₂, showing 25MV/cm versus 9.6 MV/cm and 9 MV/cm respectively.

The charges at the Si interface were studied based on C-V measurements. The flatband voltage of Ta₂O₅ - HfO₂ nanolaminates grown on Si₃N₄ was determined to be -1.1V and the calculated fixed charge density was about $8.3 \times 10^{10} \text{ cm}^{-2}$. There were methods discussed in chapter 2 that can be used to measure interface charge density, it either requires a MOSFET device or some theoretical data that involves very complicated calculation. Therefore, no interface charge density results were reported.

Several issues remain to be solved in the future for this study. Using water as the oxygen source will cause the Si surface oxidation if no barrier layer was used. There are possible alternatives to resolve this problem such as using N₂O or NO to replace current DI water. At least the oxidation rate should be much lower than using water and the thickness of silicon oxide layer (if it exists) can be dramatically reduced, therefore relieve the negative effect on dielectric constant.

It is always desired to fabricate MOSFET devices using the high k films investigated. Transistors using Ta₂O₅ and ZrO₂ have been recently reported, however transistors made with the nanolaminates have not been studied yet. Special attention should go to the HfO₂ since it had been reported as etch-stop material. To make the studied films applicable in manufacturing, reactive ions etching with proper etch rate and selectivity to silicon would be critical. For MOSFET applications the dielectric films must be etched down to source and drain which have shallow junctions. It is essential to control the etch process in order to protect the junction area.

Gate-electrode material is closely related to the dielectric reliability and gate leakage. There are many other choices, such as polysilicon, TiN, Pt or other metal stacks, that may improve the dielectric properties. The deposition of gate material is very important in respect of the ultra thin dielectric film. The interface between gate and dielectric needs to be studied as well.

A theoretical study on the dependence of dielectric constant on film thickness is critical for high k materials. There are many contrary results in literature. It is puzzling that dielectric constant of bulk material has been reported for ultra thin film by some researchers. An in-depth investigation including experiments and simulations would be necessary to resolve the issue.

The charges inside the nanolaminates would be of interest since there are many interfaces within the dielectric material. The effect of these charges on the leakage and reliability should be examined.

Finally, with the shrinkage of feature size, deposition and characterization of high dielectric constant material will continue to be one of the most interesting research topics in the future.

Vita

The author, Hui Zhang, was born in Ying Kou, Liao Ning, China, in January, 1972. She enrolled in Central South University of Technology in 1990 and received a B.E. in Material Science and Engineering in 1994. After working for Hunan Research Institute of Material and Metallurgy in Changsha, Hunan for one year, she enrolled in the Department of Material Science and Engineering at Oregon Graduate Institute of Science and Technology in 1995 and received her M.S. in Material Science in 1997. At the same year, she entered the Department of Electrical Engineering at Oregon Graduate Institute and obtained her M.S. and Ph.D. in Electrical Engineering in 1998 and 2000, respectively. She has authored several scientific publications during the years at OGI. She married Jianxiong Zhao in 1995.