THIN FILM TRANSISTORS IN POLYSILICON

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To My Parents

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ABSTRACT

THIN FILM TRANSISTORS IN POLYSILICON

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The n- and p-channel field effect transistors have been fabricated in as-deposited and grain boundary passivated polysilicon thin films. The performance of the thin film transistors (TFT's) is characterized and compared for different process conditions. The major cause for the degradation of subthreshold behavior and for the anomalous leakage current in these devices is the presence of the deep level trap sites in grain boundaries.

The *I-V* characteristics are modeled in correlation with the polysilicon material properties, from a unified point of view. A concept of "effective doping" resulting from trapped carriers in grain boundaries is introduced to describe the electrostatics involved therein. The theoretically predicted results are compared with the experimental data and are shown to be in satisfactory agreement. The limitations of the theory are also discussed.

CHAPTER 1

INTRODUCTION

It may be a surprise to most of us that the thin film transistor (TFT) was the first solid-state amplifier ever patented. Surely enough the first US TFT patent was issued to Lilienfeld[1] in 1933, and another was granted to Heil [2] (in Germany) in 1934, which was 13 years before the birth-date of the point contact junction transistor. Lilienfeld's devices would not have worked, judging from the benefit of hindsight. But judging from Heil's very competent description, he had all the right ideas and may actually have made the first transistor if he had tried a proper material (such as tellurium on his list). In the early 1960's, many industrial laboratories were engaged in active research on both MOSFET's and TFT's, with the bulk of effort going to the MOS. Those also working on TFT's at the time were GE, RCA, IBM, Raytheon, Zenith, Hughes and Westinghouse in U.S., and Philips in The Netherlands. The TFT's did not develop rapidly because of the poor reproducibility and unstable device performance resulting from poorly characterized polycrystalline II-VI compound films and evaporated insulators. In the mid-1960's MOSFET's were chosen for integrated circuits. Consequently, most industrial laboratories

dropped out of research on TFT's and only few have continued the effort.

The thin film transistors have recently attracted considerable attention in many areas of modern electronics. With process parameter optimization, small-grain TFT's yield good gate voltage swings and high ON/OFF current ratios[3-5], allowing them to be used in a wide variety of potential applications, such as high-density SRAM's and DRAM's, three-dimensional integrated circuits, and switching elements in large-area panel displays. This latter area is an exciting high-technology entry into the race for a share of the lucrative modern display market.

Traditionally efforts were directed towards making TFT's in II-VI materials. However, stoichiometry problems are difficult to control in II-VI compounds, such as CdSe for n-channel transistors and tellurium for p-channel transistors, and the poor gate insulator for those materials induces high surface state densities and reduces the device performance. Among all the materials which have been tested for thin film transistor fabrication, polysilicon is the most attractive candidate. The mature silicon-based planar processing techniques and a high quality thermally grown oxide yield high performance thin film transistors. The new passivation techniques, such as H^+-implantation, greatly improve the carrier mobilities and performance uniformity over large areas.

On the other hand, because of the presence of grain boundary trap sites in polycrystalline materials, the TFT's performance is not as good as that of

bulk devices. The physical parameters influencing device operation are currently under active investigation.

This thesis is devoted to the fabrication, characterization and modeling of TFT's. The discussion is divided into six chapters. Chapter 2 presents the physics and electrical properties of polycrystalline silicon that are related to the device performance, including the experimental conduction data and theoretical analysis and discussions. The fabrication of n- and p-channel thin film transistors studied in this work is graphically described in Chapter 3. The devices chosen for study are fabricated in both as-deposited and H^+-implanted polysilicon thin films in order to examine the effects of grain boundary passivation. In Chapter 4, device characterization data are presented. The leakage behavior, subthreshold and drive currents are measured and discussed. The I-V characteristics is modeled in Chapter 5. The unified model presented herein is capable of describing the device operation in both n- and p-channel TFT's. A concept of "effective doping" is introduced in this model to simplify the electro-statics in the channel. Chapter 6 is the summary of the work.

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CHAPTER 2

ELECTRICAL PROPERTIES OF POLYSILICON THIN FILMS

2.1 Introduction

The physics of TFT's discussed in this work is naturally dependent on the physical and electronic properties of the polycrystalline silicon thin film materials which are presented in this chapter. The discussion will be confined to only those properties pertinent to the device operations.

Polycrystalline silicon is composed of single crystalline grains of different crystallographic orientations separated from each other by a thin grain boundary. These boundaries, in turn, consist of layers of disordered atoms and provide a different conduction medium. The disordered structure in grain boundaries gives rise to a high density of interface states which play an important role in determining the electrical properties of polysilicon. The interface states trap carriers from the ionized dopant atoms. This decreases the mobile carrier density in grains and results in the creation of a grain boundary barrier potential. The potential barrier impedes the motion of majority carriers from one grain to the other, resulting in a decrease in carrier mobilities. Indeed, the

transport properties of polysilicon are found to be markedly different from that of single crystal silicon.

Seto [1] proposed the first comprehensive theory of carrier transport in polysilicon based on the trapping model. He assumed that the trap states are monoenergetic and are located below the intrinsic level in p-type polysilicon. The carrier transport across the grain boundary potential barrier was taken to be dominated by the thermionic emission process. He showed for the first time that there is a minimum mobility as a function of doping concentration in small grain polysilicon. This minimum value occurs near the doping concentration for which (i) the grain boundary barrier height is maximum, (ii) the grains are just depleted completely and (iii) the grain boundary trap sites are filled.

Later on many scientists extended and modified Seto's theory, which included the work of Baccarani[2], Kumar and Satyam[3], Martinez and Piqueras[4], Saraswat and Kamins[5], and Lu *et al.* [6,7] All of these are based on thermionic and field emission theory.

Considering the polycrystalline materials as consisting of crystalline grains and amorphous-like grain boundaries, Kim *et al* [8] have derived a conduction formulation which is based on a combination of drift and diffusion carrier transport. They modeled the grain boundary as an amorphous conductor connected in series with a crystalline grain. Specifically, in this model carriers were taken to be transported mainly via Brownian diffusive motion. The

theory was capable of quantifying Seto's and Lu *et al.*'s experimental data.

A continuous distribution of trap sites in the band gap was introduced in number of polysilicon conduction models[4]. This distribution results in a complicated mathematical formulation in describing the I-V behavior of polysilicon. The electrical conduction mechanism in polycrystalline materials is still under investigation and the understanding is not complete. The present work uses the monoenergetic trap level model, for simplicity.

2.2 Grain Boundary Barrier Potential

The presence of grain boundaries which trap mobile carriers from grains creates a barrier potential near grain boundaries. A quantitative evaluation of this potential (V_B) can be carried out, based on the charge neutrality condition and the depletion approximation. An electron/hole trap site is neutral when it is free of charge and negative/positive with a trapped electron/hole. The trapped charge density per unit area in the boundary is given by

$$N_t = \frac{N_T^p}{1 + 2e^{(E_F - qV_B - E_T^p)/k_B T}} - \frac{N_T^n}{1 + 2e^{(E_T^n - E_F - qV_B)/k_B T}} \tag{2.1}$$

where N_T^n/N_T^p is the number of trap sites of electrons/holes per unit area in grain boundaries, E_F the Fermi level and E_T^n/E_T^p the trap level for electrons/holes.

Consider a unit element of polysilicon in a p-type sample. In the one

dimensional depletion model the depletion depth is

$$W = \frac{N_t}{2 \cdot N_A} \tag{2.2}$$

with N_A denoting doping concentration. The charge distribution in the unit element of polysilicon consisting of a grain and a grain boundary, is shown in Figure 2-1. The associated Poisson equation reads as

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_s} \tag{2.3}$$

with

$$\rho(x) = \begin{cases} -qN_A & (-W < x < W) \\ 0 & (x < -W,\ x > W). \end{cases} \tag{2.4}$$

The equation can be solved with the boundary conditions that both potential and space charge field is zero at the edge of depletion depth, viz.

$$\phi(W) = \phi(-W) = 0 \tag{2.5}$$

and

$$\frac{d\phi(W)}{dx} = \frac{d\phi(-W)}{dx} = 0\ . \tag{2.6}$$

The solution is given by

$$E(x) = \begin{cases} -\dfrac{qN_A}{\epsilon_s}(x - W) & (0 < x < W) \\ -\dfrac{qN_A}{\epsilon_s}(x + W) & (-W < x < 0), \end{cases} \tag{2.7}$$

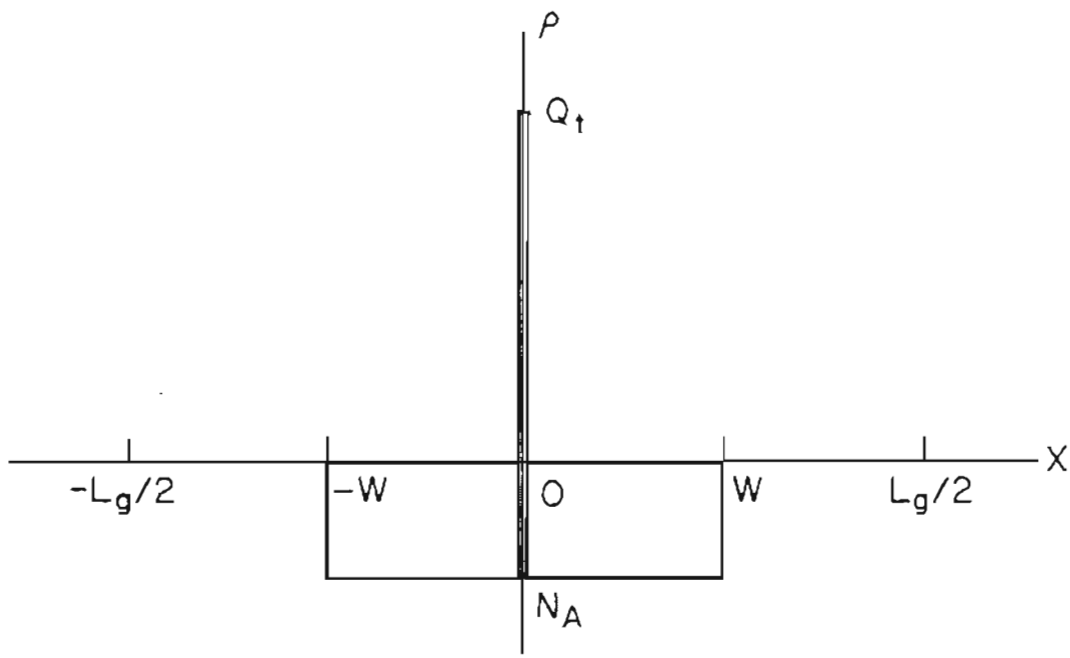

Figure 2-1 Charge distribution in a unit element of p-type polycrystalline silicon with a grain size L_g, assuming doping concentration N_A is lower than N^* and the depletion model. W is the depletion depth.

and

$$\phi(x) = \begin{cases} \dfrac{qN_A}{2\epsilon_s}(x-W)^2 & (0<x<W), \\ \dfrac{qN_A}{2\epsilon_s}(x+W)^2 & (-W<x<0), \end{cases} \tag{2.8}$$

and is illustrated in Figures 2-2 and 2-3, respectively. The height of the potential barrier V_B is obtained at $x = 0$ as

$$V_B = \frac{qN_A W^2}{2\epsilon_s} = \frac{qN_t^2}{8\epsilon_s N_A} . \tag{2.9}$$

For a low or moderately doped sample at equilibrium, the average hole and electron concentrations in grains are given respectively by

$$\bar{p} = n_i e^{(E_i - E_F)/k_B T} \left[\frac{L_g - 2W}{L_g} + \frac{2}{L_g} \int_0^W e^{-q\phi(x)/k_B T} dx \right] \tag{2.10a}$$

$$\bar{n} = n_i e^{(E_F - E_i)/k_B T} \left[\frac{L_g - 2W}{L_g} + \frac{2}{L_g} \int_0^W e^{q\phi(x)/k_B T} dx \right] \tag{2.10b}$$

Therefore, the charge neutrality condition in a grain and its boundary becomes

$$\bar{p} + N_t/L_g = \bar{n} + N_A \tag{2.11}$$

with N_t, $\bar{p}$ and $\bar{n}$ given by (2.1) and (2.10).

The values of N_t, E_F, V_B and W are obtained by solving (2.1), (2.2), (2.9) and (2.11) simultaneously with a given set of parameters of E_T, N_A and

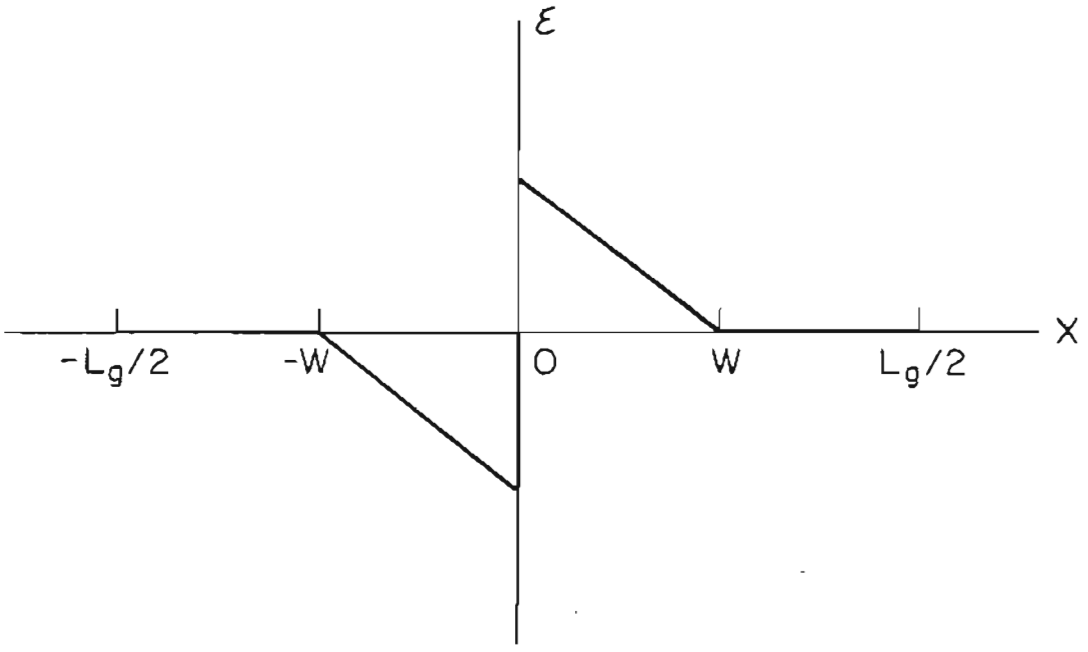

Figure 2-2 Electric field in the unit element, resulting from the space-charge in the depletion region.

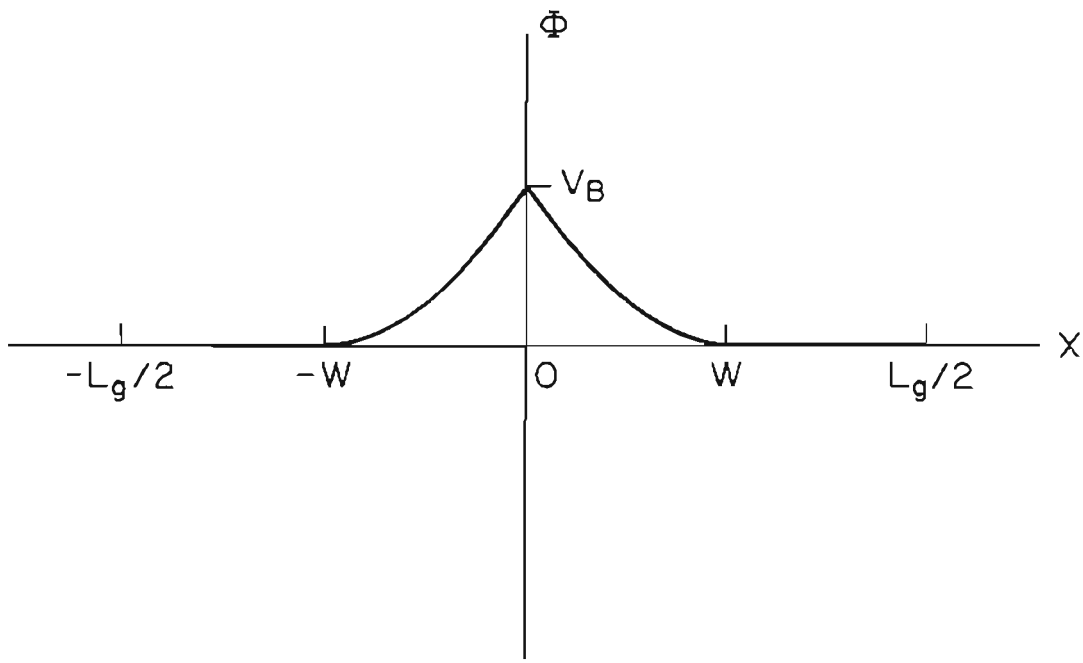

Figure 2-3 Corresponding potential distribution. The maximum of this potential (V_B) is located near the grain boundary and is given by (2.8).

L_g. A typical plot of the barrier potential as a function of doping concentration is shown in Figure 2-4 for different grain sizes and trap levels. The peak of the V_B-value is located near the critical doping concentration (N^*) which is approximately given by

$$N^* \approx N_T/L_g. \tag{2.12}$$

The maximum value of V_B is reduced as the trap level E_T moves away from the mid-gap. This is a direct consequence of Fermi statistics. The barrier potential is significant for the doping concentration near N^*. The existence of V_B results in two conditions i.e. (i) the depleted space-charge, N_A and (ii) the depletion depth, W. With a simpler model proposed by Seto[1], the barrier potential is estimated by

$$V_B = \begin{cases} \dfrac{qN_A L_g^2}{2\epsilon_s} & (N_A < N^*) \\ \dfrac{qN_T^2}{8\epsilon_s N_A} & (N_A > N^*) \end{cases} \tag{2.13}$$

The maximum value of V_B in this model is over-estimated for doping concentration close to N^*. But, (2.13) is a good approximation for $N_A << N^*$ and $N_A >> N^*$ and is independent of trap level E_T.

Figure 2-5 shows the Fermi level as a function of p-type doping concentration. The Fermi level lies near the mid-gap for low doping concentrations and rapidly moves away as doping increasing near N^*, and finally approaches

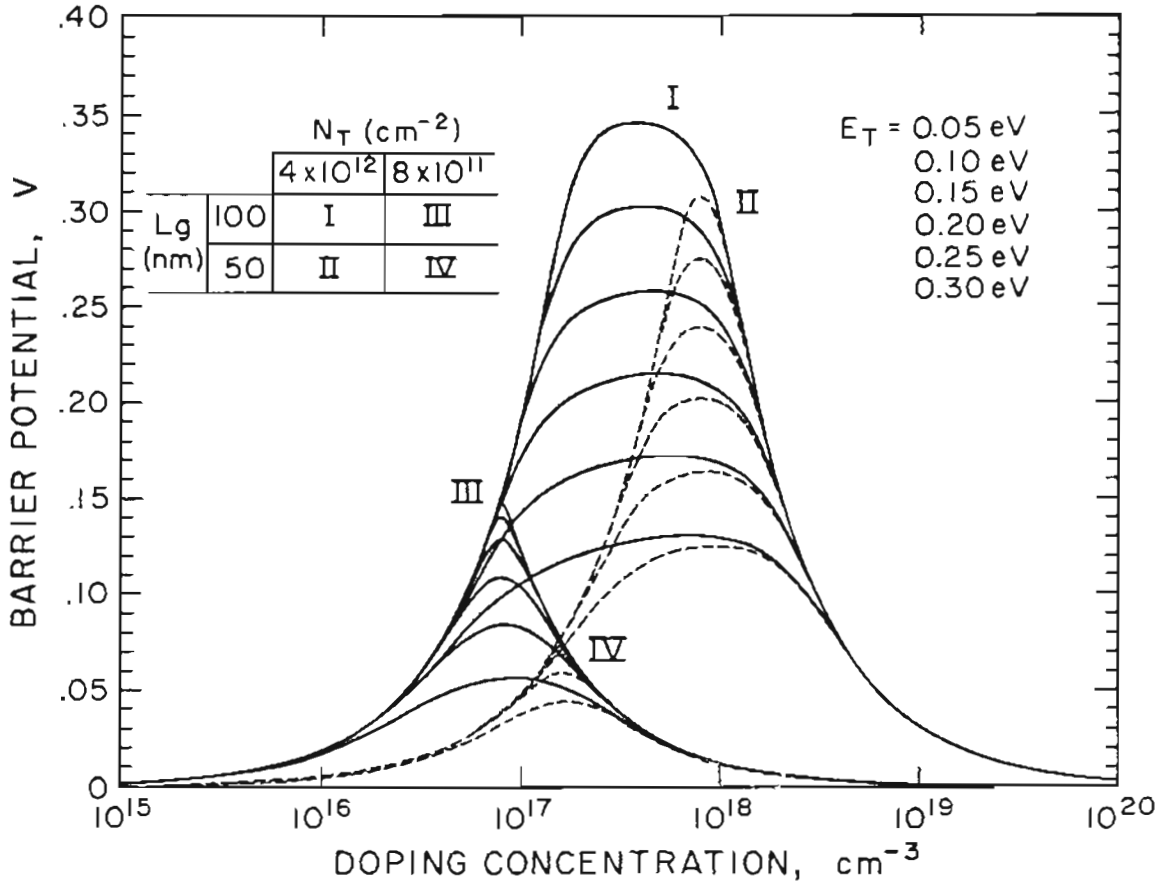

Figure 2-4 The magnitude of V_B versus doping concentration for different trap densities, levels and grain sizes. The six curves from top to bottom are calculated for E_T-values ranging from 0.05 to 0.30 eV away from the mid-gap.

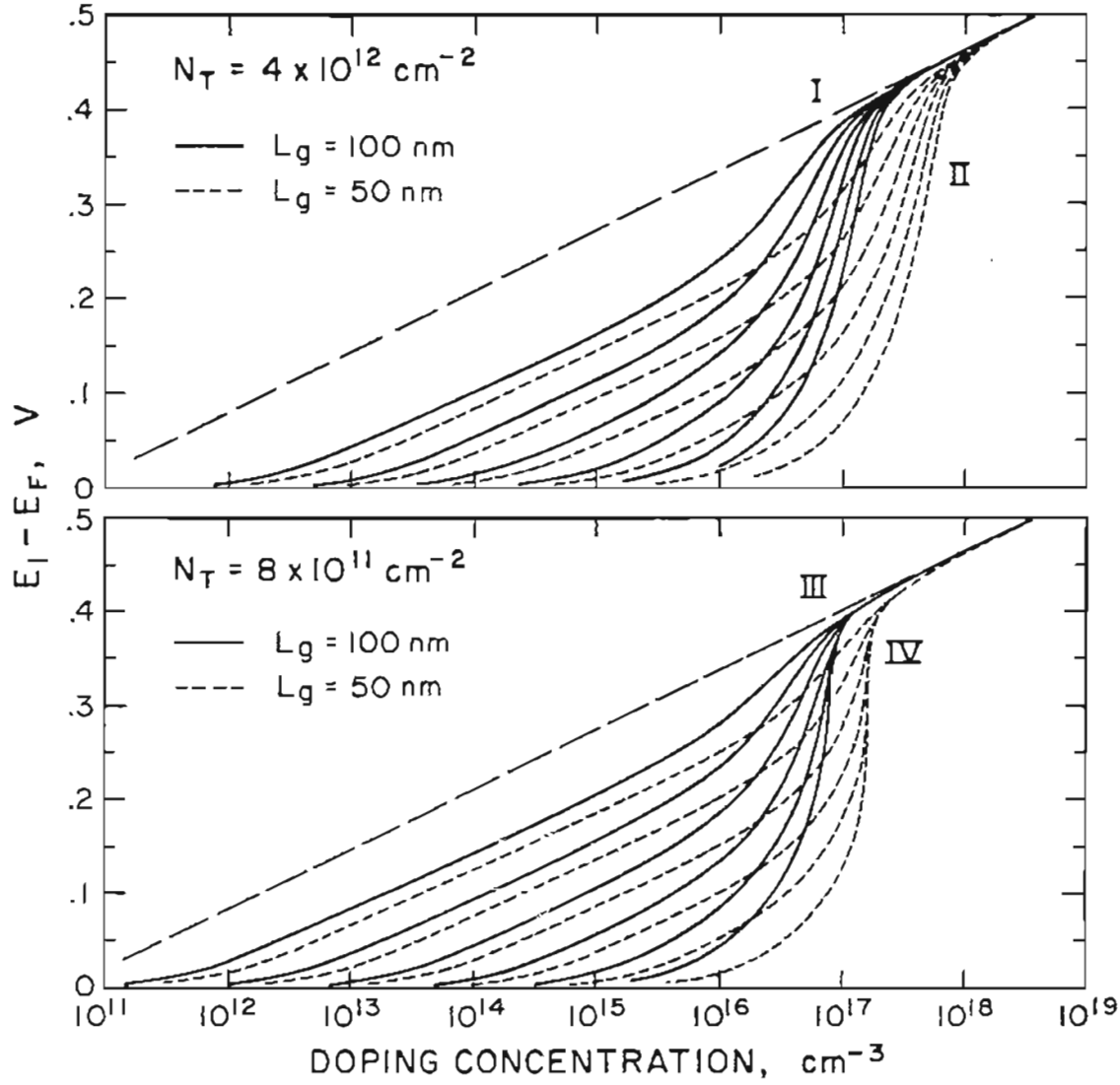

Figure 2-5 The Fermi-level in polycrystalline silicon. The parameters used for calculation are the same as those in Figure 2-4. The straight dashed line is the Fermi level in single crystalline silicon with Boltzmann approximation.

the Fermi level of crystalline silicon. For a wide low doping range $N_A << N^*$, almost all of the mobile carriers provided by dopant atoms are trapped in the grain boundaries and the grains are depleted of mobile (majority) carriers. The sheet resistance of the films in this range remains essentially constant with the doping concentration. With increasing doping concentration, however, the grain boundary trap sites are saturated and the mobile carrier density increases in grains and eventually approaches the value of N_A. The sharp decrease of E_F at $N_A \sim N^*$ reflects this behavior. The conduction properties in polysilicon are thus seen to be directly correlated to the grain boundary properties.

2.3 Conduction Properties in Polysilicon Thin Films

2.3.1 Sample Preparation

The experiment is designed to investigate the resistivity of polysilicon as a function of doping concentration, bias condition and temperature. Resistor bars of different aspect ratios (W/L) were fabricated in low-pressure chemical-vapor-deposited (LPCVD) polycrystalline silicon thin films with different doping concentrations. These films with a thickness ranging from 200 to 400 nm were deposited at 600°C on 300-500 nm thermal oxide grown on $<100>$ silicon wafers. To eliminate surface leakage, the test structures were encapsulated with 400 nm thick deposited oxide. The dopant activation was carried out in a 900°C anneal in nitrogen for 30 minutes. The final grain size (L_g) of

undoped samples was measured to be 50 ± 10 nm.

Some of the devices were passivated with nitride overcoat, followed by a 400°C anneal, in order to drive hydrogen into grain boundaries, reduce the density of trap sites (dangling bonds) therein, and enhance the conductivity.

2.3.2 *I-V* Characteristics of Undoped Samples at Room Temperature

The sheet resistance for different doping concentration is shown in Figure 2-6 and is nearly a constant in low and moderate doping range. In passivated samples the sheet resistance is lower than that of unpassivated ones by a factor of about 50.

The *I-V* data obtained from undoped samples are chosen for discussion, since in this case there is no space charge barrier potential near the grain boundary, which eliminates the unnecessary complications arising from V_B and exposes for interrogation the inherent role of grain boundaries, as it affects the carrier transport under a bias.

The room temperature *I-V* data are presented in Figure 2-7 for resistor bars, all of width W = 12 μm but of different electrical lengths L. From the extrapolation of sheet resistance versus drawn-length, the lateral diffusion of boron from the p^+ contact region was found to be 1 μm and excluded from the drawn-length. All of these *I-V* curves are typically linear in the small voltage range and strongly nonlinear for large bias.

The models based on thermionic or field emission theory for conduction in

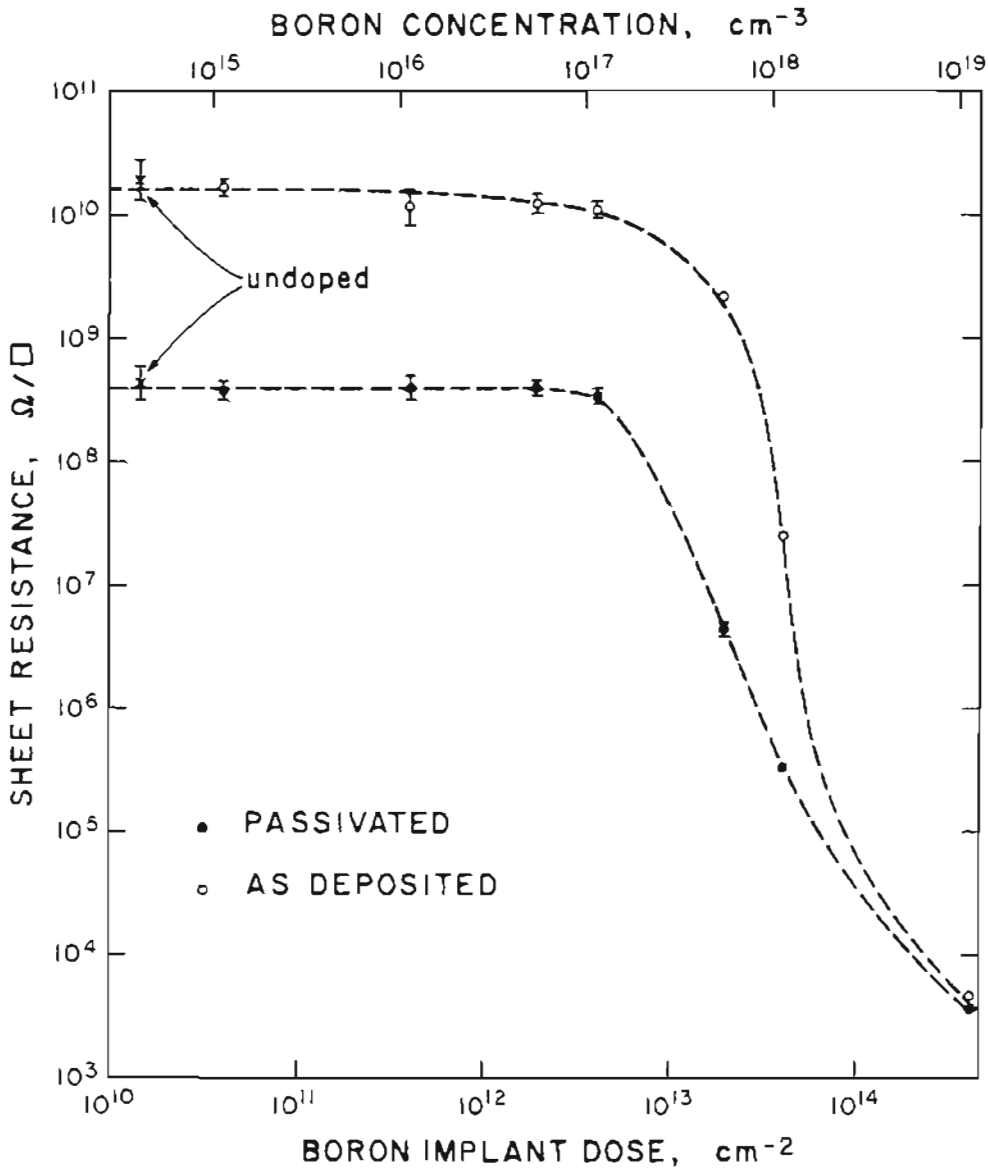

Figure 2-6 The sheet resistance versus boron concentration in as-deposited and nitride passivated polycrystalline silicon thin films at room temperature. The film thickness is 300 nm.

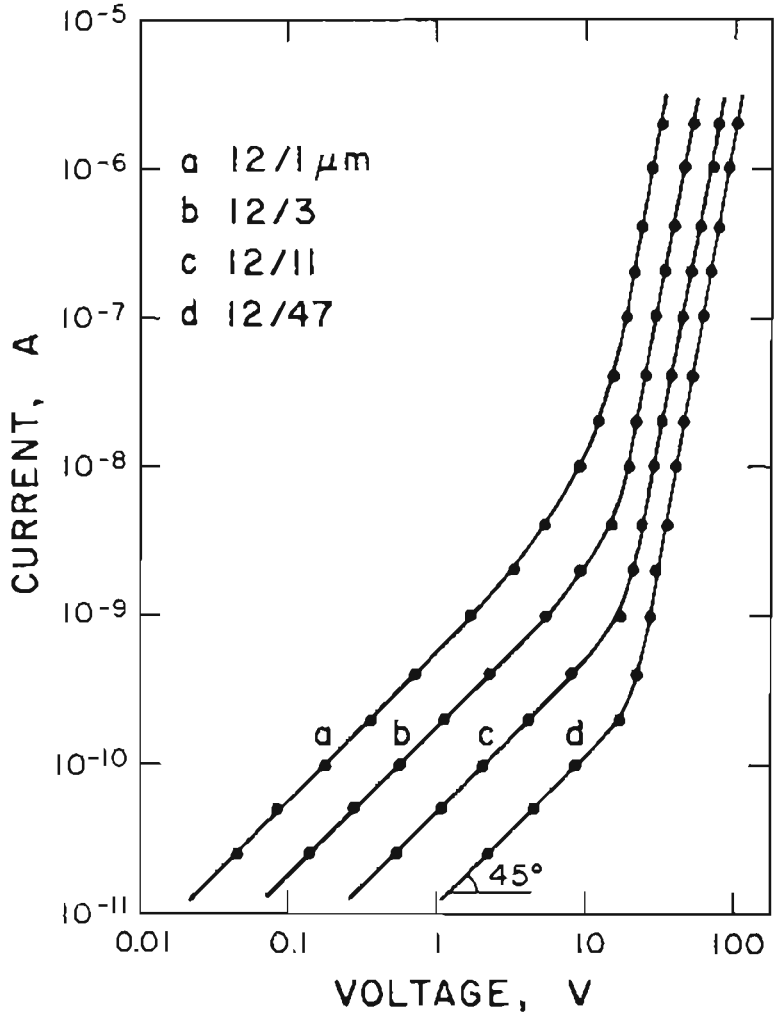

Figure 2-7 The current-voltage characteristics in undoped polycrystalline silicon resistor bars with a film thickness of 300 nm, width 12 μm and length of 1, 3, 5, 11, 23 and 47 μm.

polycrystalline silicon introduced a field-dependent conductivity and proposed a current density to take the form[9]

$$J = J_0 \sinh(qV/2k_B TN_g) = J_0 \sinh(qEL_g/2k_B T), \tag{2.14}$$

where $N_g = L/L_g$ is the number of grains comprising the resistor bar length, k_B the Boltzmann constant, T the temperature and E the average field applied. To compare with the theory, the same data are replotted in Figure 2-8 in a coordinate system of sheet resistance,

$$R_s = (V/I)(W/L) \tag{2.15}$$

versus the average field strength $E = V/L$. If (2.14) is valid, the current density should be same for given applied field and the curves in Figure 2-8 should then overlap. In the large field regime, the data depart drastically from this prediction and therefore cannot support an interpretation based on any thermionic and field emission theory.

2.3.3 Temperature Behavior

The temperature dependence of the sheet resistance is shown in Figure 2-9. The upper data set (open circles) was obtained at small currents (< 25 pA) to minimize the Joule heating within the sample. The measured temperature coefficient of resistance (TCR), $\partial(\ln R_s)/\partial(1/k_B T)$ is 0.56 eV which evidently corresponds to the activation energy (E_a) of intrinsic concentration n_i ($E_g/2$). Figure 2-9 also presents the sheet resistance data measured with 25 volts across 1 μm long resistor bar. The temperature characteristics of sheet

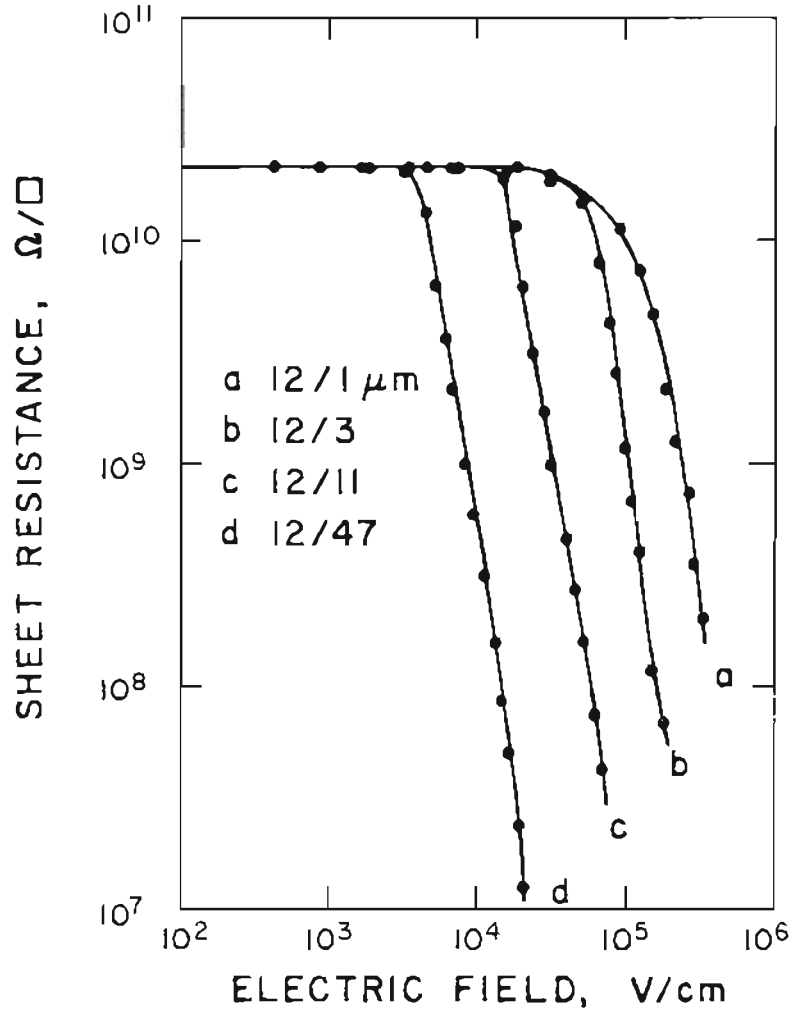

Figure 2-8 The sheet resistance $R_s = (V/I)\cdot(W/L)$ versus the average electric field $E = V/L$.

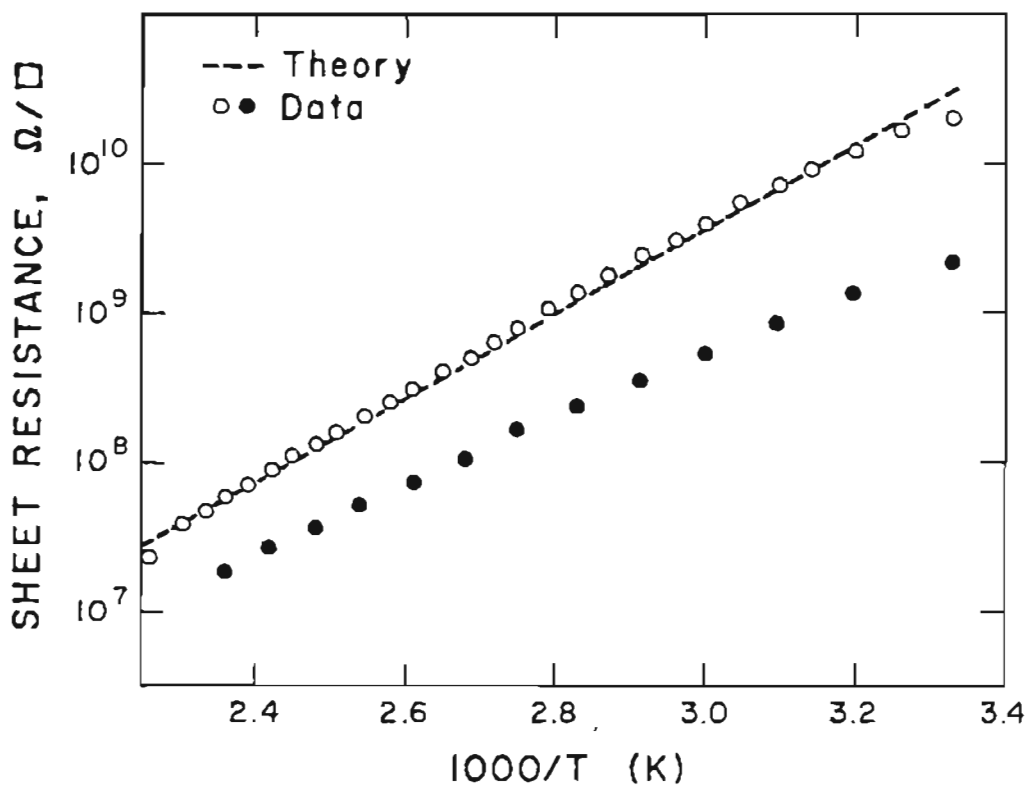

Figure 2-9 The sheet resistance in undoped samples versus the chuck temperature. The open circles are the data measured with a small bias (current less than 25 pA), and filled circles with 25 V applied to 1-μm resistor bar.

resistance according to an emission theory is proportional to $\exp(E_a - qV/2N_g)/k_BT$. In this case, $qV/2N_g \simeq 0.625$ eV is greater than E_a determined in the limit of small bias voltage to be 0.56 eV. Eq. (2.14) thus predicts that the sheet resistance should increase exponentially with the increasing chuck temperature. This prediction is again not supported by the experimental data.

2.3.4 Photo-current Characteristics

To further examine the carrier transport property in undoped polysilicon materials, a simple optical experiment was conducted using a He-Ne laser. The photon-induced guest-carriers, (n_{ph}) undergo the same conduction mechanism as those host-carriers (n_i). However, the number of guest-carriers are primarily dependent on the light intensity and less affected by other factors, such as temperature and bias conditions. The photo current (I_{ph}) was obtained by substrating dark current (I_d) from the current with laser light on. In Figure 2-10 and 2-11 are presented the ratio of photo and dark currents, and photo current itself, both as a function of applied voltage. The resistor bar with L = 1 μm was illuminated at 2.8 and 7 mW intensities with a spot size of $\sim$ 3 mm. The photogenerated guest-carrier

$$n_{ph} = (\Phi_l/\hbar\omega)\alpha\tau, \tag{2.16}$$

which is given in terms of photon flux in the polycrystalline silicon film $(\Phi_l/\hbar\omega)$ with Φ_l being the light intensity, the attenuation coefficient (α) and

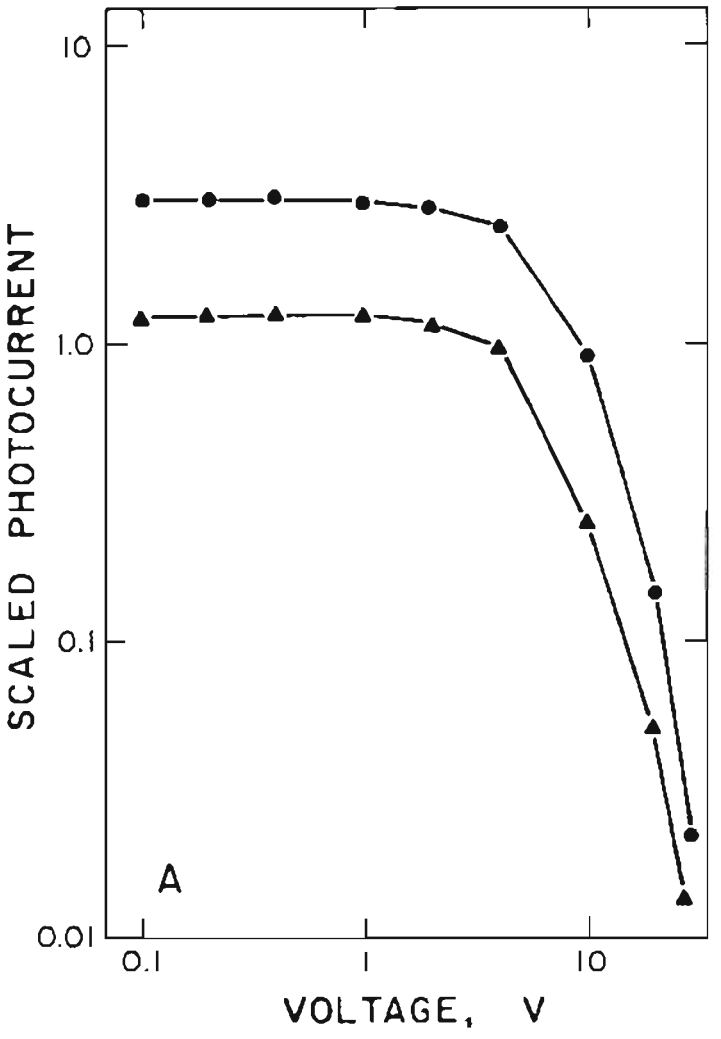

Figure 2-10 Photo-current scaled with dark current, $I_{ph}/I_{dark} = I_{lil}/I_{dark} - 1$ versus applied votltage. The sample investigated was 300 nm-thick, 12 μm-wide and 1 μm-long and illminated with a He-Ne laserbeam of a spot size 3 mm at power levels 7 mW (●) and 2.8 mW (▲).

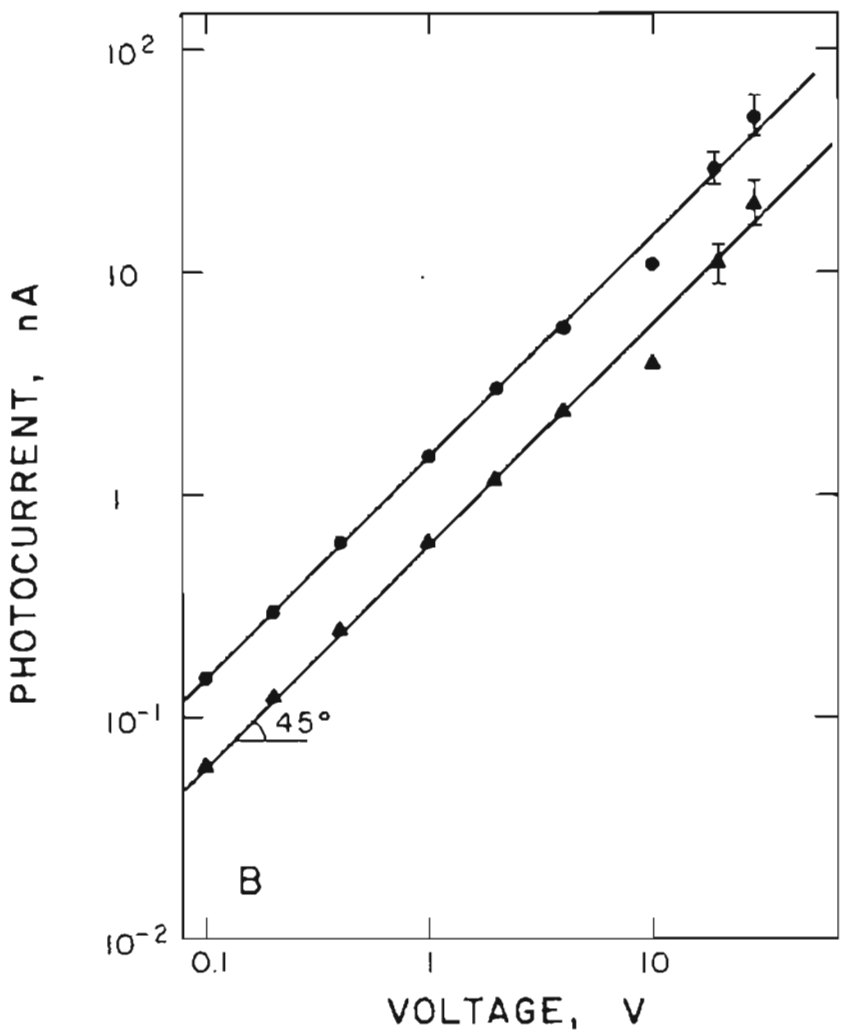

Figure 2-11 Extracted photo-current, $I_{ph} = I_{lit} - I_{dark}$ versus applied voltage. The testing conditions were same as those in Figure 2-10.

the carrier lifetime (τ), are swept across the resistor bar akin to the host-carriers (n_i). The following behaviors are expected for the thermionic or field emission models:

(i) the ratio of photo-current with respect to dark-current

$$I_{ph}/I_d = n_{ph}/n_i \tag{2.17}$$

should be independent of applied voltage, if the sample temperature does not change appreciably, and

(ii) the voltage dependence of the photo-current should exhibit the same non-linearity as that of the dark-current.

The measured ratio I_{ph}/I_d, however, decreases from $\sim$ 3 at small voltage to $\sim$ 0.01 at 20 V. The photo-current at 20 V is predicted from (2.14) to be greater than that at 1 V by a factor about 10^8. In the experiment, I_{ph} is linear with applied voltage up to 20 V ($E = 2\times10^5$ V/cm) and the observed value of $I_{ph}(20\text{V})/I_{ph}(1\text{V})$ is only 20. Again, the experimental data do not support a thermionic emission formulation for the current.

2.4 Discussions

These independent sets of data suggest that the nonlinear I-V characteristics in polysilicon cannot be attributed to the field-enhanced conductivity resulting from the grain boundary potential barrier. This leaves the Joule heating within the sample as one of the possible alternative mechanisms

responsible for the observed nonlinear I-V behavior. Indeed, the decreasing ratio, I_{ph}/I_d with increasing V is a signature for self heating of the sample. With the elevated local sample temperature, n_i will then grow exponentially, while n_{ph} may increase slightly with T via the temperature dependent attenuation coefficient, $\alpha(T)$. At milliwatts intensity for 3 mm-spot size, the direct laser-induced sample heating is negligible, as is borne out by the two I_{ph} values being directly proportional to the incident beam intensities over the entire voltage range.

The carrier transport in undoped samples is dictated by impurity and phonon scattering, as in single crystalline silicon. Yet, the mere presence of a grain boundary fundamentally affects the carrier transport in giving rise to a strong nonlinear I-V behavior. The data strongly indicate that the efficient local heating near grain boundaries is indeed operative and should be considered in conduction models.

In the diffusion-drift approach, the current density in an undoped sample is given by

$$J = q\mu n_i(T)\cdot(V/L), \tag{2.18}$$

with $\mu \simeq \mu^n + \mu^p$ given in terms of electron and hole mobilities in polycrystalline silicon. In the absence of grain boundary potential barriers, the electron and hole mobilities as derived by Kim *et al* [8] are

$$\mu^n = \mu_c^n/[1+(\delta/L_g)(\mu_c^n/\mu_{gb}^n)(n_g/n_{gb})] \ . \tag{2.19a}$$

$$\mu^p = \mu_c^p/[1+(\delta/L_g)(\mu_c^p/\mu_{gb}^p)(p_g/p_{gb})] \qquad (2.19b)$$

where n_{gb}/p_{gb} is the electron/hole concentration in amorphous grain boundaries beyond the mobility shoulder (the conduction or valence bands difference bewteen crystal and amorphous silicon for n-type or p-type materials)[10] which determines the quasi band gap therein; δ the grain boundary width and μ_{gb}^n/μ_{gb}^p the extended state electron/hole mobility in grain boundaries. For the intrinsic sample with no barrier potential, the current should be linear with voltage, in this model. Any departure from linearity is assumed to arise from the sample heating, via the temperature dependence of the intrinsic carriers.

With increasing voltage which induces a concomitant elevation in sample temperature, the intrinsic concentration grows exponentially, compared to the photogenerated carrier density which increases linearly with temperature ($n_{ph} \propto T$ via the temperature dependence of the lifetime). Hence, the ratio of photocurrent with respect to dark current, I_{ph}/I_{dark} should fall with increasing voltage. This is consistent with the data (see Figure 2-10). On the other hand, the predicted photocurrent density from eq. (2.18) with n_{ph} replacing n_i should not be affected by sample temperature and should increase linearly with voltage. This prediction is explicitly borne out in Figure 2-11.

The local temperature increase within samples has been modeled and discussed phenomenologically, and a quantitative analysis has been presented by

Kim *et al*[11]. The experimental data can be explained by the model. Indeed, in view of the inconsistency of the data and field emission models, local Joule heating is perhaps the only possibly alternate mechanism remaining, which can explain the nonlinear I-V behavior.

The electrical conduction in undoped polycrystalline silicon thin films has been examined. The current-voltage curves obtained from these samples exhibit nonlinear behavior at current levels as low as a few nanoamperes and field strength of 5×10^3 V/cm. In this reversible and nonlinear I-V regime, current does not scale with respect to the applied field. This unambiguously indicates that the nonlinear I-V behavior cannot be attributed to any field-enhanced conduction mechanism. The Joule heating within the sample is experimentally shown to be operative and is consistent with the photoconductivity data.

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CHAPTER 3

THIN-FILM TRANSISTOR FABRICATION

3.1 Introduction

The field-effect transistors were fabricated in low-pressure chemical-vapor-deposited (LPCVD) polycrystalline silicon thin films for characterization and modeling. The schematic cross-sectional view of the n-channel (n^+-p-n^+) and p-channel (p^+-p-p^+) device structures are sketched in Figure 3-1. Since the grain boundary properties have a drastic effect on the electrical characteristics of polysilicon materials, the reduction of trap states by passivating grain boundaries is helpful in improving device performance. During passivation, reactive atomic hydrogen is incorporated into grain boundaries and attached to the dangling bonds. As a result, the grain boundary trap state density reduces and effective mobility increases. Hydrogen for passivation can be obtained from plasma silicon nitride [1,2] or H^+-implantation, [3] followed by a anneal around $400-450°C$.

In this work, the thin film transistor samples were divided into 5 groups by using different process parameters, including devices fabricated in as-

deposited and passivated polysilicon thin films.

Test structures for C-V measurement were also designed and fabricated.

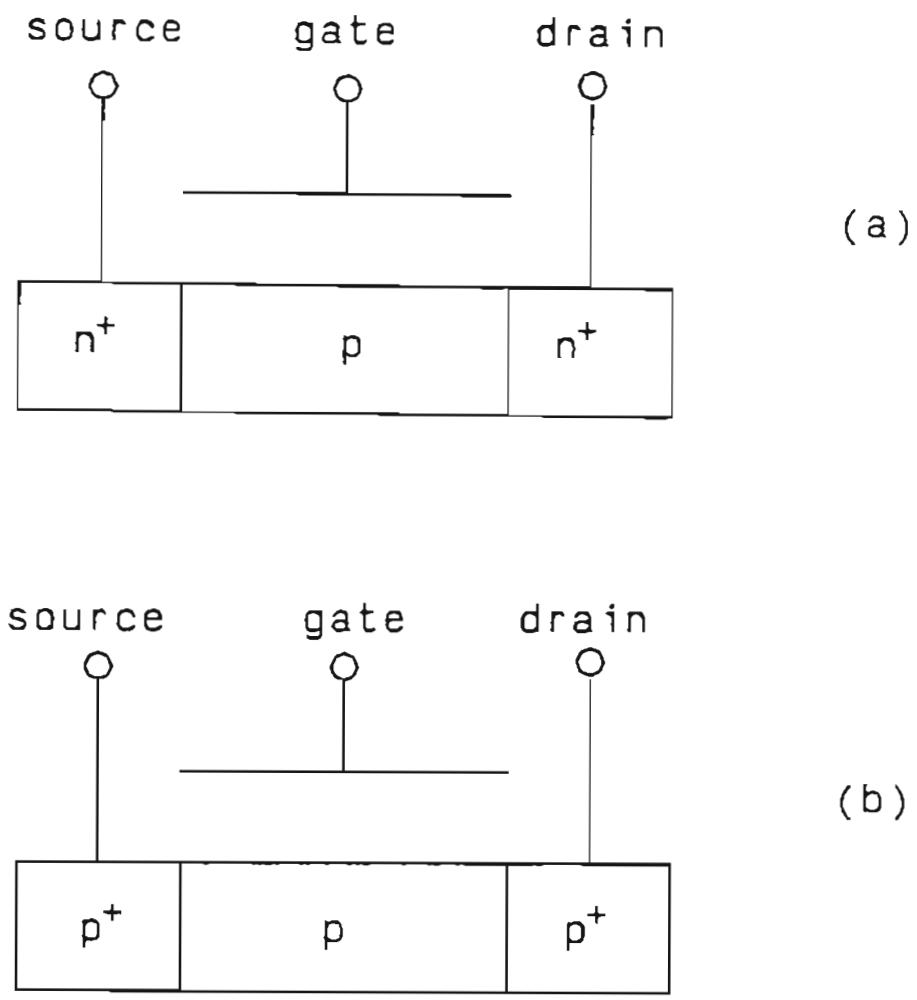

Figure 3-1 Schematic cross-sectional view (a) for n^+-p-n^+, n-channel and (b) for p^+-p-p^+, p-channel devices.

3.2 Polysilicon Thin-Film Transistor Samples Preparation

The starting material for device fabrication was 20 Ω-cm <100> p-type silicon wafers.

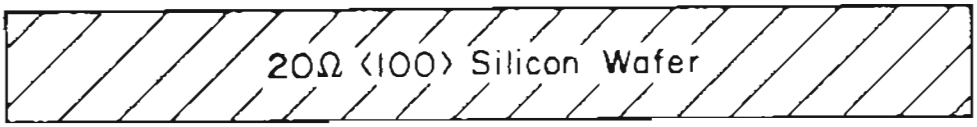

Figure 3-2(a) RCA cleaned silicon wafer as substrate for TFT's fabrication.

After a routine RCA cleaning which removes organics and heavy metal particles from the surface, the wafers were oxidized in pyrogenic steam at 1050°C for 35 minutes. Thermal oxide with a thickness of 500 nm was grown on the wafer to separate transistors from the substrate.

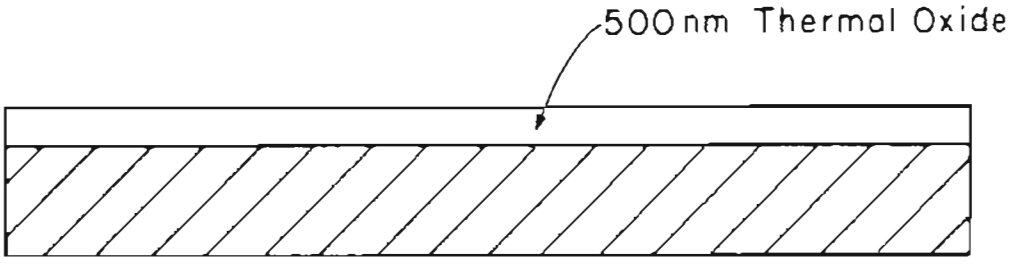

Figure 3-2(b) Thermal oxide grown on the wafer to a thickness of 500 nm.

A 200 nm-thick polycrystalline or amorphous silicon layer was deposited through the thermal decomposition of silane:

$$SiH_4 = Si + 2H_2$$

on the oxide in a commercial LPCVD system at a presure of 0.2 Torr. The deposition temperatures selected were: 620°C (high-temperature) to produce polycrystalline channel layer and 540-550°C (low-temperature) for amorphous layer. The channel doping was carried out by ion implantation with a boron dose of $6-8\times10^{11}$ cm^{-2}. The poly/amorphous silicon was then patterned with photoresist and etched into individual islands.

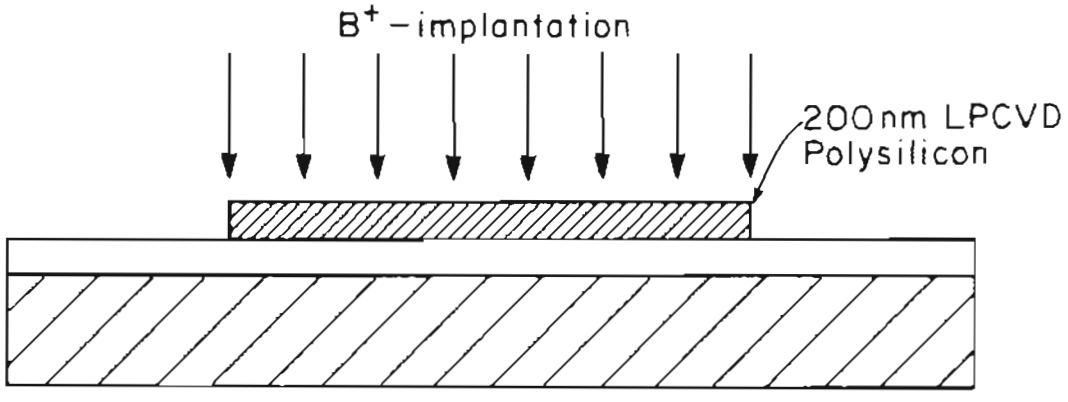

Figure 3-2(c) 200 nm-thick silicon layer deposition followed by $11B^+$-implantation and then pattern and etch into individual islands.

Following a piranha clean, a gate oxide layer was grown in dry oxygen.

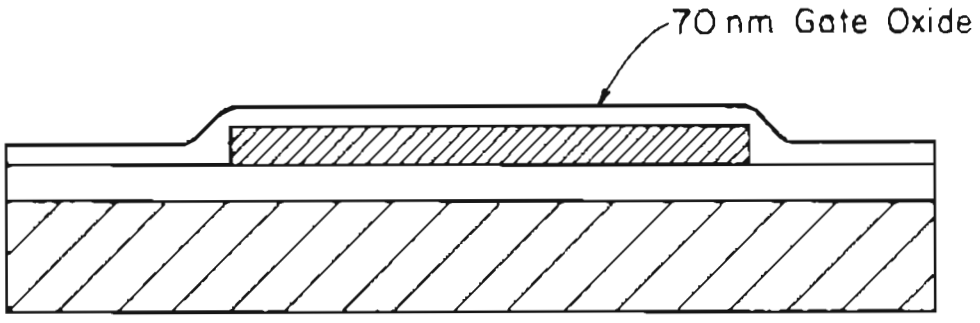

Figure 3-2(d) Gate oxide grown in dry oxygen.

Part of the samples had a second gate insulator layer which was formed by LPCVD silicon nitride. The deposition was carried out at 800°C:

$$3H_2SiCl_2 + 4NH_3 = Si_3N_4 + 6HCl + 6H_2$$

at a presure of 0.2 Torr for 15 minutes. The nitride oxidation was also carried

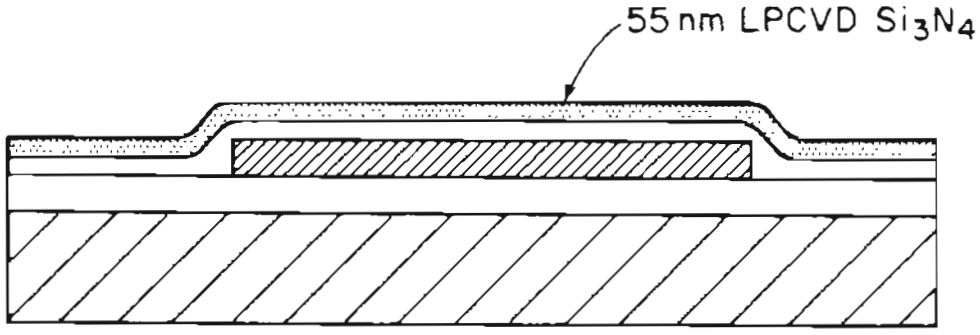

Figure 3-2(e) Second layer of gate insulator formed by LPCVD silicon nitride deposition followed by nitride oxidation.

out in pyrogenic steam. The resulting layer of approximately 10 nm-thick oxidized silicon nitride served as an etch-stop for the next process step.

The polysilicon gate was deposited at a thickness of 200-400 nm, using the same conditions as the channel deposition. It was then patterned and etched. Before implanting the source and drain, a thin oxide layer was grown on top of the polysilicon, to ensure that the peak of dopant profile was located near the surface.

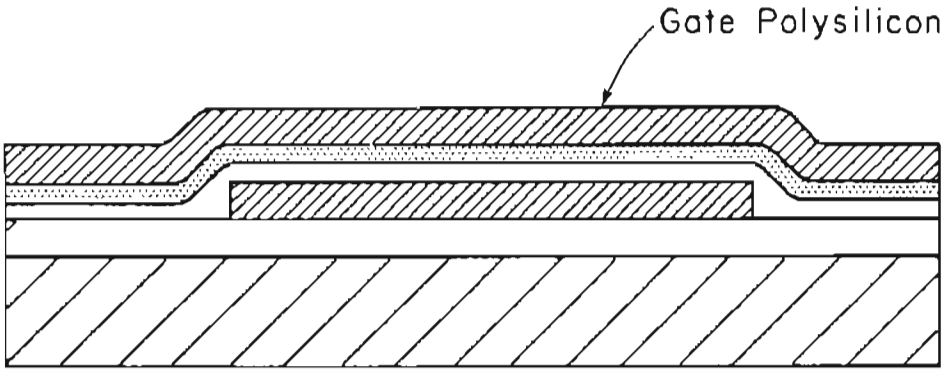

Figure 3-2(f) Gate polysilicon layer deposition.

Self-aligned sources and drains were formed by arsenic or phosphorus implantation for n-channel and boron for p-channel devices, respectively. The samples were then annealed at 900-920°C for 60 minutes in oxygen. This served several purposes: (i) drive-in for activating dopant atoms; (ii)

recrystallizing the low-temperature-deposited amorphous channel layers into polycrystalline silicon; and (iii) forming a protective oxide layer to improve the dielectric integrity.

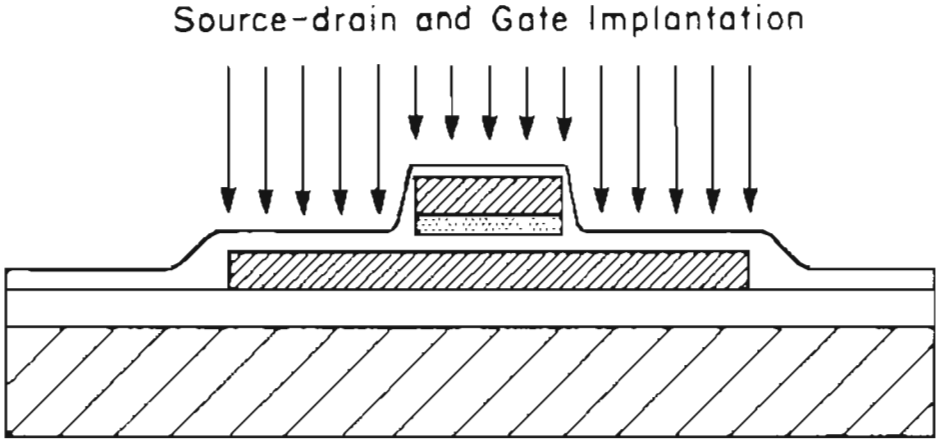

Figure 3-2(g) After gate pattern and etch, a thin oxide layer was grown and self-aligned source-drain and gate were implanted simultaneously.

The plasma silicon nitride overcoat as a hydrogen diffusion source was deposited at 290°C to a thickness of 900 nm. The devices were then annealed in N_2 atmosphere.

Processing was completed by contact pattern, etch, 1-μm aluminum with 1.5-percent Si deposition, pattern, etch, and 400°C forming gas (15% H_2+85% N_2) sintering.

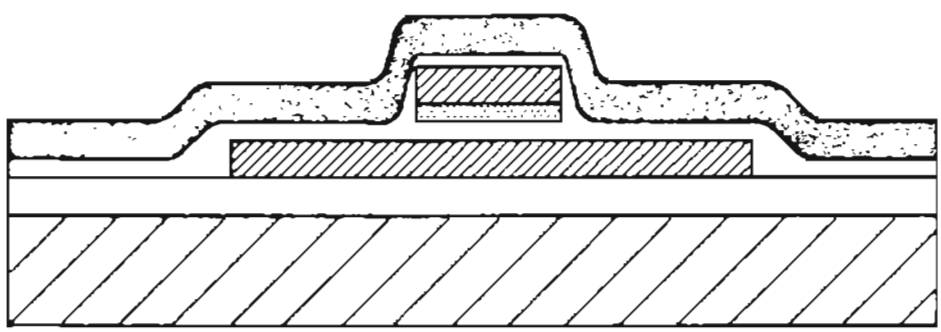

Figure 3-2(h) Plasma nitride overcoat.

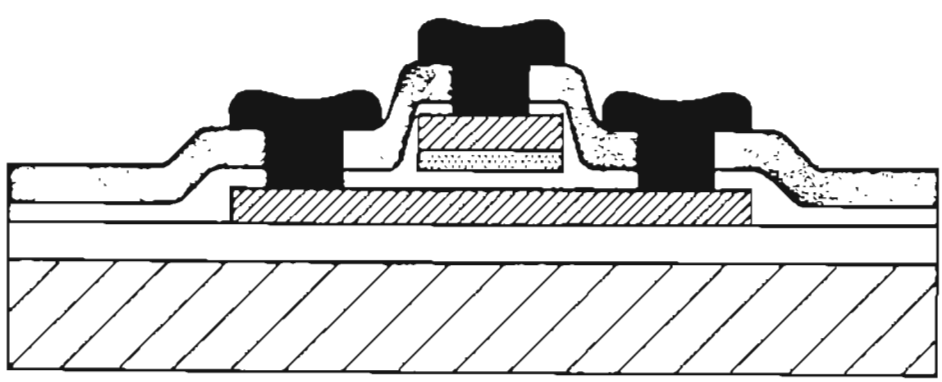

Figure 3-2(i) Metallization by aluminum with 1.5-percent silicon.

Some of the devices were H^+-implanted with different doses for grain boundary passivation, followed by anneal to activate the H-atoms and remove the surface damage due to implantation. The major process steps are graphically illustrated in Figure 3-2. The processing parameters are listed in Table 3-1.

Table 3-1

Parameters	Sample					Unit
	#1	#2	#3	#4	#5	
Channel type	n	n	p	n	p	-
Deposition temperature	620	540	540	550	550	°C
Film thickness	200	190	190	200	200	nm
Channel boron dose	7×10^{11}	6×10^{11}	6×10^{11}	8×10^{11}	8×10^{11}	cm^{-2}
Gate oxide thickness	37	71	71	60	60	nm
Gate nitride thickness	-	55	55	-	-	nm
Source/drain dopant	$75As^+$	$31P^+$	$11B^+$	$75As^+$	$11B^+$	-
Source/drain dose	3×10^{15}	5×10^{15}	5×10^{15}	4×10^{15}	2×10^{15}	cm^{-2}
H^+-dose	-	1×10^{12}	1×10^{12}	1×10^{15}	1×10^{15}	cm^{-2}

Table 3-1 Process parameters for TFTs fabrication.

3.3 Test Structure for C-V Measurement

In a related experiment, C-V structures were fabricated as shown in Figure 3-3. The upper polysilicon layer was heavily doped and served as a gate electrode. The gate dielectric consisted of 20 nm of oxide. The lower, electrically active layer consisted of 500 nm undoped, n-doped (phosphorus, 4×10^{12} cm^{-2}) or p-doped (boron, 4×10^{12} cm^{-2}) polysilicon. This lower layer was in electrical contact with the single crystal silicon substrate which was low-resistivity n-type for n-doped, and p-type for p-doped and undoped samples. This substrate also served as a "low" electrode in the C-V measurement.

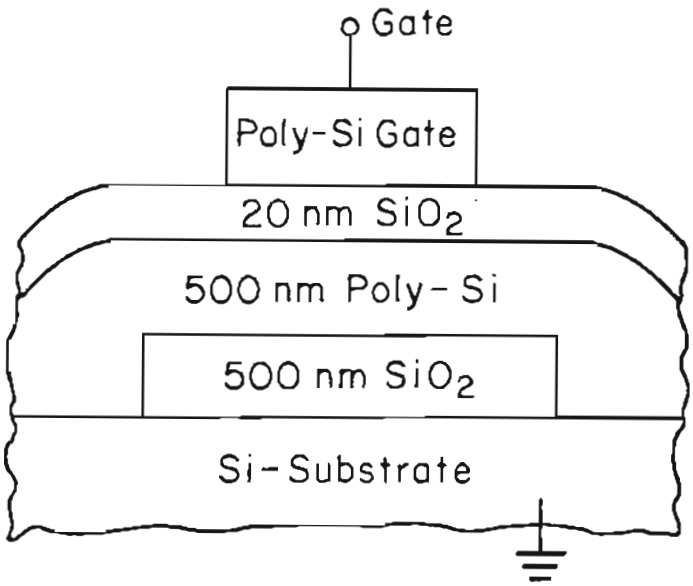

Figure 3-3 The test structure used for C-V measurements.

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CHAPTER 4

DEVICE CHARACTERIZATION

4.1 Introduction

The devices, fabricated as described in Chapter 3, are characterized with the use of a Ruckers-Koll probe station connected to Keithley voltage sources and electrometer, controlled by a Hewlett-Packard 8290 computer. The testing circuit is shown in Figure 4-1.

The lateral diffusion of dopant ions from source and drain contact regions into the channel was found to be $\sim$ 1 μm from the extrapolation of drain current plotted as a function of drawn-length. The channel length is obtained by excluding lateral diffusion length from the drawn-length. At fixed gate and drain voltages (except in the leakage regime of device operation), the currents scale with the channel length.

The transconductance, I_D-V_G (drain current versus gate voltage), characteristics for devices with different process conditions are presented in Figures 4-2 through 4-7. The n-channel TFT's data observed from sample #1 are presented in Figures 4-2 and 4-3, and those from sample #2 in Figures 4-4

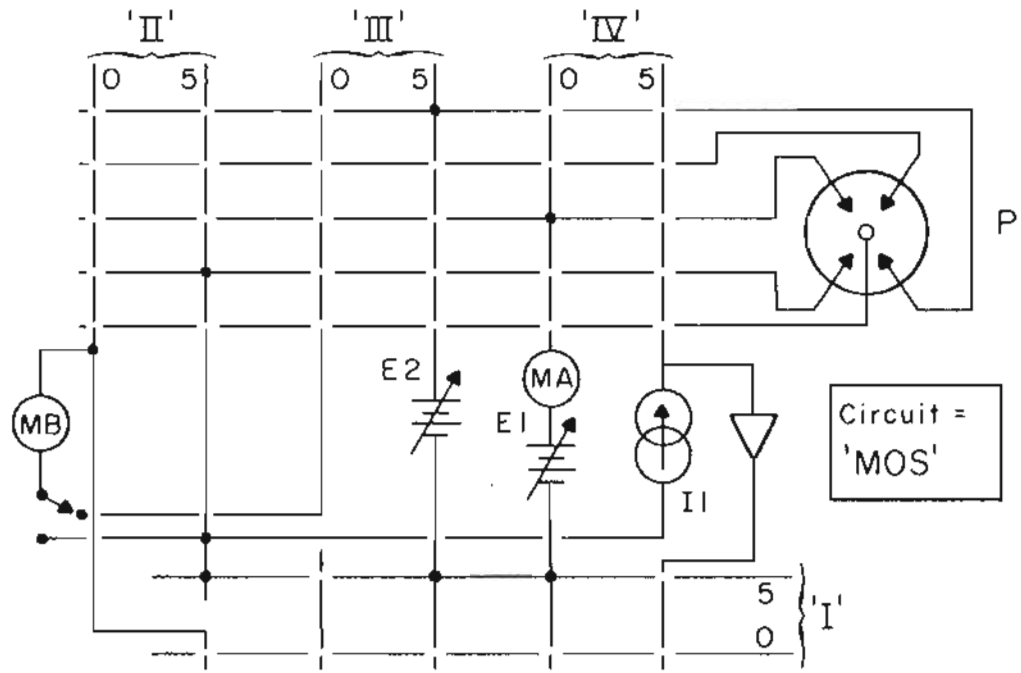

Figure 4-1 The testing circuit for thin film transistor characterization. E1 and E2 are Keithley 230 programmable voltage sources, I1 Keithley programmable current source, MA/MB Keithley 619 electrometer/multimeter, P Rucker & Koll 683A probe station and the switch box HP 3495A scanner. All are controlled by a Hewlett-Packard 9816 computer.

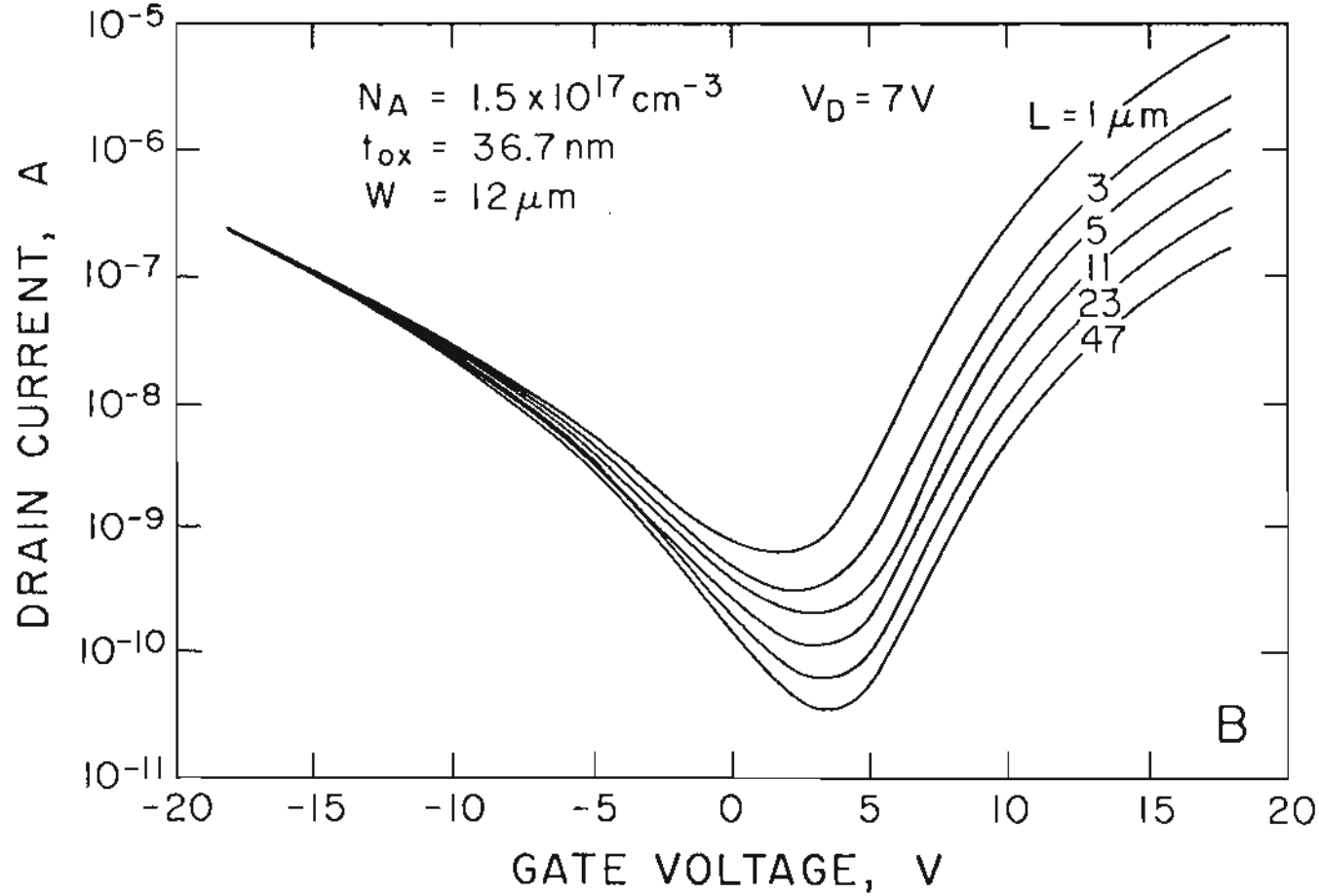

Figure 4-2 Transconductance I_D-V_G data obtained from sample #1 for channel length = 1, 3, 5, 11, 23 and 47 μm at a fixed drain voltage V_D = 7 V. The channel length becomes less important in affecting the leakage current at large negative gate voltages.

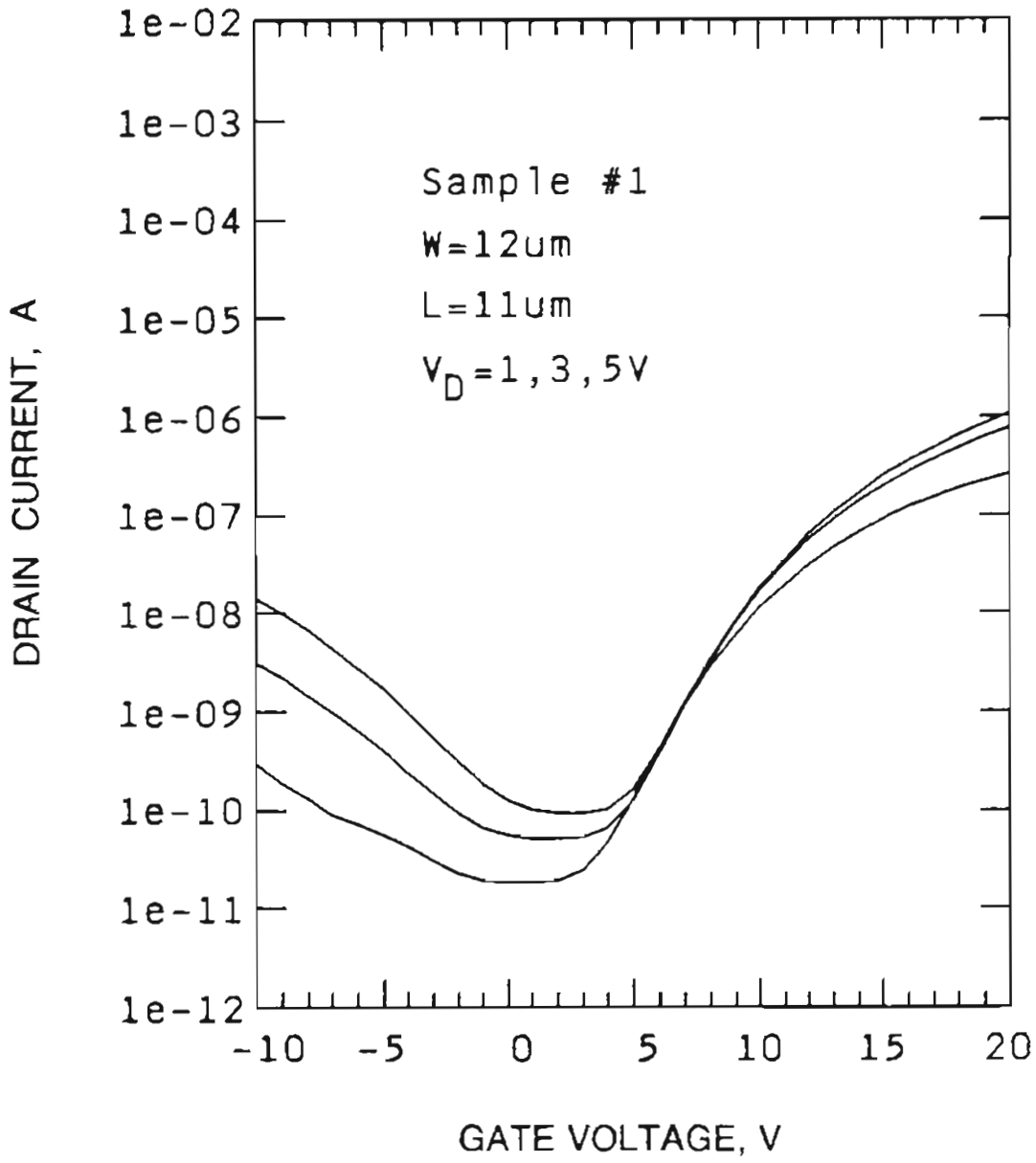

Figure 4-3 Transconductance I_D-V_G data obtained from sample #1, with a 11 μm-long device for V_D = 1, 3 and 5 V, respectively.

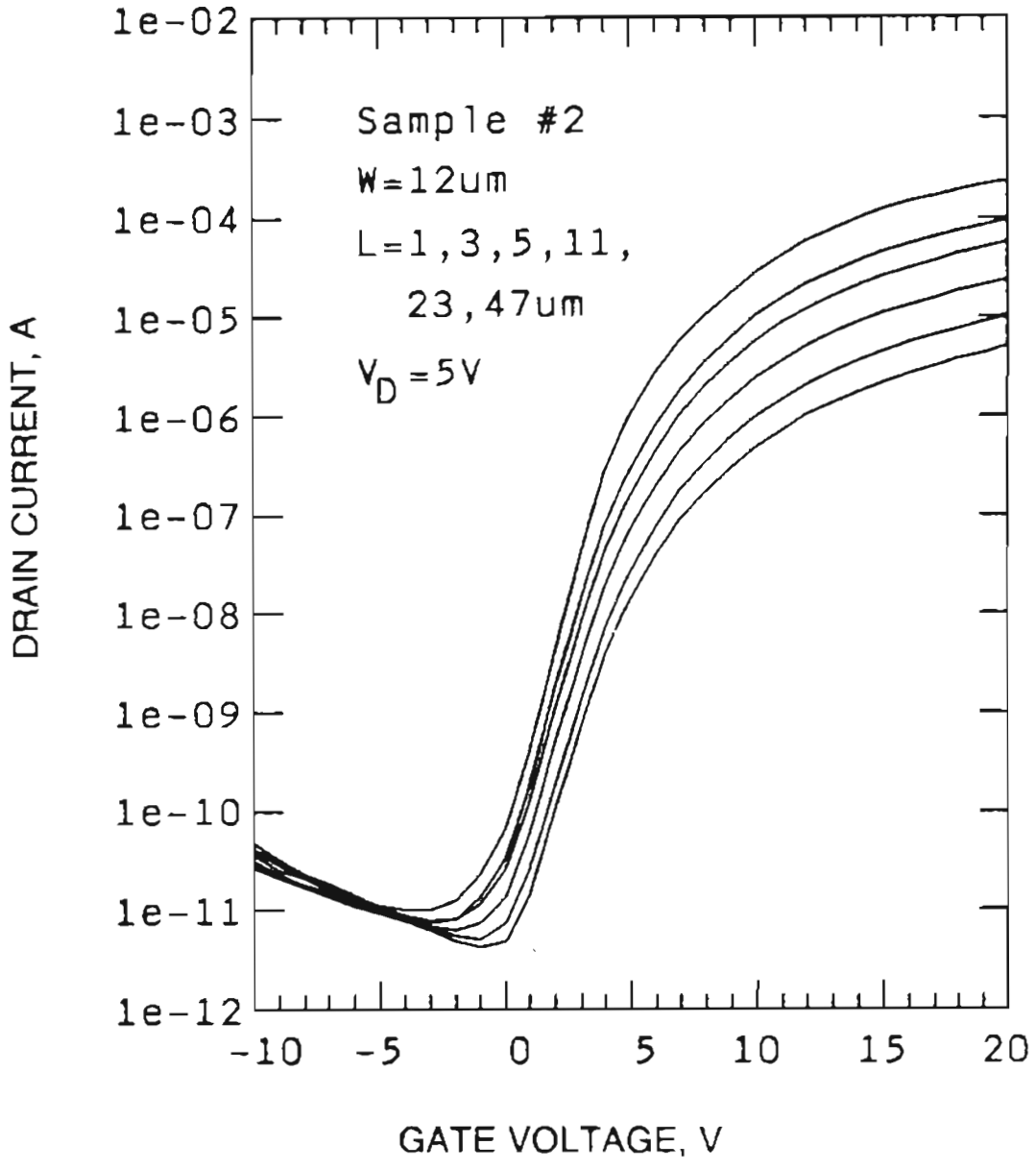

Figure 4-4 Transconductance I_D-V_G data obtained from sample #2 for all channel lengths. Note in this case the junction behavior has been improved due to nitride passivation, and the leakage current

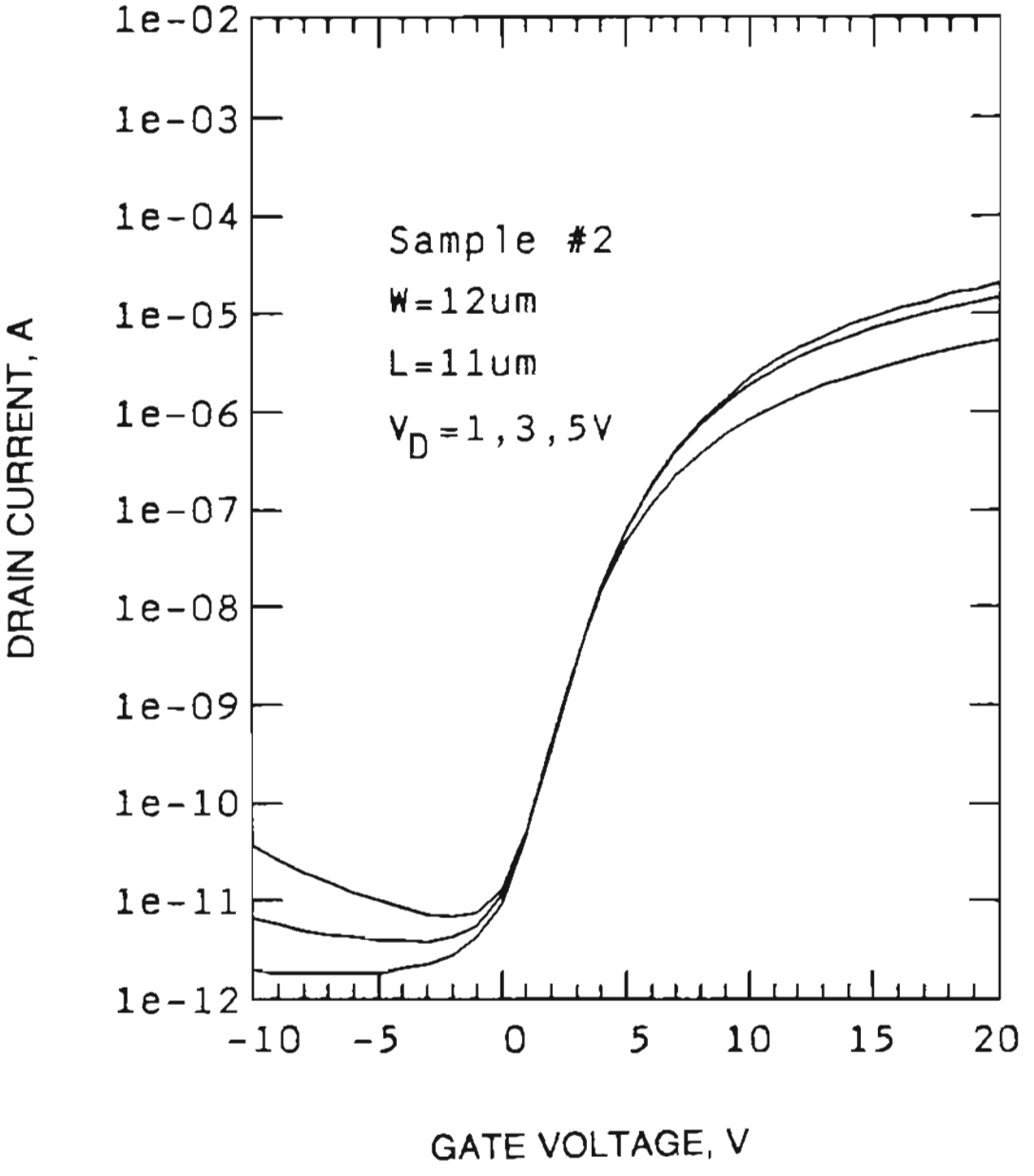

Figure 4-5 Transconductance I_D-V_G data obtained from sample #2, with a 11 μm-long device for V_D = 1, 3 and 5 V, respectively.

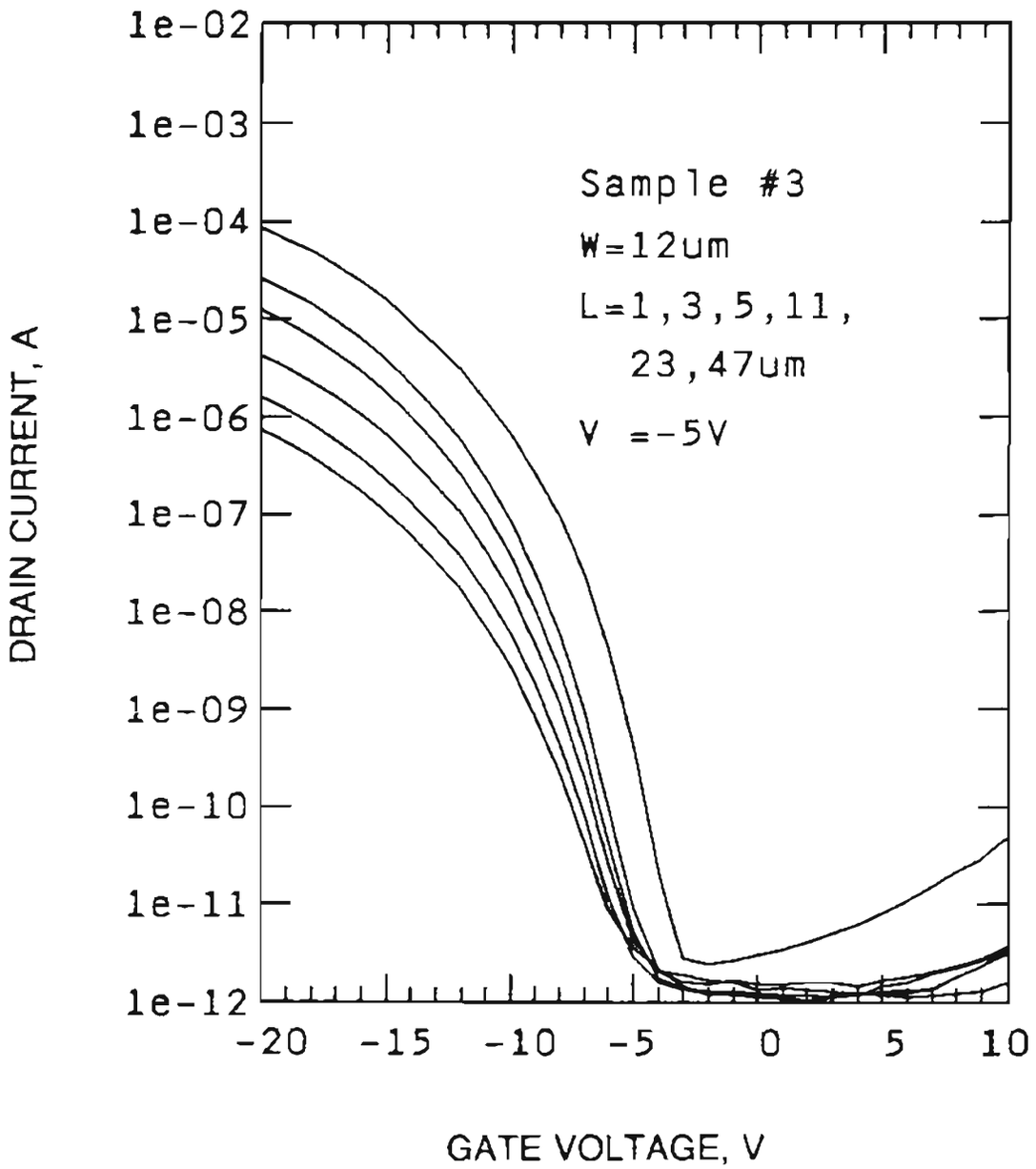

Figure 4-6 Transconductance I_D-V_G data obtained from sample #3 for all channel lengths with V_D = -5 V. It appears that the junction behavior is better than that in n-channel devices of sample #2.

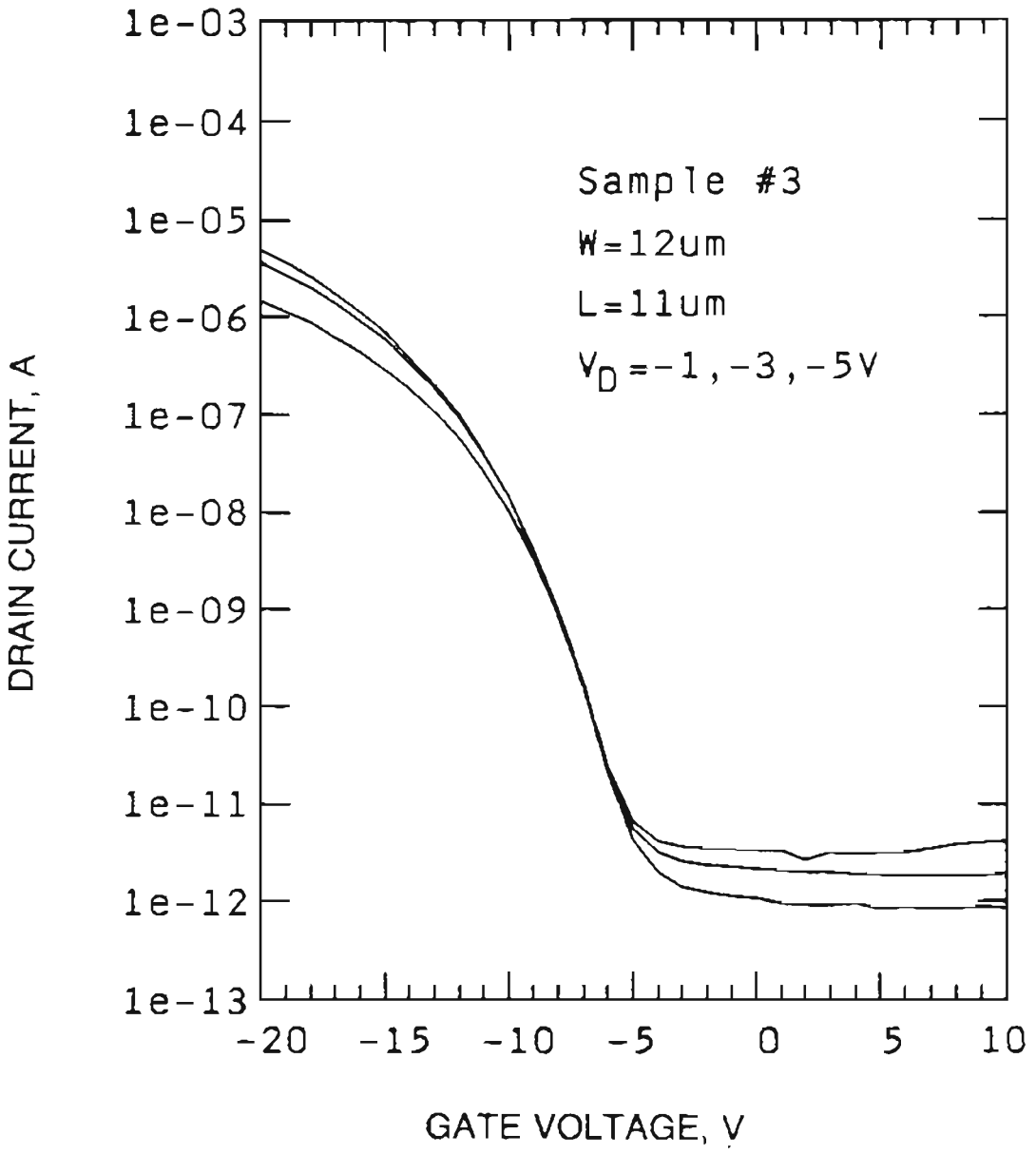

Figure 4-7 Transconductance I_D-V_G data obtained from sample #3, with a 11 μm-long device and V_D = −1, −3 and −5 V.

and 4-5, and the p-channel data are plotted in Figures 4-6 and 4-7, respectively. The I_D-V_G data in Figures 4-3, 4-5 and 4-7 are from one device for several different drain voltages while the data in Figures 4-2, 4-4 and 4-6 are from selected devices with different channel lengths at a fixed drain voltage. The transconductance I_D-V_G curve covers the leakage, subthreshold and drive current regimes.

4.2 Leakage Behavior and Discussion

The leakage current is the drain current in the negative/positive gate voltage range for n-/p-channel devices. In this section the gate voltage will be considered to be confined to the leakage regime. Note that the leakage current increases with both $|V_G|$ and $|V_D|$.

There are two parameters directly affecting the leakage behavior. The first parameter is the resistance of the reverse-biased polysilicon p-n junction at the drain-end, R_j, which depends sensitively on the drain voltage applied. The second parameter is the channel resistance R_{ch} which changes dynamically with the gate voltage. The relative importance of these parameters is dependent on the specific process conditions. The total resistance R of the device is provided by R_j and R_{ch}, connected in series,

$$R = R_j + R_{ch} \tag{4.1}$$

and the leakage current is given by

$$I_L = V_D/R. \tag{4.2}$$

Because of the leaky nature of polysilicon p-n junctions especially those in high-temperature deposited films, the higher channel resistances resulting from a lower mobility and lower carrier concentration could be comparable with or greater than the leaky-junction resistance in small gate voltage range, and primarily determine the leakage level. With increasing magnitude of gate voltage, the channel resistance reduces rapidly, as more majority carriers are

accumulated in the channel, whereas, the junction resistance varies primarily with drain voltage. These lead to a strong dependence of the leakage current on gate and drain voltages as well as on channel lengths. This is explicitly borne out in these figures. For high-temperature-deposited devices with fixed gate and drain voltages (see Figure 4-2), I_L approximately scales with channel lengths. This indicates that R_{ch} is indeed greater than R_j in these devices.

With increasing magnitude of gate voltage in the leakage regime, the channel conductance is greatly enhanced by accumulated majority carriers. Eventually the channel resistance is reduced to a level much lower than that of the junction. The leakage current is primarily determined by the junction resistance, regardless of the channel length. This is again borne out by the data presented in Figure 4-2 which shows that for large values of $|V_G|$ the leakage levels are all about same.

The leaky behavior of the reverse biased p-n junction in unpassivated films can be observed in Figure 4-3 where the leakage current increases exponentially with drain voltage (for $V_G < 0$).

The grain boundary trap states are responsible for the leaky behavior of polysilicon p-n junctions. These trapping states give rise to the enhanced generation/recombination within the depletion regions[1], and/or field emission in the grain boundaries[2]. Another important effect of the trap states is that they greatly enhance the tunneling probability of carriers across the thin potential barrier near the drain-end (see Figure 4-8) created by the high

voltage difference between gate and drain[3]. A quantitative analysis of this tunneling is required in order to understand the leakage behavior in TFT's.

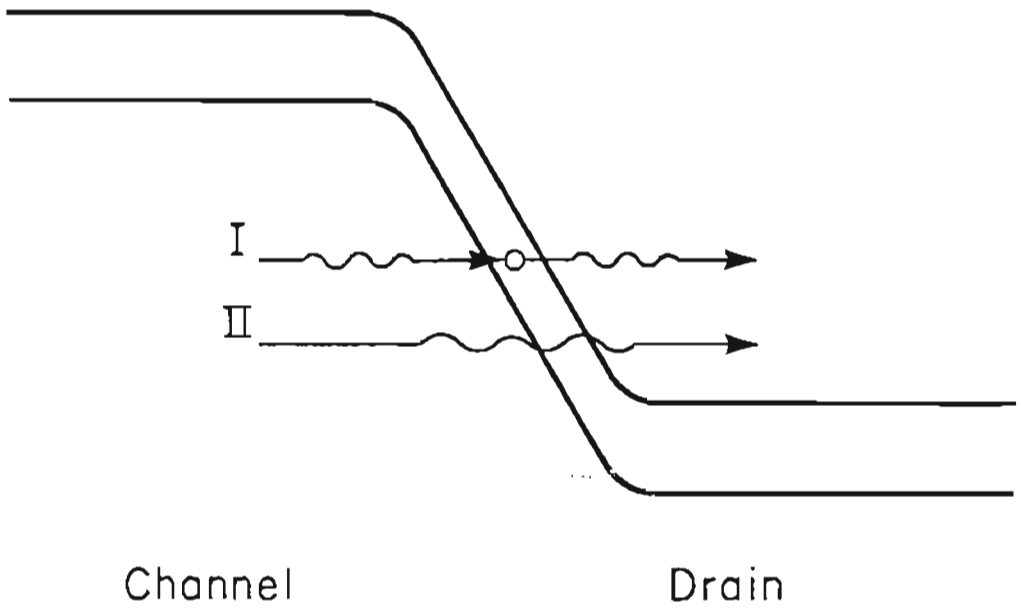

Figure 4-8 The energy band near the drain-end for a negative gate voltage applied to a n-channel TFT. A thin potential barrier is developed. The electron tunneling through this barrier is significant due to the trap states in the grain boundaries therein. Note that the tunneling probability in step I (case of polysilicon TFTs) is higher than that in step II (case of single crystal MOSFETs).

4.3 Subthreshold Current and Discussion

The subthreshold current is the drain current for gate voltage in the range between leakage and drift, and is generally believed to be dominated by the diffusion component. The observed subthreshold slope ($\partial \ln I_D / \partial V_G$) in polysilicon TFT's is usually smaller than that in bulk silicon MOSFET's.

For a small gate voltage beyond the leakage region, the drain current grows nonlinearly with increasing drain voltage, especially at higher V_D as shown in Figure 4-9. This I-V behavior resembles the typical nonlinear I-V characteristics observed in bulk polysilicon thin films, and can be understood in terms of a large operating field and impact ionization-induced hot-electron/hole. With the absence of a substrate contact, the hot-carriers, which would give rise to substrate current in bulk silicon MOSFET's, are all collected at the source and greatly enhance the current.

With increasing gate voltage, the electric field at the drain is reduced and the hot-carrier-generation becomes inefficient. That is, at a larger drain voltage and small gate voltage, the current decreases with increasing gate voltage (see Figure 4-9). This hot-carrier-induced current behavior can significantly degrade the device performance in the subthreshold regime. Without the hot-carrier generation, the subthreshold slope would be much larger than that observed.

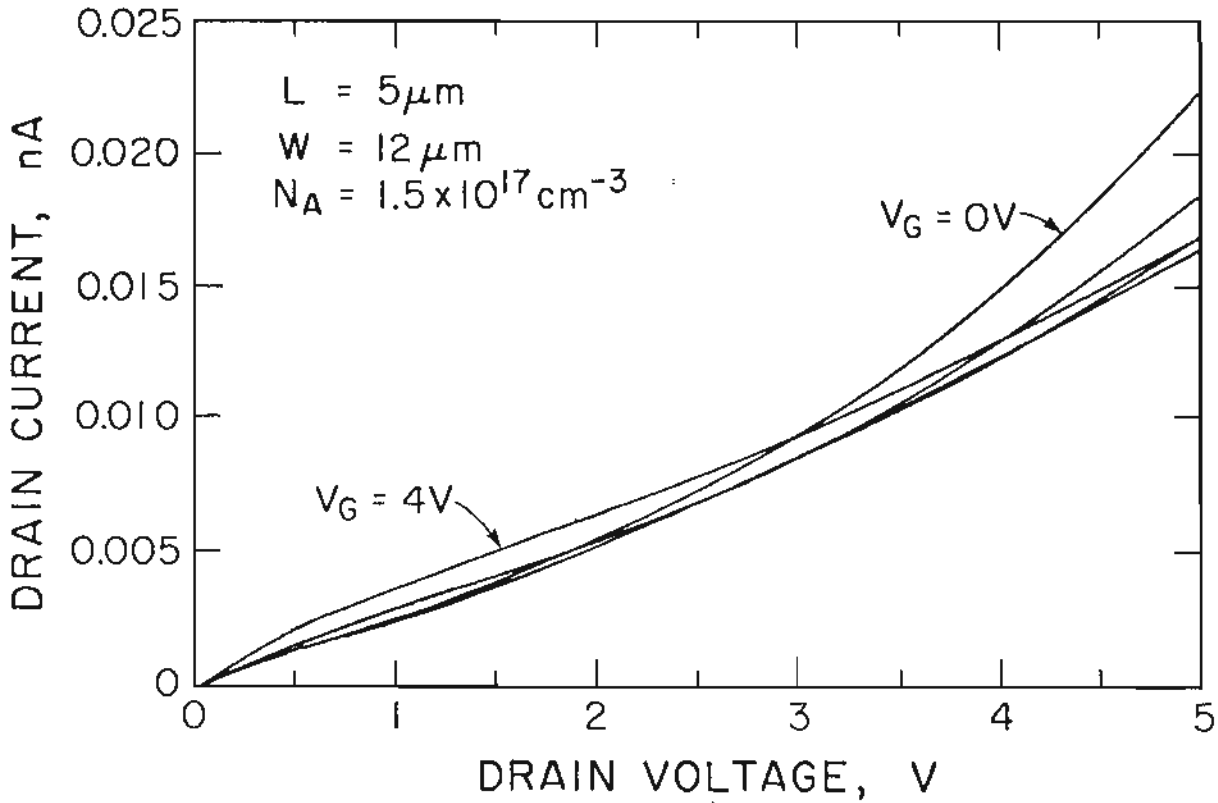

Figure 4-9 Drain characteristics with small gate voltages. The data was obtained from a 11 μm-long device of sample #1. Note that for a large drain voltage, the current decreases with increasing gate voltage.

4.4 Drive Current and Discussion

The drain current as a function of drain voltage at large gate voltage exhibits well-behaved transistor I-V characteristics as is shown in Figure 4-10. The drift-dominated current increases with V_D in the linear region and reaches saturation region in which current is almost a constant. With further increasing drain voltage, the current increases nonlinearly with V_D and exhibits a hot-carrier induced soft-breakdown. In short n-channel TFT's ($L = 5$ μm or less), this behavior can be observed at lower drain voltage. However, the p-channel devices have a better I_D-V_D characteristics, as shown in Figure 4-11. It appears that the hot-electrons near the drain-end are responsible for the current enhancement at large drain voltages. This enhancement is significant at small gate voltages (see Figure 4-9) and/or in shorter devices (see Figure 4-11), especially in n-channels.

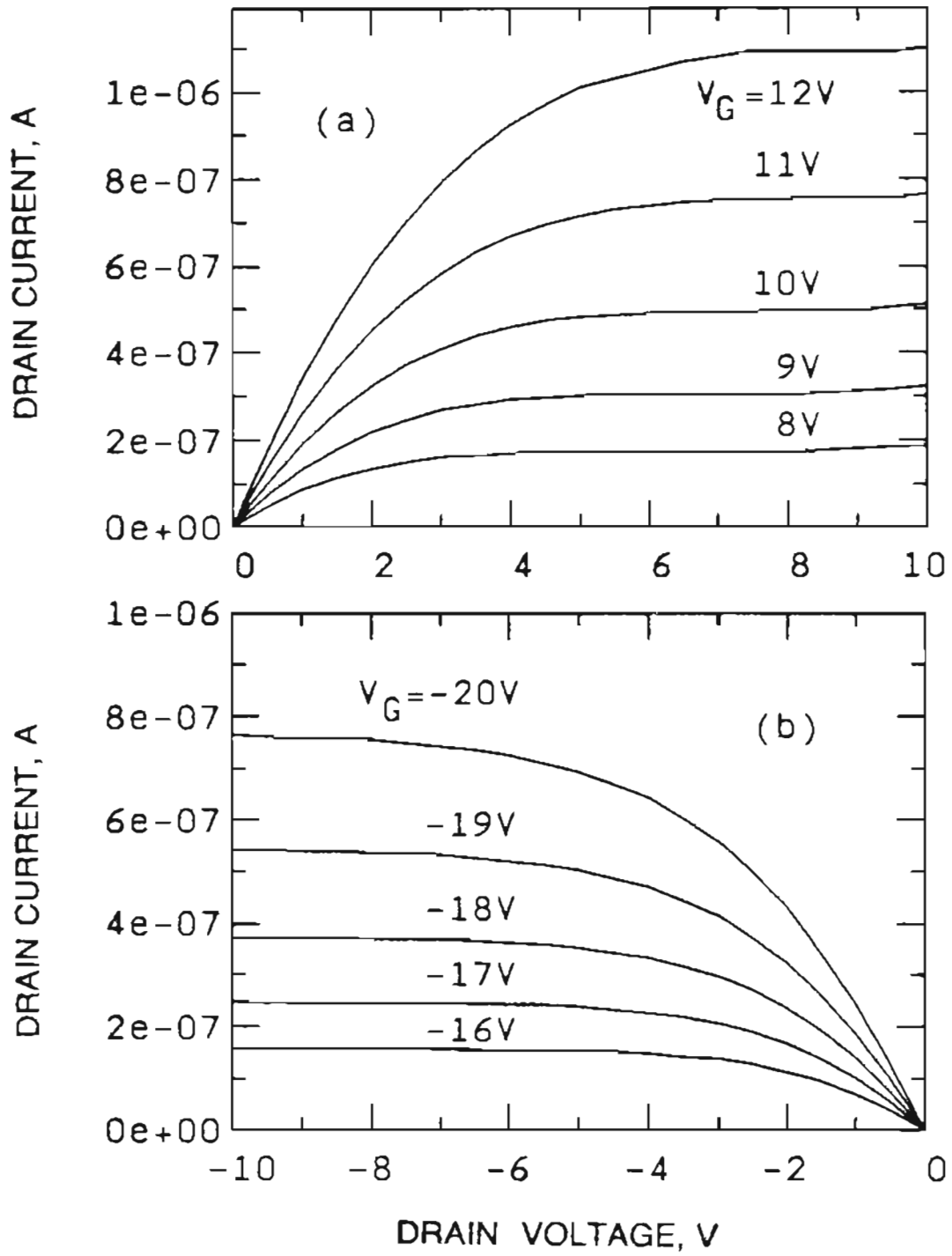

Figure 4-10 Drain characteristics of long (47 μm) channel TFT's. The data were obtained from sample #2 (a), n-channel, and sample #3 (b), p-channel.

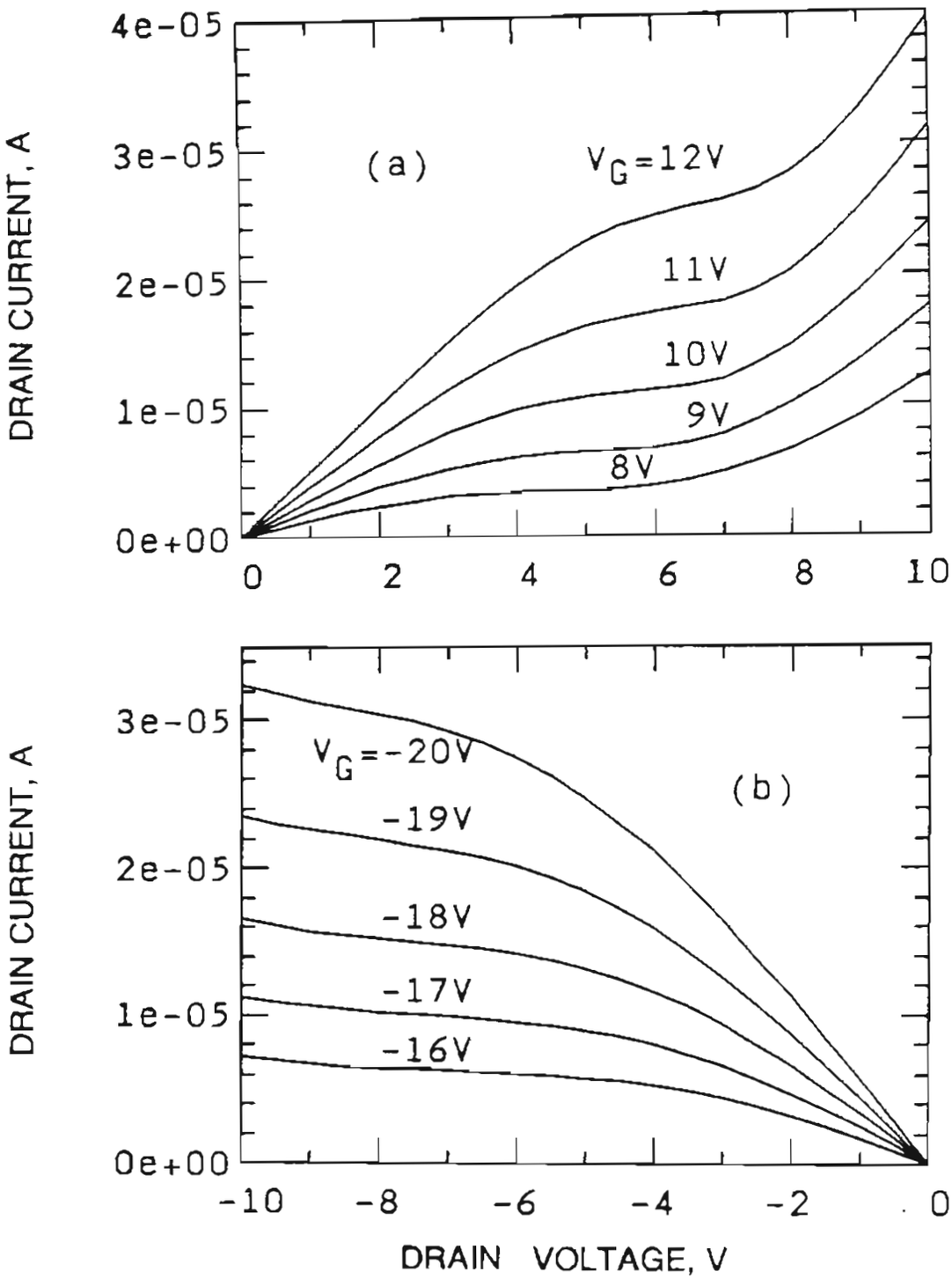

Figure 4-11 Drain characteristics of a short (3 μm) channel TFT. The hot-carrier induced drain current enhancement can be observed at large drain voltage range, and this effect is more pronounced in n-channel devices.

4.5 Gate Insulator Breakdown

The gate insulator breakdown is examined with sample #1 (with a measured gate oxide thickness of 36.7 nm) to test the dielectric strength. A positive gate voltage was applied in the absence of drain voltage. The oxide breakdown is evidenced in the gate voltage range between 21.5 and 27.5 V. The pre-break current was typically a few tenths of a microampere. 100 devices were tested and no channel length dependence of the breakdown voltage was observed in the experiment. The breakdown voltage distribution is plotted in Figure 4-12. with an average value of 25.4 V. The corresponding gate field strength at breakdown is about 7×10^6 V/cm*. This is a satisfactory result for polysilicon oxide.

* The silicon oxide breakdown field is about 10^7 V/cm, see reference[4].

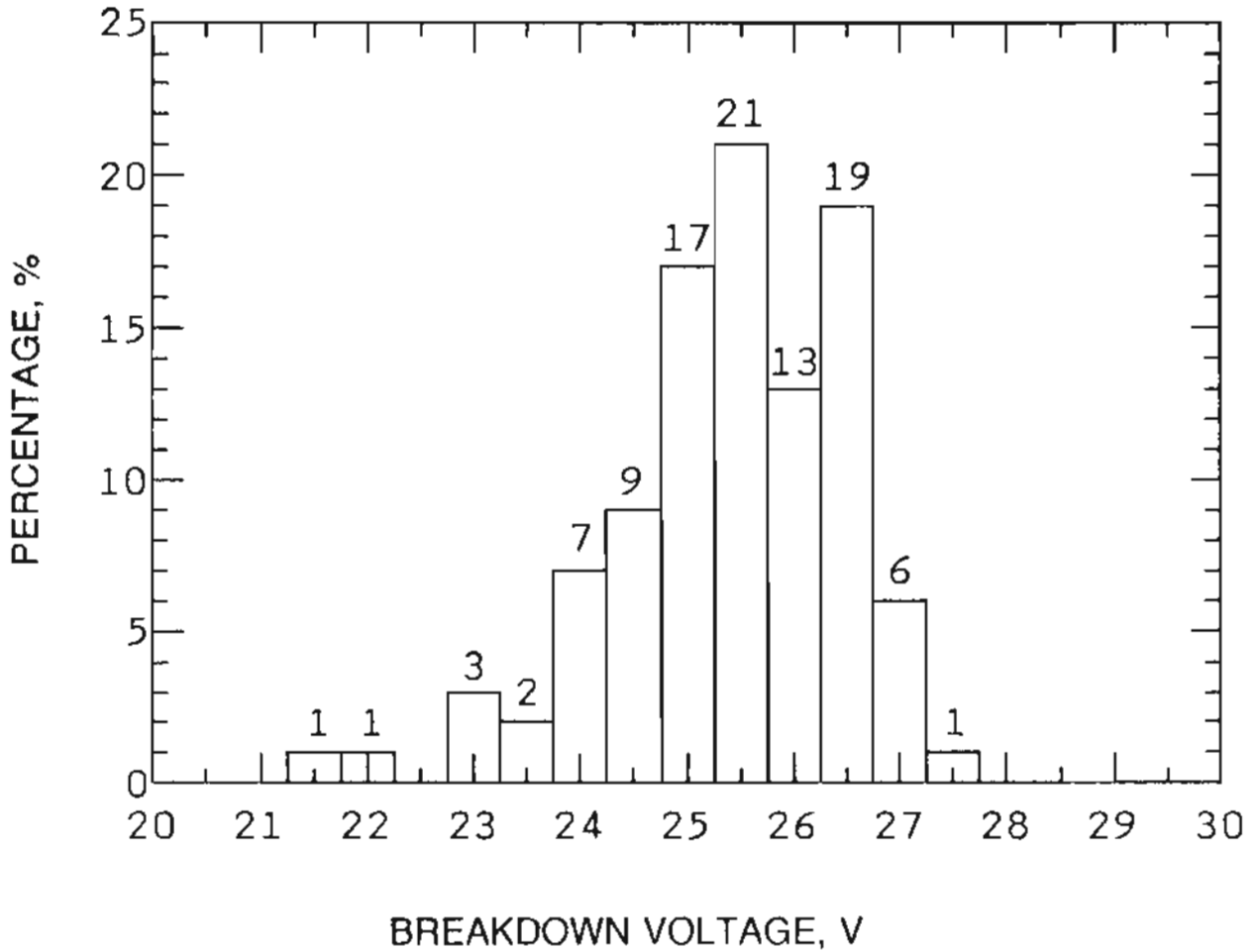

Figure 4-12 Gate oxide breakdown voltage distribution. The average breakdown voltage is 25.4 V. The corresponding breakdown field is 7×10^6 V/cm, with a gate oxide measured to be 36.7 nm-thick.

4.6 Threshold Voltage and Channel Mobility

Conventionally, by measuring the drain current in the saturation region (I_{DS}), the threshold voltage (V_T)and channel mobility (μ_{ch}) may be extracted by plotting $\sqrt{I_{DS}}$ versus V_G. A constant threshold voltage can be found from the intercept and channel mobility from the slope[4]. But, it is difficult to find these parameters in polysilicon TFT's from the experimental data, since both μ_{ch} and V_T in this case vary with the gate and/or drain voltage. The square root of saturated drain current is plotted versus gate voltage in Figure 4-13. With the conventional method, the threshold and mobility values thus obtained are listed in Table 4-1. The higher threshold voltage and lower channel mobility, together with a larger leakage level, typically describe the properties of the polycrystalline TFT's, compared with single crystalline MOSFET's.

Table 4-1

Parameters	Sample					Unit
	#1	#2	#3	#4	#5	
Channel mobility	0.1	7	11.5	10.5	1.8	$cm^2/V \cdot s$
Threshold voltage	11.2	5	−12	2	−4	V

Table 4-1 Parameters were extracted from samples #1, 2 and 3 (W=12μm, L=11μm), and from samples #4 and 5 (W=50μm, L=50μm), with corresponding gate insulator thickness given in Table 3-1.

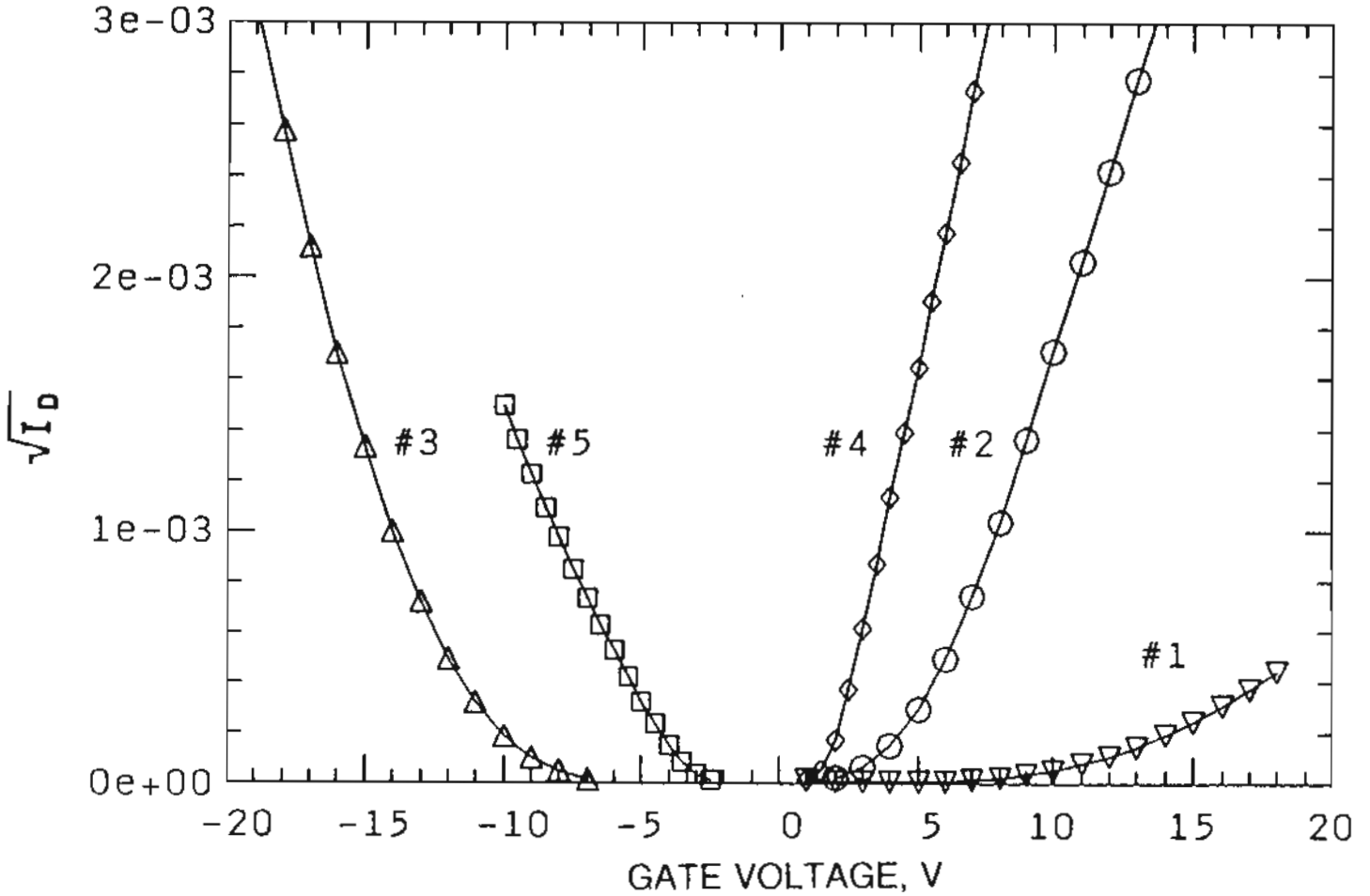

Figure 4-13 The square root of saturated drain current versus gate voltage. The extracted threshold voltage and channel mobilities are listed in Table 4-1, from the intercepts and slopes, respectively. This extraction is not accurate for polysilicon TFTs as will be explained in next charpter.

4.7 Effect of Grain Boundary Passivation

The large density of grain boundary trap sites are primarily resulting from the dangling bonds in interfaces of grains with different crystal orientations. By passivation, the hydrogen atoms are introduced into grain boundaries and the number of dangling bonds are reduced. Those devices passivated by H^+-implantation were characterized and the improved I-V behavior is presented in Figures 4-14 and 4-15. It can be clearly observed from these figures, by comparing with the data from unpassivated devices, that

(i) The threshold voltage is shifted to negative positive) gate voltage for n-channel (p-channel) devices. The effect is similar to the case of a large amount of donor (acceptor) impurity atoms being implanted into a p-type (n-type) substrate.

(ii) The ON current level is improved to a higher level, which implies that the channel mobility is increased due to passivation.

(iii) The leakage level appears to be lowered after passivation. This shows that hydrogen passivation also improve the leaky junction behavior, by effectively reducing the trap density in grain boundaries.

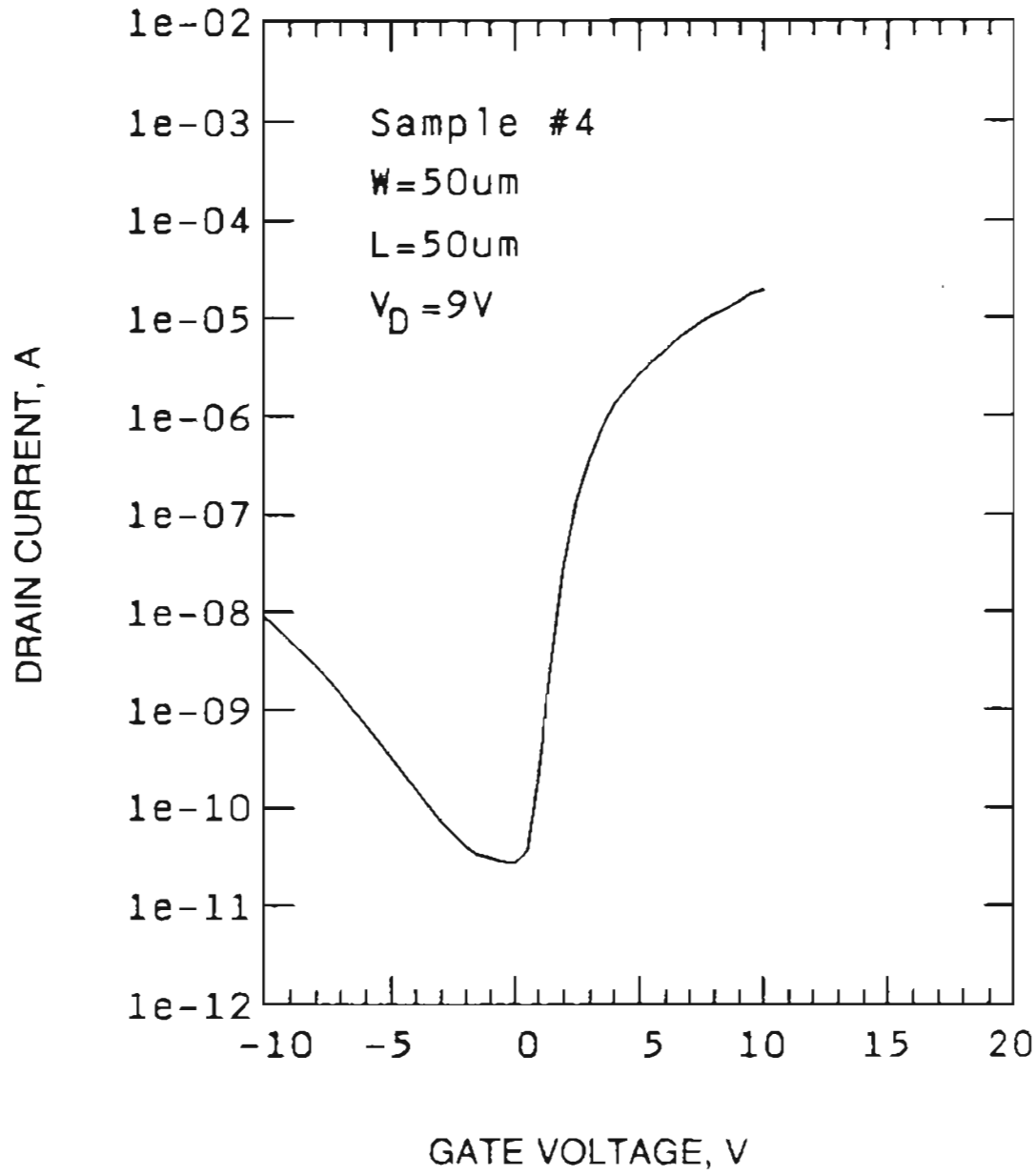

Figure 4-14 Transconductance I_D-V_G data from passivated (H^+-implanted) n-channel TFT's (sample #4).

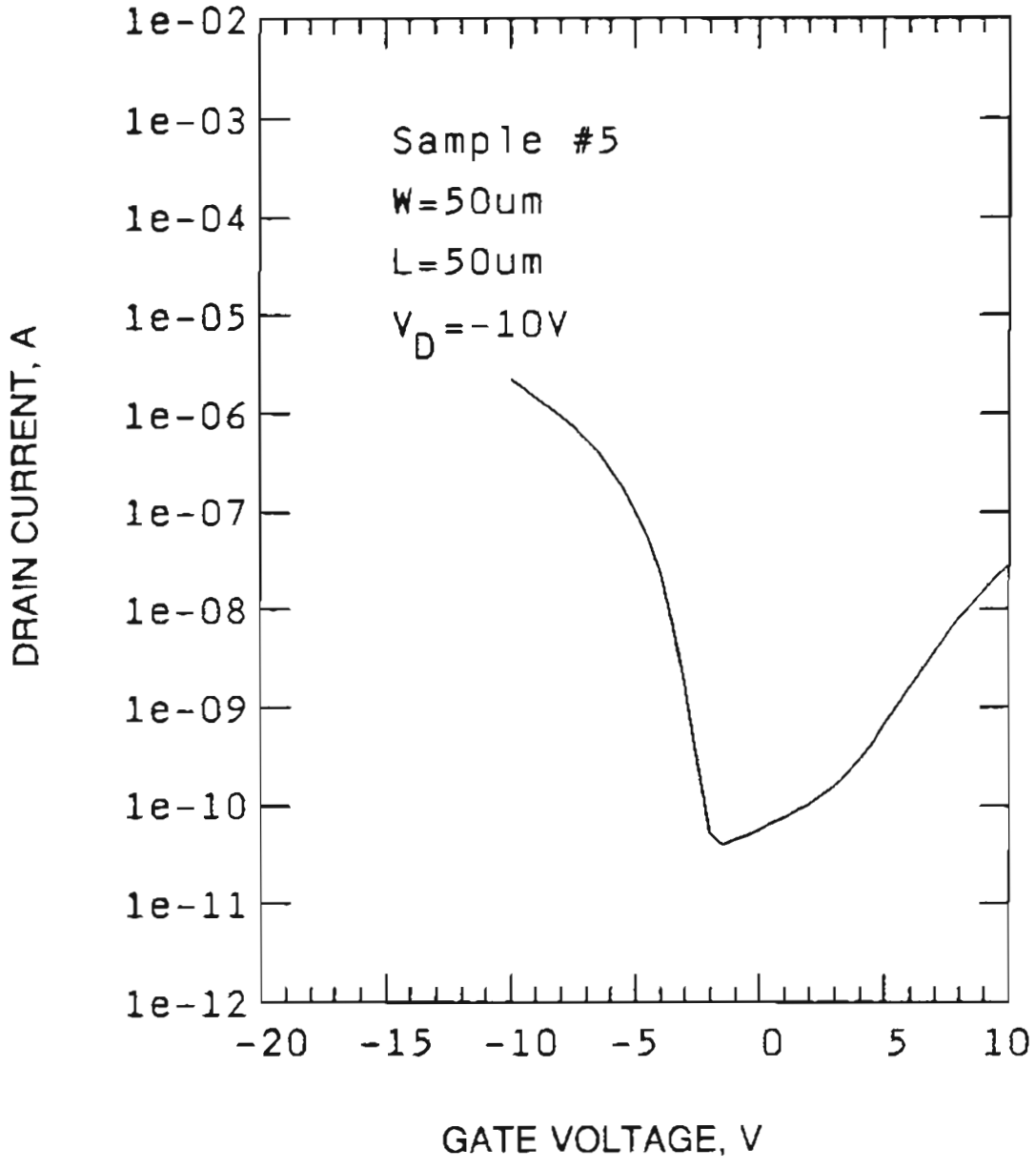

Figure 4-15 Transconductance I_D-V_G data from passivated (H^+-implanted) p-channel TFT's (sample #5).

4.8 Results from C-V Measurement

In the test structure for C-V measurement, the high resistance of the lower (active) polysilicon layer resulted in large, distributed RC time delays which made a conventional high frequency capacitance measurement impossible. This problem was circumvented by performing the C-V measurement, using a quasi-static technique[5]. The test structure had an area of 4×10^4 μm^2 and a capacitance of approximately 70 pF. The resulting C-V curves were independent of ramp direction or ramp rates less than 0.1 V/s. The latter indicates that RC time delays were no longer a problem. To maximize the sensitivity and resolution, final C-V measurements were performed with a ramp rate of 0.1 V/s.

The measured C-V curves for undoped, n-doped and p-doped samples are shown in Figure 4-16. The data were obtained from a 4×10^4 μm^2 structure. The observed maximum capacitance of approximately 70 pF is consistent with the known 20 nm dielectric thickness. In all samples, the minimum capacitance observed, approximately 52 pF, occurred near zero gate bias. Note that the three curves are almost identical and independent of doping and type. This anomalous behavior will be explained in the next chapter.

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CHAPTER 5

MODELING OF THIN FILM TRANSISTORS

5.1 Introduction

The starting polysilicon thin film considered in this work is limited to undoped and/or p-type doped with a doping concentration below the critical value ($N_A < N^*$). Hence, polysilicon grains are depleted of mobile carriers at equilibrium and there is a band bending resulting from the potential barrier, V_B.

The Poisson equation for channel inversion or accumulation constitutes one of the key issues in modeling TFT's. The major complication in the analysis arises from the presence of barrier potential. But, a question to be raised is, is it possible to incorporate the role of barrier potential in a simple tractable manner?

Due to the presence of grain boundary trap sites in polycrystalline materials which results in grain boundary barrier potentials, the analysis of the electrostatics in polysilicon TFT's is more complicated than that of bulk devices. In polysilicon TFT's, the associated Poisson equation is three-dimensional. A

number of researchers have analyzed the problem both numerically and analytically[1-8] and some insights have begun to emerge. Depp *et al*[1] numerically analyzed the electrostatics in the film, by using a distributed trap model and achieved quite satisfactory results. For example, Anwar and Khondker[7] have recently performed systematic numerical analysis of the channel barrier potential and the corresponding mobility as a function of gate voltage in polysilicon n-channel MOSFET's and showed that, (i) with the increasing gate voltage, the barrier potential is reduced to an insignificant level ($V_B < k_B T$) and (ii) the channel mobility levels off at the maximum value attainable for given set of process parameters. Both barrier potential and channel mobility change dynamically under gate bias mainly in the range of small gate voltage. Other investigators have also reported the similar results[3,6].

TFT's usually exhibit a large leakage current, presumably resulting from the soft breakdown of the junction or from enhanced generation/recombination processes via grain boundary trap sites[6]. The large leakage current level makes it difficult to observe experimentally the V_G-induced dynamic change in channel mobilities[6,7]. Improved device performance is sought from grain boundary hydrogenation[9,10] and/or laser recrystalization[11,12] both of which are thought to greatly reduce the trap density. The present work is primarily focused on small grain ($L_g \leq 100$ nm) and grain boundary passivated TFT's with low or moderate channel doping ($N_A < N^*$). All of these efforts may reduce the grain boundary barrier potential to a small

value.

5.2 Electrostatics analysis

First consider an n-channel device. The channel conduction (excluding that in the leakage regime) is provided by the V_G-induced minority carriers near the surface. This inversion charge layer is separated from the bulk by a space-charge region. As the inversion sets in, the Fermi level moves up across the midgap near the surface. The trapped holes are released from the grain boundary while electron trap sites are filled. With electrons replacing holes in grain boundary trap sites, there is no source or sink of field lines along the channel to support the grain boundary barrier potential. For gate voltages greater than the flat band voltage (V_{FB}) by a few $k_B T/q$, the barrier potential is practically nonexistent near the surface[8]. In this model, at the onset of inversion and beyond (electrons replacing holes in grain boundaries at the surface, which requires $V_G \geq V_{FB} + \mathcal{O}(0.3\ \mathrm{V})$), the barrier potential is taken to be zero to the first order of approximation. For small gate voltage (leakage regime) the barrier potential is still preserved and plays an important role in determining the leakage behavior of the device.

The polysilicon thin films are modeled to consist of columnar grains of identical size L_g, rising up from the substrate (see Figure 5-1). The grain boundaries run perpendicular or parallel to the channel. The positive x-direction is chosen from the surface to bulk and the positive y-direction from

the source to drain. In the presence of gate voltage, the resulting fixed charge in the space-charge region ($x < a$) illustrated in Figure 5-2(a) now consists of uncompensated acceptor ions in grains and charge sheets of trapped electrons in grain boundaries which are separated by a distance of grain size L_g. Both of them are equally important in determining the surface band bending.

A concept of "effective doping concentration", N_{eff} is introduced here[1] to represent the fixed space-charge density averaged over the unit element of polysilicon thin film:

$$N^n_{eff} = N_A - 2Q_t/L_g \tag{5.1}$$

with a superscript n representing the case of n-channel. The factor of 2 is introduced by considering columnar grains in the film. At the onset of inversion and beyond ($E_F > E_i$), Q_t is mainly contributed by trapped electrons. Assuming that all electron trap sites for $E_F > E_i$ are filled due to the band bending, the electron charge sheet density is approximately given by

$$Q_t = -Q^n_T \qquad (E_F > E_i). \tag{5.2}$$

Hence,

$$N^n_{eff} = N_A + 2N^n_T/L_g \qquad (0 \leq x \leq a). \tag{5.3}$$

The second term, given in terms of the grain boundary trap density of electrons (N^n_T) and the average grain size (L_g), is the additional fixed volume space-charge density near the surface; a is the location where $E_F = E_i$ (see Fig-

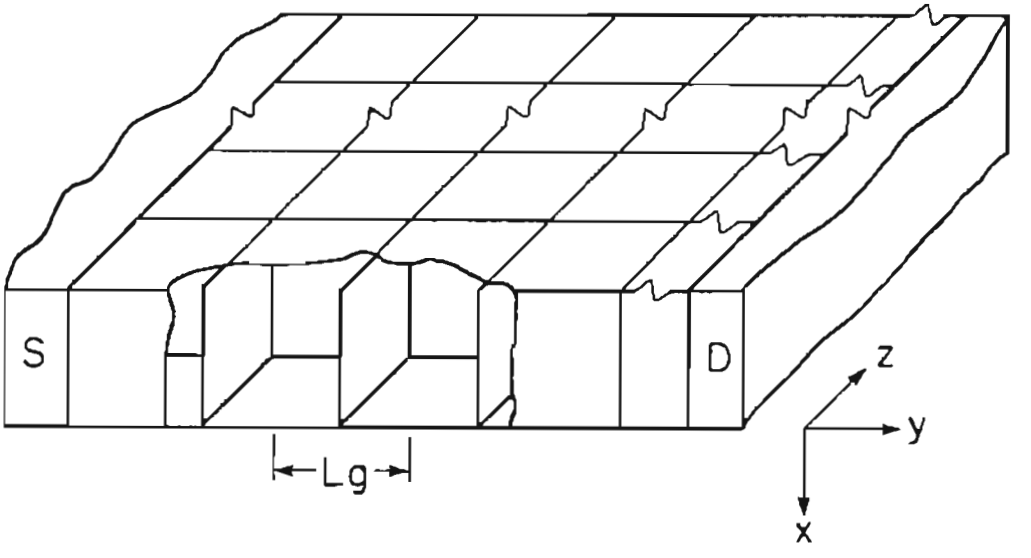

Figure 5-1 Cross sectional view of the polysilicon TFT channel consisting of columnar grains with an average grain size L_g and a height of film thickness t_f.

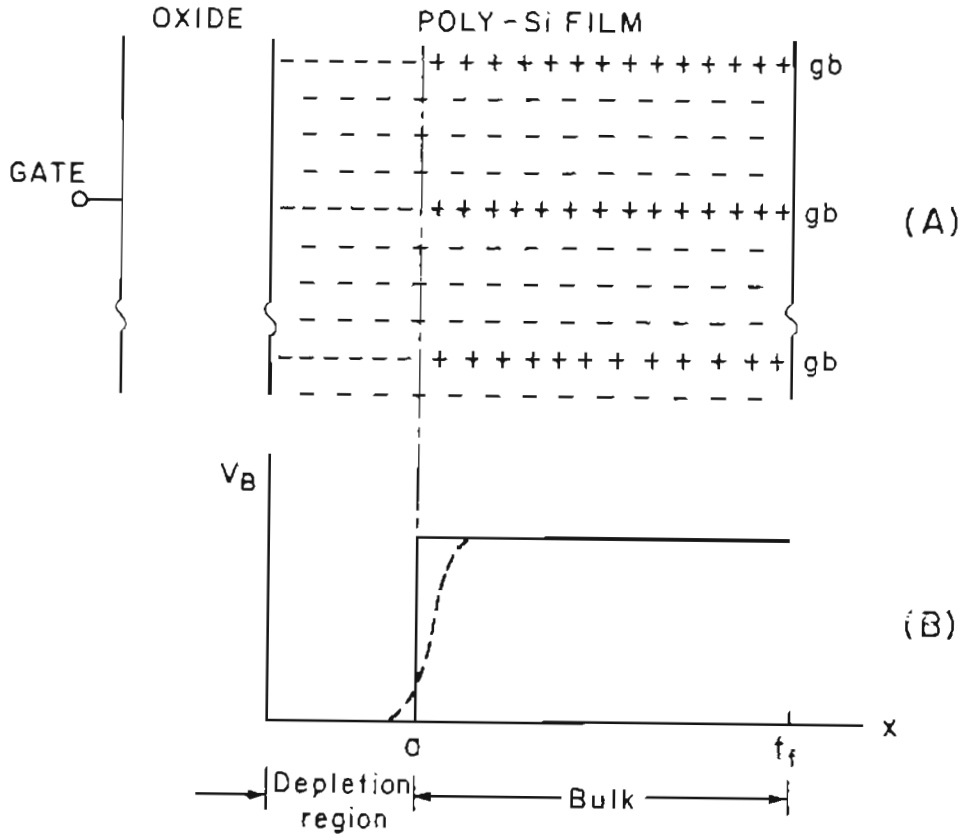

Figure 5-2 (a) Fixed space-charge configuration in n-channels under a gate bias with gb's denoting grain boundaries. (b) Corresponding grain boundary barrier potential V_B as a function of film depth. The dashed and solid line represent the actual V_B profile and the approximation made in this model.

ure 5-2(b)).

Similarly in p-channel devices, as the band bends up under a gate bias ($V_G < 0$), the grain boundary trap sites near the surface are filled with accumulated holes. The corresponding fixed charge sheets are likewise converted into a volume charge density and the effective doping is given by

$$N^p_{eff} = N_A - 2N^p_T/L_g \qquad (0 \leq x \leq b) \tag{5.4}$$

where superscript p is for p-channel case and b represents the position where the hole trap sites are filled and approximately indicates the edge of the space-charge region (see Figure 5-3). The excess mobile holes accumulated in the region $x < b$ together with N^p_{eff} are responsible for the surface band bending and shield gate field lines. The primary role of the trapped holes in providing the dominant component of the space-charge is same as that of trapped electrons in n-channel devices.

Neglecting the barrier potential, the associated Poisson equation is reduced to a 1-D problem,

$$\frac{d^2\phi^j(x)}{dx^2} = \frac{q}{\epsilon_s}(N^j_{eff} - p + n) \qquad (j = n, p) \tag{5.5}$$

Here, the effective doping, N^n_{eff}, N^p_{eff} are given by (5.1) and (5.3); p, n are the hole and electron concentrations, respectively.

The essential features of 1-D electrostatics are summarized in Figure 5-3. In the bulk film ($x > a$ for n-channel and $x > b$ for p-channel) the dopant ions are compensated by trapped holes in grain boundaries and to a lesser

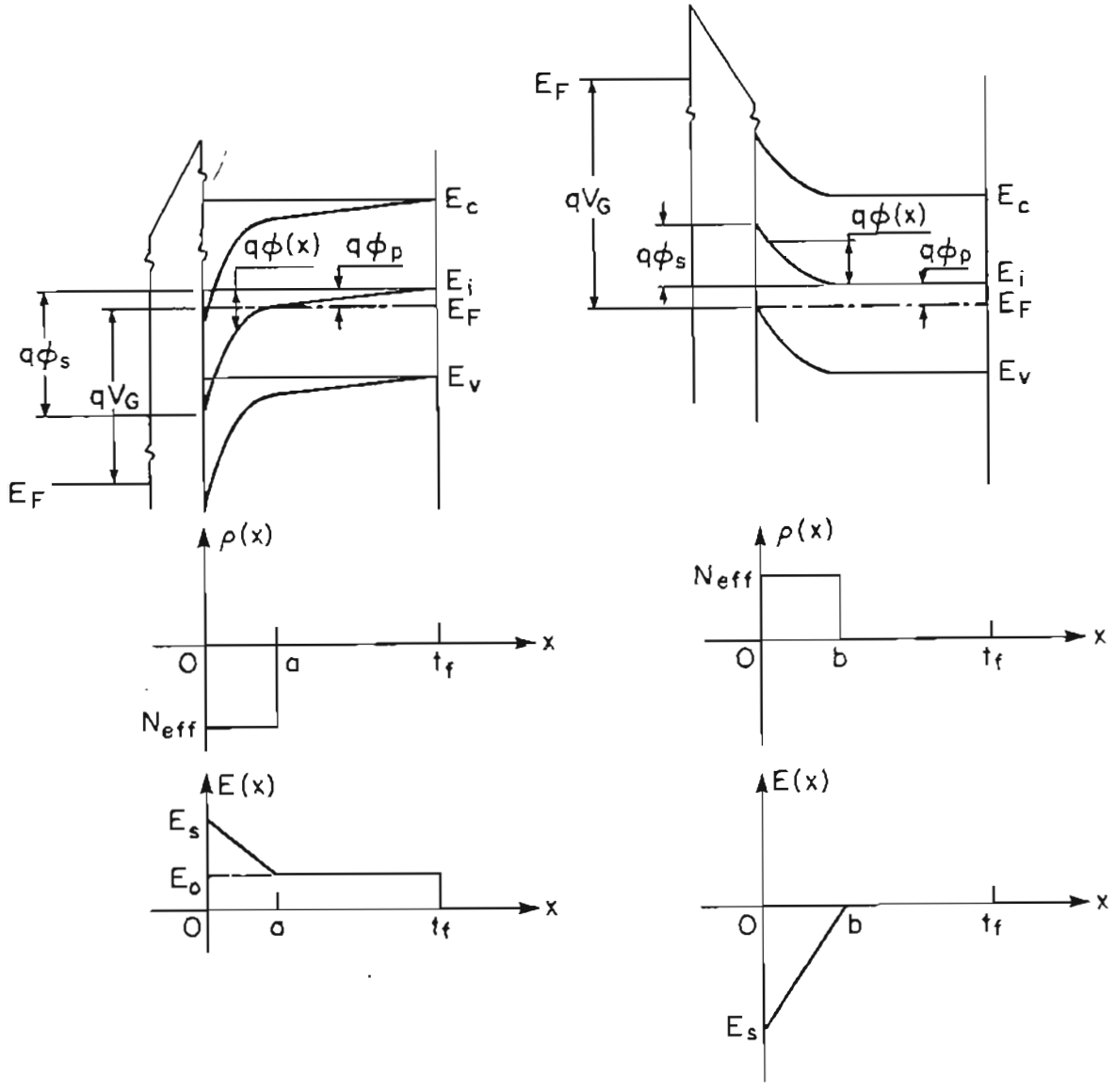

Figure 5-3 The surface band bending, fixed space-charge configuration and electric field, (a) for n-channel with a positive gate voltage and (b) for p-channel with a negative gate voltage.

extent by mobile holes in the grains and there is an overall charge neutrality prevaling. In the space-charge region ($x < a$ for n-channel and $x < b$ for p-channel) the fixed space-charge density is primarily contributed by the trapped electrons/holes.

The 1-D Poisson equation (5.5) can be treated in the usual manner. The first integration relates surface field of n- and p-channels to the respective surface potential as

$$(E_s^n)^2 = \frac{2q}{\epsilon_s}\left\{\frac{n_i}{\beta}[\exp-\beta(\phi_s^n-\phi_p)+\exp\beta(\phi_s^n-\phi_p)-2] + N_{eff}^n(\phi_s^n-\phi_p)\right\}+[\phi_p/(t_f-a)]^2 \tag{5.6a}$$

$$(E_s^p)^2 = \frac{2q}{\epsilon_s}\left\{N_{eff}^p\phi_s^p+(n_i/\beta)[e^{\beta\phi_p}(e^{-\beta\phi_s^p}-1)+e^{-\beta\phi_p}(e^{\beta\phi_s^p}-1)]\right\} \tag{5.6b}$$

where $\phi_p = E_i - E_F$ is the Fermi level at equilibrium, t_f the film thickness and ϕ_s the surface potential. The superscripts n and p stand for n- and p-channel devices, respectively. ϕ_s^n and ϕ_s^p are implicitly given by the depletion depth a and b (see Figure 5-3) as

$$\phi_s^n = \phi_p t_f/(t_f-a)+qN_{eff}^n a^2/2\epsilon_s \tag{5.7a}$$

$$\phi_s^p = qN_{eff}^p b^2/2\epsilon_s \tag{5.7b}$$

With the surface potentials related to the surface fields, the gate voltage is divided between the oxide and polysilicon thin film as

$$V_G^j = E_s^j \epsilon_s / C_{ox} + \phi_s^j + V_{FB}^j \qquad (j = n, p) \tag{5.8}$$

where C_{ox} is the gate capacitance per unit area and

$$V_{FB}^j = \phi_{ms}^j - qN_{ss}/C_{ox} \qquad (j = n, p) \tag{5.9}$$

is the flat band voltage, ϕ_{ms}^j the work function difference and N_{ss} the surface state density.

5.3 Channel Mobility

The quantitative description of the channel mobility in polysilicon TFT's constitutes a key problem in modeling the performance of the devices. The measured channel mobility in polysilicon TFT's is smaller than the corresponding value in bulk silicon devices, often by several orders of magnitude. The improved device performance should therefore depend on maximizing the mobility via the optimal choice of process conditions. This in turn, requires a clear physical understanding of various factors affecting the mobility.

The channel mobility in n-channel TFT's is that of minority carriers. When the channel is inverted, the grain boundary barrier potential becomes insignificant and (from now on) does not affect the channel mobility.

The mobility in the conduction channel for TFT's is analyzed in this work, based upon a distributed resistivity model, which was proposed recently by Kim *et al*[13]. With barrier potential V_B taken to be zero in the conduction

channel, the mobility therein would take the form of Eq. (2.19). The electron mobility (in n-channel) and hole mobility (in p-channel) are explicitly given by

$$\mu^n = \mu_c^n/[1+(\delta/L_g)(\mu_c^n/\mu_{gb}^n)(n_c/n_{gb})] \ . \tag{5.10a}$$

$$\mu^p = \mu_c^p/[1+(\delta/L_g)(\mu_c^p/\mu_{gb}^p)(p_c/p_{gb})] \tag{5.10b}$$

where n_c/p_c and μ_c^n/μ_{gb}^p is the electron/hole concentration and the electron/hole mobility in crystalline grains, respectively, μ_{gb}^n/μ_{gb}^p the electron/hole extended state mobility in grain boundaries, n_{gb}/p_{gb} the electron/hole concentration beyond the mobility shoulder[14] in grain boundaries, and δ the width of grain boundary.

Furthermore, the carriers in the channel undergo additional surface scattering. This is incorporated phenomenologically by introducing an attenuation factor η to describe the channel mobility. Thus,

$$\mu_{ch}^j = \eta\mu^j. \tag{5.11}$$

The value of η is very dynamic and sensitive to the process conditions[6].

In polysilicon the carrier mobility is characterized by phonon and impurity scattering in grains (μ_c) and Brownian diffusive motion in grain boundaries (μ_{gb}). The effective mobility value can, therefore, range from μ_{gb} ($\sim$ 1 cm^2/V sec) to crystalline value of μ_c, depending on the weighting factors involved.

The fact that the surface potential ϕ_s in TFT's varies with gate voltage

gives rise to a gate voltage dependence of the channel mobility. This is due to the dependence of n_c/n_{gb} in n-channel or p_c/p_{gb} in p-channel devices on gate voltage (see (5.10)), since these concentrations are functions of surface potential controlled by gate voltage.

5.4 Drain Current

First consider n-channel devices. When a positive voltage (V_G) is applied to the gate (with source grounded, i.e. $V_S = 0$), an inversion layer is induced at the polysilicon-oxide interface. Assuming that a small voltage (V_D) is applied to the drain, a current will flow through the conduction channel. The drain current is then determined by the channel resistance and is proportional to the small drain voltage. This is the linear region. When drain voltage increases, the drain current becomes sublinear and eventually reaches a pinch-off point beyond which the drain current remains essentially a constant. This is the saturation region. All of these I-V behaviors are similar to those in bulk silicon MOSFET's. Therefore, the quantitative expression for the drift current can be derived in a manner entirely analogous to conventional MOSFET's.

A few assumptions are made: (i) a flat band voltage (V_{FB}) exists which results from the work function difference between gate and channel, and oxide trapped charges, (ii) long channel and small grain size so that N_{eff} can be regarded as uniform over the channel, (iii) large gate voltage and small drain

voltage, that is, the transverse field in x-direction is much larger than the longitudinal field in y-direction. This is the gradual channel approximation.

The application of a drain voltage gives rise to the channel voltage (V_{ch}) which is distributed along the channel and varies as a function of location (y), with $V_{ch}(0) = V_S = 0$ and $V_{ch}(L) = V_D$. The surface charge per unit area after strong inversion consists of both fixed and mobile carriers

$$Q_s(y) = Q_{fix}(y) + Q_{mob}(y). \tag{5.12}$$

The fixed charge is contributed by N^n_{eff} in the region $x < a$

$$Q_{fix}(y) = -qN^n_{eff}\,a \approx -\sqrt{2qN^n_{eff}\epsilon_s|\phi_s + V_{ch}(y)|} \tag{5.13}$$

From the charge neutrality condition, this surface charge density should be equal to that on the gate (Q_{gate}) which is given by

$$Q_{gate}(y) = [V_G - V_{FB} - V_{ch}(y) - \phi_s]C_{ox}. \tag{5.14}$$

With (5.12), (5.13) and (5.14), the surface mobile charge density over a unit area is found to be

$$Q_{mob}(y) = -[V_G - V_{FB} - V_{ch}(y) - \phi_s| + \sqrt{2qN^n_{eff}\epsilon_s|\phi_s + V_{ch}(y)|} \tag{5.15}$$

The resistance element in the channel can be specified by

$$dR = \frac{dy}{q\mu(y)n(y)\cdot Wt} = \frac{dy}{\mu(y)Q_{mob}W} \tag{5.16}$$

with t being channel thickness and $qn(y)\cdot t = Q_{mob}(y)$. The voltage drop across this element is

$$dV = I_D \cdot dR = \frac{I_D\, dy}{W\mu(y)\mid Q_{mob}(y)\mid}, \tag{5.17}$$

where I_D is independent of y.

The similar analysis is also applied to the p-channel case in which the mobile carriers are accumulated holes. The integration

$$\int_0^L I_D\, dy = \int_0^{V_D} W\mu(y)\mid Q_{mob}(y)\mid dV \tag{5.18}$$

with $\mid Q_{mob}\mid$ in (5.15) yields a unified current expression applicable to both n- and p-channel devices:

$$I_{dr}^j = \frac{W}{L}\mu_{ch}^j C_{ox}\left\{(V_G - V_{FB}^j - \phi_s^j - \frac{1}{2}V_D)V_D \right. \tag{5.19}$$

$$\left. - \frac{2}{3}\cdot\frac{\sqrt{2q\epsilon_s \mid N_{eff}^j\mid}}{C_{ox}} \times \cdot[(\mid V_D \mid + \mid \phi_s^j \mid)^{3/2} - \mid \phi_s^j \mid^{3/2}]\right\} \qquad (j = n,\ p)$$

with $j = n/p$ representing that for n-/p-channels. It may be informative to rewrite the general expression by introducing a threshold voltage (V_T) for both cases:

$$I_{dr}^j = (\frac{W}{L})\mu_{ch}^j C_{ox}(V_G - V_T^j - \frac{1}{2}V_D)V_D \tag{5.20}$$

with

$$V_T^j = V_{FB}^j + \phi_s^j + \frac{2}{3}\cdot\frac{\sqrt{2q\epsilon_s \mid N_{eff}^j\mid}}{C_{ox}} \times \tag{5.21}$$

$$[(\mid V_D \mid + \mid \phi_s^j \mid)^{3/2} - \mid \phi_s^j \mid^{3/2}] \qquad (j = n, p)$$

At the onset of strong inversion, the surface potential is approximately

$$\mid \phi_s \mid = \mid \phi_B \mid \pm \phi_p \tag{5.22}$$

with

$$\phi_B = \frac{k_B T}{q} \cdot \ln \frac{\mid N_{eff}^j \mid}{n_i}$$

by Boltzmann approximation. Note that at small drain voltage, the threshold voltage is insensitive to the gate voltage. However, with a larger drain voltage, $\mid V_T^j \mid$ increases significantly with increasing $\mid V_G \mid$. This behavior originates specifically from the large value of N_{eff}^j.

In the subthreshold regime the gate voltage is low and the surface potential is not large enough to ensure a strong inversion and/or accumulation. The drain current then is the subthreshold current. This region connects the ON and OFF state of the transistor and is very important for device operation.

The drain current under weak inversion and/or accumulation is taken to be dominated by diffusion, as in conventional MOSFET's theory, resulting from the concentration gradient of inverted electrons in n-channel or accumulated holes in p-channel,

$$I_{diff}^j = \frac{W}{L} \mu_{ch}^j k_B T n_i t^j (1 - e^{-\beta \mid V_D \mid}) e^{\pm \beta(\phi_s^j - \phi_p)} \qquad (j = n, p) \tag{5.24}$$

where + is for n-channel and − for p-channel; $t^j = (\beta \mid E_s^j \mid)^{-1}$ are the mobile charge layer thicknesses[15]. This subthreshold current expression shows that the drain current in this region varies exponentially with ϕ_s. The V_G-dependence of the current is implicitly given by Eqs. (5.6), (5.7), (5.8) and (5.24). The subthreshold slope, $\partial \log I_D / \partial V_G$ thus calculated is often larger than that observed in the experiment. This suggests that with an increasing surface potential, more mobile carriers are getting trapped into grain boundaries and less current increase can be observed. In this case, a multi-trap level model might describe the device operation more precisely.

The theoretical results from the model described above are calculated, in an association with film properties, process parameters and few fitting parameters.

(i) The surface potentials as a function of the gate voltage are calculated and plotted in Figure 5-4. A large surface band bending can develop in p-channel devices as well as in n-channel MOSFET's. This in turn leads to a large subthreshold current ratio. The result is different from the previous model[6] and is a consequence of N_{eff}.

(ii) The threshold voltage in polysilicon TFT's changes appreciably with both gate and drain voltage, which is computed and shown in Figure 5-5 for both types of devices. For a small drain voltage, the threshold V_T is insensitive to the changing gate voltage. However, when a large drain voltage is applied, the magnitude of threshold $|V_T|$ increases substantially with increasing gate

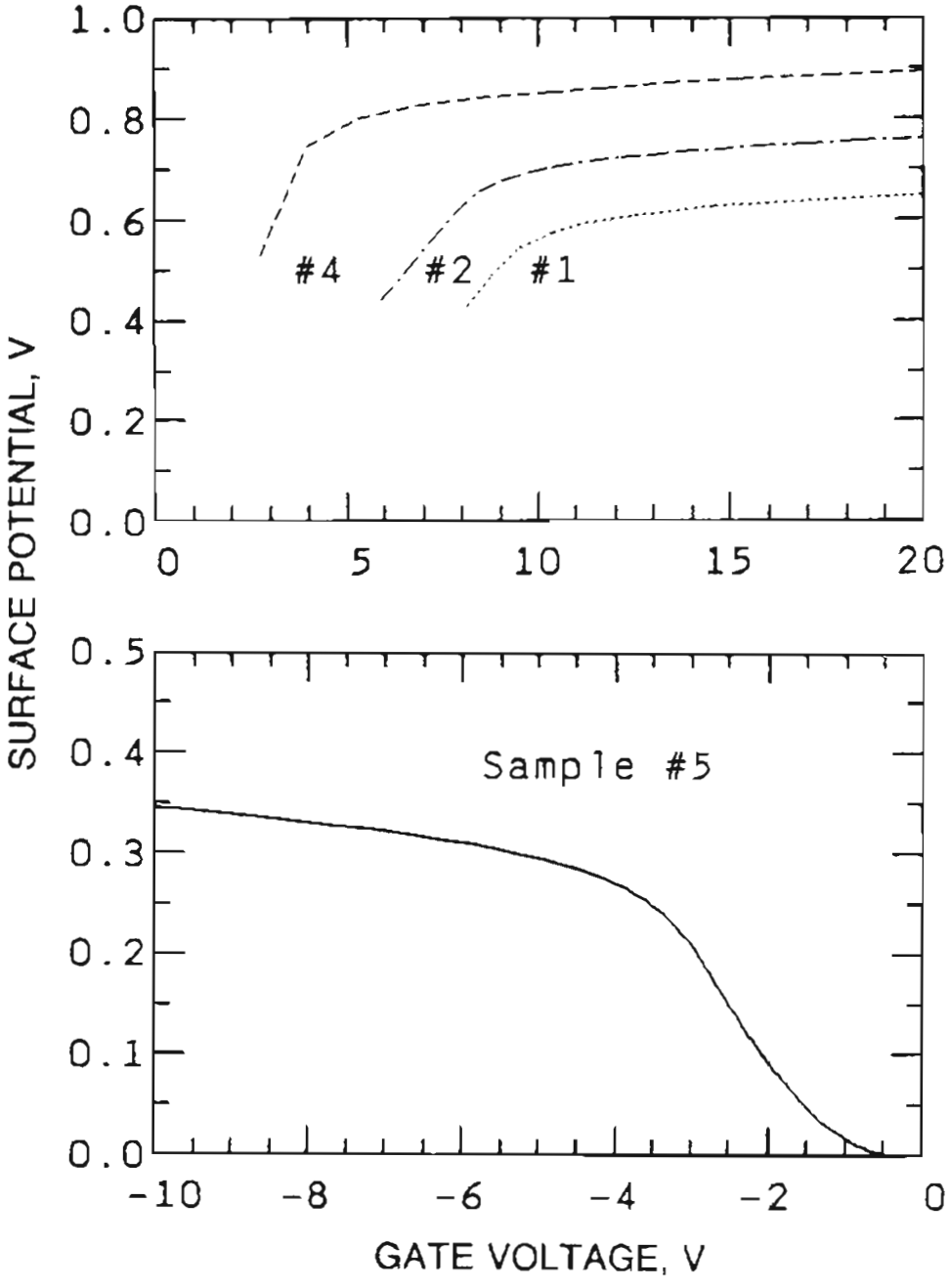

Figure 5-4 Calculated surface potential versus gate voltage, (a) for n-channels (sample #1, 2 and 4) and (b) for p-channel (sample #5). The parameters used are listed in Table 3-1 and 5-1.

voltage. This results in a reduced saturation current level.

(iii) Figure 5-6 presents the channel mobilities for both inverted electrons and accumulated holes as a function of V_G. These mobilities are shown to be slightly dependent of gate voltage at a value of $\sim$32 and $\sim$8 $cm^2/V \cdot s$ for electrons and holes, respectively. Since the threshold voltage cannot be approximated as a constant, a conventional procedure for extracting channel mobility can not be applied to these devices. In this theory, mobilities depend on gate voltage via the ratio of carrier concentrations in the grain and grain boundary. The two parameters significantly influencing the ratio are the barrier potential V_B and the position of the mobility shoulder (Δ')[14] from the conduction (n) or valence (p) band edge. Here, V_B is taken to be zero, and Δ' is assumed to be 0.015 eV for the n-channel and 0.046 eV for the p-channel. This results in a near-constant channel mobility over the gate voltage range examined. The channel mobility in unpassivated devices is often observed to be less than 1 $cm^2/V \cdot s$ and also depends significantly on gate voltage[16,17]. These tendencies are correlated with a larger value of Δ'. With grain boundary passivation the trap density is reduced and the trap level is shifted away from the mid-gap[18], and the grain boundary mobility shoulder also appears to be lowered, resulting in higher channel mobility.

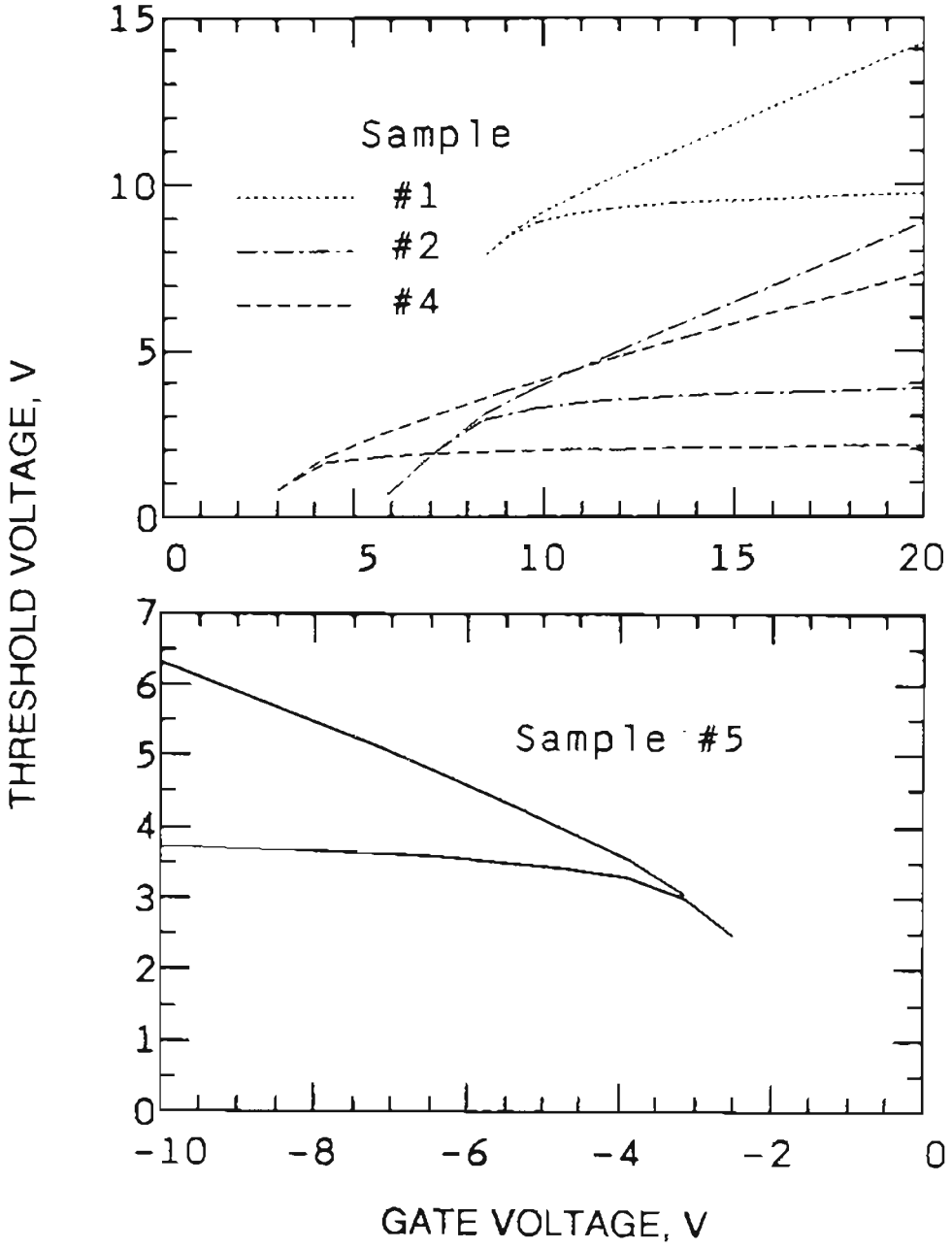

Figure 5-5 Calculated threshold voltage versus gate voltage, (a) for n-channel and (b) for p-channel. The lower branches are for small drain voltage ($V_D \simeq 0$V) and the upper branches for large (saturation) drain voltage. The parameters used are listed in Table 3-1 and 5-1.

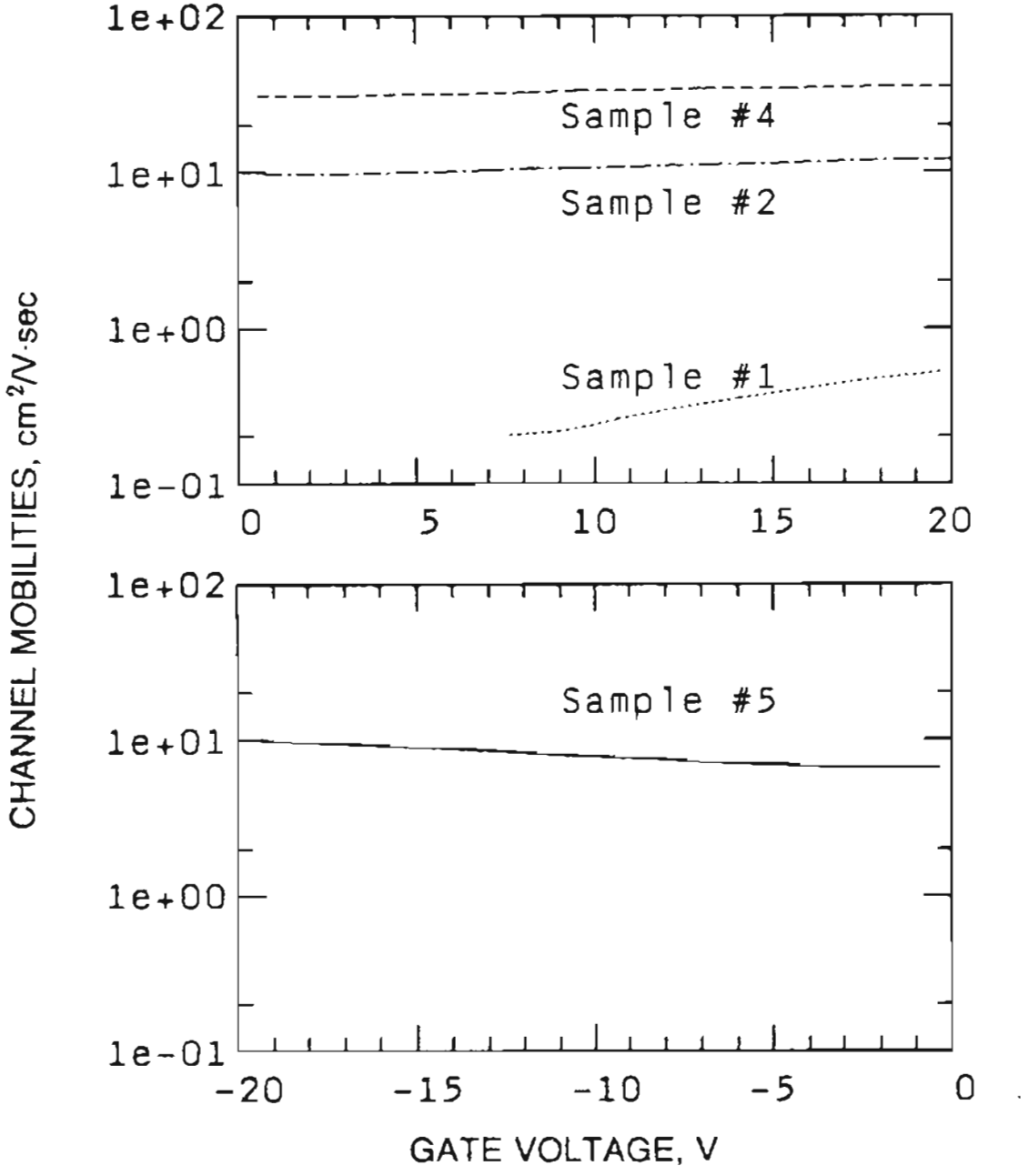

Figure 5-6 Calculated channel mobilities, (a) for n-channels (sample #1, 2 and 4) and (b) for p-channel (sample #5). The parameters used are listed in Table 3-1 and 5-1.

5.5 Operation in Undoped Channels

In the present analysis, the channel doping ($N_A < N^*$) does not critically influence the device performance. The large value of N_{eff} is mainly contributed by $2Q_T/L_g$ which plays the role of ionized dopant atoms in determining the electrostatics[1]. In fact, many working devices were fabricated in undoped polysilicon thin films[1,10]. The present model is still operative in undoped channels.

The "effective channel doping" in this case is simplified to be

$$N^j_{eff} = \pm 2N^j_T/L_g\,, \qquad (0 \le x \le a;\ j = n, p) \tag{5.25}$$

which yields a unified expression of surface field for both n- (+) and p-channel (−) devices:

$$E_s^2 = (2qn_i/\epsilon_s\beta)(e^{-\beta\phi^j_s} + e^{\beta\phi^j_s} - 2) + (2q/\epsilon_s)N^j_{eff}\phi^j_s, \tag{5.26}$$

where ϕ^j_s is given by the depletion depth a ($b = a$ in this case):

$$\phi^j_s = qN^j_{eff}a^2/2\epsilon_s \tag{5.27}$$

with $\phi^n_s > 0$ for n-channel and $\phi^p_s < 0$ for p-channel devices, respectively. The current expression in both subthreshold and drift region are same as (5.24) and (5.19).

A few comments are due at this point.

(i) In polysilicon TFT's, the presence of grain boundary trap sites results in large fixed space-charge densities. The device therefore behaves like a "heavily

doped" transistor in which the threshold voltage changes appreciably with both gate and drain biases.

(ii) The I-V behavior of both n- and p-channel TFT's has been shown to be described by the common formulation. This is a feature unique in polysilicon TFT's, and is a direct consequence of the presence of grain boundary trap sites. Specifically, the behavior of surface inversion or accumulation under gate bias is same. This point is illustrated in Figure 5-7 where the surface space-charge densities are plotted as a function of surface potential ϕ_s. Indeed, the electron inversion and hole accumulation near the surface exhibit similar functional dependence on surface band bending. This is in marked contrast with the accumulation of majority carriers in bulk silicon devices.

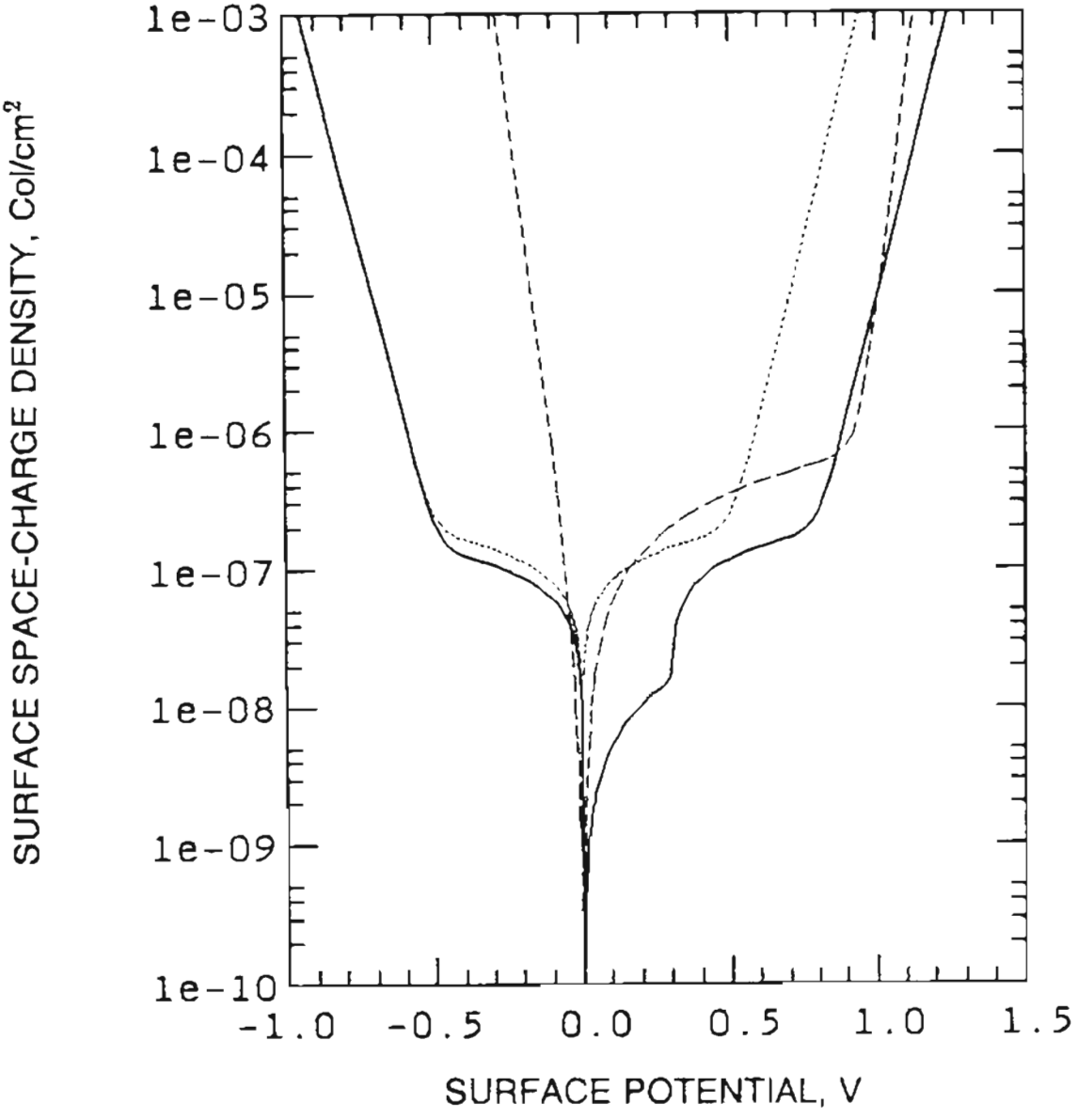

Figure 5-7 Calculated surface space-charge density per unit area versus surface potential, with $\phi_s > 0$ for n-channel and $\phi_s < 0$ for p-channel. The solid lines are for p-doped (N_A) and the dotted lines for undoped polysilicon channels. The dashed lines are for single crystal silicon case with a doping concentration of N_{eff}.

5.6 Comparison with Experimental Data

The theoretical I-V characteristics was computed using all the process parameters except the effective doping concentration and the channel mobility. To determine those two quantities, a few fitting parameters were used: the density of trap states Q_T, average grain size L_g, width of grain boundary δ, the mobility shoulder and surface scattering coefficient η.

Figures 5-8 through 5-10 show the plots of the transconductance I_D-V_G characteristics as predicted by this work with the corresponding experimental data points plotted in these figures with circles. The curves in Figure 5-8 are for sample #1, n-channel devices in unpassivated polysilicon thin-films. The similar curves in Figure 5-9 and 5-10 are for both n- and p-channel transistors in H^+-implanted (passivated) films. The parameters used for calculation are listed in Table 3-1 and 5-1.

By examining the values of η in Table 5-1, it is interesting to note that for unpassivated devices, η-value is only a few hundredths, while for passivated transistors, η is enhanced by a factor about one order. It appears to suggest that passivation can reduce the surface state density and improve the channel-oxide interface quality. This explanation is consistent with the passivation induced reduction in grain boundary trap densities. The same behavior was found in other experiments[6].

The results of the C-V measurement from the test structures (as discussed in Chapter 4) are shown to be remarkably consistent with this model

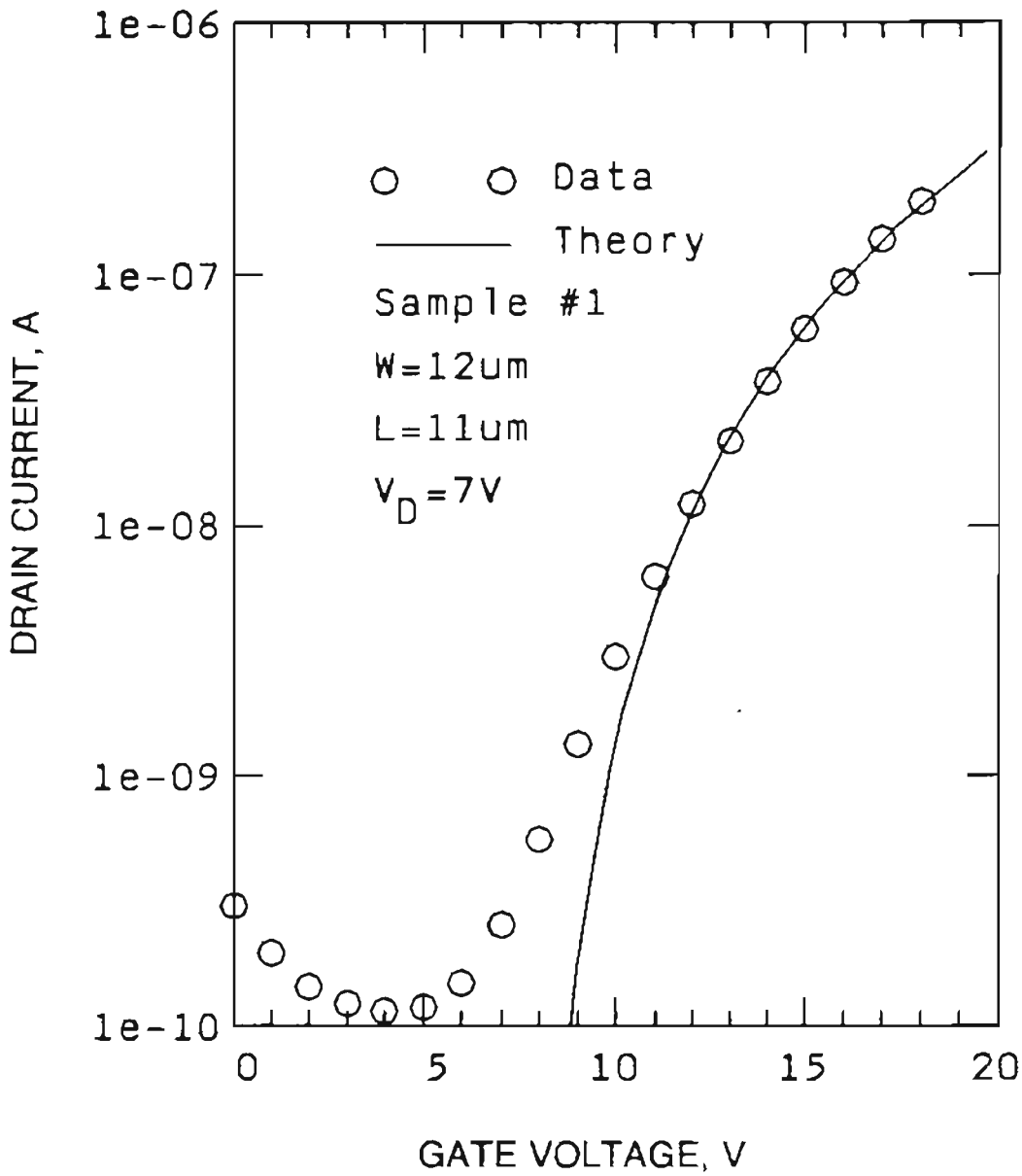

Figure 5-8(a) Comparison between theory and experimental data. The solid line are theoretical results and the open circles (○) are data measured from sample #1. The fitting parameters for calculation are listed in Table 5-1.

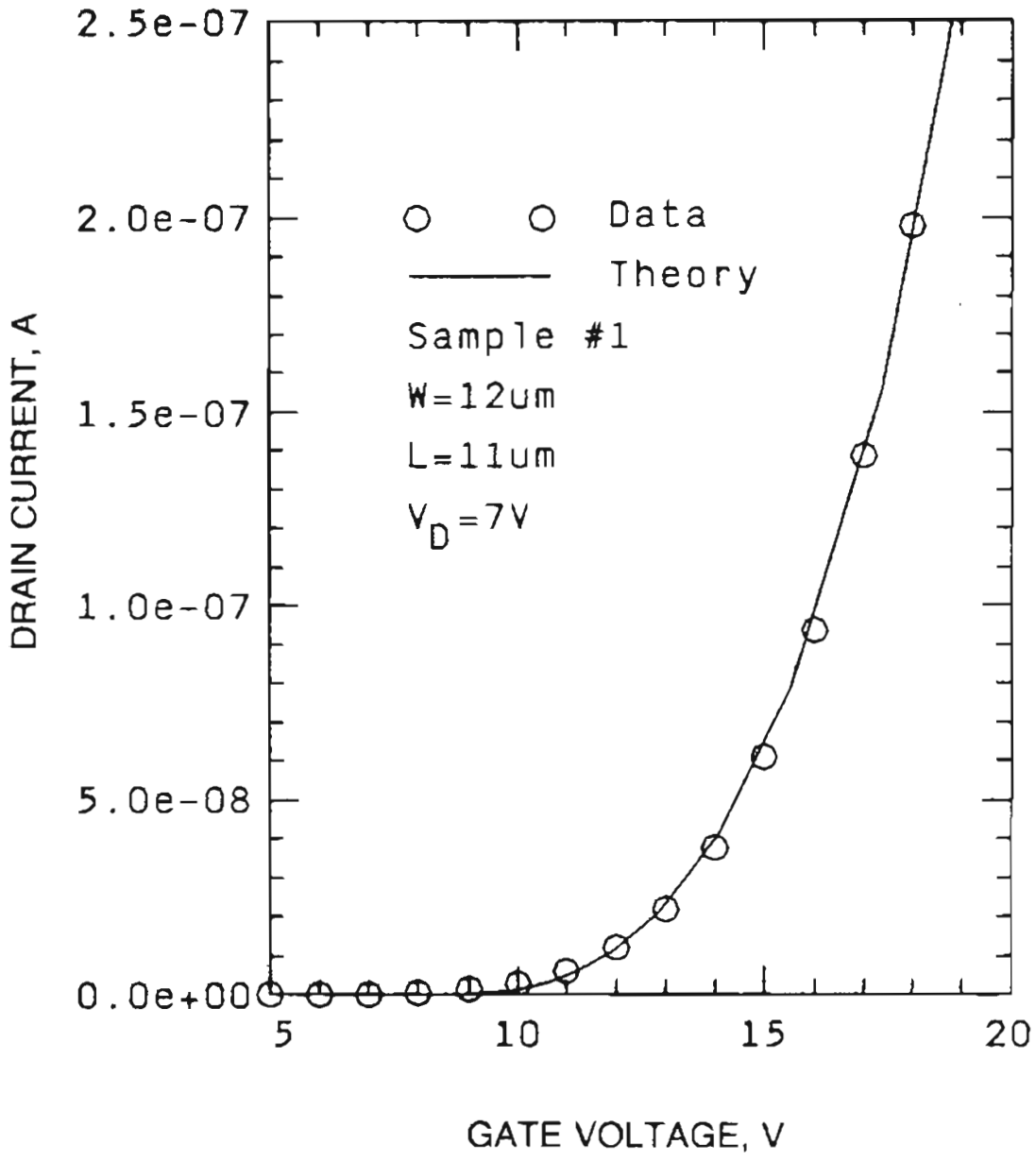

Figure 5-8(b) The same data as in Figure 5.8(a) plotted in linear scale.

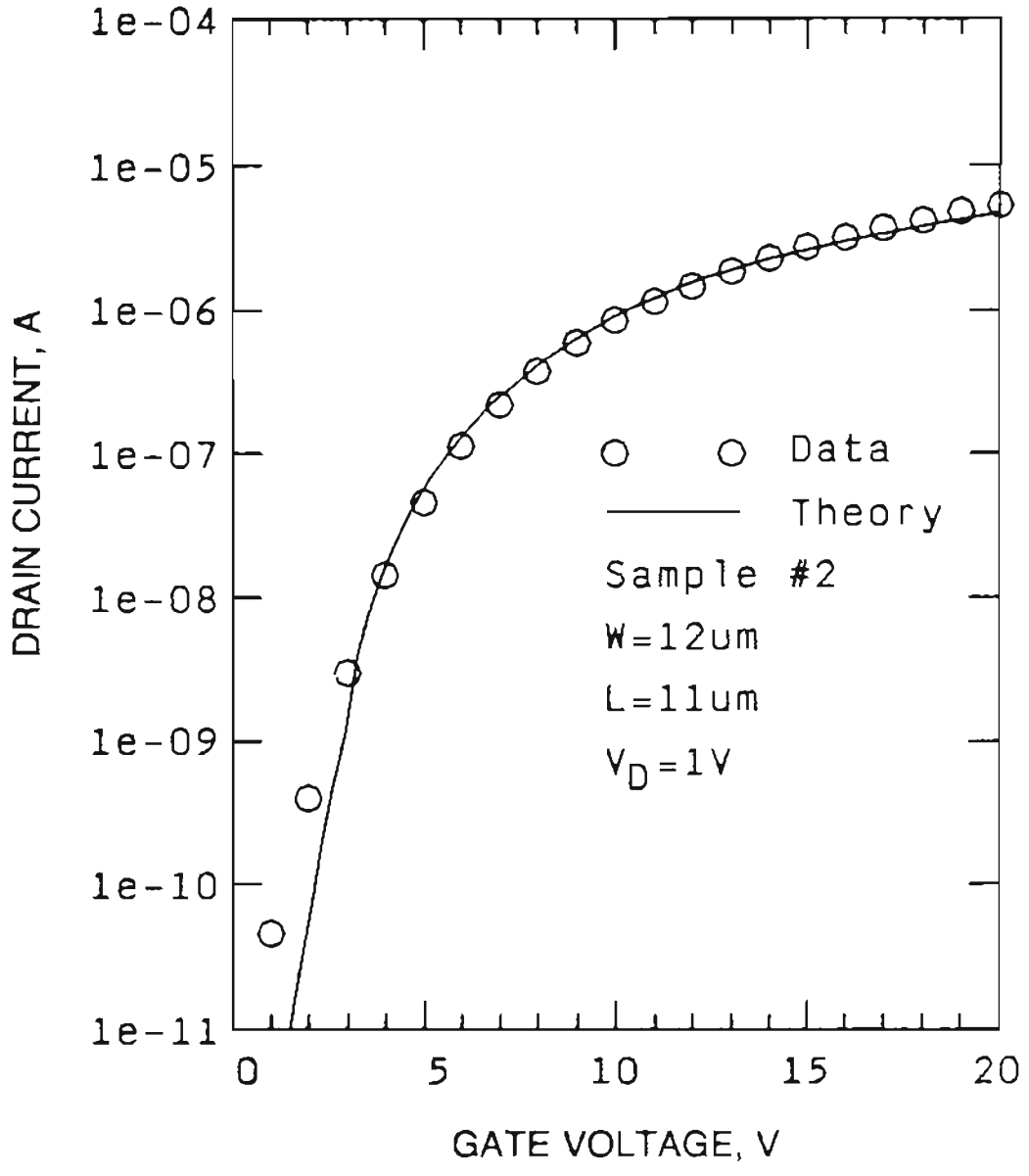

Figure 5-9(a) Comparison between theory and experimental data. The solid line are theoretical results and the open circles (○) are data measured from sample #2. The fitting parameters for calculation are listed in Table 5-1.

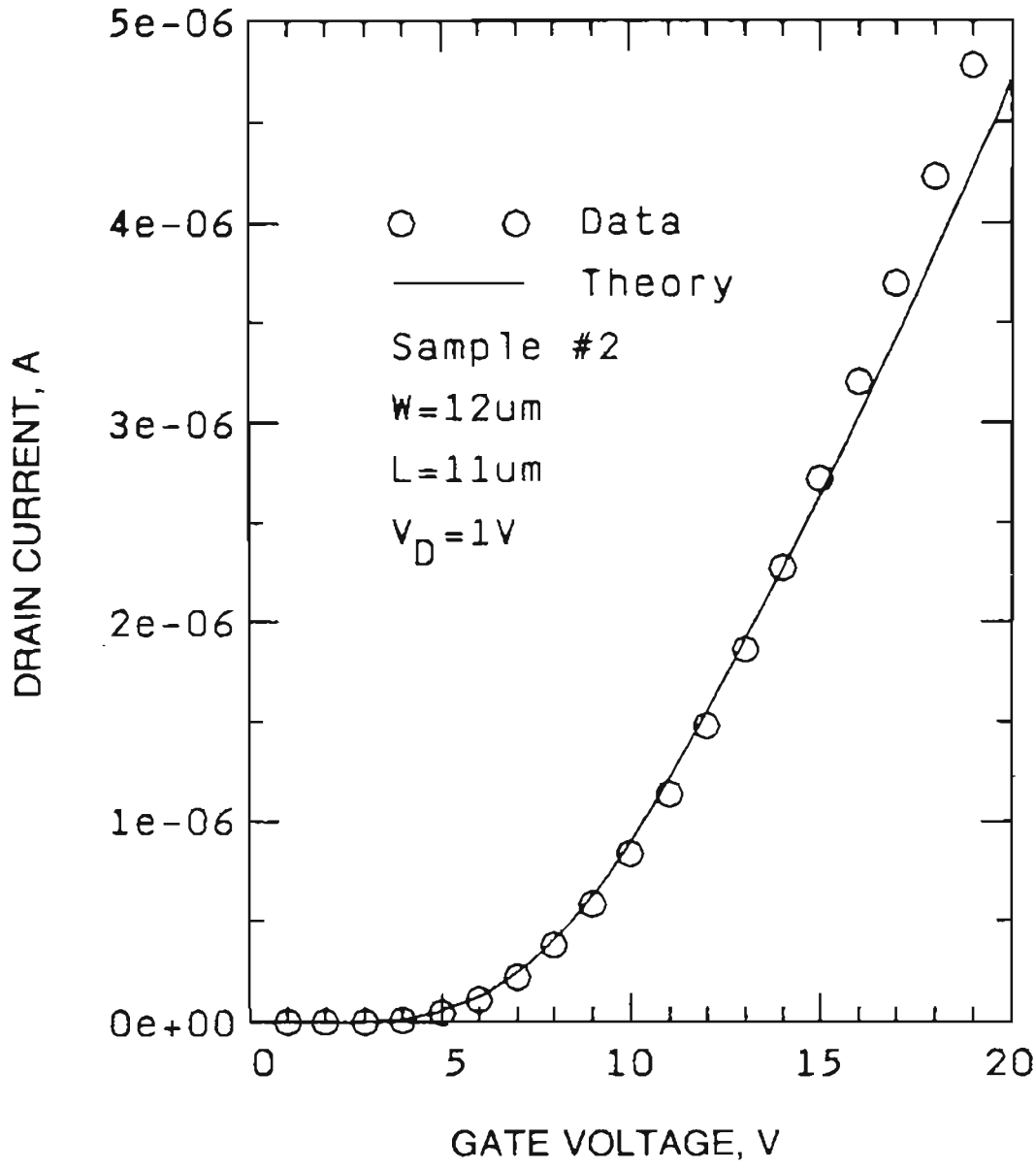

Figure 5-9(b) The same data as in Figure 5-9(a) plotted in linear scale.

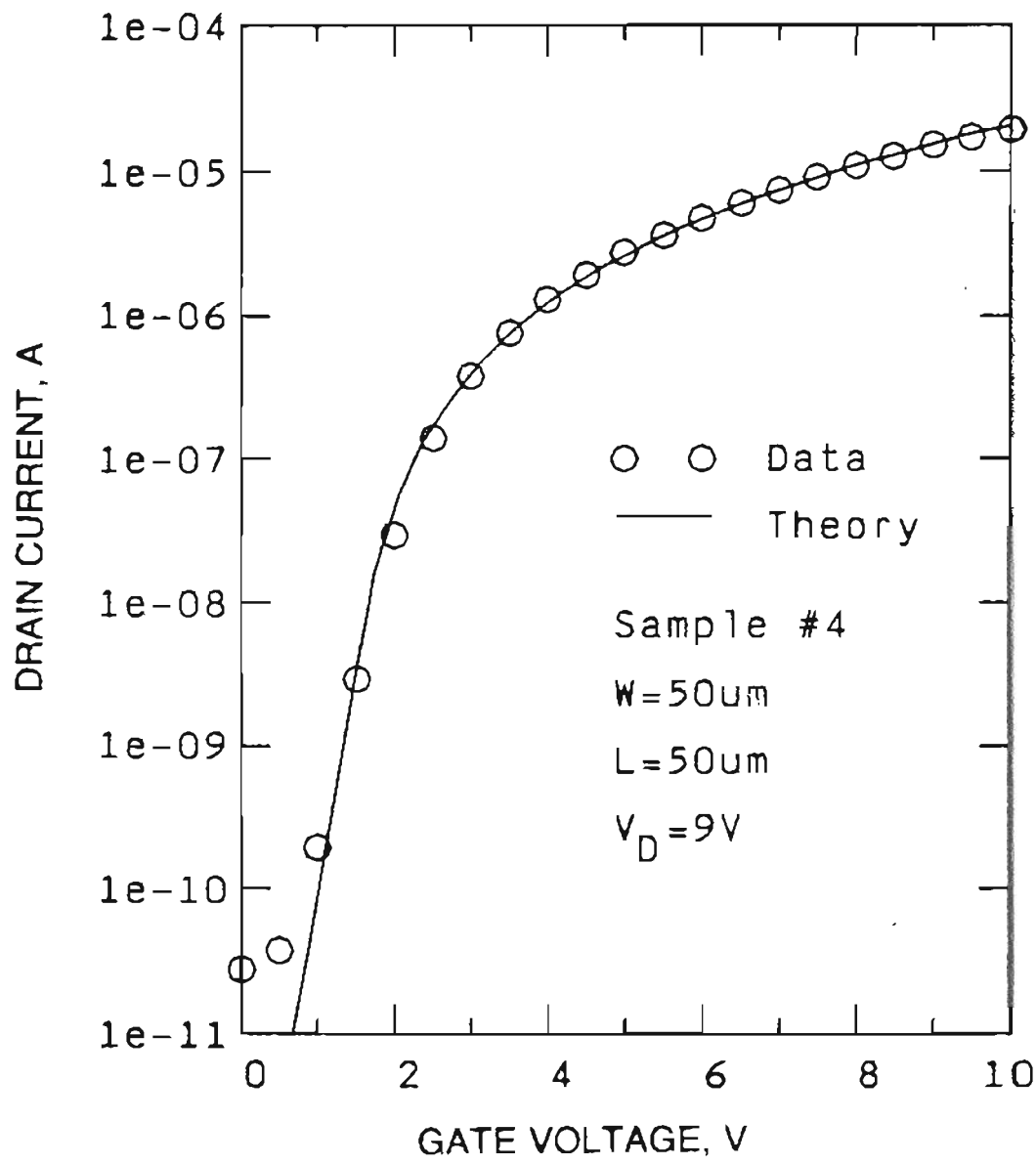

Figure 5-10(a) Comparison between theory and experimental data. The solid line are theoretical results and the open circles (○) are data measured from sample #4. The fitting parameters for calculation are listed in Table 5-1.

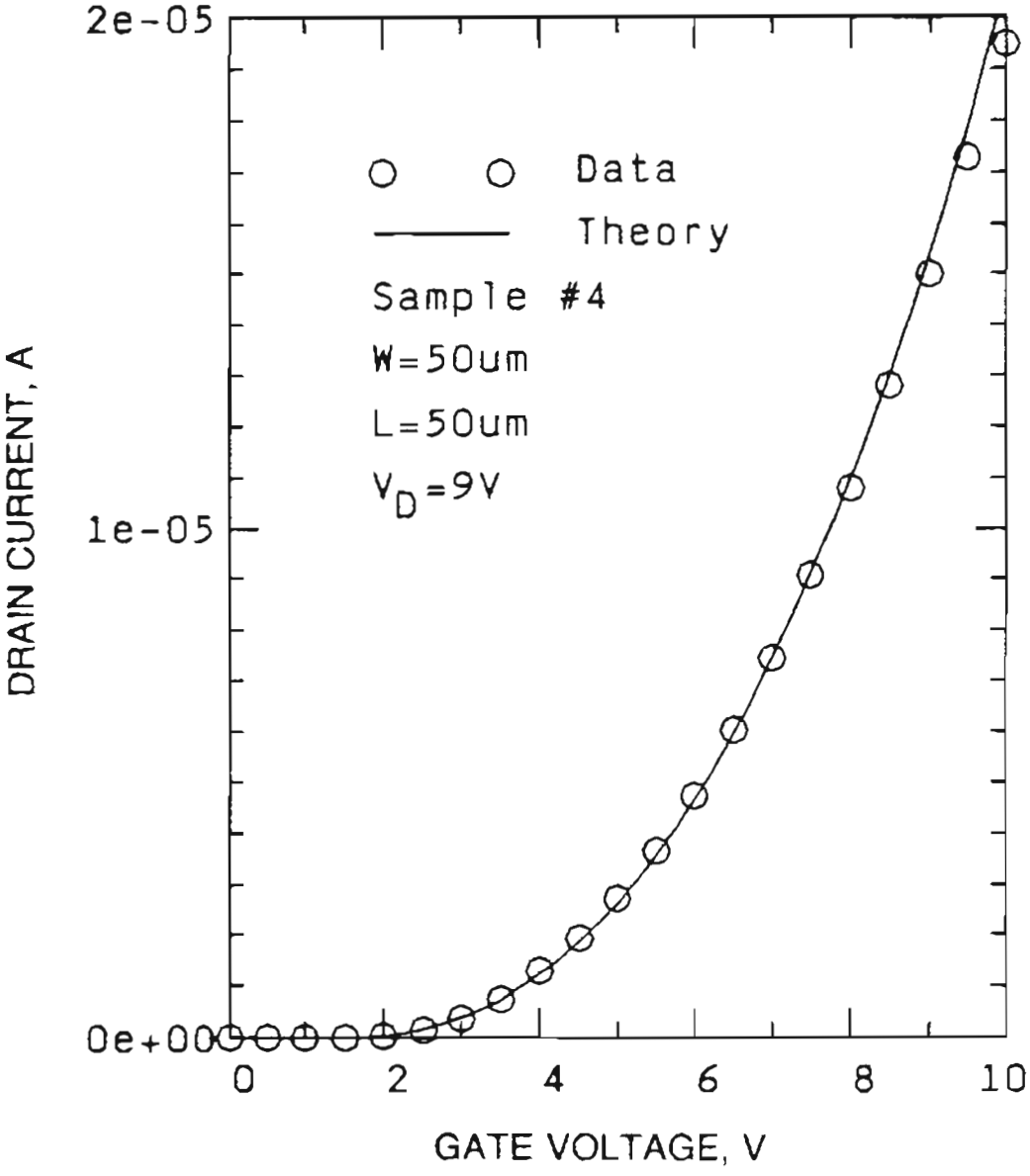

Figure 5-10(b) The same data as in Figure 5-10(a) plotted in linear scale.

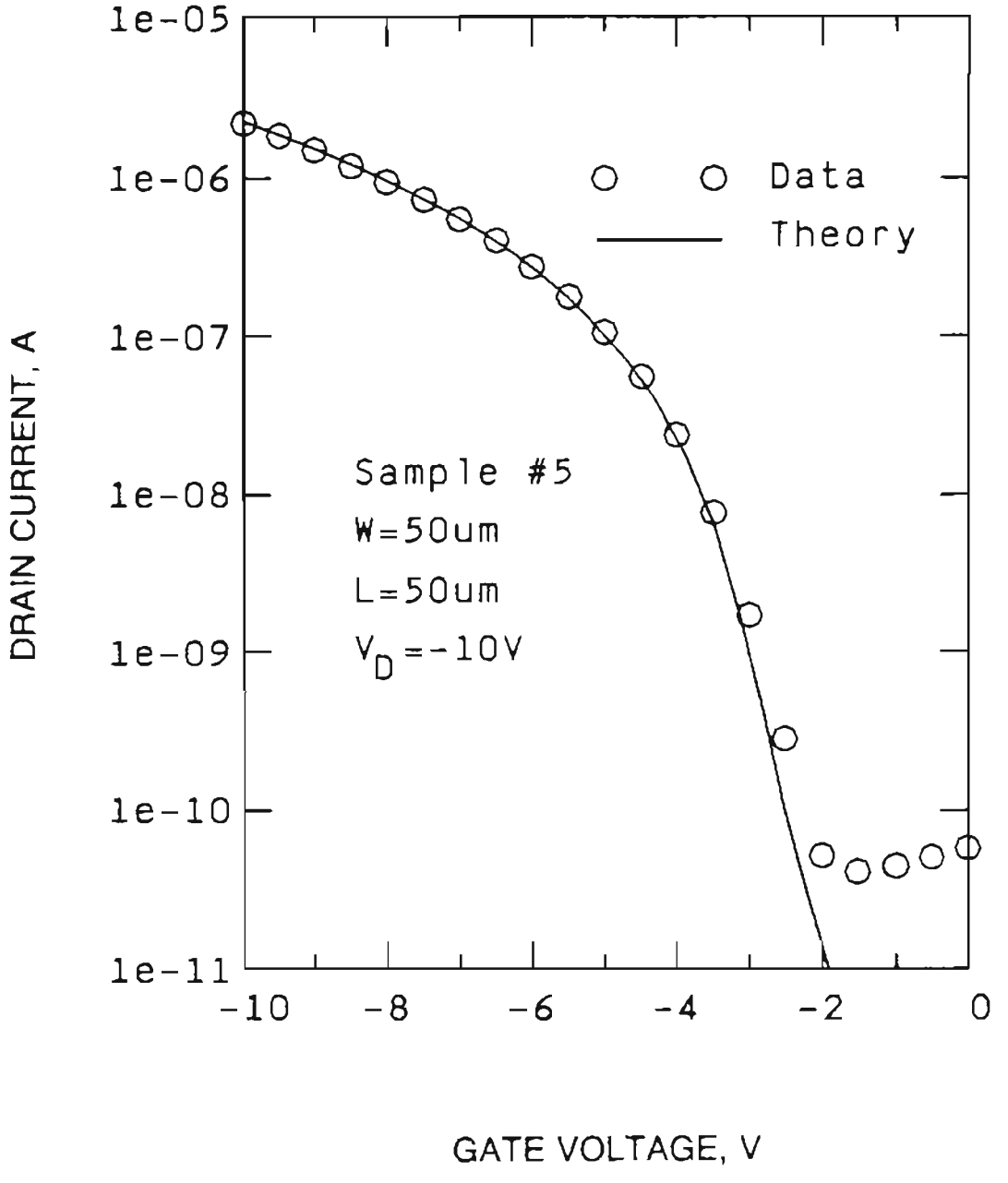

Figure 5-11(a) Comparison between theory and experimental data. The solid line are theoretical results and the open circles (○) are data measured from sample #5. The fitting parameters for calculation are listed in Table 5-1.

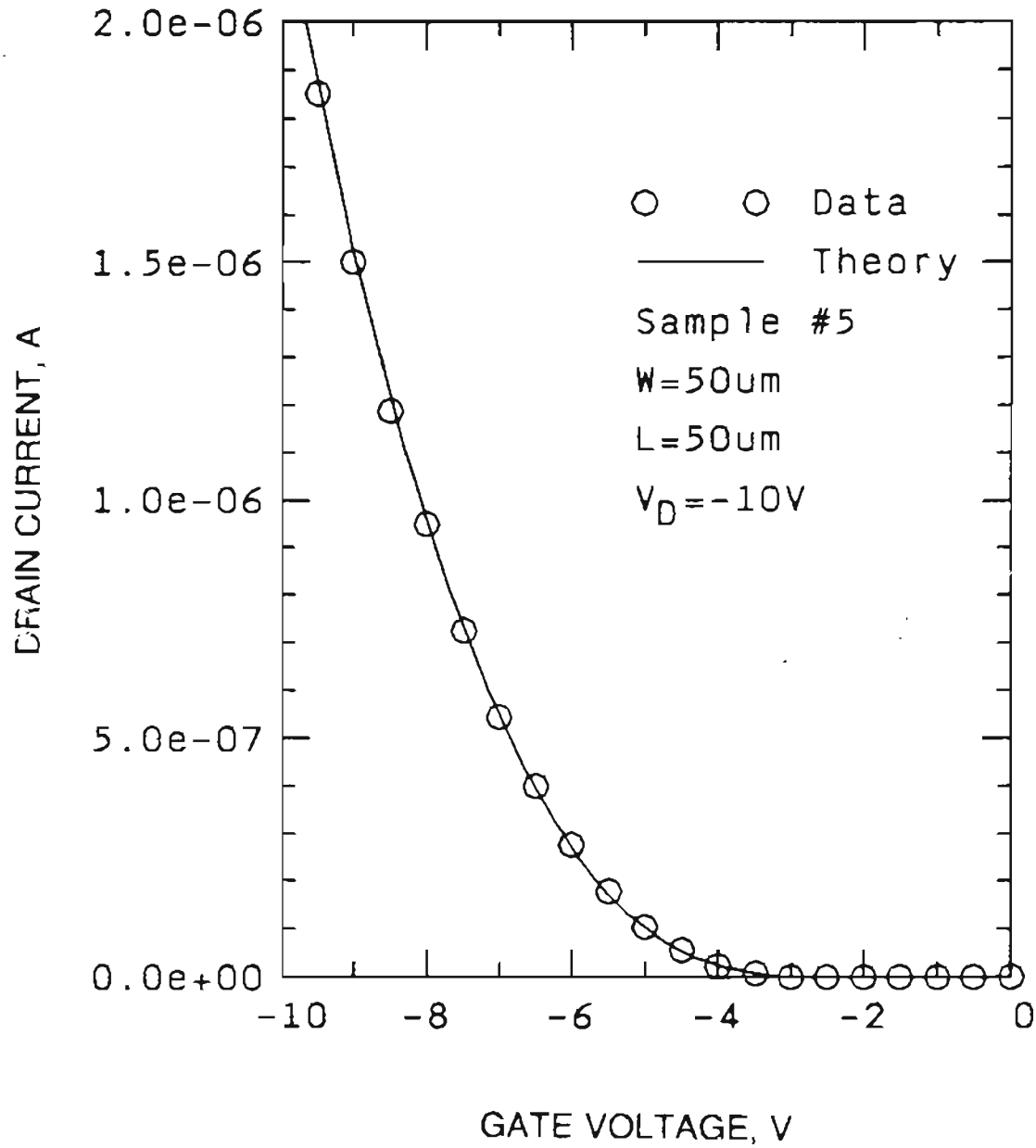

Figure 5-11(b) The same data as in Figure 5-10(a) plotted in linear scale.

based on the concept of "effective channel doping" (see Figure 4-16). Since the "effective trap density" in these devices is much larger than the external dopant concentration, the C-V behavior is completely controlled by N_{eff}, and the effect of dopant type and concentration are irrelevant.

From the observed capacitance minimum, it is possible to estimate the value of N_{eff} by using the depletion model. Assume an abrupt depletion layer edge, although not strictly valid for small depletion layers (i.e. depletion depth less than or about equal to the Debye length). Then the depletion depth is found from

$$d = \epsilon_s \cdot A / C_D \tag{5.28}$$

with A being the capacitor area and C_D the depletion capacitance. From the C-V data shown in Fig. 5.13, the depletion depth is determined to be 17 nm. The effective dopant concentration in the depletion layer can, in turn, be estimated by

$$d = \sqrt{2\epsilon_s \phi_s / qN_{eff}}. \tag{5.29}$$

The effective doping is found to be 2.2×10^{18} cm^{-3}. In this calculation, ϕ_s has been taken as one half the band gap, since the Fermi level is pinned near mid-gap in this case. Indeed, the value of N_{eff} is seen to be much larger than the dopant concentrations used. This explains the identical C-V curves for different doping.

Table 5-1					
Parameters	Sample				Unit
	#1	#2	#4	#5	
N_T	1×10^{13}	1×10^{12}	8×10^{11}	8×10^{11}	cm^{-2}
E_T	0.1	0.1	0.2	0.2	eV
L_g	50	50	100	50	nm
δ	2	2	2	2	nm
Δ'	0.1	0.045	0.015	0.045	eV
μ_c	700	700	700	300	$cm^2/V\cdot s$
μ_{gb}	2	2	2	2	$cm^2/V\cdot s$
η	0.07	0.5	0.45	0.45	–
N_{ss}	0	1×10^{12}	6×10^{11}	3×10^{11}	cm^{-2}

Table 5-1 Fitting parameters used for theoretical calculations in Figures 5-8 through 5-11.

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CHAPTER 6

SUMMARY OF THE WORK

In this thesis, both n-channel and p-channel Polysilicon thin film transistors have been fabricated, characterized and modeled, using a unified formulation. The discussion was focused on small grain and grain boundary passivated devices. The highlight of the results are as follows.

(i) The primary role of grain boundary trap sites from the device operation point of view is to provide a large effective doping, N_{eff}. For n-channel device, N_{eff} is contributed by trapped electrons near the surface, while for a p-channel device, N_{eff} is due to trapped holes. This effective doping plays the role of ionized dopant atoms and determines the surface band bending under gate bias. The concept of "effective doping" has been shown to be operative and consistent with the observed C-V data.

(ii) The electrostatics for n- and p-channels and the operational principles of the devices are same. A simple comparison between n-channel and p-channel devices are listed in Table 6-1. The device operation is shown to be symmetric.

Table 6-1

	N-channel	P-channel
Channel Material	p-type	p-type
Gate Voltage	+	−
Fixed Charge	−	+
Mobile Charge	−	+

(iii) The p-channel, accumulation-mode field effect transistor is a feature unique in polycrystalline thin films.

(iv) The large value of "effective doping" renders the threshold voltage appreciably dependent on both gate and drain voltage. A constant threshold approximation cannot be applied to the thin film transistors in polycrystalline materials.

(v) For small grain and grain boundary passivated devices, the channel mobility remains nearly constant and independent of gate voltage. However, the value of mobility depends sensitively on grain boundary properties, such as trap density, level and mobility shoulder.

(vi) The threshold voltage is mainly controlled by trapped carriers near the

polysilicon surface and is difficult to be adjusted by a small amount of external channel doping.

(vii) Hydrogen passivation can significantly reduce the trap density in grain boundaries. This increases the channel mobilities and lowers the threshold voltage. The gate voltage swing is also improved due to passivation via enhanced surface band bending. The new process technique, in which the channel films are Si^+-implanted, and then recrystallized at around 600 °C to form low-angle grain boundaries and grow large grains, can also reduce the effective doping and improve the device performance.

(viii) The calculated subthreshold slope is sometimes larger than the experimental data, especially, from unpassivated devices. This is due to a monoenergetic trap level assumption which may result in an overestimation of the subthreshold slope, via the gate voltage dependence of the surface potential.

(ix) A quantitative understanding of the leakage behavior remains one of the unsolved problems.

VITA

The author was born in Gooshan on November 8, 1957. He moved to Jiangyin in 1963 when he began his schooling. He graduated from Nantsing High School in 1974 and worked in a commune for the next two years. He was a technician in the electronic products R & D group in Jiangyin Business Machinery Plant from 1976 to 1978. In 1978, he enrolled in Huazhong University of Science & Technology (HUST) where he majored in solid-state electronics. The author received his degree Bachelor of Science and earned a faculty position in the Department of Solid State Electronics, HUST in January, 1982. He began to pursue his doctoral degree at Oregon Graduate Center in 1984. During the course of study he has been a technical consultant for polysilicon thin film transistor technology development at Tektronix, Inc. and performed design, characterization, modeling and improving devices.

The author has contributed following technical papers and books:

1. F. Qian, D. M. Kim, and G. Kawamoto, "Inversion/Accumulation-mode polysilicon thin film transistors: Characterization and unified modeling," submitted to *IEEE Trans. Electron Devices.*
2. F. Qian, D. M. Kim, H. K. Park, and J. L. Sachitano, "Inversion-mode MOSFET's in polycrystalline silicon thin films: Characterization and modeling," *IEEE Trans. Electron Devices,* ED-34, No.12, 1987.

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The author has had following meeting presentations:

1. F. Qian, D. M. Kim, and G. Kawamoto, "Polysilicon thin film transistors," Portland International Conference and Exposition on Silicon Materials and Technology, Portland, Oct. 12-13, 1987.
2. F. Qian, H. K. Park, and D. M. Kim, "Enhancement-mode MOSFET's in LPCVD polysilicon thin films," Portland International Conference and Exposition on Silicon Materials and Technology, Portland, June 30-July 2,1986.