GETTERING OF IMPURITIES IN INDIUM PHOSPHIDE SUBSTRATES FOR THE GROWTH OF HIGHER PURITY EPILAYERS

Rayluck Joy B. Alcantara
B.S., University of the Philippines, Quezon City, Philippines

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The thesis " Gettering of Impurities in Indium Phosphide Substrates for the Growth of Higher Purity Epilayers" by Rayluck Joy B. Alcantara has been examined and approved by the following Examination Committee:

Wallace B. Leigh
Assistant Professor
Thesis Research Advisor

Rajendra Solanki
Associate Professor
Resident Thesis Advisor

John S. Blakemore
Professor

Paul R. Davis
Professor

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To my mother

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CHAPTER 1

INTRODUCTION

Indium phosphide (InP) is now established as a technologically important material. Its device applications include LED's, microwave devices, heterostructure lasers and photovoltaic cells. Among the properties that make it suitable for these applications are its high peak-to-valley ratio in its velocity-field characteristics, large thermal conductivity and smaller electron-diffusion coefficient at the same normalized field as compared to GaAs. In addition, the energy gap of InP is close to the optimum value for the efficient conversion of solar to electrical energy [1].

Most of the device applications of InP require the epitaxial growth of high quality layers on substrates. This is not easily achieved however. One of the most serious problems encountered is the outdiffusion of both major dopants and residual impurities from substrate to epilayer during growth. This often results in changes in the conductivity type of substrate and epilayer and the degradation of the electron mobilities of the epilayer.

One way to minimize outdiffusion is to getter out the impurities from substrates before growth. This study aims to explore two possible gettering techniques to improve InP substrates used for epitaxial growth. The first technique involves the simple annealing of the substrates in a controlled atmosphere. The second involves the alloying of indium (In) onto the backside of the samples and subsequent annealing. Efforts were made to optimize annealing parameters such as time, temperature and the composition of the ambient medium.

Both techniques involve the formation of damaged regions on the semiconductor surfaces. In simple annealing, this can be due to the creation of vacancies on the surface during the thermal treatment. In the alloying of a metal onto a semiconductor surface, damage is created by the layer of metal atoms which has diffused into the semiconductor. According to theories on the mechanism of outdiffusion in semiconductors, the damaged regions characterized by dislocations and vacancies , act as chemically reactive sites which can capture impurities [2]. Impurities which have accumulated on the semiconductor surface can be removed by etching. Past studies show that gettered/etched substrates result in better quality epilayers [3,4]. The results of the present study for the low purity substrates agree with these previous findings. They show that In-alloying of low purity substrates results in epilayers with better electrical and optical properties.

The effects of the gettering processes were determined by various characterization techniques. Optical microscopy was used to study changes in the morphology of the substrate surfaces. Photoluminescence was used to determine the relative purity and defect levels of the samples. Hall measurement was done on epilayers on both gettered and ungettered substrates.

Chapter II of this thesis reviews related studies and presents the theoretical background for the present problem. It briefly discusses the most common major dopants and residual impurities in InP. It also reviews previous studies on thermal redistribution and gettering techniques in InP and GaAs. Chapter III discusses the gettering procedure and Chapter IV, the characterization procedure. Chapter V presents the results and discussion. Finally, Chapter VI gives the conclusions.

CHAPTER II

BACKGROUND OF STUDY

A. Impurity and Thermal Redistribution Studies in InP

Evaluation of substrate gettering techniques requires knowledge of impurities in the material of interest. In this study, the gettering techniques are aimed at minimizing the outdiffusion into epilayers of major dopants and residual impurities. Thus a discussion of previous studies on residual impurities and major dopants is important. Studies on impurity identification in undoped InP has established zinc as the most common residual acceptor in undoped melt-, vapor-, and solution-grown InP [5-7]. In semi-insulating LEC InP, the most common compensating dopant used is iron (Fe) or chromium (Cr). A comprehensive review of impurities in InP is given in reference [43]. In addition, Table I gives a summary of impurities in InP as determined by PL measurements.

There seems to be a considerable number of studies on the behavior of impurities in InP during thermal annealing. A review of these studies is given below. Most of the studies focus only on the thermal redistribution of the various impurities. Removal of the surface-segregated impurities and subsequent epitaxial growth to determine the effect of gettering on the outdiffusion of impurities during growth were not part of these experiments. Very few studies were conducted along these lines.

Table I. Photoluminescence Measurements for Acceptors in InP

Acceptor	T (K)	Nature of Transition	Energy of Transition (eV)	Binding Energy (meV)	Growth Method	References
Zn	4.2	DA	1.3740	45.5	LEC, VPE LPE	[6]
	4.2	BA	1.3780	"	"	
Be	1.7	DA	1.3780	41.3	LEC, VPE LPE	[7]
	11.6	BA	1.3810	"	"	
Mg	4.2	DA	1.3810	38.8	LEC	[6]
	4.2	BA	1.3847	"	"	
Ca	4.2	DA	1.3780	41.7	LEC	[6]
	4.2	BA	1.3818	"	"	
Cu	6	Cu-complex	1.348		VPE	[5]
	80	BA	1.355		"	[8]
Cd	50	BA	1.362	58	LPE	[5]
Hg	50	BA	1.32-1.33	98	LEC	[5]
C	1.7	DA	1.376	44.6	LEC	[7]
Mn	2	BA	1.184	230	LPE	[9]
Fe(I)	6	$^5T_2$-^5E	0.35	770	LEC	[9],[10]
(II)	2	BA/DA	1.135	270		
Cr	6	$^5T_2$-^5E	0.85	---	---	[11]

BA - band-to-acceptor
DA - donor-to-acceptor

The study of thermal redistribution of impurities in InP was initially motivated by the concern over adverse effects of high temperature processing on material properties. Secondary Ion Mass Spectrometry (SIMS) measurements have shown considerable thermal redistribution of the bulk compensating dopant Cr in SI GaAs [3]. This was found to result in lower resistivity n-type material. Similar concern for the thermal conversion of SI InP due to the redistribution of the bulk compensating dopant Fe has resulted in many similar studies on this material. Recent studies combine SIMS and PL in investigating the surface segregation of Fe either as as major dopant or as a residual impurity [12,13,14].

In a study of Cr and Fe redistribution in SI InP, Oberstar et.al. [14] observed that annealing with an Si_3N_4 cap leads to an accumulation of transition metals within the first 500 A of the surface and a depletion of impurities extended to a depth of about 1 μm. The anneals were conducted at 550°C and 750°C for 30 minutes. The 750°C anneals resulted in less impurity concentrations in the bulk and greater pile up at the surface [14].

Studies of the thermal redistribution of residual impurities have also been conducted [2, 18]. Considerable research has been done on the behavior of zinc (Zn), Cr, Fe and manganese (Mn) (as residual acceptors) under high temperature conditions. Zn, generally considered as a fast diffusing element in InP was found to migrate toward the surface of the samples during annealing. SIMS measurements on annealed undoped InP samples indicate that Cr, Mn, Fe and Zn migrate toward the surface and pile up over varied depths depending on the element: 5000 A for Mn and Fe, 4-5 μm for Cr and 2-3 μm for Zn. A depletion zone occurring after the accumulation region was observed for Fe. It extends up to 3 μm. No depletion zones were observed for Cr, Mn, and Zn

[2].

It appears that a second motivation for the study of impurity redistribution is based on the need to improve substrates for epitaxial growth. It was found that the temperature conditions during epitaxial growth induce the segregation of trace impurities near the surface of the substrate [13,18,24]. Subsequent outdiffusion of these impurities into the growing epitaxial layer was found to degrade the quality of the resulting epilayer [3,4].

Outdiffusion of impurities into epilayers during growth was first discovered for transition metals in III-V compounds. From tests of GaAs layers on Cr and Fe- doped substrates, Lang and Logan found Deep Level Transient Spectroscopy (DLTS) signals from Cu , Fe and Cr in the layers grown at 850^{o}C. However, they attributed this to the surface contamination of the substrate before growth rather than from the outdiffusion of impurities during growth. White et al. examined VPE layers on Cr-doped substrates using a photocapacitance technique. They found a signal due to Cr in the layers. It was then thought that the Cr diffused into the layers during growth. Cox and DiLorenzo found that the first few microns of epilayers on SI substrates were of higher resistivity than expected. They believed that this was due to the outdiffusion of bulk compensating impurities from substrate to epilayers during growth. Although these findings all seem to point to the occurrence of outdiffusion of impurities during growth the reports are quite ambiguous [15].

Tuck et al. [15] tested the proposition in a direct way. Substrates were homogeneously doped with radioactive Cr using diffusion. Epitaxial layers were then grown on these substrates and then examined for the radiotracer. The findings show the presence of radioactive Cr in the epilayers. This result could only mean that Cr diffused into the layers during growth [15].

There seems to be fewer studies of the thermal redistribution of donors. Most of

the studies are on sulfur (S), which is a major dopant for n-type InP or a residual impurity in undoped samples. Studies of the effects of sealed ampoule annealing of S-doped InP indicate that S is a rapidly diffusing element in n-type InP [16,17]. Its diffusion coefficient is two orders of magnitude greater than that of Zn [16]. Similar studies on tin (Sn)- and selenium (Se)-doped InP also reported large diffusion coefficients. These studies combined defect etching and cathodoluminescence (CL) imaging to detect diffusion fronts in the samples [16,17].

There had also been studies of n-type residual impurities. These studies involved S and Si. SIMS measurements showed that the accumulation of these residual donor impurities is 2 to 3 times deeper than that of the acceptors [18].

Studies on impurity redistribution have presented possible mechanisms for the surface accumulation of these impurities. Findings show that dopants or residual impurities migrate toward defect-rich regions on substrate surfaces. Such surface defects may have been a result of strain due to the high temperature conditions during annealing; thermal mismatch between encapsulant and substrate during annealing; surface states and/or surface impurities giving rise to a near surface electric field and mechanical damage [2].

It is also believed that the surface segregation of residual acceptors in InP is related to the presence of indium vacancies. The formation of these vacancies is thought to be induced by thermal treatments. The uphill diffusion of acceptors can be described by the following chemical reaction:

$$V_{In} + M^{+}_{i} = M^{-}_{In} + 2h^{+}$$

V_{In} is an indium vacancy, M^{+}_{i} is an acceptor metal atom in an interstitial position and M^{-}_{In} is the same metal atom in a substitutional site [2].

On the other hand, it is thought the uphill diffusion of donors is induced by the presence of phosphorus vacancies. Such mechanism may be summarized in an equation similar to that given above, this time, with a phosphorus instead of an indium vacancy and a donor atom instead of a metal acceptor atom. But why the accumulation of donors is faster and thus extends deeper into the substrate than that of acceptors is not clear from these explanations [2].

Optimization of annealing parameters has been a matter of deep concern in the gettering of impurities. Various ambient media, temperatures and durations have already been tried. Studies on the gettering of acceptors Fe and Cr resulted in greater surface concentration and deeper accumulation in anneals in an H_2 ambient. Findings show that redistribution seems to be slower in inert media such as He, Ar and H_2-Ar mixtures [18]. Although there had been similar work on the other acceptors Zn and Mn, it seems that the influence of ambient media on these impurities' thermal redistribution is a relatively unexplored area.

The donor impurities S, Sn, Se were found to outdiffuse rapidly in doped n-type InP samples annealed in vacuum. Using defect etching and CL imaging, deep diffusion fronts were observed in n-type and SI Fe-doped or p-type crystals [16].

B. Thermal Redistribution and Electrical Properties

During a high temperature treatment, the segregation of impurities may alter the electrical properties of some regions in a semiconductor. Impurities diffusing into the surface may change the carrier concentration, resistivity and conductivity type at the surface. This phenomenon is known as thermal conversion.

Thermal conversion was first observed in GaAs in 1960. J.T. Edmond and J.J. Wysocki presented initial reports on this phenomenon. Edmond found that samples of n-type GaAs became p-type or less strongly n-type as a result of the heat treatment. The anneals were done in vacuum at 1000^{o}C with durations from 15 to 60 hours [36]. Edmond pointed to copper (Cu) contamination from quartz ampoules as the possible cause of the conversion.

Wysocki found that n-type GaAs with a carrier concentration of 5 x 10^{16} or less invariably converted to p-type when it was heated in vacuum at 800^{o}C for short times. Measurements were made of the diffusion constant and the activation that characterize the conversion. The data obtained matched those for Cu diffusion. Hence, Wysocki's findings support Edmond's point of view [37].

It seems that there was a brief pause in research activity on thermal conversion after the initial findings. In 1975, this area received renewed attention from researchers because of poor performance of microwave devices made on active layers grown on converted material [38]. Epitaxial growth starts with heating the substrate up to the working temperature. This can induce the pile up of impurities on the surface. During growth, these impurities diffuse into the growing layer.

In 1970, Munoz, et. al. presented strong evidence that p-type conversion in n-GaAs is not due to contamination but is related to the formation of Ga and As

vacancies. The changes in carrier concentration as function of As vapor pressure showed the acceptors to be associated with As vacancies[39].

Studies on changes in conductivity type due to high temperature treatment seem to dominate research on thermal conversion. In general, experiments reveal that type conversion depend on the annealing parameters. J. Hallais et al. found that annealing SI GaAs at 750 ^{o}C in vacuum or in an H_2 ambient creates a p-type surface layer [40]. They attribute this to Ga vacancy formation for vacuum annealing and an accepter at E_V + 110 meV for H_2 annealing. Watanabe et * al. reported that suppression of p-type conversion in SI GaAs can be achieved by annealing in $H_2/Ar/As_4$. The thermal stability of the samples was thought to be due to minimized V_{Ga} and V_{As} formation. This then results in the suppression of Cr-outdiffusion and of Mn_{Ga} and Si_{As}- V_{As} complex formation.

Most studies point to depletion or accumulation of the bulk or major dopants as the main cause of the type conversion. Feng et. al. found that Mn and Cr deplete near the surface of SI GaAs annealed with an SiO_2 encapsulant. Their experiments also indicated that the dopants accumulate under capless annealing [41]. These observations are supported by an earlier finding by Y. Sato in 1973. In a study of annealing of SI GaAs doped with Cr, Sato found that a thin n-type conductive surface is formed on the sample surface when annealing is done with an SiO_2 encapsulant. He concluded that the cause of the conductive layer formation is a decrease in the concentration of Cr which compensates undesirable donors in SI GaAs [27].

Klein found that the conversion of the surface of SI GaAs samples correlates closely with (1) substantial build-up of Mn near the surface as detected by SIMS, (2) the

presence of a PL band at 1.41 eV attributed to Mn_{Ga} and (3) acceptors with 0.1 eV activation energy (i.e Mn) dominating the conductivity of the type-converted layers. These findings point to the accumulation of Mn on the semiconductor surface as the main cause of thermal conversion in the SI surface.

Thermal stability is also a matter of deep concern in the fabrication of planar GaAs devices. Ion implantation into SI GaAs substrates is done to form the active regions for microwave FET's and analog and digital IC's. Complete electrical activation of the implanted impurities and healing of the implantation damage requires annealing. This high temperature treatment however often results in lower resistivity surface regions. Studies of thermal conversion in ion-implanted GaAs are reviewed in Section B of this Chapter.

In general, most of the studies reviewed above combine PL, SIMS and Hall measurements in investigating thermal conversion. PL was used to identify impurities that have accumulated in sample surfaces. SIMS was performed to determine the depth distribution of the impurities. Hall data were taken to determine how the thermal processes affected the electrical properties.

This study mainly utilizes PL and Hall data in developing the gettering techniques. Unlike other studies however, it focuses more attention to the analysis of Hall data. Device applications of epitaxial structures require carefully controlled electrical characteristics. Since this study aims to develop substrate gettering techniques for improved epilayers, analysis of Hall data is important.

C. Gettering Techniques

Gettering involves the removal of impurities from specific regions in semiconductor samples. It has been done on Si in order to remove impurities from device regions. This is required to produce high yielding VLSI.

There are two major types of gettering processes: extrinsic and intrinsic gettering. In extrinsic gettering, damage or stress in the semiconductor lattice is created by external means. In most cases, such defects are generated on the backside of the wafer although studies have also been made on frontside gettering. The defects thus created act as sinks into which impurities are trapped [19].

Gettering regions in Si include thermal processing induced damage-rich regions at the surface, ion-implantation induced damage (I^2- damage) region and a phosphorus diffused region. Gettering of impurities in Si has been extensively studied in the past two decades [20].

Native defects such as those induced by oxygen precipitates in Si can also act as sites into which impurities can be captured. This occurs in intrinsic gettering. Of the two gettering processes, extrinsic gettering has been widely used in both Si and GaAs in the gettering of mobile metallic impurities [19].

Of great relevance to this study are the studies of gettering in GaAs. To the knowledge of this author, most studies of gettering in GaAs involve extrinsic gettering. Much of the research done focused mainly on Cr gettering in SI substrates.

T.J. Magee et al. investigated the use of mechanical backside damage gettering in improving the quality of GaAs substrates and VPE layers on SI GaAs. Polished front surfaces of the samples were coated with 2000 A of SiO_2. This film served as the scratch protection layer during the backside damage operations. A rotary abrasive unit

was used to create macroscopic concentric damage grooves (≤30 μm) at the backsurface of the sample. After the damage process, the SiO_2 layer was removed and a 1000 A thick Si_3N_4 encapsulant was formed on the frontside at 200°C by plasma deposition. Anneals were then performed in an H_2 ambient at temperatures in the range 750-900°C. A vapor etch was next done after which the epitaxial growth was performed [21].

The samples were then analyzed using TEM. The TEM results show laterally continuous array of dislocation structure extending to a depth of 1.5 μm below the depth of damage grooves at the backside. SIMS profiles also show significant concentration of gettered Cr within the region approximately equal to the width of the damage region.

The effect of gettering on the front surface of the substrate was also studied. Backside-damaged as well as control substrates were annealed for 1 hour at 750°C. A Si_3N_4 layer (1000 A) was plasma deposited at 200°C at the frontside to serve as the encapsulant. After etching in H_2SO_4:H_2O_2:CH_3COOH (3:1:1) solution for 2 minutes the samples were analyzed using TEM. The results show considerably less etch figures in the gettered sample.

SIMS was used to determine the effect of gettering on Cr redistribution during the epitaxial growth. SIMS profiles of the Cr concentration in VPE layers on both gettered and control substrates were obtained. The results show that Cr has outdiffused rapidly during deposition in layers grown on both gettered and control substrates. However, the level of outdiffused Cr is significantly higher for the epitaxial layer on a control substrate.

In another study, Magee, et al explored the possibility of performing back-surface gettering with a highly desirable low temperature anneal. They found that although this is possible,it requires long annealing periods [22].

Studies have also been done on gettering into I^2 damaged regions. Bozler et. al.

reported the first work done on ion implantation damage gettering in GaAs. Si and Ne implantations were made into the polished face of SI Cr-doped samples. The depth of damage was estimated to be 1 μm for Ne^+ and 0.6 μm for Si^+. After the implantations, the samples were overcoated with Si_3N_4 on the polished face and SiO_2 on the front and backsides. These were then annealed at 750°C for 16 hours in flowing nitrogen. The encapsulants were removed following the anneals and the samples were subsequently etched in 5:1:1 H_2SO_4:H_2O_2:H_2O for one minute to remove the ion-implantation damaged layer. Epitaxial growth was then performed on gettered as well as control substrates [4].

A C-V technique was used to determine impurity profiles of the epilayers grown on both gettered as well as control substrates. The profiles show that the electron concentration in the epilayer on the control sample decreases with distance from the surface. The profiles of the ion-implantation damaged wafers are flat. The first result was thought to be due to the outdiffusion of compensating impurities or defects from the substrate. The flat profile of the epilayers on the I^2-damaged samples can be explained by the gettering of the impurities into the damaged regions.

An interesting study on Cr gettering from SI GaAs involves the creation of damage on the sample surface by the alloying of Au layers. Magee et al. reported the first work on the effect of contact alloying on the redistribution of Cr at annealing temperatures in the range 350-370°C. Cr-doped GaAs substrates and Sn-doped LPE layers grown on SI substrates were used in the study. Gold films were vapor deposited on the samples at room temperature on precleaned samples at vacuum levels < 10^{-8} Torr. The samples were then annealed at 350°C in a flowing H_2 environment [23].

TEM analyses were made on alloyed annealed as well as alloyed but unannealed samples. For this analysis, layers were then removed and the samples etched in H_2SO_4

:H_2O_2 :CH_3COOH (3:1:1) solution for 2 minutes. The analyses revealed a complex array of dislocations in the form of nests and tangles in alloyed and annealed samples. In contrast, no such arrays were found in control substrates or in unannealed Au/GaAs structures. The amount of damage was proportional to the annealing time. It was also found that the defect density induced by alloying is directly proportional to the initial film thickness.

SIMS profiling was done on the samples without the removal of the alloyed film. The results show that the Au has diffused into the GaAs substrate. They also showed that Cr piled up near the surface within the region into which the Au has penetrated. These results suggest that the alloying of Au films on SI GaAs substrates creates a damage-rich region within the GaAs lattice. This induced damage can serve as an effective gettering region for Cr.

Simple thermal annealing without mechanical damage or I^2-induced damage can also be an effective gettering technique. S.C. Palmateer et al. used heat treatment in H_2 ambient to getter Mn into the frontside of Cr-doped SI GaAs substrates. The Br_2/methanol polished samples were ultrasonically cleaned (TCE, acetone, methanol, DI water) and etched (10:1:1) (H_2SO_4:H_2O_2:H_2O). They were then cleaved into two halves. One half served as the control and the other was loaded vertically into a slotted graphite block in a furnace (quartz tube). These latter samples were baked for 24 hours in H_2 at 750^oC [3].

Heat treated and non-heat treated samples were then ultrasonically cleaned and etched in (10:1:1) H_2SO_4:H_2O:H_2O. These were then loaded for epitaxial growth by Molecular Beam Epitaxy (MBE). The epitaxial layers were then studied using SIMS, C-V profiling and DLTS.

C-V profiling was performed to determine free carrier densities in the epilayers.

The results of such analysis showed rapidly decreasing electron densities toward the epilayer-substrate interface for the non-heat treated samples. This was interpreted to be due to the outdiffusion of Mn into the epilayer during growth. On the other hand, epilayers grown on heat-treated-polished samples showed uniform free carrier profile from substrate to epilayer.

The SIMS analyses indicate that epilayers on non-heat treated substrates show a build up of Mn at the substrate-epilayer interface. The layers grown on heated/polished substrates show that the Mn interface build-up and surface accumulation was eliminated by the prebake/polish procedure.

DLTS measurements show a reduction of deep level hole concentrations by a factor of 2-3 in layers grown on heated/polished substrates.

As already mentioned in Section A of this Chapter, there seems to be a considerable number of studies on the behavior of impurities in InP during thermal annealing. Most of the studies focus only on the thermal redistribution of the various impurities. Removal of the surface-segregated impurities and subsequent epitaxial growth to determine the effect of the gettering technique on the outdiffusion of impurities during growth were not part of the experiments. A few studies which take the latter problem into consideration are presented below.

D.E. Holmes and R.G. Wilson investigated the behaviour of Fe in SI InP substrates during growth by LPE. They used SIMS and PL measurements to study the redistribution of Fe. A number of the substrates were preheated for 2 minutes at 650^{o}C before the growth which proceeded at temperatures within the range 580-720^{o}C. Some of them were heated up to 40 minutes to enhance redistribution effects. These latter samples were not used for growth but were analyzed for the effects of the preheat. SIMS measurements on these samples revealed an accumulation from 0.1 to 0.2 μm and a

depletion region up to about 0.6 μm. The surface accumulation was verified qualitatively by PL measurements. The intensity of the 0.35 eV PL peak associated with Fe was measured before and after several micrometers were removed from the surface by etching. The peak intensity was generally lower for the etched samples than for unetched samples. Very little accumulation was indicated by SIMS profiles of unheated samples [12].

SIMS measurements were also done on the epilayers grown on preheated, non-solution etched and preheated, solution-etched substrates. The results indicate greater outdiffusion of Fe into epilayers during growth for heated, unetched substrates. The study also showed that preheating substrates at 700-697°C for 10 minutes and subsequently etching them leads to less outdiffusion of Fe during growth compared to preheating temperatures of 599-591° C for 90 minutes.

CHAPTER III

CHARACTERIZATION PROCEDURE

A. Characterization of As-received Substrates

To determine the relative purity of the substrates prior to gettering, the Hall effect measurement was performed. The van der Pauw technique was used to measure the sheet resistance and Hall effect. A detailed discussion of this technique is found in reference [28]. Figure 1 shows the diagram of the measurement system.

Ohmic contacts were made by soldering indium onto the semi-insulating substrate using an ultrasonic bonder. The contacts were placed on the four corners of the square samples ~6 mm on a side.

An optical microscope was used to examine surface morphologies of samples at certain points during the processing. It was used to determine the surface quality of the as-received substrate, the frontside of the annealed substrate and front-and backsurfaces of the indium-alloyed substrate and that of the epilayers.

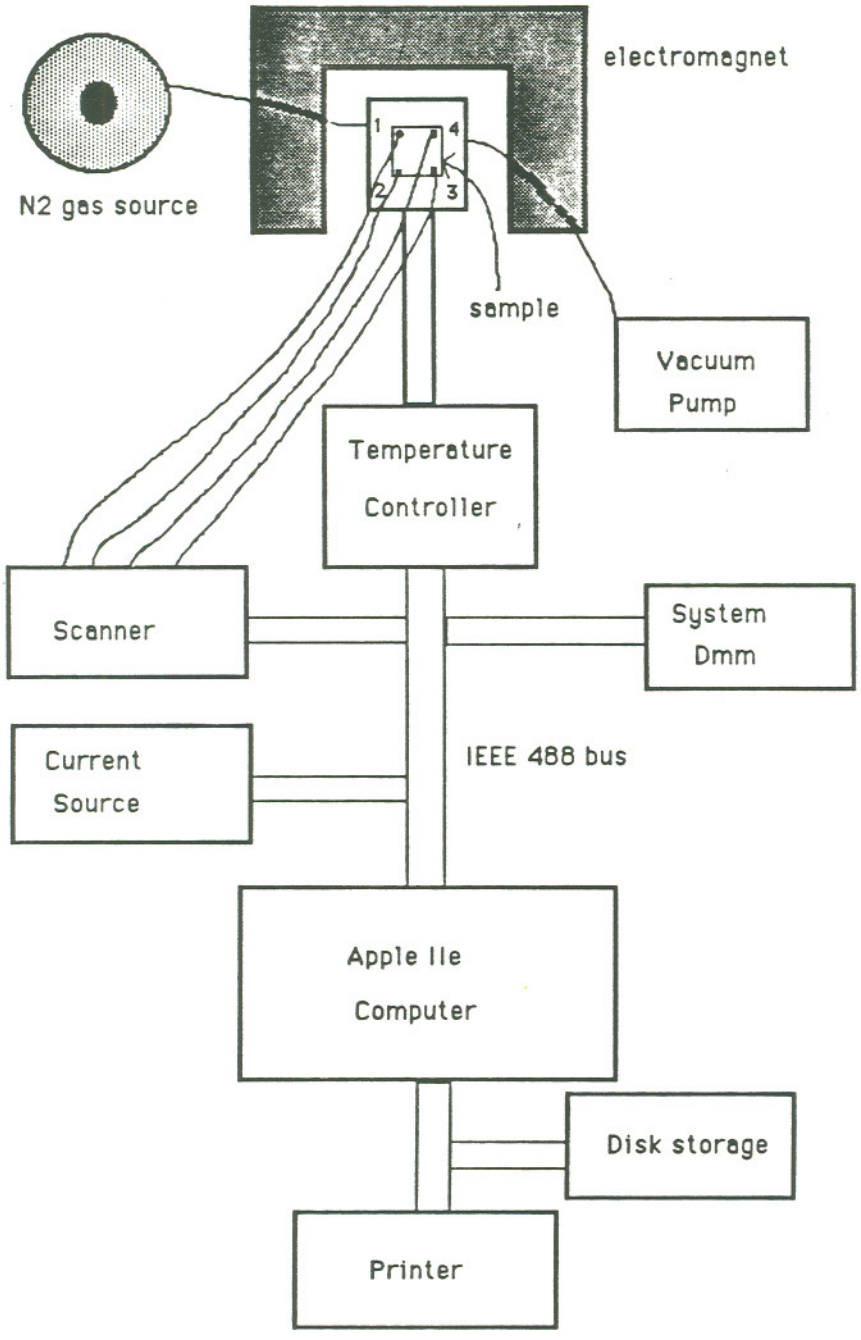

Figure 1. Schematic of the Hall Effect System

B.Growth of Epilayers

Organometallic Vapor Phase Epitaxy (OMVPE) was used to prepare the epitaxial samples. The system is a TMIn (trimethylIndium) , atmospheric pressure, commercial CSI reactor described in detail in Ref. [28]. Undoped InP layers 0.5 μm thick were grown on the SI substrates. Three samples, one as-received, one annealed and one In-alloyed were loaded into the OMVPE system in one growth run. Thus, all three samples were subjected to the same growth conditions. The growth conditions are summarized below:

$T = 600^{o}C$,

$H_2 = 4$ L/min,

$PH_3 = 296$ cc/min,

TMIn = 203 cc/min,

t = 1 hr.

These parameter values were found to be optimum for the growth of InP homoepitaxy by previous studies using the OGC OMVPE system [28].

C. Characterization of Epilayer

The Hall effect measurement was performed on the epilayers over the temperature range 80-350^{o}K. Ohmic contacts were formed by evaporating Au-Ge onto the epilayers. A mask with circular holes approximately 0.8 mm in diameter arranged in a square pattern was used. Within the evaporator, the sample was held at about 4 cm above the Au-Ge source. The evaporation was carried out at a vacuum level of around $5x10^{-6}$ Torr. Subsequent annealing was done in an argon ambient at T=350^{o}C for one minute. Indium was then soldered onto the contacts with wires connected to the In solder. The quality of the contacts were examined using a Tektronix 370 programmable curve tracer.

In addition to resistivity, mobility, Hall coefficient and carrier concentration, compensation ratios were also determined from Hall data. The derivation of the compensation ratios from Hall data can be done in two ways: (1) using carrier concentration versus temperature data and (2) by the mobility versus temperature analysis. Analysis of the temperature variation of carrier concentration is not reliable for determining N_A and N_D for samples which do not have sufficient carrier freeze-out or which have significant impurity band conduction over most of the temperature range considered [29]. Examination of the Hall data for the epilayers showed insufficient carrier freeze-out and low room temperature mobilities. This implies the use of the mobility analysis method.

The mobility analysis method consists of estimating N_A and N_D from the Brooks-Herring mobility formula for ionized impurity scattering. This requires that one

must choose a temperature at which the contribution of lattice scattering to the overall mobility is negligible. Hall data (i.e. mobility and carrier concentration) at 77°K can be used to a reasonable approximation.

The Brooks-Herring equation for the ionized impurity scattering mobility is given by:

$$\mu_I = \frac{3.28 \times 10^{15} \left(m/m^*\right) \varepsilon_o^2 T^{3/2}}{(2N_A + n)\left\{\ln(b+1) - b/(b+1)\right\}} \text{ cm}^2 \text{V}^{-1}\text{sec}^{-1} \qquad (1)$$

where

$$b = \frac{1.29 \times 10^{14} \left(m^*/m\right) \varepsilon_o T^2}{n^*}$$

and n^* is an effective screening density given by

$$n^* = n + \frac{(n + N_A)(N_D - N_A - n)}{N_D}$$

Assuming that donor deionization does not occur, $n=N_D-N_A$ and $n^* = n$. Thus equation (1) can be used to determine N_A directly from known n and μ_I at a given temperature. N_D can be determined from the relation $n=N_D-N_A$. From these, the compensation ratio N_A/N_D can be computed.

Photoluminescence was performed on the epilayers at 80^oK to determine the effects of gettering. The measurements were conducted using a slightly different configuration from that used in Ref.[28]. The excitation was provided by a Kr-Ar ion laser (4579-6471A) and the luminescence analyzed by a Jarrel-Ash monochromator. It was detected by a Si detector coupled to a conventional lock-in amplifier system. Input and output slit widths of the monochromator were kept at 1.5 mm since it results in maximum output intensity [28].

The sample was mounted using cryo-con grease on the low temperature pad of an MMR cryostat which cooled the sample to 80^oK using an N_2 gas supply. The laser beam was always focussed near the center of the sample to avoid edge effects. Figure 2 is a schematic of the PL system.

Alignment of the laser was done for each run using the visible emission from an AlGaAs sample. The intensity of the PL spectra for the InP were also normalized with respect to the band-edge peak of this AlGaAs sample.

Intensities of the band-edge peaks normalized with respect to that of the AlGaAs sample were compared.

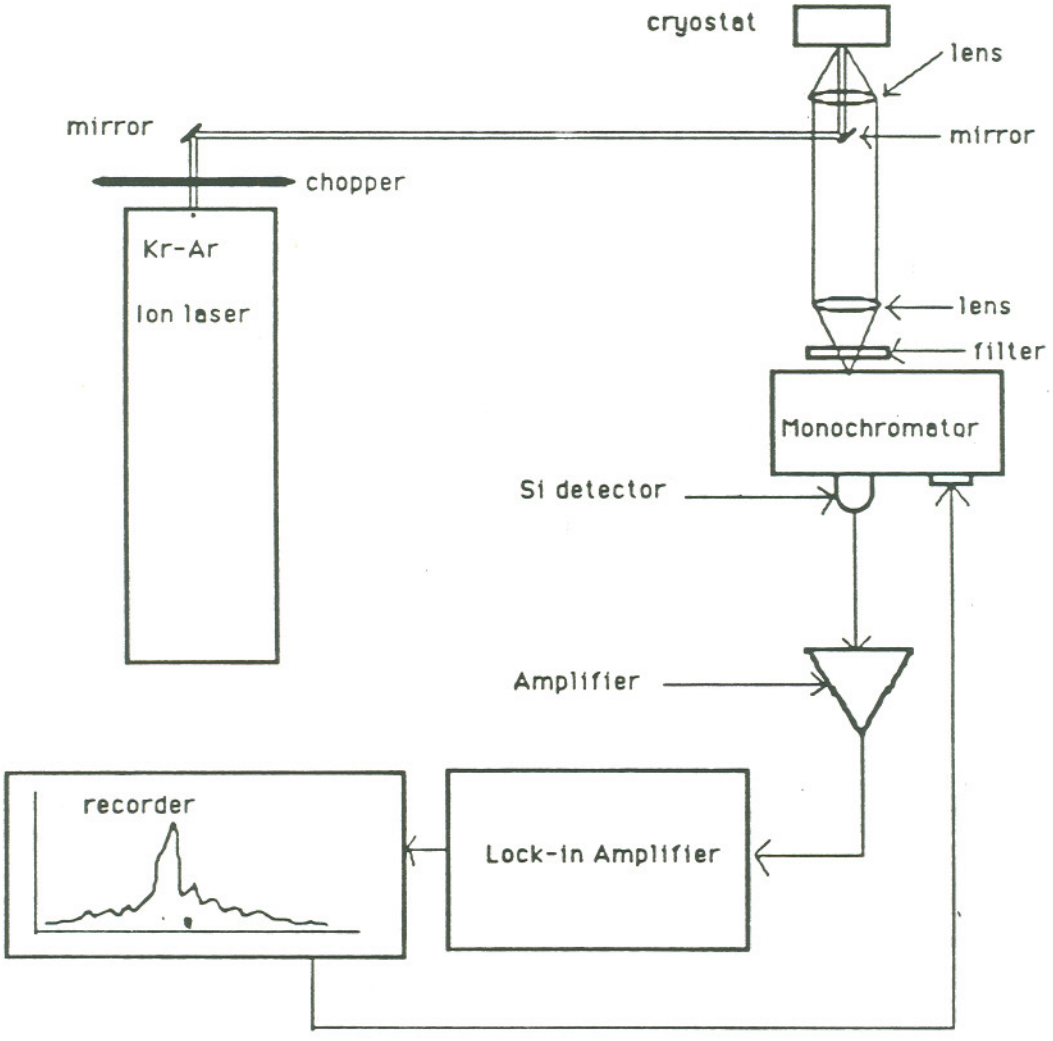

Fig. 2: Schematic of the Photoluminescence system

CHAPTER IV

GETTERING PROCEDURE

Two gettering techniques were explored in this study: simple annealing and backside-alloying with indium. Annealing was chosen because once the optimum conditions are determined, the processing steps are easy to carry out. The use of backside alloying with In was motivated by the successful gettering of impurities into polysilicon deposited on the backside of Si wafers [19].

Three samples cleaved from the same wafer were used in the experiment. One served as the control sample and two were prepared for gettering by simple annealing and In-alloying. The control substrate did not undergo any other pregrowth processing except for the etching which is done on any substrate before growth.

A. Simple Annealing

Optimum conditions for annealing depend largely on the purity of the sample. Since the purity of the semiconductor samples is difficult to reproduce, there is a need to determine the optimum annealing conditions for each sample.

Optimization of annealing parameters can be carried out in two ways. First, one can use the solution to the diffusion equation for the diffusion of the particular impurity from the sample. This approach, however, is rather involved. It requires careful modeling of the diffusion process. As in Jordan's model for the outdiffusion of Mn in GaAs (refer to Appendix I) the approach involves analysis of the defect chemical reaction through which an impurity atom alternately hops from an interstitial position to a substitutional site within the crystal. It then requires incorporation of additional terms

(pertaining to the kinetics of the defect chemical reaction) to the diffusion equation [26].

The second approach builds upon results of previous gettering experiments and is thus an experimental approach. This approach was used in this study. Trial anneals were done to determine the optimum temperature, duration and composition of the ambient. After each trial anneal, ocular or microscopic examination of the surface and PL were performed to detect any changes in the substrate surfaces.

In previous studies of annealing of SI InP substrates, the anneals were carried out either below 700°C for 6-24 hrs in H_2, H_2-Ar and PH_3 or at 700-750°C either in PH_3+H_2 or in H_2-Ar ambient (refer to Sec. A, Chapter 2).

Three trial anneals were done on InP test samples. All of them avoided the lengthy thermal treatment of the previous studies mentioned above. The result of the anneals are summarized in Table 2

Table 2: Result of trial anneals

Test Sample	T (C)	t (hr)	Ambient	Result/s
undoped InP	750	2	0.1% $PH_3 + H_2$	Severe pitting on frontside
InP:S (n^+)	750	2	1% PH_3+H_2	No visual change on polished surface; PL spectrum unchanged
InP:S (n+)	750	0.5	1% PH_3+H_2	No visual change in polished surface; FWHM of band edge peak reduced by 40%

Severe damage of the frontside must be avoided since any damage on the substrate is propagated into the epilayer. This disqualifies the parameters for trial 1. In trials 2 and 3, the surfaces remained polished. However, for sample 3, there was a 40% reduction in the FWHM of the band-edge peak compared to that of the unannealed substrate. This represents a change in the doping density of the sample. This effect is not desirable since doping densities of substrates are usually formulated for the specific device application of the material. The parameters of trial 2 were therefore deemed to be the most desirable.

The SI InP samples used in the actual experiments were commercial-grown by ICI Americas and DOWA Mining Co. The electrical properties of the samples at room temperature are shown in Table 3.

Table 3: Electrical Properties of Substrates used in the Study

	ICI Americas	DOWA Mining Co.
ρ (Ω-cm)	1.752×10^7	5.390×10^7
n (cm^{-3})	2.748×10^8	7.375×10^7
μ (cm^2/V-s)	1534	1862
Orientation	(100)	(100)
Dopant	Fe	Fe
Conductivity type	n	n

Two samples from each wafer were annealed at 750°C for 2 hrs in 1% $PH_3 + H_2$.

The phosphorus in the ambient is intended to prevent rapid deterioration of the substrate surface which would be detrimental to subsequent epitaxial growth. The anneals were performed in the CSI 325 OMVPE reactor at OGC.Details of this reactor are given in [28]. Figure 3 shows the annealing set-up in the reactor tube.

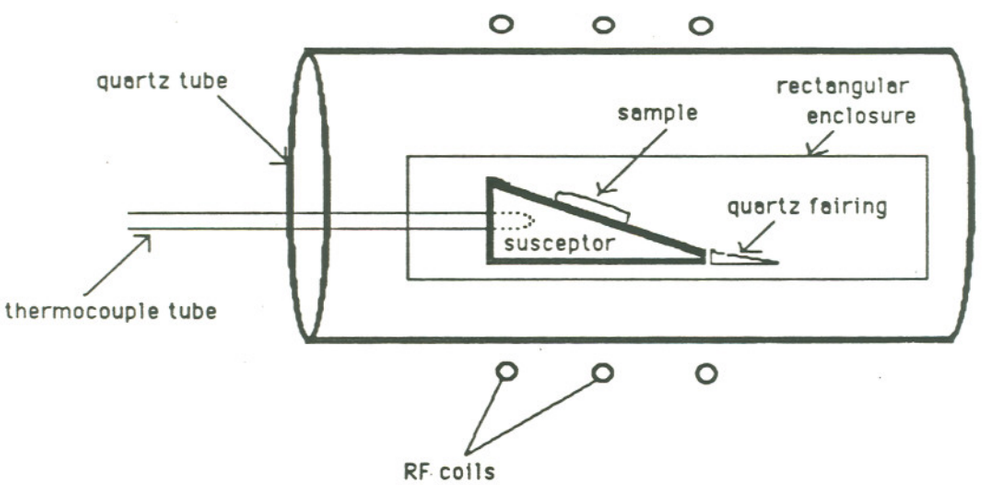

Figure 3: Annealing set-up in the CSI 325 OMVPE reactor tube

CHAPTER V

RESULTS AND DISCUSSION

A. Hall Data Analysis

Room temperature Hall effect measurements are the easiest to perform and the data can provide a quick assessment of the quality of the epilayers. In addition, room temperature data are valuable since most devices operate at room temperature. The room temperature Hall data for the epilayers on the ICI substrates are shown in Table 4.

All epilayers are n-type as indicated by negative Hall coefficients. The epilayer on the In-alloyed sample has the highest room temperature mobility. The carrier concentration of this sample is the highest and its resistivity lowest among the three samples. This would lead one to say that the In-alloyed sample has the best quality at room temperature. It is necessary, however, to look at the temperature scanned Hall data and PL measurements to be able to make conclusive statements regarding the purity of the samples.

Table 4: Room Temperature Hall Data for Epilayers on ICI Substrates

Sample	Resistivity (Ω-cm)	Mobility (cm^2/V-s)	Carrier Type	Carrier Concentration (cm^{-3})
ASR	7.422	543	n	1.546×10^{15}
ANN	17.19	408	n	8.882×10^{14}
INA	0 .1189	1344	n	3.904×10^{16}

ASR - Epilayer on as-received substrate
ANN - Epilayer on annealed substrate
INA - Epilayer on In-alloyed substrate

Figures 4 and 5 show the temperature dependence of the mobility and carrier concentration respectively of the three epilayers. Note that the mobility of the epilayer on the In-alloyed substrate decreases monotonically with increasing temperature. However, this is not true for the epilayers on the as-received and annealed substrates. From liquid nitrogen temperatures, the mobilities of both epilayers rapidly plunge downwards at the 180-200^{o}C temperature range and then increase thereafter. For the epilayer on the as-received sample, the mobility decreases again after increasing at 200^{o}C from whence it shows very little variation

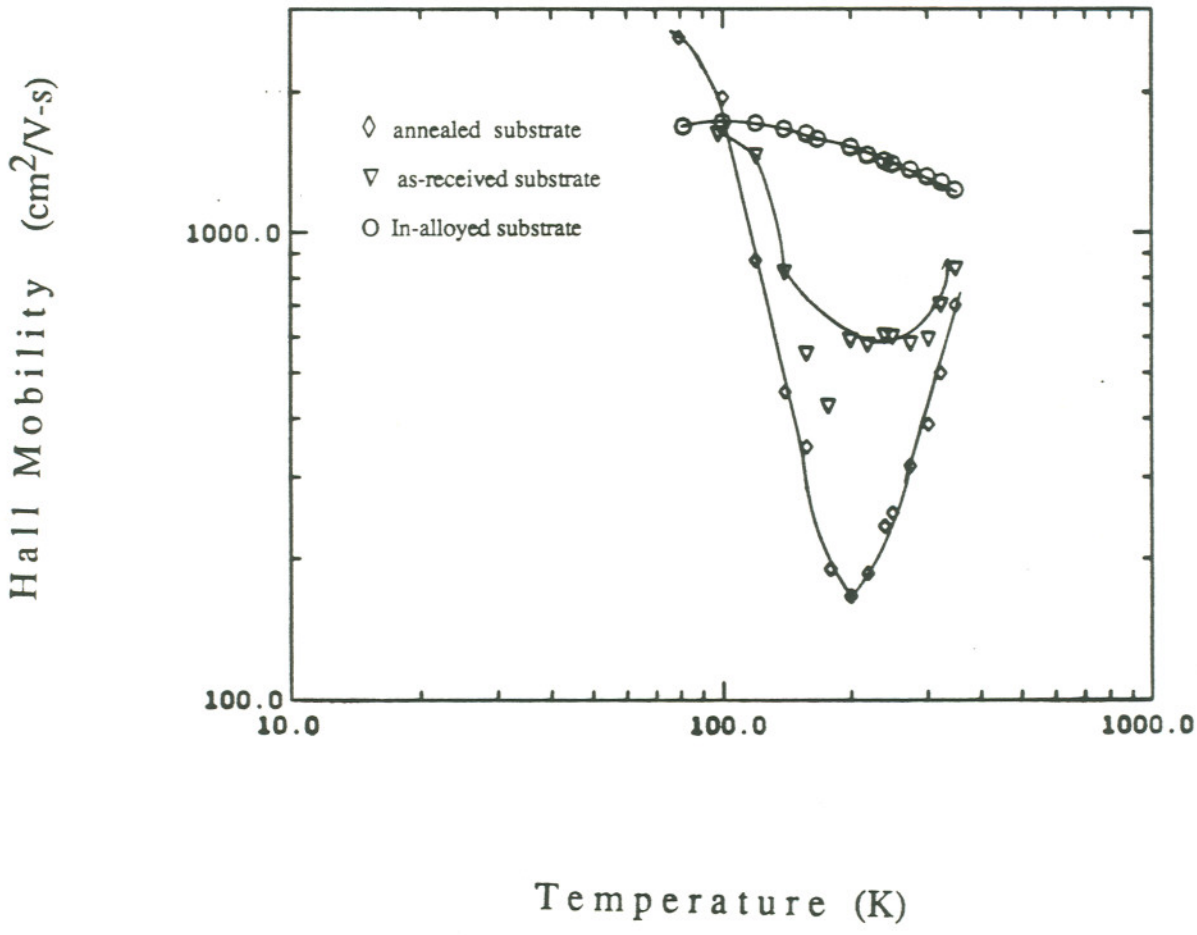

Fig. 4 : Temperature Dependence of the Hall Mobility for Epilayers on ICI Substrates

until it resumes its upward climb at around 250°C.

The compensation ratios obtained for the three samples are shown in Table 5.

Table 5 : Compensation Ratios for Epilayers on ICI Substrates

Epilayer on	Compensation Ratio
as-received substrate	0.896
annealed "	0.917
In-alloyed "	0.865

The In-alloyed sample has the least compensation ratio while the annealed sample has the highest value.

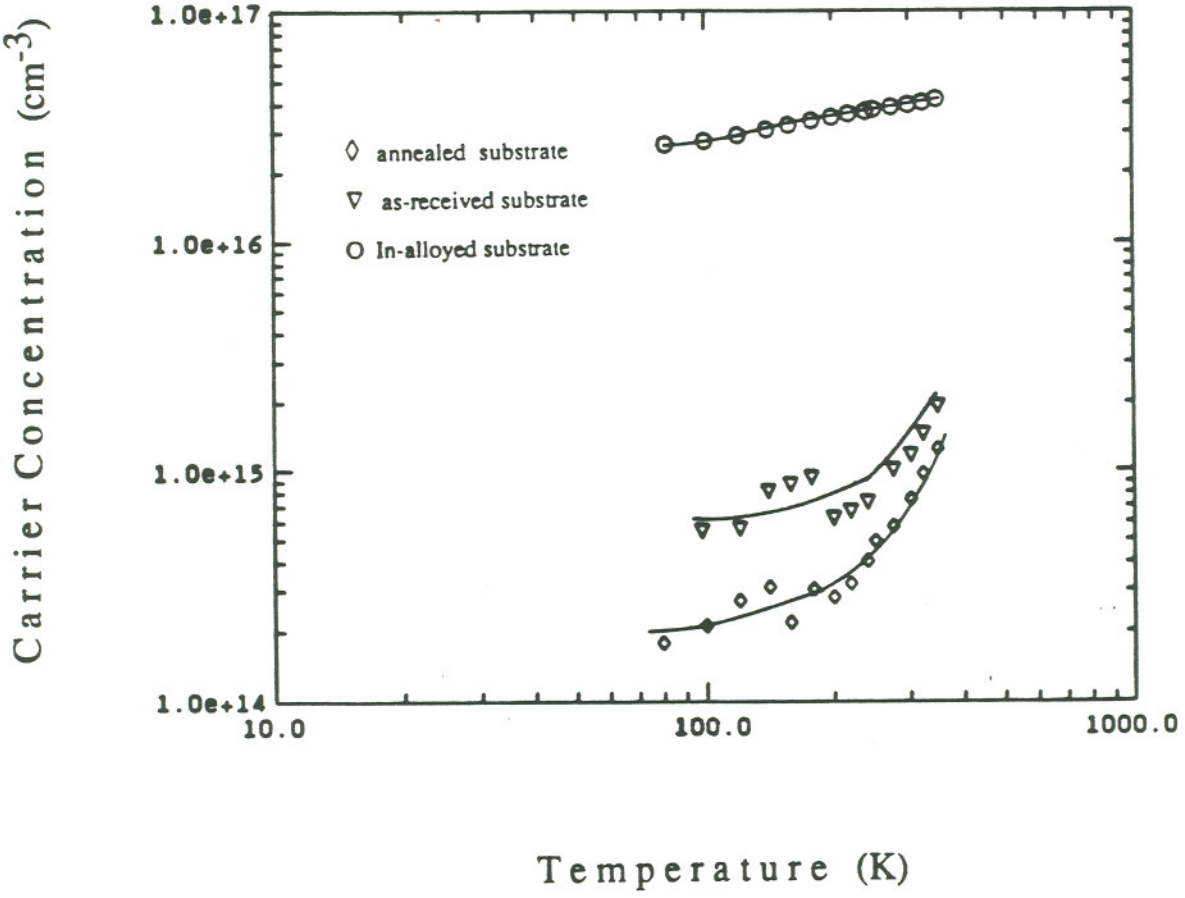

Fig. 5 : Carrier Concentration versus Temperature plot for Epilayers on ICI Substrates

Table 6 shows the room temperature Hall data for the epilayers on DOWA substrates. Note that the as-received sample has the highest room temperature mobility. However, this mobility value is not significantly greater than that of the annealed substrate. Nevertheless, as compared to Table 4, the epilayer on the as-received DOWA substrate has a higher mobility compared to that on the as-received ICI substrate.For the DOWA samples, the carrier concentration of the as-received sample is higher than the annealed sample although it is lower than the In-alloyed sample.

Table 6 :Room Temperature Hall Data for Epilayers on DOWA Substrates

Sample	Resistivity (Ω-cm)	Mobility (cm^2/V-s)	Carrier Type	Carrier Concentration (cm^{-3})
ASR	0.5676	1565	n	7.027×10^{15}
ANN	0.7751	1507	n	5.342×10^{15}
INA	0.4058	1203	n	1.278×10^{16}

Again all epilayers are n-type as indicated by negative Hall coefficients. Figures 6 and 7 show the Hall mobility and carrier concentration versus temperature plots for the three epilayers. Table 7 shows the compensation ratios computed for the three samples.

Table 7 : Compensation Ratios for Epilayers on DOWA Substrates

Sample	Compensation Ratio
ASR	0.500
ANN	0.633
INA	0.958

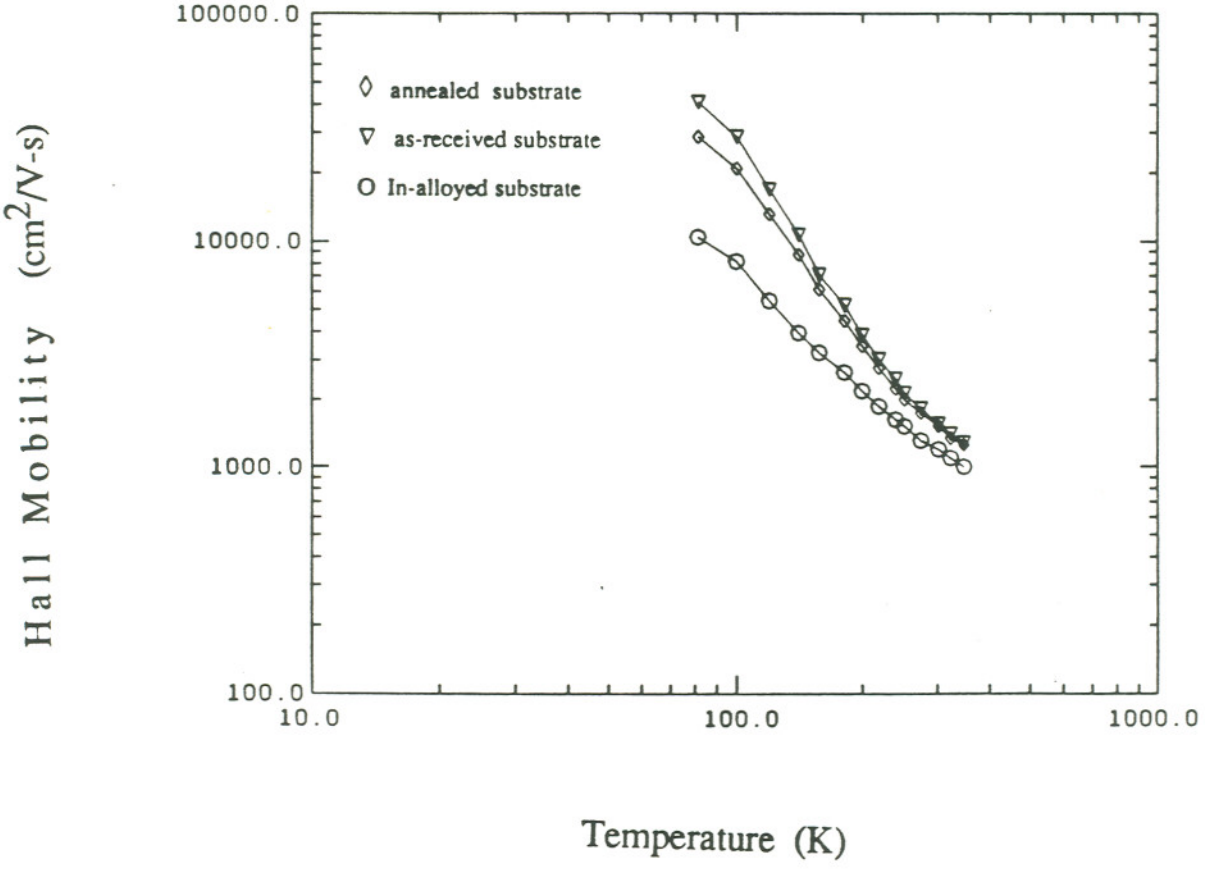

Fig. 6 : Mobility versus Temperature plot for Epilayers on DOWA Substrates

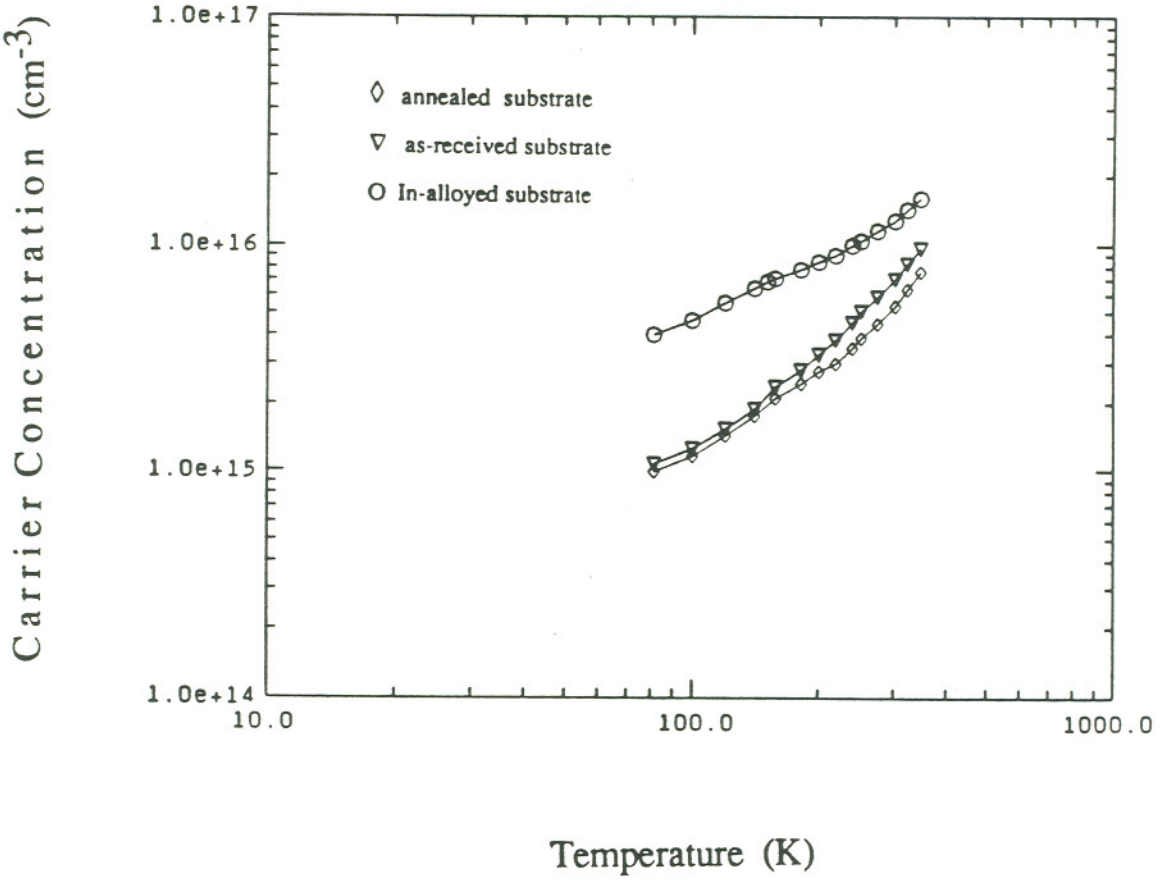

Fig.7 : Carrier Concentration versus Temperature Plot for Epilayers on DOWA substrate

B. Discussion of Hall Data Analysis

For the epilayers on ICI substrates, the temperature variation of mobility for the annealed and as-received samples is uncommon and has stimulated much thought on the part of the author. A reasonable explanation would be related to changes in two depletion regions in the epilayer. One region is located in the vicinity of the metallurgical junction between the substrate and epilayer. The other is located near the surface and is due to a surface potential.

Depletion effects can pose as a major problem in Hall measurement [29,30,31,32]. Parallel conduction in the depletion regions can result in an overestimate of the carrier concentration. It can also lead to an underestimate of the mobility since the mobility in the space charge region is most likely lower than the rest of the epilayer.

Lepkowski et al. [32] studied the temperature variation of the surface and interface depletion widths for GaAs grown on SI substrates and found that the depletion widths decrease with increasing temperature. This suggests then that it is possible to observe an increase in mobility as temperature increases for similar samples. This explains the rise in mobility in the temperature range from 200-350^{o}C.

Another possible explanation is the inhomogeniety of the epilayers. Anomalously high mobilities have been observed in compound semiconductors which were grown under metal-rich conditions and which may have metallic inclusions or precipitates [33]. A metallic inclusion has a greater conductivity and thus mobility than the medium. This raises the effective mobility of the layer.

Lepkowski, et al. [32] proposed a method to correct for surface and interface depletion effects in obtaining carrier concentrations and mobilities. However, this

method assumes fixed surface and interface potentials which may not be true for the variable temperature condition to which the low purity samples were subjected. Whitney and Uwai [35] proposed a second method which involved obtaining the difference between two successive Hall measurements one before and one after a controlled etch. However, this method is difficult to control for the very thin epilayers in this study.

Because corrections could not be made for the depletion and inhomogeneity effects, the mobility and carrier concentration values obtained may not reflect the real values for the as-received and annealed samples. However, the mere presence of anomalous behavior which can be accounted for by these effects implies that the purity of these samples is inferior compared to the In-alloyed sample.

Furthermore, the temperature variation of the depletion widths is governed by the activity of impurities (whether these impurities are being ionized or deionized or in the case of traps, whether they are trapping free carriers or being emptied of trapped carriers in the temperature range considered). For the annealed and as-received samples, the depletion widths are sensitive to temperature variations. This suggests that the density of impurities in the depletion regions are greater for these samples compared to the In-alloyed sample.

The statement that the In-alloyed sample has the highest purity among the three samples is strengthened by the compensation ratios obtained. The ratios indicate that the In-alloyed sample is the least compensated. This means that this sample has the least acceptor impurity incorporation compared to the other two samples. Since the layers were grown in the same run, any differences in impurity incorporation could only be due to differences in the extent of outdiffusion from the substrate during growth. Because the In-alloyed sample has the least acceptor impurity incorporation, it must have the least

extent of outdiffusion. It follows that the In-alloying was effective in gettering acceptor impurities from the substrate before the growth.

Simple annealing seems to have degraded the epilayer quality instead of improving it. This is indicated by electron mobility which is the lowest among the three samples.

For epilayers on DOWA substrates, note that the as-received sample has the highest Hall mobility throughout the temperature range 80-350^{o}K. Also, note the absence of anomalous temperature behavior of the mobility for all samples. This may mean that the amount of inhomogeneities in these samples is less than that of the epilayers on ICI substrates. It may also mean combined impurity and depletion effects is less compared to the ICI samples. Also, note that the as-received sample has the lowest compensation ratio while the In-alloyed sample has the highest. This implies that the as-received sample is the purest while the In-alloyed one the least pure among the three.

If mobility and compensation ratios are used as indicators of purity, the results then consistently suggest that the as-received sample is the purest among the three. This means that In-alloying was, this time, not effective in removing impurities from the substrates before growth. Instead it has resulted in a poorer quality epilayer.

C. Photoluminescence Analysis

Figure 8 shows the PL spectra of the epilayers on ICI substrates. Note that the intensity of the band-edge peak of the epilayer on the In-alloyed substrate is significantly higher than those on as-received or annealed substrates. This means that the In-alloyed sample has the highest PL efficiency.

PL efficiency increases with increasing probability of radiative recombination and decreases with increasing probability of non-radiative recombination. One would then conclude that the In-alloyed sample has the highest radiative recombination and lowest non-radiative recombination probability. It follows that the other two samples have lower radiative recombination and higher non-radiative recombination probability.

Figure 9 gives the PL spectra for the epilayers on DOWA substrates. The spectra show again that the as-received sample has the highest intensity of the band-edge peak suggesting the highest PL efficiency among the three. The In-alloyed sample has the lowest band-edge peak intensity and thus lowest PL efficiency. Using the arguments mentioned for the ICI samples, these results would then imply greater amount of defects and/or impurities for the annealed and In-alloyed samples compared to the as-received sample.

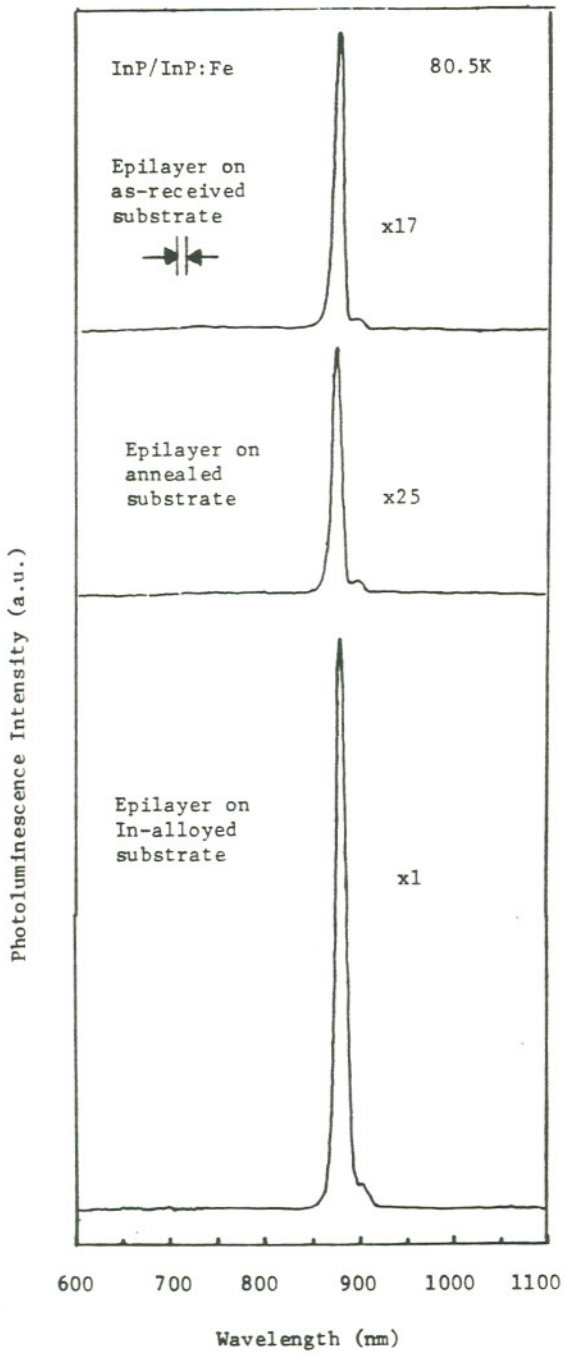

Fig. 8: PL Spectra of the Epilayers on ICI Substrates

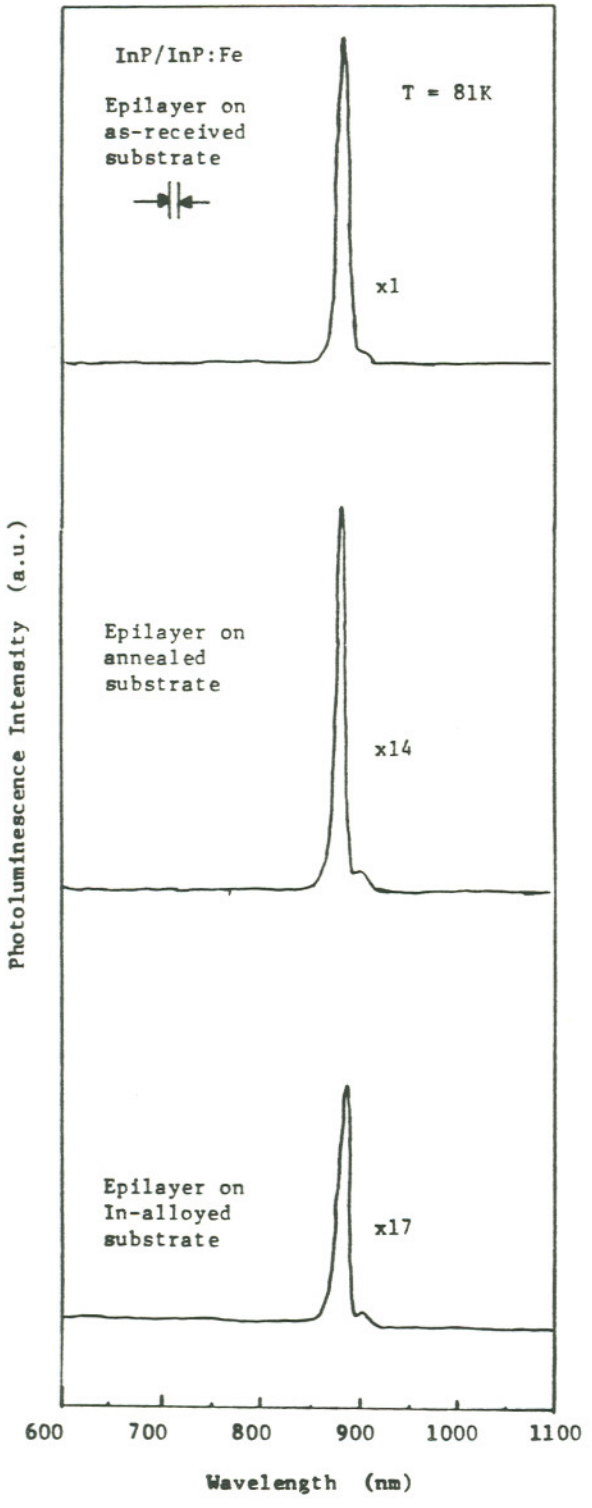

Fig. 9 : PL Spectra of Epilayers on DOWA Substrates

D.Discussion of Photoluminescence Analysis

The results for the epilayers on ICI substrates are of great interest and can be of considerable value in InP technology. High luminescence efficiency is required by devices such as LED's and laser diodes. In-alloying can be developed in InP technology as an effective technique for the gettering of low purity substrates for optoelectronic devices. The development of the technique, however, requires a good understanding of recombination processes in semiconductors. In the following discussion, the PL results for the ICI samples are explained in terms of recombination phenomena.

Non-radiative recombination can occur via (1) Auger recombination (2) surface recombination and (3) recombination through impurities or defects [42]. The probability of Auger recombination is significant only for highly doped samples. For these samples the probability of carrier-carrier interaction is high. Since the samples of the study have carrier concentrations in the range 10^{14}-10^{16} cm^{-3} the probability of Auger recombination is insignificant. The three epilayers were grown in the same run and the surfaces went through the same processing. Thus, to a reasonable extent, the surface states are similar.This reduces the possiblity of surface recombination producing differences in PL efficiencies.

This leaves us with just one more mechanism to explain the differences in the PL efficiencies - non-radiative recombination via impurities or defects.

The results then indicate that non-radiative recombination via impurities and/or defects is more probable in the as-received and annealed samples. This can mean that the concentration of impurities or defects is greater for these samples.

Determination of transition probabilities is a quantum mechanical problem and is

rather involved. The probability of a given recombination process is determined by a host of factors. Thus the presence of an impurity does not always lead to enhancement of non-radiative recombination and suppression of radiative transitions. But considering the electrical measurements presented earlier, the above statements regarding the purity of the three samples suggested by the PL measurements may indeed be plausible.

The above discussion implies that the PL results are consistent with those for the Hall data. This strengthens the observation that the epilayer on the In-alloyed ICI substrate has the highest purity. It also reiterates the statement that In-alloying was effective in gettering impurities from the substrate prior to growth.

It is interesting to note that the epilayer on the annealed ICI sample has the lowest PL efficiency. This indicates that this sample has the lowest purity among the three. It also supports the observation made earlier that annealing seems to have degraded the epilayer quality. However, this does not necessarily mean that simple annealing cannot be effective as a gettering technique. It is possible that the annealing parameters were not optimized. It is also possible that the accumulated impurities were not completely etched off before growth. Thus, instead of minimizing outdiffusion of impurities during growth, annealing has, in fact aggravated it.

E. Discussion of ICI versus DOWA Results

Why In-alloying was effective for ICI and not for DOWA samples is an interesting question to answer. Possible explanations can be presented to account for this result. The DOWA substrate has greater mobility compared to the ICI substrate. This may mean that the ICI substrate has a greater density of residual acceptor impurities compared to the DOWA substrates. It is established that diffusivity is concentration dependent. For example, it is well-known that the diffusion coefficient of Zn in GaAs increases with Zn concentration. If we assume this to be true for the acceptor impurities in the substrates used in the study, then the diffusivity of these impurities is greater for the ICI substrate. This may mean more effective gettering of impurities for this substrate since gettering into the damage-rich region requires diffusion over long distances within the bulk into the vicinity of the surface. Using the same argument, acceptor impurities in the DOWA substrates have less diffusivity compared to those of the ICI substrates. This implies slower diffusion which reduces the effectiveness of the gettering process.

A second explanation is related to the surface saturation limit for outdiffusing impurities. The maximum concentration of impurities which can accumulate at the surface is proportional to the maximum surface defect density in that region of the semiconductor. The DOWA wafer backside was polished while that of the ICI was not. Thus, the ICI wafer backside has a greater defect density compared to that of the DOWA. It follows that the In metal used for alloying has a greater diffusivity in the ICI compared to the DOWA sample. This means that the effective gettering region is larger for the ICI substrate implying better gettering for this sample.

Chapter VI

CONCLUSIONS

Gettering techniques - simple annealing and In-alloying - were performed on semi-insulating InP substrates to improve their purity for subsequent epitaxial growth. Efforts were made to optimize the gettering parameters for each technique.

Semi-insulating Fe-doped substrates from two manufacturers (ICI Americas, DOWA Mining Co.) were used in the study.The DOWA wafer was the higher purity substrate based on Hall data. Epilayers were grown on gettered and ungettered substrates for each sample. Hall and PL measurements were used to establish the effects of gettering.

The highest purity epilayer among the ICI samples was obtained by In-alloying the substrate prior to growth. This is indicated by room temperature mobility and PL efficiency which are significantly higher than those for epilayers on annealed or control substrates. It is deemed that this result can be of significant importance in InP technology. Further studies should be conducted to develop this gettering technique as a means of obtaining higher purity InP for optoelectronic applications.

The other results are as follows:

1. The epilayers on as-received and annealed ICI substrates exhibited anomalous mobility and carrier concentration versus temperature behavior. The In-alloyed sample did not exhibit this behavior. The anomalous temperature behavior of the mobilities and carrier concentrations of the as-received and annealed samples suggest inhomogeneity and impurity + depletion effects. This strengthens the conclusion made about the relative purity of the samples.

2. The epilayer on the annealed ICI substrate has the lowest room temperature mobility and carrier concentration. Thus annealing did not improve the quality of the epilayers. Instead, it resulted in the degradation of the epilayers -a result which can be attributed to incomplete etching of surface-accumulated impurities and/or unoptimized annealing parameters.
3. The epilayer on the as-received DOWA substrate had the highest room temperature mobility and PL efficiency compared to In-alloyed and annealed samples. None of the samples showed anomalous electrical behavior. Thus, In-alloying and annealing were not effective in improving the purity of the epilayers.

Why In-alloying did not result in higher purity epilayers in the case of the DOWA samples can be explained as follows:

1. The DOWA substrate has a higher mobility and thus lower density of residual impurities. This being so, the impurities have a lower diffusity which leads to less effective gettering in this substrate.
2. The ICI substrate had a greater density of defects at the backside compared to the DOWA substrate. Thus the diffusivity of the deposited In would be greater in the ICI sample. This suggests that the effective gettering region was larger for the ICI substrate resulting in more effective gettering for this substrate.

As in the case of the ICI samples, the lack of effectiveness of annealing in gettering of impurities in the DOWA substrates is thought to be due to incomplete etching of surface-segregated impurities and/or unoptimized annealing parameters.

Future studies on the same techniques should consider the following:

1. Annealing parameters must be carefully optimized. Ideally, this can be done by a combination of mathematical modeling of the outdiffusion problem and experimental techniques similar to the one used in this study.
2. Thicker layers should be grown on the gettered and ungettered substrates. This would prevent depletion effects from dominating and complicating electrical measurements. This would also enable the experimenter to correct for depletion effects using the Hall measurement based on differential profiling proposed by `Whitney and Uwai.

To summarize, this study has demonstrated the potential of indium-alloying as an InP substrate gettering technique for obtaining higher purity epilayers. However, its effectiveness is sensitive to initial density of both residual impurities and major dopants in the substrate. More studies must be done to fully develop this technique.Simple annealing failed to improve substrate quality. There is a need to optimize annealing parameters to increase effectiveness of this technique.

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APPENDIX I

A Theory of Outdiffusion in Semiconductors

In general, gettering involves diffusion of impurities into specific regions in a semiconductor. The problem at hand deals with the gettering of impurities into the semiconductor surface. Thus it requires a good theoretical basis for the outdiffusion of impurities from the bulk into the semiconductor surface.

A number of mechanisms have been presented to explain the outdiffusion of impurities in semiconductors. All of them are based on the idea that the movement of an impurity in a lattice is made up of a series of random jumps. In substitutional diffusion, impurity atoms wander through the crystal by jumping from one lattice site to the next thus substituting for the original host atom [24]. This requires the presence of a vacancy, however. At diffusion temperatures, the vacancies are entering from the surface and are generated from internal sites such as dislocations. The diffusion rate will depend, in this case, primarily on the vacancy concentration which, in turn, is a function of partial vapour pressures of the major constituents and the impurity content. The equilibrium concentration of vacancies is quite low. Thus one expects substitutional diffusion to be rather slow [25].

Another mechanism which is specially applicable to III-V compounds is the vacancy pair mechanism. In this case, the vacancies on two sublattices (metal vacancies and anion vacancies) may tend to associate together and form vacancy pairs. The impurity atoms may diffuse via these vacancy pairs. Vacancy pairs are said to be more mobile than simple vacancies. Their concentration is a function of temperature only and

cannot be altered by partial vapour pressures of the major constituents [25].

A mechanism in which diffusion occurs at a faster rate is the interstitial diffusion. Here impurity atoms move through the crystal lattice by jumping from one interstitial site to the next. However, pure interstitial diffusion is not a probable mode of diffusion at high temperatures. At these temperatures, interstitials interact with other defects [25].

Of special interest is an interstitial diffusion that occurs via a dissociative mechanism. In this case, impurity atoms occupy both substitutional and interstitial sites. The interstitial species, however, move more rapidly than the essentially immobile substitutionals. The dissociative mechanism by which a substitutional atom can become an interstitial is the controlling factor for this process [24].

The interstitial-substitutional diffusion mechanism just discussed was proposed by Frank and Turnbull in 1956 to explain the diffusion of Cu in Ge. The diffusion of Cu, Ni and Au in Si and of Zn, Cd and Cu in GaAs have been explained by this mechanism [26].

A deeper understanding of the process of outdiffusion in semiconductors calls for an analysis of the diffusion equation [27]. For simple diffusion in a concentration gradient where the diffusion coefficient is concentration independent, the diffusion equation is written as

$$\frac{\partial N}{\partial t} = D \frac{\partial^2 N}{\partial x^2} \qquad (2)$$

By applying the appropriate boundary conditions, one can generate a solution to this equation. The solution would give the distribution of the diffusing impurity in the

semiconductor.

Consider the case of outdiffusion from an originally homogeneous sample. Suppose the sample is doped to a level C_1 and is raised to a high temperature at t = 0. The dopant diffuses out and if it is pumped away so that no solute vapour collects near the specimen, the boundary conditions are:

$$N = 0 \qquad t > 0, x = 0$$

$$N = N_1 \qquad t = 0, x > 0$$

The solution is

$$N = N_1 \operatorname{erf} \frac{x}{2\sqrt{DT}} \tag{3}$$

Figure 10 shows the plot of equation (3). It is interesting to note that most of experimental data on thermal redistribution of impurities is semiconductors disagree with equation (3). This implies that outdiffusion processes in semiconductors are complicated. There is a need to consider many factors that affect the movement of impurity atoms during outdiffusion.

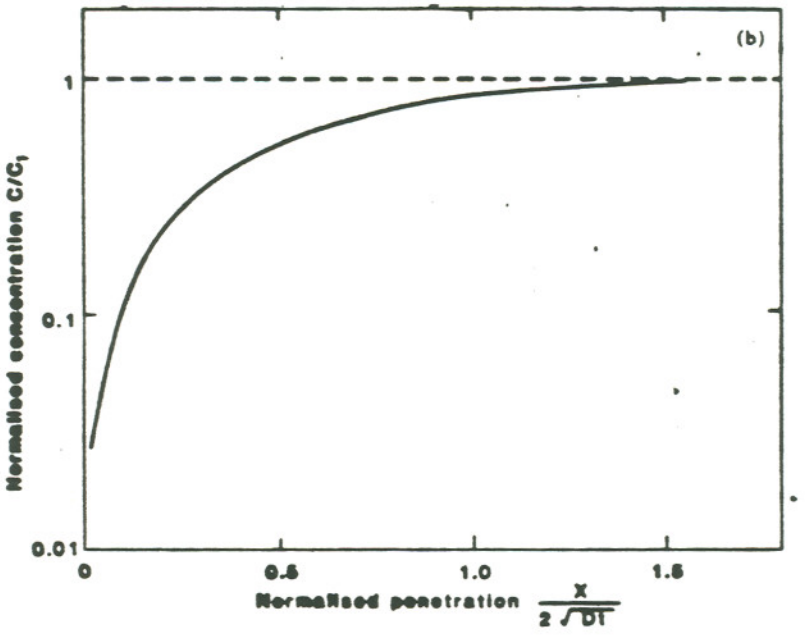

FIG. 10. Prediction for the depth profile of concentration of outdiffusing impurities. Taken from Tuck et.al.[15]

A.S. Jordan formulated a model that explains the "uphill" diffusion of Mn in GaAs [26]. His model used the interstitial-substitutional mechanism of Frank and Turnbull. It assumes that Mn atoms are distributed betweeen substitutional and interstitial sites. Diffusion takes place when a Mn interstitial is captured by a Ga vacancy. On the other hand, a Mn substitutional on a Ga site can undergo dissociation and end up in an interstitial position leaving behind a Ga vacancy. The interrelationship among these species can be represented by the following associative-dissociative defect chemical reaction:

$$V_{Ga} + Mn_i \rightleftharpoons Mn_{Ga} \qquad (4)$$

The corresponding rate equation is

$$\frac{\partial N_s}{\partial t} = k_2 N_v N_i - k_1 N_s \qquad (5)$$

N_s , N_i , N_v = concentrations of substitutionals, interstitials and vacancies respectively

k_1 , k_2 = rate constants for backward and forward reactions

Jordan assumed tht dislocations neither annihilate nor create vacancies. He used equation (5) as a sink term in the diffusion equations for Mn_i and V_{Ga}. These equations are

$$\frac{\partial N_i}{\partial t} + k_2 N_i N_v - k_1 N_s = D_i \frac{\partial^2 N_i}{\partial x^2} \qquad (6)$$

$$\frac{\partial N_{V^-}}{\partial t} + k_2 N_i N_v - k_1 N_s = D_v \frac{\partial^2 N_v}{\partial x^{26}} \qquad (7)$$

D_i , D_v = diffusion coefficients of Mn_i and V_{Ga} respectively

Jordan further introduced the following postulates:

1. During diffusion, the total amount of Mn in the wafer (thickness 2l) is conserved.
2. Since substitutionals have a greater solubility than interstitials, nearly all Mn atoms in the wafer exist as substitutionals before annealing. That is, at t=0 at any x, $N_{tot}=N_s$, $N_i = 0$ and $N_v =0$.
3. At the annealing temperature, the equilibrium vacancy concentration, N_v^o is reached instantaneously only at the surface.
4. In the center of the slice there is a deficit of vacancies. Hence $\partial N_s/\partial t = -k_1 N_s$ follows from the dominant backward reaction of equation (4).
5. The interstitials thus generated diffuse to the surface according to equation (6).
6. Near the surface, there is an abundance of vacancies. Thus the forward reaction in equation (4) is dominant. Therefore equation (6) becomes

$$\partial N_s/\partial t = k_2 N_v N_i \text{ and } N_s = k_2 \int_o^t N_i N_v \, dt + N_{tot} \qquad (8)$$

Jordan's main objective was to solve equation (8). The solution will give the desired distribution profile for the outdiffused Mn atoms that end up in substitutional

sites. Note that the key quantity in the approximate determination of N_s is the indiffusing N_v. In the absence of dissociation, which is insignificant near the surface, the term $k_1 N_s$ in equation (7) can be neglected. The boundary conditions from the postulates would then be

at $t = 0$, $N_v = 0$ for all x

for all t, $N_v = N_v^o$ at $x = 1$

or $N_v = N_v^o$ at $x = 1$

and $\partial N_v / \partial x = 0$ at $x = 0$

A Laplace transformation technique was used to derive the Ga-vacancy concentration from equation (7). The resulting solution is:

$$N_v = \frac{N_v^0}{2} \sum_{n=0}^{\infty} \left\{ \exp\left[-(2n+1)1 - x\right]\sqrt{B} \ \operatorname{erfc}\left[\frac{(2n+1)1 - x}{2\sqrt{D_v t}} - \sqrt{D_v B t}\right]\right\}$$

$$+ \sum_{n=0}^{\infty} \left\{ \exp\left[\left[(2n+1)1 - x\right]\sqrt{B}\right] \operatorname{erfc}\left[\frac{(2n+1)1 - x}{2\sqrt{D_v t}} + \sqrt{D_v t}\right]\right\}$$

$$+ \frac{N_v^o}{2}\left\{\text{expression as above but } '-x \leftrightarrow x\right\} \qquad (9)$$

where $B = k_2 N_i / D_v$

The interstitial concentration profile was derived to be:

$$N_i = N_{tot}\left(1 - e^{-k_1 t}\right) + N_{tot}\frac{4}{\pi}\sum_{n=0}^{\infty}\frac{-1}{2n+1}\cos\frac{(2n+1)\pi(1-x)}{2l}$$

$$x\left[\frac{k_1\tau}{(2n+1)^2} + \left(\frac{k_1\tau}{(2n+1)^2}\right)^2 + ..\right]\left\{\left[\exp\left[-\left(t/\tau\right)(2n+1)^2\right]\right] - e^{-k_1 t}\right\} \quad (10)$$

In order to solve equation (8), it is necessary to first solve (9) and (10). Jordan solved for N_i and N_v in equation (9) and (10) by fitting values of D_i, D_v, k_1, k_2, N_{tot} and N_v^o that satisfactorily agree with the data of Klein. These values of N_i and N_v were then used to solve for N_s as a function of depth with annealing time as a parameter. N_s is plotted in Figure 11.

Jordan's model is applicable to Mn is GaAs. But there is reason to believe that the diffusion of other metal impurities in GaAs or even in InP may be understood using a similar model. However, the outdiffusion of donors in either GaAs or InP may be slightly different. Nevertheless, the model can be a useful guide in formulating mathematical models for the outdiffusion of different impurities in III-V compounds.

DEPTH (cm)

FIG. 11. Depth Profile of Mn Substitutionals as predicted by Jordan.

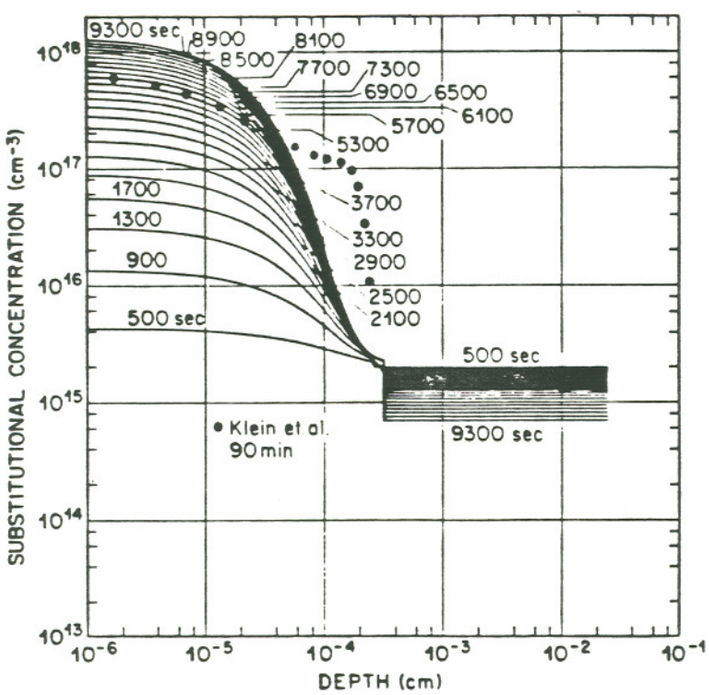

FIG. 11. Depth Profile of Mn Substitutionals as predicted by Jordan.

VITA

The author was born in Ilocos Norte, Philippines on January 25, 1957. She grew up and was educated in Manila. In 1974, after graduating as class Valedictorian at the Quezon City Science High School, she started pursuing a BS Physics degree at the University of the Philippines on a scholarship funded by the National Science Development Board. She obtained the undergraduate degree in 1978. Immediately , she took up a teaching position at the Department of Mathematical Sciences and Physics of the University of the Philippines at Los Banos (UPLB). She taught basic physics courses in this University until 1980 when she started pursuing a Master in Science Teaching (physics and chemistry) at the De La Salle University in Manila. After completing the masteral degree in 1982 she returned to UPLB and continued teaching physics. In 1983, she was elected Coordinator of the Physics Division of the newly formed Institue of Mathematical Sciences and Physics at UPLB. As Coordinator, she developed materials for physics instruction and organized the Division's preparation of a proposal for a BS Applied Physics program. She served as coordinator of the Division until September, 1986 when she came to the United States to pursue a masteral degree in Applied Physics.