

# DEFECTS IN DUAL IMPLANTED SILICON

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## ABSTRACT

### Defects in Dual Implanted Silicon

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Ion implantation is an effective method of introducing dopants in silicon in a controllable and reproducible manner. A principle side effect of ion implantation is the permanent displacement of the host atoms as the ions enter the lattice and collide with the host atoms. This damage can be reduced by high temperature annealing.

In this investigation, the strain compensation hypothesis was examined by studying the defects in dual implanted Ge<sup>+</sup>/B<sup>+</sup> and As<sup>+</sup>/B<sup>+</sup> in (100) Si after annealing. The damage distribution was simulated using the TRIM computer program and the concentration profiles using Suprem III. The defects were characterised using cross section transmission electron microscopy and correlated with the computer simulations.

The elimination of dislocation loops for a specific combination of Ge<sup>+</sup>/B<sup>+</sup> implant parameters and annealing temperature was confirmed using cross section TEM. Using the same implant and annealing conditions for As<sup>+</sup> pre-amorphisation, resulted in a significant reduction in the dislocation loop density.

TRIM (TRansport of ions in Matter) was used for estimating the damage distribution in the

silicon. For the case where dislocation loops are eliminated, the damage distribution profiles for Ge<sup>+</sup> and B<sup>+</sup> are closely matched. Ge<sup>+</sup> produces lattice expansion and B<sup>+</sup> produces lattice contraction. The closely matched damage profiles for Ge<sup>+</sup> and B<sup>+</sup> indicate that volume compensation is possible which reduces the net lattice strain. As<sup>+</sup>/B<sup>+</sup> implants also result in a significant reduction in the dislocation density and correlates with the closely matched damage distributions from TRIM.

For the implant and annealing conditions used in this investigation, the diode leakage currents at -5 V were 10<sup>-11</sup> amps for furnace annealed (950 C/30 min) samples and 10<sup>-9</sup> amps for rapid thermal annealed (1050 C/30 secs) samples. These very low leakage currents are due to the dislocation loops being far removed from the junction depletion region.

## CHAPTER 1

### INTRODUCTION

For nearly twenty years, ion implantation has been widely used to introduce dopants into a wide range of substrates in a controllable and reproducible manner. The depth is controlled by adjusting the accelerating energy and the dopant concentration is controlled by monitoring the ion current during implantation. There is an important side effect associated with ion implantation. Ion collisions disrupt the lattice by generating a large array of defects. After several ions have been implanted, an initially crystalline lattice will be changed to a highly disordered state and annealing is necessary to repair the damage and activate the dopant. A comprehensive study of the implantation induced defects is available (1).

Following post implantation anneal, the most common defects are dislocations (1). The dislocations are detrimental to device performance. For example, the gettering of impurities to the core of dislocations in the damaged region can increase the leakage currents of a p-n junction traversed by the dislocations (1-4).

The dislocations can be eliminated by high temperature anneals but this procedure is not preferred because of rapid diffusion of dopants such as boron. There is an interesting reference in the literature about elimination of dislocations in Ge<sup>+</sup> pre-amorphised silicon (5). In (100) silicon containing dual implants of Ge<sup>+</sup> and B<sup>+</sup> and furnace annealed at

850 C, the dislocations have been completely eliminated for a certain combination of implantation doses and energies. The investigators have used cross section transmission electron microscopy (XTEM) to show the presence or absence of the dislocations under varying implant parameters and annealing conditions. The boron atom is smaller and the germanium atom is larger in size than the silicon atom. The elimination of dislocations is attributed to compensation of strains in the silicon lattice by the boron and germanium atoms (5). X-ray diffraction has been used in a few cases to measure the lattice strain in implanted silicon (6-8).

The purpose of this investigation is to examine the strain compensation hypothesis (5) proposed for the elimination of dislocations in (100) Si with dual Ge<sup>+</sup>/B<sup>+</sup> implants and furnace annealed. p<sup>+</sup>/n junctions were fabricated by first pre-amorphising (100) silicon with 60 or 170 KeV Ge<sup>+</sup> ions and followed by 10 KeV B<sup>+</sup> ion implant. The samples were subjected to a three step anneal to promote regrowth of the damaged (amorphous) layer, activate the B and eliminate or reduce the implantation defects. The damage distribution was estimated using the TRIM computer program (9) and also directly observed using cross section TEM. The concentration profiles, before and after anneal, were simulated using the Suprem III computer program (10). The quality of the p<sup>+</sup>/n junctions and the effects of the implantation induced defects were assessed by measuring diode leakage currents under reverse bias.

These experiments were repeated using As<sup>+</sup> instead of Ge<sup>+</sup> for pre-amorphisation. The purpose of the As<sup>+</sup>/B<sup>+</sup> dual implant and anneal is to determine if the dislocation loops can

be reduced in density or eliminated as in the Ge<sup>+</sup>/B<sup>+</sup> dual implant and anneal. Arsenic has nearly the same mass as Ge but As (radius=2.00 Å) is larger than Ge (1.17 Å). Arsenic pre-amorphisation will produce the same sign of lattice strain as Ge because both atoms are larger than Si. Boron implantation will generate strain of opposite sign because boron (0.9 Å) is smaller than silicon (1.12 Å). Is it possible to eliminate or reduce the dislocation density using As<sup>+</sup> pre-amorphisation? In this investigation, the damage distribution profiles due to Ge<sup>+</sup> and As<sup>+</sup> pre-amorphisations are estimated using TRIM. These are compared with direct observation of the defect structures using XTEM.

Before concluding this section, the usefulness of pre-amorphisation will be stated. The scaling down of VLSI circuits towards the submicrometer range requires the making of shallow source and drain structures in order to minimise short channel effects such as threshold and punchthrough shifts (11). Shallow n<sup>+</sup>/p junctions for n-channel MOS devices can be fabricated conveniently using As<sup>+</sup> ion implantation and subsequent furnace annealing. The heavy mass of As limits the penetration depth of the implanted ions, and its low diffusivity permits high temperature annealing to remove the implantation damage and to activate the implanted dopants. A high quality abrupt n<sup>+</sup>/p junction can be readily obtained after annealing.

It is considerably more difficult to obtain shallow p<sup>+</sup>/n junctions required for the p-channel devices using B<sup>+</sup> implantation and conventional furnace annealing. This is due to the large range of the B<sup>+</sup> ions and the high diffusivity of B in Si. The high diffusivity limits the temperature and duration of the post implantation annealing, which makes complete

electrical activation and complete removal of the implantation damage difficult to achieve. The residual defects can result in junction leakage or increased sheet and contact resistivity.

A much shallower penetration depth is obtained with  $\text{BF}_2^+$  implantation as compared to the same energy  $\text{B}^+$  implantation. The implantation of  $\text{BF}_2^+$  molecular ions into Si has been reported to have the advantages of higher electrical activation after low temperature annealing and lower leakage current for p+/n junctions compared with  $\text{B}^+$  implantations (12-14).

A recent approach to address the problem associated with shallow p+ junction formation includes the following:

- 1) pre-amorphising the Si surface to eliminate the crystalline channels and
- 2) rapid thermal annealing (RTA) to minimise dopant diffusion.

Pre-amorphisation by Ar (15), Ne (16), Si (17-19), or Ge (20, 21) has been reported. Ge+ implantations, performed at room temperature produce sharp crystalline/amorphous (c/a) interfaces. In the case of a sharp c/a interface, post-implantation low temperature annealing at 500-600 C will promote the regrowth of crystalline Si by solid phase epitaxy (SPE) from the interface to the top surface (22, 23). Defect free shallow p+/n junctions have been reported for dual Ge+/B+ ion implantation and annealing (24-27).

The objective of this investigation was to examine the validity of the strain compensation hypothesis (5) in the elimination of dislocation loops. The hypothesis was checked by examining defects in dual implanted and annealed Ge+/B+ in (100) silicon and in dual implanted As+/B+ in (100) silicon. The defect structures were examined using cross

section TEM. The damage distribution was simulated using TRIM and concentration profiles using Suprem III. The p+/n junction quality was assessed from leakage current measurements under reverse bias.

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## CHAPTER 2

### EXPERIMENTAL PROCEDURES

#### 2.0 PROCEDURES

The processing conditions examined in this investigation are given in Table 2.1 below:

Table 2.1  
Ion Implantation Parameters

| AMORPHISATION<br>DOSE $\text{cm}^{-2}$ | AMORPHISATION<br>ENERGY KeV | DOPANT (Boron)<br>DOSE $\text{cm}^{-2}$ | DOPANT (Boron)<br>ENERGY KeV |
|--|-----------------------------|---|------------------------------|
|  |                             | 3e15                                    | 10                           |
| 4e14 Ge                                | 60                          | 3e15                                    | 10                           |
| 4e14 Ge                                | 170                         | 3e15                                    | 10                           |
| 4e14 As                                | 60                          | 3e15                                    | 10                           |
| 4e14 As                                | 170                         | 3e15                                    | 10                           |

A silicon wafer without the above treatments was used to establish the baseline. The Ge+/B+ implanted wafers were the focus of this investigation. However, supporting evidence was acquired from As+/B+ implanted samples to test the strain compensation hypothesis discussed in Chapter 1. Samples were subjected to a three step furnace anneal given below:

450 C/30 min + 600 C/30 min + 950 C/30 min, nitrogen atmosphere.

Any reference to annealing in the text implies the above three step process unless otherwise specified.

The purpose of the 450 C anneal is to sharpen the crystalline/amorphous interface and homogenise the amorphous layer (1). The 600 C anneal promotes recrystallisation of the amorphous region through solid phase epitaxy and completes the dopant activation. At 950 C, defects at the original amorphous/crystalline interface and below the interface, are either eliminated or reduced to a minimum density characteristic of the annealing temperature. Detailed discussions of the effects of low and high temperature anneals on the regrowth process and defect redistribution are published (2,3).

The investigative methods used in this study are stated below:

- 1) The primary investigative technique used to study the defects was transmission electron microscopy (TEM), selected area electron diffraction and micro diffraction. (100) silicon wafers were implanted according to the schedule in Table 2.1 and subjected to a three step anneal. Cross sectional TEM samples were prepared by mechanical polishing and ion milling (4). A Hitachi H-800 scanning transmission electron microscope was used to determine changes in the number and location of the defects.
- 2) An attempt was made to determine the lattice strain due to the implant induced defects using double crystal x-ray rocking curve analysis (DCD). Lattice strain is expected to cause low level intensity oscillations in the tail of the peak which can easily be

masked by the background. In this investigation, the brightness of the x-ray tube was not sufficient to reveal the intensity oscillations. There are many references on the subject of x-ray diffraction for strain measurements and one which is a comprehensive discussion of theory and practice (5).

- 3) Computer programs such as TRIM (6) (TRansport of Ions in Matter) and Suprem III (7) were used to characterise the lattice damage in the as-implanted Si and the concentration profiles of the implanted species. These programs have yielded interesting results and reasonable agreement with direct observations using XTEM.
- 4) Finally, a study of defects in semiconductor materials can be meaningful if a correlated with device performance. Diodes were fabricated using the process conditions in Table 2.1 and annealed. Leakage currents were measured under reverse bias and correlated with the defect structure.

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## CHAPTER 3

### COMPUTER SIMULATION OF DOPANT AND DAMAGE PROFILES

#### 3.0 INTRODUCTION

The emphasis in this section is to characterise the ion implantation damage using TRIM and concentration profiles using Suprem III. TRIM (1) is used to determine the range statistics and damage profiles for B and Ge implants in Si and compare the locations of the end damage with direct observations of the defects from XTEM. Suprem III (2) is used to plot the concentration profiles of the implanted species. For example, the change in the B concentration profile due to pre-amorphisation is determined using Suprem III.

Suprem III allows the user to simulate the various processing steps used in the manufacture of silicon integrated circuits. Examples of processing steps simulated by Suprem III include diffusion, oxidation, ion implantation, Si epitaxial growth, etching and others. A structure whose processing is being simulated can be made up from one to ten layers each of which is composed of one to ten possible materials. To begin the Suprem simulation all of the coefficients and parameters for the materials and impurities must be input and the initial structure defined. These functions are accomplished by the INITIALISE statement. In its simplest form the initial structure is a single layer of substrate material. Suprem has a built-in library of default coefficients that can be used. The results from Suprem simulation are available in both printed and graphic forms.

Suprem is a comprehensive program for simulating silicon device processing. TRIM (TRansport of Ions in Matter) is very focussed in its scope. TRIM calculates the penetration of ions into solids. The ions may have energies from 10 eV to 2 GeV. The program will accept complex targets made up of compound materials with upto three layers with each layer being a different material. TRIM will calculate the final distribution of ions and also the kinetic phenomena such as target damage, energy loss in electronic interactions, nuclear interactions, ionisation, recoils and phonons.

### 3.1 RESULTS AND DISCUSSION

The data from TRIM will be presented first. TRIM uses the Monte Carlo method for determining the ion penetration statistics such as projected range ( $R_p$ ), straggle (uncertainty in the range), skew and kurtosis. Skew is the assymetry in the range distribution and is expressed as a positive number if the peak is shifted toward the surface or a negative number if the peak is shifted away from the surface. Kurtosis describes the distribution at the tail end of the profile (3).

The damage distribution is generally expressed in terms of vacancies produced and energy deposited by the ion as it travels through the lattice. Calculation of the damage distribution is based on the Kinchin-Pease theory (4) and subsequent refinements (5-7). In the discussions to follow, the range statistics and damage distribution from TRIM will be correlated with the direct observation of defects from cross section TEM (XTEM).

### 3.1.1 TRIM SIMULATION FOR B+ IMPLANT IN Si

The B+ ion dose used in this investigation is  $3 \times 10^{15}/\text{cm}^2$  and implant energy is 10 KeV. These parameters are well below the critical values required to amorphise Si using B+ ion implantation (7,8). Hence the damage from the B+ ions will consist of isolated and clusters of point defects which do not overlap to form a continuous amorphous layer. Figure 3.1 is a schematic of the ion trajectories for 10 KeV B+ in Si. The B+ ion exhibits considerable lateral range, particularly when compared with trajectories for heavier ions such as Ge+ and As+ shown in later figures.

Figure 3.2 shows the B+ ion ranges as a function of depth. The ion range profile has a negative skew and is consistent with the behaviour of low mass, low energy ions (3). The range (389 Å) is consistent with published values (3). In this investigation XTEM samples were examined and dislocation loops were found at a depth below the implant surface which corresponds to the range calculated by TRIM. This will be further discussed in Section 4.1.2 where XTEM results are presented.

Figure 3.3 shows the vacancies (damage) produced as a function of depth. The ions create more vacancies close to the surface and as they travel deeper they lose energy and come to rest. To displace a Si atom from its equilibrium site requires 14-15 eV and a 10 KeV B+ ion transfers 30 eV/0.3 nm of travel in silicon (8). The B+ ion has sufficient energy to create vacancies. The vacancy concentration profile shows defects even past the projected range (389 Å) and may be due to the straggle.

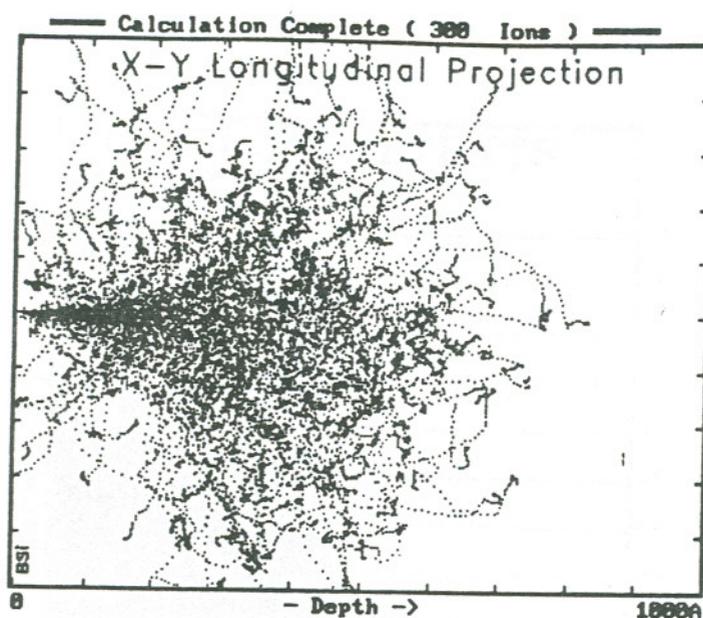


Figure 3.1: Ion trajectories for 10 KeV B<sup>+</sup> ions in silicon.

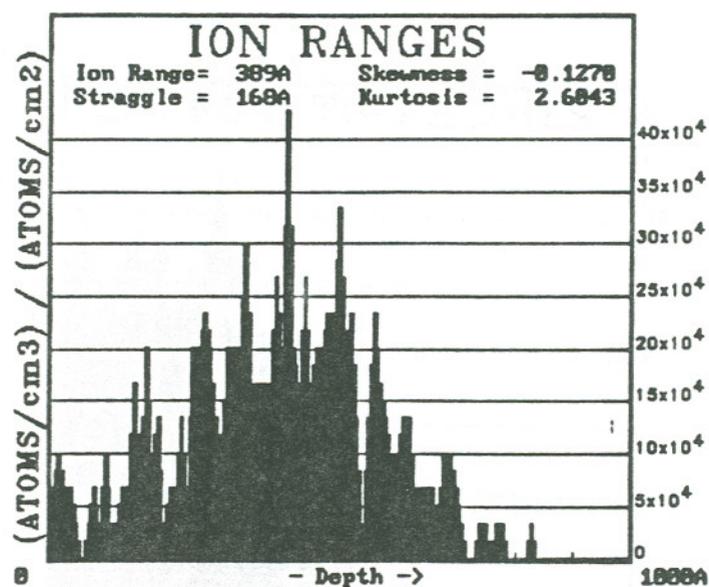


Figure 3.2: Distribution of ion ranges for 10 KeV B<sup>+</sup> ions.

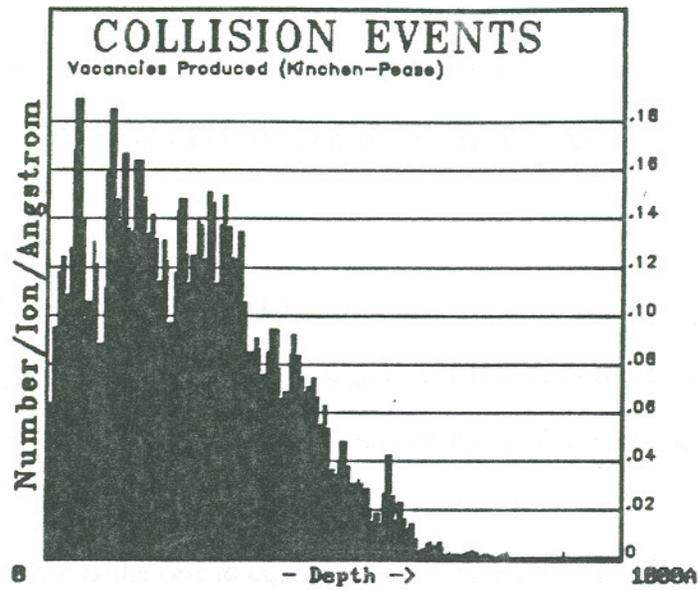


Figure 3.3: Distribution of vacancies produced by the 10 KeV B+ ions.

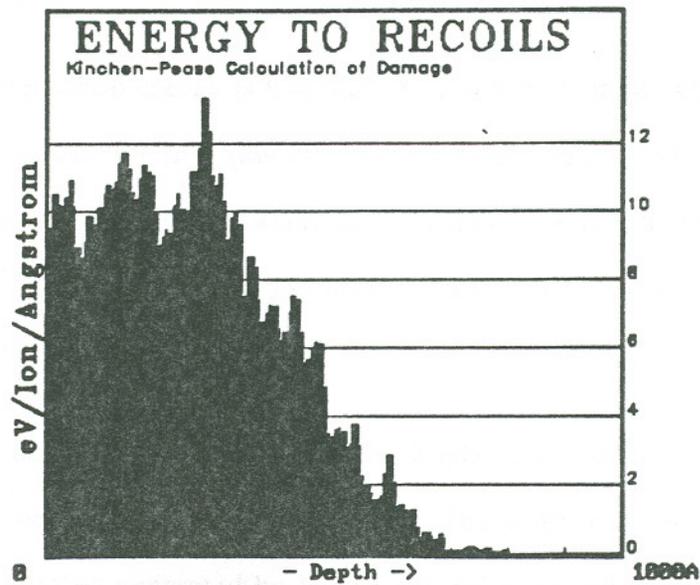


Figure 3.4: Distribution of the energy to recoils (damage) for 10 KeV B+ ions.

From Suprem III, Figure 3.18, the peak in the as-implanted B concentration profile is at a depth of 400 Å and is in agreement with the peak in the damage distribution (389 Å) from TRIM. For a light ion such as B<sup>+</sup> (11 amu) implanted into a heavier target such as Si (28 amu), the dopant concentration and defect distributions are expected to follow each other (3).

The damage distribution can also be expressed as the energy loss per unit length or energy to recoils as in Figure 3.4. The energy loss per unit length is the sum of two terms: the nuclear stopping term and the electronic stopping term. The stopping power is usually represented as  $dE/dx$ . In order to produce displacements of atoms from their sites, the nuclear interaction term is the one to consider. For 10 KeV B<sup>+</sup>, using TRIM the electronic and nuclear interaction terms are estimated to be as follows:

$$* (dE/dx)_{\text{electronic}} = 10.75 \text{ eV/Å}$$

$$* (dE/dx)_{\text{nuclear}} = 7.9 \text{ eV/Å}$$

Since the nuclear interaction energy is less than the electronic interaction energy, it is not surprising that the 10 KeV B<sup>+</sup> ions produce low level damage. TRIM also estimates the number of vacancies produced per B<sup>+</sup> ion to be 80 which is too low to produce amorphous regions. As a result, the 10 KeV B<sup>+</sup> ions produce isolated and clusters of point defects but not a continuous amorphous layer.

In the next section, the damage produced by Ge<sup>+</sup> implants will be analysed using TRIM. The nuclear interaction energy is the dominant term. The number of vacancies produced is 10 to 20 times the number generated by B<sup>+</sup> ions. Unlike the lighter and low energy B<sup>+</sup> ions, the heavier Ge<sup>+</sup> ions produce extensive damage and amorphisation.

### 3.1.2 TRIM SIMULATION FOR Ge+ IMPLANT IN Si

The Ge+ ion has a mass of 74 amu compared to 11 amu for B+. The implant energies for Ge+ used in this study are 60 and 170 KeV compared to 10 KeV for B+. The Ge+ dose and implant energies are sufficient to produce a continuous amorphous layer below the implant surface. This has been confirmed using XTEM discussed in Section 4.1.3 and also consistent with other citations (7,9). The high implant energies will drive the Ge+ ions deeper into the Si than in the case of the 10 KeV B+ ions and produce thicker damaged layers. Since the Ge+ ions are much heavier than the target Si, the peak in the defect distribution is expected to lag the peak in the ion distribution.

Figure 3.5 is a schematic of the 60 KeV Ge+ ion trajectories in Si. Comparing with Figure 3.4 for B+ ions, the lateral range or lateral spread of the Ge+ ions in Si is much less. A heavy ion such as Ge+ has a higher forward momentum and produces high density damage in a tightly bound volume of the target. Figure 3.6, is a TRIM plot of the Ge+ ion ranges in the target Si. The range is 480 Å and straggle is 171 Å. Ge+ being much heavier than B+, the skew is a positive value of 0.3727. The tail distribution, measured by the kurtosis is comparable to that for the 10 KeV B+ ions.

Next, the damage produced by the 60 KeV Ge+ ions in silicon is considered. As in the case of the B+ ions, the damage is expressed in terms of the vacancies and the energy to recoils. Figure 3.7 shows the collision events or vacancies produced by the 60 KeV Ge+ ions in Si. Comparing with Figure 3.3 for B+ ions, the number of vacancies produced by the Ge+ ions at any depth is about 10 times the number for B+ implant.

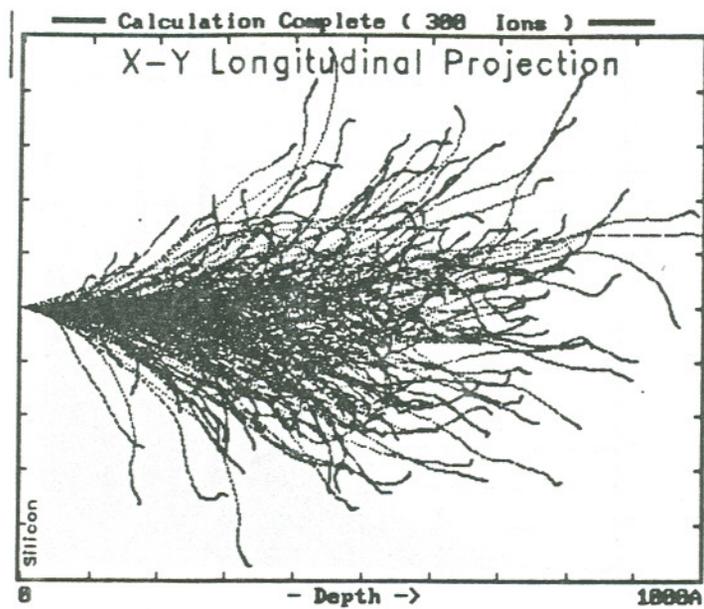


Figure 3.5: Ion trajectories for 60 KeV Ge+ ions in silicon.

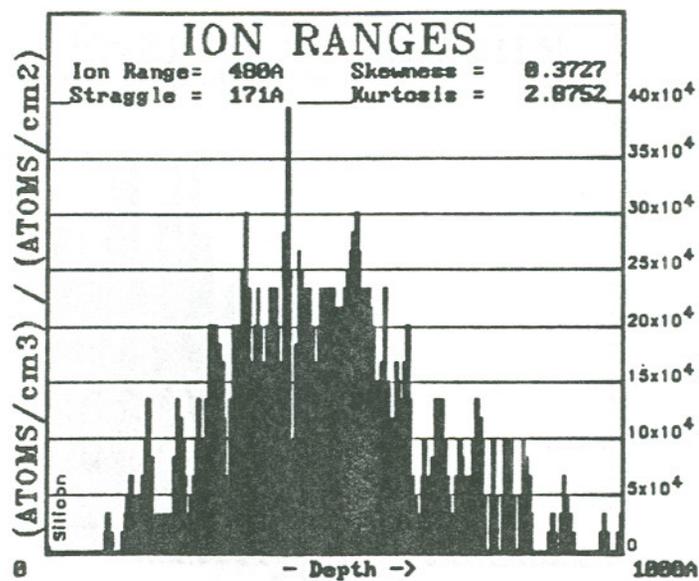


Figure 3.6: Distribution of ion ranges for 60 KeV Ge+ ions.

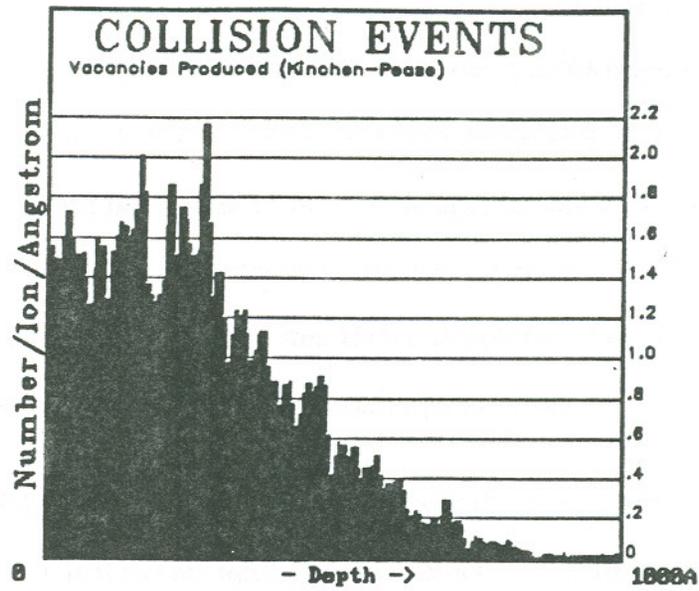


Figure 3.7: Distribution of vacancies produced by the 60 KeV Ge+ ions.

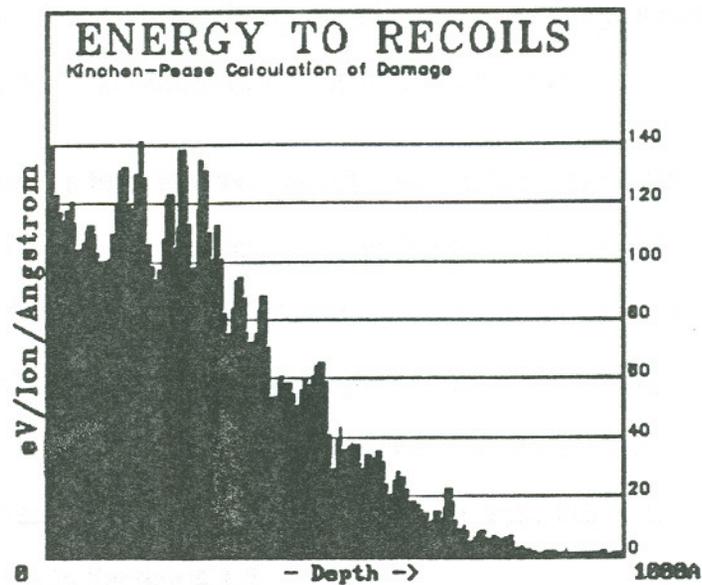


Figure 3.8: Distribution of the energy to recoils (damage) for 60 KeV Ge+ ions.

The large number of defects produced by the 60 KeV Ge<sup>+</sup> ions is because of the high nuclear interaction energy term. From TRIM, the  $(dE/dx)_{\text{nuclear}} = 120 \text{ eV/\AA}$  and  $(dE/dx)_{\text{electronic}} = 15 \text{ eV/\AA}$  for 60 KeV Ge<sup>+</sup> ions. In the case of the 10 KeV B<sup>+</sup> ions, the nuclear interaction term is an order of magnitude smaller and also less than the electronic interaction term. From TRIM the estimated damage per B<sup>+</sup> ion is 80 vacancies/ion and the damage per Ge<sup>+</sup> ion is 789 vacancies/ion. Hence the 60 KeV Ge<sup>+</sup> ions can be expected to produce extensive damage in the form of an amorphous layer.

Figure 3.8 is a TRIM plot of the energy to recoils or the energy/unit distance deposited by the 60 KeV Ge<sup>+</sup> ion as it travels through the Si lattice. Comparing with Figure 3.4 for B<sup>+</sup> ions, the Ge<sup>+</sup> ions deposit an order of magnitude higher energy/unit distance. In summary, the 60 KeV Ge<sup>+</sup> ions produce amorphisation of the silicon due to the high nuclear interaction energy term, the large number of vacancies produced and the high value of energy loss per unit distance travelled in the silicon lattice. The preceding data from TRIM is verified by XTEM observations discussed in Section 4.1.3.

The end of damage can be estimated from the tail portion of the distribution in Figure 3.8. Only 14-15 eV is required to displace a Si atom from its lattice site. In Figure 3.8 the depth corresponding to 15 eV is about 650 Å and signifies the end of damage. Using XTEM, a narrow band of defects are observed at a depth of 600 Å and the region between the wafer surface and the defect band has been confirmed to be amorphous by micro diffraction. There is good correlation between the end of damage from TRIM and XTEM. The XTEM results are discussed in Section 4.1.3.

For an ion heavier than the target atom, the defect distribution peak is expected to lag the concentration distribution peak (3). This is indeed the case for the Ge<sup>+</sup> ion implanted in Si. From Figure 3.7, the peak in the vacancy (damage) distribution plot is at 450-500 Å. From the Suprem III plot, Figure 3.20, the peak in the Ge concentration occurs deeper at 1000-1100 Å demonstrating agreement with theory.

What happens when the Ge<sup>+</sup> ion energy is increased from 60 KeV to 170 KeV maintaining the same dose? Figure 3.9 shows the ion range distribution for the 170 KeV Ge<sup>+</sup> ions in Si. The range is 1027 Å and the straggle is 300 Å. Upto a depth of 350-375 Å, there is no evidence of implanted Ge<sup>+</sup>. This correlates with the as-implanted Ge concentration profile from Suprem III, Figure 3.22.

The distribution of the collision events in Figure 3.10 shows that the Si lattice is damaged to a depth of 1500 Å. The damage depth can also be estimated from the energy to recoils in Figure 3.11. The minimum displacement energy for the Si atom from its lattice is 14-15 eV. In Figure 3.11, the energy to recoils (damage) approaches 14-15 eV at a depth of approximately 1700 Å. Hence the depth of the damage layer from Figures 3.10 and 3.11 are in close agreement. TEM microstructures in Section 4.1.3, show that dislocation loops are formed at a depth of 1600 Å. It can be concluded that the end of damage for the 170 KeV Ge<sup>+</sup> is approximately 1500-1700 Å and there is good correlation in the results from TRIM and XTEM.

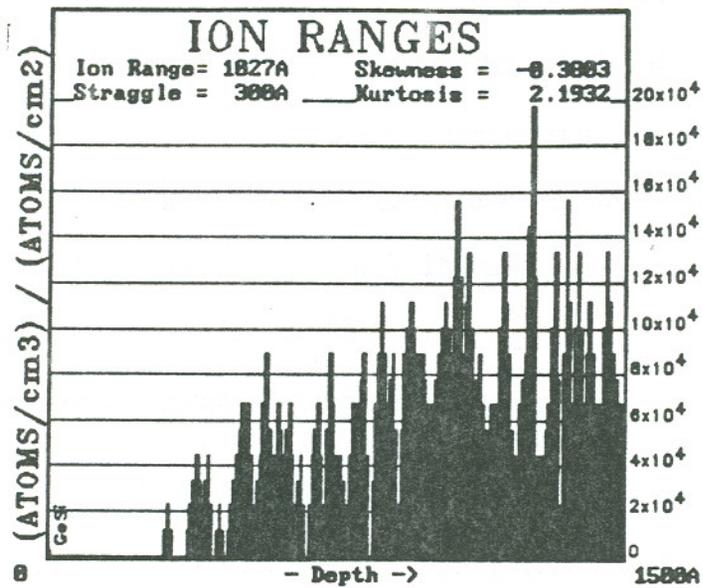


Figure 3.9: Distribution of ion ranges for 170 KeV Ge<sup>+</sup> ions in silicon.

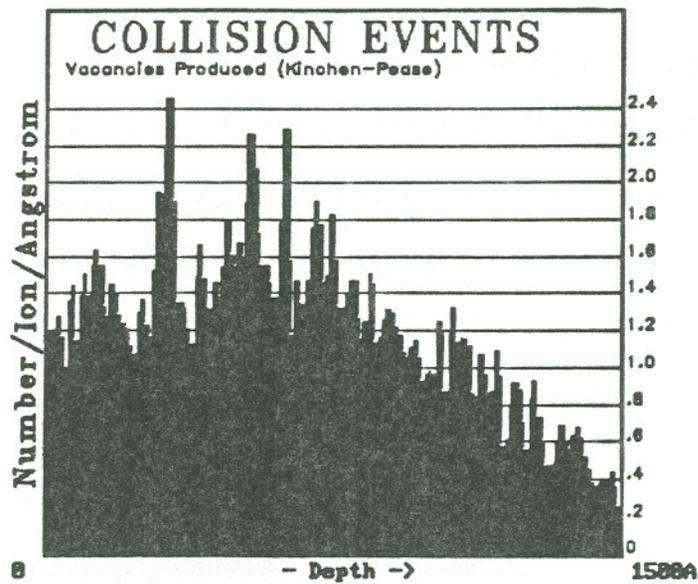


Figure 3.10: Distribution of vacancies produced by the 170 KeV Ge<sup>+</sup> ions.

As stated in Chapter 1, the strain compensation hypothesis for defect elimination will be examined by substituting As<sup>+</sup> instead of Ge<sup>+</sup> for pre-amorphising the silicon. The TRIM simulation was performed for As<sup>+</sup> to determine if there is similarity with the results from the Ge<sup>+</sup> implants discussed above. The plots for 60 KeV As<sup>+</sup> are shown in Figures 3.12-3.14 and for 170 KeV As<sup>+</sup> in Figures 3.15-3.17. The conclusion is, implanting As<sup>+</sup> ions with the same dose and energy as Ge<sup>+</sup>, the TRIM plots for ion ranges, collision events and energy to recoils are found to match closely with those for Ge<sup>+</sup>.

From Figure 3.14, the end of damage is 750 Å for the 60 KeV As<sup>+</sup> ions at a recoil energy of 14-15 eV. For 60 KeV As<sup>+</sup> ions, dislocations are observed at a depth of 1000 Å in XTEM samples, reported in Section 4.1.4. For the 170 KeV As<sup>+</sup> ions, the damage depth estimated from TRIM is 1700 Å and is in good agreement with the XTEM results in Section 4.1.4.

With the above discussion, a study of the damage produced in Si by B<sup>+</sup>, Ge<sup>+</sup> and As<sup>+</sup> ions using TRIM, is concluded. In the as-implanted condition, TRIM is useful for determining the range statistics, nuclear and electronic energy loss components and damage profiles. There is good agreement between the range statistics from TRIM and other citations. Estimates of the end of damage from TRIM are also in good agreement with direct observations of defects in XTEM samples reported in Sections 4.1.3 and 4.1.4.

However, TRIM does not have provision for the following:

- 1) Determining the damage parameters for dual implants.
- 2) Determining concentration profiles of the implanted species.
- 3) Annealing the sample.

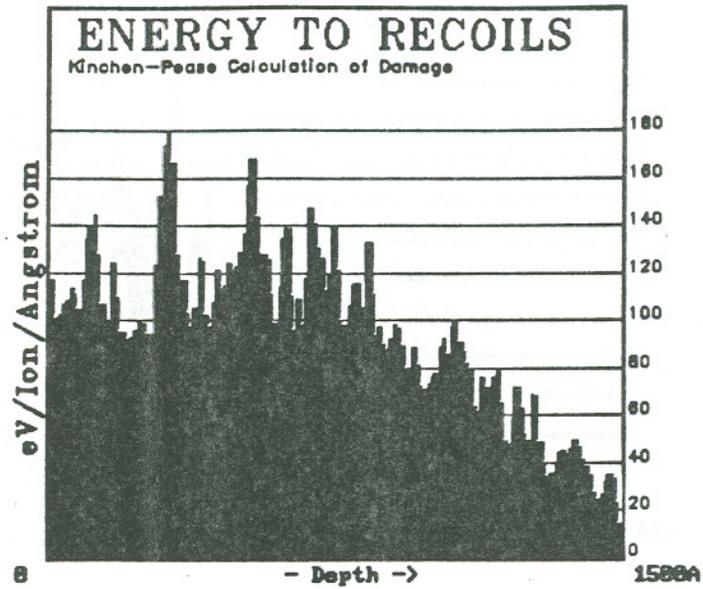


Figure 3.11: Distribution of the energy to recoils (damage) for 170 KeV Ge+ ions.

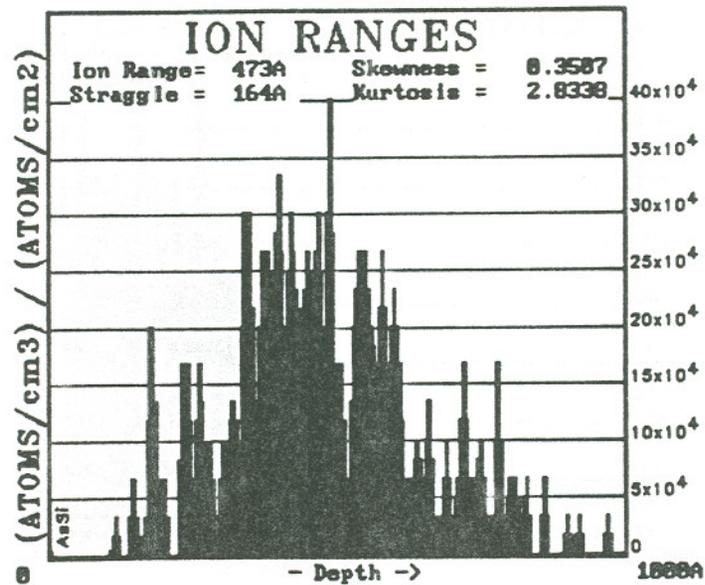


Figure 3.12: Distribution of ion ranges for 60 KeV As+ ions in silicon.

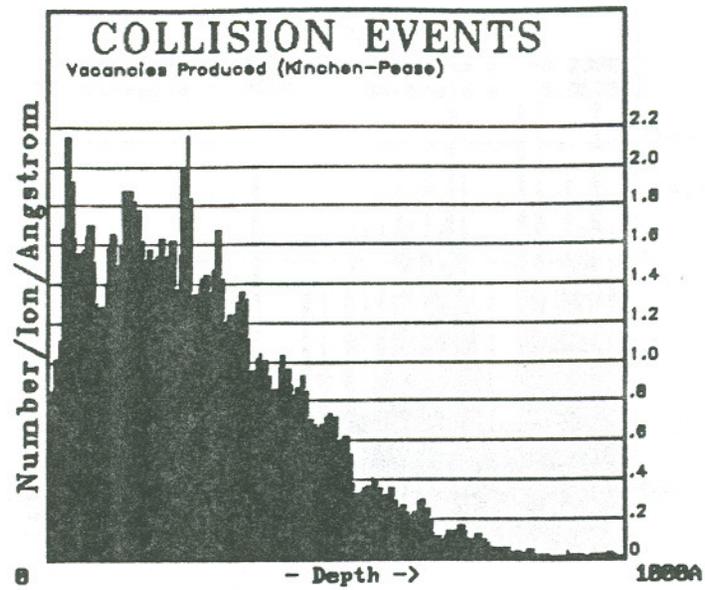


Figure 3.13: Distribution of vacancies produced by the 60 KeV As+ ions.

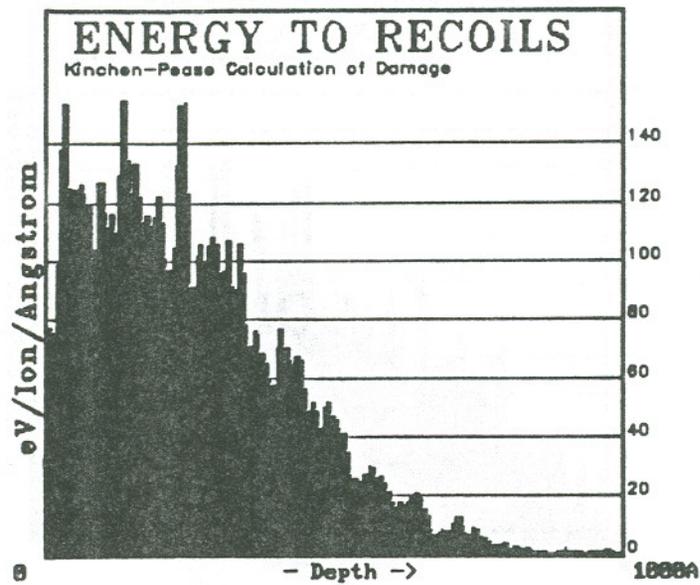


Figure 3.14: Distribution of the energy to recoils (damage) for 60 KeV As+ ions.

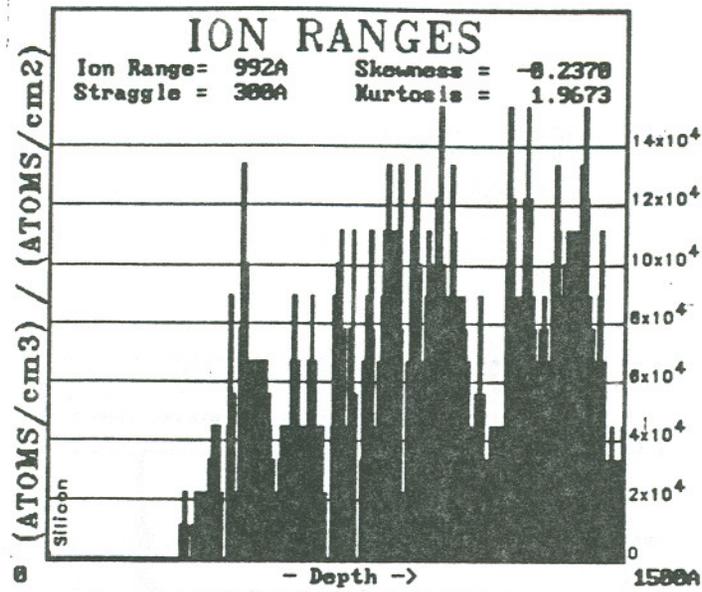


Figure 3.15: Distribution of ion ranges for 170 KeV As+ ions in silicon.

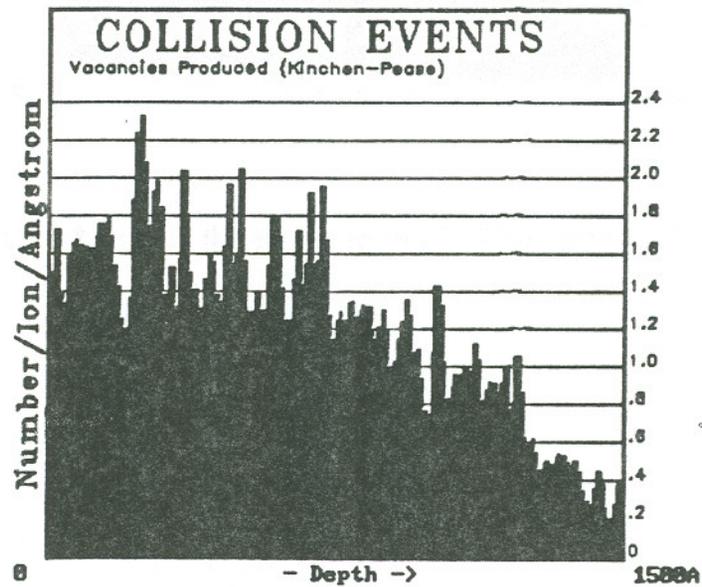


Figure 3.16: Distribution of vacancies produced by the 170 KeV As+ ions.

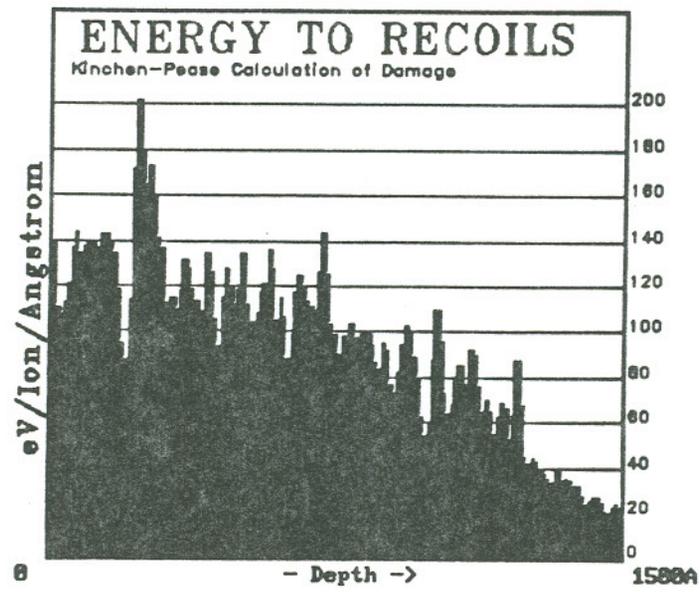


Figure 3.17: Distribution of the energy to recoils (damage) for 170 KeV As+ ions.

Suprem is a comprehensive program for simulating individual processing steps and integrating them to form a whole device. In this investigation, Suprem III was used for determining the concentration profiles in the as-implanted and annealed conditions and the junction depths. The results from Suprem III simulation are presented in the next section.

### 3.1.3 SUPREM SIMULATION OF CONCENTRATION PROFILES FOR IMPLANTED AND ANNEALED (100) SILICON

A summary of the processing conditions and the corresponding concentration profiles from Suprem III are given in Table 3.1 below.

Table 3.1  
Implantation and Suprem Concentration Profiles

| IMPLANT TREATMENT<br>DOSE/ENERGY        | ANNEALING<br>TREATMENT<br>950 C/30 min | SUPREM PROFILES<br>(CONCENTRATION) |
|---|--|------------------------------------|
| 3e15 cm <sup>-2</sup> B+/10 KeV         | with & w/o                             | Figures 3.18, 3.19                 |
| 4e14 Ge+/60 KeV plus<br>3e15 B+/10 KeV  | with & w/o                             | Figures 3.20, 3.21                 |
| 4e14 Ge+/170 KeV plus<br>3e15 B+/10 KeV | with & w/o                             | Figures 3.22, 3.23                 |

From Figures 3.18 and 3.19, the B penetrates deep into the silicon and the profile is rather abrupt even after the anneal. Pre-amorphisation does have an effect on the B profile.

Without pre-amorphisation, Figure 3.18, the B penetration is about 1900 Å. With 60 KeV Ge+ pre-amorphisation, Figure 3.20, the maximum penetration of B is about 1200 Å. Pre-amorphisation restricts the B+ penetration and the B profile is contained within the pre-amorphised layer. After the 950 C/30 min anneal, the Ge profile has not changed noticeably because Ge is a very slow diffuser in Si. However, boron diffuses past the pre-amorphised layer.

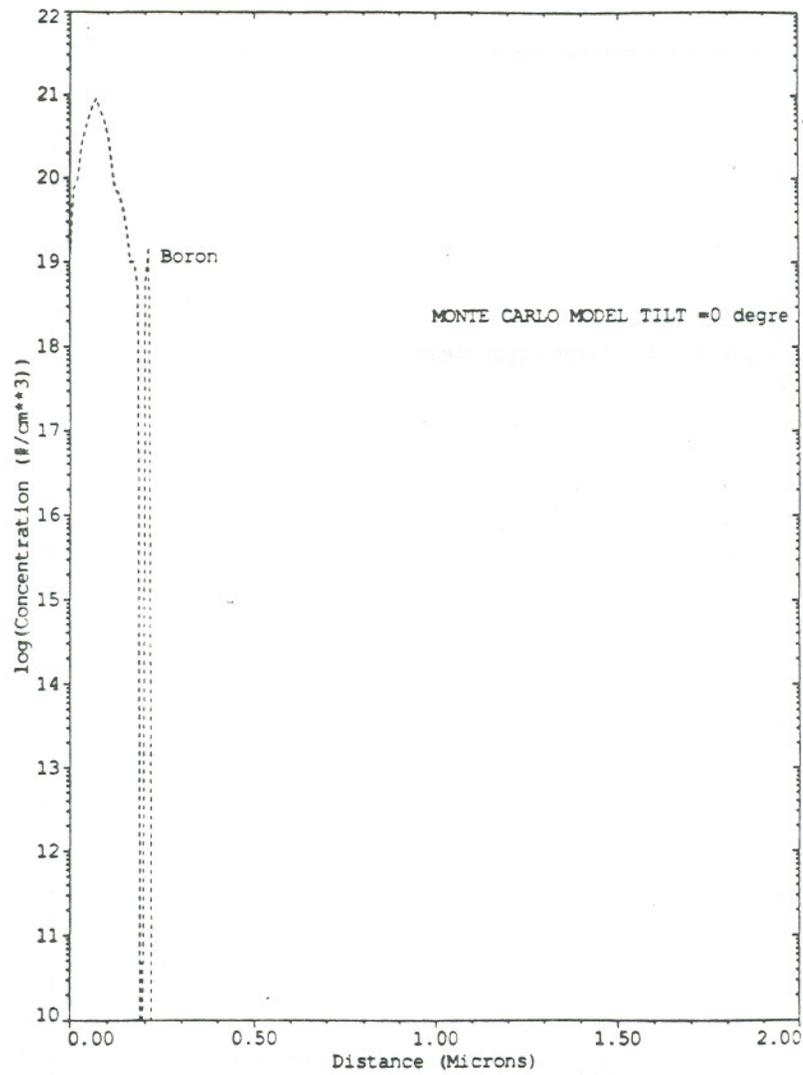


Figure 3.18: As-implanted B profile. No pre-amorphisation

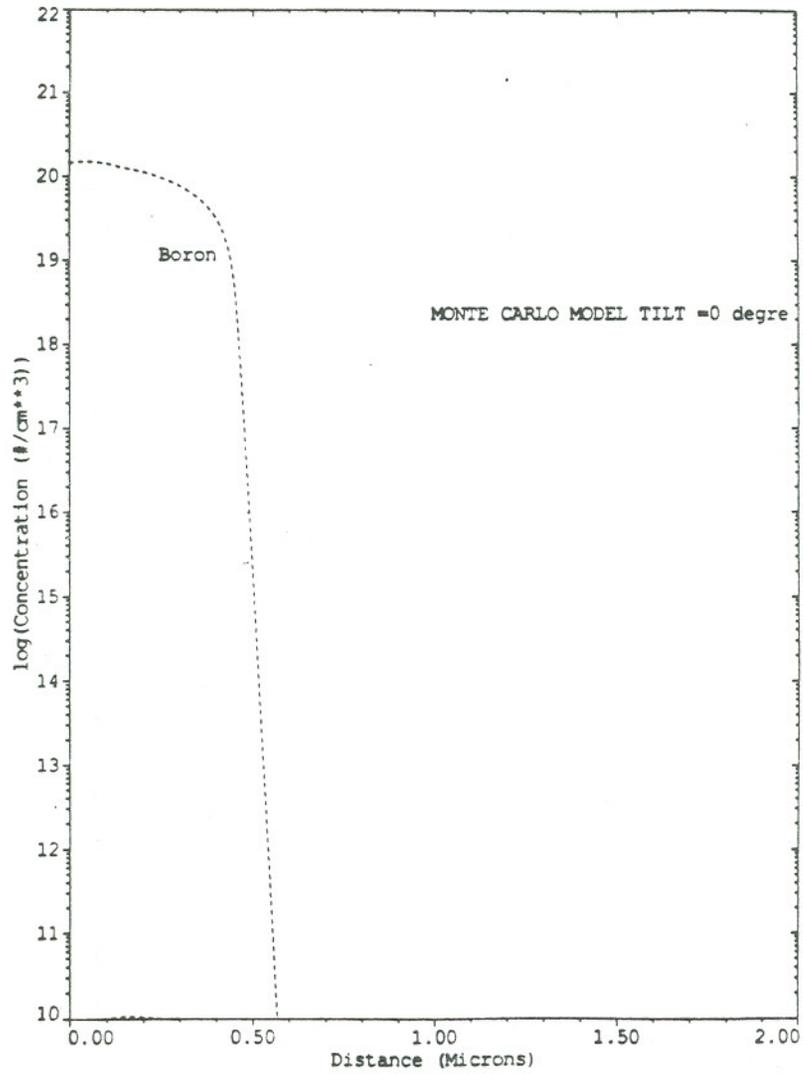


Figure 3.19: Annealed B profile. No pre-amorphisation.

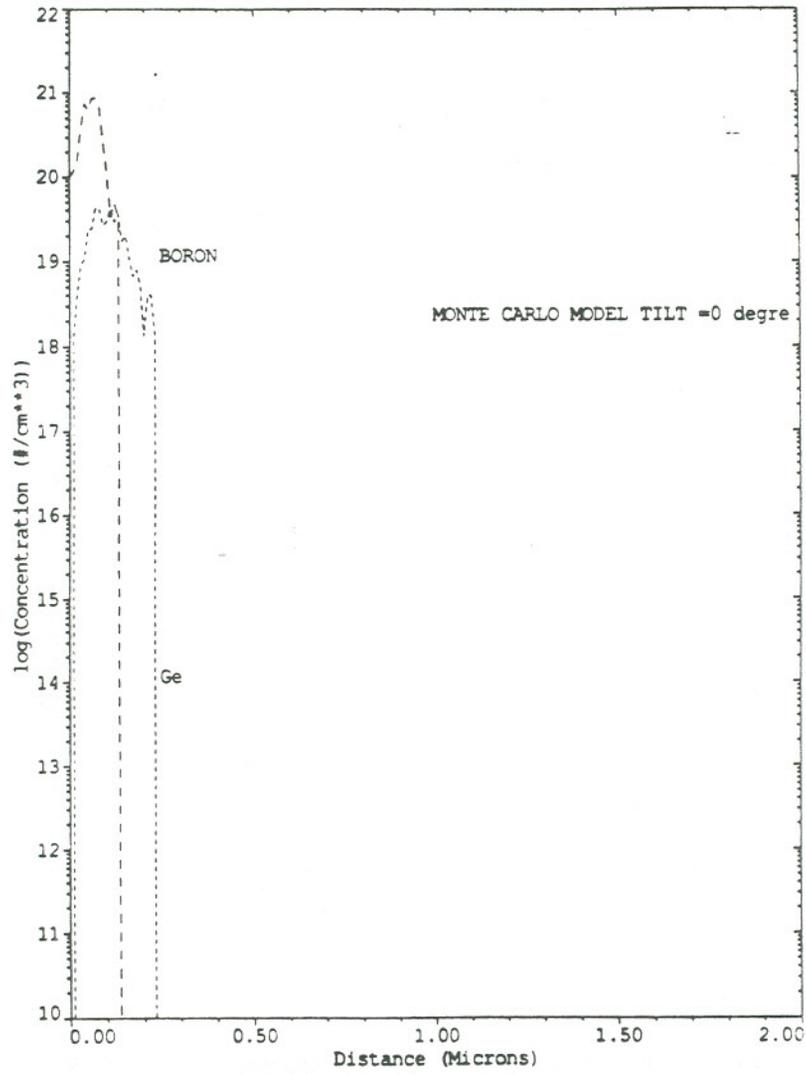


Figure 3.20: 60 KeV Ge+ pre-amorphisation and 10 KeV B+ implant. No anneal.

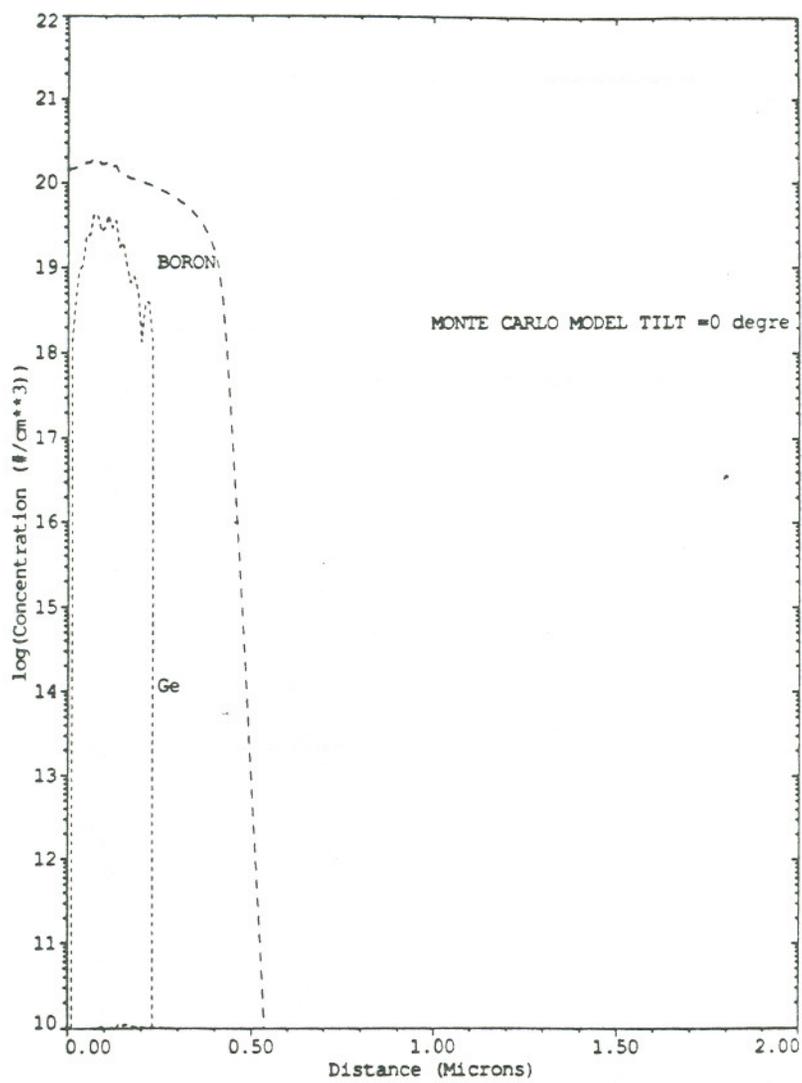


Figure 3.21: 60 KeV Ge+ pre-amorphisation and 10 KeV B+ implant. Annealed.

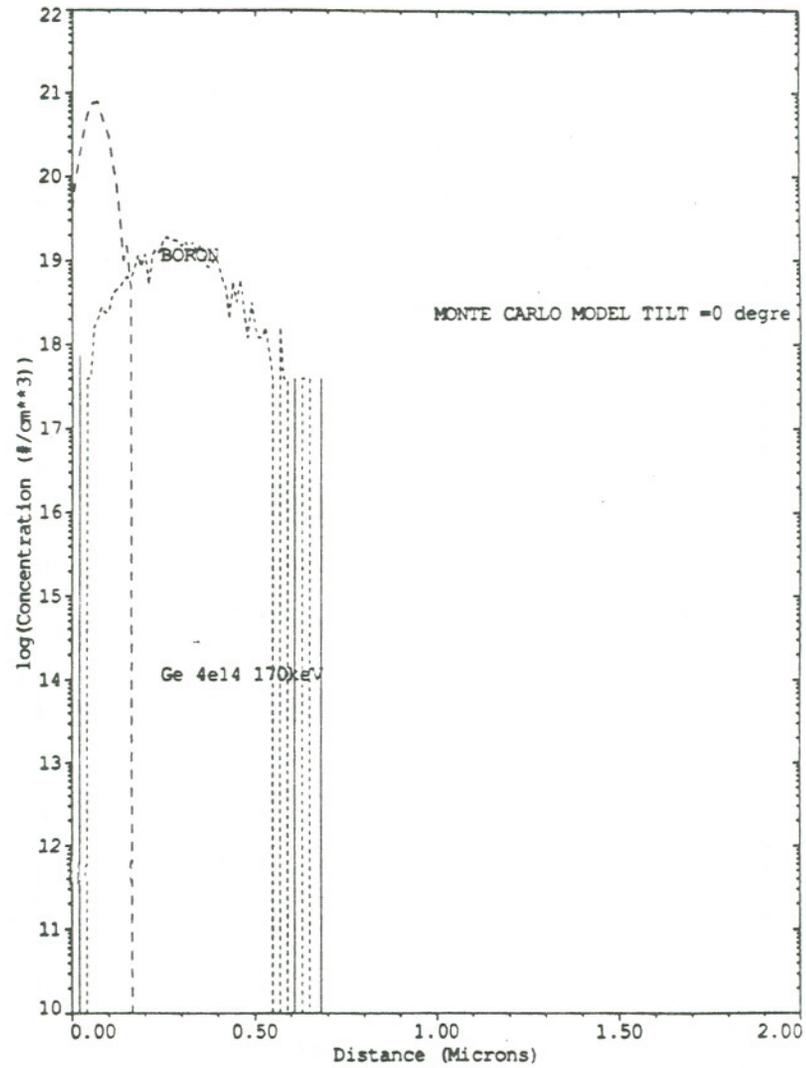


Figure 3.22: 170 KeV Ge+ pre-amorphisation and 10 KeV B+ implant. No anneal.

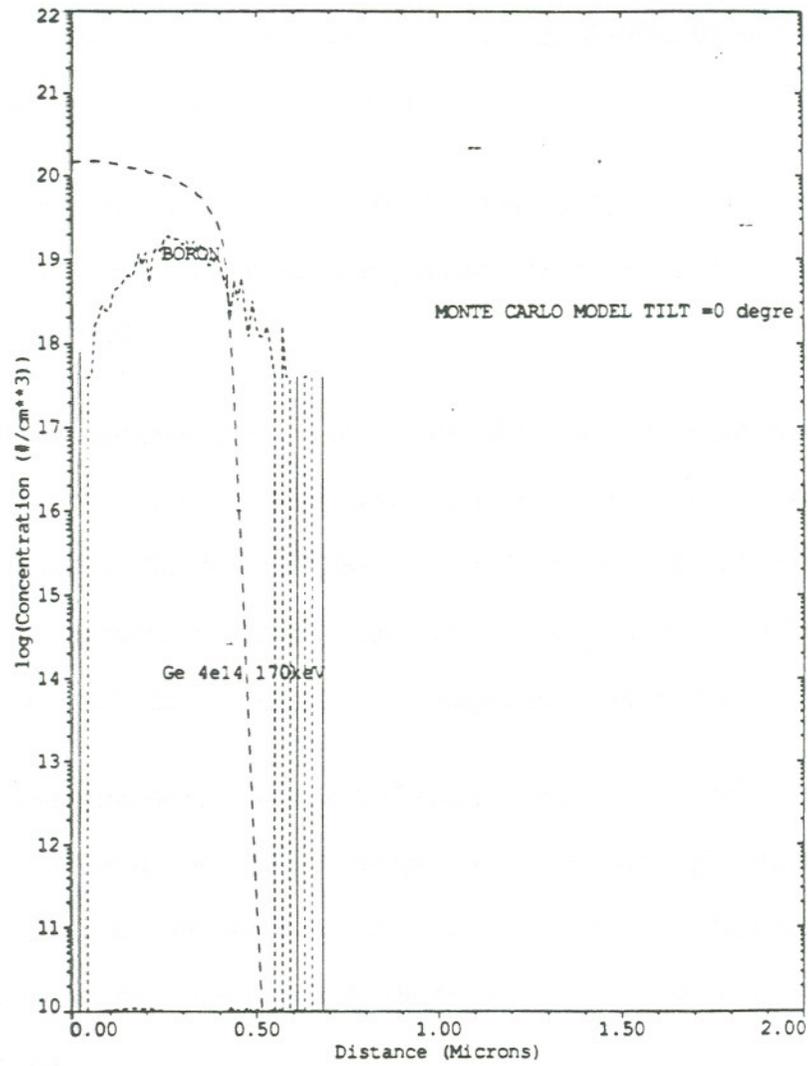


Figure 3.23: 170 KeV Ge+ pre-amorphisation and 10 KeV B+ implant. Annealed.

This may be due to the extended annealing process used in this investigation. It is likely that rapid anneals at elevated temperatures may limit the B diffusion such that the B profile is contained within the pre-amorphised layer.

The effect of increasing the Ge<sup>+</sup> pre-amorphisation energy from 60 KeV to 170 KeV will be discussed. With reference to the as-implanted Ge<sup>+</sup> and B<sup>+</sup> profiles in Figure 3.22 the observations below are relevant:

- 1) The Ge concentration profile does not start from the surface but from a depth of 350-400 Å below the surface. This observation is consistent with the ion range distribution from TRIM for 170 KeV Ge<sup>+</sup> in Figure 3.9. The 170 KeV implant energy drives the Ge<sup>+</sup> ions deep into the Si, causing increasing damage as it travels deeper into the lattice and little or no damage close to the surface.
- 2) The B penetration depth in Figure 3.22 is approximately 200-300Å deeper than in Figure 3.20 for 60 KeV Ge pre-amorphisation. The higher pre-amorphisation energy is associated with deeper B penetration. To account for the foregoing, the defect (vacancies) distributions created by the 60 and 170 KeV Ge<sup>+</sup> ions have to be considered.

Comparing Figures 3.8 and 3.11, the 60 KeV Ge<sup>+</sup> ion deposits higher energy in the near surface regions (<300 Å) compared to the 170 KeV Ge<sup>+</sup> ions. Comparing Figures 3.7 and 3.10, the 60 KeV Ge<sup>+</sup> produces a higher concentration of vacancies in the near surface region (< 300 Å) compared to the 170 KeV Ge<sup>+</sup>. It is clear from

TRIM that there is reduced damage in the near surface regions for the 170 KeV Ge<sup>+</sup> ions thereby enabling deeper penetration of the B<sup>+</sup> ions.

After annealing at 950 C/30 min, the B profile in Figure 3.23 is contained within the Ge concentration profile, contrary to the results in Figure 3.21. The significant point is that the annealed B profile predicted by Suprem III, is the same for all implant and annealing conditions used in this investigation. This may be a consequence of the extended time at the annealing temperature of 950 C.

Consider the unannealed B profiles in Figures 3.18, 3.20 and 3.22. Compare with the annealed B profiles in Figures 3.19, 3.21 and 3.23. In all cases, the B profiles exhibit a sharp drop off. Without pre-amorphisation, the B profile would be expected to show channeling at concentrations below  $1 \times 10^{15} \text{ cm}^{-2}$ . Boron channeling in Si is well established (3,7). We do not see evidence of channeling for the B distribution predicted by Suprem III in Figures 3.18-3.23. Channeling is highly dependent on the angle of incidence and the substrate orientation.

It is probable that the B tails will be better defined as the number of incident ions in the Suprem III INITIALISE statement is increased to very high values. In this investigation, the computations were limited to 1000 ions which may be adequate to accurately represent the concentration profiles upto the projected range. A more accurate representation of the tail region of the profile may require a significant increase in the number of ions (say 10,000 ions) in the INITIALISE STATEMENT and a corresponding increase in the computational time.

### 3.1.4 JUNCTION DEPTH FROM SUPREM III PROFILES

The background arsenic concentration is  $1e16 \text{ cm}^{-2}$ . The junction depths are estimated from the annealed profiles in Figures 3.19, 3.21 and 3.23. In Table 3.2 the junction depths are compared with the location of the defect bands from TRIM and XTEM.

Table 3.2  
Implant Treatment and Defect Location

| TREATMENT<br>(DOSE/ENERGY)   | JUNCTION DEPTH<br>(A) | DEFECT LOCATION<br>(A) |
|--|-----------------------|------------------------|
| $3e15 \text{ cm}^{-2} \text{ B}^+ / 10 \text{ KeV}$<br>annealed                          | 4900 A                | 500 A                  |
| $4e14 \text{ Ge}^+ / 60 \text{ KeV}$<br>$3e15 \text{ B}^+ / 10 \text{ KeV}$<br>annealed  | 4800 A                | no dislocation loops   |
| $4e14 \text{ Ge}^+ / 170 \text{ KeV}$<br>$3e15 \text{ B}^+ / 10 \text{ KeV}$<br>annealed | 4500 A                | 1500-1600 A            |

From Table 3.2, it is evident that the defects are far removed from the junction and this is beneficial for the electrical characteristics of the junction. In Chapter 5.0, diode leakage currents are examined with reference to the implantation defects. At this point it will suffice to say that as long as the defects are far removed from the junction and the edges of the depletion layer, the defects will not have an adverse effect on the diode performance. This is indeed the case for diodes fabricated using the treatments above.

### 3.2 CONCLUSIONS

TRIM and Suprem III computer simulation models have been used to characterise the ion implantation statistics, implantation damage and dopant concentration profiles. The main conclusions are as follows:

- 1) The projected range and straggle for B<sup>+</sup> and Ge<sup>+</sup> from TRIM compares favourably with citations in the literature.
- 2) TRIM also estimates (a) the energy loss due to nuclear and electronic interactions (b) energy to recoils and (c) damage (vacancies) in as-implanted samples. Using the kinetic data from TRIM it is shown that the 10 KeV B<sup>+</sup> cannot produce a continuous amorphous layer in the (100) Si. The end of damage from TRIM and the location of dislocation loops from XTEM are in good agreement.

For 60 KeV Ge<sup>+</sup> pre-amorphisation, the end of damage from TRIM closely corresponds to the location of the defects from XTEM. The 60 KeV Ge<sup>+</sup> produces a continuous amorphous layer below the implant surface confirmed by XTEM and correlates with the high values of the nuclear interaction energy and energy to recoils predicted by TRIM. For 170 KeV Ge<sup>+</sup> pre-amorphisation, there is once again good correlation between the end of damage predicted by TRIM and the location of defects from XTEM.

- 3) The concentration profiles for the as-implanted and annealed conditions are determined using Suprem III. Ge<sup>+</sup> pre-amorphisation reduces the B<sup>+</sup> penetration by about 30-35%. After annealing at 950 C/30 min, the B profiles do not show any

changes. The B profiles show a sharp drop off even after the 950 C anneal. For the INITIALISE parameters used in this investigation, B channeling tails have not been observed in the Suprem III plots.

- 4) The annealed junction depths are estimated to be 4500-4900 Å from the Suprem plots. The defects bands occur at much shallower depths (<2000 Å). The wide separation between the defect band and the junction is beneficial for the electrical performance of diodes. The defects do not have an adverse effect on the reverse leakage currents of diodes, as explained in Chapter 5.0.

### 3.3 REFERENCES

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## CHAPTER 4

# TRANSMISSION ELECTRON MICROSCOPY INVESTIGATION OF THE IMPLANTATION DAMAGE

### 4.0 INTRODUCTION

Ion implantation is extensively used to dope semiconductor substrates. The incoming ion transfers its energy to the host lattice via nuclear and electron interactions. Nuclear interactions are responsible for the lattice imperfections in the form of Frenkel pairs, i.e., interstitials and vacancies. Ion implantation degrades device performance. For example, the gettering of impurities to the core of the dislocations in the damaged region increase the leakage currents of a p-n junction traversed by the dislocations (1).

Sub-micron device technology is the driving force for understanding the types of implantation damage, how they arise and what influences the defect annealing kinetics. As devices shrink, deep diffusion of the dopants is not acceptable due to problems such as punch through in field effect transistors. Methods for dissolution of the defects are sought which do not result in a significant increase in the junction depths.

The physical damage from ion implantation can be examined using Rutherford backscattering (RBS) and/or transmission electron microscopy (TEM). RBS yields depth information as well as lattice location (vacancies/interstitials) information. From TEM, the origin and type of damage can be ascertained.

In this Chapter, the objective is to examine cross section TEM samples and determine the type of defects and their spatial distribution. Direct observation of the defects will be correlated with estimates of the damage from TRIM in Chapter 3.

## 4.1 RESULTS AND DISCUSSION

### 4.1.1 CROSS SECTION TEM MICROSTRUCTURES

XTEM was used to determine the following:

- 1) The location of the defects with respect to the top surface of the wafer.
- 2) The type of defects, whether dislocation loops or stacking faults or dislocation networks or a combination thereof.
- 3) Processing conditions under which the defect density is noticeably reduced or eliminated.

All implanted wafers were furnace annealed in nitrogen per schedule below:

450 C/30 min + 600 C/30min + 950 C/30min.

At 450 C, the amorphous/crystalline interface is expected to sharpen and the amorphous layer homogenised (2). The 600 C anneal will recrystallise the amorphous layer and activate most of the dopant. The 950 C anneal will minimise or eliminate the implantation induced defects in the vicinity of the c/a interface. Also the 950 C anneal will maximise the dopant activation. A drawback of the 950 C furnace anneal is that the B will diffuse rapidly into the bulk Si and increase the junction depth.

Cross section TEM (XTEM) samples were examined for the defects produced by the ion implantation and annealing. Diffraction contrast was used to image the defects. Excellent reviews of the kinematical and dynamical theories of diffraction are available (3,4). The TEM images were taken under bright field axial illumination with the beam parallel to (110) pole and (111) pole. The  $g_{220}$  and  $g_{002}$  reflections were used because the defect contrast intensity was maximum for this reflection. A two beam condition was used with  $s > 0$ ,  $s$  is the deviation from the exact Bragg condition. The habit plane and Burgers vector of the dislocations were determined as explained in the reviews of diffraction contrast (3,4).

#### 4.1.2 DEFECTS IN B+ ION IMPLANTATED (100) SILICON

In this section, the defect microstructures produced by 10 KeV B+ ion implantation in the Si wafer surface, are discussed. Figure 4.1, is representative of defects introduced by B+ implantation and annealed according to the three step treatment stated above. There is no Ge+ pre-amorphisation and the B+ dose is  $3 \times 10^{15} \text{ cm}^{-2}$  and the implantation energy is 10 KeV. The defects in Figure 4.1 consist of dislocation loops (DLs) on the (111) planes of the Si lattice with Burger's vector  $a/2[110]$ . The loops form within in a band and the center of the band is located approximately 500 Å from the surface. This value is close to the projected range of 389 Å from TRIM simulations for 10 KeV B+ in Si in Section 3.1.1. The spread of the dislocation loops within the band may be due to the straggle associated with the B+ ion range.

As the ion travels through the solid, it loses energy essentially by two mechanisms, nuclear and electronic interactions. It is the nuclear interactions that are solely responsible

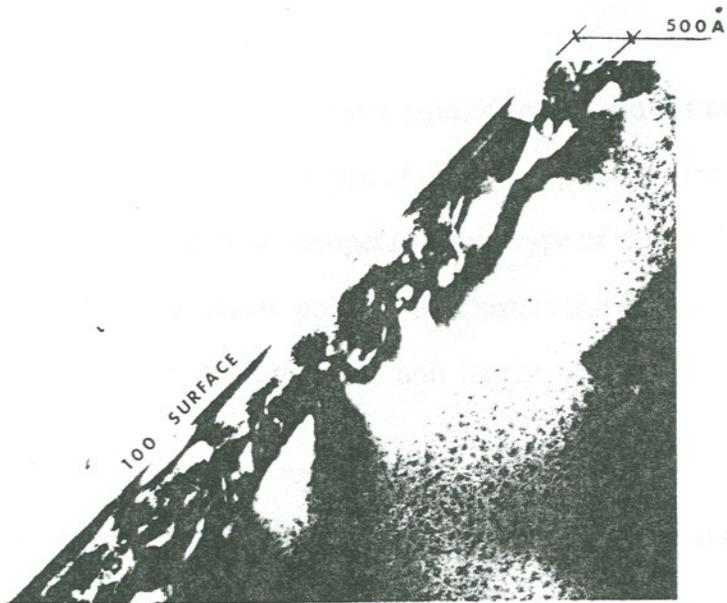


Figure 4.1a: Boron implant and annealed. Dislocation loops 500 Å from the surface.

BF  $g = 220$ .

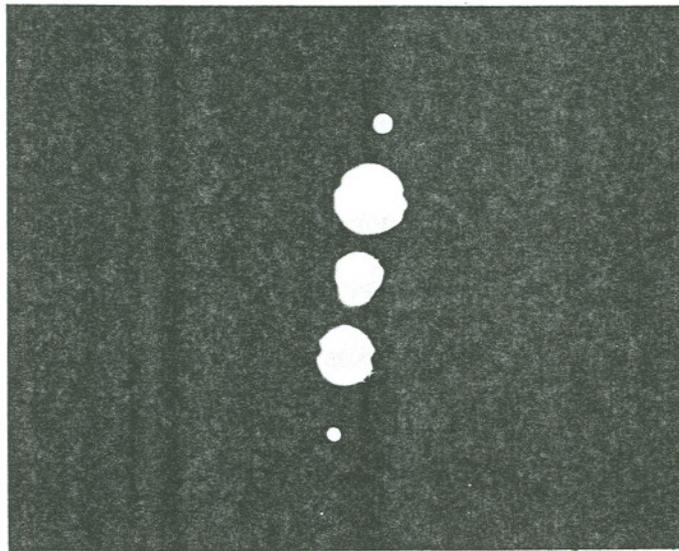


Figure 4.1b: Selected area diffraction pattern for above region. [110] zone.

for displacement of the target atoms from their equilibrium positions and damage the crystallinity of the lattice (5). The nature and type of damage depends on the type of ionic species, energy, angle of incidence, dose, temperature and type of target. The ion induced damage consists of interstitials, vacancies, point defect clusters and dislocations. Larger the amount of energy transferred to the lattice per unit length of ion travel, the more the damage.

If  $E_t$  is the energy transferred to a target atom during collision with an ion and  $E_d$  is the minimum energy required to displace a target atom (related to the binding energy) then the following results have been proposed (5):

- 1)  $E_t < E_d$ , target atom is excited but no displacement.
- 2)  $E_t > E_d$ , simple displacement and formation of isolated point defects.
- 3)  $E_t > 2E_d$ , displacements plus secondary lattice disorder.
- 4)  $E_t \gg E_d$ , large disorder, defect clusters and continuous amorphous layers.

Values of  $E_t$ , the energy transferred in a collision, have been published as a function of the incident ion energy (6). For 10 KeV B<sup>+</sup> ions used in this investigation,  $E_t = 30$  eV/0.3 nm. The 0.3 nm corresponds to the average interatomic spacing in Si. Only nuclear scattering is assumed responsible for the damage. The displacement energy,  $E_d$ , for Si is estimated to be 14 eV from  $E_d = 4 E_b$ , where  $E_b$  is the binding energy (6).

Given  $E_t = 30$  eV and  $E_d = 14$  eV,  $E_t = 2E_d$  for the 10 KeV B<sup>+</sup>. The energy transferred by the 10 KeV B<sup>+</sup> ions is just sufficient to cause localised displacements or small defect clusters and not a continuous amorphous layer. If the implant energy is insufficient to form an amorphous layer the defects form at a depth corresponding approximately to the peak of

the impurity distribution (projected range,  $R_p$ ). This is also referred to as Category I damage (1).

It follows from the above discussion that after the 10 KeV B<sup>+</sup> ion implantation, the Si lattice has a concentration of point defects at a depth corresponding to the projected range of B<sup>+</sup> in Si. The evolution of dislocation loops from the point defects, as a function of annealing treatment has been extensively studied. The generally quoted model (7-9) is based on recombination of interstitials and vacancies. After the recombination, point defect clusters 20-30 Å in size remain. These clusters were found to evolve through a series of Shockley partial dislocations into the stable perfect dislocation loops on the (111) planes with  $a/2[110]$  Burger's vector. The loops are elongated in the [110] direction and the Burger's vector normal to the long axis of the loops.

In Figure 4.1, the dislocation loops lie on the (111) planes elongated in the [110] direction with Burger's vector  $a/2[110]$  in agreement with the proposed model (7-9). Also, the location of the DLs agrees with the projected range calculated from TRIM. The 10 KeV B<sup>+</sup> ions do not produce a continuous amorphous layer below the wafer surface. The dislocation loops in Figure 4.1 are not positioned along a sharp interface and the stagger in the location of the DLs can be attributed to the straggle in the B<sup>+</sup> ion range.

Next, the defects will be examined in Si which has been preamorphised with Ge<sup>+</sup> prior to B<sup>+</sup> implantation.

#### 4.1.3 DEFECTS IN Ge<sup>+</sup> PRE-AMORPHISED AND B<sup>+</sup> IMPLANTED (100) SILICON

In this section, the damage induced by the dual implant in which the first step is pre-amorphisation using Ge<sup>+</sup> ions and the second step is the B<sup>+</sup> ion implant, is discussed. The XTEM microstructures are for the processing steps given below:

- 1) (100) Si pre-amorphised with  $4 \times 10^{14}/\text{cm}^2$ , 60 KeV Ge<sup>+</sup> ions.
- 2) The above wafer is implanted with  $3 \times 10^{15}/\text{cm}^2$ , 10 KeV B<sup>+</sup> and furnace annealed in nitrogen at 450 C/30min + 600 C/30min + 950 C/30min.
- 3) (100) Si pre-amorphised with  $4 \times 10^{14}/\text{cm}^2$ , 170 KeV Ge<sup>+</sup> ions followed by B<sup>+</sup> ion implant at  $3 \times 10^{15}/\text{cm}^2$ , 10 KeV, plus a furnace anneal sequence as in (2) above.

Ge<sup>+</sup> is significantly heavier than B<sup>+</sup>; the atomic mass for Ge<sup>+</sup> is 74 amu compared to 11 amu for B<sup>+</sup>. The Ge<sup>+</sup> ions are implanted at 60 and 170 KeV compared 10 KeV for the B<sup>+</sup> ion implantation. At 60 KeV,  $>500 \text{ eV}/0.3 \text{ nm}$  is transferred by each Ge<sup>+</sup> ion as it travels through the Si lattice (6). The energy transferred by the Ge<sup>+</sup> ions far exceeds the displacement energy of 14 eV for Si. Hence the 60 KeV and 170 KeV Ge<sup>+</sup> ions will cause extensive displacement damage and produce a continuous amorphous layer from the surface to a finite depth below. From TRIM data, Section 3.1.2, the range of the 170 KeV Ge<sup>+</sup> ions is 2-3 times the range of the 60 KeV Ge<sup>+</sup> ions and therefore a thicker amorphous layer will be formed with the 170 KeV Ge<sup>+</sup> ions.

When an amorphous layer is formed during implantation, the defects associated with the c/a interface are classified as Category II damage (1). The crystalline region below the c/a interface is damaged by the recoil atoms and the defects consist of excess interstitials. Upon annealing at high temperature,  $> 900$  C, the interstitials evolve into dislocation loops (1). The defect structures due to the Ge<sup>+</sup> ion pre-amorphisation plus B<sup>+</sup> ion implant are discussed below.

Figures (4.2a, b, c) are XTEM microstructures from Si implanted with 60 Kev Ge<sup>+</sup> ions only. There was no B<sup>+</sup> implant and no annealing. In Figure 4.2a, there is a very narrow,  $<50$  Å wide, dark band of defects located 650 Å below the surface. The region above the narrow band of defects has been examined by micro diffraction in the TEM. The presence of an amorphous layer is confirmed by the diffraction rings shown in the micro diffraction pattern in Figure 4.2c.

The end of damage is estimated to be 600 Å from TRIM, Section 3.1.2, using energy to recoil data. In theory, the end of damage occurs in the crystalline region below the amorphous/crystalline interface and the damage consists of interstitials (1). There is close agreement between the end of damage (600 Å) estimated from TRIM and the measured depth (650 Å) of the defect band in Figure 4.2a. These results are also in agreement with theoretical and experimental observations reported elsewhere for Ge<sup>+</sup> implantation in Si (10,11).

The fine structure of the narrow defect band was not resolvable even at high magnifications, Figure 4.2b. It is therefore reasonable to state that the damage within the

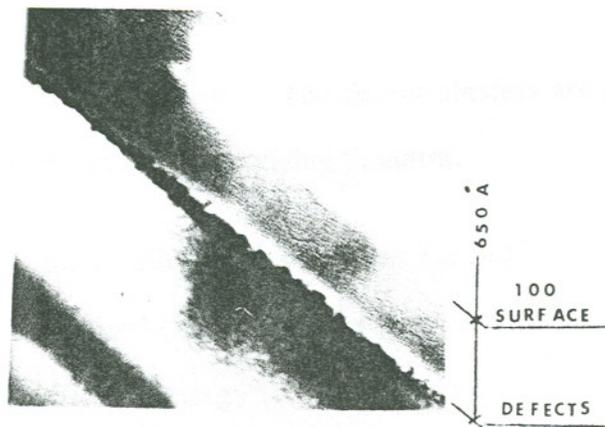


Figure 4.2a: 60 KeV Ge+ pre-amorphisation. Narrow band of defects.

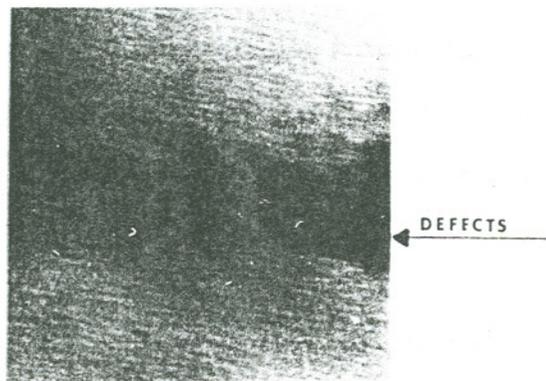


Figure 4.2b: Defects at higher magnification.  
300 KX

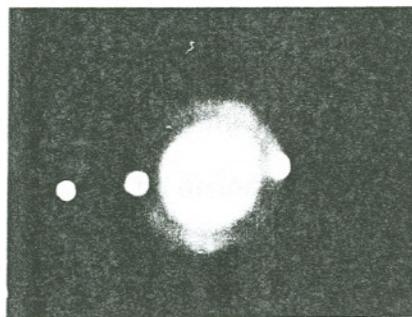


Figure 4.2c: Diffraction rings due to amorphous layer.

narrow band consists of point defect clusters. The defect clusters are generated by the primary Ge<sup>+</sup> ions and the recoil cascades comprising Si atoms.

The next step is to examine the XTEM microstructures for  $3 \times 10^{15}/\text{cm}^2$ , 10 keV B<sup>+</sup> ions implanted in the Ge<sup>+</sup> pre-amorphised (100) Si. It was shown in Section 4.1.2 that the 10 KeV B<sup>+</sup> ions transfer just sufficient energy to produce point defect clusters and not a continuous amorphous layer below the surface. Hence the B<sup>+</sup> ions are not expected to compound the damage already produced by the Ge<sup>+</sup> pre-amorphisation.

The implant parameters for Ge<sup>+</sup> pre-amorphisation have a significant influence on the residual defect density after annealing. It is possible to eliminate the dislocation loops given the proper combination of Ge<sup>+</sup> and B<sup>+</sup> ion implant parameters. The microstructures for the two cases listed below are noticeably different.

- 1)  $4 \times 10^{14}/\text{cm}^2$ , 60 KeV Ge<sup>+</sup> followed by  $3 \times 10^{15}/\text{cm}^2$ , 10 KeV B<sup>+</sup> implants plus anneal at (450 C/30min + 600 C/30min + 950 C/30min).
- 2)  $4 \times 10^{14}/\text{cm}^2$ , 170 KeV Ge<sup>+</sup> followed by  $3 \times 10^{15}/\text{cm}^2$ , 10 KeV B<sup>+</sup> implants plus anneal at (450 C/30min + 600 C/30min + 950 C/30min).

Figure 4.3 is representative of the XTEM microstructure for the dual implant and anneal treatment (1) above where there are no dislocation loops. Upon increasing the Ge<sup>+</sup> pre-amorphisation energy from 60 KeV to 170 KeV, dislocation loops are present as shown in Figure 4.4. The DLs in Figure 4.4 are located at a depth of 1500-1600 Å from the surface and correlates well with the end of damage estimated by TRIM for the 170 KeV Ge<sup>+</sup> ions. The DLs are extrinsic and form on the (111) planes with Burgers vector  $a/2[110]$ . The

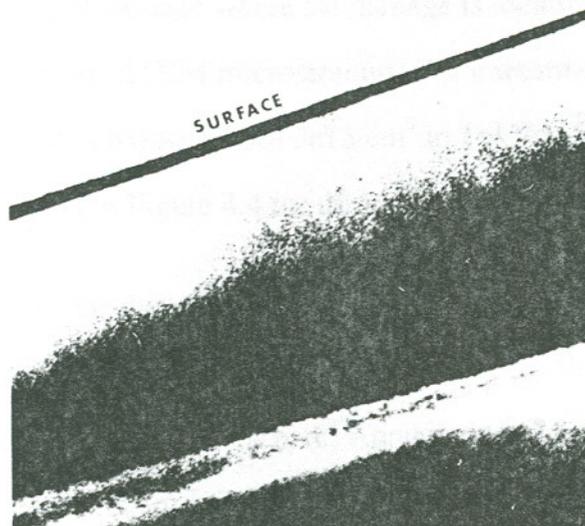


Figure 4.3: 60 KeV Ge+/10 KeV B+ annealed. No dislocations.

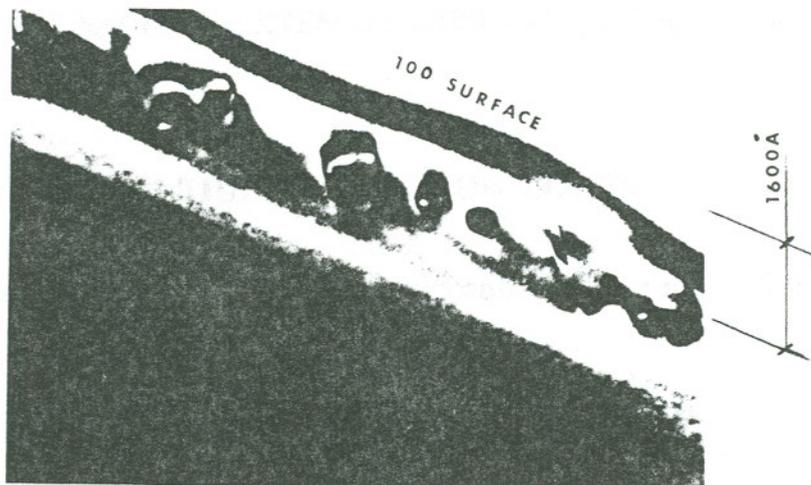


Figure 4.4: 170 KeV Ge+/10 KeV B+ annealed. Dislocation loops present.

defects belong to Category II damage where the damage is localised in a region below the c/a interface. Figure 4.5 is an XTEM microstructure for a treatment similar to (2) above except that the B<sup>+</sup> ion dose is reduced from 3e15/cm<sup>2</sup> to 1e15/cm<sup>2</sup>. The defect structure in Figure 4.5 is identical to that in Figure 4.4 for the higher B<sup>+</sup> ion dose.

The absence of DLs may be due to one or more of the following: (a) Dissolution of subcritical size point defect clusters upon annealing at 950 C; (b) Volume compensation and strain relief in the vicinity of the c/a interface; (c) Annihilation of excess vacancies by a comparable number of excess interstitials. The mechanism applicable in this case is discussed in Section 4.1.4.

In summary, it is possible to eliminate the dislocation loops for the dual implant 60 KeV Ge<sup>+</sup>/10 KeV B<sup>+</sup> treatments. Increasing the Ge<sup>+</sup> ion energy to 170 KeV causes the DLs to appear. The location of the DLs from XTEM and TRIM are in good agreement..

#### **4.1.4 ELIMINATION OF THE DISLOCATION LOOPS**

The likely mechanism for elimination of the dislocation loops in the dual implant plus annealing treatment is discussed in this section.

In Figure 4.3 corresponding to the 60 KeV Ge<sup>+</sup>, 10 KeV B<sup>+</sup> plus annealing, there are no dislocation loops. Increasing the Ge<sup>+</sup> energy to 170 KeV, results in a band of dislocation loops below the c/a interface.

In this investigation, the Ge<sup>+</sup> ions (60, 170 KeV) and B<sup>+</sup> ions (10 KeV) have sufficient energy to displace Si atoms from their equilibrium sites. Under suitable annealing conditions, such as the three step anneal used in this study, most atoms will be restored to substitutional sites. The radii of Si, Ge and B are 1.17 Å, 1.22 Å and 0.9 Å respectively. Therefore, boron occupation at substitutional sites will cause localised shrinkage and Ge occupation at substitutional sites will cause localised lattice expansion. In the region of recoil damage just below the c/a interface if there are roughly equal number of B and Ge atoms, their opposing lattice distortions can be compensated and prevent the formation of dislocation loops.

There is a hypothesis for explaining the absence of DLs and requires that the lattice strain in the vicinity of the c/a interface be minimised by a net volume compensation between the Ge and B atoms occupying substitutional sites in the silicon lattice (11). In silicon implanted with  $3 \times 10^{14}/\text{cm}^2$ , 60 KeV Ge<sup>+</sup> followed by  $3 \times 10^{15}/\text{cm}^2$ , 10 KeV B<sup>+</sup> and furnace annealed at 800 C no dislocation loops were observed (11). In this investigation, no dislocation loops were observed for silicon implanted with  $4 \times 10^{14}/\text{cm}^2$ , 60 KeV Ge<sup>+</sup> followed by  $3 \times 10^{15}/\text{cm}^2$ , 10 KeV B<sup>+</sup> and annealed, confirming the earlier finding.

Results from the TRIM computer simulation program in Sections 3.1.1 and 3.1.2 can be used to further support the volume and strain compensation postulate (11). The data from TRIM in support of the volume/strain compensation mechanism, includes the following:

- 1) Ion Ranges for 60 KeV Ge<sup>+</sup> and 10 KeV B<sup>+</sup> ions.
- 2) Distribution of Collision Events (vacancies) for the ions above.

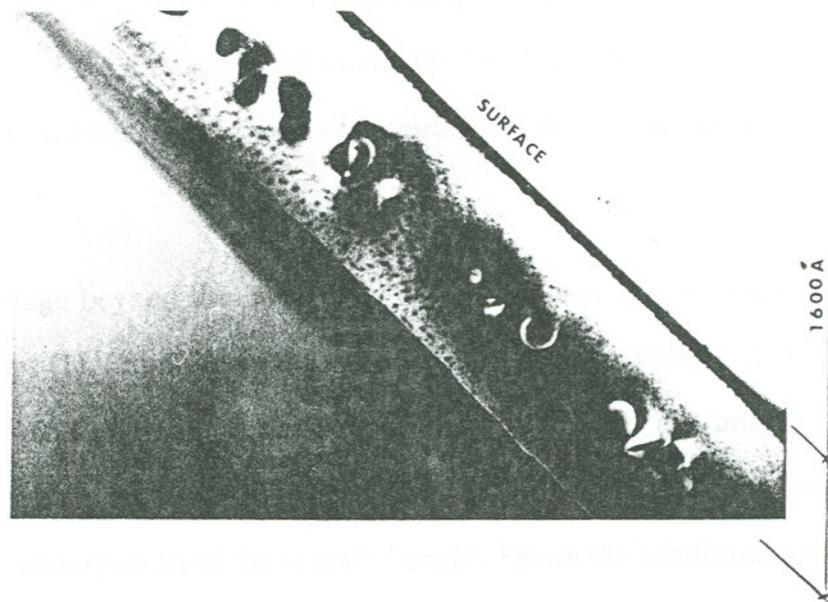


Figure 4.5: Boron dose reduced from  $3 \times 10^{15} \text{ cm}^{-2}$  to  $1 \times 10^{15} \text{ cm}^{-2}$ . Same dislocation density as Figure 4.4.

The Ion ranges for 60 Kev Ge<sup>+</sup> and 10 Kev B<sup>+</sup> ions are shown in Figures 4.6a and 4.6b and they match quite well. The Collision Events is a measure of the vacancies produced. Comparing Figures 4.7a and 4.7b, the distribution of vacancies for the Ge<sup>+</sup> and B<sup>+</sup> ions is comparable. The B<sup>+</sup> dose in this investigation is roughly 10x the Ge<sup>+</sup> dose and hence the vertical scale in the B<sup>+</sup> Collision Events plot has to be multiplied by 10 to compare with the plot for Ge<sup>+</sup>. Since the damage distributions for the 60 Kev Ge<sup>+</sup> ions and the 10 Kev B<sup>+</sup> ions are similar, volume compensation is expected in the regions where the Ge<sup>+</sup> and B<sup>+</sup> ions co-exist.

The recoil damage beyond the amorphous layer is responsible for the evolution of the dislocation loops (1). From Figure 4.2, the 60 KeV Ge<sup>+</sup> ions produce an amorphous layer approximately 650 Å thick. From Figures 4.7a and 4.7b, not only do the damage distributions match quite well but also the amount of damage at a depth greater than 650 Å is only a very small fraction of the overall damage. Hence the conditions are favorable for minimising the lattice distortion and preventing the nucleation of dislocation loops.

Using a similar argument, the results from TRIM show that in (100) Si the ion ranges and damage distributions differ significantly for 170 Kev Ge<sup>+</sup> ion implant and 10 Kev Be<sup>+</sup> ion implant. For dual implants of 170 KeV Ge<sup>+</sup>/10 KeV B<sup>+</sup>, there is significant recoil damage beyond the c/a interface and hence dislocation loops are formed during subsequent annealing. The results from TRIM and XTEM for dual implants of Ge<sup>+</sup>/B<sup>+</sup> in silicon show that the volume and strain compensation hypothesis can be used to explain the presence and absence of dislocation loops.

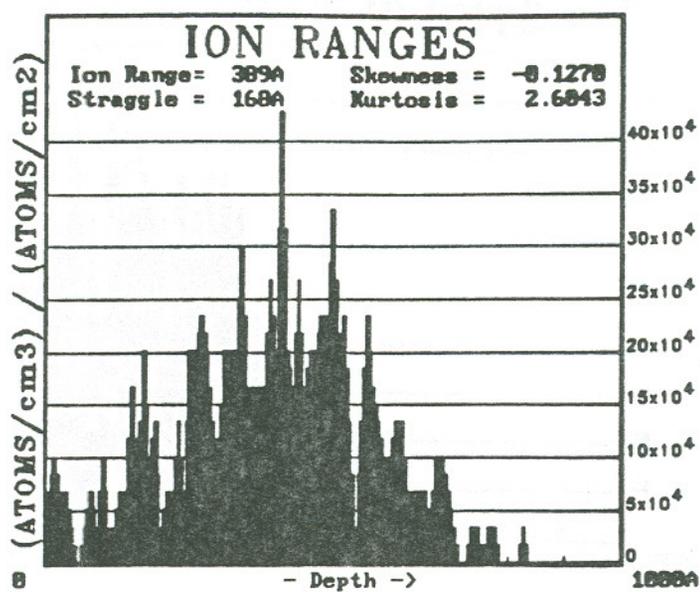


Figure 4.6a: TRIM plot of ion ranges for 10 KeV B<sup>+</sup> ions.

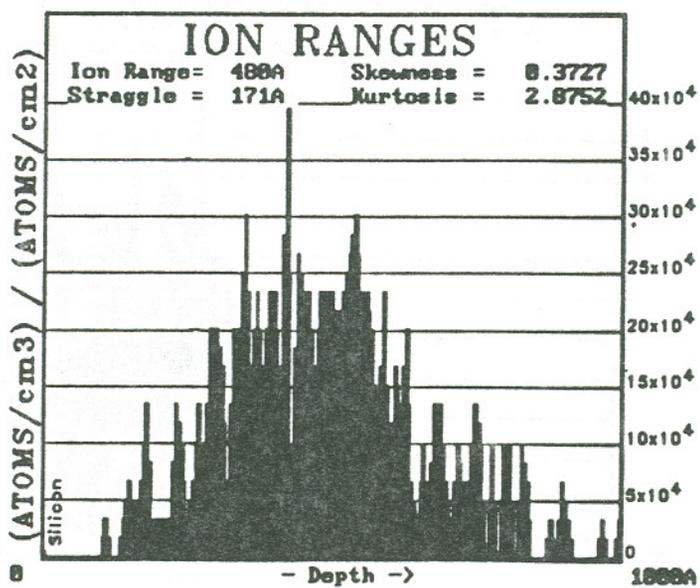


Figure 4.6b: TRIM plot of ion ranges for 60 KeV Ge<sup>+</sup> ions.

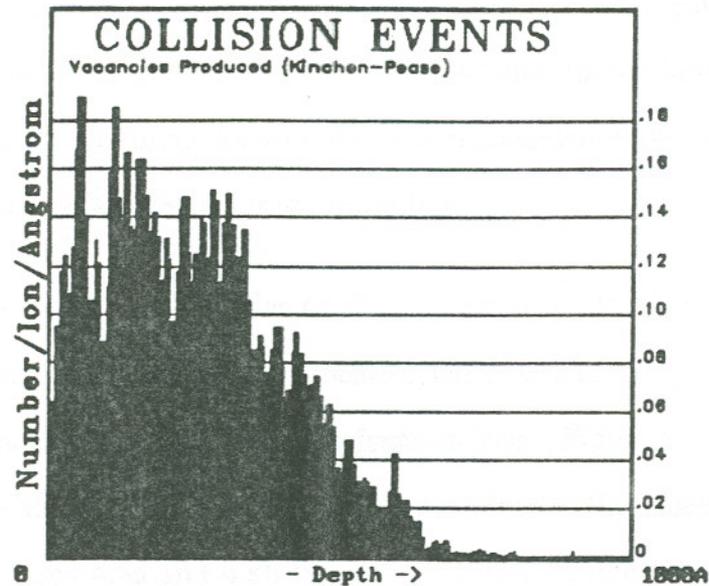


Figure 4.7a: TRIM plot of collision events (vacancies) for 10 KeV B<sup>+</sup> ions.

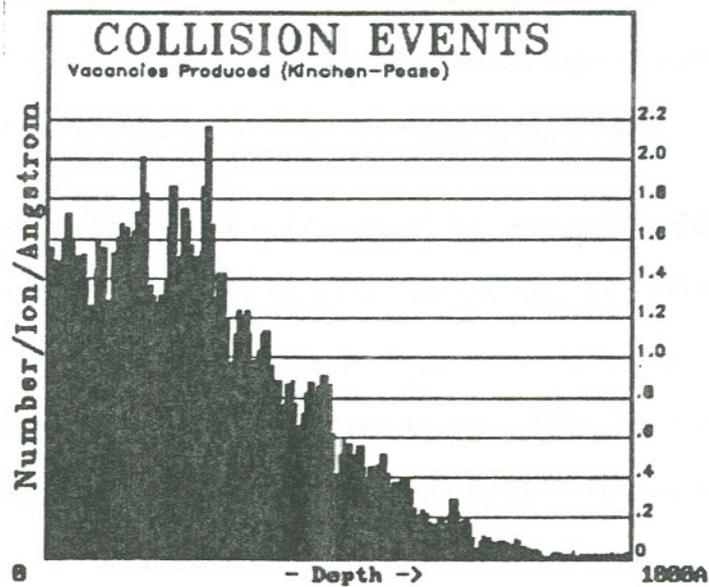


Figure 4.7b: TRIM plot of collision events (vacancies) for 60 KeV Ge<sup>+</sup> ions.

Is this hypothesis valid when Ge<sup>+</sup> is replaced by As<sup>+</sup>? Arsenic (radius=2.00 Å) like germanium (1.17 Å) is larger than silicon (1.12 Å) and causes lattice expansion. The implant and annealing conditions for As<sup>+</sup>/B<sup>+</sup> were maintained to be the same as those for Ge<sup>+</sup>/B<sup>+</sup>. The results are similar and presented below.

Figures 4.8a and 4.8b are representative of silicon implanted with 4e14/cm<sup>2</sup>, 60 KeV As<sup>+</sup> followed by 3e15/cm<sup>2</sup>, 10 KeV B<sup>+</sup> and annealed. The dose and energy are the same as for the Ge<sup>+</sup>/B<sup>+</sup> treatment that eliminated the dislocation loops, Figure 4.3. In the case of As<sup>+</sup> pre-amorphisation, the dislocation loops are not completely eliminated but the number is very few as in Figures 4.8a and 4.8b taken from different regions. It is reasonable to expect that by adjusting the As<sup>+</sup> and B<sup>+</sup> implant parameters the dislocation loops can be eliminated after annealing. Increasing the As<sup>+</sup> ion energy to 170 KeV but maintaining the same dose levels and annealing schedule, the representative XTEM microstructures are shown in Figures 4.9a and 4.9b. The dislocation loops are more in number than in Figure 4.8 but comparable to those for the 170 KeV Ge<sup>+</sup> ions in Figure 4.4.

The dislocation loops in Figures 4.8 and 4.9 are of the same type as those for the Ge<sup>+</sup> ion pre-amorphisation. The DLs form on (111) planes and  $\mathbf{b}=\mathbf{a}/2[110]$ . The edge-on orientation of the loops are also evident in Figure 4.9 and the interface is sharp. In conclusion, the differences in radii between the As and B atoms has a similar effect on the generation of dislocation loops as the Ge<sup>+</sup>/B<sup>+</sup> dual implants. The results from XTEM and TRIM for the As<sup>+</sup>/B<sup>+</sup> and Ge<sup>+</sup>/B<sup>+</sup> dual implants indicate that volume and strain compensation in the region of recoil damage below the c/a interface, may be responsible for eliminating or reducing the number of dislocation loops.

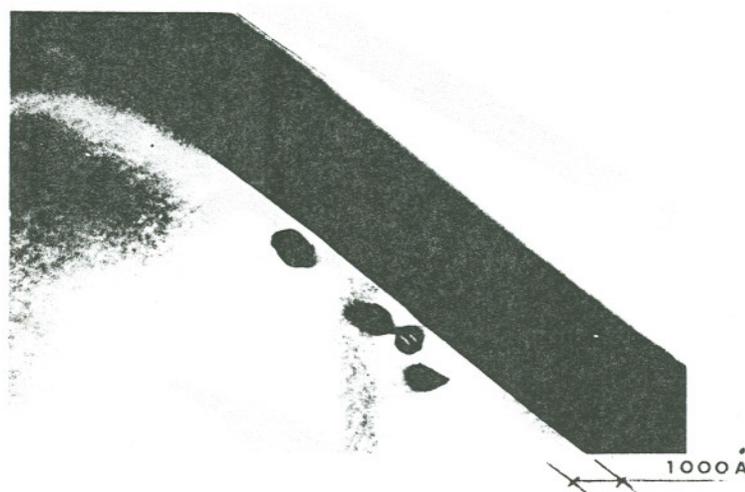


Figure 4.8a: 60 KeV As+/10 KeV B+ annealed. Isolated dislocation loops.



Figure 4.8b: Same treatment as in Figure 4.8a. Different region.

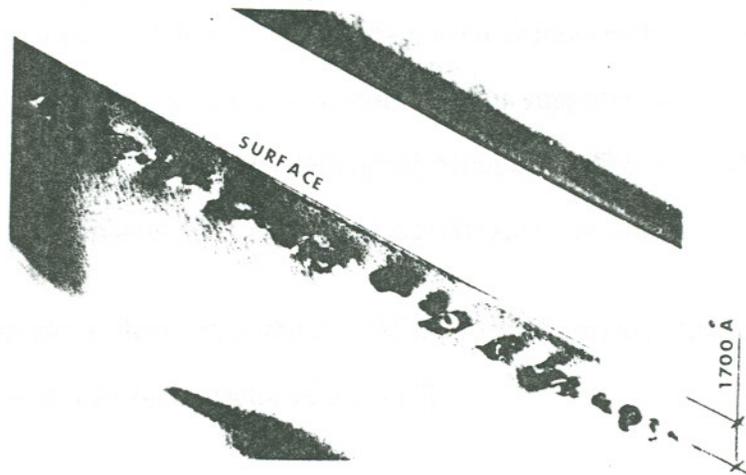


Figure 4.9a: 170 KeV As<sup>+</sup>/10 KeV B<sup>+</sup> annealed. Increased dislocation density.

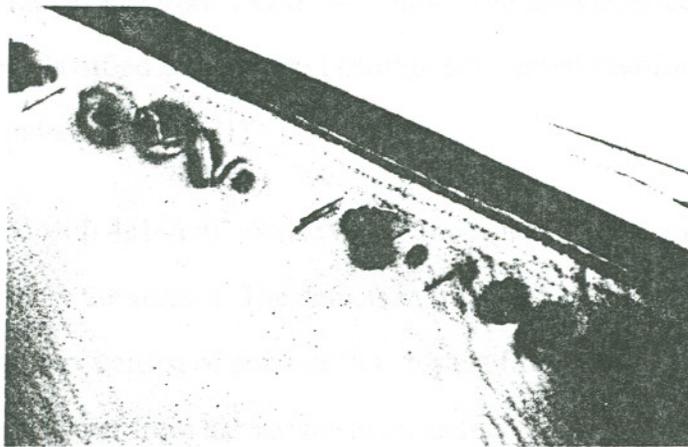


Figure 4.9b: Same treatment as Figure 4.9a. Different region.

## 4.2 CONCLUSIONS

- 1) The implantation induced defects can be eliminated or reduced by proper choice of implant parameters and annealing conditions. This is supported by the results from the XTEM microstructures and the damage distribution profiles for the 60 KeV Ge<sup>+</sup>/10 KeV B<sup>+</sup> implants and the 60 KeV As<sup>+</sup>/10 KeV B<sup>+</sup> implants.
- 2) All dislocation loops observed in the XTEM microstructures are extrinsic and form on (111) planes with a Burgers vector of  $a/2[110]$ .
- 3) There is good agreement between the XTEM observations of the dislocation loops and estimates from TRIM of the location of the defect band. Specific examples are given below:
  - 3.1) In Si implanted with 10 KeV B<sup>+</sup>, the location of the DLs is in good agreement with the projected range ( $R_p$ ) from TRIM simulation. The defects induced by the B<sup>+</sup> ion implant can be classified as Category I damage per current classification of ion implantation induced defects (1).
  - 3.2) In Si implanted with  $4 \times 10^{14}/\text{cm}^2$ , 60 KeV Ge<sup>+</sup> (no anneal), there is a narrow defect band 650 Å below the surface. The defects in the band, less than 50 Å wide, are not resolvable and may consist of point defect clusters from recoil damage. The presence of an amorphous layer from the surface to the defect band is confirmed by TEM micro diffraction. The thickness of the damage layer is consistent with the estimates from the recoil damage distribution using TRIM.

- 3.3) In Si implanted with 170 KeV Ge<sup>+</sup>/10 KeV B<sup>+</sup> and annealed, the extrinsic dislocation loops are located 1500-1600 Å from the surface in agreement with estimates from TRIM.
- 4) As<sup>+</sup> pre-amorphisation has a similar effect on the dislocation density as Ge<sup>+</sup> pre-amorphisation. The volume and strain compensation hypothesis proposed for Ge<sup>+</sup>/B<sup>+</sup> (11) is also applicable for As<sup>+</sup>/B<sup>+</sup> implants.

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## CHAPTER 5

### DIODE LEAKAGE CURRENTS OF p+/n JUNCTIONS

#### 5.0 INTRODUCTION

In Chapters 3 and 4 the emphasis was on characterising the damage from the ion implantation process using computer simulation programs and direct observation of defects in the TEM. It was shown that the processing conditions can eliminate or create defects such as dislocation loops. Direct observation of the defects in the TEM were shown to be in good agreement with computer simulation of the damage profiles.

The one remaining issue is to evaluate the effect of the processing variables on the electrical performance. The quality of p+/n junctions is assessed by measuring the leakage currents in diodes under reverse bias. The leakage current measurements will be correlated with observations of the lattice damage and recovery discussed in Chapters 3 and 4.

There are excellent treatments on the physics of p/n junctions including some of the original works (1-4). The primary issue is the role of structural defects on the I-V curve. Is there a specific contribution of the defects to the the diode current? Shockley's original expressions adequately predict the I-V characteristics of a narrow band gap Ge p/n junction, which is considered an ideal case (1). There are no traps and no generation currents in the depletion layer (space charge region at the metallurgical junction). For a wide band gap material such

as silicon, there is deviation from the ideal case due to many factors, significant among which is the generation and recombination (G-R) of carriers in the depletion layer (4).

There are two types of recombination: (a) Direct recombination in which an electron in the conduction band and a hole in the valence band recombine without assistance of any intermediate states; and (b) Recombination by the trapping of electrons and holes by localised energy levels deep in the forbidden energy gap. These energy levels are associated with certain impurities and structural defects (4). Dislocations are an example of the structural defects. The latter is commonly observed in silicon which is doped and/or subject to radiation (4).

Under non-equilibrium conditions, such as the application of a bias voltage to the p/n junction, the following will be observed (4):

- 1) Recombination of the carriers may dominate in the space charge region when a p/n junction is forward biased.
- 2) Generation of current carriers may dominate in the space charge region when a p/n junction is reverse biased.

Generation currents are leakage currents which are activated if the non-equilibrium driving force is a reverse bias or a source of photons. It is not customary to operate a diode in the reverse bias mode and leakage currents in the range of  $10^{-8}$  to  $10^{-9}$  amps are acceptable.

In this Chapter, the leakage current measurements will be analysed with reference to the defect locations. For the processing conditions used in this study, the diodes exhibit very low leakage currents and hence the junctions can be considered as high quality.

## 5.1 RESULTS AND DISCUSSION

In order to correlate the diode leakage currents and the defect structures, the following information is required:

- 1) Location of the defects.
- 2) Location of the depletion region relative to the defects.
- 3) Measurements of the leakage currents.

The leakage currents reported below correspond to a reverse bias of -5 volts. The location of the defects is obtained from the XTEM results in Sections 4.1.2 and 4.1.3. The depletion region width can be calculated since the dopant concentrations are known. The background dopant concentration is  $N_D = 1e16/cm^2$ . The acceptor (boron) concentration is estimated as  $N_A = 1e20/cm^2$  from the annealed B profile generated by Suprem III and discussed in Section 3.1.3. The depletion widths of the p+ and n type regions were calculated using expressions from text books (4,5).

The total depletion width is estimated to be 3700 Å at zero bias, assuming an abrupt B profile. The assumption of an abrupt B profile is supported by the data from Suprem III, in Section 3.1.3. When a reverse bias is applied, the built-in potential is increased by the amount of the bias voltage and this in turn increases the depletion width. Since the concentration of the p-type dopant (B) is much higher than the the n-type dopant, the depletion width on the p+ side is negligible. The depletion width is almost entirely contained in the n-type region.

The leakage currents corresponding to a reverse bias of -5 V are tabulated in Table 5.4 below.

Table 5.4  
Leakage Currents for Furnace Annealed Wafers

| TREATMENT                                      | JUNCTION DEPTH | DEFECT LOCATION      | LEAKAGE CURRENT |
|--|----------------|----------------------|-----------------|
| 3e15 cm <sup>-2</sup> /10 KeV B+, annealed     | 4900 A         | 500 A                | 8e-11 amps      |
| 4e14/60 KeV Ge+<br>3e15/10 KeV B+<br>annealed  | 4800 A         | No dislocation loops | 7e-11 amps      |
| 4e14/170 KeV Ge+<br>3e15/10 KeV B+<br>annealed | 4500 A         | 1500-1600 A          | 1e-9 amps       |

For the above treatments, the leakage currents are extremely low. The defects are located at a shallower depth compared to the metallurgical junction. The defects are entirely in the p+ region and far removed from the junction. The minimum separation between the defect band and the junction is at least 3000 A. The edge of the depletion layer in the p+ region is very close to the junction and hence the defects are far removed from the edge of the depletion layer. Since the depletion layer is free from traps such as dislocation loops, the leakage currents are very low.

A second batch of samples were subjected to a rapid thermal anneal instead of the three step furnace anneal. The implanted samples were annealed at 600 C for 60 minutes to promote regrowth of the amorphous layer and activate the dopant. Then the wafers were subject to a rapid thermal anneal at 1050 C for 30 sec. The leakage currents are in the nano amp range

and are acceptable although not as low as for the furnace annealed samples. The leakage currents for the RTA samples are given in Table 5.5 below.

Table 5.5  
Leakage Currents for RTA Wafers

| TREATMENT                     | LEAKAGE CURRENT |
|-------------------------------|-----------------|
| 10 KeV B+ and RTA             | 8e-11 amps      |
| 60 KeV Ge+/10 KeV B+ and RTA  | 5e-9 amps       |
| 170 KeV Ge+/10 KeV B+ and RTA | 1e-10 amps      |

By modifying the RTA schedule, the leakage currents can be increased or decreased. The annealing times in the RTA are of very short duration, typically 10-30 seconds, and the dislocation loops are not likely to be annihilated. It would be of interest to correlate the location of the defect bands from XTEM with the location of the metallurgical junction and leakage currents. The low values of leakage currents may be due to the dislocation loops being outside the depletion region although their relative positions are unknown in this investigation.

## 5.2 CONCLUSIONS

The conclusions from the leakage current measurements are as follows:

- 1) For the implant and furnace annealing conditions used in this investigation, the leakage currents are very low and hence the junctions are of high quality. Even though dislocation loops exist, they are located far from the edges of the depletion layer. Hence the dislocations do not act as traps which generate high leakage currents under bias.
- 2) Low leakage currents in the nano amp range have also been measured for diodes fabricated from RTA processed samples. The B diffusion depth will be much shallower for the RTA treatment compared to the furnace anneal treatment. This is a benefit in designing and fabricating shallow junctions for sub-micron devices.

### 5.3 REFERENCES

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### **BIOGRAPHICAL NOTE**

The author was born in Vizag, AP, India. He grew up in the city of Madras in southern India. He completed his B. Tech. in Metallurgical Engineering from the Indian Institute of Technology in Madras and Ph. D. in Metallurgical Engineering (Materials Science) from the University of Washington in Seattle. He has worked at Mannesmann Tally Corporation in Kent, Wa., in engineering and management positions. The author left industry to retrain and acquire new skills in an area close to materials science and hence his decision to pursue graduate studies at OGI. The author is married to Shoba and has a son Rajeev and a daughter Roshini.