MAJORITY VERSUS MINORITY
HOT-CARRIER INJECTION IN MOSFETs

Yuan Tang

B.S. Electrical Engineering
Changsha Institute of Technology, China, 1982

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The dissertation "Majority Versus Minority Hot-Carrier Injection in MOSFET s" by Yuan Tang has been examined and approved by the following Examination Committee:

Dae Mann Kim, Advisor
Adjunct Professor
Tektronix, Inc.

V. S. Rao Gudimetla
Assistant Professor

Raj Solanki
Associate Professor

Babak Sabi
Intel Corporation

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I dedicate this dissertation to my parents

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ABSTRACT

MAJORITY VERSUS MINORITY HOT-CARRIER INJECTION IN MOSFETs

Yuan Tang, Ph.D.

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Supervising Professor: Dae Mann Kim

A new model of MOSFET operation in the overthreshold region is proposed. Here, the two-dimensional Poisson equation is solved analytically, while the current continuity equation is solved iteratively in a self-consistent feedback scheme. As a result, both the channel field and the surface mobile charge distributions have been quantified over the entire region of the device operation. Additionally, a simple working model of the maximum channel field E_L at given device bias has been devised. The accuracy of this model has been tested experimentally.

This new E_L-model has been applied to investigate the hot-carrier effects in MOSFETs. Specifically, the concept of majority vs. minority hot-carrier injection into the gate oxide is introduced. With this concept, the hot-carrier induced device degradation in the n- and p-channel MOSFETs is analyzed from a unified viewpoint. This E_L-model is further used to examine, theoretically and experimentally, the device lifetime.

CHAPTER 1

Introduction

Today's integrated circuits owe their rapid increase in levels of integration to the technology development of MOSFETs, which stands for Metal-Oxide-Silicon Field Effect Transistors. Up to the late 1960's, the semiconductor device technology was primarily centered around bipolar transistors. At that point in time people saw the emergence of MOSFETs, and a concomitant rapid increase in levels of integration. MOSFETs dissipate much less power than bipolar devices and therefore can be employed at much greater packing densities. Furthermore, yields of MOSFETs, especially at small dimensions, are greater than those of bipolar devices due to a much lower process complexity. Another basic advantage of MOSFETs over bipolar transistors is their inherent self isolation, that is, adjacent transistors do not interact unless there is a surface channel between them. This property avoids the need for the pn-junction-isolated wells used in conventional bipolar technology and results in a substantial area saving for MOSFET circuits over bipolar circuits. Therefore we talk of very large levels of integration today, we generally refer to the status of MOSFETs.

The chronological advances of MOSFETs are divided into three phases:

1. The discovery phase from the patent disclosure of the field effect conductance modulation in 1928 by Lilienfeld to the invention of the enhancement-

mode inversion-layer MOSFET in 1960 by Kahng and Atalla;

2. The basic technology development phase from the MOS C-V technique in 1961 by Moll and Terman to the one-transistor dynamic-random-access memory (DRAM) cell in 1968 by Dennard;

3. The advanced development and volume production phase from 1 kilobit DRAM in 1970 to the present application-specific microprocessor and 4-megabit DRAM [1].

The evolution of MOSFET technology has been symbolized with the shrinking of the channel length. At the early stage of the technology, a channel length of 50 μm was typical. The corresponding small scale integration is in an order of 2^1-2^6 (2-64). Today channel length of 1 μm is becoming conventional and several million transistors can be integrated into one chip. It is predicted that by the year 2000, a 256M-byte flash memory using 0.25 μm geometry on a side of 0.7 inch die is projected to sell for $1 per megabyte. Here each cell of the memory is equivalent to one MOS transistor [2].

When the dimension is scaled down, the problems are numerous, and the potential solutions are even more numerous. For example, X-ray and electron beam lithography technique is used to improve resolution; refractory silicide technique is used to increase conductivity and lightly doped drain and various gate spacer structures are used to enhance the device reliability.

Aside from questions such as electromigration, electron static discharge (ESD), and punchthrough below the channel region, the "hot-carrier" issue is

a major reliability concern especially for short channel MOSFETs. The phenomenon is best understood with reference to Fig. 1-1 where schematic cross section of a MOSFET is plotted. The channel lateral field close to drain end E_L is very high, when the MOSFET is operated in the saturation region, i.e, $0 \leq |V_G - V_T| \leq |V_D|$, here V_G, V_D and V_T denote the gate bias, drain bias and threshold voltage respectively. Gaining enough energy from the field, the channel carriers (electrons for n- and holes for p-channel devices) react with the lattice violently and cause impact-ionization, thereby creating electron-hole pairs. Since both the channel carrier and generated electron-hole pairs are associated with high energy, they are called hot-carriers. A fraction of these hot-carriers have the chance to overcome the potential barrier at the interface and are get trapped in the oxide. The resulting device degradation is usually measured by the parameter shifts in transconductance Δg_m, threshold voltage ΔV_T and saturated drain current ΔI_{DSAT}. This hot-carrier injection induced device degradation is known as the hot-carrier effects. Since the lateral channel field increases with decreased channel length, the hot-carrier effects are aggravated in short channel MOSFETs. It is therefore important to study these hot-carrier effects when the channel length is scaled down to a quarter of a micrometer.

In Chapter 2, a new formulation is presented for modeling E_L, which triggers the hot-carrier effects. In Chapter 3, the hot-carrier effects in p-channel MOSFETs is examined both experimentally and theoretically, and a two-region bias model is introduced. In Chapter 4, the two-region bias model

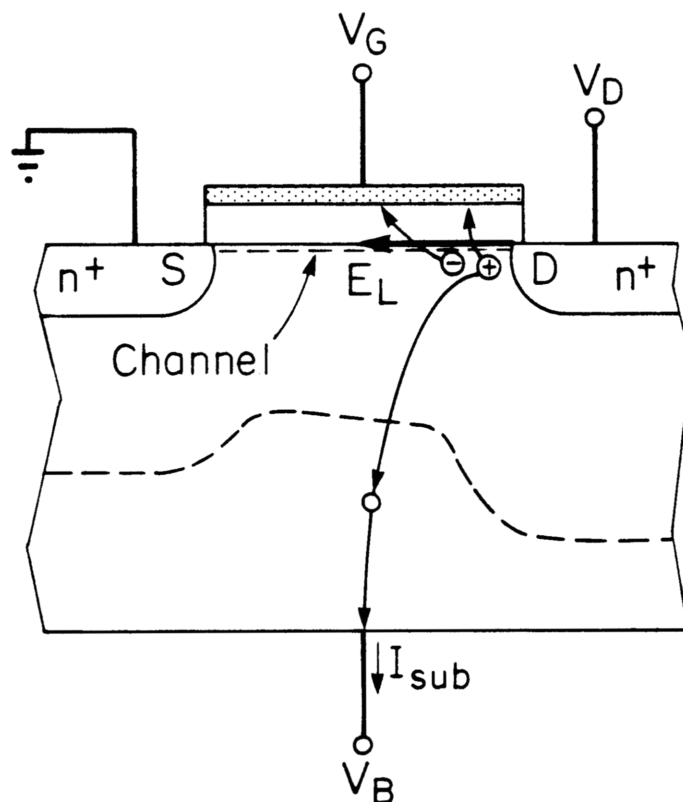


Fig. 1-1 The schematic cross section of a n-channel MOSFET. When the device is biased in the saturation region $0 < V_G - V_T < V_D$, the very high lateral channel field E_L triggers both impact-ionization and hot-carrier injection into the oxide.

is extented to the n-channel case, describing thereby the hot-carrier effects in MOSFETs from a unified viewpoint. The new model of E_L is utilized to characterize the substrate current I_{SUB} and gate current I_G . These currents are important predictors of hot-carriers effects in MOSFETs. The excellent agreement achieved between the theory and the measurements verifies the two-region bias model for hot-carrier injection. In Chapter 5, the E_L-model is further applied to the study of device lifetime.

CHAPTER 2

On-State MOSFETs Operation Modeling

2.1 Introduction

The channel field at drain end, E_L has long been recognized as the critical element in hot carrier effects in MOSFETs [3]. Specifically, when a MOSFET is operated in the saturation region, $0 < |V_G - V_T| < |V_D|$, the field is so high that it can trigger both impact ionization and injection of hot carriers into the oxide. Therefore, a proper estimation of E_L is fundamental to the study of the hot carrier effects. A model estimating E_L as a function of device biases and parameters, has been presented [3]. However, when this model is substituted into the well known expression of substrate current [4], the bell-shaped substrate current versus gate bias observed in saturation region can not be reproduced. In order to understand the discrepancy between the theory and the observation, it is necessary to emphasize why the channel field E_L can reach such a high value in the saturation region.

The answer can be found by tracing back to the device operation in the linear region, as simulated in the classical GCA (Gradual Channel Approximation) method [5],[6]. The core of GCA is the expression ((8.3.16) of [5]) of mobile charge density, Q_m, in terms of device biases and parameters. In this expression, the amount of carriers induced in a channel position by a given gate bias is further modulated by the drain bias V_D . The closer is the

position to the drain, the more are the carrier there to be drained away. Less carrier density (Q_m) in a position will induce more voltage drop and higher channel field, E, therein. The product of Q_m and E remains constant, so that drain current I_D is a constant (current continuity). Since the drain end of the channel has the least carrier density, it has the maximum channel field E_L. The same V_D will produce a higher E_L for a smaller $|V_G|$, since there are less induced carriers to be drained away.

Since GCA method simulates this "draining away" process simply and clearly, it has been taken as guide to understand the MOSFET operation. Unfortunately, as an approximation, the GCA results in $Q_m = 0$ for $|V_D| = |V_G - V_T|$ ((9.1.7) of [5]). Hence the analysis becomes ineffective beyond this point. The discontinuity of a model does not mean the discontinuity of the device physics. In fact, Q_m can not reach zero at any drain voltage less than infinity [7]. Instead, when V_D is increased beyond the saturation point, the mobile charge sheet close to drain is drained off to become thin to the extent that this condition is described as the channel "pinch-off". This thinness of Q_m immediately illustrates the highvalue of E_L in the saturation region. Therefore, a model which can characterize E_L properly beyond the pinch-off has to be a model which can describe this "draining away" process, in terms of small but finite Q_m.

The numerical simulation is obviously one choice of qualified approaches. By solving both Poisson and current continuity equations one grid point by

another (p.500 of [5]), this method can take even detailed device effects into rigorous consideration. However, in addition to its considerable consumption of computer time, this way of calculation makes it difficult to visualize and extract principles of device operation.

A two-section approach [8], from which the prevailing E_L model [3] was derived, has been devised to characterize analytically the MOSFET operation in the saturation region. The basic idea of this approach is to find E_L's dependency on given biases by considering the size of the rectangular drain section, as shown in Fig. 2-1. Here, the depletion edge of the drain section, x_1, is determined by V_G. The extension of the drain section in lateral direction ΔL is equalized to the increment of drain current, ΔI_D ((8),(9) of [8]), and hence, according to Ohm's law ((7) of [8]), the increment of drain bias, ΔV_D. Varying with the size, the amount of charge contained in the section then determines E_L ((13) of [8]) by Gauss's law. The approach can be summarized using a flow chart of $E_L \propto$ total charge $\propto \Delta L \propto \Delta I_D \propto \Delta V_D$.

In this two-section approach, **mobile charge distribution** and the current continuity condition have not been considered. Therefore, the main reason for E_L attaining a high value in the saturation region i.e, the "draining away" process, has not been taken into account. This point can be further clarified by considering a lateral field component normal to the bold line in Fig. 2-1. As a result of 2-D numerical simulation [9], the potential contours in the figure indicate that the lateral field component is strong **at the sur-**

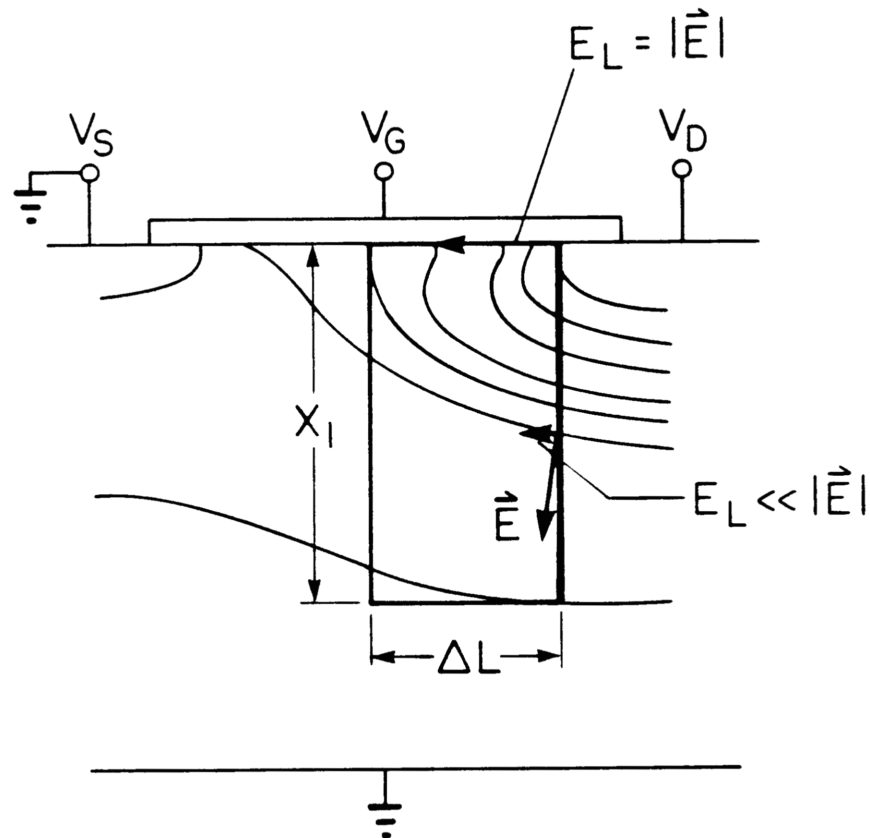


Fig. 2-1 A computer simulation result of 2-D potential contours, for an n-channel MOSFET biased in the saturation region ($V_G - V_T = 2$ V, $V_D = 5$ V). Along the bold boundary of the rectangular drain section, the strength of the lateral field declines drastically from the surface down to the depletion edge, as evidenced by the direction change of the potential contours.

face (perpendicular to the contours), and weak **at depletion edge** (nearly parallel to the contours). This **distinctive** variation in the lateral field is due to the fact that the channel field is strongly influenced by the current continuity condition (or the "draining away" process), while the field in the depletion region is mainly determined by Poisson equation. Without introducing the mobile charge density, the 2-section approach could not incorporate this essential distinction. Instead, E_L was assumed to be constant along the bold line and was taken out of the integration ((13)-(14) of [8]). Since the approach has reflected only one aspect of device physics, it is valid in showing device output characteristics, but when used to characterize E_L, both the approach and its simplified version [3] underestimate E_L .

In this chapter, we report a new approach of modeling E_L, utilizing a self-consistent feedback scheme for characterizing MOSFET operation in overthreshold region. In this approach, Poisson's equation is solved analytically, while current continuity equation is solved iteratively to specify simultaneously both the mobile charge and channel field distributions along the surface. Since the resulting channel field is very sensitive to a given mobile charge distribution, the iteration converges fast. The speed of the calculation is comparable to that of an analytical approach. The essence of this approach is in line with the GCA method. Both methods accomplish characterizing the on-state of device operation by evaluating the mobile charge distribution along the surface. The difference between the two, however, is that this feedback scheme further enables the evaluation of Q_m and E in the saturation

region.

In this approach, the physical processes operative in the saturation region are simply a natural continuation of those in the linear region. Because of this unified treatment of two bias regions, partitioning the channel into two sections becomes unnecessary. By highlighting the "draining away" process, this approach also enables the extraction of a simple version of E_L model in the saturation region.

In Sec. 2.2, the methodology is described. In Sec. 2.3, the results are presented. The discussion includes the comparison of the extracted E_L model with the prevailing E_L model. In Sec. 2.4, the concluding remarks are made.

2.2 Model Description

By solving both Poisson and current continuity equations in the cross-section shown in Fig. 2-2. the MOSFET operation in the overthreshold region, can be characterized.

2.2a Solving Poisson Equation Analytically

Using the coordinates given in Fig. 2-2, the 2-dimensional Poisson equation can be written as,

$$\nabla^2\phi(x,y) = -\frac{qN_A(x,y)+Q_m(y)\ \delta(x-T_{ox})}{\epsilon_{si}} \quad \text{for } x \geq T_{ox} \qquad (2\text{-}1)$$

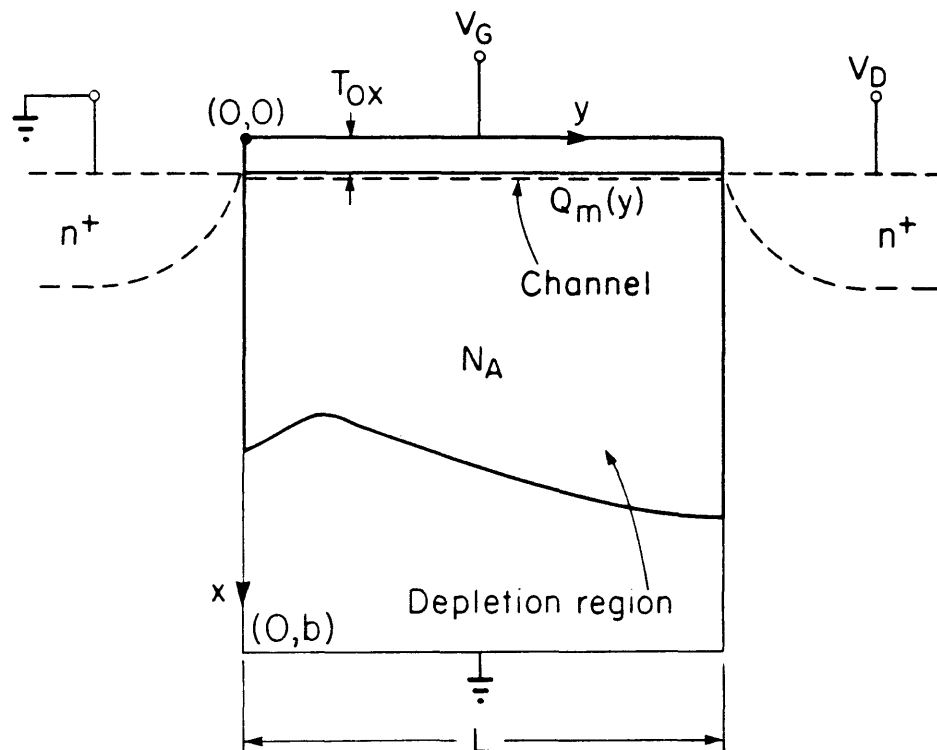


Fig. 2-2 The schematic cross section of an n-channel transistor in which the Cartesian coordinate (x,y) is indicated. The depletion region is charged with doping concentration N_A, and a sheet of mobile carrier is distributed along the surface, when the device is at on-state.

with T_{ox} representing the thickness of the oxide; $\phi(x,y)$ the potential at point (x,y); $qN_A(x,y)$ the fixed charge distribution of substrate doping in the depletion approximation; and $Q_m(y)$ (C/cm^2) the mobile charge distribution along the channel. The carrier sheet is taken to be located at the surface by the δ-function [7].

In this chapter, two techniques developed for solving (2-1) analytically have been adopted from Ref.[10], which modeled MOSFET in the underthreshold region;

(a) Green's theorem in which the Green's function on the boundaries is zero for the Dirichlet boundary conditions. The potential distribution $\phi(x,y)$ is,

$$\phi(x,y) = \int\int \frac{\rho(x',y')}{\epsilon} G(x,y;x',y')dx'dy' - \int \phi(x',y') \frac{\partial G}{\partial n'} ds' \qquad (2\text{-}2)$$

where $\rho(x',y')$ represents the total charge distribution on the right hand side of Poisson equation (2-1), $\nabla^2 G = -\delta(x-x')\delta(y-y')$, $\phi(x',y')$ is the potential distribution on the boundaries, n is the outward direction on the boundaries, and ϵ is the dielectric permittivity that is a constant for a homogeneous system.

(b) An image charge transformation technique. In this technique, the image charge densities are introduced at each side of the Si/SiO_2 interface, so that $\phi(x,y)$ must satisfy the continuity of both the transverse electric field and normal electric displacement at the interface. This technique enables a

rigorous analysis of the problem associated with different dielectric permittivities of the oxide and the silicon substrate. The technique is especially useful for obtaining the potential at the interface. The interface potential is most sensitive to the difference of the dielectric constants.

Since we have used the same rectangular geometry in Fig. 2-2 as that used by Lin & Wu [10], the series-form Green's function [11] and the details of these two techniques, can be used here. However, distinctions existing in determining boundary conditions, depth of the depletion region, and the contents of $\rho(x,y)$ between under- and over-threshold cases have to be considered.

As shown in Fig. 2-2, when the bias changes from under- to over-threshold region, the method of Ref.[10] can be directly applied in deciding potentials on gate electrode ($x=0$, $0 \le y \le L$), on substrate ($x=b$, $0 \le y \le L$), and on the two edges of oxide ($0 \le x \le T_{ox}$, $y=0$ and $y=b$), assuming that V_{GS} and V_{GD} are linearly distributed along the edges. However, since V_G is high in the overthreshold region, its influence on the left and right boundaries inside the substrate, ($T_{ox} \le x \le b$, $y=0$ and $y=L$), can no longer be neglected, in contrast with low V_G case. We will discuss the boundary conditions on these two lines in Section 2.2c. We also leave to Sec. 2.2c the modification required for determining depletion edge, hence the fixed charge distribution in the substrate. In the following, we determine the distribution of mobile charge sheet, $Q_m(y)$, which is zero for $V_G < V_T$ but should be incorporated in the charge term $\rho(x,y)$, in the Green theorem integration (2-2) for $V_G > V_T$.

It has thus far been made clear that the potential ϕ at any point (x,y), especially at the surface, can be uniquely determined if the total charge (mobile and fixed) distributions and boundary conditions are given.

2.2b Solving Current Continuity Equation Iteratively

The drain bias drops along the channel and ends at the source. Hence, the mobile charge density at the source end is independent of V_D and can be estimated as $Q_m(0) = C_{ox}(V_G - V_T)$ [5], where C_{ox} (F/cm^2) is the oxide capacitance. For the rest of channel positions $0 < y < L$, the density is initially estimated as $Q_{m,i}(y) = Q_m(0)\ r_i(y)$, with r(y) denoting an arbitrary, yet monotonously decreasing function, satisfying the conditions, $0 < r_i(y) < 1$ and $r_i(0) = 1$. For example, $r_i(y) = 1 - y/3L$. The subscript i indicates that the distribution except $Q_m(0)$ is hypothetical for the given biases V_G and V_D . However, $Q_{m,i}$ can be used anyhow as a possible mobile charge distribution for formally solving Poisson equation.

The deviation of $Q_{m,i}$ from the true distribution Q_m can be detected by the current continuity equation [6]. In overthreshold region, only the drift current component needs to be considered for simplicity, viz.

$$\mu(y)\ Q_{m,i}(y)\ E_i(y) = P_i \qquad 0 \le y \le L \qquad (2\text{-}3)$$

Here P_i is a constant and is proportional to I_D. The channel mobility, μ is in general a function of V_D and V_G via drift velocity saturation or surface scattering [5]. For simplicity of discussion, μ is treated as a constant; $E_i(y)$ is

the lateral channel field ($E(y) = -\partial\, \phi(T_{ox},y)/\partial y$), which is obtained by **solving Poisson equation from the given estimated mobile charge distribution** $Q_{m,i}(y)$.

Since (2-3) should be valid at any point along the channel, P_i can be evaluated at the source end, $P_i = \mu(0)\, E_i(0)\, Q_m(0)$. Obviously, if the obtained $E_i(y)$ is substituted into the left side of (2-3) and the equation can not be satisfied, i.e., the product of the three quantities at position y (> 0) is not equal to the given value at position $y = 0$ (P_i), $Q_{m,i}(y)$ is not the real distribution $Q_m(y)$.

By changing the form of (2-3) slightly, another round of distribution $Q_{m,i+1}(y) = r_{i+1}(y)\, Q_m(0)$, can be generated from existing $Q_{m,i}$ and E_i, viz.

$$r_{i+1}(y) = r_i(y) + \alpha \left(\frac{\mu(0)E_i(0)}{\mu(y)E_i(y)} - r_i(y) \right) \tag{2-4}$$

This $Q_{m,i+1}(y)$ again is to be used to get the corresponding $E_{i+1}(y)$. Here α ($<< 1$) is an adjustable constant used to control the iteration process of (2-4). As shown in (2-4), once (2-3) is satisfied, that is, if $(\mu(0)E_i(0))/(\mu(y)E_i(y)) - r_i(y) = 0$, the iteration converges, i.e, $r_{i+1}(y) = r_i(y)$, and $Q_{m,i+1} = Q_{m,i} = Q_m(y)$.

Eq. (2-4) is a feedback scheme, in which the current continuity equation (2-3) plays a complementary role with Poisson equation (2-1). Suppose that $|Q_{m,i}| < |Q_m|$ at point y, a smaller voltage drop will result from the Green's function integration in (2-2). Equivalently, a bigger $1/|E_i(y)|$ will result from

the differentiation of the surface potential. However, by (2-4), this 1/E leads to a positive compensation to the original carrier density, which makes $|Q_{m,i+1}|$ closer to $|Q_m|$ than $|Q_{m,i}|$ is. Similarly, the feedback scheme leads at any channel position, a negative compensation to the $|Q_{m,i}|$, if it is larger than what it should be. When the scheme produces a zero compensation along the channel, both equations (2-1) and (2-3) are satisfied. In this way, the solution can be found for any overthreshold bias, and the boundary between linear and saturation region has inherently vanished. Also, $Q_m(L)$, and E_L ($\equiv E(L)$) can be quantified simultaneously for $|V_D| > |V_G - V_T|$, no matter how thin $Q_m(L)$ has been drained to or correspondingly how high E_L is.

It has been found from the program execution that the resolved channel field E is sensitively dependent upon the carrier sheet density. In other words, the feedback is strong. With a close initiation, for example, using the carrier distribution, $Q_m(y)$ of a neighboring bias (0.2V apart), the solution for a given bias can be obtained within 4-5 loops.

The calculated distributions of the channel lateral field E and carrier density Q_m are shown in Fig. 2-3a as functions of channel position, y, for a linear bias of a n-channel device. The device is of $W/L = 20/0.9$ μm; doping density $N_A = 10^{16}$. The corresponding values calculated from GCA model [6] are also shown in Fig. 2-3a. At the source end, where $Q_m(0)$ and $E(0)$ calculated by these two different methods are same. This is to be expected, since these two methods should give identical $I_D \propto Q_m(y)\,E(y)$ in the linear region.

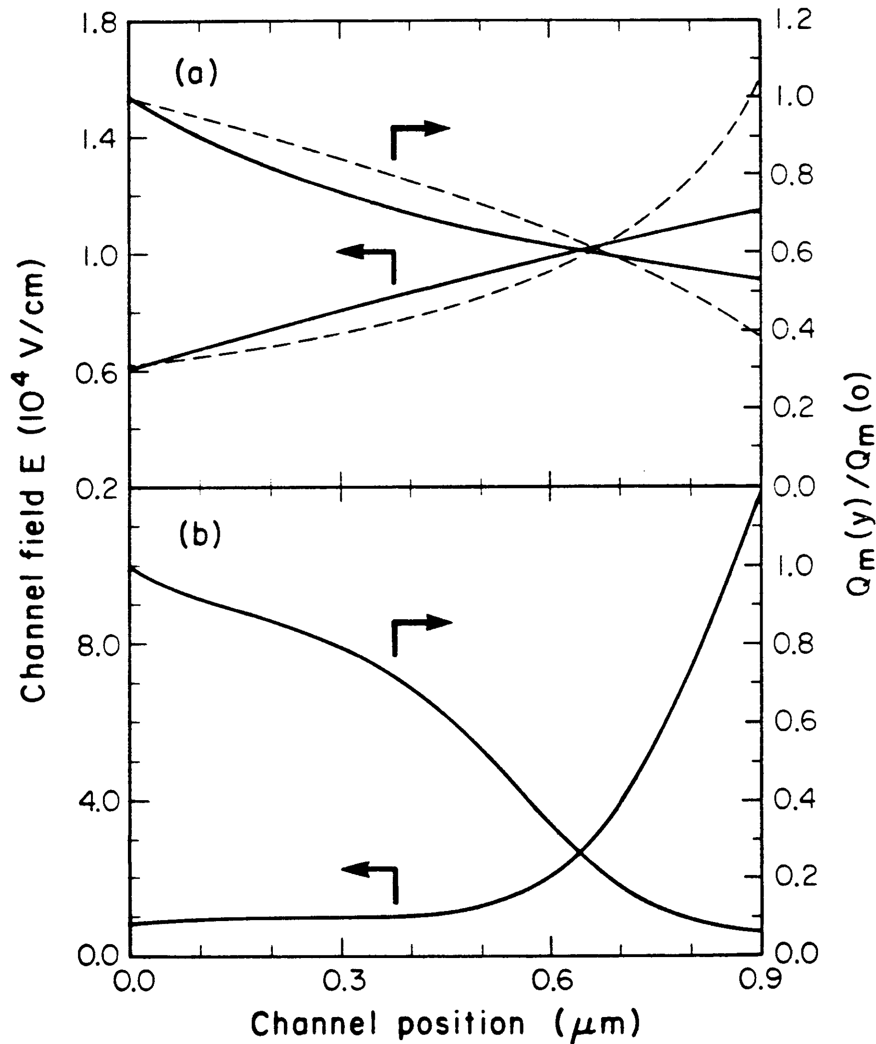


Fig. 2-3 Lateral channel field E(y) and mobile charge distributions $Q_m(y)$ calculated by the feedback scheme (solid line) and GCA method (dash line), (a) for a linear region bias ($V_G - V_T = 1.3$ V, $V_D = 0.8$ V), and (b) for a saturation region bias ($V_G - V_T = 1.3$ V, $V_D = 2.8$ V). The n-channel device is of $T_{ox} = 15$ nm, $W/L = 20/0.9$ μm, $N_A = 10^{16}$ cm^{-3}.

At the drain end, however, the GCA result of $Q_m(L)$ is lower and associated E_L is higher than those two values calculated by the feedback scheme. This shows clearly that the GCA method over-approximates the "drain away" process. In fact, according to GCA, E_L goes to infinity ($Q_m(L) = 0$) at the edge of linear region, as well documented [5]. According to the present feedback scheme, however, $Q_m(L)$ remains finite, although small, and E(L) is finite in the saturation region, as shown in Fig. 2-3b.

2.2c Involving V_G's Role in Affecting Boundary Conditions

As mentioned in Sec. 2.2a, in the overthreshold region, V_G's role in determining Dirichlet boundary conditions must be considered, along lines of Fig. 2-2 ($T_{ox} \leq x \leq b$, y=0 and y=L).

In Fig. 2-4a, the chest-shaped cross section bounded by bold lines is brought into Cartesian coordinates (s,t). In this expanded area, the one-dimensional potential distribution of a $p - n^+$ junction is used to the boundaries in the substrate (I-A) and (F-E). For the rest of bold boundaries, the determination of potential distribution is straightforward, and is detailed in Appendix 2-I. With all boundary conditions made available for a given bias, the potential on the lines (J-K and L-M) of the expanded area in Fig. 2-4a, can be obtained by solving Poisson equation in the expanded area. In this way, the role of gate bias, the boundary condition on line H-G, is included in the calculation. The resulting potential distributions along J-K and L-M can

Fig. 2-4 (a) The schematic cross section of an n-channel transistor in the coordinate (s,t), (b) with the conformal transformation in (2-5), the chest-shaped area in z (= s + it) plane is transferred into the upper-half of w (= u + iv) plane.

then be used as boundary conditions to get surface potential in the (x,y) coordinates of Fig. 2-2.

Green's theorem has again been employed in solving Poisson equation in the area shown in Fig. 2-4. Since no Green's function of Dirichlet boundary conditions exists for the chest-shaped area, the z (= s + it) plane has been transformed into w = u + iv plane shown in Fig. 2-4b by the conformal mapping,

$$z = \frac{2h}{\pi(1+\lambda)}\left[\tanh^{-1}\left(1-\frac{d_2}{w^2}\right)^{1/2} + \lambda\,\tanh^{-1}\left(1-\frac{d_1}{w^2}\right)^{1/2}\right] \qquad (2\text{-}5)$$

where, constants λ, h and d_1 and d_2 are dependents of the given device geometry T_{ox} and r. The detailed derivation of (2-5) can be found in Appendix 2-II. As a result, the area bound by bold lines in Fig. 2-4a is transferred into the upper-half plane in Fig. 2-4b, the bold boundary in z plane is transferred into the bold boundary in w plane, which is the real axis of the u-v coordinates. The Green's function of Dirichlet conditions for the upper-half plane is well known [12];

$$G(u,v,u',v') = \frac{1}{2\pi}\ln\left(\frac{(u-u')^2 + (v+v')^2}{(u-u')^2 + (v-v')^2}\right)^{1/2} \qquad (2\text{-}6)$$

which is zero for v = 0. By transferring all boundary conditions and charge distributions from z to w plane, the potential at point (u,v) of w plane or equivalently at (s,t) of z plane, can be found from the Green's integration,

$$\phi(u,v) = \int \frac{Q_m^w}{\epsilon} G ds' + \int\int \frac{qN_A^w}{\epsilon} G du' dv' - \int \phi \frac{\partial G}{\partial u'} du'. \qquad (2\text{-}7)$$

Here "w" indicates the charge distribution scaled by Jacobian factor at any point. In (2-7), the first term (contribution from Q_m) is a line integral along the dashed ellipse in Fig. 2-4b. The major and minor axes of the ellipse are calculated from the device geometry, T_{ox} and r. The third term (contribution from boundary conditions) is again a line integral along the u axis. The second term (contribution from N_A) is an area integration on the four sectors of the fan-shaped area. The boundary of the depletion region is approximated by connecting each two neighboring points of ABCDE in Fig. 2-4b with a piece of an ellipse. The lengths of axes for each ellipse, and lower/upper angular limits of the integral for each sector therefore can be determined by the positions of each two points.

Points A and E are located at the depletion edges at the source and drain ends. The depletion depth at the midpoint C is initially estimated by the simple expression, $(4\epsilon_{si}|\phi_p|/qN_A)^{1/2}$ with $\phi_p = 0.026 \ln(N_A/n_i)$ (volt). Points B and D can be reasonably placed. The positions of the three points C, B, D then are adjusted slightly by the computer until the calculated potentials from (2-7) are zero at the points on the depletion boundary (A-B-C-D-E).

With the depletion region thus specified, the potentials along the two lines (J-K) and (L-M) are calculated using (2-7). In Fig. 2-5, an example of the calculation is presented. Note that the potentials drop to zero at the

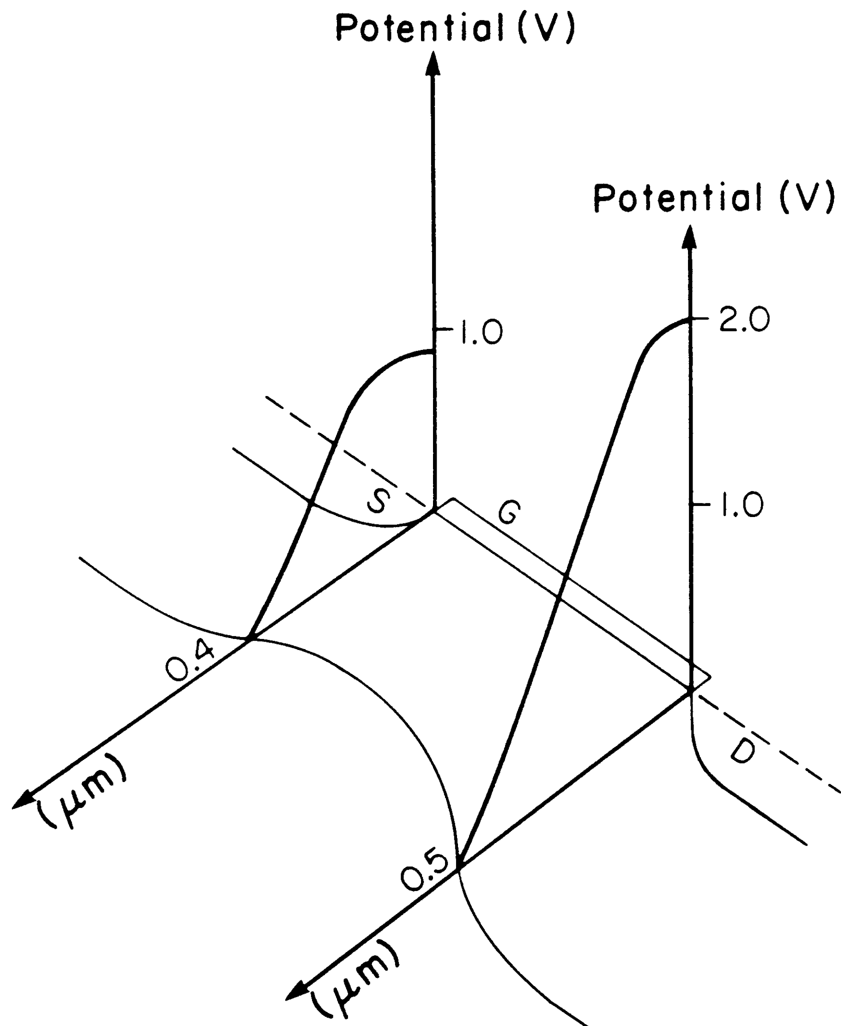


Fig. 2-5 An example of calculated potential distributions along the two lines in the substrate. The calculation incorporated V_G's role as a part of boundary condition. The n-channel device with channel length L = 1.4 μm was biased at $V_G = 2.0$ V and $V_D = 1.2$ V.

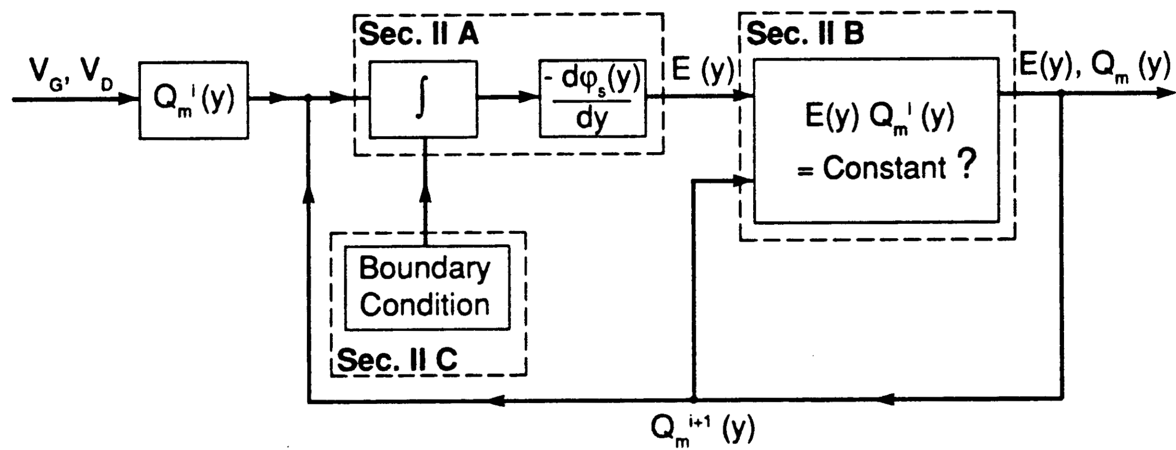


Fig. 2-6 A flow chart of the self-consistent feedback scheme.

depletion edge. These potential profiles constitute the boundaries of Fig. 2-2.

In order to give a clear picture of the analysis, a flow chart of this feedback scheme is plotted in Fig. 2-6. The main chain in this scheme is the complementary calculations of E(y) and $Q_m(y)$ at the surface, which is a simple and fast convergent process. As an auxiliary part, what we have presented in this subsection is novel, but not unique. In addition, it is not necessary to run this part for every loop, since the surface quantities are insensitive to both the potentials along lines J-K and L-M, and the boundary of the depletion region.

2.3 Results and Discussion

For the flow chart of the feedback scheme plotted in Fig. 2-6, the input is the device bias, i.e, V_G ($> V_T$) and V_D, the output is the associated mobile charge density $Q_m(y)$ and the lateral field E(y) distributions, with y representing the channel position (in the coordinates of Fig. 2-2). According to Ohm's law, the output then gives the the drain current under the overthreshold bias,

$$I_{DS}(V_G,V_D) = W\ \mu(y)\ E(y)\ Q_m(y) \qquad 0<y<L \qquad (2\text{-}8)$$

with W denoting the channel width. Since (2-8) is valid at any point along the channel (see (2-3)), one may express I_{DS} in terms of the quantities at the source end as

$$I_{DS}(V_G,V_D) = W\ \mu(0)\ E(0)\ Q_m(0) \qquad (2\text{-}9)$$

where, (i) the carrier density $Q_m(0)$ is independent of V_D; (ii) lateral field E(0)

remains small, compared with that at drain end E(L) in the saturation region.

The I-V characteristics calculated for an n-channel device is shown in Fig. 2-7. The device is of $W/L = 20/0.7$ μm, the oxide thickness $T_{ox} = 15$ nm, $N_A = 10^{16}$ cm^{-3}, the mobility $\mu(y) = 680$ $cm^2(Vs)^{-1}$, and the contact diffusion depth $T_j = 0.15$ μm. The corresponding measured I-V data is also shown in the same figure with solid lines. The agreement between the calculation and measurement is satisfactory. Here, the scaling of I_{dsat} with V_G, known as the vertical field effect [5] has been recently shown to be due to Pauli exclusion principle operative in the degenerate channel inversion [13]. The theoretical I-V curve presented in the figure has taken this effect into account.

As shown in Fig. 2-7, for fixed V_G , the calculated I_D tends to saturate as V_D is about to exceed $V_G - V_T$. This saturation behavior is due to the saturation of E(0) with increasing V_D . When a device is biased in the linear region, $Q_m(y)$ distributes itself rather uniformly along the channel, Therefore $|E(0)|$ ($= |d\phi(y)/dy|$, for y=0), commensurates with V_D . With higher V_D , $Q_m(y)$ becomes increasingly uneven, the source end shares less voltage drop. Hence the slope of I_D vs. V_D curve becomes smaller. With further increase in V_D , Q_m near the drain becomes so small that the total increased drain bias ΔV_D drops within a short distance immediately adjacent to the drain. Source end thus shares essentially zero voltage drop, and E(0) remains relatively constant, viz. the current saturates. This E(0) saturation behavior can be exam-

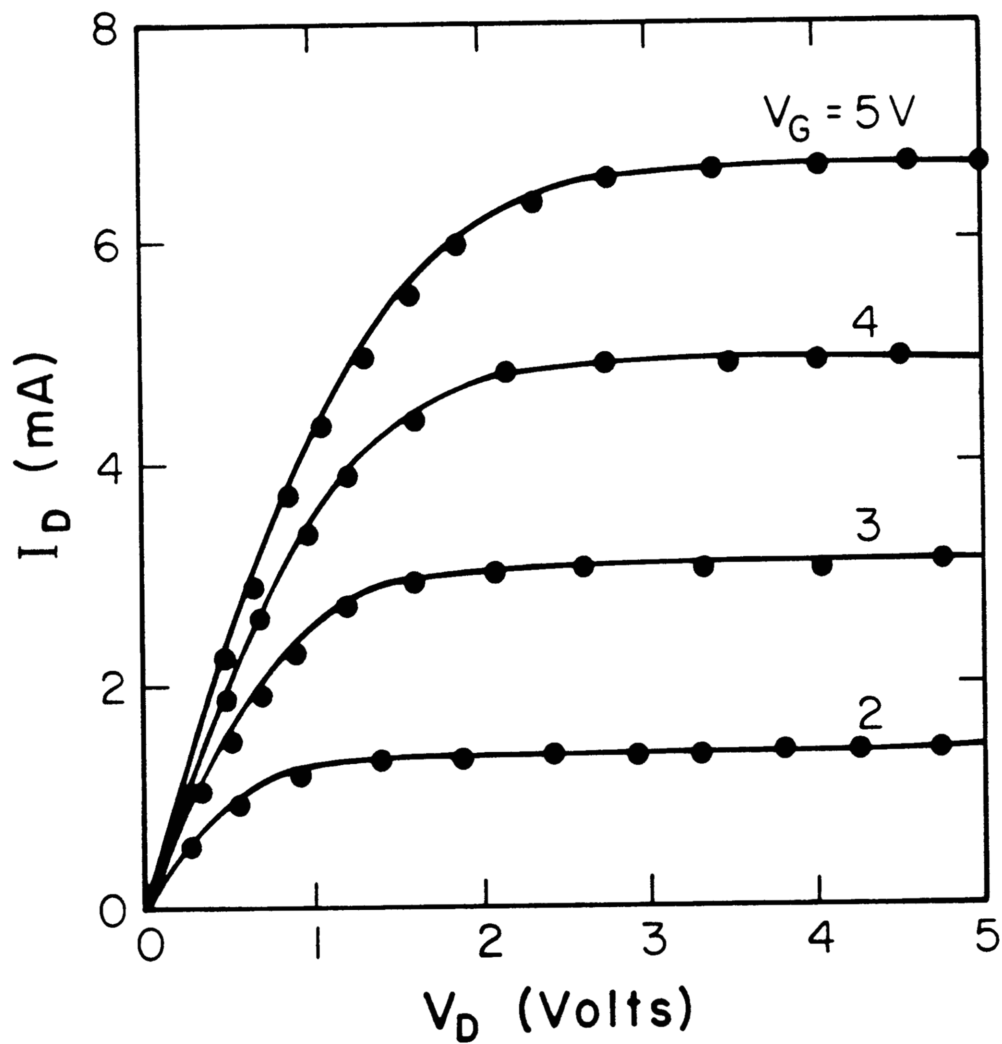
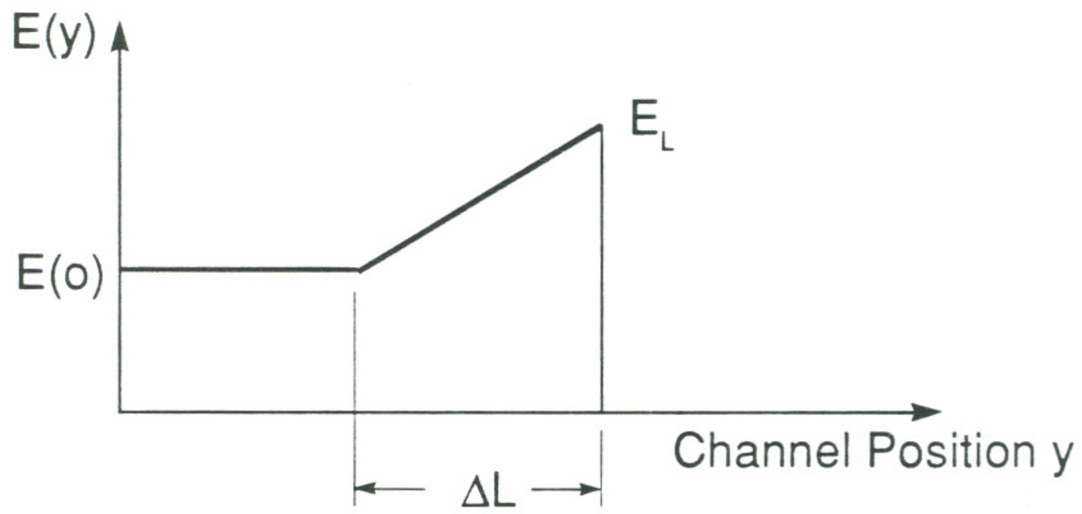


Fig. 2-7 The calculated (dot) and measured (solid line) I-V characteristics for an n-channel device with T_{ox} = 15 nm, W/L = 20/0.7 μm, N_A = 10^{16} cm^{-3}.



$$\Delta L \propto \frac{V_G - V_T}{V_D}$$

Fig. 2-8 A schematic channel field profile in a MOSFET.

Table I. E(o), E_L for different L, V_G and V_D

Applied: $V_G - V_T = 2.3$ V, $\gamma = 0.5$			$V_D = 1.0$ V
L (μm)	E(o) (10^4 V/cm)	E_L (10^4 V/cm)	Area (V)
1.4	0.60	0.80	0.99
1.2	0.65	1.00	1.01
1.0	0.80	1.20	1.02
0.8	0.98	1.51	1.02

Applied: $V_G - V_T = 1.3$ V, $\gamma = 0.57$			$V_D = 1.6$ V
L (μm)	E(o) (10^4 V/cm)	E_L (10^4 V/cm)	Area (V)
1.4	0.45	3.48	1.60
1.2	0.50	4.00	1.57
1.0	0.60	4.80	1.57
0.8	0.75	5.76	1.52

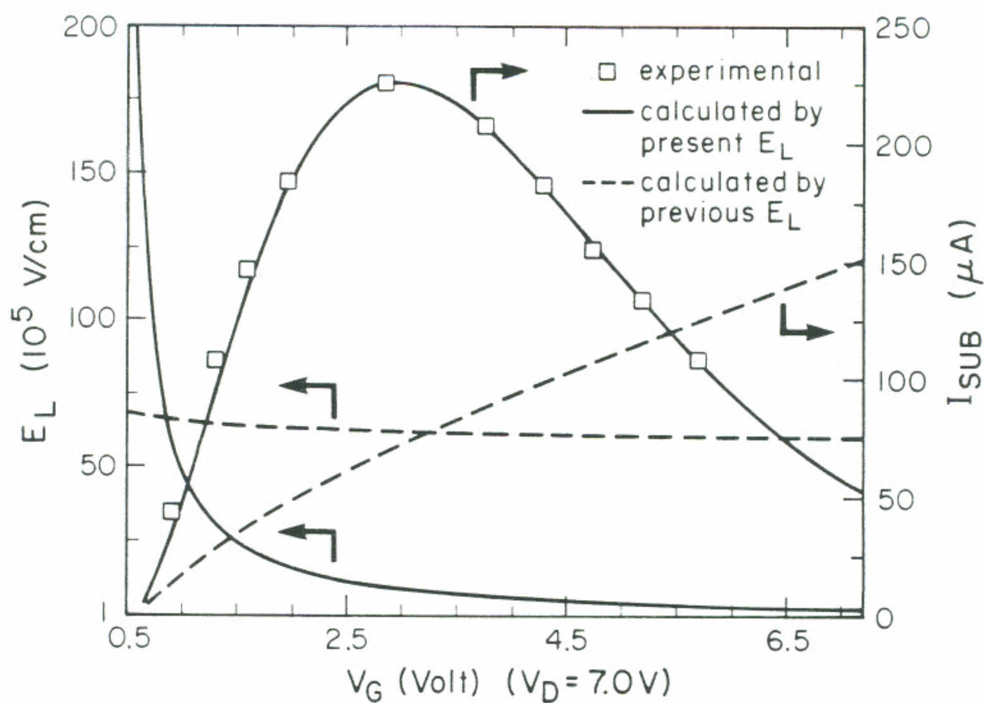


Fig. 2-9 Channel field at drain end E_L with respect to V_G ($< V_D = 7.0$ V) calculated by (2-13) and (2-14) (solid line), and the corresponding E_L and I_{SUB} calculated by the previous model (dash line), and the measured I_{SUB} (open sqare), for an n-channel device with $L = 0.7$ μm, $T_{ox} = 15$ nm, $N_A = 10^{16}$ cm^{-3} .

ined explicitly with the use of the feedback scheme.

It is also shown in Fig. 2-7 that I_D (or E(0)) saturates earlier for a smaller V_G, and the degree of saturation can be described by a factor, $(V_G - V_T) / V_D$. For a smaller V_G, the uniform carrier sheet for $V_D \approx 0$ is thinner ($Q_m(0)$ in (2-9)) than that of a larger V_G; therefore, it will reach an uneven distribution earlier when V_D increases.

We have constructed a schematic channel field profile to simulate this behavior. As shown in Fig. 2-8, V_D equals the area under the profile,

$$V_D = E(0)L + (\Delta L/2)(E_L - E(0)) \qquad (2\text{-}10)$$

where $\Delta L = \alpha L$, and the constant α

$$\alpha = \gamma (V_G - V_T)/V_D \qquad (2\text{-}10a)$$

is proportional to the saturation factor $(V_G - V_T)/V_D$. When a device is biased towards saturation, (larger V_D or smaller V_G), ΔL becomes smaller, meaning that Q_m is drained thinner, and consequently V_D drops more at the drain end. The data of E(0) and E_L listed in Table I, calculated by the feedback scheme for various biases and channel lengths, justifies the profile of Fig. 2-8. As shown in Table 2-I, the applied V_D agrees well with the area obtained from (2-10) for $\gamma \approx 0.5$.

By replacing $Q_m(0)$ with $C_{ox}(V_G - V_T)$, and equaling (2-9), which is valid for the entire overthreshold region, to the conventional saturated drain current expression [3],

$$I_{DSAT} = (W/L)\, \mu_{eff}\, C_{ox}\, (V_G - V_T)^2/2, \tag{2-11}$$

one finds E(0) of saturation region in device bias as,

$$E(0) = \frac{\mu_{eff}}{\mu(0)} \frac{V_G - V_T}{2L} \tag{2-12}$$

Here the effective mobility μ_{eff}, taking into account the drift velocity saturation, is smaller than the mobility at source end $\mu(0)$. As shown in (2-12), E(0) is independent of V_D in the saturation region.

Furthermore, upon substituting (2-12) into (2-10), a simple E_L-model in device saturation region is obtained as

$$E_L = \frac{1}{L} \left(\frac{4V_D^2}{V_G - V_T} - \frac{2V_D}{m} + \frac{V_G - V_T}{2m} \right) \tag{2-13}$$

with $m = \mu(0) / \mu_{eff}$ and $\gamma = 0.5$. Here, E_L is specified explicitly as a function of device biases, i.e., V_G and V_D , and device parameters, i.e., L, and $V_T(V_{FB}, N_A, T_{ox})$ and m. The E_L-curve in the saturation region calculated by (2-13) with the choice of m = 2 is plotted in Fig. 2-9 (solid line). As shown in the figure, E_L is extremely high at $V_G \approx V_T$ region. This is due to the fact that the device saturation is deepest at this region, and the degree of saturation is properly described by the saturation factor used in the profile of Fig. 2-8. Only at this high value of E_L, holes can gain enough energy to be injected into the oxide, and form a small gate current in n-channel device. Note that the potential barrier of holes at the Si/SiO_2 interface is much

higher than that of electrons [5]. The hole gate current in a magnitude of 10^{-15}A were detected and reported by Hofmann *et al.* [14] and Heremans *et al.* [15], in the region $V_G \approx V_T$. As V_G increases, E_L decreases drastically, as shown in Fig. 2-9. This is due to the fact that the degree of saturation is quickly lessened with inceasing Q_m . For comparison, E_L-values calculated from the previous model, $E_L = (V_D - V_{DSAT}(V_G,L))/(x_1,x_2)^{1/2}$ [3], is plotted in the same figure, where x_1 and x_2 are the device parameter related constants. Note that in the E_L-model of [3] and [8], E_L changes weakly with V_G in the saturation region. It neither reaches an extremely high value at $V_G \approx V_T$ region, nor drops quickly afterwards. This is due to the fact that in [8] and [3], the increase of total charge in the drain section, maily depletion charge, is considered to be the primary reason for the increase of E_L.

With the use of E_L-model of (2-13), the substrate current in the saturation region can be evaluated with the well known expression [4],

$$I_{SUB} = C_1 \, I_{DSAT} \exp\left(-\frac{B_1}{E_L}\right) \qquad (2\text{-}14)$$

where C_1 and B_1 are constants. I_{DSAT} can be obtained from either measurement or calculation (see (2-11)). The constants C_1 and B_1 can be determined from two I_{SUB} data points. The theoretical I_{SUB} curve thus obtained is shown in Fig. 2-9. The excellent agreement between theory and data justifies E_L model of (2-13). The E_L curve calculated from the previous model does not decrease fast enough as a function of V_G . Consequently, the corresponding

I_{SUB} curve follows the monotonously increasing I_{DSAT} curve ((2-11)) in this bias region (See Fig. 2-9). The proper characterization of I_{SUB} using (2-13) has paved the way for further modeling of I_G in MOSFETs [16].

It is also shown in (2-13) that E_L is proportional to L^{-1} and V_D^2, instead of just V_D, as predicted in [3] and [8]. The stress induced device degradation is maximum at $V_{G,p}$, where $V_{G,p}$ denotes V_G value at which I_{SUB} (or I_G) reaches peak value $I_{SUB,p}$ (or $I_{G,p}$) for an n- (or p-) channel device [1],[14]. However, devices always break at a $|V_G|$ value which is lower than $|V_{G,p}|$, because of the very high E_L at this bias (see Fig. 2-9). When an acceptable E_L at a low $|V_G|$ is used as the criteria for device breakdown, the square root relationship between power-supply voltages and design rule for submicrometer geometry devices (conventional & LDD structure) can be straightforwardly derived from (2-13),

$$\text{acceptable } V_D \propto (\text{ acceptable } E_L\ )^{1/2} \times L^{1/2} \qquad (2\text{-}15)$$

This relationship of (2-15) has been obtained experimentally and reported by Kakumu *et al.* [17].

2.4 Conclusions

By solving Poisson and current continuity equations concurrently, it is shown that the on-state MOSFET operation is governed by the "draining away" process, not only in the linear region but also in the saturation region. When a MOSFET is biased towards saturation, more free charges are drained

away. This leads to more voltage drop at drain end, and less voltage drop at source end. The former is responsible for the high channel field at the drain end, and the latter is responsible for the saturation of drain current. The maximum channel field E_L is influenced by V_D, V_G and L all through their impact on mobile-charge sheet distribution along the surface. Because of the mechanism, E_L is proportional to V_D^2, V_G^{-1} and L^{-1}. Therefore E_L changes much more rapidly with respect to these variables than has been predicted in the previous models. These strong functional dependences have been verified by observations in various aspects. The analysis and the models of this work have already proven to be useful in hot-carrier effects [16]. It may find further application in the study of device scaling, LDD structure, and nonvolatile devices.

2.5 Appendix 2-I. Boundary Conditions

For given device bias V_G, V_D and the device geometry, the boundary conditions for the potential ϕ, in the coordinates (s,t) of Fig. 2-4a, can be determined as follows,

(i) on the gate electrode (H-G), $\phi = V_G - V_{FB} = V'_G$, where V_{FB} is the flat-band voltage;

(ii) on the two edges of gate oxide (H-J, G-L), with $0 \leq t \leq T_{ox}$,

$$\phi(t) = V'_G - t\,(V'_G - V_S)/T_{ox} \tag{2-16}$$

at source end, and

$$\phi(t) = V'_G - t\,(V'_G - V_D)/T_{ox} \tag{2-17}$$

at drain end, where $V_S = 0V$ is the bias on the source;

(iii) along the profile of source electrode (J-I), $\phi = V_S$, along the profile of drain electrode (L-F), $\phi = V_D$;

(iv) finally, the 1-D potential distribution of a $p-n^+$ junction can be applied to the boundaries in the substrate (I-A, F-E), with $r < t < t_0$,

$$\phi(t) = \phi_i + V_A - \frac{qN_A t^2}{2\epsilon_{si}} \left[\ln(t/r) - 0.5(1 - (t/r)^2)\right] \tag{2-18}$$

where ϕ_i is the built-in potential of the junctions, $V_A = V_S$ at source end, $V_A = V_D$ at drain end, t_0 is defined as the distance where $\phi(t_0) = 0$ V by (2-18), for $t > t_0$, $\phi(t) \equiv 0$.

2.6 Appendix 2-II. Conformal Transformation

A convenient starting point is the example detailed in [18] (Chapter IV, p.99). The example transforms the z-space ($z = s + it$) shown in Fig. 2-10a into the upper half plane of the z_1-space sketched in Fig. 2-10b :

$$z = \frac{2h}{\pi(1+\lambda)} \left[\tanh^{-1} \left(\frac{z_1 - 1}{z_1 + a} \right)^{1/2} + \lambda \tanh^{-1} \left(\frac{z_1 + 1}{z_1 + a} \right)^{1/2} \right] \qquad (2\text{-}19)$$

with

$$\tanh \left(\frac{\pi r (1+\lambda)}{2h\lambda} \right) = \sin \left(\frac{\pi r (1+\lambda)}{2h} \right) \qquad (2\text{-}20)$$

which determines λ in terms of h and r. Having determined λ,

$$a = \coth^2 \left[\frac{\pi r (1+\lambda)}{2h\lambda} \right] + \cot^2 \left[\frac{\pi r (1+\lambda)}{2h} \right] \qquad (2\text{-}21)$$

Figure 2-10a represents the left half of the MOSFET geometry. Introduce a new transformation,

$$z_2 = z_1 + a \qquad (2\text{-}22)$$

Then, the z_1-space is mapped into z_2-space as shown in Fig. 2-10c. An additional transformation,

$$w^2 = z_2 = z_1 + a \qquad (2\text{-}23)$$

completes the conformal transformation, mapping the whole MOSFET geometry into the upper half plane of the w-space (see Fig. 2-4). By substi-

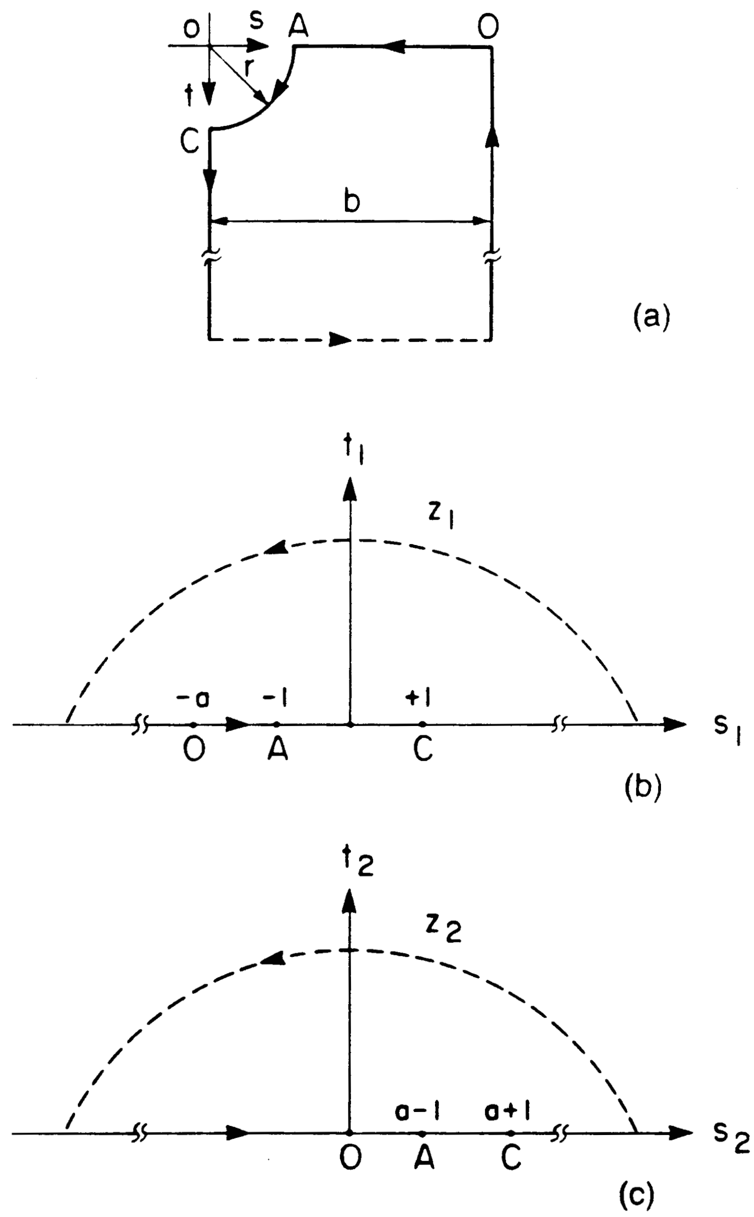


Fig. 2-10 Two successive conformal transformations from the left-half of the device cross section ((a)).

tuting (2-23) into (2-19) one finds (2-5) in Sec. 2.2c. The quantities, d_1 and d_2 appearing in (2-5) are defined as,

$$d_1 = a - 1 \tag{2-24}$$

$$d_2 = a + 1 \tag{2-25}$$

To make the z-w transform explicit, let

$$\left(1-\frac{d_i}{w^2}\right)^{1/2} = R_i\, e^{i\theta_i} \qquad i=1,2 \tag{2-26}$$

Using $w = u + iv$ in (2-26) one can obtain R_i, θ_i in terms of u, v as

$$R_i = \frac{1}{u^2+v^2}\left\{\left[(u^2+v^2)^2-d_i(u^2-v^2)\right]^2+(2d_iuv)^2\right\}^{1/4} \tag{2-27}$$

and

$$\theta_i = \frac{1}{2}\tan^{-1}\frac{2uvd_i}{(u^2+v^2)^2-d_i(u^2-v^2)} \tag{2-28}$$

Upon using the identity

$$\tanh^{-1}(R\, e^{i\theta}) = \frac{1}{2}\ln\left(\frac{1+Re^{i\theta}}{1-Re^{i\theta}}\right) \tag{2-29}$$

and inserting (2-27), (2-28) in (2-5) there results

$$x=\frac{b}{\pi(1+\lambda)}\left[\ln\frac{(1+R_2^{\,4}-2R_2^{\,2}\cos2\theta_2)^{1/2}}{1+R_2^{\,2}-2R_2\cos\theta_2}+\lambda\ln\frac{(1+R_1^{\,4}-2R_1^{\,2}\cos2\theta_1)^{1/2}}{1+R_1^{\,2}-2R_1\cos\theta_1}\right] \tag{2-30}$$

$$y=\frac{b}{\pi(1+\lambda)}\left[\tan^{-1}\left(\frac{2R_2\sin\theta_2}{1-R_2^{\ 2}}\right)+\lambda\tan^{-1}\left(\frac{2R_1\sin\theta_1}{1-R_1^{\ 2}}\right)\right] \qquad (2\text{-}31)$$

For $u > 0$,

$$0 < \tan^{-1}[f(u>0)] < \pi$$

and for $u<0$

$$\tan^{-1}[f(u<0)] = 2\pi - \tan^{-1}[f(u>0)]$$

Here f represents the argument of inverse tangent function.

With the use of (2-30) and (2-31), one can relate x,y into u,v or vice versa.

CHAPTER 3

Two-Region Gate Bias Stress in P-Channel MOSFETs

3.1 Introduction

Hot-carrier induced effects in p-channel MOSFETs have been extensively examined in the literature [19]-[25]. Much of the investigations were understandably focussed on the worst case stress conditions, where $|V_G|$ is small and the gate current is maximum [19]-[21]. The stress induced effects for large gate bias have also been examined [22],[23]. However, the relationship existing between these two cases has not been investigated. The comparison of device degradation in these two regions is needed from the device lifetime point of view.

We examined the degradation behavior of p-channel MOSFET with p^+−poly gate electrode and 15 nm oxide thickness at fixed drain voltage ($|V_D| = 8V$) while varying $|V_G|$ from 0 to $|V_D|$. In this entire range of device saturation, the gate bias was found to divide into two regions in terms of the polarity of gate currents and the associated device degradation behaviors which are distinctly different from each other. The physical mechanisms inherent in these two bias regions are examined, and a model of the gate current is presented.

3.2 Two Regions of Gate Bias

Figure 3-1 presents the substrate (I_{SUB}) and gate (I_G) currents vs $|V_G|$, measured from p-channel device at fixed V_D ($|V_D| = 8V$). As shown in the figure, there are two distinct I_G curves bearing opposite polarity. This divides the gate bias into two regions; region I for $0 \leq |V_G| \leq 4V$; region II for $4V \leq |V_G| \leq 8V$. The appearance of electron and hole gate currents in I and II respectively can be understood as follows.

As well known, the impact ionization induced hot carriers contribute to I_G when injected into the oxide. Which carrier species actually contributes I_G is dictated by the device bias conditions. Figure 3-2 schematically depicts the equipotential and electric field lines for region I and II near the drain end. Two factors influence lateral field induced hot carriers to form the gate current: (i) the redirection field, E_n, i.e., the field in the channel normal to the interface, and (ii) the vertical field in the oxide, E_{ox}. In region I where the device is strongly saturated, E_n is small while E_{ox} is large (See Fig. 3-2). In view of E_{ox} - polarity, hot electrons are pulled into the interface by E_{ox} to form I_G. In region II where the device is weakly saturated, E_{ox} is small while E_n becomes large. Thus, again in view of the polarity of E_n, hot holes are redirected into the interface by E_n. Inasmuch as device degradation is caused by hot carrier injection into the oxide, i.e., I_G, each region will have its own degradation behavior.

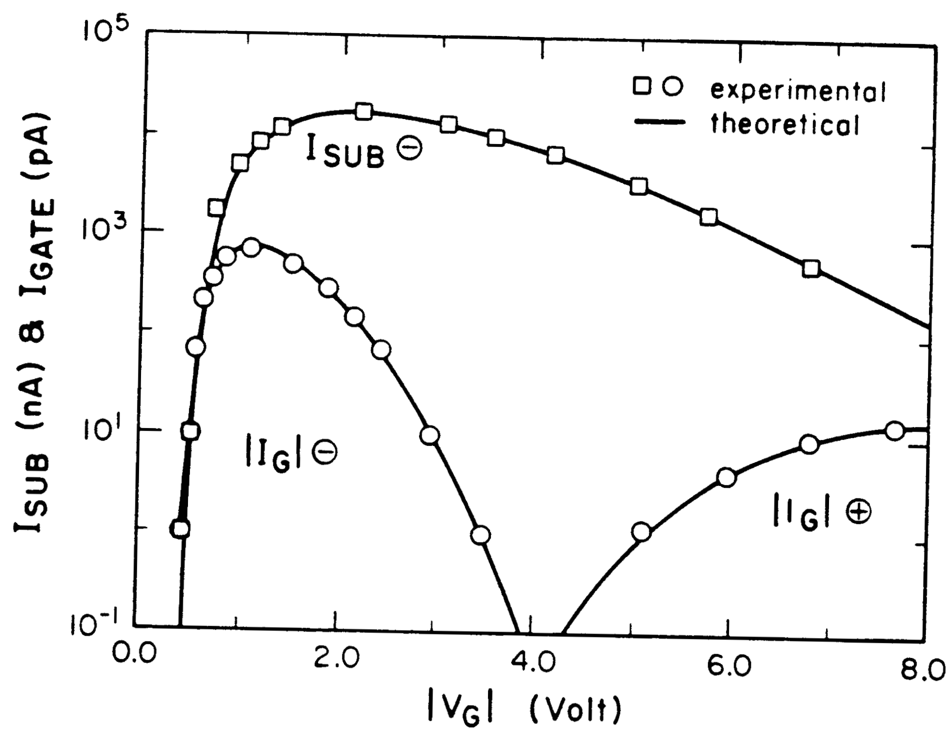


Fig. 3-1 Substrate (I_{SUB}) and gate (I_G) currents vs $|V_G|$, and the theoretical fit, for fixed $|V_D| = 8.0$ V in p-channel device: $W/L_{eff} = 20/0.4$ μm; oxide thickness $T_{ox} = 15$ nm; standard process LDD structure.

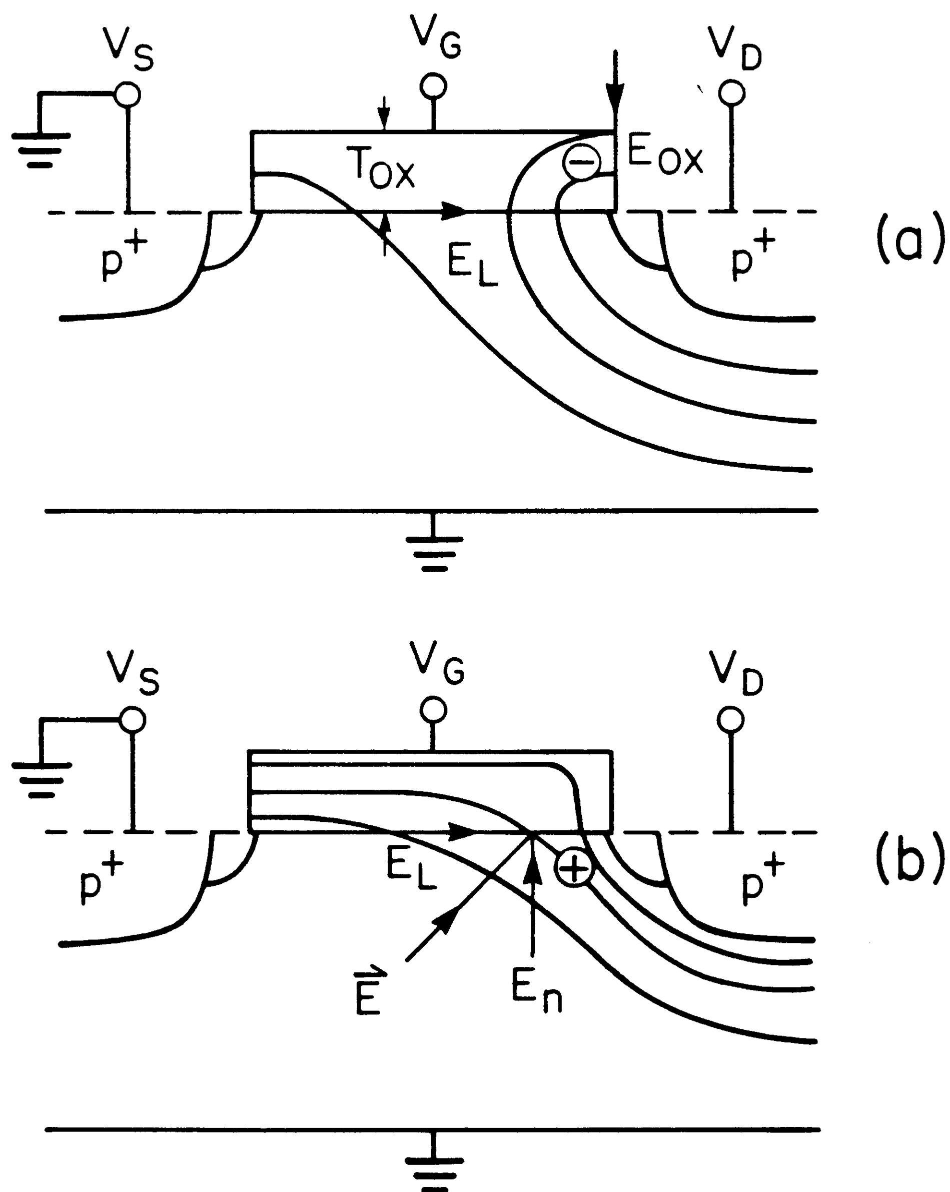


Fig. 3-2 Schematic diagram of the equipotential and electric field lines for (a) region I ($|V_G| << |V_D|$) and (b) region II ($|V_G| \approx |V_D|$) bias conditions.

3.3 Device Degradation Characteristics

Figure 3-3 summarizes the shifts in device parameters, g_m and $|V_T|$ versus V_G for different stress times. The noteworthy features of the data are: (i) The magnitudes of parameter shift for given stress time well reflects that of I_G in both regions, as expected. (ii) The parameter shifts distinctly undergo a **change in sign**, as V_G is swept from one region to another. Specifically, the hot electrons which are injected into the oxide and subsequently trapped therein (in region I) are shown to cause positive shift in g_m, hence negative shift in $|V_T|$. Similarly, hot holes in region II induce the corresponding parameter shift in opposite direction. (iii) With increasing stress time, the boundary between region I and II, as evidenced by the sign of parameter shift changes appreciably. For instance, g_m at $|V_G| = 3.4$ V exhibited positive shift during small stress time. With increasing time, however, g_m shift becomes negative. This indicates that region II was broadened to the left of $|V_G| =$ 3.4 V value. (iv) For a given V_G, the parameter shift in region I saturates as a function of stress time, while that in region II remains cumulative in time (see the $|V_T|$ - shift data).

3.4 Discussion

The polarity and time dependence of the parameter shift are interelated with each other. In region I, trapped electrons produce electric field which reenforces the gate field line near the interface. As a consequence, near the

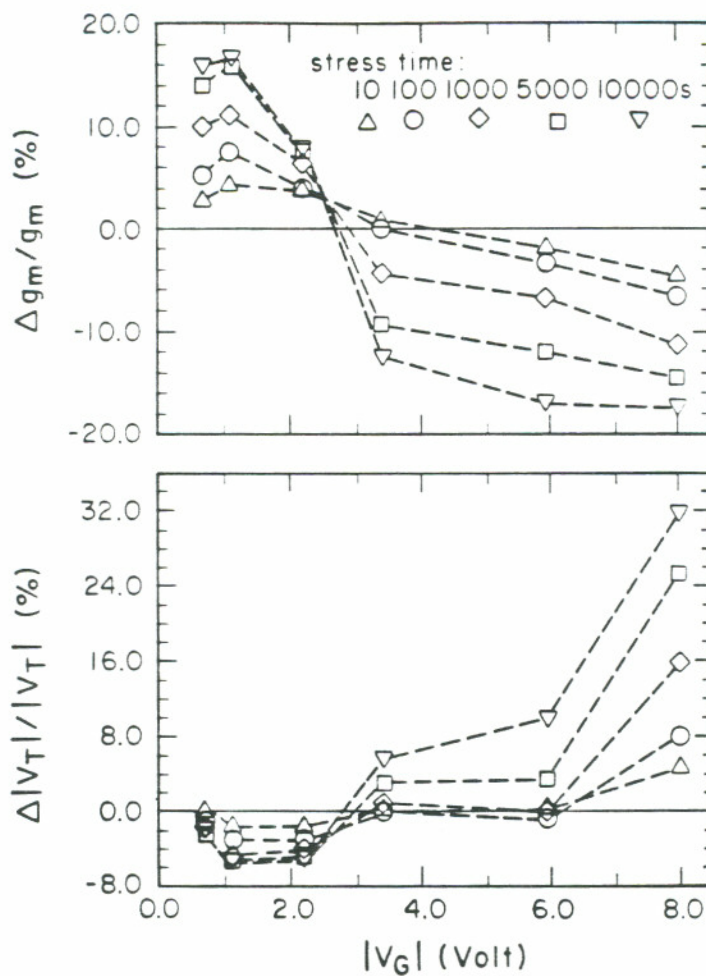


Fig. 3-3 Shifts in g_m and $|V_T|$ versus $|V_G|$ for fixed $|V_D| = 8.0$ V at different stress times. The p-channel devices are of $W/L_{eff} = 20/0.4$ μm; oxide thickness $T_{ox} = 15$ nm; standard process LDD structure.

drain end, band bends deeper, mobile hole density increases and the lateral electric field, E_L decreases. Therefore, I_{DSAT} and g_m should increase and $|V_T|$ should decrease. This reasoning is in agreement with the shortening of effective channel length, i.e., hot-electron-induced punchthrough effect [19].

Furthermore, the decreased lateral electric field alleviates the high field induced degradation effect, resulting in saturated parameter shift. The appreciable change in boundary between region I and II again is consistent with decreased lateral field as a function of stress time. The trapped hole near the drain in region II gives rise to device degradation characteristics **exactly opposite to that of hot-electrons**.

3.5 Simple Model of I_G, I_{SUB} and E_L

The two-region gate stress model is put into mathematical form by fitting I_{SUB} and I_G. As discussed in Ref.[3], substrate current, which strongly depends on the lateral field, can be viewed as a source for the gate currents in both regions. The gate current is further governed by the normal field above the interface, E_{ox}, and below the interface, E_n, in region I and region II, respectively. We first model phenomenologically the lateral channel field at the drain end, E_L. The channel field profile in saturation is sketched in Fig. 3-4. The high field region is denoted by $\Delta L = \alpha L$ with $\alpha \equiv (V_G - V_T)/2V_D$, L being the channel length. For strong saturation, $\alpha << 1$, ΔL shortens, and the pinch-off region broadens (see Fig. 3-4). Thus, $V_D = E(0)L + (E_L - E(0))\Delta L/2$. The saturation current is given in terms of

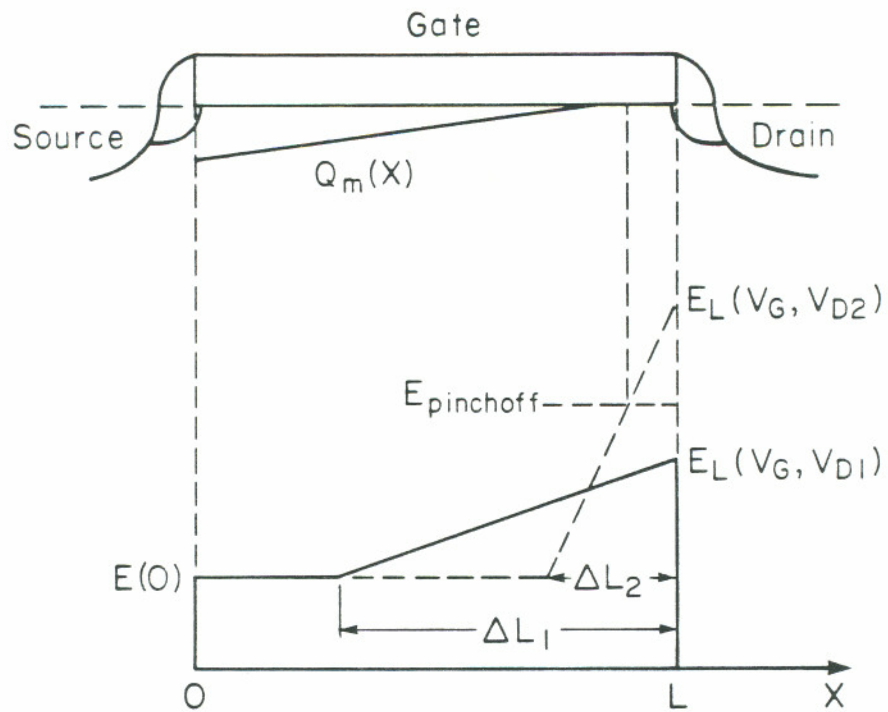


Fig. 3-4 A simple model of lateral channel field profile in device saturation. ($|V_{D2}| > |V_{D1}|$)

channel width, carrier sheet, mobility and field at the source end as $I_{DSAT} = W\, Q_s(0)\, \mu(0)\, E(0)$. Also, from MOSFET model, $I_{DSAT} = (W/L)\, \mu_{eff}\, C_{ox}\, (V_G - V_T)^2/2$, μ_{eff} representing the effective mobility. With $Q_s(0) = C_{ox}\,(V_G - V_T)$, E_L can be expressed as

$$E_L = \frac{1}{L}\left(\frac{4{V_D}^2}{(V_G - V_T)} - \frac{2V_D}{m} + \frac{V_G - V_T}{2m} \right) \tag{3-1}$$

where $m = \mu(0) / \mu_{eff}$, and $m > 1$ due to drift velocity saturation [25].

With the use of (3-1), I_{SUB} can be calculated by the well known expression [4],

$$I_{SUB} = C_1\, I_{DSAT} \exp\left(-\frac{B_1}{E_L}\right) \tag{3-2}$$

Here, the constants C_1 and B_1 can be determined from two data points of I_{SUB} and I_{DSAT}. The theoretical I_{SUB} curve with the choice of $m=2$ is presented in Fig. 3-1 and the agreement with the measured I_{SUB} data is shown to be satisfactory. Next, the gate current which consists of two terms, can be modeled as

$$|I_G| = |I_{SUB}| \left[C_{2I} \exp\left(-\frac{B_{2I}}{E_{ox}}\right) + C_{2II} \exp\left(-\frac{B_{2II}}{E_n}\right) \right] \tag{3-3}$$

Here C_{2j}, B_{2j} are again constants and the subscript j refers to region I and II. The exponential factor incorporates the probability of hot carriers transversing through the oxide. According to the two gate bias region analysis,

$E_{ox} = (V_D - V_G) / tox$, while $E_n = \eta V_G$, η being the proportionality factor. Each term in (3-3) becoming dominant in its respective region can be clearly seen from the dependence of E_{ox} and E_n on V_G. The theoretical I_G curve obtained from (3-3) is again shown to agree satisfactorily with the data. (See Fig. 3-1)

3.6 Conclusions

The gate bias is shown to divides into two regions, I and II, according to the distinctly different behavior of gate currents and the associated degradation characteristics. For short stress times more serious device degradation results in region I than that in region II. However, in long time limit the parameter shift in region II also becomes substantial and may be worse than that of region I. The similarities and differences between n- and p-channel MOSFET degradation behavior will be extensively discussed elsewhere.

CHAPTER 4

Majority vs. Minority Hot-Carrier Injection in MOSFETs

4.1 Introduction

The hot-carrier effects in MOSFETs have been extensively studied. The pioneering works [3],[26]-[28] in this area initially focused on the n-channel MOSFET and analyzed the device degradation induced by hot electrons, in correlation with the observed substrate current and electron gate current. Several papers subsequently pointed out that hot holes could also induce a significant degradation in n-channel devices [22],[29],[30]. A gate current made up of hot holes was found near $V_G \approx V_T$ and its effect on the device degradation was examined [14],[15]. Furthermore, a comprehensive analysis of the n-channel MOSFET, including a 2-dimensional simulation with the use of MINIMOS 2 program indicated that the gate current is contributed by either electrons or holes, depending on the gate bias conditions used [14]. Nevertheless, the existence of hole gate current did not draw much attention, mainly because the detected current level was too small ($\approx$ femto-Amperers). To date, the effect of holes in device damage has remained a subject of controversy.

The role of hot electrons was also emphasized in p-channel devices. The conventional approach has been to view the electron gate current and the associated degradation in p-channel devices in a manner identical to the case of n-channel devices [20],[25]. In fact, a model of electron gate current,

developed for n-channel devices was extended nearly verbatim to the case of p-channel devices [25]. However, several papers [22],[19],[23],[31] have discussed the p-channel device degradation resulting specifically from hole injection in high $|V_G|$ region from a different viewpoint. It therefore remains to be further elucidated whether or not the electron gate currents observed both in n- and p-channel devices are to be viewed in an identical context.

In this chapter, the hot carrier injection in both n- and p-channel devices are analyzed from a unified point of view. This unified approach is based on the two-region gate bias, which was briefly reported earlier [32]. In our model, the device saturation naturally divides into two regions, namely high and low $|V_G|$ regimes. Each region is characterized by its own inherent electric field distribution. Accordingly, two gate currents and two types of device degradation behavior are shown to be associated in these bias regions both in n- and p-channel MOSFETs. This two-region gate bias model puts the prevailing controversies regarding the role of holes into a proper perspective. In the present analysis, it is the hole gate current in p-channel devices that is viewed as counterpart of electron gate current in n-channel devices.

In Sec. 4.2, the experimental results measured from p- and n-channel devices are presented. The concept of majority vs. minority hot carrier injection is introduced. In Sec. 4.3, with the concept, the observed current and degradation data are qualitatively explained. In Sec. 4.4, the analysis is put into a simple and closed mathematical form. Here, the lateral channel field at the drain end, a key quantity for hot carrier effects, is phenomenologically

modeled. In Sec. 4.5, a few concluding remarks are made.

4.2 Experimental Results

The identical p- and identical n-channel devices used in the experiments are of channel width to effective channel length ratio $W/L = 20/0.4\ \mu m$; oxide thickness $T_{ox} = 15$ nm; p^+- poly gate for p-channel device; n^+- poly gate for n-channel device; standard LDD structure.

Figure 4-1 presents the substrate (I_{SUB}) and gate (I_G) currents, measured from the p-channel MOSFET over the entire range of device saturation, viz, $0 \leq |V_G| \leq |V_D|$. Note that I_{SUB} consists of hot electrons, which have the opposite polarity from the carriers induced under gate bias (holes). In contrast to I_{SUB}, there are two distinct gate currents bearing mutually opposite polarity. These gate currents divide the device saturation into two regions.

We define the low $|V_G|$ range ($0V \leq |V_G| \leq |V_D| / 2$) as region I and the high $|V_G|$ range ($|V_D| / 2 \leq |V_G| \leq |V_D|$) as region II. The carriers induced by the gate bias in the channel are called in this dissertation as "majority carriers". Those carriers bearing the opposite polarity from the majority carriers are called as "minority carriers". This classification makes it possible to bring out the physics of hot carrier injection independent of channel type. According to this classification, as Fig. 4-1 shows, the gate current in **region I** consists of **minority** carriers, while that in **region II** is contributed by **majority** carriers.

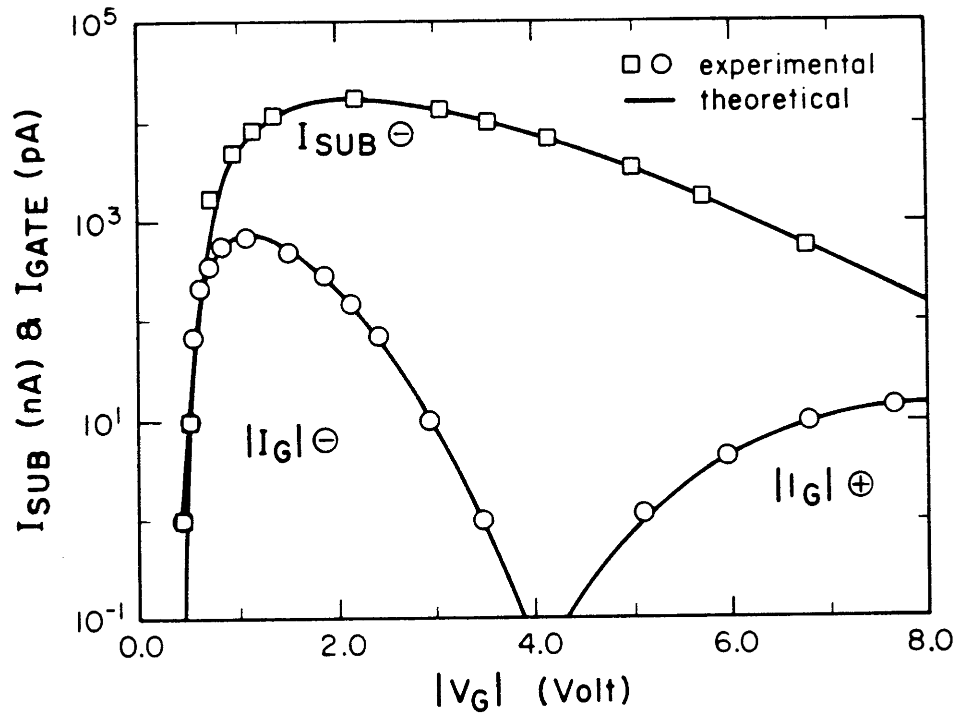


Fig. 4-1 P-channel substrate (I_{SUB}) and gate (I_G) currents versus magnitude of gate voltage $|V_G|$, and the theoretical fit, for fixed drain voltage $|V_D| =$ 8.0 V.

Figure 4-2 presents the substrate and gate currents, measured from n-channel MOSFET at fixed V_D (7V), again over the whole range of device saturation ($0V \leq V_G \leq V_D$). Compared with Fig. 4-1, one can notice a few symmetric features : (i) I_{SUB} is made up of minority carriers (holes) and is generally of the same shape as that in Fig. 4-1. The substrate current always consists of minority carriers, since they are pushed out into the substrate by the voltage difference between drain terminal and substrate; (ii) In region II, I_G again consists of majority carriers (electron), similar in both shape and magnitude with its counterpart in p-channel device. However, there is no appreciable gate current in region I. This absence of gate current constitutes a striking difference between n- and p-channel cases.

Figure 4-3 presents parameter shifts, in g_m, I_{DSAT} and $|V_T|$, measured from the identical p-channel devices as a function of V_G for different stress times. By comparison with Fig. 4-1, it is seen that the device degradation is directly influenced by the the gate current, as evidenced by the following observations: (i) The magnitude of parameter shift for given time is commensurate with the magnitude of I_G-level; (ii) The parameter shifts distinctly undergo the change in sign, as V_G is changed from one region to another. The gate current made up of minority carriers (electron) in region I suggests that minority carriers, once injected into the interface and oxide, induce positive g_m and I_{DSAT} shift and negative $|V_T|$ shift. Similarly, the majority carrier (hole) injection into the interface in region II is shown to results in parameter shifts in the opposite direction; (iii) The effect of majority versus

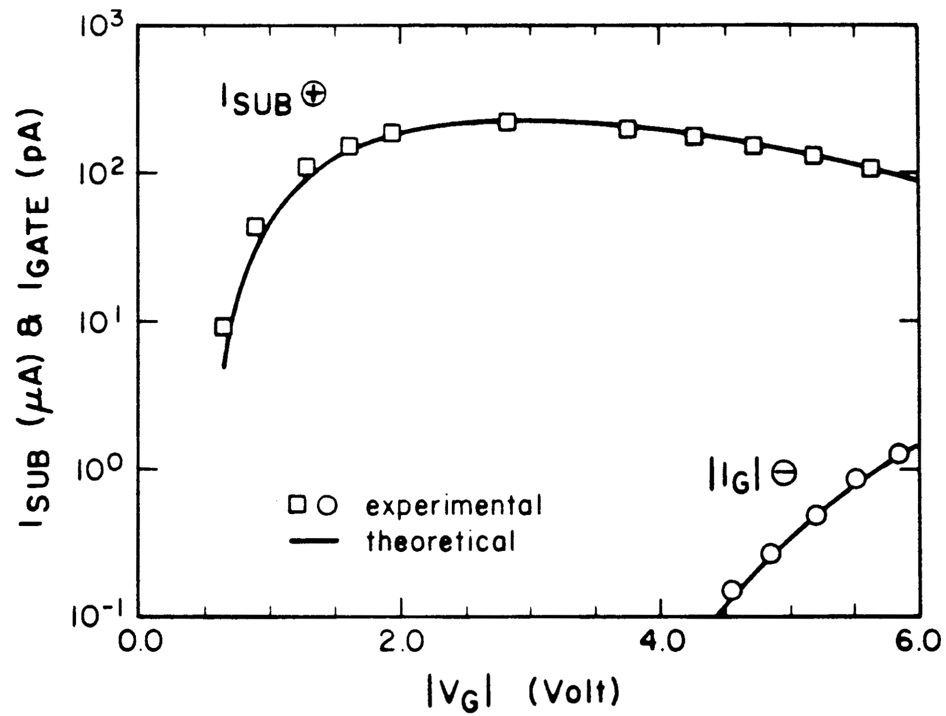


Fig. 4-2 N-channel substrate (I_{SUB}) and gate current (I_G) versus gate voltage V_G , and the theoretical fit, for fixed drain voltage $V_D = 7.0$ V.

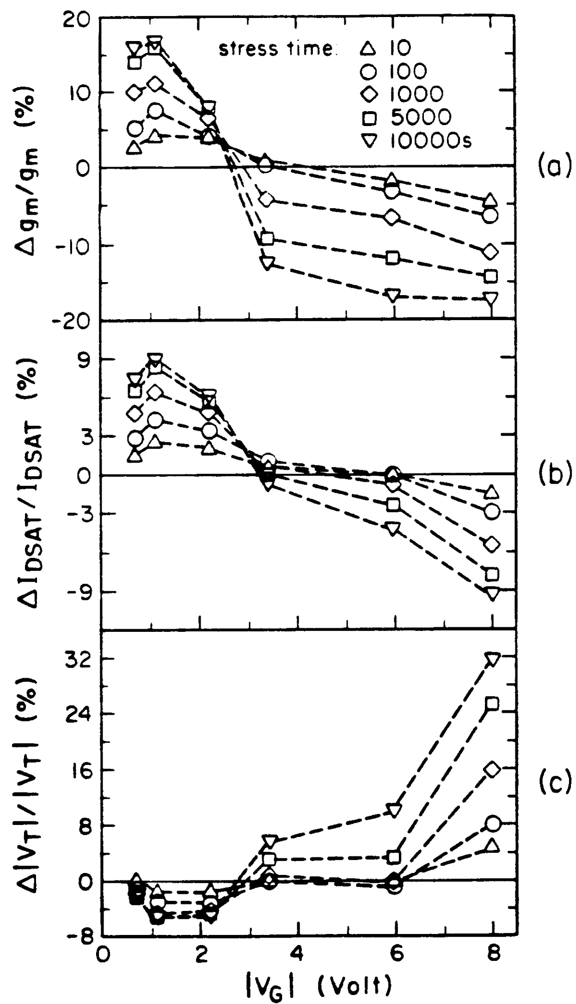


Fig. 4-3 P-channel parameter shifts in (a) transconductance, g_m; (b) saturated drain current, I_{DSAT}; and (c) magnitude of threshold voltage, $|V_T|$ versus magnitude of gate voltage $|V_G|$ for fixed drain voltage $|V_D| = 8.0$ V at different stress times.

minority carrier injection being drastically different is further evidenced by the clear change in time of the boundary between region I and II. For instance, g_m at $|V_G| = 3.4$ V exhibits positive shift for small stress time. With increasing time, however, g_m shift becomes negative, indicating the broadening of region II; (iv) For given V_G, the parameter shift in region I saturates in time, while that in region II is cumulative in time (See $|V_T|$-shift data). Since majority vs. minority type trapping induces the opposite effects, the device degradation can be also classified into majority versus minority type.

Figure 4-4 presents the shift in g_m, and I_{DSAT} , measured from the identical n-channel devices as a function of V_G for different stress times. The V_T shifts have not been presented here, because they are not substantial compared with other shifts. Similar to the case of p-channel device, the g_m and I_{DSAT} shift negatively in region II, indicating that the degradation is of majority type. However, the degradation is also of majority type in region I. This is another difference between n- and p-channel cases.

4.3 Physics of Two-Region Behavior

The two-region behavior of gate currents and corresponding degradation presented in Sec. 4.2 can be understood by analyzing the electric field distributions under different gate biases.

Three factors primarily determine the gate current; (i) E_L, the surface lateral field near the drain, generating electron-hole pairs via impact

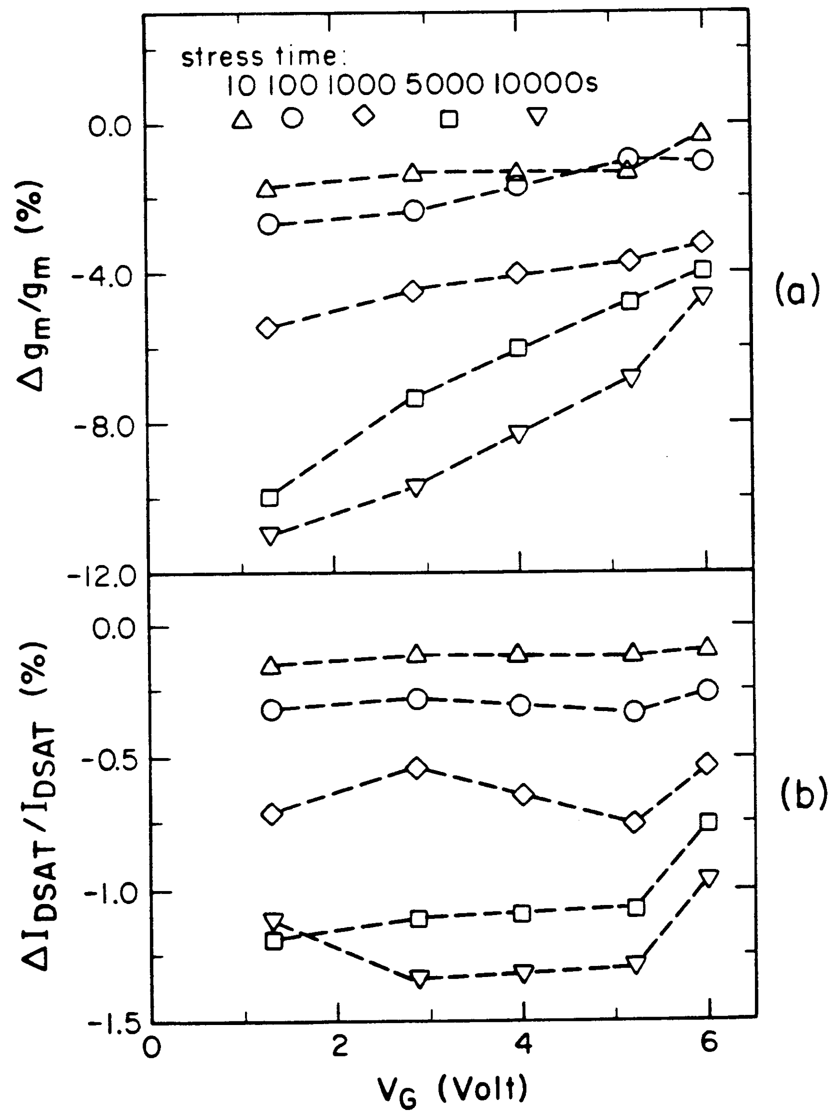


Fig. 4-4 N-channel parameter shifts in (a) transconductance, g_m; and (b) saturated drain current, I_{DSAT} versus gate voltage V_G for fixed drain voltage $V_D = 7.0$ V.

ionization and providing sufficient kinetic energy for carriers to overcome the potential barrier at the interface, (ii) E_n, the normal field near the drain below the interface, redirecting the hot carriers' movement toward the interface and (iii) E_{ox}, the normal field near the drain in the oxide, pulling the injected hot carriers to the gate electrode.

In Fig. 4-5, the equipotential lines in the cross-section of a p-channel device are schematically drawn for both region I (4-5a) and region II (4-5b). The same figure can be applied to n-channel devices with proper changes in bias polarity. The strength of a field can be determined according to whether the field is perpendicular or parallel to the potential contour.

In bias region I, where the device is strongly saturated, E_L is strong, as expected. The transverse component below the interface E_n is weak. However, the transverse component above the interface E_{ox} is strong and is of the polarity for pulling hot minority carriers to the gate electrode.

In bias region II, the device is weakly saturated, and E_L is weaker than that of region I, nevertheless, E_L is still capable of producing hot carriers, as evidenced by I_{SUB} in region II. It is also seen that, in this bias region, E_{ox}, the vertical component above the interface, becomes insignificant and E_n, the vertical component below the interface becomes signigicant. Furthermore, E_n is in a direction of redirecting majority type carriers into the interface.

Since a weak field has no influence on either type of hot carrier, the gate current in each region is contributed by the hot carrier whose type can benefit

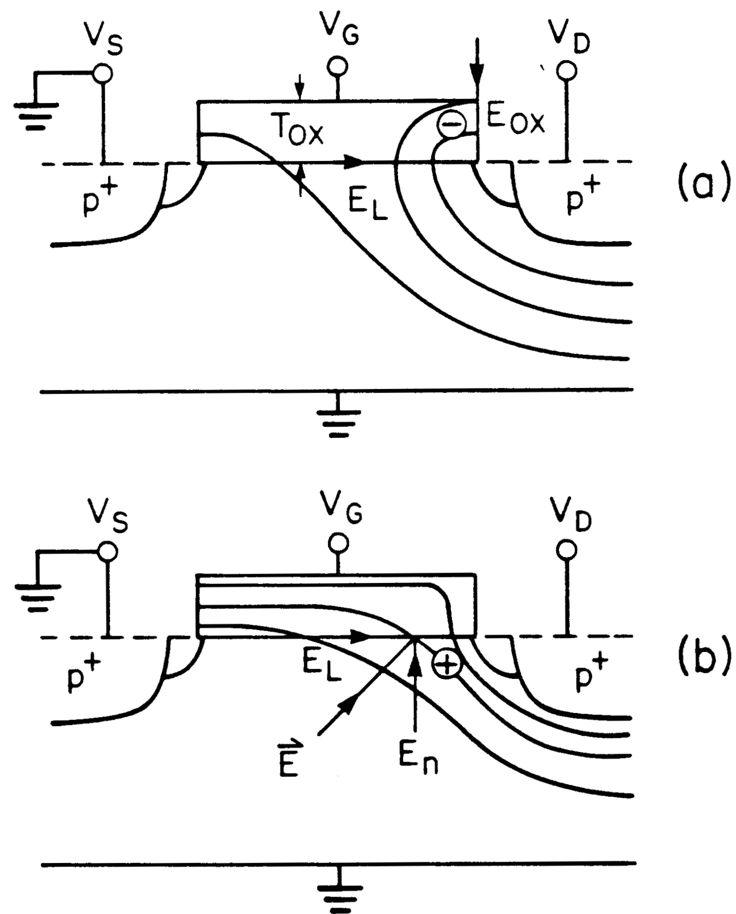


Fig. 4-5 Schematic diagram of equipotential and electric field lines in p-channel device for (a) region I ($|V_G| << |V_D|$); and (b) region II ($|V_G| \approx |V_D|$) bias conditions.

from the strong field. The above electrostatic consideration thus explains, (i) the substrate current made up of minority carriers in both regions, (ii) the majority type gate current and degradation in region II for both p- and n-channel devices, (iii) the minority type gate current and degradation in region I for p-channel device. The absence of minority type gate current and the presence of the majority type degradation in an n-channel device in region I, can be explained with the help of Fig. 4-6.

The typical band diagram for bias region I of a n-channel device is plotted in Fig. 4-6. As shown in this figure, the interface potential barrier for holes (4.8 eV) is much larger than that of electrons (3.1 eV). Since the weak redirection field plays no role in this bias region, smaller potential barrier renders injection of hot electron into the oxide much more likely than that of holes. However, as majority carriers, the injected electrons are prevented from reaching the gate by the strong field present in the oxide and therefore trapped in the oxide close to the Si/SiO_2 interface. This accounts for both the absence of gate current and the presence of majority type degradation in this region.

In contrast, the minority carriers (holes) have an extremely low probability to overcome the interface barrier. However, once these carriers get into the oxide, they can be easily pulled into the gate electrode. This does happen at $V_G \approx V_T$ region, where E_L is extremely high. The small hole current thus formed were observed and reported by Hofmann *et al.* [14] and Heremans *et al.*[15].

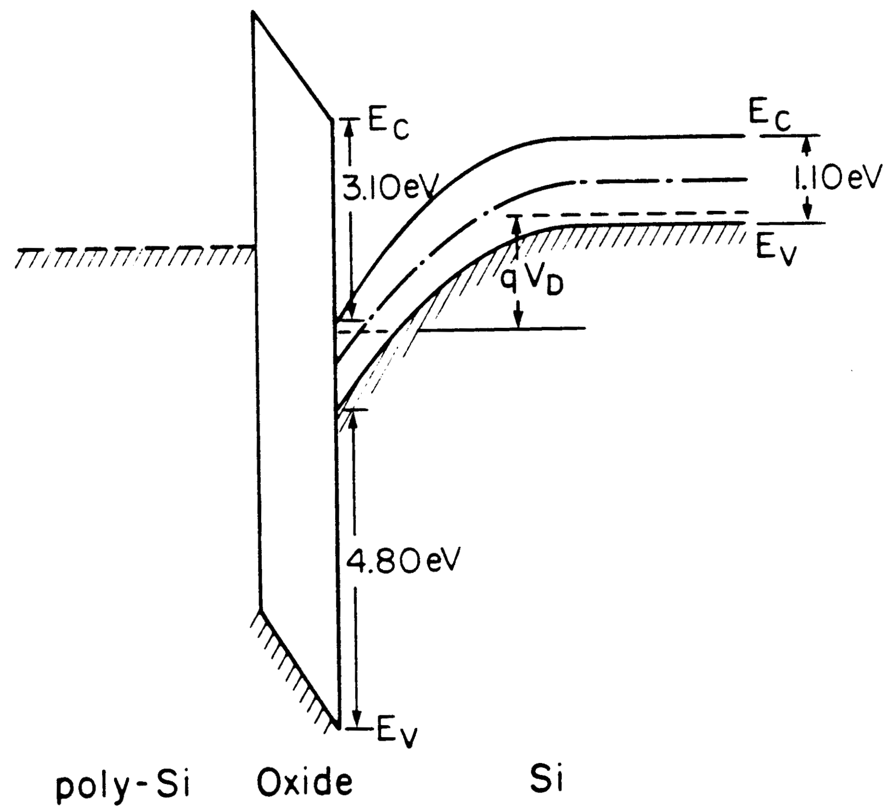


Fig. 4-6 Energy-band diagram at drain end of a n-channel device biased in region I ($V_G << V_D$).

The polarity of parameter shift and other features of degradation versus trapped carrier type can also be explained from a unified point of view. When the trapping is of minority type, the trapped carriers can, in turn, help gate bias to induce more majority carriers near the drain ("HEIP" effect, [19]). Therefore, $|V_T|$ shifts negatively (See Fig. 4-3, region I). The decreasing magnitude of V_T resulting from stress is directly responsible for the broadening of region II with increasing stress time, for given V_G (Fig. 4-3). With more majority carriers near the drain end, the conductance therein is increased and lateral high field is alleviated. These effects lead to positive g_m and I_{DSAT} shifts and also the saturation in time of the degradation (Fig. 4-3, region I).

The effect of the majority type trapping is exactly opposite to that of minority type trapping. It results in negative g_m shift and unsaturated behavior of degradation vs stress time. (See region II in Fig. 4-3 and both regions in Fig. 4-4).

4.4 Model of Two-Region Bias Behavior

In this section, the electric field analysis (Fig. 4-5) considered in Sec. 4.3 is put into a mathematical form. Additionally, a simple model for the substrate current and gate currents in both regions is given.

The lateral electric field E_L at the drain end has been extensively discussed in Sec. 2.3. E_L is given by,

$$E_L = \frac{1}{L}\left[\frac{4V_D^2}{V_G - V_T} - \frac{2V_D}{m} + \frac{V_G - V_T}{2m}\right] \qquad (4\text{-}1)$$

With the closed-form E_L model, the substrate current can be calculated from the well known expression [4],

$$I_{SUB} = C_1\, I_{DSAT} \exp\left(-\frac{B_1}{E_L}\right) \qquad (4\text{-}2)$$

The constants C_1 and B_1 can be determined from two data points of I_{SUB} and I_{DSAT}. The theoretical I_{SUB} - curve obtained with the choice of $m = 2$ for both n- and p-channel devices are presented in Figs. 4-1 and 4-3. The agreement is shown to be satisfactory. A properly modeled substrate current as a function of applied voltages and device parameters paves way for analyzing gate currents.

According to the two-region gate bias model, the two vertical fields above and below the interface are given as $E_{ox} = (V_D - V_G)/T_{ox}$, and $E_n = \eta\, V_G$. Here T_{ox} is oxide thickness and η the proportionality constant.

It is seen from this expression that E_{ox} and E_n as functions of V_G become dominant in region I and II, respectively. With the substrate current used as the source, the gate current can be expressed as

$$|I_G| = |I_{SUB}| \left[C_{2I}\exp\left(-\frac{B_{2I}}{E_{ox}}\right) + C_{2II}\exp\left(-\frac{B_{2II}}{E_n}\right) \right] \tag{4-3}$$

The explicit dependence of E_{ox} and E_n on gate bias renders each term in (4-3) dominant in its respective region. The constants C_{2j}, B_{2j} (with j denoting I and II) can be determined from two data points of I_{SUB} and I_G. The I_G-curves calculated from (4-3) are shown in Figs. 4-1 and 4-3. The agreement between theory and data is again seen to be satisfactory.

4.5 Conclusion

This chapter has analyzed hot-carrier injection in MOSFETs base on , (i) the two region gate bias model; (ii) the majority vs. minority hot carrier injection concept; (iii) distinct roles of vertical field below and above the Si/SiO_2 interface.

The bias region I is characterized by strong lateral field, E_L, strong normal field above the interface, (E_{ox}) and weak normal field below the interface, (E_n). In this region, for p-channel devices, and in most part of this region, for n-channel devices, it is the electron that can overcome the potential barrier and get into the oxide. As the minority carriers in p-channel device, the electrons are further pulled towards the gate to form a large gate

current, normally observed in this region, and degradation is of the minority type. As the majority carriers in n-channel device, the electrons are opposed from reaching the gate but the degradation is of majority type. At $V_G \approx V_T$ region, E_L is extremely strong. Holes, the minority type carriers of n-channel devices, have a chance to get into the oxide, forming a very small gate current, and causing minority type degradation.

The bias region II is characterized by E_L strong but weaker than the case of region I, weak E_{ox} and strong E_n. Since E_n always redirects the majority carriers into the interface, both degradation and I_G are of the majority type for both p- and n-channel devices. The gate current in p-channel device is seldom observed, since the hole is the majority carrier for p-channel device.

In n-channel device, degradation is of majority type in the entire bias region and the degradation should therefore correlate with the substrate current. In p-channel device, the type of degradation does change from region to region, and the degradation should correlate with gate currents.

The two region bias analysis leads to the general gate current expression, which accounts for the opposite polarity in region I and II, as observed. The two region bias model may also prove useful for predicting device lifetime and for examining AC stress effects, where the gate pulsing spans over the entire device saturation.

CHAPTER 5

MOSFETs Lifetime Prediction

5.1 Introduction

The strong correlation existing between substrate current I_{SUB} and hot-carrier induced degradation of n-channel MOSFETs has long been recognized, and utilized for specifying the device lifetime, τ [3];

$$\frac{\tau\, I_D}{W} = C \left(\frac{I_{SUB}}{I_D} \right)^{-1} \tag{5-1}$$

where τ is defined as the stress time necessary to cause, say 10% parameter shifts; I_D the drain current; W the channel width; C and m the fitting constants. Equation (5-1) shows that τ for devices of same process under all bias conditions and channel lengths, can be determined from the measured currents, I_D, I_{SUB} once C and l are determined. As pointed out [33],[34], however, (5-1) is not capable of incorporating the effect of varying drain bias V_D or channel length L. For any given V_D or L, C in (5-1) needs to be redefined from stress experiments to fit the data. Such limitation of (5-1) is also associated with the similar model of p-channel devices [25], for which gate current I_G is the predictor of device degradation.

Naturally, the degradation dependence on L or V_D is one of the main concerns in device reliability. It is therefore necessary to quantify this dependence. In this paper, we present an alternative empirical model, addressing

this basic issue. Once a few fitting parameters are determined from the stress data in a given process run, the model can predict τ as a function of V_D and L in both n- and p-channel devices.

The devices used in this paper are of oxide thickness $T_{ox} = 15\ \mu m$, W $= 20\ \mu m$, n^+-poly gate for n-channel, p^+-poly gate for p-channel devices, and standard LDD structure. Channel length ranges from 0.4 μm to 1.1 μm.

5.2 The Phenomenology of the Model

It is the strong channel field at drain end, E_L that triggers both impact-ionization and the hot-carrier injection into the oxide, hence the degradation in a MOSFET. In the saturation region, we proposed a model of E_L in the form [32],

$$E_L = \frac{1}{L}\left(\frac{4V_D^2}{V_G - V_T} - \frac{2V_D}{m} + \frac{V_G - V_T}{2m}\right) \qquad (5\text{-}2)$$

Here, the constant, m ($1 < m < 2$) adjusts the effective carrier mobility in the channel arising from its longitudinal field dependence. Equation (5-2) simulates the physics underlying the rapid growth of E_L beyond the channel pinch-off, resulting from the current continuity condition in a 2-D electrostatic environment. Specific comparison of (5-2) with other models [3] derived from the two section analysis [8] will be presented elsewhere. It is sufficient to point out here, however, that this E_L-model can correctly quantify the measured I_{SUB} and I_G as a function of V_G , V_D and L [32].

In the saturation region $0 \le |V_G - V_T| \le |V_D|$, for n-channel devices, the hot-electron induced degradation dominates most of the gate bias (excluding $V_G \approx V_T$). Therefore the degradation should correlate with I_{SUB}. In contrast, in p-channel devices, the type of degradation does change from low to high $|V_G|$ region, and therefore, the degradation should correlate with the gate current in each region [32]. In lifetime estimation, it is sufficient to examine τ for the worst case parameter shift, f_{max} (ΔI_{DSAT}, Δg_m) at $V_{G,p}$. Here $V_{G,p}$ denotes the V_G value at which I_{SUB} or I_G reach their respective peak values, $I_{SUB,p}$ or $I_{G,p}$. For convenience, we introduce the variable x to represent either V_D^{-1} at fixed L or L^{-1} at fixed V_D . Since the correlation between I_{SUB} or I_G and degradations exists for any x, the dependence of f_{max} on x can be found via the dependence of $I_{SUB,p}$ or $I_{G,p}$ on x.

An $I_{SUB}-V_G$ curve can be obtained for a given x from (5-2). For each x, $I_{SUB,p}$ can be found. Hence an $I_{SUB,p}$ versus x curve can be obtained from the family of $I_{SUB}-V_G$ curves. Similarly, an $I_{G,p}$ versus x curve can be obtained from a family of I_G-V_G curves for p-channel devices. In Fig. 5-1, the calculated $I_{SUB,p}$ for n-channel, and the electron $I_{G,p}$ for p-channel devices are presented versus x, together with the corresponding data. All the curves in the figures are perfectly or approximately linear in a semilog plot. This indicates that $I_{SUB,p}$, $I_{G,p}$ are exponentially dependent on x, and so are the corresponding degradations, viz. $f_{max} \propto \exp(\beta x)$, β being a constant with respect to x. On the other hand, it has been shown that the degradation

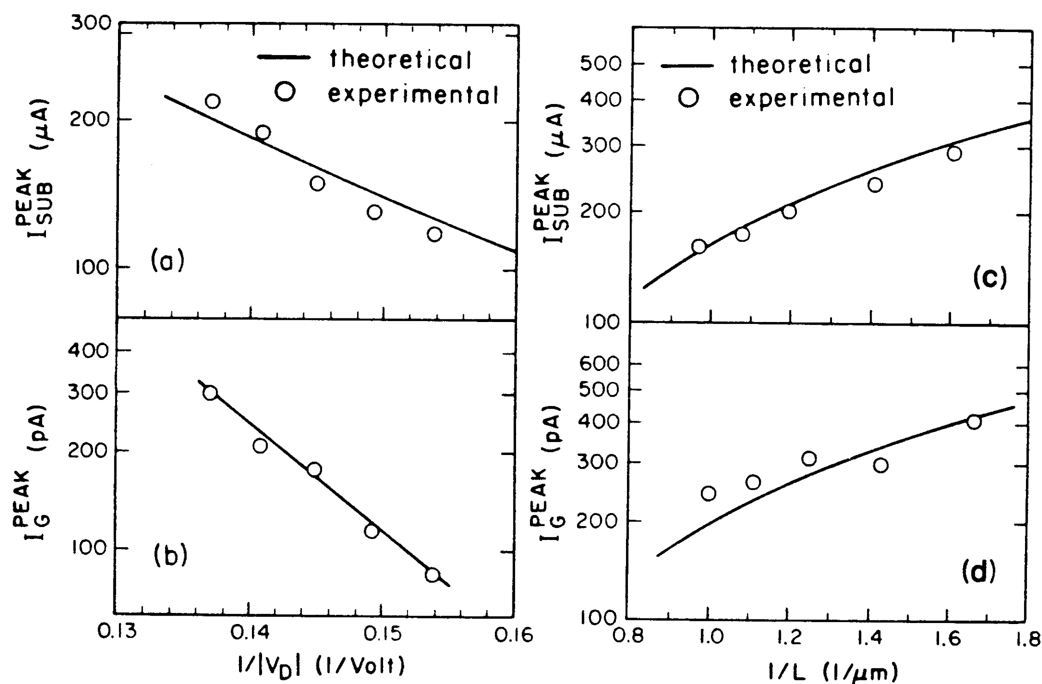


Fig. 5-1 (a) Semilog plot of theoretical (solid lines) and experimental (open circles) peak substrate current $I_{SUB,p}$ in n-channel devices, and (b) peak electron gate current $I_{G,p}$ in p-channel devices, versus V_D^{-1}, the device channel length is L = 0.7 μm; (c) $I_{SUB,p}$ in n-channel devices, and (d) $I_{G,p}$ in p-channel devices, versus L^{-1}, the drain biases were fixed at $|V_D| = 7.3$ V.

obeys power law versus stress time t [3], viz. $f_{max} \propto t^n$, n being a constant with respect to t. Thus, if it is further assumed that β is independent of t, and n is independent of x, one may write,

$$f_{max} = A \exp(\beta x)\, t^n \tag{5-3}$$

where A is a constant.

5.3 Discussion

We stressed n- and p-channel devices to obtain the f_{max}-data for different V_D's at fixed L and also for different L's at fixed V_D. Typical results are shown in Fig. 5-2 and Fig. 5-3.

Fig. 5-2a presents the worst case g_m-shifts measured from n-channel devices (L = 0.7 μm) versus stress time t in a log plot with $x=V_D^{-1}$ used as a parameter. The g_m-data are clearly shown to be aligned with linear curves running parallel with each other. This indicates that f_{max} follows the power law in t, with the power n independent of x (See (5-3)). The same set of data points are plotted Fig. 5-2b vs. x in a semilog scale, with t used as a parameter. Again, the data points follow a set of parallel straight lines, suggesting that β in (5-3) is indeed independent of t.

The assumptions underlying (5-3) are thus confirmed by the stress data. The three constants in (5-3) can therefore be determined from any three data points of different stress conditions, $f_{max}(x_0,t_0)$, $f_{max}(x_0,t_1)$ and $f_{max}(x_1,t_0)$. For the data of Fig. 5-2, the constants were determined to be A=95.87, β=-

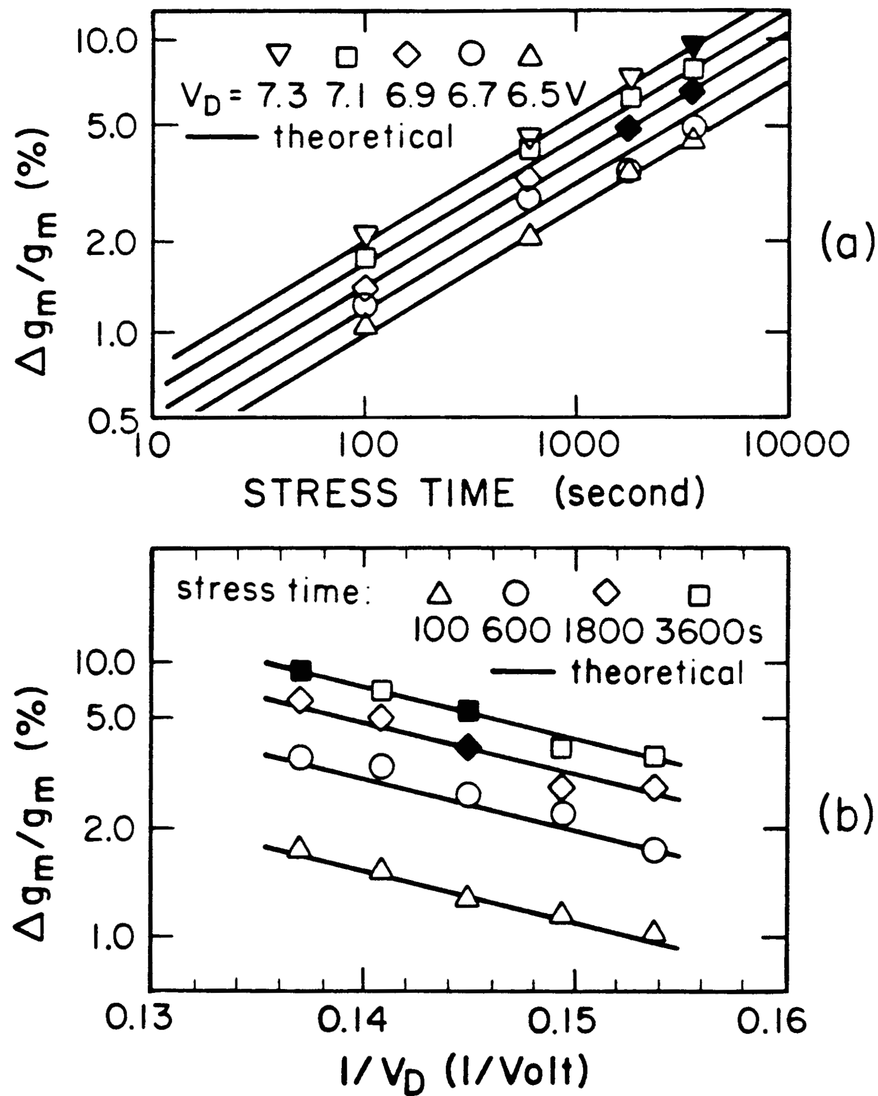


Fig. 5-2 The measured and calculated parameter shifts in g_m stressed at V_G values of $I_{SUB,p}$ in n-channel devices, (a) versus stress time t for different V_D values in a log plot, and (b) versus V_D^{-1} for different t values in a semilog plot. The device channel length is L = 0.7 μm. The three data points shown in solid symbols were used to determine the constants in Eq.(5-3).

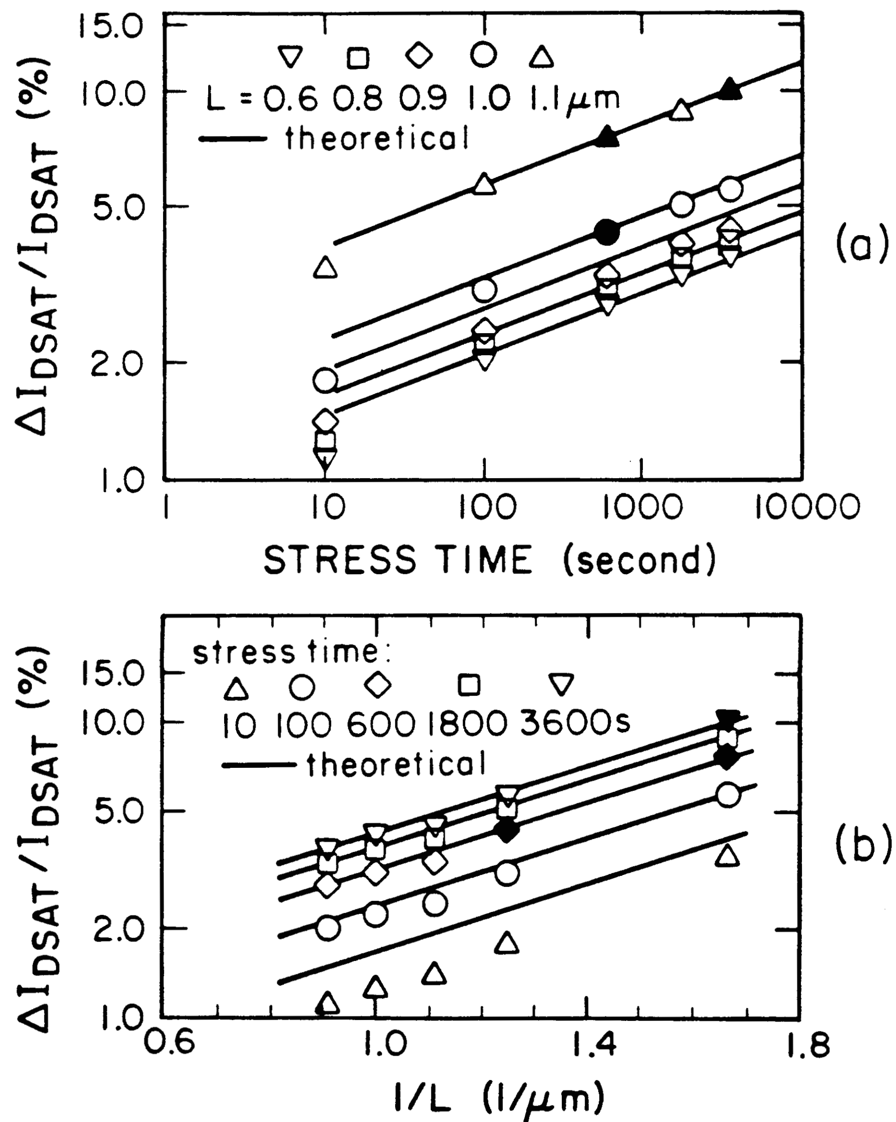


Fig. 5-3 The measured and calculated parameter shifts in I_{DSAT} at V_G values of electron $I_{G,p}$ in p-channel devices (a) versus t for different L values in a log plot, and (b) versus L^{-1} for different t values in a semilog plot. The drain biases were fixed at $|V_D| = 7.3$ V. The three data points shown in solid symbols were used to determine the constants in Eq.(5-3).

42.92 V, n = 0.433. With these constants, we can calculate the parameter shifts for any V_D or t values. The results (the solid lines in Fig. 5-2) give an excellent agreement with the experimental data.

Fig. 5-3 presents the I_{DSAT}-shifts versus x (= L^{-1}) measured from p-channel devices, which were stressed at $V_{G,p}$ values of electron $I_{G,p}$ with V_D = 7.3 V. The associated constants A = 230.8, β = 1.3039 μm and n = 0.1553 were extracted in a similar way. The resulting prediction using (5-3) was compared with the experimental data. Again, the agreement between theory an data is shown to be satisfactory.

However, as shown in Fig. 5-3a, for all data set, the slope is very large for short stress times but significantly reduces to a smaller value beyond 100 seconds. The same sets of data, when plotted vs x with t used as the parameter (Fig. 5-3b), explicitly shows that the slope of the data set of the smallest stress time is larger than the rest.

This bimodal degradation behavior in time of p-channel device is expected, as discussed in [5]. For a fresh sample, the time rate of change in device degradation is large for the first few seconds of stress, since the hot-electron injection is greatly enhanced by the strong oxide field in the low $|V_G|$ bias region. With increased electron trapping in the oxide, however, the field produced by the trapped charge itself slows down the degradation [5]. The degradation rate, therefore, reaches a smaller but stable value within a short period of time. In estimating τ, this transient degradation behavior can be

neglected and one may analyze the stable slopes which are independent of t as shown in Fig. 5-3.

5.4 Conclusion

In summary, the worst case lifetime τ_w, in both n- and p-channel MOSFETs is given by inverting (5-3) in the form,

$$\tau_w = (f_{max}/A)^{1/n}\exp(-\beta x/n) \tag{5-4}$$

This model directly specifies τ_w as a function of V_D and L without resorting to I_{SUB} or I_G. The exponential factor in (5-4) is rooted in a new E_L-model of (5-2). Equation (5-4) is valid for both n- and p-channel devices. The model can also be extended to V_G-values other than $V_{G,p}$ by scaling f_{max} correspondingly with I_{SUB} or I_G at the given V_G.

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