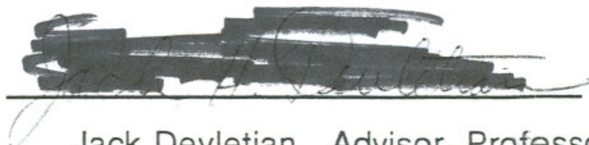
The Microstructural Effects of Metallization and Heat Treatment on Thin Gate Oxide for Use in Sub-Micron MOSFETs

John M. Mc Carthy
B.S. Physics, State University of New York at Stony Brook, 1969
M.S. Materials Science and Engineering
Washington State University,1987

A thesis submitted to the faculty of the
Oregon Graduate Institute
of
Science & Technology
in partial fulfillment of the requirements for the degree
Doctor of Philosophy in
Materials Science and Engineering
January 1996

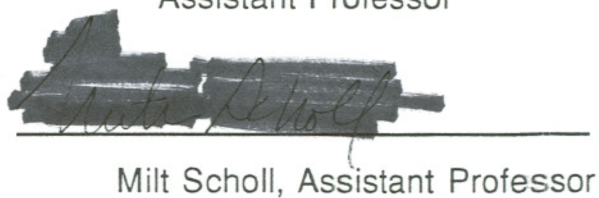
The dissertation "The Microstructural Effects of Metallizations and Heat Treatment on Thin Gate Oxide for Use in Sub-Micron MOSFETs" by John M. Mc Carthy has been examined and approved by the following Examination Committee:



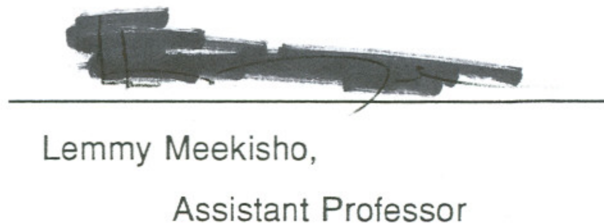
Jack Devletian, Advisor, Professor

Dr. Ken Cadien, Intel

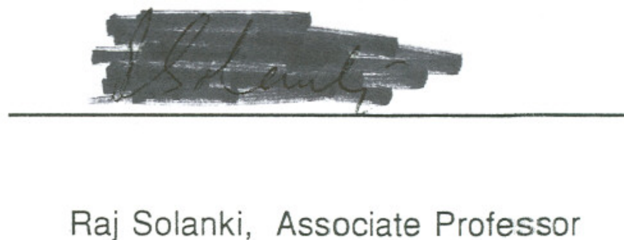
James T. Stanley,
Assistant Professor



Milt Scholl, Assistant Professor



Lemmy Meekisho,
Assistant Professor



Raj Solanki, Associate Professor

Dedication

I dedicate this work to my wife Karen whose patience, support and advice helped me complete this difficult task.

ACKNOWLEDGEMENT

Bill Wood for the opportunity to pursue a doctorate in materials science

Leo Yau and his group at Intel for the electronic devices, BVG measurements, guidance and an interesting problem

Ken Cadien of Intel for his patient mentoring

Uhle Dahmen and his group at the National Center for Electron Microscopy at Berkley for the atomic resolution images of the SiO_2/Si interface and planar sections of the SiO_2

Jim Cser for his help with focused ion beam milling of TEM cross sections

Locke Christman of FEI Company for the FIB produced SIMS profile of the Al-.5Cu electrode

Glenn Ramirez for his micro-hardness measurements in Appendix III

TABLE OF CONTENTS

CHAPTER 1: INTRODUCTION 1

CHAPTER 2: OUTLINE OF EXPERIMENTS 5

CHAPTER 3: BACKGROUND 7

The Microstructure of SiO_2 10

Barrier Layers 14

The Microstructure of Metallizations 16

Interface Microstructures and Effects on Performance 16

The Thermodynamics of Interfacial Reactions 19

Gate Leakage Currents and Breakdown Voltage
Measurements 20

Analytical Electron Microscopy 22

High Resolution Electron Microscopy 23

Summary 23

CHAPTER 4: EXPERIMENTAL PROCEDURES 25

CHAPTER 5: RESULTS 34

SiO_2/Si as Deposited 36

SiO_2/Si Heat Treated for 2hrs at 400ºC in N_2 39

Al-1Si/SiO_2/Si as Deposited 40

Al-1Si/SiO_2/Si Heat Treated for 2hrs. at 400ºC in N_2 42
. Al-1Si/SiO_2/Si, 12hrs. at 400ºC in N_2 + Furnace Cool 44
Al-.5Cu/SiO_2/Si as deposited 48
Al-.5Cu/SiO_2/Si, 2hrs at 400ºC in N_2 51
Al-.5Cu/SiO_2/Si, 4hrs at 400ºC in N_2 54
Al-.5Cu/SiO_2/Si, 11.25hrs at 400ºC in N_2 63
Cr/SiO_2/Si as Deposited 66
Cr/SiO_2/Si, 2hrs at 400ºC in N_2 68
Cr/SiO_2/Si, 12hrs. at 400ºC in N_2 + Furnace Cool 72
Ti/SiO_2/Si, as Deposited 75
Ti/SiO_2/Si, 2hrs at 400ºC in N_2 76
Al Deposited on 7nm TCA SiO_2 Electron Beam Irradiated 78
W Deposited on Heat Treated SiO_2 Electron Beam Irradiated . . 81

CHAPTER 6: DISCUSSION 83

Comparison of the Al-1Si and Al-.5Cu Results 83
Cr on SiO_2 Results 87
Tables and Graphs of Results 88
Si Diffusion in the SiO_2 and BVG Performance. 107
The Reduction of Si Diffusion into the Al-.5Cu Electrode . . . 108
Microstructural Effects on the SiO_2 Caused by Si Diffusion. . 112
Electrode Grain Growth and BVG Performance 114
The Effect of Voids, Pores and Channels on Electrodes 119
The Effects of Si Diffusion on the Electrodes 119

Microstructural Changes in the SiO_2 Due to Heat Treatment . 123
Interface Roughness and Heat Treatment 126
Reaction Layers at the Interfaces 127
Summary 129

CHAPTER 7: Conclusions 132

References 134

Appendix i. BVG oxide Measurements, Histograms, Probability
Plots and Wafer Maps 139

Appendix ii. Hardness Measurements for Al, Al-Cu and Al-W . . . 170

Appendix iii. Determination of the Stress Levels in the SiO_2
Heat Treated for 4hrs. with a Directly Deposited
Al-.5wt%Cu Electrode 173

Biographical Note 176

LIST OF TABLES

1. Resistivities of Conductors 18
2. BVG Measurements for Metallization Disk Arrays on (100) Si Wafers with 7nm of Silica 35
3. Electrode Thickness, Growth Rate and BVG vs. Hours of Heat Treatment 90
4. The SiO_2/Si Reaction Layer Thickness 92
5. The Metal/Silica Reaction Layer Thickness 95
6. Silica Thickness and Heat Treatment 97
7. Electrode Grain Diameter and Heat Treatment Duration 99
8. Post Heat Treatment Si Diffusion Depths into Electrodes . . . 102
9. Silica/Si Interface Roughness and Heat Treatment 103
10. Electrode/Silica Interface Roughness and Heat Treatment . 103
11. Silica Structure and Heat Treatment 105

LIST OF FIGURES

1 a. Typical MOSFET 8

b. High speed sub-μm MOSFET 9

2 a. Optical image of (100) Si wafers with metallization 27

b. Enlargement of metallization disks 28

3 Optical image of FIB produced TEM cross-section 29

4 SEM image of FIB produced TEM cross-section 30

5 a. Atomic resolution TEM image of SiO_2 as deposited planar section 37

b. Atomic resolution image of SiO_2 as deposited transverse cross-section 38

6 a. TEM bright field image of planar section of SiO_2 heat treated for 2hrs at 400ºC 39

b. Atomic resolution image of planar section of SiO_2 heat treated for 2hrs. and decorated with W islands 40

7 TEM image of as deposited Al-1Si with selected area diffraction pattern of interfaces 41

8 a. TEM bright field and dark field of Al-1Si heat treated for 2hrs at 400ºC 43

b. TEM bright field and dark field images of nanocrystalline quartz in failed oxide 43

c. Al-1Si-2hrs, compositional profile 44

9 a. Bright field TEM image of Si, SiO_2 , Al-1Si and diffusion formed poly-Si after 12 hrs at 400ºC 45

9 b. SEM of cleaved Al-1Si metallization disks as
deposited and heat treated for 12hrs 46
c. Compositional profile for Al-1Si, 12hrs at 400ºC 47
10a. TEM bright field image of interfacial region of Al-.5Cu
as deposited with diffraction pattern 49
b. Al-.5Cu as deposited compositional profile 50
11a. TEM bright field image and diffraction pattern Al-.5Cu
heat treated for 2hrs. 52
b. Compositioinal profile for Al-.5Cu-2hrs 53
12a. TEM bright field image and diffraction pattern
for Al-.5Cu-4hrs 55
b. Compositional profile for Al-.5Cu-4hrs 56
c. Compositional profile showing Cu segregation 57
13a. TEM bright field image, planar section Al-.5Cu -4hrs 60
b. TEM bright field /dark field pair Al-.5Cu-4hrs 61
c. Planar section of oxide showing grain like structures
and diffraction pattern, Al-.5Cu-4hrs 62
d. FIB produced SIMS profile of Al-.5Cu-4hrs 63
14a. Bright field TEM image and diffraction pattern for
Al-.5Cu-11.25hrs 64
b. Bright field TEM image for Al-.5Cu-2hrs with a less
distinct diffusion zone for the Al and Cu 64
c. Compositional profile for Al-.5Cu-11.25hrs. 65
15. Bright field TEM image and diffraction pattern for
as deposited Cr 67

16a. Bright field TEM image and diffraction pattern for
Cr -2hrs 69
b. High resolution image of the SiO_2/Si interface for
Cr-2hrs 70
c. Compositional profile for Cr-2hrs 71
17a. TEM bright field and diffraction pattern for Cr-12hrs 73
b. Compositional profile for Cr-12hrs 74
18 TEM bright field and diffraction pattern for Ti as deposited. 75
19a. Bright field TEM Ti-2hrs 77
b. Diffraction pattern interfacial regions 77
c. Diffraction pattern Si 77
d. Diffraction pattern Si and Ti_3Si 77
20. Bright field TEM image and diffraction pattern for
as deposited SiO_2 79
21. Series of diffraction patterns produced by a region of
as deposited SiO_2
a. without Al 80
b. with Al 80
c. following electron irradiation 80
22. Atomic resolution TEM image of W islands deposited on heat
treated SiO_2 81
23. Diffraction patterns before and after electron irradiation
for W on heat treated SiO_2 82
24. Graph of electrode thickness vs. heat treatment time
for Cr 90

25. Graph of electrode thickness vs. heat treatment time
for Al-.5Cu 91
26. Graph of electrode thickness vs. heat treatment time
for Al-1Si 91
27. Si/SiO_2 reaction layer thickness as a function of time
at 400ºC in N_2 for Al-1Si 93
28. Si/SiO_2 reaction layer thickness vs. time for Cr 94
29. Si/SiO_2 reaction layer thickness vs. time for Al-.5Cu 94
30. Al-1Si/SiO_2 interface reaction layer thickness vs. time 95
31. Al-.5Cu/SiO_2 reaction layer thickness vs. time 96
32. Al-1Si electrode oxide thickness vs. time 98
33. Al-.5Cu electrode oxide thickness vs. time 98
34. Al-1Si grain diameter vs. time at 400ºC in N_2 100
35. Al-.5Cu grain diameter vs. time at 400ºC in N_2 100
36. Cr grain diameter vs. time at 400ºC in N_2 101
37a. Selected area electron diffraction pattern
as deposited, high and low Si flux oxides 106
b. Bright field TEM of oxide heat treated with Al-.5Cu
for 4hrs., planar section 106
38. Selected area electron diffraction pattern showing
increase in texture with increased heat treatment
time. 117

ABSTRACT

THE MICROSTRUCTURAL EFFECTS OF METALLIZATION AND HEAT TREATMENT ON THIN GATE OXIDE FOR USE IN SUB-MICRON MOSFETs

John M. Mc Carthy

Supervising Professor: Jack Devletian

Metals deposited directly on thin gate oxide to test the quality of the oxide must be stable. This research tests the stability of metals for possible use in gate oxide monitor current flow tests (GOM) or as a gate electrode in sub-micron MOSFETs.

Arrays of metallization disks with 5mm and 0.8mm diameters of Al-1wt%Si, Al-.5wt%Cu, Ti and Cr were magnetron sputter deposited directly on 7nm of thermally grown SiO_2 on (100) Si wafers and then heat treated at 400ºC in N_2 to determine the effect of heat treatment on break-down voltage(BVG) for the MOS thin film devices. Al-1wt%Si and Al-.5wt%Cu were also deposited on poly-Si electrodes. BVG measurements were performed on as deposited and heat treated patterned wafers. Analytical electron microscopy was performed on transverse cross-sections and planar sections of the devices to correlate good and bad BVG performance with microstructural changes that occurred during heat treatment. A mechanism of oxide breakdown was proposed based on observed changes in microstructures and chemistries of the thin films.

Metallizations that maintained a high BVG, Cr and Al-.5wt%Cu, were given extended heat treatments to test stability and to characterize their diffusion barriers, nanometer scale layers of Cr_2O_3 and Al_2Cu respectively, which limited diffusion of the substrate Si into the electrode. Al-1wt%Si, the electrode with the lowest as deposited BVG, was given an extended heat treatment to characterize the mechanisms of change in the metallization, silicon dioxide and Si which lead to SiO_2 breakdown.

Structural changes in the oxide were detected with electron diffraction patterns following heat treatment. Nearest neighbor distances were reduced and nano-crystalline quartz appeared in the originally completely amorphous silica heat treated with an Al-1wt%Si electrode. The mechanisms of reduction of the BVG for oxides during heat treatment with a metallization is structural damage to the amorphous silica caused by the diffusion of Si from the substrate through the oxide into the electrode, the difusion of metal into the oxide and reduction of oxide thickness by reaction with the metallization. The Al-1wt%Si as deposited directly on SiO_2 and heat treated, had the lowest BVG's and had sustained the greatest number of atomic displacements which resulted in quartz crystallites forming within the vitreous silica.

1. INTRODUCTION

The reduction of the dimensions of structures in microelectronic devices makes the control of diffusion and nanometer scale defects crucial to the performance and reliability of these devices. The ability to produce stable, defect free thin layers of insulators and conductors reduces leakage currents, increases the break down voltage and increases service life. Interfaces that are atomically flat minimize surface states and traps which decrease the numbers of charge carriers and their mobility. A flat interface also decreases parasitic capacitance which limits the speed at which a device can run. Reactions between the metallization and the gate oxide must be eliminated or limited to preserve defect free thin films with flat interfaces. Reactions include precipitation, diffusion and phase changes within and between the component thin films which can cause the degradation of the gate electrode and oxide and may contaminate the Si substrate. In the submicron metal-oxide-silicon-field-effect transistor (MOSFET) diffusion distances are smaller between metal conductors and the Si since the insulating layers have been reduced to less than 10nm bringing metals such as Ag, Au, Cu, or Al close to the Si/SiO_2 interface and the shallow junctions of the MOSFET where trapping states can be introduced and the performance of the device degraded. The reduced surface area of the gate electrode in the sub-micron MOSFET increases current densities in the commonly used, highly doped, high resistivity poly-Si (500μohm-cm) to the point that power limits

require the use of a lower resistivity conductor such as stable refractory W deposited directly on the gate oxide or a lower melting point metal such as Al or Cu deposited on barrier layers such as TiN or Ti-W are necessary to limit diffusion.(1) Pores, pinholes and small grain size are microstructural defects that limit the effectiveness of the barrier layer as a conductor and a diffusion barrier. The gate structure can also be degraded by pores in the oxide which serve as rapid diffusion and low resistance current paths to the silicon.(2,3) Diffusion and the proximity of dissimilar materials can lead to phase changes at interfaces (precipitates) which at best roughen interfaces and if on a scale approaching the thickness of the thin films can cause shorts or degrade diffusion barriers. The films used in semiconductor devices must not go through unexpected phase changes that may roughen the interface or introduce undesirable electronic characteristics during processing or during subsequent service. These microstructural defects and characteristics visible and measurable in an analytical TEM/STEM, can control the performance of thin films in microelectronic devices.

The deposition of microstructural and electronic defect free homogeneous oxide thin films on semiconductor substrates at low temperatures is desirable to produce predictable shallow junction devices that are less susceptible to environmental breakdown and interdiffusion. The techniques to produce such films are low pressure chemical vapor deposition, plasma enhanced chemical vapor deposition and the dry thermal growth of oxide. This research

gives a better understanding of the mechanisms of change in single and multilayered metallic electrodes on high quality thermally grown 7nm silicon dioxide through detailed TEM/STEM microstructural analysis. Understanding diffusion and phase changes in the gate structure will permit the control of degradation such as poly-Si dopant depletion(4) and the reduction of the resistivity of the gate oxide. Metals were deposited on 6 to 8nm thick oxide films on a Si substrate. Heat treatments on the MOS devices were done in a quartz lined furnace with an N_2 ambient. Break down voltage measurements were done on heat treated specimens and on as deposited MOS devices.

The microstructure of the metal electrode and its interface with the silica were studied. Features such as grain size and interface roughness were measured. In studying the insulator, the conductor and the diffusion barrier, if present, emphasis was placed on understanding diffusion processes, microstructural changes and phase changes at interfaces and within the thin films in these reduced vertical dimension devices. A new mechanism of oxide degradation is proposed. Defects associated with poor performance or severe breakdowns were identified.

The goal of this work is to identify conductors for use in thin films to permit the rapid fabrication of metal/oxide/Si (MOS) devices with an as deposited high oxide breakdown voltage which is maintained during heat treatment. This MOS device will permit the rapid testing of thin gate oxide during the manufacture of sub-μm

MOSFETs. Such conductors could also be used to produce MOSFETs with high speed, high charge carrier mobility and low power consumption.

2. OUTLINE OF EXPERIMENTS

The creation of ohmic contacts to the source and drain of a MOSFET, following Ti deposition, requires heat treatment at 400ºC to form $TiSi_2$ in a N_2 ambient for 2 hours. Czochralski Si wafers, 6 inches in diameter with 7nm of oxide on the surface had arrays of 5mm disks of metal 0.2μm in thickness deposited by magnetron sputtering. Single film metallizations deposited directly on the oxide included Al-1wt%Si, Ti, Al-.5wt%Cu and Cr. Metallizations using doped poly-Si as an electrode include Al-1wt%Si and Al-.5wt%Cu. These wafers were given a heat treatment at 400ºC in N_2. In addition to complete wafers deposited with a large number of metal disks small portions of wafers deposited with Al-1wt%Si, the worst BVG performer, Cr and Al-.5wt%Cu the best performers were given extended heat treatments to better understand thermally caused microstructural changes in the Al-1Si and test the stability of the Al-.5Cu and Cr electrodes. Findings in this study establish the formation of a hard (see Appendix II) relatively high melting point Al-Cu intermetallic at grain boundaries and interfaces to stabilize soft, low melting point Al. Analytical electron microscopy was performed on planar sections and transverse cross-sections of these metal-oxide-silicon(MOS) devices. Interface roughness, inter and intra film phase identification, thickness, grain size, composition and texture were measured and comparisons between the control and the heat treated specimens made. Correlations were made between heat treatment caused

microstructural changes and performance as indicated by breakdown voltage measurements.

In addition to experiments with thin metal films of the thickness to be used in devices(100-300nm), electron transparent metal films (less than 100nm) were deposited on the gate oxide. TEM/STEM in-situ experiments with planar sections of the metal, metal/SiO_2 and metal/SiO_2/Si were performed. Planar sections of the in-situ and heat treated metal disk specimens permit the examination of hundreds of square microns of interface whereas transverse cross-sections produce interface areas limited by the thickness of the foil($<0.1\mu m$). Selected area electron diffraction of these planar sections provided high sensitivity to small volume fraction phase changes at the interface allowing characterization of the nucleation and initial growth of new phases. Initial nucleation could also be studied if growth was interrupted in the 0 to 3nm thickness range for the metallization layer or layers. The large sample of interface insured that the microstructures observed would be representative.

3. BACKGROUND

A metal-oxide-silicon-field effect transistor (MOSFET) is a switch that permits current to pass between it's source and drain by applying a field through a thin oxide layer to a narrow channel of Si (gate) between the source and drain . A early design and a high performance submicron MOSFET design with W vias is shown in figure1. Notice that much of the areas of metal contacts of source, drain and gate are above the field oxide to minimize parasitic capacitance, the relatively high resistance poly-silicon electrode and the very thin 7nm gate oxide.

A thin gate oxide causes four major problems; increased leakage currents, the accelerated introduction of metal from the electrode to the doped Si substrate containing the source, the drain and the gate channel, the accelerated migration of Si and dopants into the gate electrode and possible phase changes in these diffusion zones. Leakage currents, diffusivities, the thickness of films and grain size will largely determine how soon, the degree of and types of microstructural changes that occur in these multi-layer MOS devices during processing heat treatments and service.

Phase changes will occur at interfaces and be small in volume fraction at first. Electron diffraction will permit the detection of these phases and their identification during the early stages of nucleation and growth.(5) Conventional methods of detection such as X-ray diffraction and Rutherford backscatter techniques would

not detect layers of materials less than 20nm thick nor do they give morphological and exact location information available from electron microscopy.(6) Analytical electron microscopy can give a much more detailed and complete microstructural evolution of the films and reduce the thickness detection limit by an order of magnitude.(5) A large part of the research will involve identifying the sources of reactants and the reaction products following heat treatment.

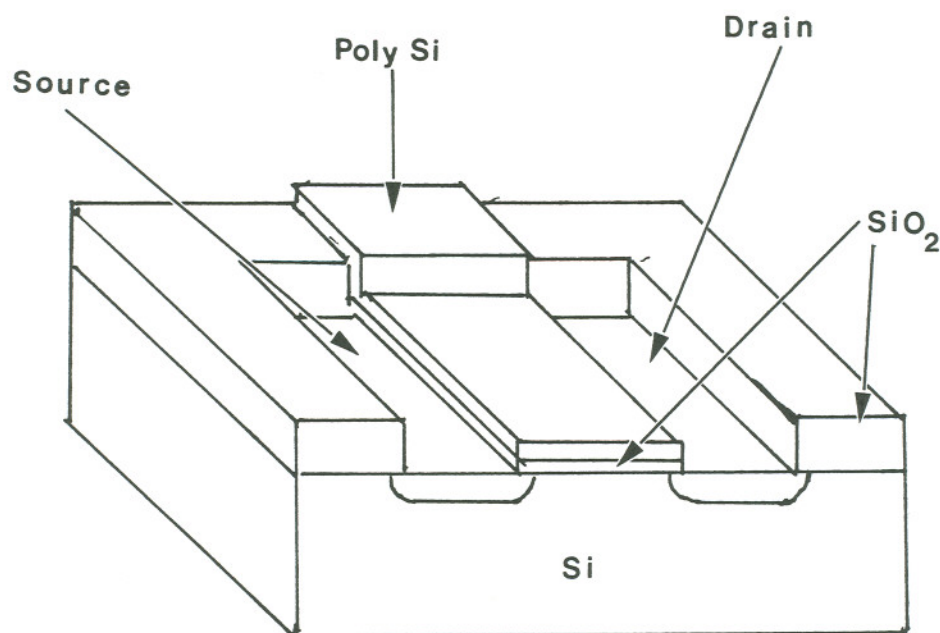


Figure 1a. Typical MOSFET with a doped polysilicon gate electrode.

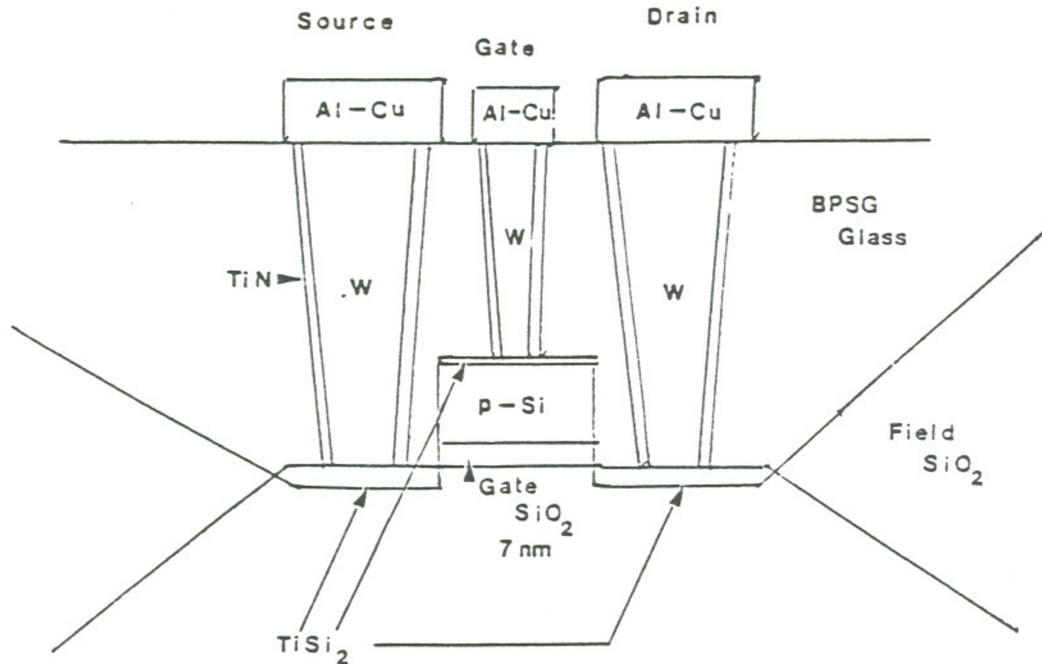


Figure 1b. Very high speed sub-μm MOSFET with W vias.

The commonly used, effective, thick and low conductivity poly-silicon electrode adds to the series resistance of the device and adds a step to the fabrication process. A metallization that would be compatible with direct contact to the Si of the drain and the source and to the SiO_2 of the gate would simplify fabrication, provide a rapidly deposited test electrode, increase read-write frequency and diminish power consumption. W and Mo, refractory metals, directly deposited on SiO_2 have been successfully used as

gate electrodes.(7-16) Alternatively a thin, high conductivity, diffusion barrier-electrode such as TiN or Ti-W could be used instead of a poly-silicon electrode.

In the following sections the thin film building blocks of a sub-micron MOSFET gate structure are discussed; the SiO_2, diffusion barriers, metallizations and the interfaces. The final sections discuss the primary characterization techniques; analytical electron microscopy, high resolution electron microscopy and break-down voltage measurements.

The Microstructure and Properties of SiO_2

Thermally grown and chemical vapor deposited (CVD) SiO_2 used in the electronics industry is an amorphous solid with short range order having a Si atom at the center of a tetrahedron covalently bonded to 4 oxygen atoms at the vertices of this unit cell with equal O-Si-O bond angles. The tetrahedra in turn have common O atoms at their vertices with other tetrahedra producing Si-O-Si bonds with random angles. These tetrahedra at most have a common edge but never a common face forming a randomly connected network with a variable density and pores which does not tile space as do the unit cells of crystalline material.(17-19) Material with this type of short range order is referred to as vitreous. Thermally grown vitreous silicon dioxide has high resistivity, limited reactivity, diminishes the dangling bond concentration at the surface of Si from

10^{15} to $10^{10}/cm^2$(17) and is a poor diffusion barrier compared to chemical vapor deposited (CVD) SiO_2. These properties and characteristics help to define the advantages gained and problems encountered when attempting to fabricate a gate with 6 or 7nm of silicon dioxide. SiO_2, thermally grown in a dry O_2 ambient, diminishes trapping states at the Si surface best and has the lowest trap density within the oxide. The pores provide low resistance leakage current and rapid diffusion pathways through the oxide.

SiO_2 is grown on a (1 0 0) Si wafer with a minimum number of electronic defects by heat treatment in a double walled quartz tube furnace containing an O_2 ambient. The free energy of transformation for this oxide is -180kcal/mole at 400ºC making it a very stable compound.(20) Oxide grown thermally has the highest surface state reduction at the Si/SiO_2 interface but high diffusion coefficients for metals. A nanometer of the interfacial oxide is reported to be a sub-oxide where the Si/O ratio approaches 1 for the first few atomic layers. (21-24) Thermal oxide grown with water vapor present in the ambient shows no evidence of pores suggesting that it is a better diffusion barrier than dry ambient thermal oxide.(25) Chemical vapor deposited (CVD) oxide has a poor reduction of surface states but is a good diffusion barrier. CVD and "wet" oxide are not good choices for use as a gate oxide due to a high density of electronic defects that result in a high density of fixed charge, a high polarization field and trapping states. In one study stable high breakdown voltage gates were fabricated by capping the thermal gate oxide with a thin layer of CVD oxide as a diffusion barrier.(18)

The growth mechanism of SiO_2 is of interest in this research because it is controlled by the diffusion of molecular oxygen through the growing SiO_2 which does not react with the migrating O once the thickness reaches 2nm.(26,27,28) The mechanisms of diffusion for O may shed light on the diffusion mechanisms for metals or other constituent elements of the MOSFET that do not react or react weakly with the oxide. The time dependence of oxide thickness was successfully determined in the 1960's with a linear-parabolic function.(29,30,31) The mass transport during initial (0 to 10nm) oxidation is much faster than predicted by Fickian diffusion implying that the oxide is less continuous and contains defects that permit direct or easier access to the Si/SiO_2 interface. This suggests a connected network of pores that provide continuous paths to the interface of lengths equal or near equal to the thickness of the oxide film. The mechanism of oxygen transport to the interface becomes Knudsen-Poiseuille flow in micropores.(32)

(1) $dn/dt = kC/L$ = atoms/cm^2/sec.

k=constant,

n=number of atoms,

t=time sec.

C=concentration of O_2 at oxide surface

L= average pore pathway through oxide

The connected pore networks are of a range of lengths and the number of these networks that are continuous from the Si/SiO_2 interface to the outer surface decreases as the oxide becomes thicker and this causes the linear time dependence of oxide growth to become parabolic. Diffusion proceeds by a combination of pore, pore network, vacancy, interstitialcy and interstitial mechanisms. Pore and pore network mechanisms dominate when the thickness of the film is less than 20nm and the film density is low. The density of point defects in the SiO_2 such as vacancies, interstitials and impurities determine the diffusion coefficient for diffusion by the vacancy or interstitial mechanisms.

An alternate description of the SiO_2 structure includes the concept of disclinations. In this description the tetrahedra do fill space but these tetrahedra are distorted to varying degrees to accomplish this. This distortion means bond lengths and angles vary from the normal SiO_2 structure. In the (3,3,5) structure 5 tetrahedra with equilateral triangles as faces are common to each bond. These tetrahedra miss filling space by 7.4º. This structure can fill space if bond lengths and angles to nearest neighbors are not the same. This variation from the normal short range order is called disclinations.(33) In this model high diffusion coefficient paths would be in regions with high disclination densities or high strain. If a region has a high concentration of interstitials there will be an increase in the number of strained bonds(disclinations). This strain in the structure is added to the normal strain developed by the inability of the SiO_2 to fill space with undistorted tetrahedra.

Disclinations are a means of describing defects in amorphous materials analogous to dislocations in crystalline material. There is no means at present to measure the magnitude or direction of the strain of disclinations as there is for dislocations.

Barrier Layers

Barrier layers are added to a metallization system to eliminate or severely impede diffusion between metal conductors and the substrate containing devices. Eighty percent of failures during service or processing of VLSI (very large scale integration) ICs (integrated circuits) can be related to the multilevel metallization. The submicron MOSFET is a component of the next level of miniaturization ULSI (ultra large scale integration). This makes barrier layers more important since diffusion distances are shorter. A barrier layer must adhere to oxide and nitride films. The metal used for interconnects must adhere to it. The barrier layer must utilize etch and deposition processes that are compatible with those of the interconnect metal. The film must contain low stress and provide a poor mass transfer path at thicknesses <200nm. Step coverage is also very important. Barrier layers are thin films and if defect structures extend through the film these structures become a controlling factor in mass transport at low temperatures. Microstructural features such as grain boundaries determine whether the film is an effective diffusion barrier. The diffusion coefficient for a grain boundary is orders of magnitude greater than the diffusion coefficient for the matrix. Bulk diffusion through the

matrix of the barrier material becomes a less effective conduit of mass when compared to the rapid diffusion along grain boundaries.(34,35) Stuffing grain boundaries by causing precipitates to nucleate and grow there can control or eliminate low temperature diffusion along these rapid pathways.(36)

Diffusion barriers fall into three major categories: stuffed, passive compound and sacrificial. Stuffed diffusion barriers are those in which solutes segregate to rapid diffusion paths such as grain boundaries where a phase change occurs to impede or stop low temperature mass transfer on that path. Passive compound barriers are usually nitrides, carbides or borides of early transition metals such as Ti or a high temperature alloy such as Ti-W(36). The passive compound barrier is a material with very strong bonds, high melting point, low reactivity with the metal and silica, low vacancy concentration at processing temperatures and high Young's modulus making distortion of the lattice difficult. These properties give this class of materials low diffusion coefficients and high stability.(36) A sacrificial boundary is one that is partially consumed by the materials that it is attempting to separate. The reaction must be self limiting and form a product of predictable thickness with a low diffusion coefficient for the elements in the materials being separated. An advantage of sacrificial barriers is that they are more complete with fewer pinholes than conventionally deposited thin films since they are formed by solid state reactions.

The Microstructure of Metallizations

Conductors to be used as contacts or interconnects must have low resistivity to minimize series resistance which is increased by the reduction of their cross-sections for the design of efficient submicron MOSFETS. Resistivity in a metal is controlled by grain size, twins, stacking faults, dislocation density, precipitate density and impurities that act as conduction electron scattering centers.(37) These microstructural characteristics can be measured and quantified easily using analytical electron microscopy for comparison and correlation with resistivity and other bulk electronic measurements. Poly-silicon, which was suitable for VLSI with a resistivity of 500 micro ohms-cm increases the power consumption as the device becomes smaller making higher conductivity metals a better choice. See table 1. Poly-Si is a proven, stable contact material for the gate oxide. When other metals are considered their reactivity with the gate oxide and the final interconnect conductor must be considered as well as compatability with subsequent processing etching and heat treatments. The microstructure and composition of a metallization will control its reactivity.

Interface Microstructures and Effects

The interface of an electronic material with other materials determines the capacitance, the barrier height, contact resistance, and numbers of trapping states. The surface of a material

introduces trapping states in the bandgap that are roughly equal to the atomic density of the crystallographic plane exposed. There is one dangling bond associated with each surface atom. The number of dangling bonds per atom at a step edge in the surface increases. The number of surface states for clean oxide free (100) Si is 10^{15}. When this surface is reacted with dry O_2 the number of states decreases to 10^{10}.(17) If the SiO_2/Si interface is along an absolutely flat (100) plane, the number of dangling bonds present at the surface is at a minimum.(38) Measurements on atomic resolution images of this interface of the gate oxide used in this experiment proved average step heights to be 0.44nm with a frequency of 17/100nm. See figure 5b. The outer surface of the oxide without metallization showed a similar roughness. This roughness increases the surface area of the interface and thereby its capacitance in addition to also increasing the number of trapping states. This increased interface area increases the voltage V_g necessary to cause the inversion of the Si surface of the gate that switches on the flow of current in the MOSFET. Parasitic capacitance limits the speed at which the device can operate. In addition to detrimental electronic effects there are also adverse stability effects. Increased interface areas for both the metal/SiO_2 and the SiO_2/Si interfaces provide more nucleation sites for phase transformations requiring less interface free energy than in the bulk. This decreases the stability of the conducting and insulating thin films. The Si/SiO_2 interface roughness has been thefocus of research and new techniques of cleaning prior to thermal oxide growth with a roughness of 0.1nm.(39-41)

Table 1. Resistivities of Conductors

	A	B	C	D	E
1	Conductor	Resistivity	Temperature Coefficient	Work function	Melting point
2		μΩ-cm	of resistance per ºC	Volts	ºC
3					
4	Ag	1.59	0.0041	4.73	961.93
5	Cu	1.67	0.0068		1083.4
6	Au	2.35	0.004	4.82	1064.43
7	Al	2.65	0.00429	4.08	660.37
8	Rh	4.51	0.0042	4.8	1966
9	Mo	5.2		4.2	2610
10	In	5.3	0.003925	5.3	156.61
11	W	5.65	0.0044	4.52 (001)	3410
12	Co	6.24	0.00604	4.4	1495
13	Ni	6.84	0.0069	5.02	1455
14	Os	9.5	0.0042	4.55	2700
15	Fe	9.71	0.00651	4.04	1535
16	TiB2	6 to 10			2900
17	Pt	10.6	0.003927	5.34	1772
18	Pd	10.8	0.00377	4.98	1554
19	Ta	12.45	0.00383	4.19	2996
20	Nb	12.5		4.01	2468
21	Cr	12.9	0.003	4.6	1857
22	Re	19.3	0.00395	5.1	3180
23	Hf	35.1	0.0038	3.53	2227
24	Zr	40	0.0044	4.21	1852
25	Ti	42		4	1660
26	ZrN	20 to 100			2980
27	HfN	30 to 100			3000
28	TiN	40 to 150			2950
29	NbN	~50			2300
30	TiC	~100			3257
31	TaC	~100			3985
32	TaN	~200			3087

The Thermodynamics of Interface Phase Transformations

Three types of solid state reactions can occur at and near an interface. There can be interdiffusion or mixing of the dissimilar materials and then precipitation of new compounds can occur on one or both sides of the interface. The reaction can be limited to the interface with little interdiffusion forming a few monolayers of reaction product. If a eutectic temperature exists(lowered melting point of the mixture relative to the melting points of the separate elements before mixing) then the stability of the contact and gate will be severely degraded by diffusion, grain nucleation and growth or melting and subsequent solidification. Phase changes at interfaces occur at lower temperatures and lower bulk concentrations than predicted by bulk thermodynamics due to the reduction of the volume of compound necessary to form a critical nucleus and continue to grow (bonds form and break by thermal movement). A tool that provides the prediction of which reactions will occur under equilibrium conditions is a ternary phase diagram with Si, metal and O axes.(42) Also if the enthalpies of formation of the reactants and products of a suspected reaction are known the difference between the sum of the enthalpies of the products and sum of reactant enthalpies predicts whether the reaction will occur. If this difference is negative it will occur.(5) Analytical Electron microscopy(AEM) of thin films subjected to rapid thermal annealing (RTA) for a range of temperatures and lengths of time permits the detection of all reactions that occur in the film until an equilibrium phase is reached.(4) This allows the construction of accurate phase

diagrams for metal, Si and O mixtures.

Gate Leakage Currents and Breakdown Voltage Measurements

A high quality gate oxide is an extremely good insulator conducting very small amounts of current. When the gate oxide is reduced in thickness to 7nm, the field becomes very high and currents begin to flow as electrons tunnel from metal contact through the oxide into the Si substrate. This current increases as the field is increased by increasing the gate bias voltage(V_g). A bias voltage of 8 volts on 7nm thick gate oxide produces a field of 11.4×10^6V/cm. The gate oxide can be poor and very conductive immediately by a catastrophic cascade of charge through the oxide or it can degrade as this strong field causes more and more charge to tunnel through the oxide until it is no longer an insulating film.(43,44) If the field in the oxide is uniform and in reality it is not, the Fowler-Nordheim leakage current (J) expression determines this tunneling current.

(2) $$J = AE^2_{ox}\exp(-B/E_{ox})$$

where A= a constant

B= a constant

E_{ox}= field strength in oxide

Good oxide has a breakdown field of 10-15MV/cm using conventional C-V spots of 5mm diameter and a probe station. Sah

estimates that if the oxide is perfect the theoretical limit is 25MV/cm. A breakdown voltage gate(BVG) measurement is obtained by two methods. Thin film metal disks are deposited on silicon dioxide on single crystal Si. A voltage with a constant rate of increase (ramp) is applied to the disk until catastrophic failure of the oxide as an insulator occurs or until a criteria current is reached. The BVG measurement is used to test the quality of oxide being produced during IC fabrication.

Recent measurements with a metallized probe fitted atomic force microscope(AFM) in direct contact with the oxide found regions with a BVG of 40MV/cm. These AFM measurements were also done on sub-micron C-V spots 500nm in diameter and the maximum BVG dropped to 30 MV/cm. This suggests that BVG has a local variation dependent on lateral position. The lateral resolution of the metallized probe technique was 40nm. The variation was 90% of the maximum BVG measured for the 1.2μm square scanned. Areas of low BVG varied from 30-300nm.(45) Conventional BVG measurements apply compression to the oxide in the vertical direction when a W-Ni probe is placed on the metal thin film disk. Compression of the oxide or actual micro cracks could explain the much lower BVG measurements obtained when the relatively heavily loaded macroscopic probe is used. The load exerted by an AFM probe is orders of magnitude less than the load exerted by a conventional probe.

Analytical Electron Microscopy (AEM) Techniques

AEM provided a means of detecting and measuring nanometer scale defects. The compositions of cylindrical volumes of material as small as 30nm in diameter and 30nm in height were measured to determine the degree of interdiffusion between films. Compositional profiles of heat treated and as deposited films were produced. Selected area and micro-diffraction provided structural information from these same small volumes to identify the crystal structures present allowing the identification of compounds present by a search of data bases. The identification accomplished by AEM on as deposited films and heat treated films is a powerful tool for predicting the temperature at which these films react and where new phases occur in the films. Dark field - bright field pairs showed directly which grains or films are producing a specific diffracted beam or set of beams. The position of a diffracted spot relative to the transmitted spot is used to determine a d-spacing of the compound's crystal structure. This d-spacing can be an identifier for that compound and using this diffraction spot to create an image of the diffracting grains produces a distribution map of the compound. AEM analysis provided feedback on the effects of processing on microstructures which may control a property important in the performance of a film.(46, 47)

High Resolution Electron Microscopy

Lattice images and atomic resolution images of crystalline/amorphous interfaces in an MOS device provided characterization on an angstrom scale of interface roughness, distortions in the lattice of a crystalline material or defects in the amorphous gate oxide. These images are actually interference patterns that are the result of constructive and destructive interference between the transmitted and scattered beams.(48) The interpretation of these images is not obvious and require simulation programs to understand. A through-focus series of images must be taken and compared with simulated images for a range of thicknesses and defocus values to correctly interpret the high resolution images.

Summary

This work identified metallizations that are compatible for use in the gate structure of sub-micron MOSFETS. Breakdown voltage measurements for the gate were used as an indicator of performance. Stability in processing was tested by heat treatments at processing temperatures and ambients on insulator and conductor thin film pairs at thicknesses used in the MOSFETS. Selected pairs with a reduced thickness metallization were subjected to in-situ transmission electron microscope experiments to determine the sequence of phase transformations. Phase transformations were

detected and characterized. Microstructural changes were also monitored on a nanometer scale. Criteria for suitable metallizations were developed and acceptable metallizations chosen from the test matrix. New mechanisms for loss of gate oxide resistivity and performance were proposed.

4. EXPERIMENTAL PROCEDURES

Arrays of metallization C-V discs with 5mm and 0.8mm diameters were magnetron sputter deposited on 6" diameter (100) Si wafers with 6 to 7nm of SiO_2. Standard techniques of producing low damage Si wafers, high quality oxide and metallizations were used by INTEL corporation to produce these 6" test wafers. See figure 2. Entire wafers or small groups of discs cleaved from the wafers were then given heat treatment in a tube furnace with a quartz liner with an ambient of N_2 at 400ºC for 2, 4, and 12 hours. Entire wafers were given the 2hr. heat treatment only. Breakdown voltage gate(BVG) measurements were performed on as deposited and post heat treatment C-V disks using a W-Ni probe station and a HP4145B to simultaneously ramp a voltage applied to the probe and measure the current flowing through the oxide. The wafer or portion of a wafer is placed on a microscope stage with the probe just above the wafer. The distance is then decreased between the probe and metallization disc until the probe deflects slightly when viewed through the microscope, indicating contact. The voltage ramp is started, voltage and current values stored and then plotted by the HP4145B to determine the voltage at which a precipitous increase in current through the oxide occurs, the BVG or a criteria current is reached. The 0.8mm diameter discs were used to stress the oxide with high current density to actual breakdown in the experiments done on portions of wafers with the Al-Cu metallization discs deposited directly on the oxide. A criteria current, 10μA, was used

to determine BVG for the large discs on whole wafers for the as deposited and 2hr. heat treatment wafers. The BVG(5mm discs) maps of the 6" wafer specimens in Appendix 1 were generated by INTEL corporation.

TEM transverse cross-sections of the metallization discs, oxide and Si substrate were then produced in a conventional ion mill or a focused ion beam milling machine (FIB) . The conventional ion milling method of producing electron transparent transverse cross sections for examination in a TEM requires the gluing of two 5mm x 2mm wide strips containing the metallization, metal surface to metal surface. A low viscosity two part epoxy containing nano-crystalline quartz was used to provide an extremely strong 0.1μm joint. This jointed bar was then cut perpendicular to the metallization to produce slices with the interfaces and glue joint in the center of a 1x2x0.5mm cross section. This section was then thinned to 6.0μm by mechanical grinding in preparation for conventional ion milling.(49) The section was mounted with Crystalbond wax on a grinding stub and ground to a 1μm finish producing a nearly scratch free surface starting with 9μm 3M SiC imperial lapping disks on glass and finishing with 1μm disks holding the stub in a Gatan precision polisher. A 50μm thick Mo washer with a 3mm O.D. and 1mm I.D. was laminated to this surface with super glue as a means of protecting the fragile joint during grinding. The specimen stub is then heated to release the specimen-washer laminate so that it can be remounted with the wax washer side down. Grinding the specimen is then continued until the Mo washer begins to grind and exposes the washer nearly to its hole. At this

point the specimen is 6μm thick.

A second support washer is then laminated to the specimen to further protect this thin section during handling. The specimen stub is again heated to release the wax and the specimen is removed horizontally to eliminate forces perpendicular to the thin section exerted by the wax. The specimen is rinsed in acetone briefly and then methanol to remove all traces of wax. The specimen is then ion milled until perforations appear at the interfaces. This produces electron transparent metallization, oxide and Si substrate simultaneously so that analytical TEM/STEM work can be done at the interfaces and within the thin films and substrate.

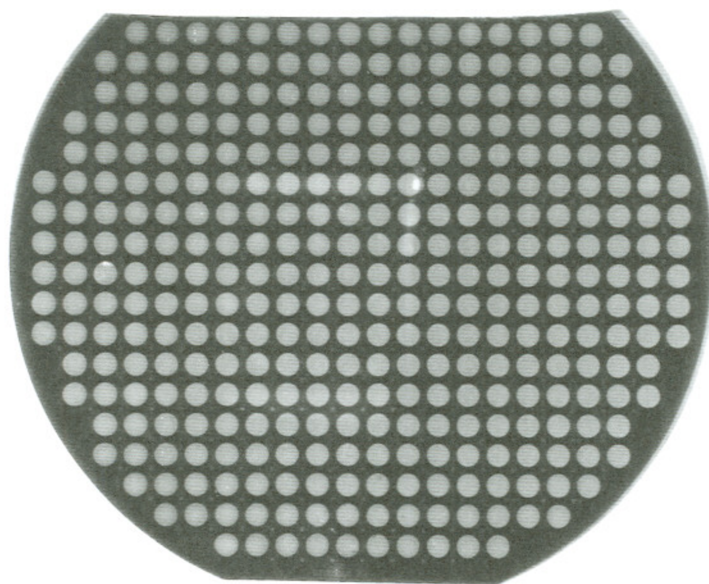


Figure 2a. Optical image of 6 inch (100) Si wafers with a thermally deposited TCA SiO_2 and magnetron sputtered 5mm diameter C/V metallization disks.

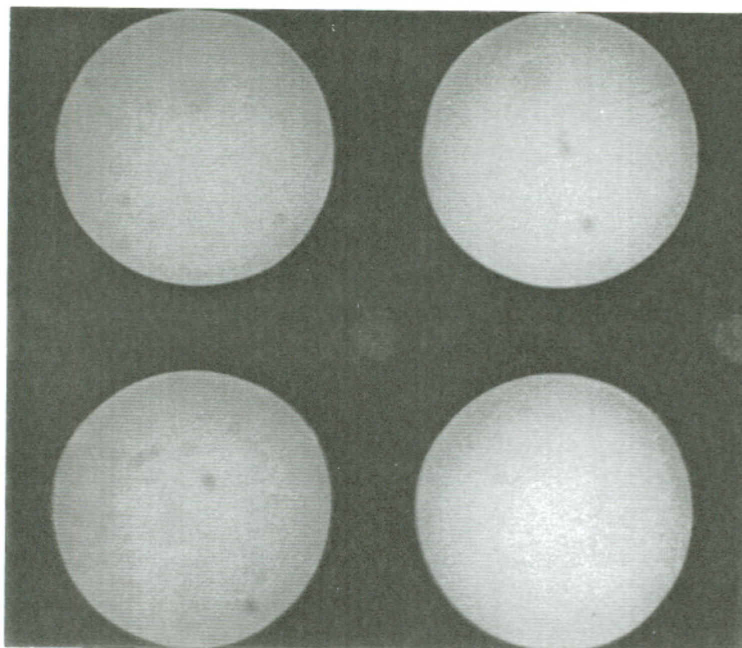


Figure 2b. Enlargement of disks.

The first step for the FIB method was cutting perpendicular to the metallization down through the SiO_2 and Si substrate with a low speed diamond saw. Two such cuts were made 500 microns apart. This bar containing metallization, oxide and substrate was then ground on the saw cut surfaces until 30 microns thick. This thin section was then reinforced by laminating a half molybdenum 3mm diameter washer to the bar. See figure 3. This specimen was then placed in a focused ion beam precision milling machine(FIB) with the metallization perpendicular to the beam direction. The FIB was then used to "write" a Pt bar on the metallization 1μm wide parallel to the vertical surfaces of the cross-section. Then 2 rectangular prisms of metallization, oxide and Si approximately 20μm wide, 15μm long and 10μm deep were removed by the FIB on both sides of the Pt masking bar. The remaining 1μm thick wall containing Pt,

metallization, oxide and Si was then milled to electron transparency. Figure 4 is a SEM image of such a FIB produced wall. The beam used to produce this image was a 200kV beam that passed through the wall to produce secondary electrons from surfaces behind the wall that in turn passed through the wall to make those surfaces visible. This is essentially the specimen preparation technique described by Bassile et. al. in reference 50. In the present study molybdenum half washers were used instead of Cu for greater rigidity.

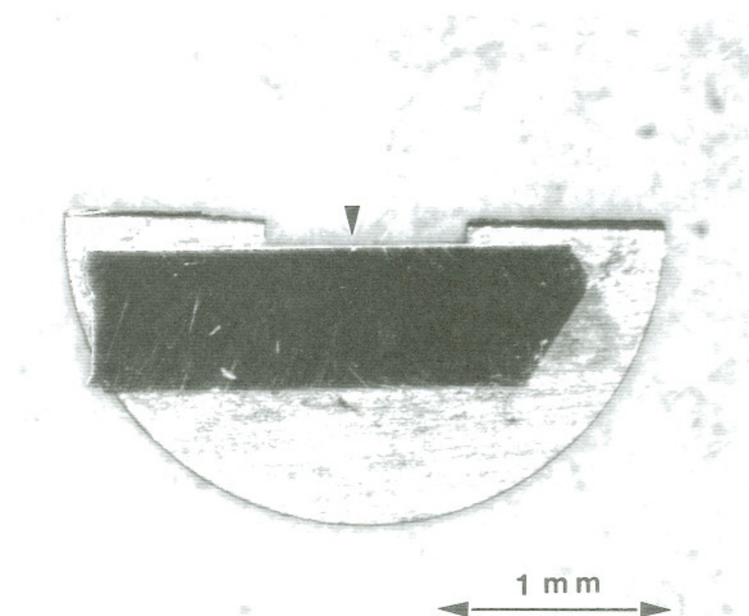


Figure 3. Optical image of FIB produced TEM cross-section. FIB produced canyon small spot at top edge center of Si bar.

The FIB production of TEM transverse cross-sections proved best for specimens with a metallization. The as deposited and heat treated oxide TEM cross-sections were produced by conventional ion milling. The deposition of the Pt bar is an energetic reaction producing heat, oxygen and hydrogen which can and do cause unwanted changes at and near the surface of the substrate. This reaction zone was 10nm. This would involve the entire 7nm of SiO_2, the interface and some of the substrate.

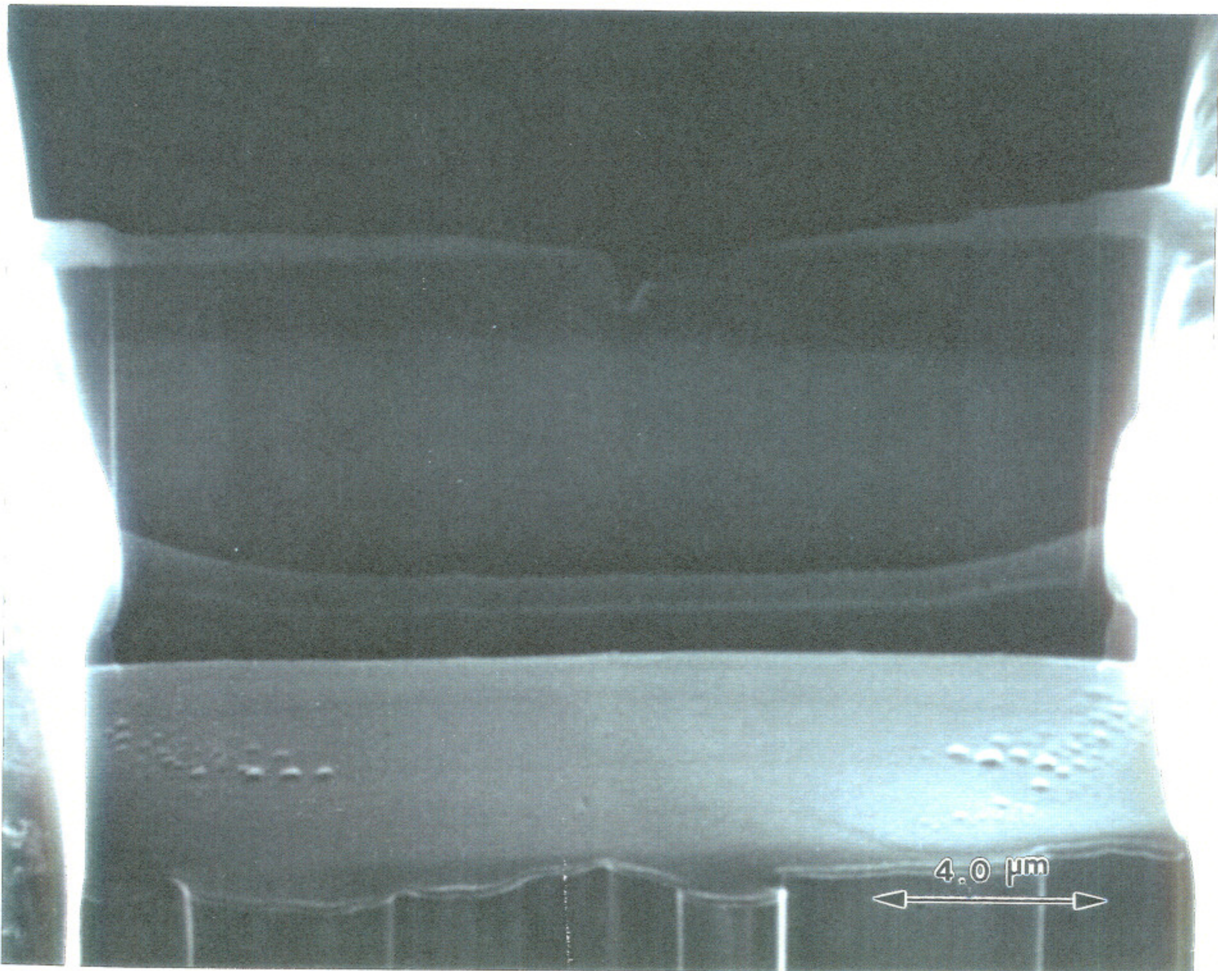


Figure 4. SEM image of FIB produced electron transparent cross section of the metal-oxide-Si substrate (MOS) device.

Specimens where it was important to preserve the experiment produced microstructure at the surface were sputter deposited with Au-Pd to protect the specimen during Pt bar deposition. This technique was used to produce specimens from the Al-.5Cu specimens to confirm segregation of Cu to the surface of the electrode.

These extremely thin and damage free cross-sections were then examined in a Hitachi H-800 200kV analytical TEM/STEM equipped with a Be window energy dispersive(EDS) X-ray detector. High resolution lattice images were taken of the interfaces of the SiO_2 with the metallization and the Si substrate(x500k-600k). The roughnesses of these interfaces were measured. Selected area electron diffraction patterns (SAD) were taken from these interface regions to detect new compounds formed by reaction of the metallization with the silica or the Si substrate. Care was taken to place the specimen at the same height in the TEM by setting the objective lens current at the same value and adjusting the height until the foil was in focus for each diffraction pattern. The d-spacings were measured directly from the diffraction pattern negatives and those d-spacings used along with EDS determined chemical composition to search the Electron Diffraction Database(EDD) to determine likely compounds (reaction products). Bright field and dark field TEM images(x100k) were taken to measure metallization thicknesses , grain size and locate reaction products. Compositional profiles were taken to characterize the diffusion of metals into the Si substrate and Si into the metallization. This was accomplished by producing a 30nm spot

with the H-800 in STEM mode which was stopped at intervals on the thin cross-section for 100 seconds of live X-ray collection starting 200nm deep in the Si substrate and stepping out to the front surface of the metallization. The unique geometry of these thin sections required that the FIB produced canyon face the X-ray detector to minimize secondary fluorescence from the bulk of the 30μm thick Si bar and the Ga contaminated walls of the canyon.

In addition to the transverse cross sections planar sections of the Al.5Cu C-V disc heat treated for 4 hrs. at 400ºC and the Al-1Si heat treated for 2hrs were produced to give more complete electron diffraction data. These sections were produced by grinding from the Si substrate side until the specimen was 5μm thick with the as deposited thicknesses of the metallization and SiO_2 preserved. The specimens were then ion milled briefly on the metallization side of the specimen to remove nearly all the metal leaving only material near the SiO_2 interface. The specimens were then completed by ion milling from the Si substrate side until perforations appeared. The planar sections were then examined in the analytical TEM/STEM. Micro-diffraction patterns, X-ray spectra, bright field and dark field images were collected to better characterize the interface over much larger areas in comparison to the areas of interface sampled by a transverse cross-sections. The planar sections also made material near the interface a much larger volume fraction of the foil which intensified weak X-ray peaks and electron diffraction spots produced by segregation and phase changes respectively at and near the interface. The planar sections also made the micro-diffraction of grains in the interfacial reaction

layer larger than the minimum spot possible.

5. RESULTS

BVG measurements where 10% of the MOS devices fail as shown in Table 2 are a good indicator of performance. Al-1Si directly deposited on the silica is a poor performer with before and after heat treatment BVGs of 0.4V and 0.2V for 10% failure, respectively. Al-.5Cu on poly-Si on silica was the best performer with an as deposited BVG of 8.4V and a post heat treatment BVG of 7.7. Cr was the best performer for metals deposited directly on the silica with pre and post heat treatment BVGs of 7.4 and 7.9V. and the only electrode tested that showed an increase in BVG following heat treatment. See Appendix 1 for the complete BVG data set. Pre and post heat treatment microstructures were characterized with analytical electron microscopy which revealed distinct changes including the appearance of new phases, crystalline defects, reduction and increase in the thickness of the gate oxide, interface roughness, lattice parameters and diffusion depths near the gate oxide. The following text, tables, images, electron diffraction patterns and compositional profiles characterize the MOS devices tested and analyzed in this research. Comparisons between electrodes with the lowest BVGs and the highest were made to identify microstructural indicators of good performance. Correlations between BVG changes and changes in microstructure were made. Changes were quantified to predict diffusion depths, determine diffusion coefficients, reaction rates, the thicknesses of electrodes and oxide.

Table 2. BVG Measurements of Metallization Disk Arrays on (100) Si Wafers with 7nm of Silica

	A	B	C	D	E
1	Metallization	Heat Treatment	10% MOS Disk Failure	50% Failure	90% Failure
2		Hours ºC	volt	volts	volts
3					
4	Al-1Si	as deposited	0.4	1.1	1.9
5		2hrs @ 400ºC	0.2	0.6	0.7
6					
7	Al-1Si/Poly Si	as deposited	7.7	7.8	8
8		2hrs @ 400ºC	7.6	7.7	7.8
9					
10	Al-Cu/Poly Si	as deposited	8.4	9.4	12.7
11		2hrs @ 400ºC	7.7	7.9	12.3
12					
13	Cr	as deposited	7.4	7.5	7.6
14		2hrs @ 400ºC	7.9	8	16.2
15					
16	Ti	as deposited	6.6	6.6	6.7
17		2hrs @ 400ºC	0.2	0.2	0.2

Control-SiO_2 as Deposited on (100)Si

Electron transparent transverse cross section and planar section of the TCA SiO_2 on (100) Si were produced for examination in the TEM to record it's microstructure before metallization and heat treatment. The transverse cross section revealed a 7nm amorphous silica layer with a roughness of 0.22 to .65nm amplitude and a frequency of 17/100nm. The ion milled planar section did not show pores or preferential milling and did not confirm earlier TEM work by Irene on chemically etched planar sections of SiO_2 which revealed 1nm pores or holes. See figure 5.

Figure 5a. TEM atomic resolution image of SiO_2 as deposited, planar section.

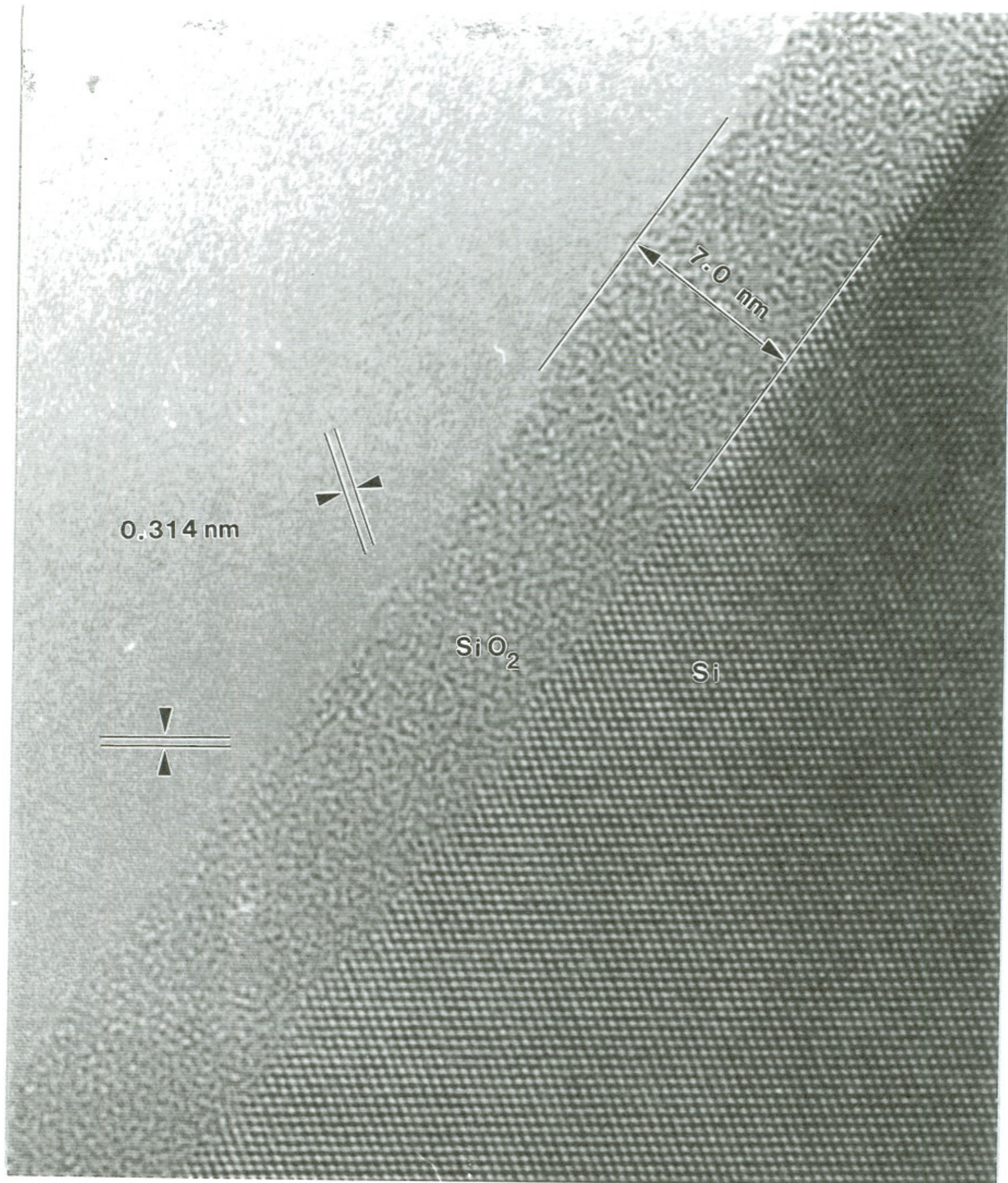


Figure 5b. SiO_2 as deposited TEM atomic resolution image, transverse cross-section.

<u>SiO_2 Heat Treated for 2 hours at 400ºC in N_2</u>

There was an increase in thickness from 7nm to 15nm due to oxidation or nitridation of the original silica. Sources of the oxygen could be impure N_2 or the Si substrate. Again there was no evidence of pores or regions of high milling rates in the ion milled planar sections. See figure 6.

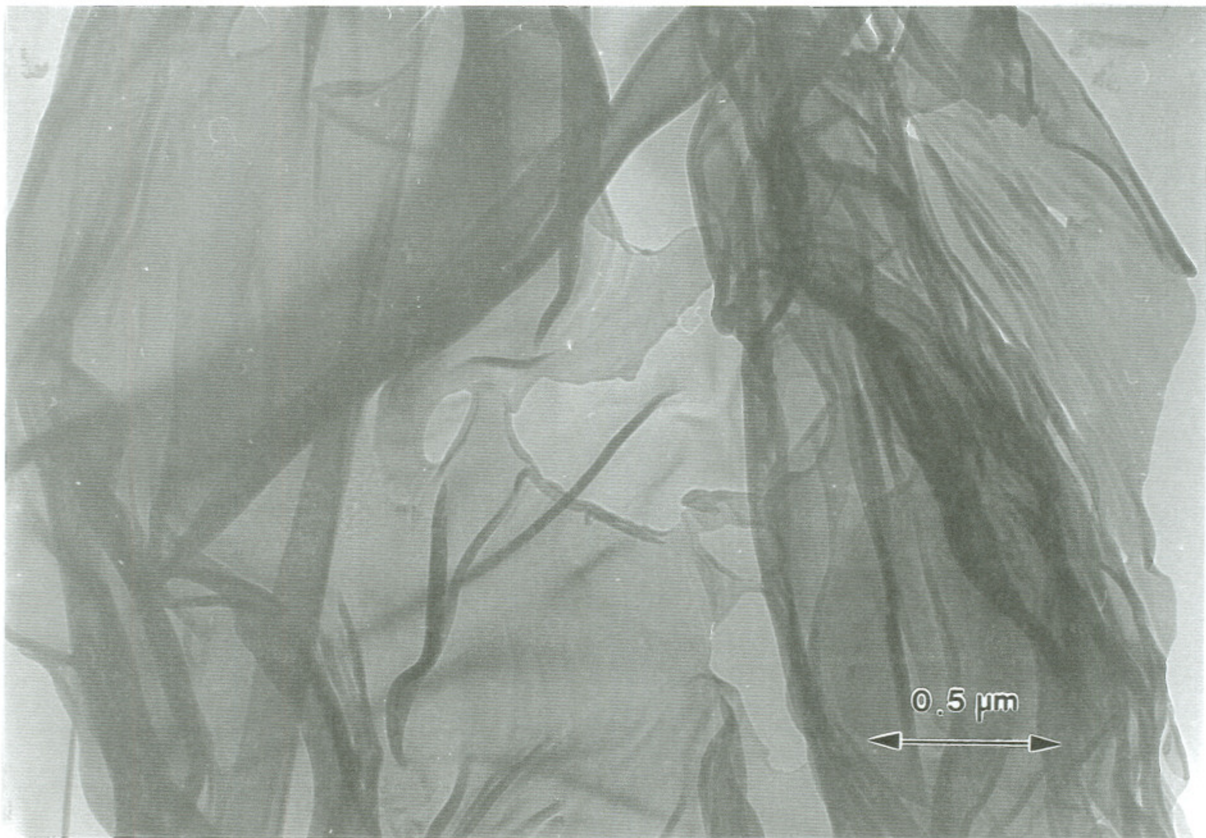


Figure 6a. TEM bright field image of planar section of SiO_2 heat treated for 2hrs. at 400ºC.

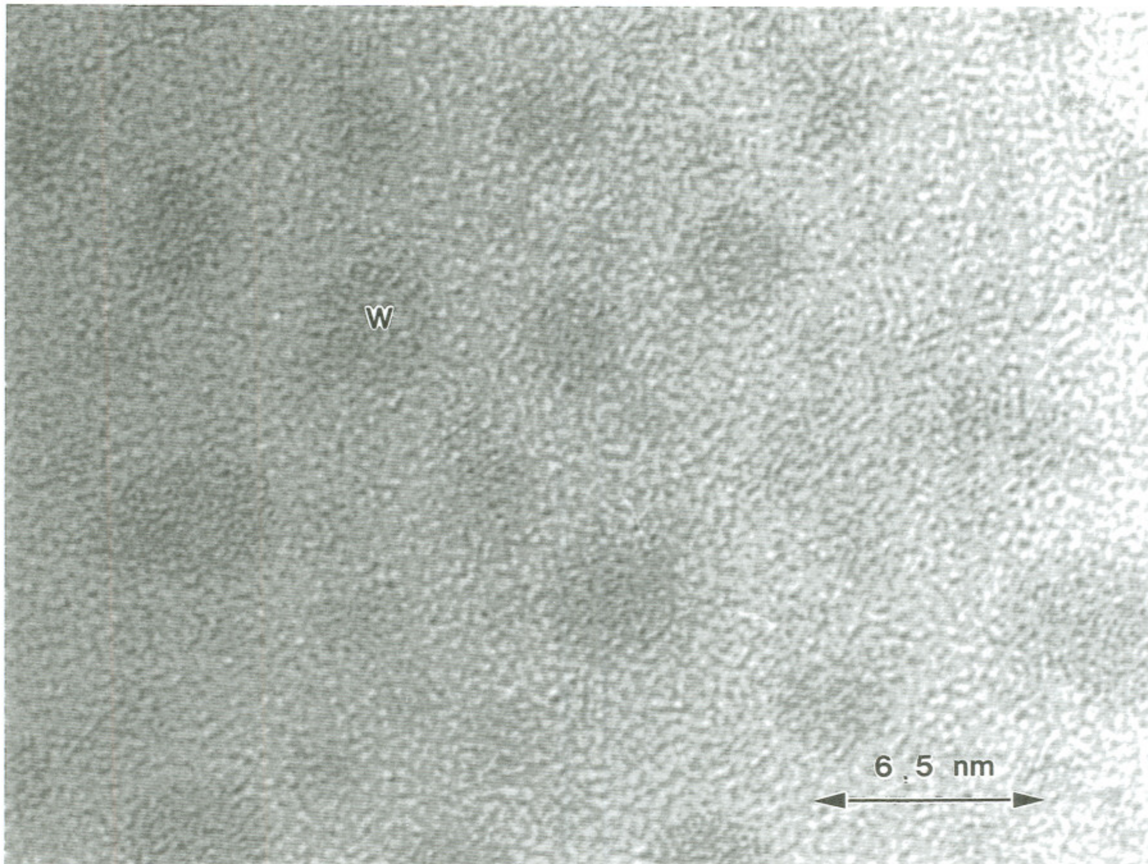


Figure 6b. Atomic resolution image of planar section of SiO_2 heat treated for 2hrs. at 400ºC and then decorated with W islands by sputtering.

Al-1Si on SiO_2 as Deposited

Selected area electron diffraction of the Al, SiO_2 and Si substrate identified Al, Al_2SiO_5 and single crystal Si to be present. The Al_2SiO_5 diffraction spots were very weak indicating a small volume fraction present. The thickness of the electrode was 90nm. The grain size was 73nm. The SiO_2 thickness was 8nm. The Si/SiO_2 reaction layer was 1 to 1.5nm thick. See figure 7.

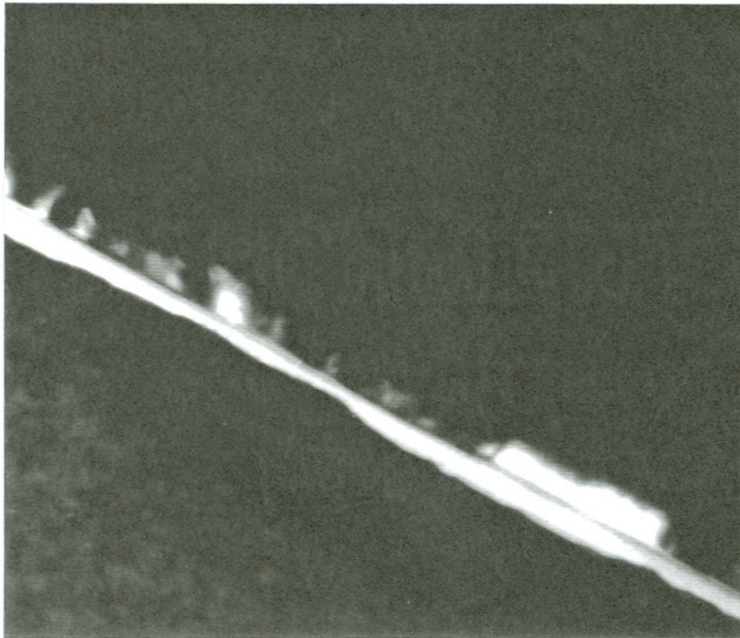


Figure 7. TEM bright field image of as deposited Al-1Si with diffraction pattern of region of $Al/SiO_2/Si$ interfaces.

Al-1Si on SiO_2, Heat Treated for 2 hours at 400ºC in N_2

Following heat treatment the Al_2SiO_5 spots became stronger and dark field images from these spots were possible. Most precipitation occurred on the Al side of the oxide to a depth of 20nm. The reaction zone on the Si side of oxide was 5-10nm thick. The reaction zone on the Al side of the oxide was 0.66nm. The step heights had a range of 0.33 to 1.49nm, average 0.6nm and a frequency of 30/100nm. The oxide thickness decreased to 6.6nm. The diffusion depth of the Si in the Al, the depth at which the Si wt% is 50, $(Dt)^{1/2}$, was 40nm. The electrode increased to a thickness of 210nm due to the diffusion of Si through the SiO_2. The oxide at the Al/SiO_2 interface roughened below Al grain boundaries increasing the thickness of the oxide by 0.5nm and the reaction zone by 1.1nm at those sites. Grain size was measured to be 214nm. A planar section of the failed oxide revealed nanocrystalline quartz within the originally completely amorphous gate oxide heat treated with the Al-1Si as shown in figure 8.

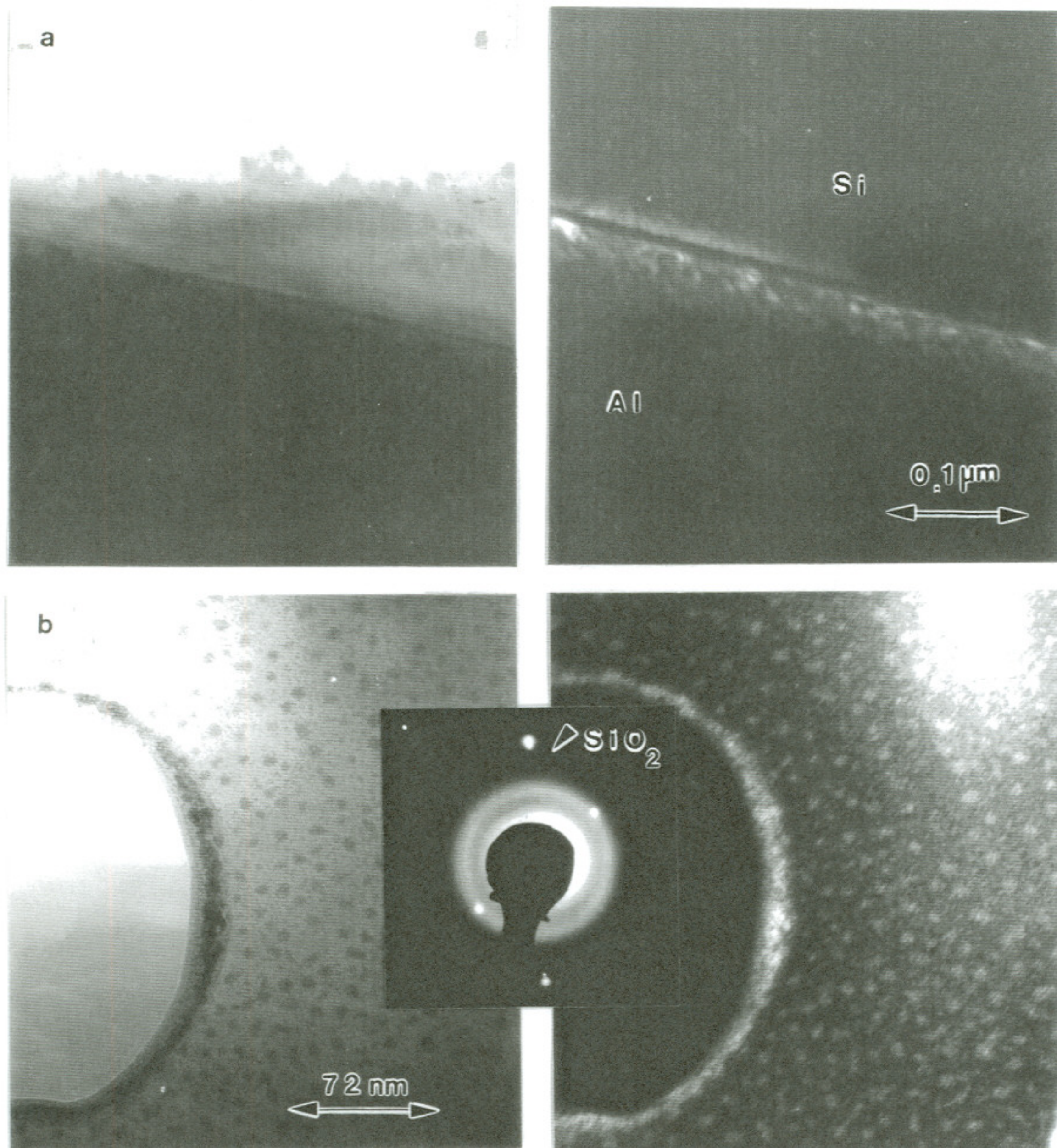


Figure 8a. TEM bright field and dark field of Al-1Si heat treated for 2hrs. at 400ºC, transverse cross section. b) TEM bright field and dark field image and diffraction pattern of nano-crystalline high quartz in failed oxide, planar section.

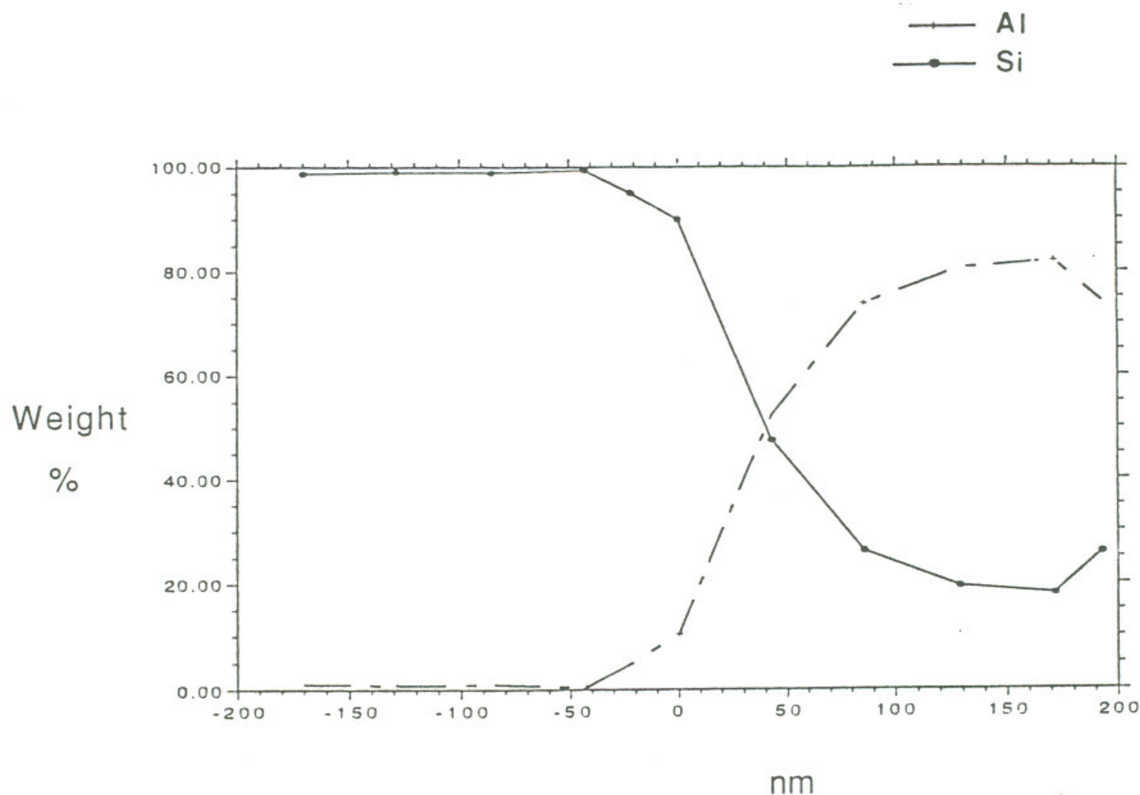


Figure 8c. Al-1Si, 2hrs at 400ºC in N_2 , compositional profile, SiO_2 interfaces at 0 and Si substrate is negative x, Al is positive x.

Al-1Si on SiO_2, Heat Treated for 12 hours at 400ºC in N_2 with Furnace Cool

This heat treatment caused significant changes in the Al electrode. The Al-1Si electrode grew to 810nm in thickness. The high volume of Si diffusion through the oxide in addition to increasing the electrode thickness caused a poly-Si layer to grow at

the electrode surface 25 to 35nm thick. The extended heat treatment increased the grain size to 1200nm. The oxide was not consumed in this process and maintained a 6nm thickness with a 1.2 nm reaction layer at the Al-1Si/SiO_2 interface. The reaction layer at the SiO_2/Si interface was 0.8nm. In addition to the Al and Si strong matrix spots in the selected area diffraction patterns, there were also faint spots indicating the presence of Si precipitates in the Al matrix and Al or Al_2SiO_5 precipitates at the SiO_2/Si interface. The diffusion distance for this heat treatment was near 0. See figure 9c.

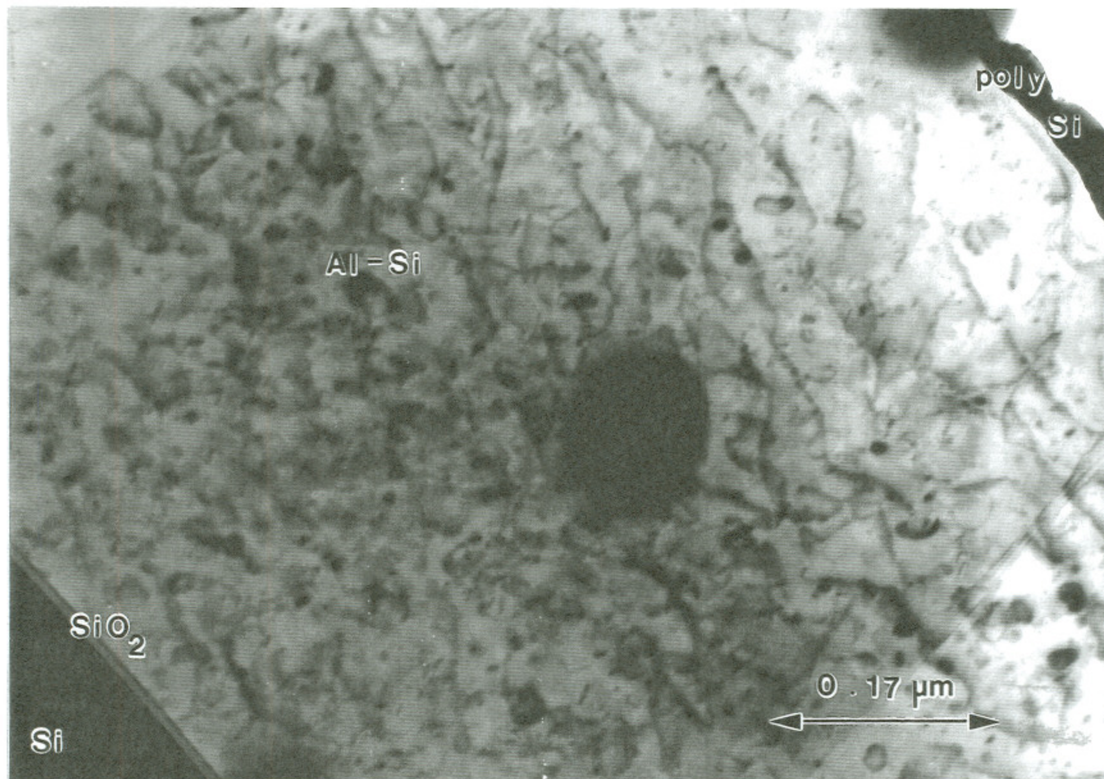
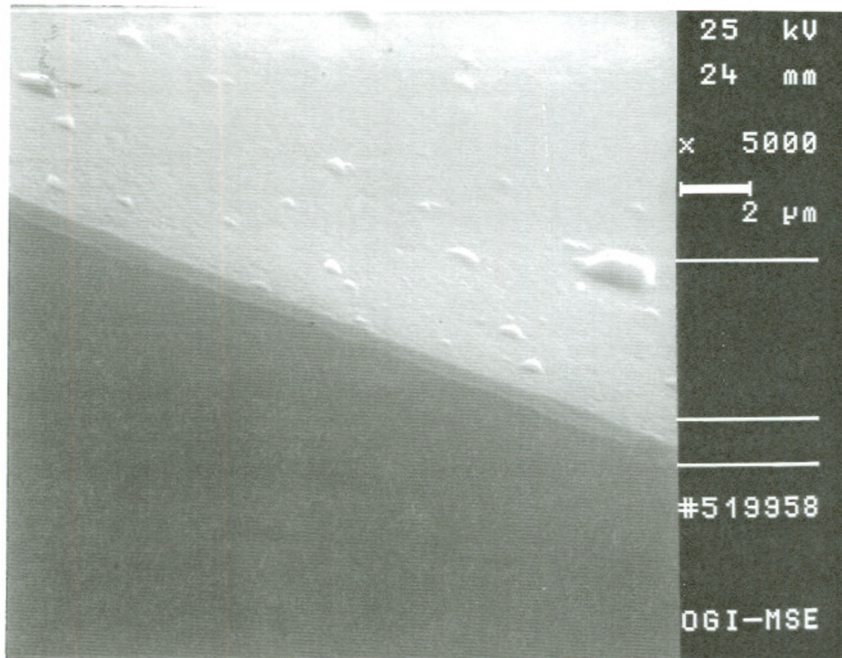


Figure 9a. Bright field TEM image of Si, SiO_2, Si diffusion enlarged electrode and poly-Si on the Al-1Si electrode surface, heat treated for 12hrs. at 400ºC.



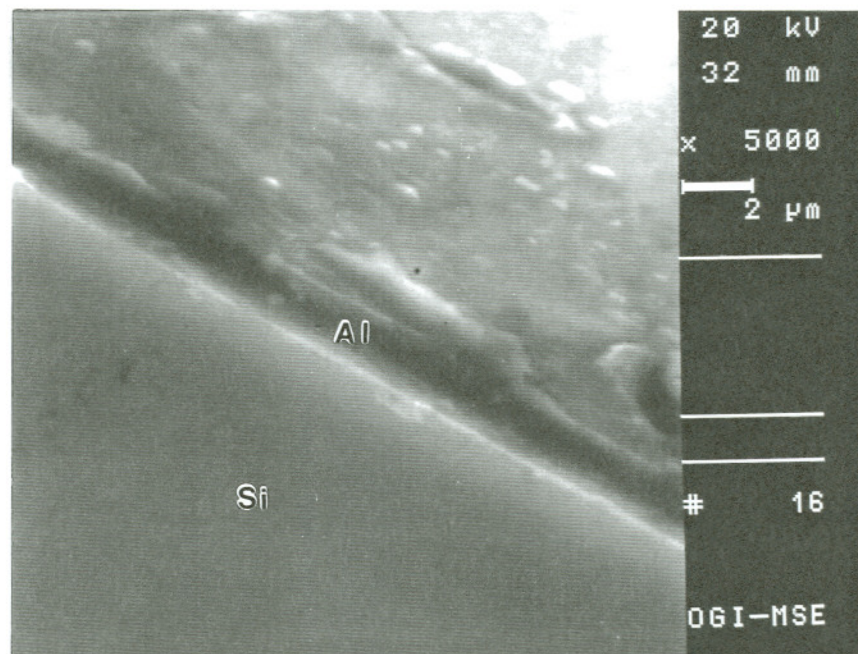


Figure 9b. SEM of cleaved Al-1Si C-V spots as deposited and heat treated for 12hrs. at 400ºC.

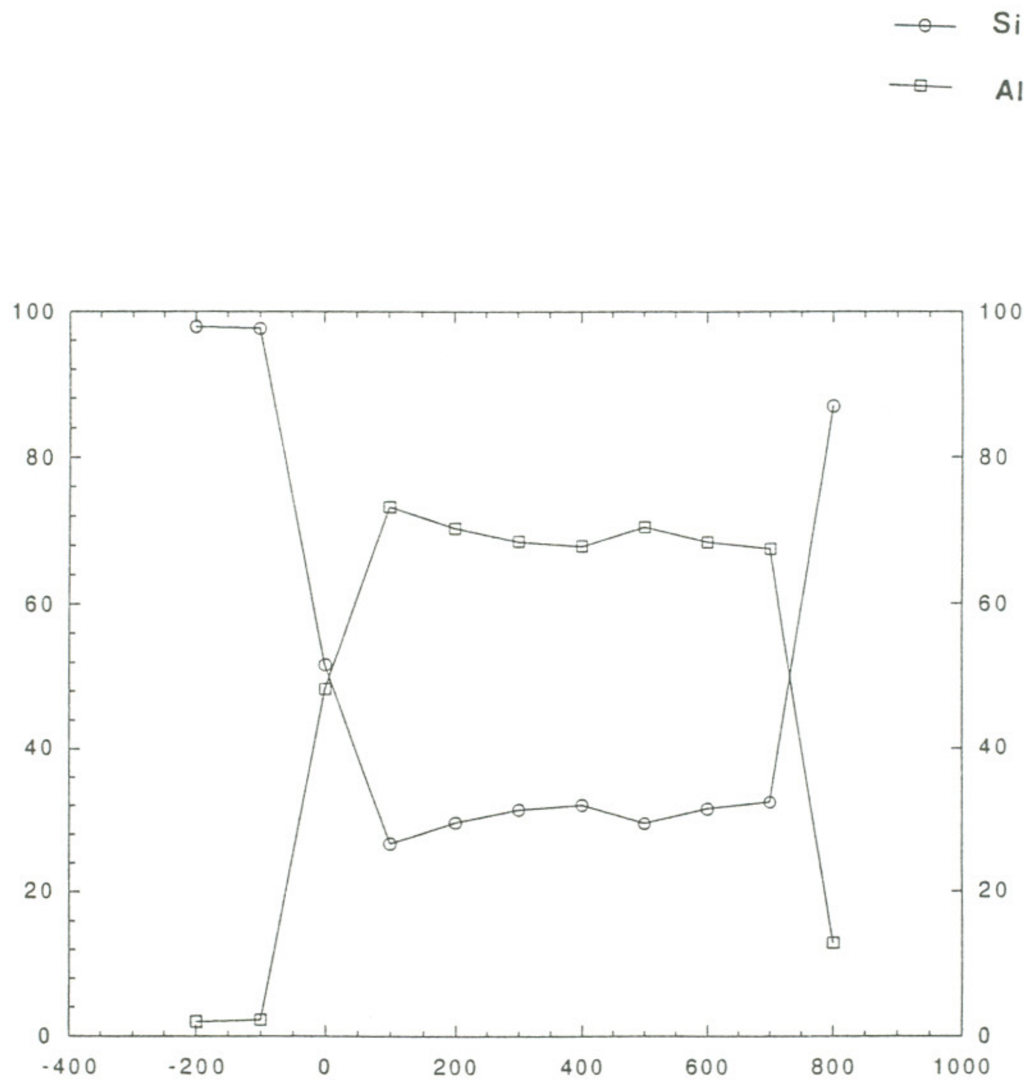
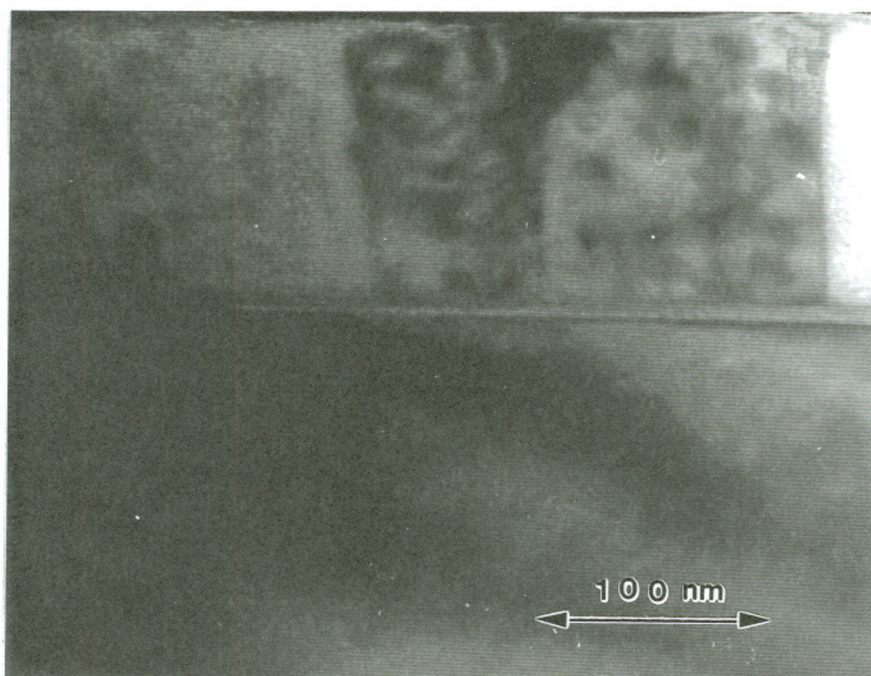


Figure 9c. Compositional profile for Al-1Si heat treated for 12hrs at 400ºC in N_2

Al-.5Cu on SiO_2, as Deposited

The oxide thickness as measured from TEM bright field images was 6nm. The diffraction patterns contained only Al and Si spots with the Al d_{111} increased by 0.006nm due to the internal stresses in the sputtered Al thin film. An annealed specimen Al-1Si heat treated for 12hrs. does not show this increase in d_{111}. There is no evidence of reaction layers at the SiO_2/Si or Al-.5Cu/SiO_2 interfaces. The wt% Si and Al profiles for this electrode show little diffusion of Al into the Si and limited diffusion of Si into the Al-.5Cu which reached between 9 and 11wt% within the electrode and 15 wt% at the surface. There was no segregation of Cu to the SiO_2 interfaces. The as deposited electrode thickness as measured from a TEM bright field image was 95nm. Grain size was 162nm. See figure 10.



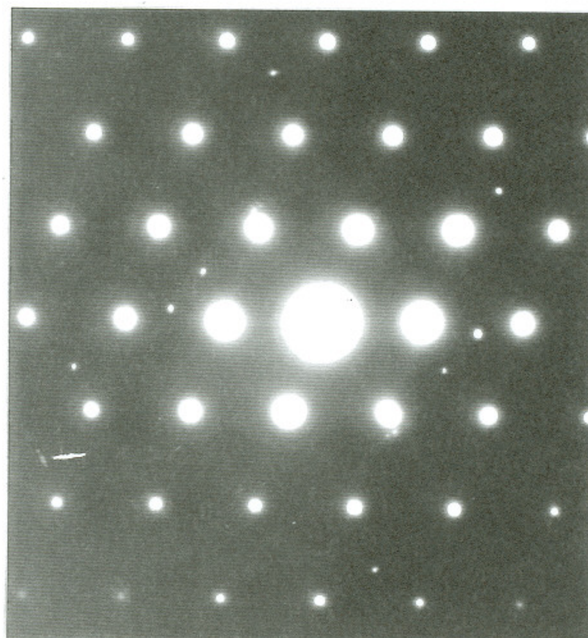


Figure 10a. TEM bright field image of interfacial region of Al-.5Cu as deposited and diffraction pattern.

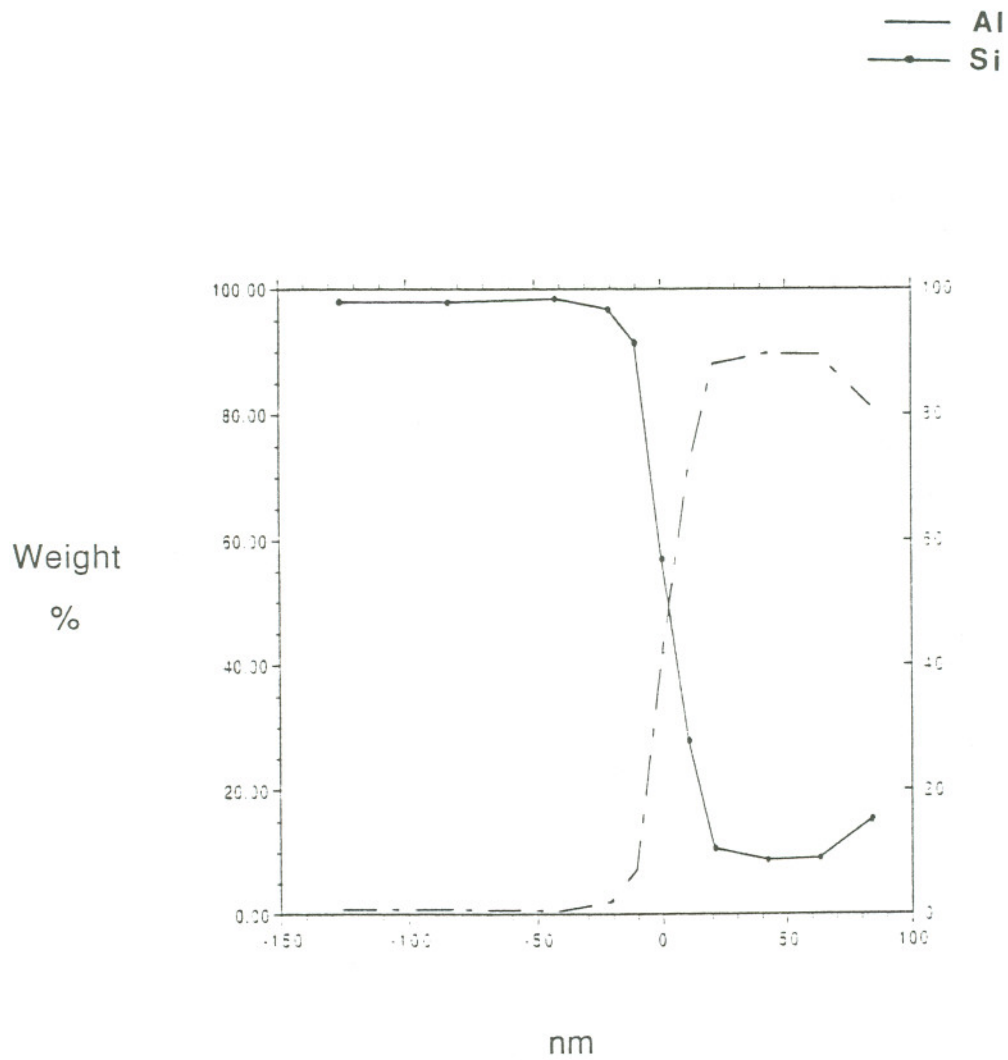
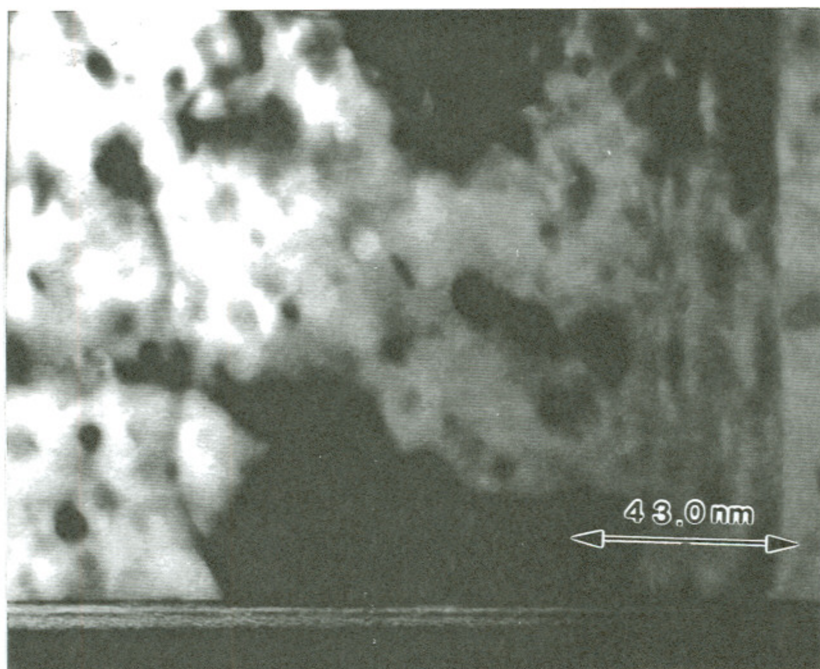


Figure 10b. Al-.5Cu as deposited compositional profile.

<u>Al-.5Cu on SiO_2, Heat Treated for 2 hours at 400ºC in N_2</u>

The oxide thickness was 6nm following heat treatment. The interfaces remained relatively flat, SiO_2/Si with step heights of 0.4 to 0.6nm and a frequency of 12.5/100nm. A 0.6nm reaction layer was present on both of the oxide interfaces. The electron diffraction patterns showed evidence of an ordered phase at the interfaces with a repeat distance of 6.38nm. There was also segregation of Cu to the SiO_2 and its interfaces. Cu segregation to the front surface was also detected. Si wt% within the electrode was 11 to 12 and rose to 24 at the top surface of the electrode. The electrode increased in thickness to 110nm. The grains grew to 370nm. See figure 11.



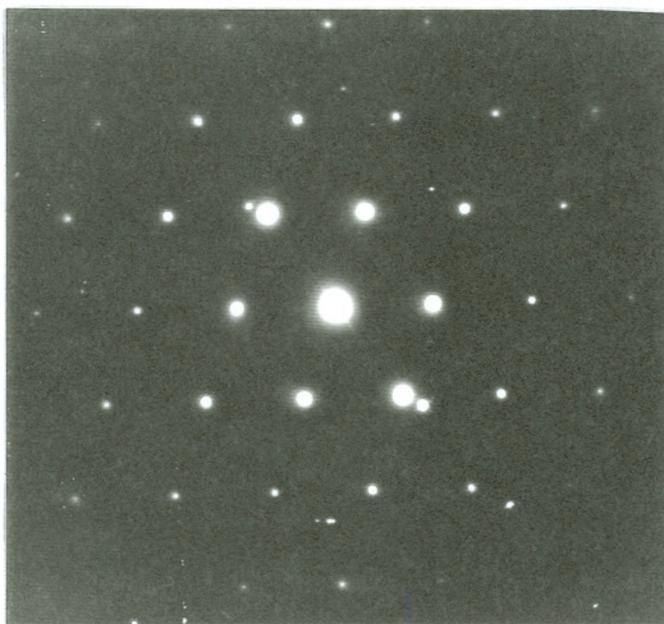


Figure 11a. TEM bright field image and diffraction pattern for Al-.5Cu heat treated for 2hrs. at 400ºC in N_2.

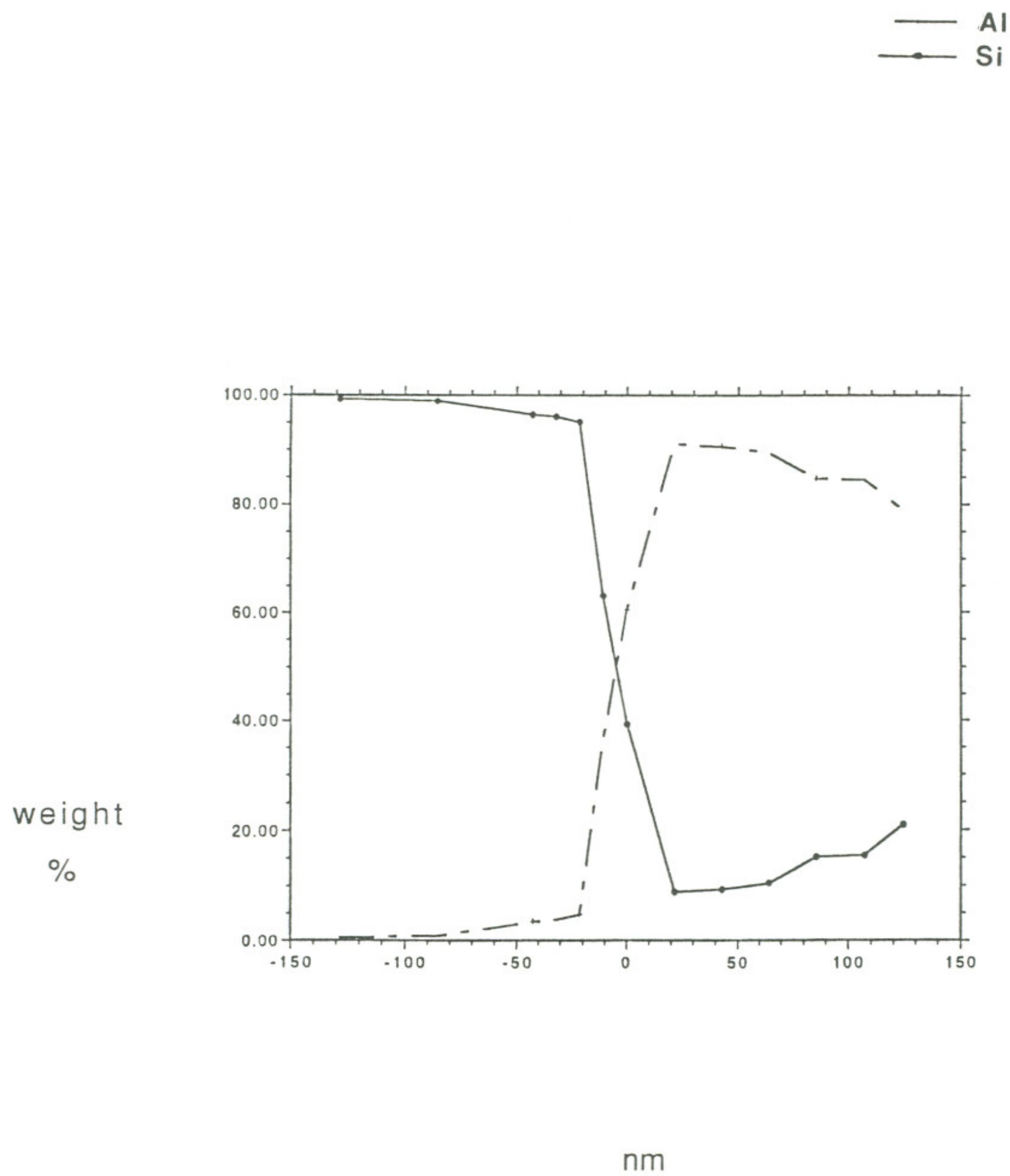
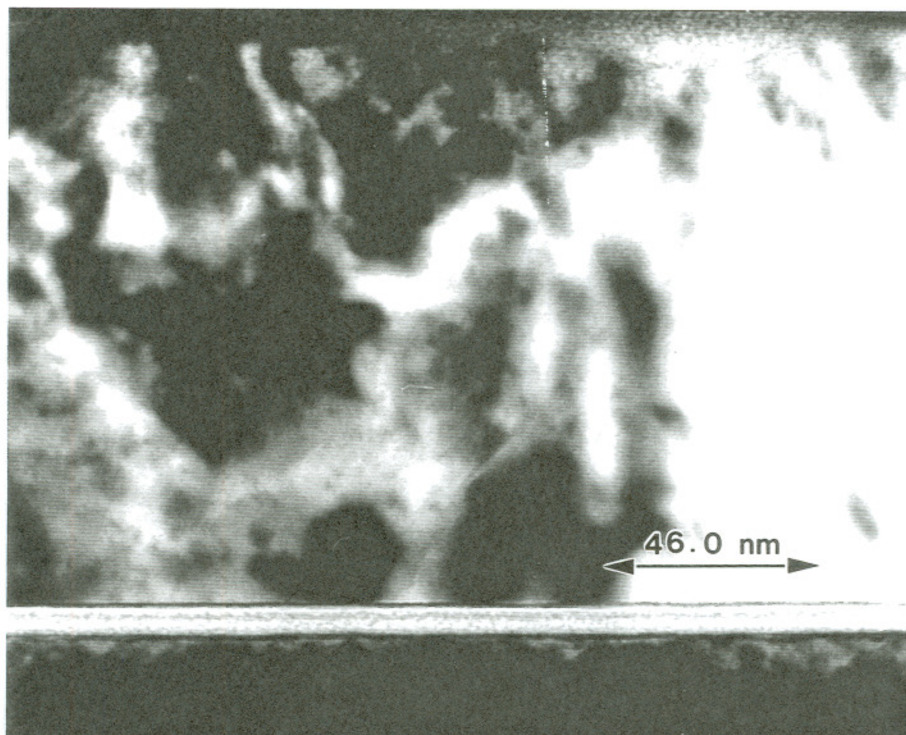


Figure 11b. Compositional profile for Al-.5Cu heat treated for 2hrs at 400ºC in N_2.

Al-.5Cu on SiO_2, Heat Treated for 4 Hours at 400ºC in N_2

Post heat treatment oxide thickness was 7.2nm. The SiO_2 interfaces show well defined reaction layers approximately 0.8nm thick. The step heights of the interface of the oxide with the reaction layer and the reaction layer with the Si substrate measured 0.2 to 0.4nm with a frequency of 5.55/100nm. There were also relatively low frequency steps of 0.8nm with a wavelength of 200nm. The reaction layer interfaces with the oxide and the Al-.5Cu had a maximum step height of 0.2nm and a frequency of 3/100nm. These interfaces with the metal were nearly atomically flat. Large steps at grain boundaries were not found. Examination of the TEM image at 4000x did not show any large scale roughness. See figures. The selected area electron diffraction patterns extra spots indicated that monoclinic $AlCu_3$, space group 10 or cubic Cu_5Si, space group 212 at the interfaces. Cu segregation was detected at the interfaces. The diffusion distance for Si into the Al-.5Cu was 15nm. See figures. Si content in the center of the electrode reached 25wt% and at the top surface 55wt%. The electrode thickness remained nearly unchanged at 135nm. Grain size increased to 650nm. See figure 12.



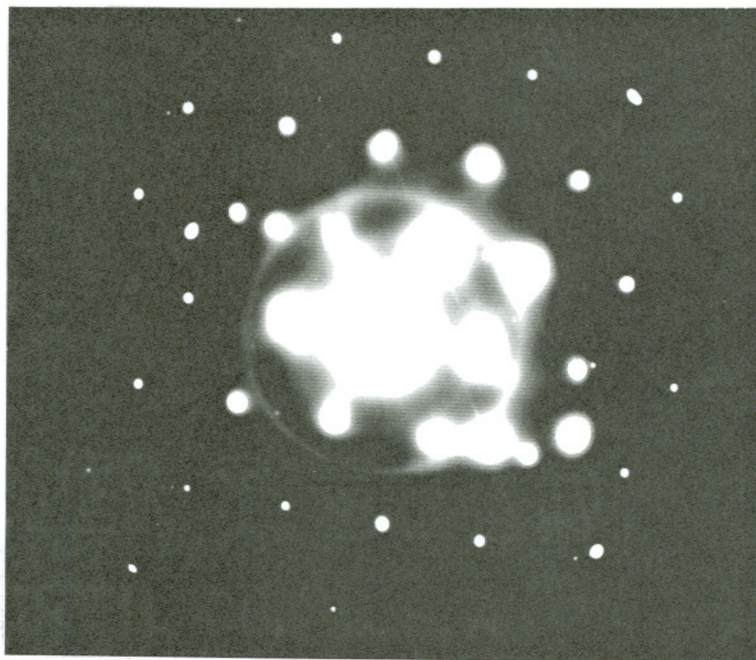


Figure 12a. TEM bright field image and diffraction pattern for Al-.5Cu heat treated at 400ºC for 4hrs in N_2.

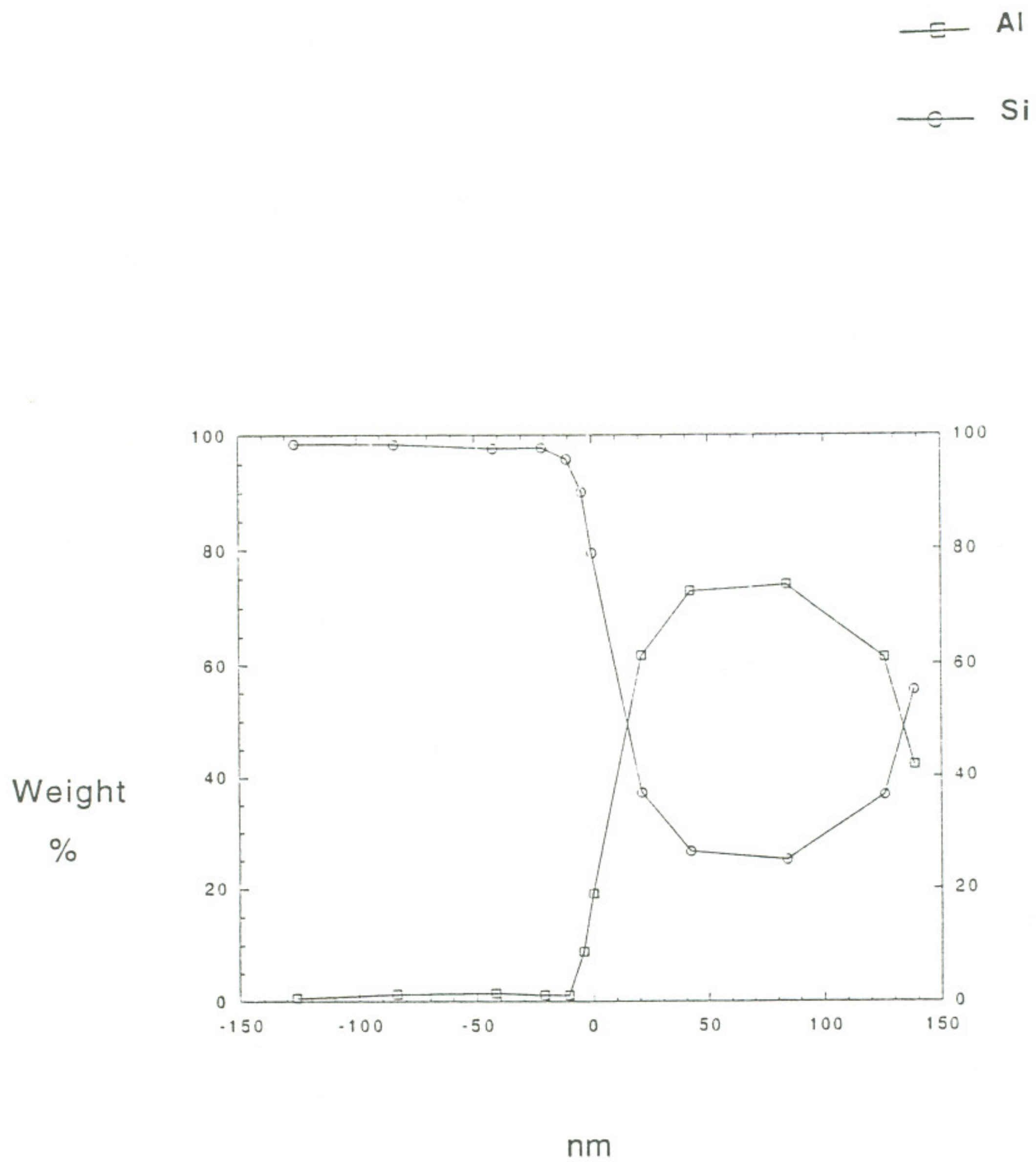


Figure 12b. Compositional profile for Al-.5Cu heat treated for 4hrs at 400ºC.

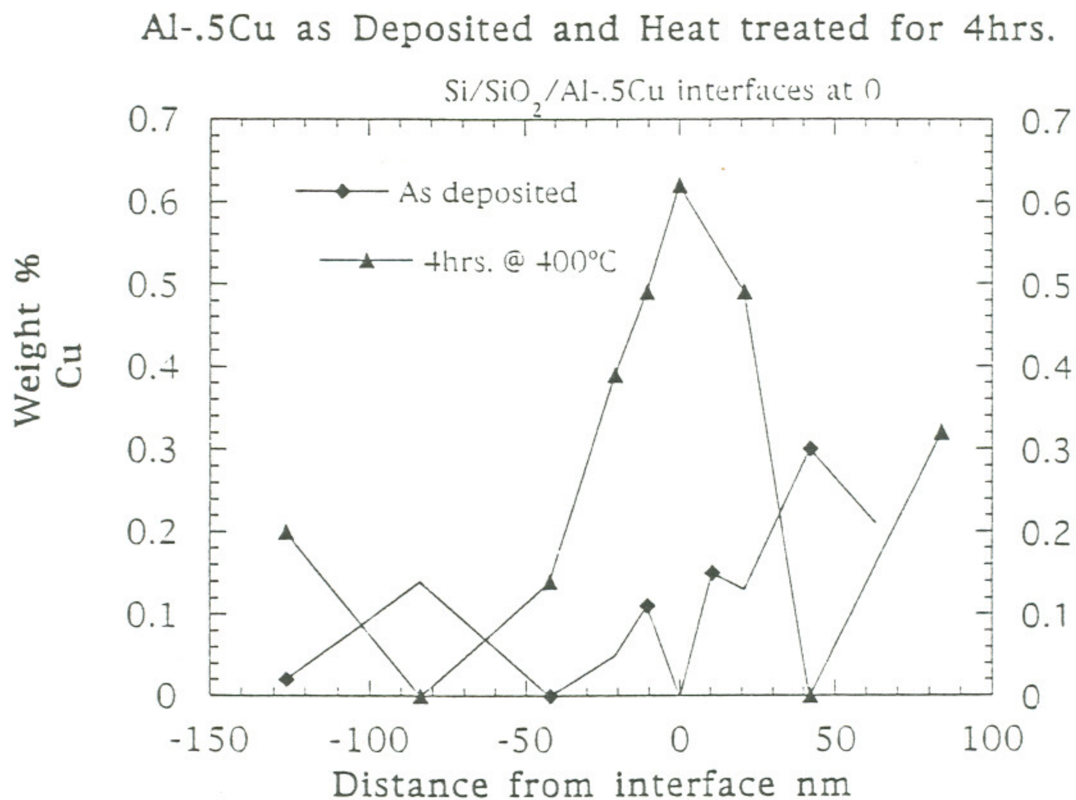


Figure 12c. Cu segregation in the Al-.5Cu electrode heat treated for 4 hours compared with an as deposited electrode without heat treatment.

In addition to a transverse cross section of this heat treated MOS structure a planar section was produced of oxide, adjacent electrode and Si substrate. A variety of electron transparent areas could be examined; entire MOS stack, SiO_2 and Si; just oxide; or metal on oxide no Si. This planar section also included areas with just the Al-Cu intermetallic reaction layer on SiO_2.

Micro-diffraction patterns produced by this planar section were collected from the reaction layers that were imaged in the transverse cross-section. See figure 12. The micro-diffraction patterns provide a more positive identification of the interfacial layers. See the diffraction pattern for one grain in figure 13a which was identified as a <311> zone for Al_2Cu and computer generated pattern for this tetragonal structure, space group 140. Grains of Monoclinic $AlCu_3$ space group 10 and AlCu space group 12 were also identified.

The dark field work on the grain in figure 13 suggests that the Intermetallic layer is on the Si side of the SiO_2. The bright field TEM image in figure 13b shows a portion of an Al grain on oxide over Si substrate. The remainder of the grain is over only SiO_2. The boundary between the two portions of the grain is marked by the last Si thickness fringe. Dark field images of the Al-Cu intermetallic at the interface in figure 13b show that the intermetallic is only present where the Si substrate is present.

The ion milled planar section also provided an opportunity to compare oxide heat treated in the presence of the metal electrode with similarly produced planar sections of as deposited oxide and

heat treated oxide. The as deposited and heat treated oxide ion milled evenly with no preferential removal but the oxide heat treated with the electrode present showed a grain like structure preferentially milled at "grain boundaries". The oxide in all cases as determined by electron diffraction was amorphous. See figure 13c. The average grain size of the "grains" in the oxide is the same as the as deposited Al grains(150-200nm). The grains in the heat treated electrode are much larger. X-ray microanalysis of sections of the planar section that were completely amorphous in its thinnest regions had as high as 33.3 wt% Cu and 27wt% Al. Al grain size of 532nm following this heat treatment measured from this planar section was comparable to the 650nm measured from images of the transverse cross section.

A focused ion beam milling workstation equipped with a SIMS produced a depth profile of the Al-.5Cu MOS device heat treated for 4hrs. The SIMS depth profile shown in figure 13d. shows increased Cu at the surface of the electrode and at the silica confirming X-ray microanalysis detected Cu segregation. This depth profile had much greater depth and lateral resolution due the slow sputtering rate and small spot size. The milling of the 135nm thick metallization took 40 minutes.

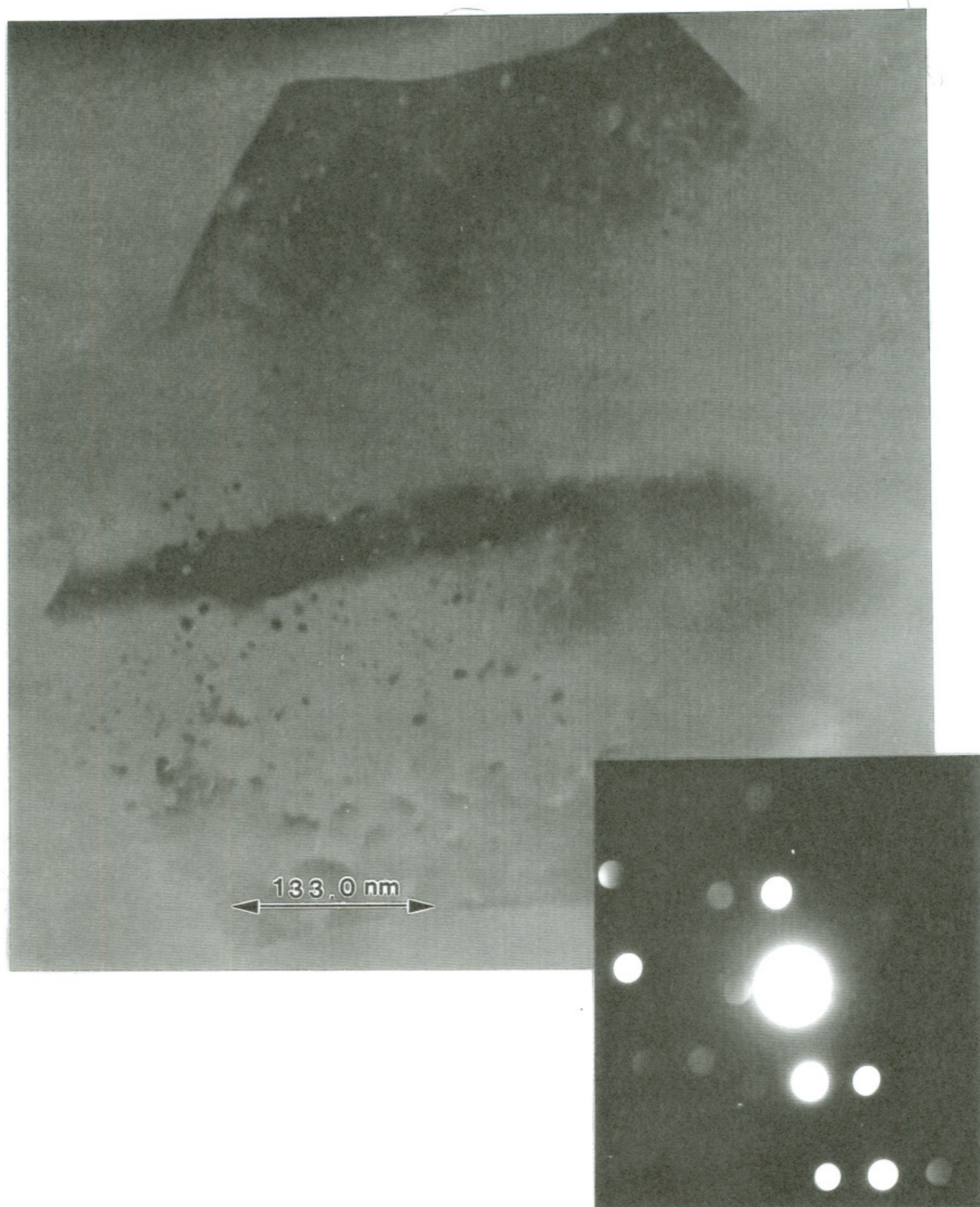


Figure 13a. TEM bright field image of planar section of Al-.5Cu heat treated for 4hrs., showing partially removed Al grain on SiO_2 and center band of Al_2Cu with microdiffraction from this intermetallic.

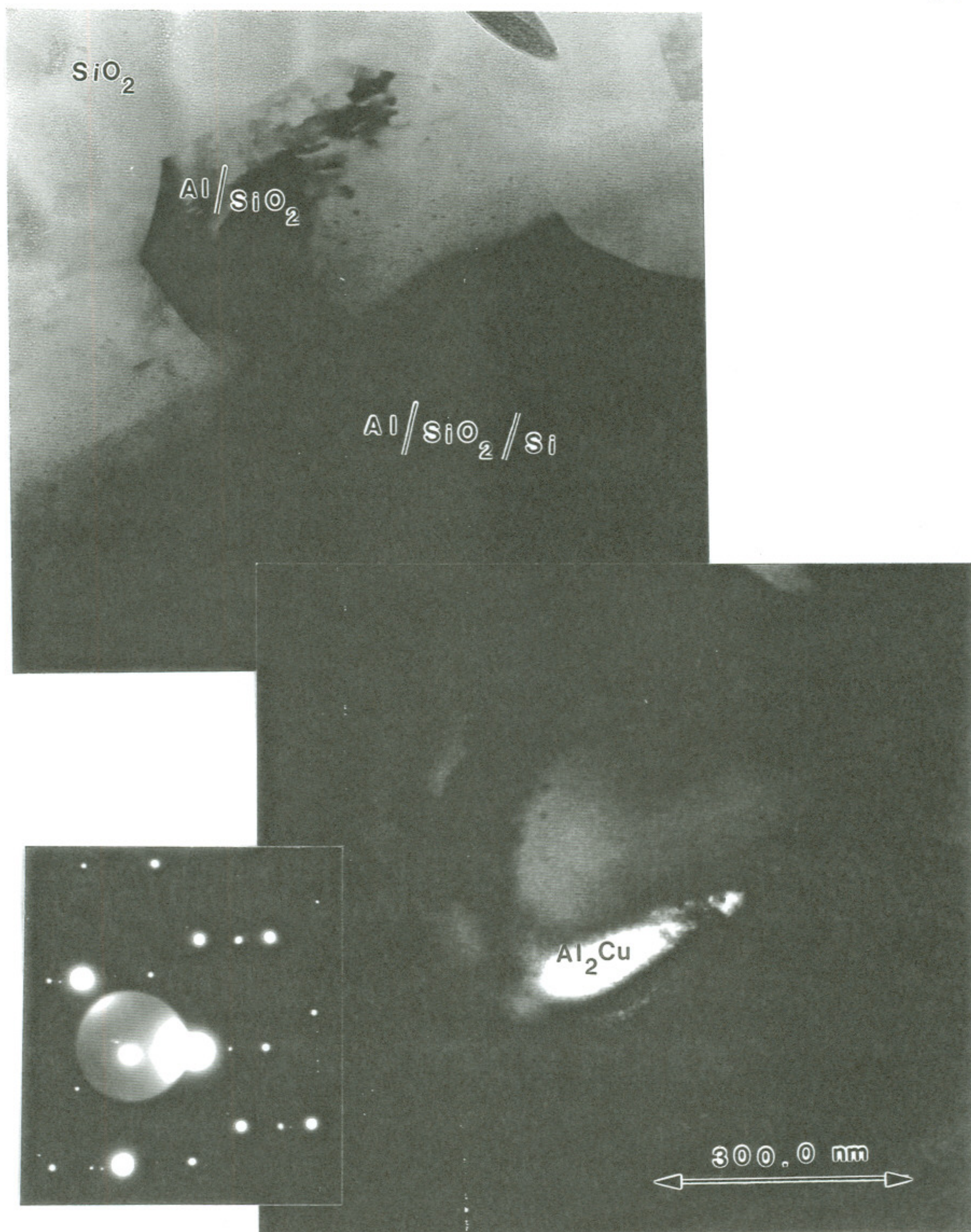


Figure 13b. TEM bright field and dark field images and selected area electron diffraction patterns with overexposed dark field Al_2Cu spot produced by the Al-.5Cu electrode heat treated for 4 hours.

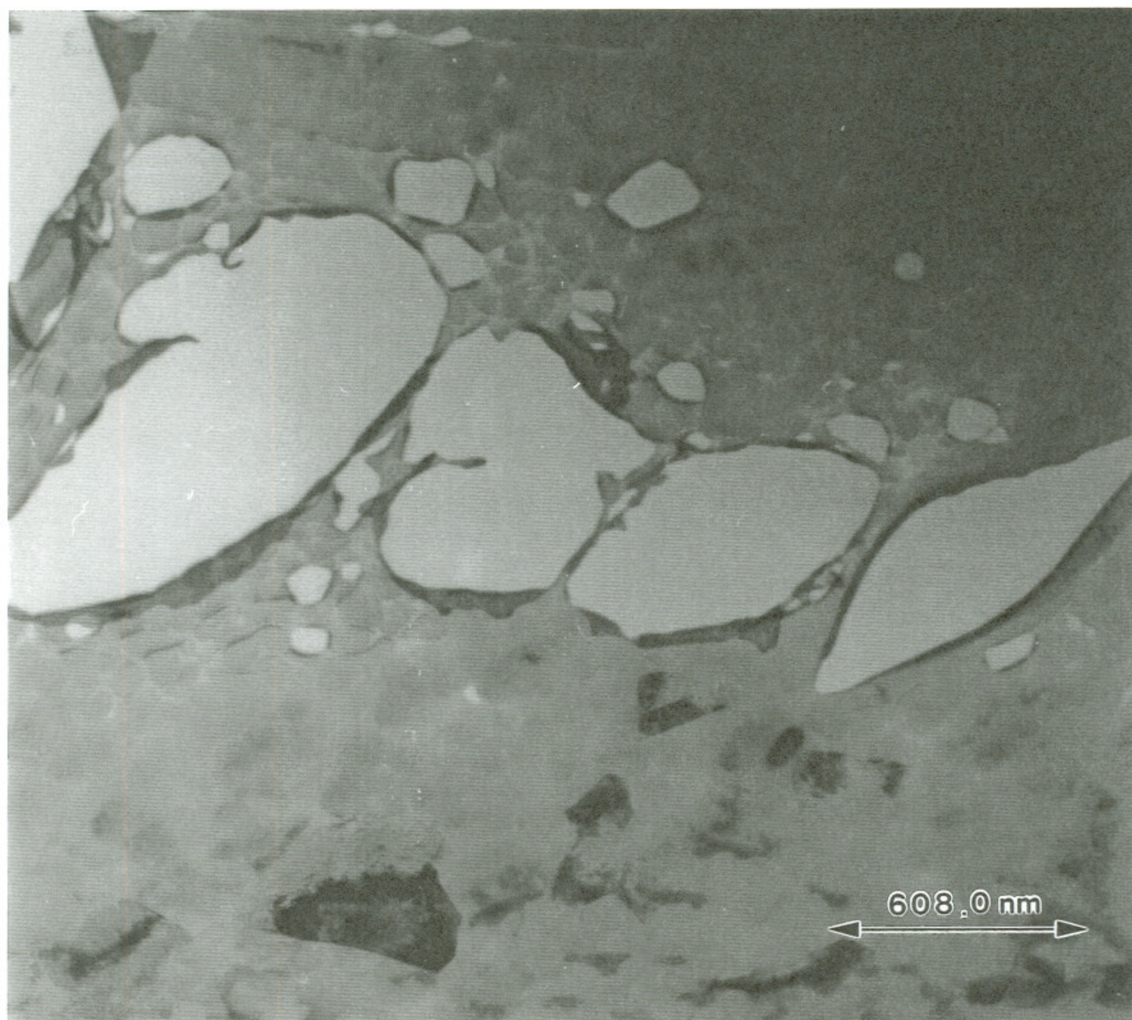


Figure 13c. Planar section of the oxide showing grain-like structures and electron diffraction produced by the oxide.

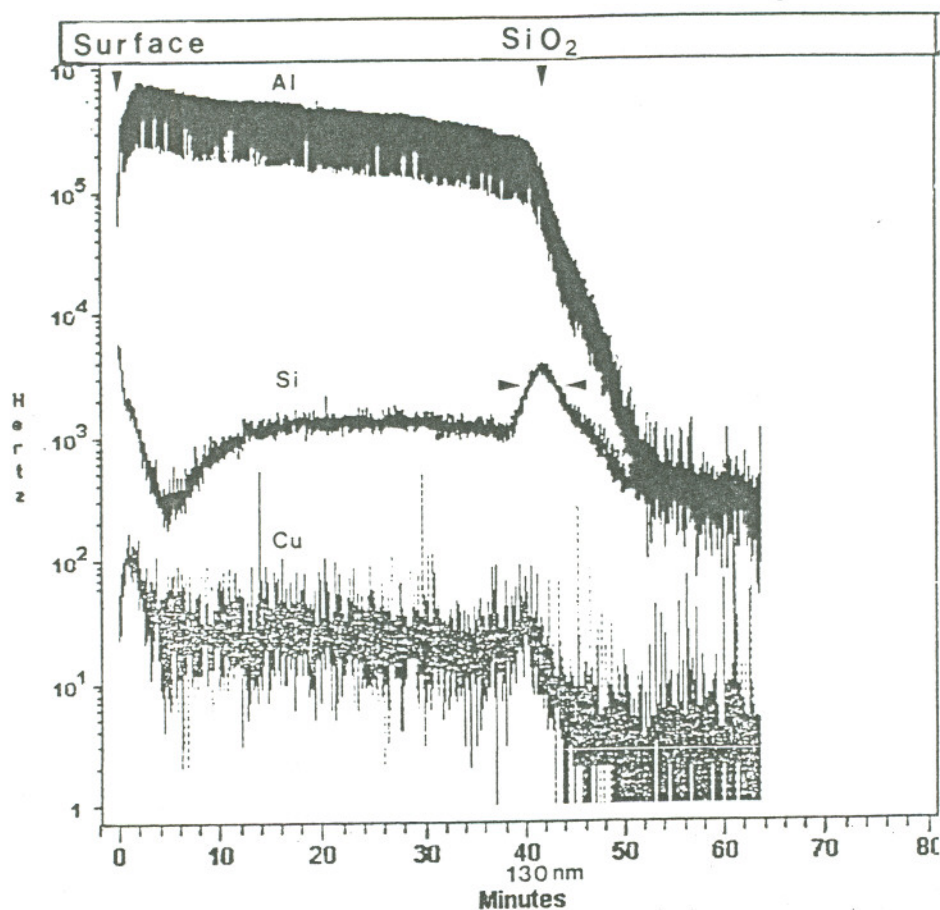


Figure 13d. FIB produced SIMS profile of Al-.5Cu heat treated for 4hrs at 400ºC in N_2

Al-.5Cu on SiO_2, Heat Treated for 11.25 Hours at 400ºC in N_2

The post heat treatment oxide thickness was 5.0nm. Reaction layer thickness increased to 1nm. Step height was 0.2 to 0.6nm with a frequency of 15/100nm. The selected area electron diffraction pattern contained weak spots that matched orthorhombic $AlCu_3$ space group 59 in addition to the strong spots produced by Al and Si. The diffusion distance of Si in the electrode increased to 9nm. At

the center of the electrode the Si content reached 20wt%. Segregation of Cu was detected at the SiO_2 and its interfaces. The electrode thickness remained nearly unchanged at 133nm with a grain size of 360nm. See figure 14.

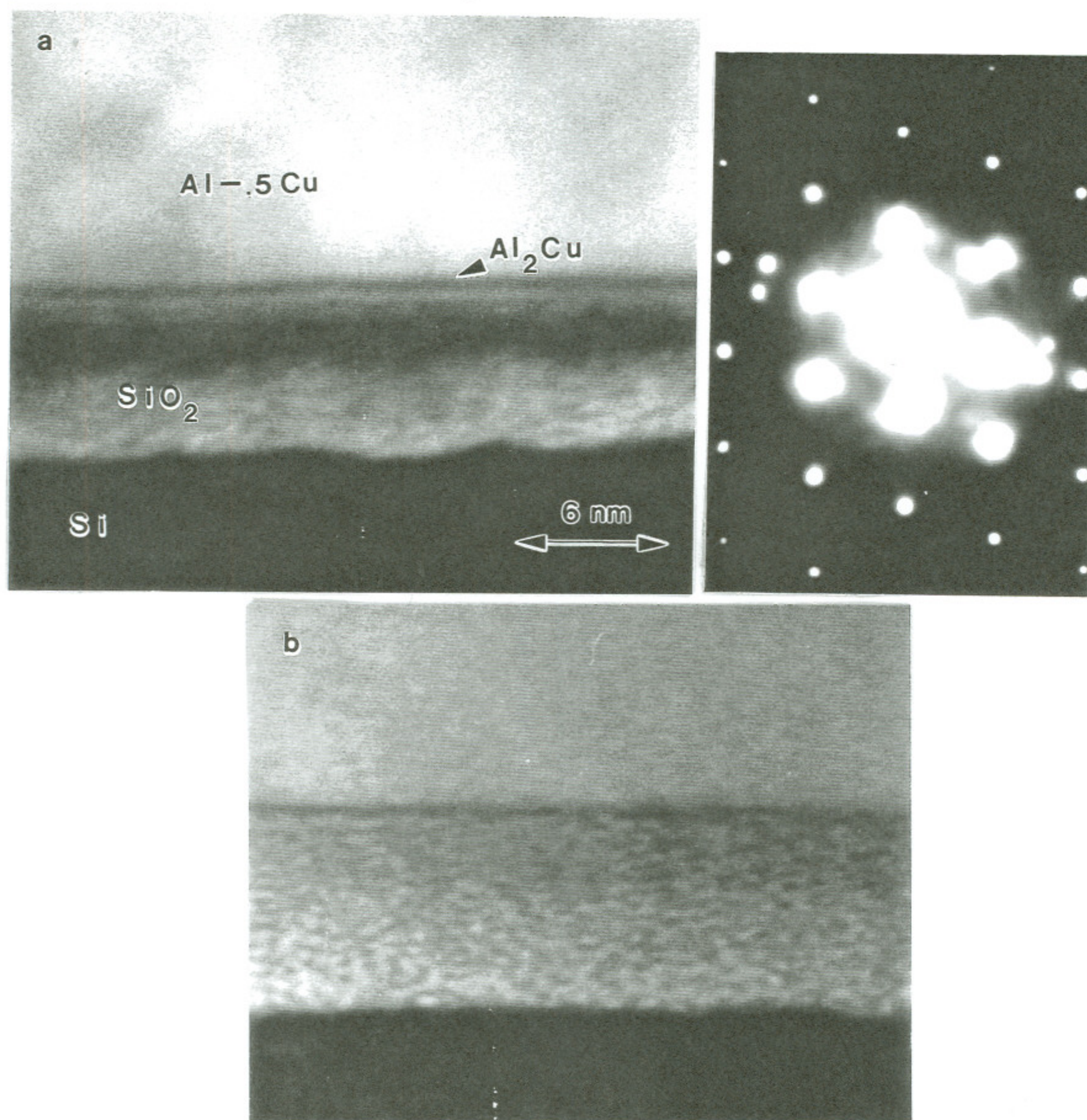


Figure 14 a. Bright field TEM image and diffraction pattern for Al-.5Cu heat treated for 11.25hrs at 400ºC. b) Bright field TEM image of cross section of Al-.5 Cu heat treated for 2hrs. with a less distinct and smaller diffusion zone in the oxide.

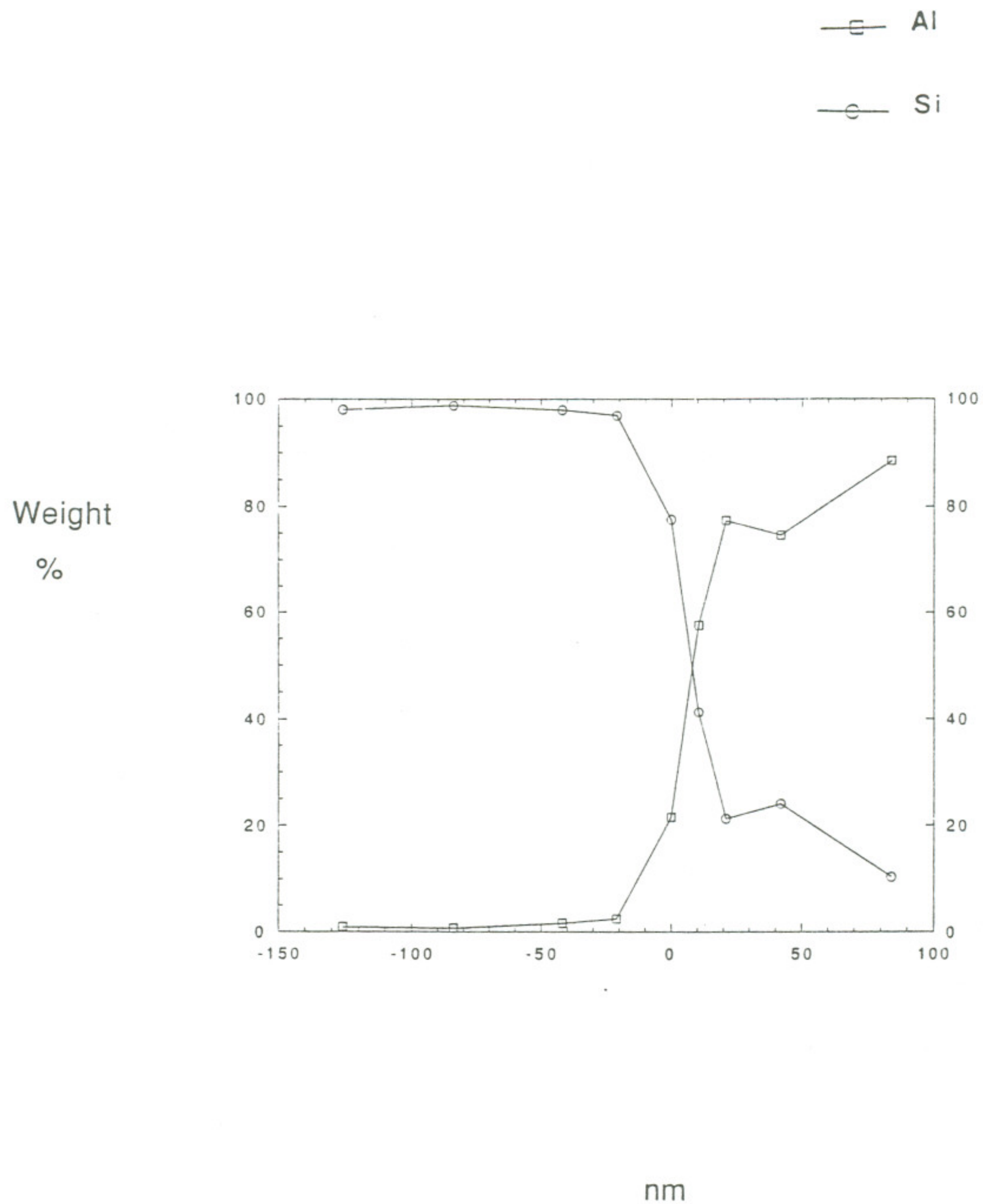


Figure 14c. Compositional profile of Al-.5Cu heat treated for 11.25hrs at 400ºC in N_2.

Cr on SiO_2, as Deposited

The as deposited oxide thickness was 4nm. The reaction layer on the Cr side of the oxide was 2nm thick and had consumed oxide in the process of forming during deposition. This reaction layer had as much as an additional 2nm of thickness at Cr grain boundaries. On the Si substrate side of the oxide the interface with the oxide had larger steps with a higher frequency than observed in the other as deposited specimens. The step heights varied 0.2 to 1nm with a frequency of 12/100nm. There is no evidence of a reaction layer here. Lattice planes are continuous and undistorted up to the interface with the SiO_2 indicating that Cr did not diffuse through the silica during deposition. The as deposited Cr when examined at high resolution revealed 0.8nm pores. The Cr electrode was 200nm thick with grain size of 19.4nm. The selected area electron diffraction patterns only contained spots associated with the Si substrate and rings associated with the Cr electrode. See figure 15.

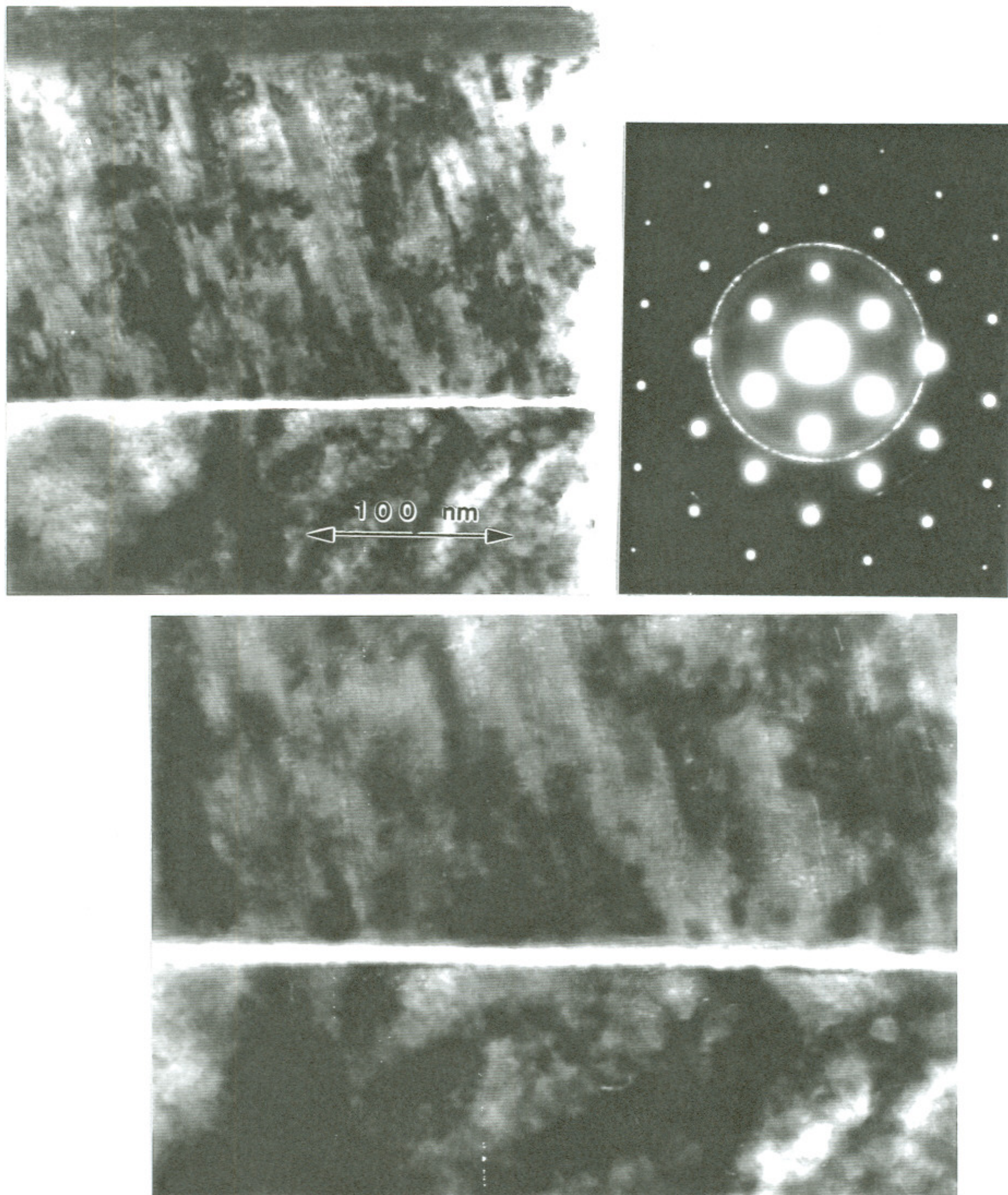


Figure 15. Bright field TEM image and diffraction pattern, as deposited Cr.

Cr on SiO_2, Heat Treated for 2 Hours at 400ºC in N_2

The oxide thickness remained unchanged at 4nm. The reaction layer on the Cr side of the oxide was unchanged but the Si substrate side showed evidence of diffusion in the first 2 or 3 atomic layers(1nm) with darker contrast. See figure 16a. Step heights at the SiO_2/Si interface were from 0.2 to 0.8nm with a frequency of 13/100nm. There were also steps in the SiO_2 of 0.4nm at Cr grain boundaries. See figure 16b. In addition to the reaction layer at the Cr/SiO_2 interface there was also a 10nm reaction layer at the top surface of the electrode. A faint ring in addition to intense Cr rings and Si spots in the selected area electron diffraction pattern indicated the existence of the reaction layers and that they were possibly Cr oxide or silicide. See figure 16a. The electrode thickness increased to 210nm with a grain size of 36nm. The Si content at the center of the electrode reached 11wt%. The diffusion distance was 10nm. Si wt% at the surface was 32 suggesting the formation of silicide there. See figure 16c.

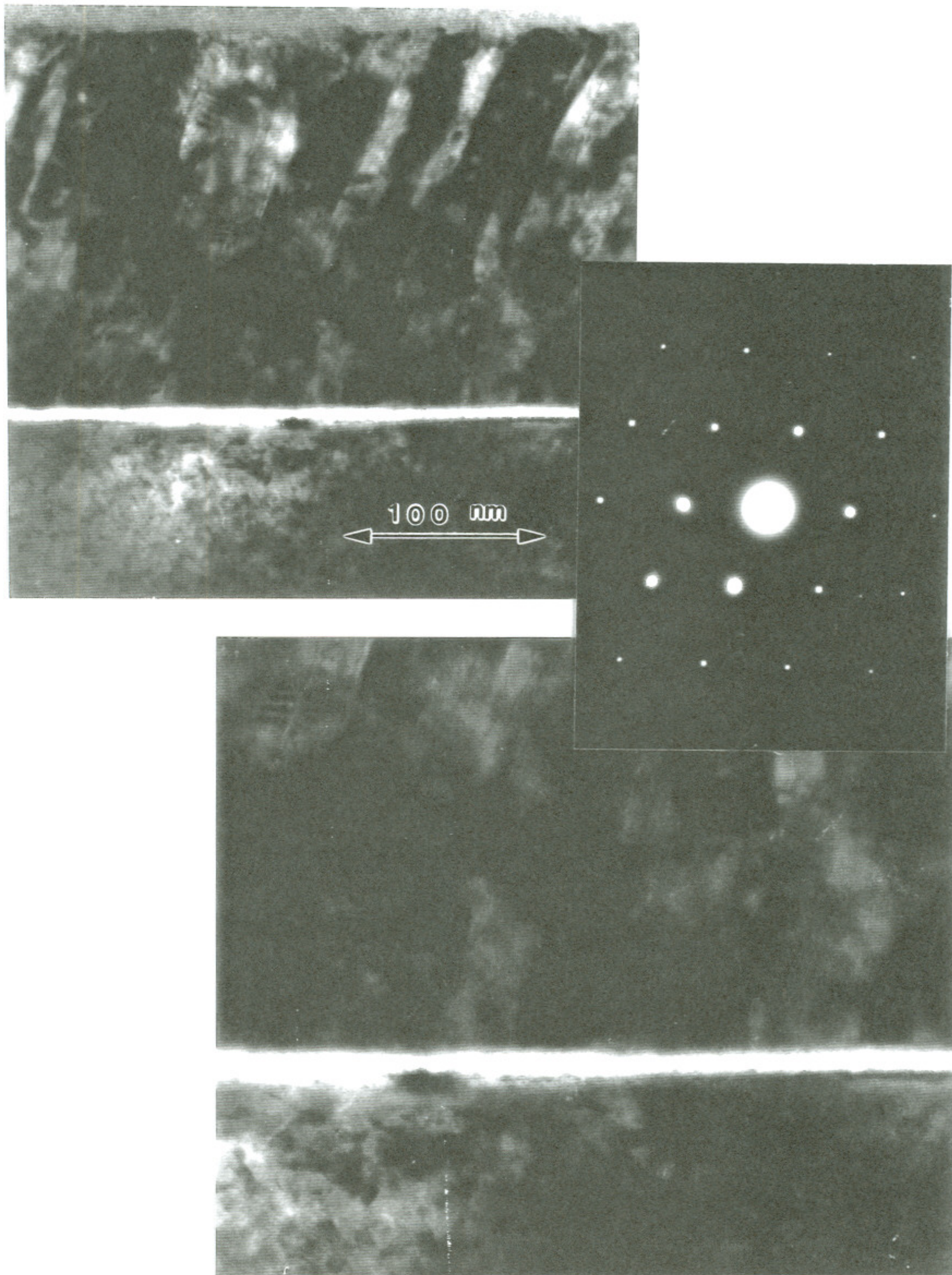


Figure 16a. Bright field TEM images and diffraction patterns of Cr heat treated for 2hrs. at 400ºC.

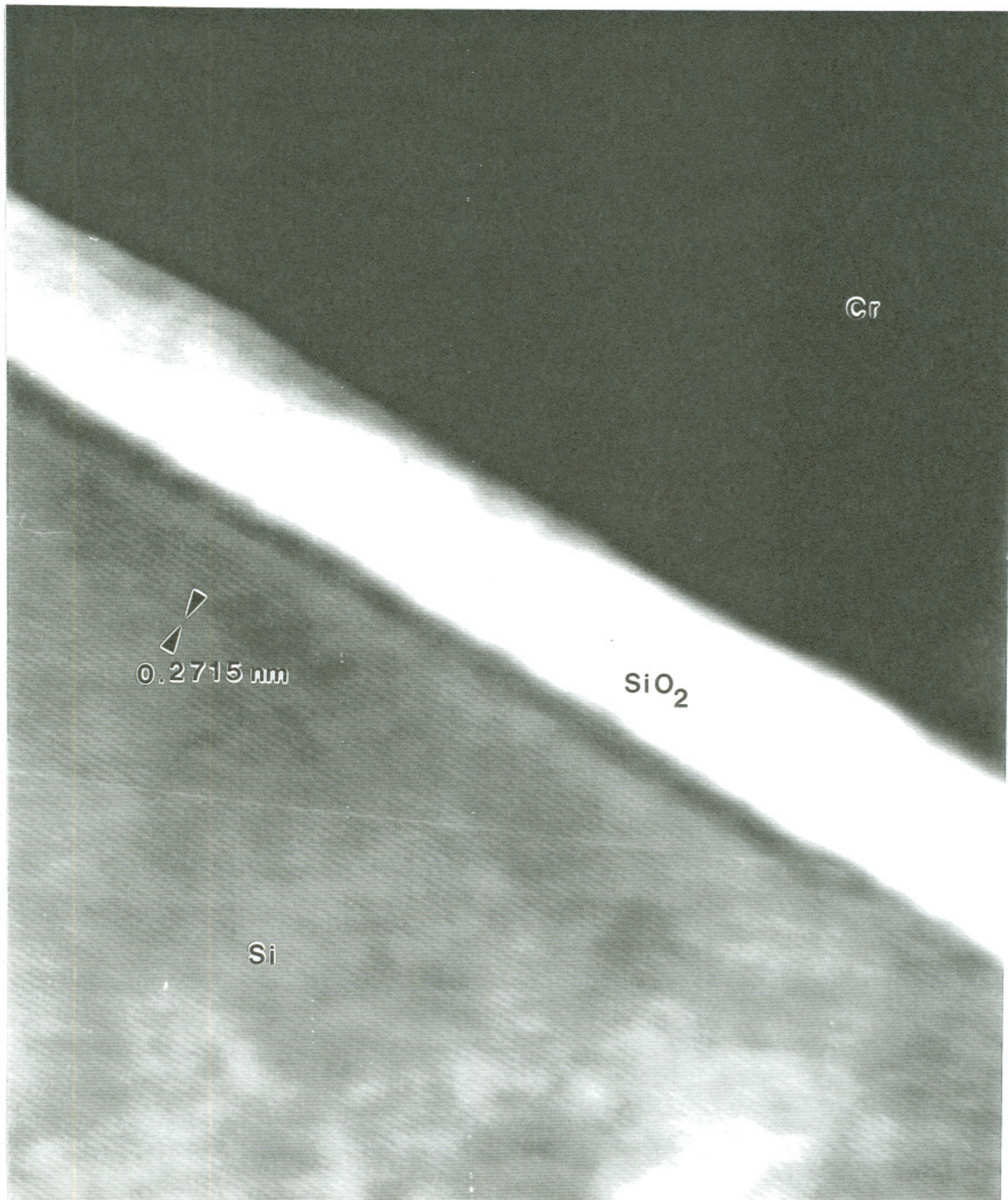


Figure 16b. High resolution image of the SiO_2 interfaces, Cr electrode, heat treated for 2hrs. in N_2 at 400ºC, Si (002) planes.

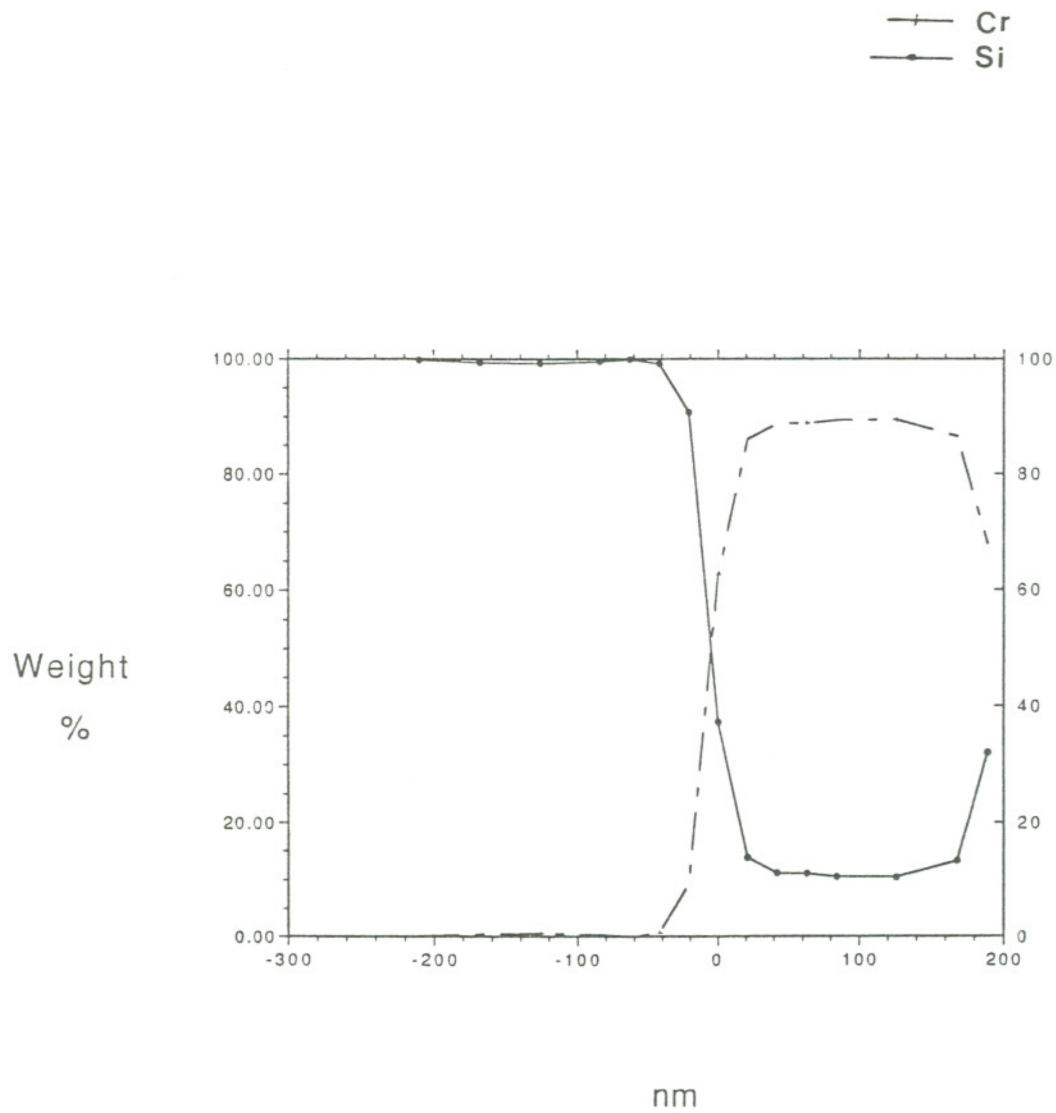
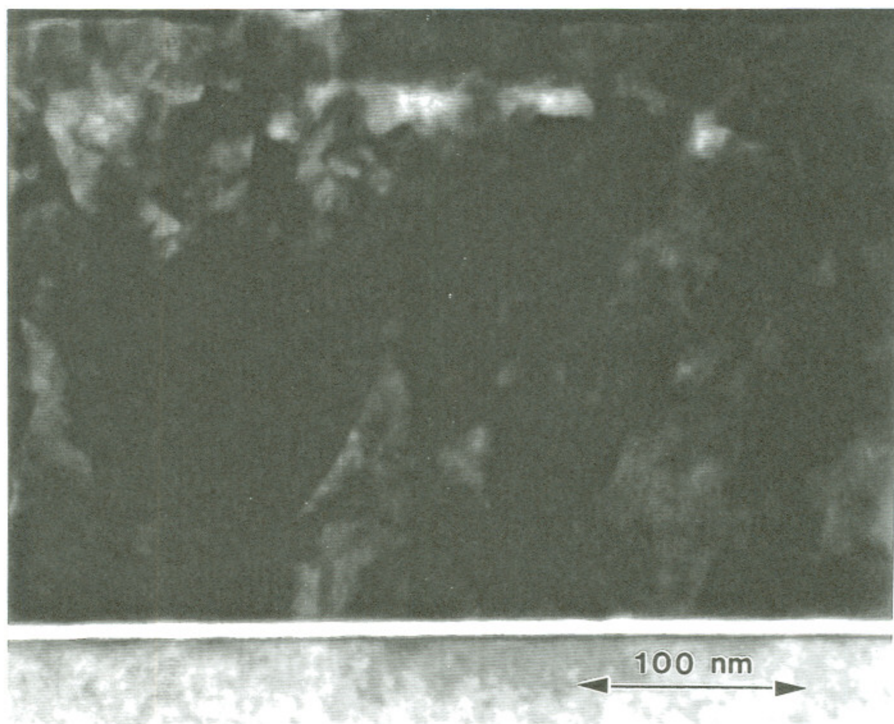


Figure 16c. Compositional profile, Cr electrode, 2hr heat treatment.

Cr on SiO_2, Heat Treated for 12 hours at 400ºC in N_2+furnace cool

The oxide thickness remained at 4nm. Step heights varied from 0.2 to 1nm with a frequency of 8.5/100nm at the oxide/Si substrate interface. The oxide interface with the Cr had steps from 0.2 to 0.6nm with a frequency of 5/100nm. The reaction layers at the Cr and the Si interfaces were 1 to 1.6nm in thickness. At the Cr interface the reaction appears to have advanced into grain boundaries. See figure 17a. A selected area electron diffraction pattern produced by the Cr, SiO_2 adjacent reaction layers, and Si substrate matches d-spacings for trigonal Cr_2O_3, space group 167 or hexagonal $CrSi_2$ space group180. See figure 17a. The electrode diffusion distance for Si increased to 10nm. The Si content at the center of the electrode was 10wt% and 20wt% at the top surface. See figure 17b. The Cr electrode was now 250nm thick and the surface reaction layer had grown to 50nm. Grain size had remained the same at 36nm.



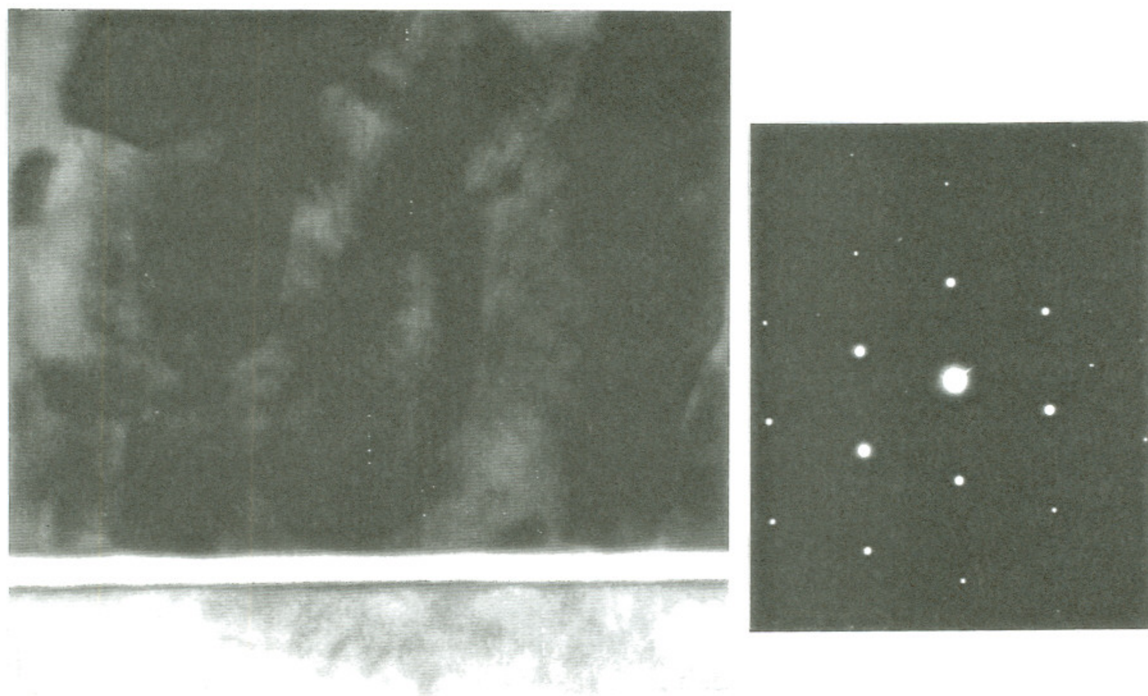


Figure 17a. Bright field TEM image and diffraction pattern for Cr heat treated for 12hrs.

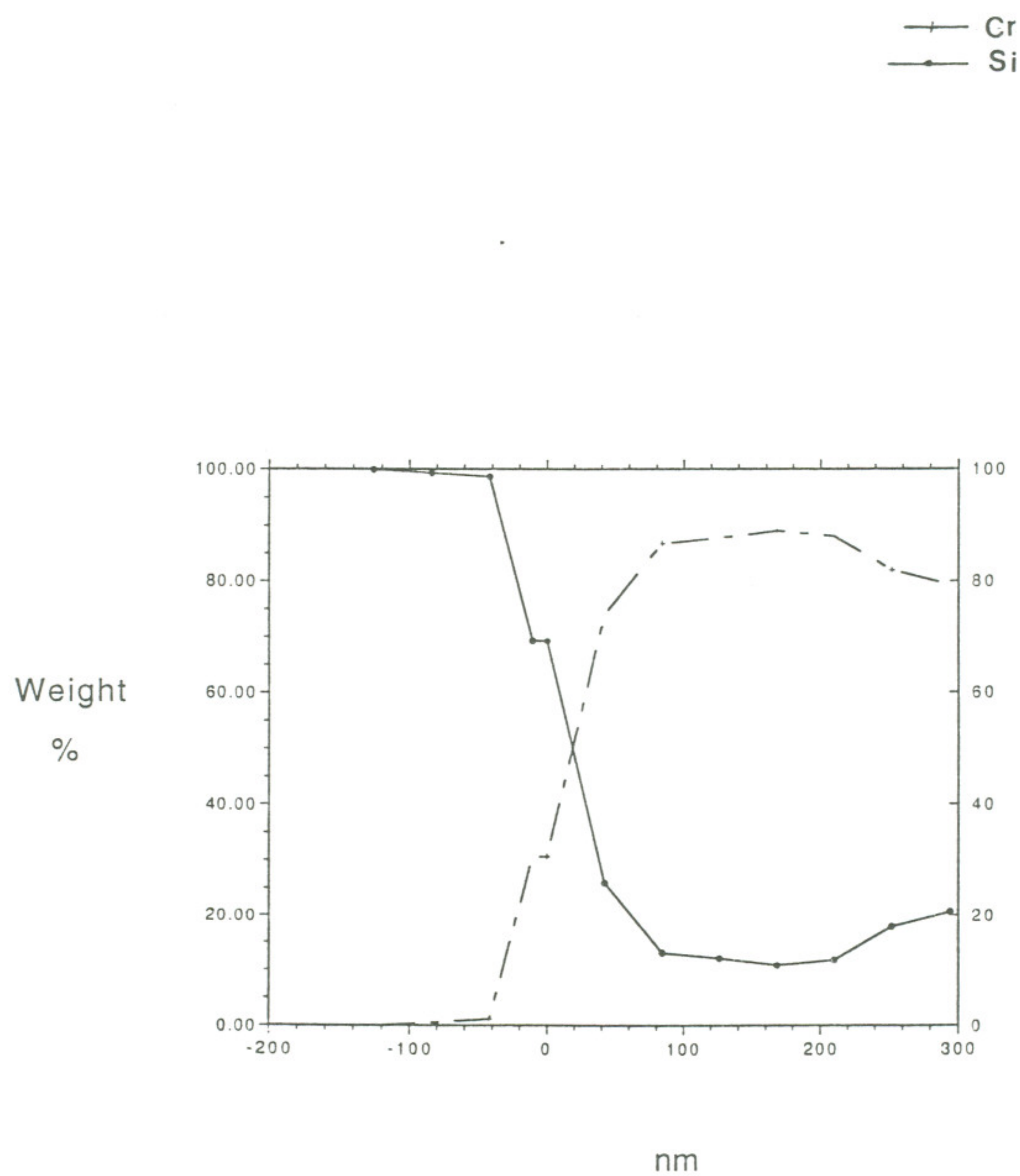


Figure 17b. Compositional profile for the Cr MOS stack heat treated for 12hrs at 400ºC in N_2.

Ti on SiO_2, as Deposited

The oxide thickness was 4nm. At the oxide/Si interface step heights varied from 0.2 to 1.2nm with a frequency of 29.4/100nm. The Ti electrode was 73.3nm thick with a grain size of 24nm. A reaction layer 3.6nm between the Ti and the oxide was present. A 2nm reaction layer was present at the silica/Si interface. Average grain size was 38.6nm. The selected area electron diffraction patterns contained strong reflections for Si and Ti and weak spots indicating orthorhombic Ti_5Si_4 space group 62 or tetragonal Ti_3Si space group 86. See figure 18.

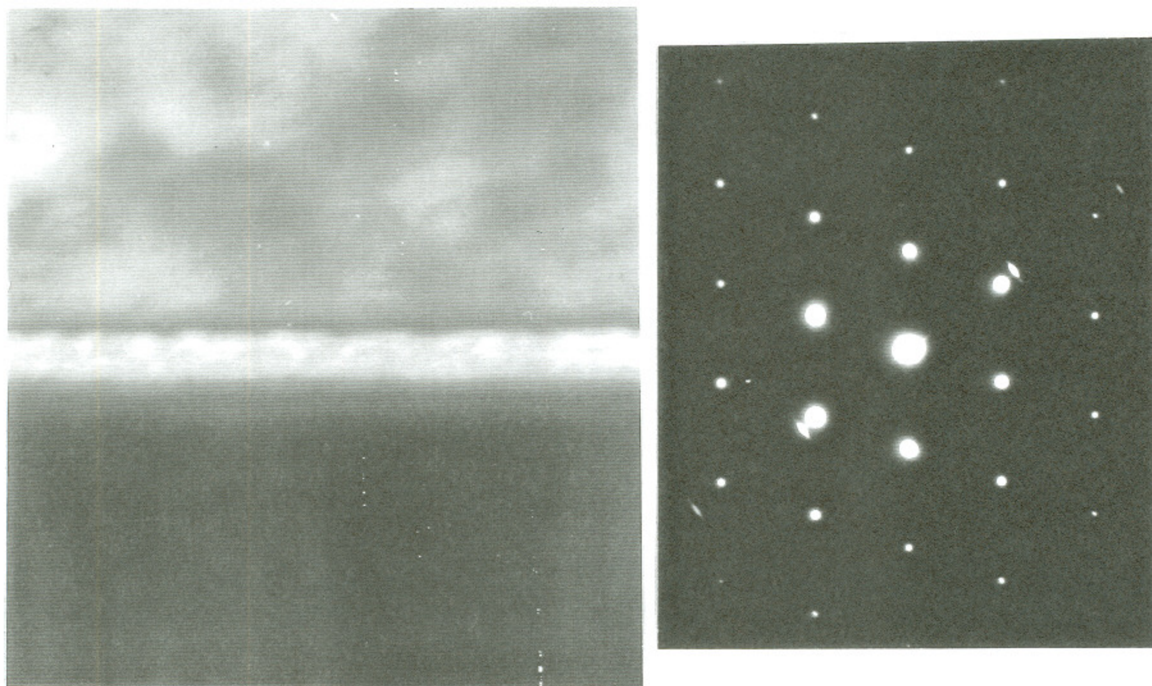


Figure 18. Bright field TEM image and diffraction pattern, Ti as deposited.

Ti on SiO_2, Heat Treated for 2 Hours at 400ºC in N_2

The oxide thickness has decreased to 2nm and due to roughness at the Ti/SiO_2 interface in some areas as thin as 1.5nm. The electrode thickness increased to 190nm. Considerable Si diffusion through the SiO_2 has occurred to produce this vertical expansion of the electrode. The average grain size was 58nm. The metal interface with the oxide has step heights of 0.5 to 1nm with a frequency of 5/100nm. These large steps coincide with grain boundaries. The reaction layer is 3nm thick at these steps and 2nm everywhere else along this interface. The interface of the oxide with the Si substrate has a 1nm reaction layer. The selected area electron diffraction pattern produced by the Si substrate, the oxide and the Ti electrode contained spots associated with the Si, Ti and Ti_3Si or Ti_5Si_4. There were more silicide reflections of greater intensity indicating a greater volume fraction but no new phases after 2 hours of heat treatment. See figure 19.

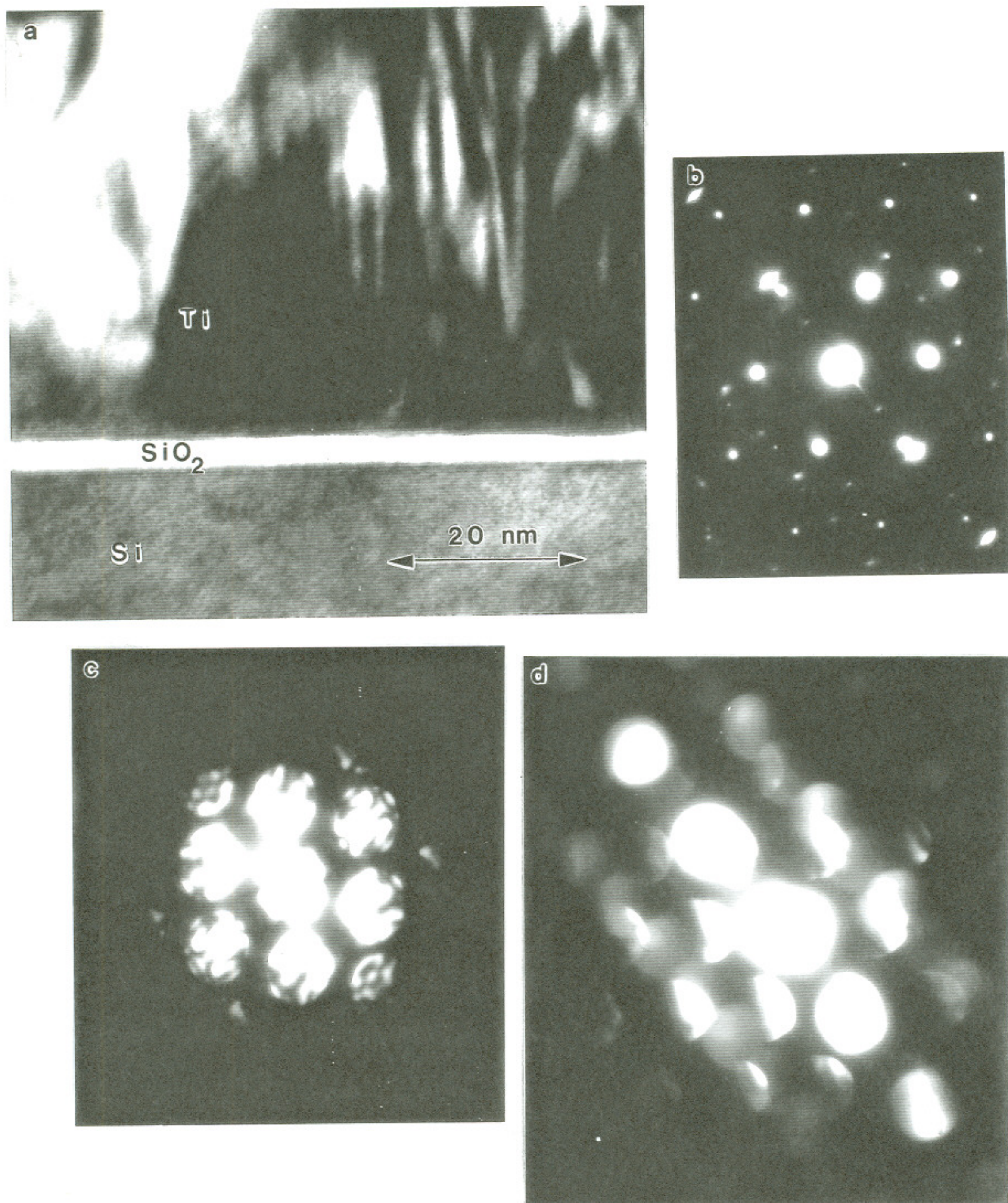
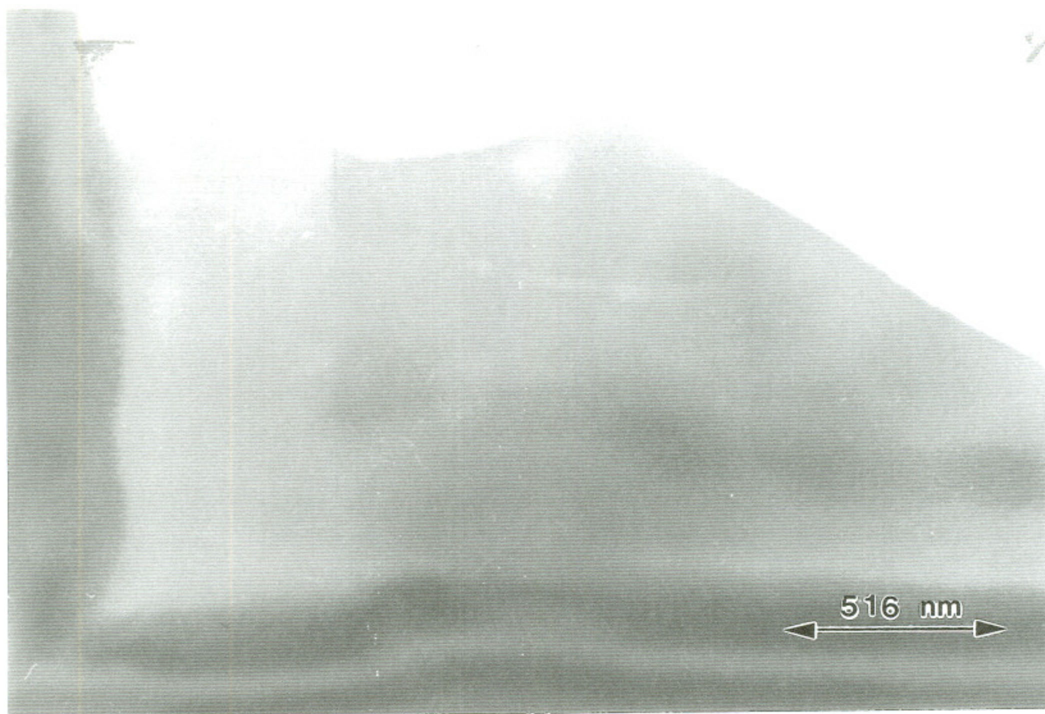


Figure 19a. Bright field TEM image and (b)diffraction pattern for Ti heat treated for 2 hr at 400ºC. c. Si only. d. Si and Ti_3Si near interface.

Al on SiO_2 + Electron Beam Irradiation

A planar section of the as deposited 7nm TCA oxide was produced for this in situ experiment. Diffraction patterns and bright field images of a web of oxide suspended between arms of remaining Si can be seen in figure 20. Less than 5nm of Al was then deposited on the oxide by evaporation in a high vacuum. The oxide and Al were then heated in a 200kV beam to cause reactions between the Al and oxide. Diffraction patterns and bright field images following the reaction are shown in figure 21. The reaction product proved to be Al_2SiO_5 and the d spacings measured from the diffraction pattern proved to be the same as those in the diffraction pattern produced by the heat treated Al-1Si specimen. The source of O_2 for the oxidation could be the gate oxide or the residual O_2 in the electron microscope vacuum. The gate oxide can be consumed reducing the thickness of the gate and as a result reducing its breakdown voltage. The O_2 can also come from the vacuum or ambient atmosphere in which the metal deposition or subsequent heat treatment is done.



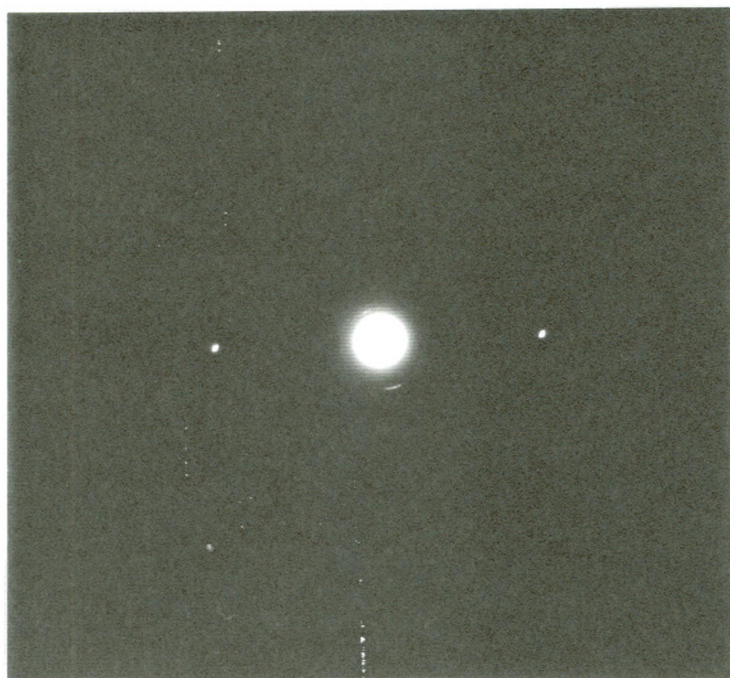


Figure 20. Bright field TEM image and diffraction pattern for as deposited SiO_2.

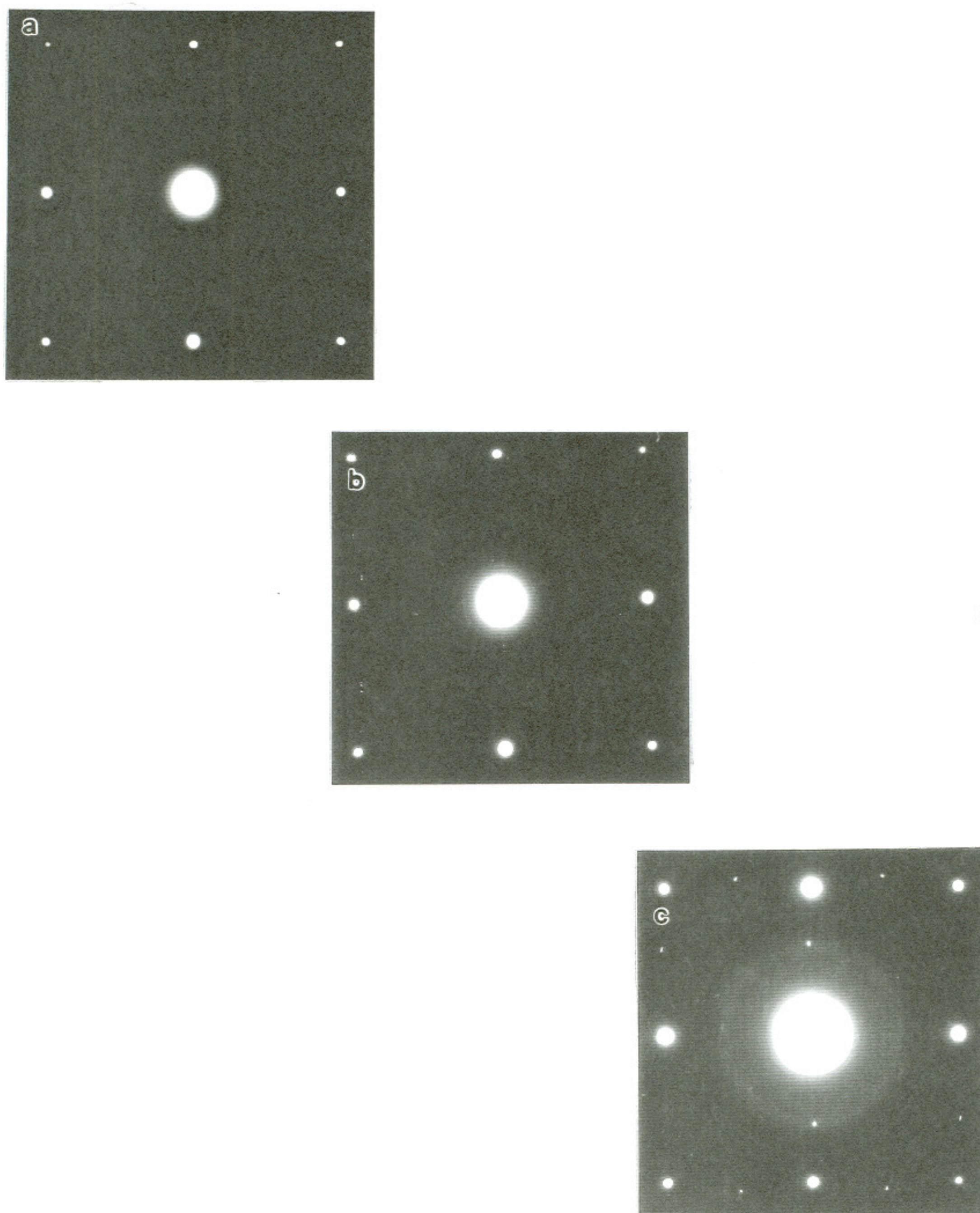


Figure 21. Series of diffraction patterns produced by a region of the oxide/Si in figure 20a. without Al. b. with Al. c. after electron irradiation.

W on SiO_2 +Electron Beam Irradiation

W was deposited directly on silica to form 3nm diameter single grain islands which are visible in the atomic resolution image in figure 22. When subjected to 200kV electron beam heating the W reacted with the silica to form WO_3 and a surplus of Si in the SiO_2. The before and after diffraction patterns in figure 23 prove this.

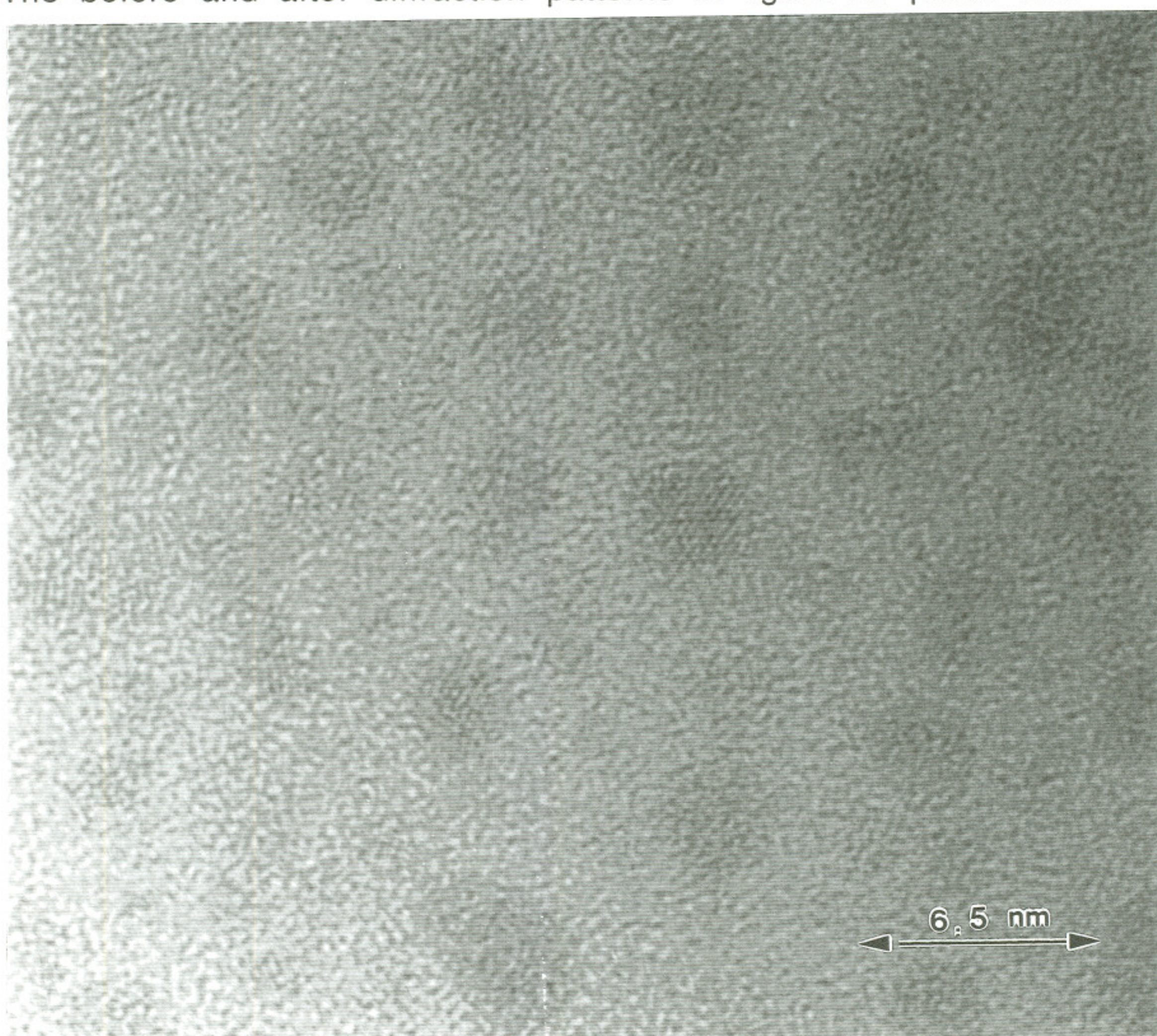
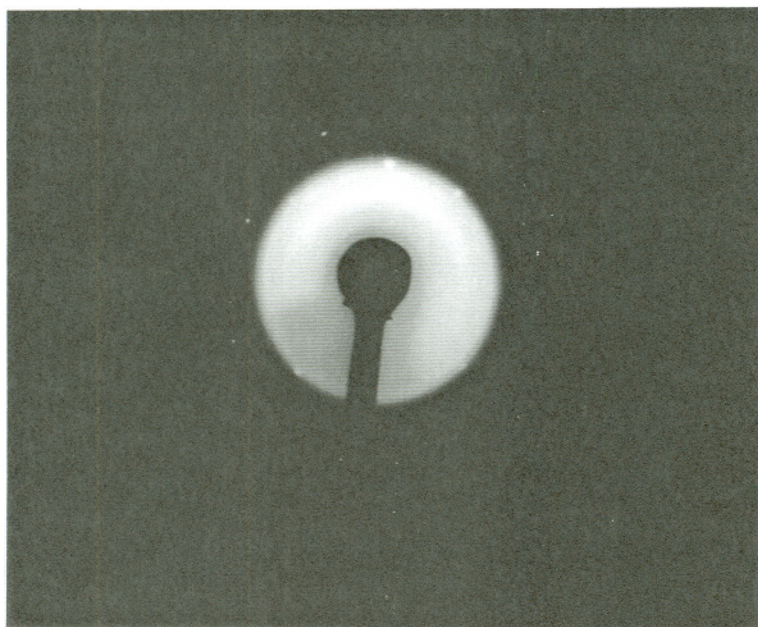


Figure 22. Atomic resolution image of W islands on heat treated SiO_2.



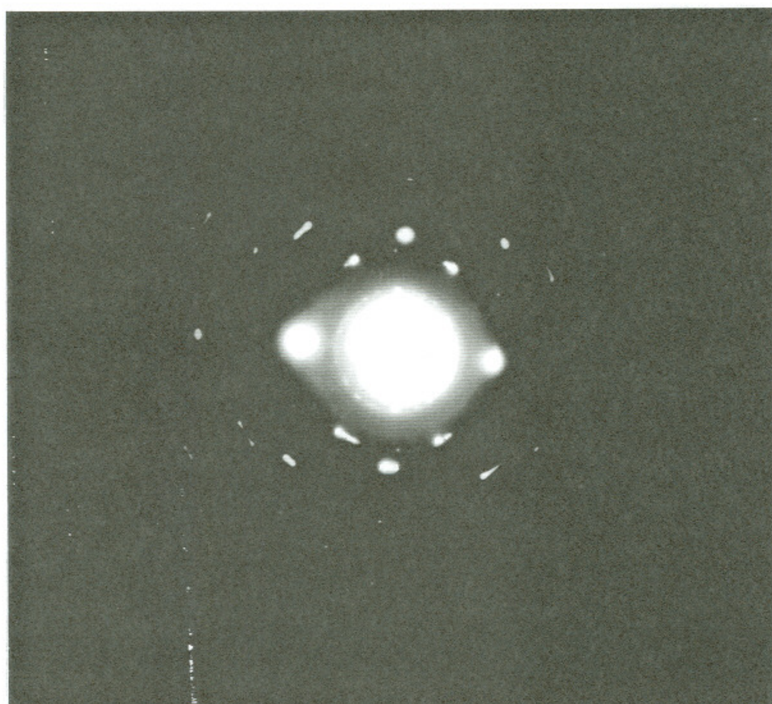


Figure 23. Diffraction patterns before and after electron irradiation for W/SiO_2.

6. DISCUSSION

Comparison of the Al-1Si and Al-.5Cu on SiO_2 Results

In addition to the 2 hour heat treatment the Al-.5Cu and the Al-1Si electrodes were given additional heat treatments for 4 and 12hrs. to enhance microstructural changes that were occurring in these electrodes. These electrodes were chosen for their good and bad BVG performance, respectively. The extended heat treatment enhanced changes were easier to detect and quantify. The enhanced microstructural changes were correlated with performance and mechanisms of change were proposed.

The Al-.5Cu electrode as deposited, gate oxide and Si substrate produced only spots associated with Si and Al in a selected area electron diffraction pattern. The as deposited Al-.5Cu/SiO_2/Si interfaces showed evidence of reaction layers by dark contrast near those interfaces. See figure 10. The Al-.5Cu specimen heat treated for 2 hours at 400ºC did show 0.8nm reaction layers and extra diffraction spots indicating the formation of new phases. See the bright field TEM image and selected area diffraction pattern in figure 11. The most probable phases to form were Al_2Cu, Al_2O_3 or Cu_2O. High resolution images show a lattice spacing of .271nm for the Si but near the Si/SiO_2 interface a larger lattice spacing and amorphous regions are visible. There are closely spaced spots near the transmitted spot in a diffraction pattern produced by the

interfacial regions indicating long range ordering with a repeat distance of 6.6nm.

The heat treated Al-1Si electrode in contrast had a reaction layer of 30nm as is shown by the dark field image in figure 8. Compositional profiles of this heat treated specimen from the Si substrate across the SiO_2 and out to the top surface of the Al-1Si and Al-.5Cu electrodes are shown in figures 8, 9, 10, 11 and 12. The Al-.5Cu electrode did not have as high a Si concentration as the Al-1Si electrode for all heat treatment durations. The Si concentration reached 50wt% at 50nm deep in the Al-1Si electrode but only 10wt% in the Al-.5Cu. The gradient of the Si concentration is much higher for the Al-.5Cu indicating a much lower diffusion coefficient for Si in Al-.5Cu. The solubility of Si in Al is very low at room temperature, .05wt%. Most of the Si in the electrode is not in solution and is therefore in the form of loops, second phase precipitates of pure Si or Al_2SiO_5. The diffusion of Cu or Al into the Si was not detectable by this profiling technique due to the 30nm spot size suggesting that the diffusion distance was much less than 30nm. Cu was found to segregate to the Al-.5Cu/SiO_2 interface, Al-.5Cu grain boundaries and the Al-.5Cu electrode top surface for the heat treated specimens. The as deposited specimen did not show this segregation of Cu. See figure 12.

The planar section of the Al.5Cu-4hr confirmed the segregation of Cu to the SiO_2 interfaces and provided complete zone axis electron diffraction patterns for a more positive identification of phases at the interface. This specimen exhibited regions with the

complete MOS device including metal, interfacial reaction layers, SiO_2 and Si substrate. See figure 13. There were also areas of this thin section that included just the metal, the interfacial reaction layer plus SiO_2 and regions with only SiO_2. The interfacial reaction layer was composed of relatively large grains approximately 100nm in diameter making a 1nm thick continuous polycrystalline boundary at the interface reproducing the size and shape of the Al grain boundary faces at the interfaces. Superlattice images of this interfacial layer for nearly a complete Al grain is shown in figure 13, supporting the contention that this layer is continuous and complete. This effect has been explained by Frear et. al. by the system seeking minimum interfacial energy between the incoherent Al_2Cu and the Al.(51) In addition to the segregation caused Al_2Cu intermetallic layer at the Al-.5Cu/SiO_2 interface there is also a reaction layer at the SiO_2/Si interface. X-ray microanalysis of the amorphous oxide layer with little or no indication of crystalline material measured high Cu and Al concentrations in this altered gate oxide.

In addition to confirming the existence of the intermetallic boundary layer, the planar section of the heat treated oxide and Al-.5Cu electrode gave insight into the oxide structure and the effects of heat treatment with the addition of metallization, effects not observed in the oxide heat treated without a metallization with the same TEM specimen preparation. Examination of the TEM bright field images of regions of only oxide reveals the oxide heat treated with metallization to be composed of broad regions of high density

bounded by narrow regions of low density. These preferentially ion milled narrow thinner regions appear as bright regions in the image. The darker thicker regions bounded by light regions have the size and shape of the Al grains of the electrode before heat treatment. The grain boundaries of the Al have a much higher diffusion coefficient for Si than the grains and would deplete Si from the regions of the oxide directly below the boundaries, triple points having the highest diffusion coefficient and therefore as seen in figure 13c. were the initiation sites of holes during the ion milling process. The Al-.5Cu electrode as deposited showed no evidence of the intermetallic diffusion barrier layer in electron diffraction patterns or X-ray microanalysis. The depletion of the silica of Si occurred at room temperature before heat treatment and during heat treatment at temperatures below the intermetallic transformation temperature when the barrier layer was not present. During ion milling the regions in the oxide below triple points develop holes first. Ion milled heat treated SiO_2 without a metallization does not show this preferential ion milling behavior. The high flux of Si through the oxide at these sites causes defects such as vacancies, low oxygen content and interstitials. These defects increase the milling rate of this less dense, strained or more weakly bonded material. This ion milling "etch" is analogous to the chemical etching of grain boundaries in metals and dislocations in Si. See figure 13c.

Cr on SiO_2 Results

Post heat treatment Cr showed an increase in grain size and pore size but no change in oxide thickness after 14hrs. at 400ºC in an N_2 ambient. The Cr MOS device as deposited had a microstructure with a high defect density characterized by fine columnar grains with a diameter of 18nm and 0.8nm diameter pores distributed evenly throughout the thin film. Following heat treatments for 2 and 12 hours, grains grew to 22 and 60nm respectively. Pores first coalesced at grain boundaries forming channels 50nm in length after 2hrs. of heat treatment. After 14 hours the channels had disappeared and large pores remained within the larger annealed grains. See figures. BVG measurements on the Cr devices as deposited were high at 7.4V and 7.9V for 10% failure following heat treatment. A 1.6nm reaction layer formed during magnetron sputtering of the Cr and does not significantly increase or decrease after 14hrs. of heat treatment in N_2. The Cr/SiO_2 interface roughness did increase during heat treatment from 0.8nm to 1.6nm after 2hrs. at 400ºC. The frequency of steps decreased from 12/100nm as deposited, first to 4/100nm at 2hrs. and then 1/100nm at 12hours. The SiO_2/Si interface roughness does not change step height or frequency, 0.3nm and 30/100nm respectively.

Tables and Graphs of the Results

In addition to comparisons between pairs of electrodes tested, the data collected from all electrodes was tabulated for easy comparison and selected results graphed for the isothermal heat treatments.

The most obvious change that occurred during heat treatment was an increase in electrode thickness due to the diffusion of substrate Si through the SiO_2 into the electrode. This growth in addition to introducing vertical stresses exerted (perpendicular to the planes of the thin films in the gate structure) on films above and below the electrode exerts stress laterally on via walls causing faults and defects in the field oxide. The expansion of the (111) d spacing by 0.005 nm represents a lattice parameter change (lateral strain) of 2.13%. This stress is transmitted to the gate oxide causing the oxide to be in tension at the Al-1Si/SiO_2 interface. The SiO_2 at the SiO_2/Si interface has been in compression since its cooling from the deposition at a temperature of 1000ºC. This stress is caused by cooling to room temperature and differences in the linear thermal coefficient of expansion for Si and SiO_2; $3.4\text{-}4.5x10^{-6}$ and $5x10^{-7}$ºK^{-1}. Stresses in the oxide at room temperature are reported to be in the range of $2\text{-}4x10^{9}$ dyne/cm.(52-54) Atoms will diffuse from regions of compression to regions of tension. These stresses add a stress driven component to the diffusion of Si to the concentration gradient driven diffusion already existing between the metal and the Si substrate. Stress in the oxide decreases resistivity. The

electrode growth rate for the Cr electrode with a diffusion barrier that formed during deposition was lowest. See table 3 and figure 24. The Al-.5Cu electrode formed a barrier during heat treatment which stopped Si diffusion between 2 and 4 hours. See figure 25. The Al-1Si electrode had the highest growth rate of 60nm/hr with no indication of decreases over the 12hrs. of heat treatment studied in this research. The electrode thickness after 12hrs. was 9 times the as deposited thickness. Growth in the tested electrodes shows a linear dependence on heat treatment time with a constant slope when reactions are not in progress forming compounds that act as diffusion barriers.

Table 3. Electrode Thickness, Growth Rate and BVG vs. Hours of Heat Treatment

	A	B	C	D	E
1	Metallization	t @400ºC	X electrode thickness	dX/dt	BVG 10% fail
2		hrs	nm	nm/hr	V
3					
4	Al-1Si	0	90	60	0.4
5		2	210		0.2
6		12	810		
7					
8	Al-.5Cu	0	95	10	8.2
9		2	110		7.1
10		4	135		5.1
11		11.25	133	0	
12					
13	Cr	0	193	5.25	7.4
14		2	203		7.9
15		12	256		
16					
17	Ti	0	73.3	58.35	6.6
18		2	190		0.2

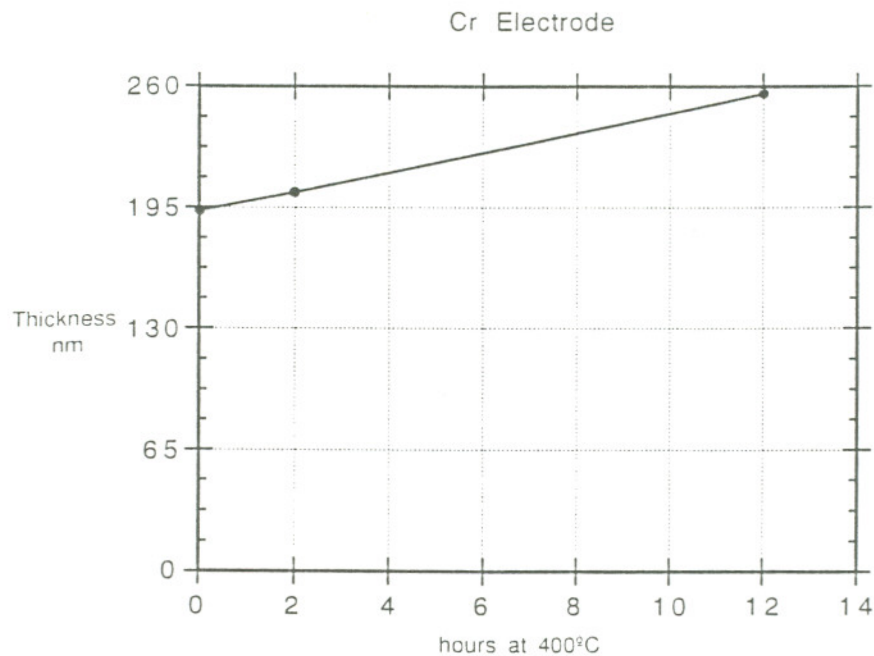


Figure 24. Thickness as a function of heat treatment time for Cr on silica

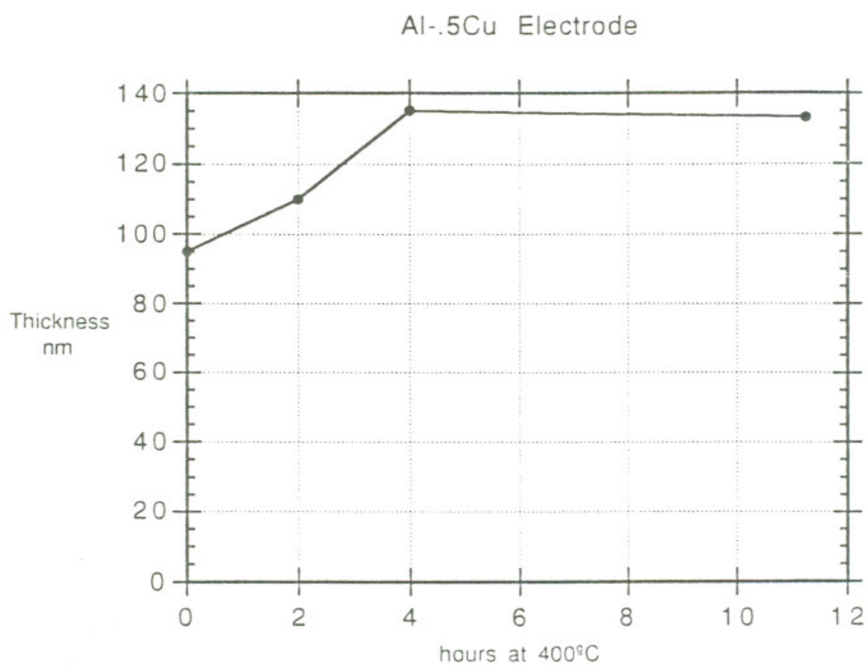


Figure 25. Thickness as a function of heat treatment time for Al-.5Cu in N_2.

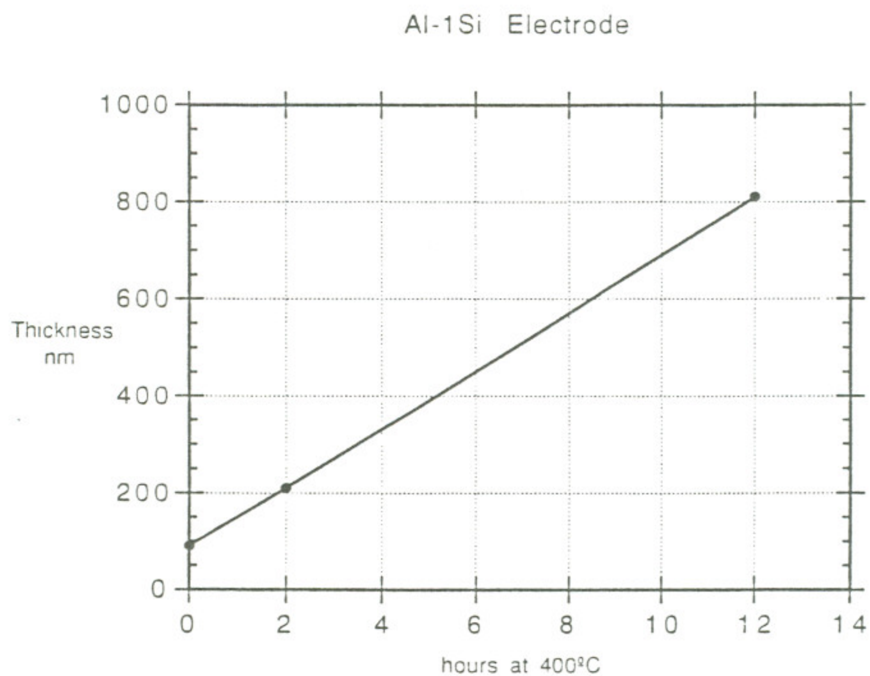


Figure 26. Thickness as a function of heat treatment time for Al-1Si in N_2.

The reaction layers at the silica interfaces can destabilize the gate structure by consuming the gate oxide and/or permitting a high flux of Si into the electrode. Reactions can also form diffusion barriers by self limiting reactions that stabilize the structure for long periods of time at elevated temperatures. Cr and Al-.5Cu formed stabilizing layers with a growth rate that declined with increased time. The Al-1Si consumed a reaction layer at the SiO_2/Si interface that formed during deposition or in the room temperature period preceding heat treatment.

Table 4. The SiO_2/Si Reaction Layer Thickness

	A	B	C	D
1	Metallization	t @ 400ºC	Silica/Si Reaction Layer	BVG 10% fail
2		hrs	nm	V
3				
4	Al-1Si	0	12.5	0.4
5		2	7.5	0.2
6		12	0.8	
7				
8	Al-.5Cu	0	0	8.2
9		2	0.6	7.1
10		4	0.8	5.1
11		11.25	1	
12				
13	Cr	0	0	7.7
14		2	1	8.4
15		12	1.3	
16				
17	Ti	0	2	6.6
18		2	1	0.2

The generation of the volume of reaction products is directly proportional to the thickness of the reaction product layer. The reaction layer at the Si/SiO_2 interface are diffusion controlled reactions as shown by the following three graphs. Cr and Al-.5Cu formed stable reaction layers with a logarithmic thickness dependence on time. The growth rate approaches zero. Al-1Si formed a reaction layer during deposition or the period at room temperature before heat treatment which was nearly consumed during heat treatment as is shown by figure 27. Ti deposited directly on SiO_2 had a similar behavior.

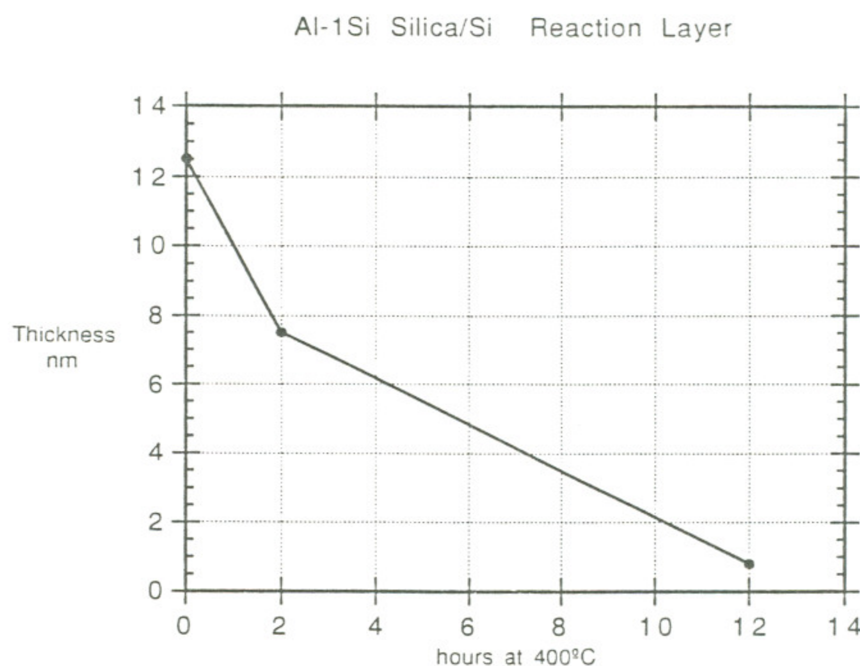


Figure 27. Si/SiO_2 reaction layer thickness as a function of time for Al-1Si

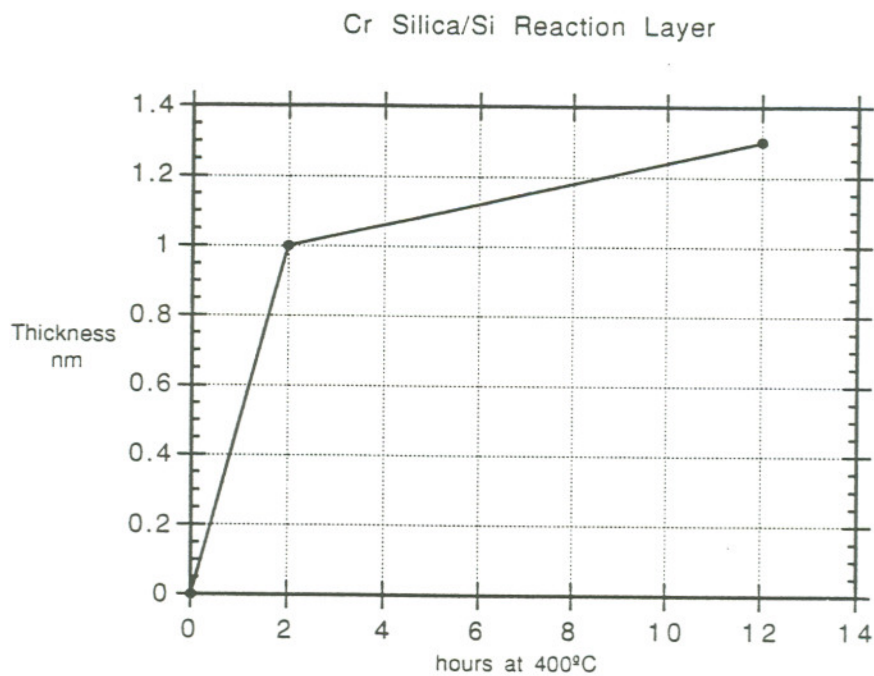


Figure 28. Si/SiO_2 reaction layer thickness vs. time for Cr

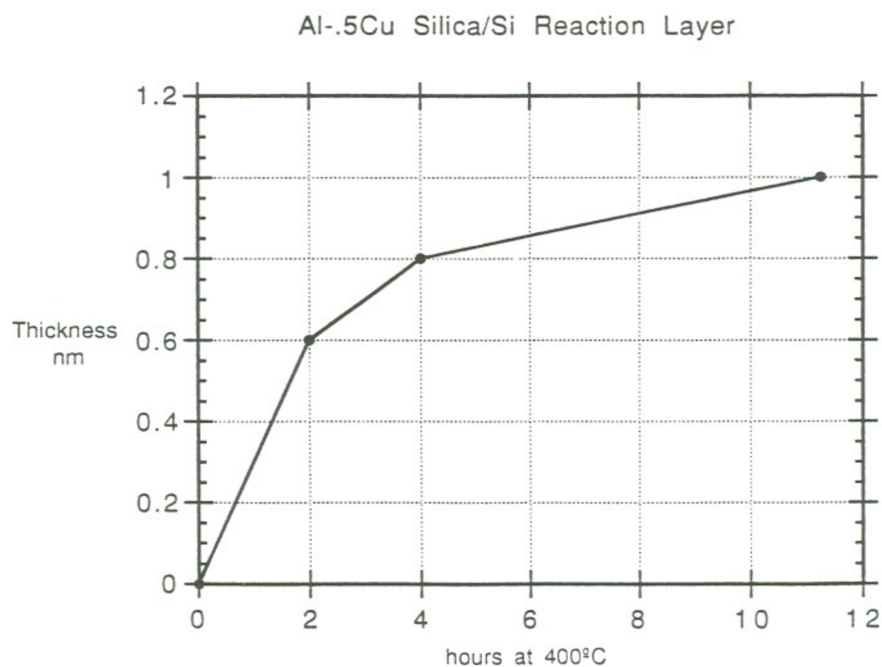


Figure 29 . Si/SiO_2 reaction layer thickness vs. time for Al-.5Cu

The metal/silica reaction layer thickness displayed a logarithmic dependence on time for both Al-1Si and Al-.5Cu. A stable layer is not necessarily a good diffusion barrier since it may have a high diffusion coefficient for Si or metal. Cr appeared to be stable for the first two hours of heat treatment but decreased during the 12hr. heat treatment.

Table 5. The Metal/Silica Reaction Layer Thickness

	A	B	C	D	E
1	Metallization	t @400°C	Metal/SiO Reaction Layer	At Grain Boundary	BVG-10% fail
2		hours	nm		V
3	Al-1Si	0	0		0.4
4		2	0.77	1.49	0.2
5		12	1.2		
6					
7	Al-.5Cu	0	0		8.2
8		2	0.6		7.1
9		4	0.8		5.1
10		11.25	1		
11					
12	Cr	0	2		7.7
13		2	2		8.4
14		12	1.3		
15					
16	Ti	0	3.6		6.6
17		2	2	3	0.2

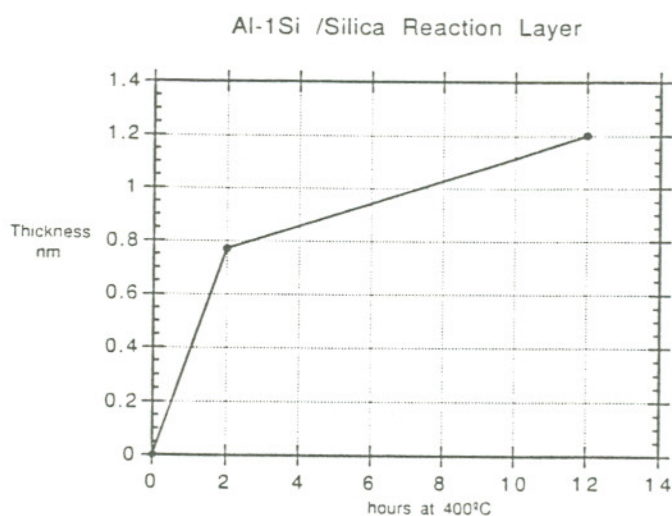


Figure 30. Al-1Si /SiO_2 interface reaction layer thickness vs. time.

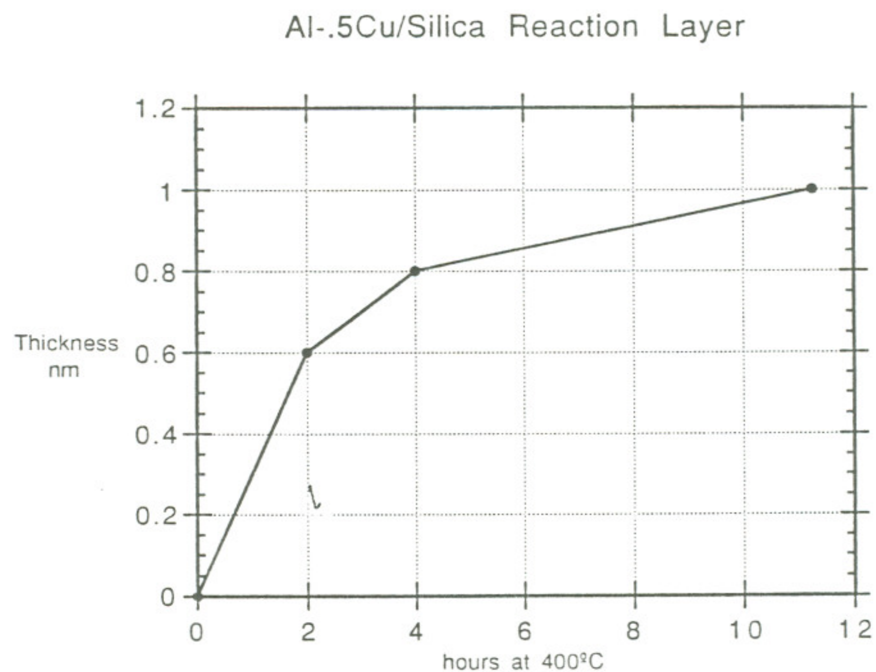


Figure 31. Al-.5Cu /SiO_2 interface reaction layer thickness vs time.

The silica thickness decreases as heat treatment time increases for specimens with a deposited electrode . The greatest loss of oxide occurs with the Ti electrode, which after 2hrs of heat treatment only has 2nm left. Typical losses were less than 2nm. Cr consumed 3nm of oxide during deposition leaving 4nm and did not change for up to 12hrs. of heat treatment.

Table 6. Silica Thicknesses and Heat Treatment Duration

	A	B	C	D	E
1	Metallization	t @ 400°C	x oxide thickness	dx/dt	BVG
2		hrs	nm	nm/hr	V
3					
4	none	0	7		
5		2	15	3.5	
6					
7	Al-1Si	0	8		0.4
8		2	6.6	-0.7	0.2
9		12	6	-0.17	
10					
11	Al-.5Cu	0	6		8.2
12		2	6	0	7.1
13		4	6	0	5.1
14		11.25	5	-0.137	
15					
16	Cr	0	4		7.7
17		2	4	0	8.4
18		12	4	0	
19					
20	Ti	0	4		6.6
21		2	2	-1	0.2
22					
23	Al-1Si/p-Si	0	6.3		7.7
24		2	8.8	1.25	7.6
25					
26	Al-.5Cu/p-Si	0	8		8.4
27		2	6	-1	7.7

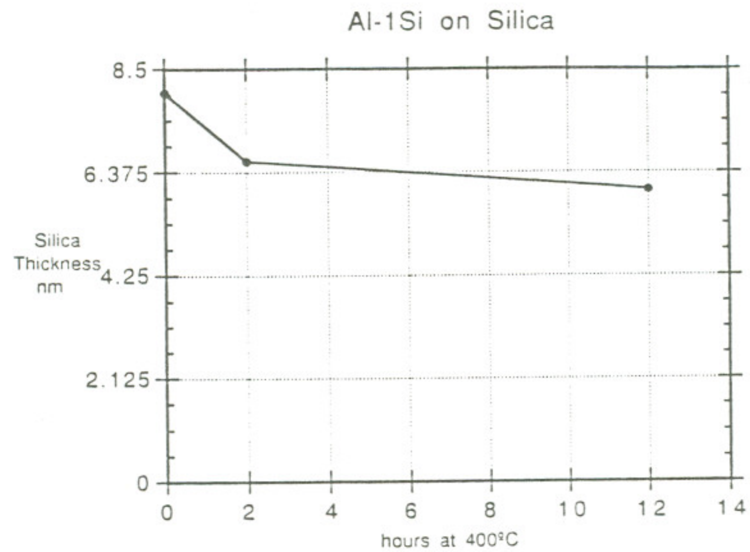


Figure 32. Al-1Si electrode oxide thickness vs. time.

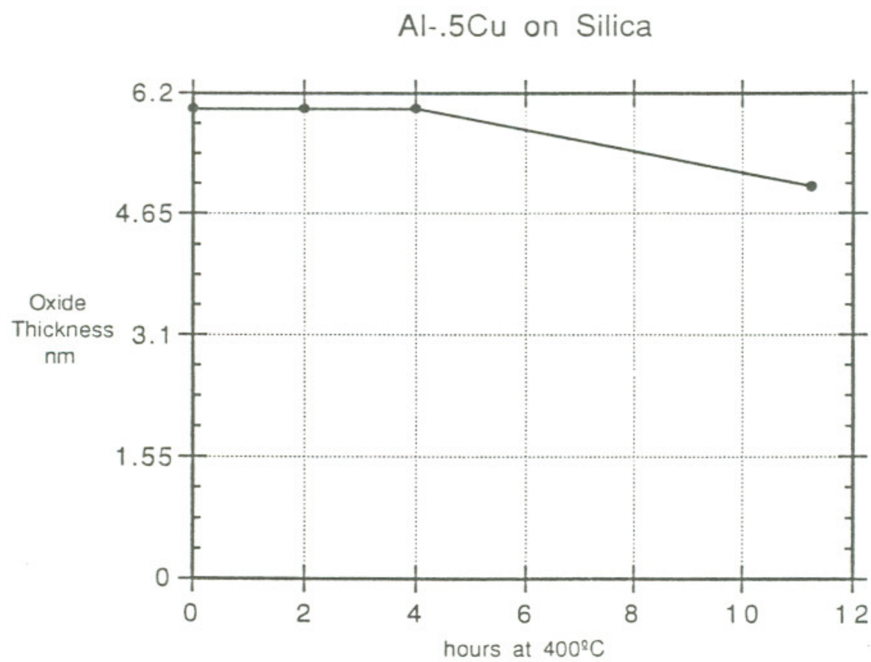


Figure 33. Al-.5Cu electrode oxide thickness vs. time.

Grain growth in the Cr and Al-.5Cu electrodes which developed diffusion barriers stopped after 2 and 4hrs. of heat treatment respectively. Al-1Si did not stop even at 12 hrs. of heat treatment. The time dependence of grain diameter is linear. If diffusion barriers form at grain boundaries the growth rate drops to 0.

Table 7. Electrode Grain Diameter and Heat Treatment Duration

	A	B	C	D	E
1	Metallization	t @ 400ºC	D Grain diameter	dD/dt	BVG 10% fail
2		hrs	nm	nm/hr	V
3					
4	Al-1Si	0	73		0.4
5		2	214	70.5	0.2
6		12	1200	93.9	
7					
8	Al-.5Cu	0	162		8.2
9		2	370	104	7.1
10		4	650	122	5.1
11		11.25	650		
12					
13	Cr	0	19.4		7.7
14		2	36	8.3	8.4
15		12	36		
16					
17	Ti	0	23		6.6
18		2	58	17.5	0.2

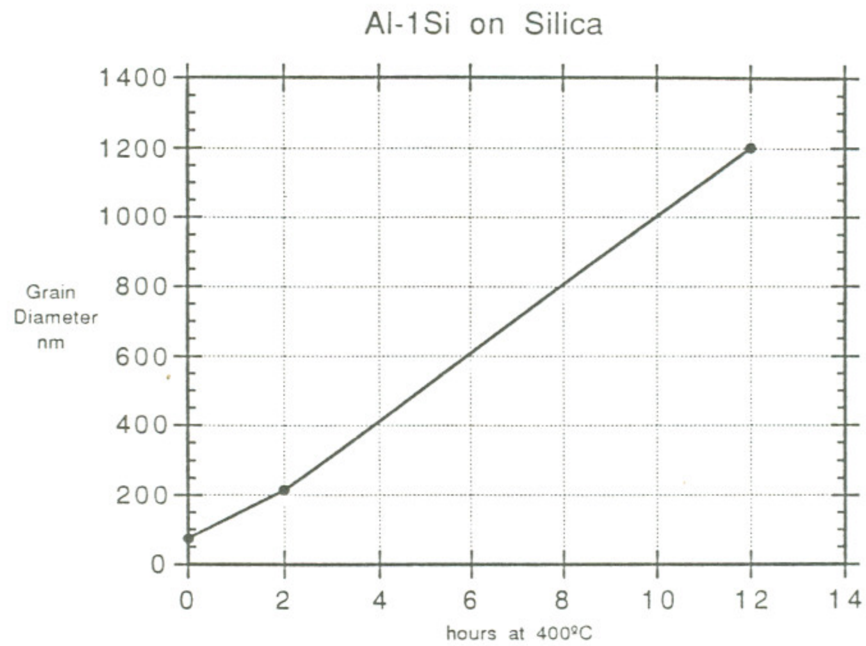


Figure 34. Al-1Si grain diameter vs. heat treatment time.

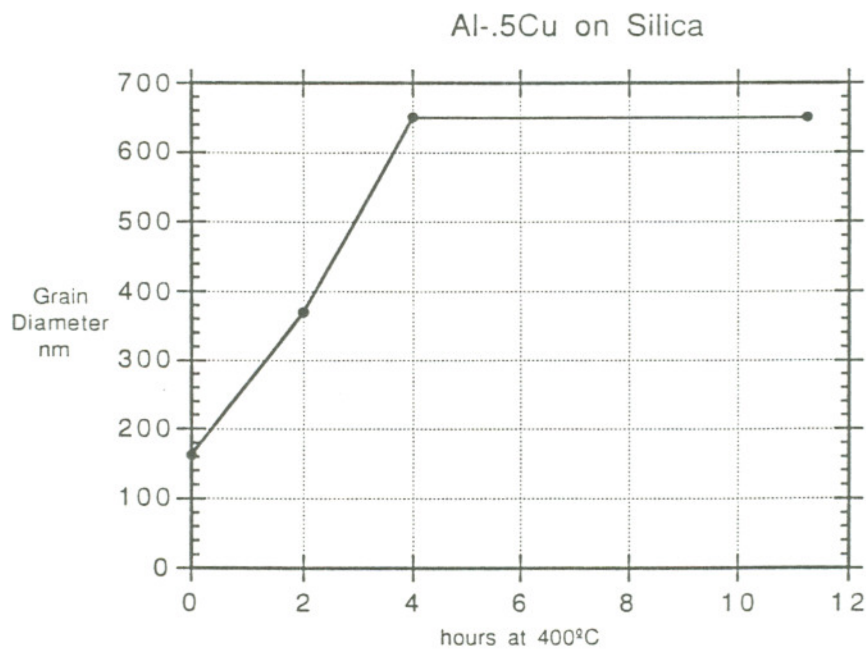


Figure 35. Al-.5Cu grain diameter vs. heat treatment time.

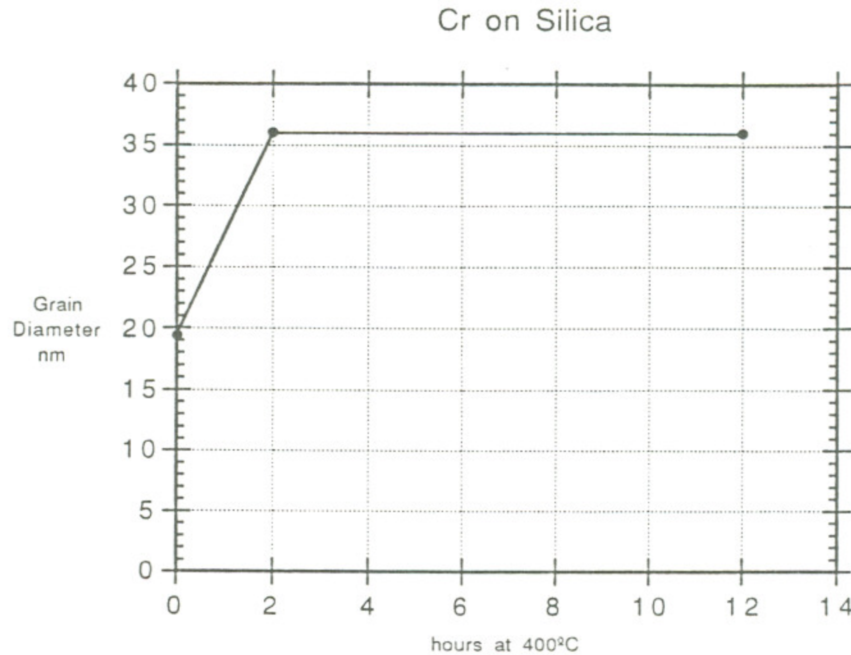


Figure 36. Cr grain diameter vs. heat treatment time.

Si diffusion depth in the first 2 hours of heat treatment is a good indicator of BVG performance. When the diffusion of the metal into the Si approaches the depth of penetration of Si into the metal then the diffusion depth loses its value as an indicator of good BVG performance. This occurs after long periods of heat treatment. The interface begins to have the concentration gradients of a Matano interface. The diffusion coefficient for the metal into the Si is much less than for the Si into the metal. If the Si diffusion depth is near 0 for 2 hrs of heat treatment at 400ºC then the BVG will be high.

Table 8. Post Heat Treatment Si Diffusion Depths into Electrodes

	A	B	C	D
1	Metallization	t @ 400ºC	x diffusion	BVG
2		hrs	nm	V
3				
4	Al-1Si	0		0.4
5		2	40	0.2
6		12	0	
7				
8	Al-.5Cu	0	0	8.2
9		2	0	7.1
10		4	15	5.1
11		11.25	9	
12				
13	Cr	0		7.4
14		2	10	7.9
15		12	10	

The silica/Si interface roughnesses(step height and frequency) do not show significant heat treatment caused changes in step heights for the electrodes for which these measurements were done. Frequency dropped from 30/100nm to 5/100nm for Ti. See table 9. The most significant heat treatment caused roughness changes at the metal/silica interface were changes in the frequency of the 1nm grain boundary steps which was inversely proportional to grain diameter. The interface within electrode grains showed little roughness for all metals. See table 10.

Table 9. Silica/Si Interface Roughness and Heat Treatment

	A	B	C	D	E
1	Metallization	t @ 400ºC	Step Height	Frequency	BVG 10% fail
2		hr	nm	#/100nm	V
3					
4	none	0	0.435	17	
5					
6	Al-1Si	0			0.4
7		2	0.6	30	0.2
8					
9	Al-.5Cu	0			8.2
10		2	0.5	12.5	7.1
11		4	0.3	5.6	5.1
12		11.25	0.4	15	
13					
14	Cr	0	0.6	12	7.7
15		2	0.5	13	8.4
16		12	0.6	8.5	
17					
18	Ti	0	0.7	29.4	6.6
19		2	0.75	5	0.2

Table 10. Electrode/Silica Interface Roughness and Heat Treatment

	A	B	C	D	E	F
1	Metallization	t @ 400ºC	Step Height	At Grain Boundary	Frequency	BVG 10% Fail
2		hrs	nm	nm	#/100nm	V
3						
4	Al-1Si	0				0.4
5		2	1.1		0.94	0.2
6						
7	Al-.5Cu	0		1	1.24	8.2
8		2		1	0.54	7.1
9		4			0.3	5.1
10		11.25		0.7	0.3	
11						
12	Cr	0			10.3	7.7
13		2			5.55	8.4
14		12			5.55	
15						
16	Ti	0			8.7	6.6
17		2		1	3.45	0.2

The Structure of SiO_2 and Resistivity

Planar sections of the 7nm silica, as deposited, heat treated without an electrode, with an Al-1Si electrode and with an Al-.5Cu electrode were examined. The oxide heat treated for 2hrs. with the Al-1Si had 1-3nm high beta quartz precipitates in the normally vitreous thin film. See figure 8a. This MOS structure failed with a BVG of 0.2V indicating a nearly complete loss of resistivity for the oxide. The increase in crystalline material in the silica decreases the breakdown voltage since the breakdown voltage for crystalline quartz is less than vitreous silica at room temperature. The quartz crystallites also introduce interfaces within the silica which are more conductive than the bulk silica.(37) The Al-.5Cu electrode maintained a high BVG of 5.1 following heat treatment for 4hrs. This oxide showed no evidence of precipitation although it did have a high Al and Cu content. As is shown by Table 11 there were changes in the nearest neighbor distances due to heat treatment and the presence of an electrode. Compared to the thermally grown dry as deposited oxide the heat treated oxides with metallizations showed considerable reductions in the nearest neighbor distances and preferential milling of the thin film in regions of high diffusion. See figures 20 and 37.

Table 11. Silica Structure and Heat Treatment

	A	B	C	D	E
1	Specimen	nearest neighbor distance	2nd	3rd	comments
2		nm	nm	nm	
3					
4	SiO_2 as deposited	0.174	0.196	0.3125±.009	fuzzy rings
5	SiO_2 +2hr@400°C	0.0814	0.123		"
6					
7	Al-.5Cu-4 SiO_2	0.123	0.219		fuzzy rings
8	low Si diffusion		0.2187		"
9			0.2187		"
10		0.112	0.2187		"
11			0.225		"
12		0.123	0.2187		"
13		0.114	0.2187		"
14		0.116	0.2187		"
15					
16	Al-1Si-2		0.2187		sharp ring
17	high Si diffusion	0.117±.01	0.174±.008	0.313±.026	fuzzy rings
18					
19	fused silica	0.162	0.265		

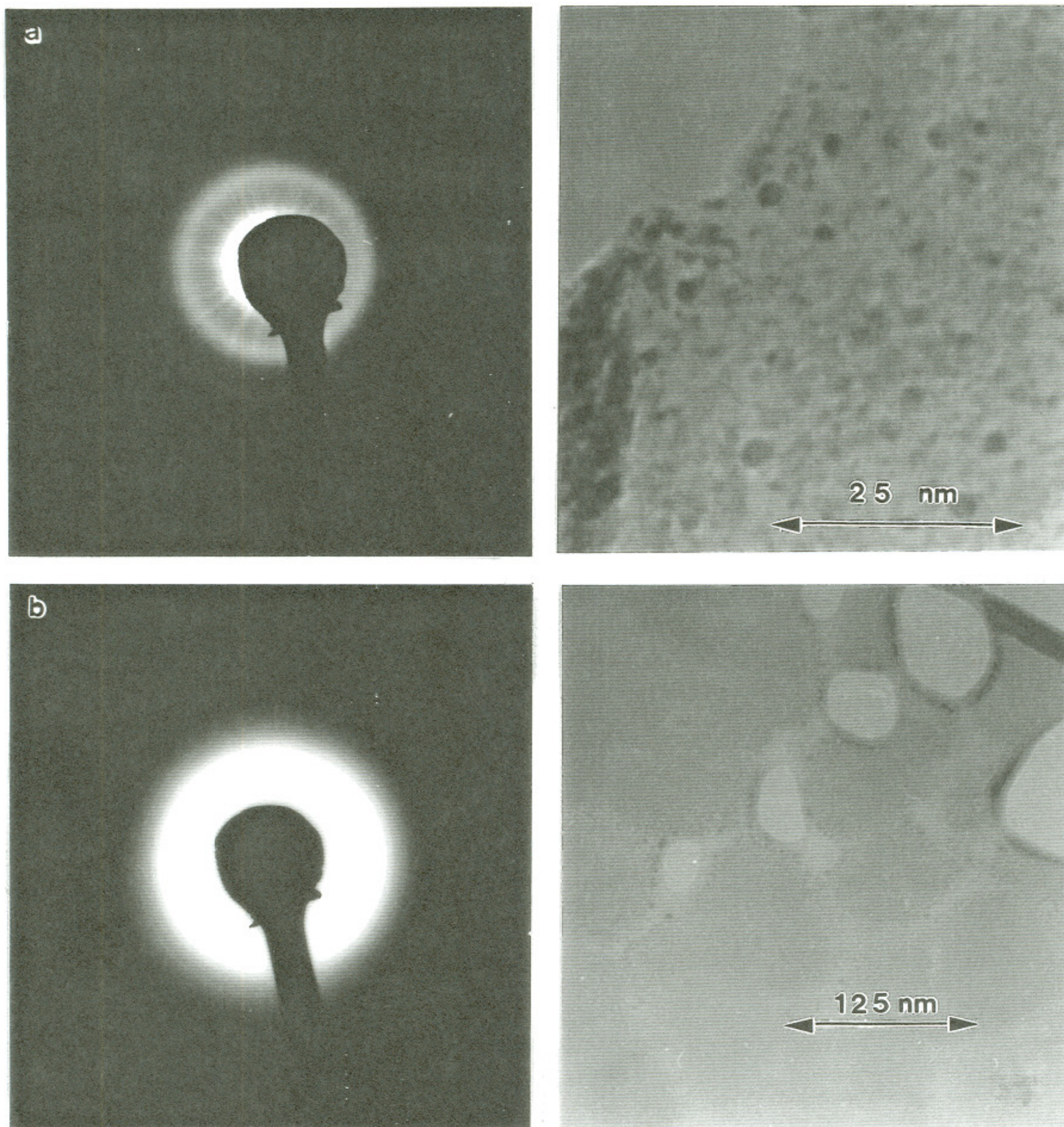


Figure 37. a. Electron diffraction pattern and bright field image for high Si flux oxide heat treated with Al-1Si. b. Same for low flux oxide heat treated with Al-.5Cu.

Si Diffusion in the SiO_2 and BVG Performance

The degree of diffusion of Si into a metallization deposited on 7nm of TCA silica is an excellent indicator of BVG performance. The total number of Si atoms that pass through the oxide will determine the damage done to the oxide. This "dose" is determined by the flux of Si atoms through the oxide which in turn is dependent on the Si diffusion coefficient first in the oxide and then any barrier layers if present and finally the metallization. This dose can be measured directly from increases in electrode thickness or integration of Si compositional profiles over the entire thickness of the metallization. The Al-1Si and Ti metallizations deposited directly on the oxide doubled their thicknesses during a 2 hour heat treatment and post heat treatment BVG measurements of 0.2 indicated a complete loss of insulating properties for these oxides. See table 2. In the absence of a diffusion barrier the flux of Si is unimpeded and the increase in the thickness of these electrodes have a linear dependence on time with a high growth rate. The electrodes that performed well such as Al-.5Cu and Cr had small increases in thicknesses following heat treatments or a parabolic growth dependence on time.

The Reduction of Si Diffusion into the Al-.5Cu Electrode

The reduction of the diffusion of Si into the Al electrodes deposited on extremely thin thermal oxide on a Si substrate when 0.5 wt% Cu is added to the Al, is the result of inverse Kirkendall segregation of this Cu at interfaces and grain boundaries until concentrations are reached where transformation to an intermetallic compound occurs. These atom currents are generated by vacancy flow (vacancy winds) to vacancy sinks such as free surfaces, grain boundaries, dislocations, interfaces and voids. The atomic flow is opposite to the vacancy flow with the element with the smallest diffusion coefficient segregating at the sink.(56) Once transformation occurs simultaneous Cu depletion of the adjacent Al matrix adds a concentration gradient driven diffusion mechanism governed by Ficke's law. Using a microprobe (1μm microanalysis volume resolution) no segregation at vacancy sinks was detected in reference 45 for the Al-Cu system. Submicron segregation would have been missed by microprobe microanalysis. Segregation of Cu to grain boundaries and interfaces was observed during TEM in-situ experiments with Al-1.5Cu thin films where μm size precipitates of Al_2Cu formed.(57) These intermetallic layers at the SiO_2 interfaces and metallization grain boundaries form a diffusion barrier that limits the Si that is taken on by the electrode. Once this barrier forms, the diffusion of Si into the Al is slowed or stopped. The compositional profiles, the planar sections and high resolution imaging show that Cu segregated at interfaces and grain boundaries to form an Al-Cu intermetallic. The diffusion coefficient of Si in a

disordered solid solution is much higher than in an ordered Al-Cu intermetallic (56) strongly suggesting that the 0.6nm reaction layer visible in figure 8 is ordered Al_2Cu as found by a search of the EDD incorporated in an electron diffraction simulation program "Desktop Microscopist". The diffusion mechanisms in this multi-layered thin film structure are determined by the crystal lattice structure, ordering, density, thickness, grain size and chemical composition of the films. The 7.0nm thick amorphous SiO_2 has diffusion coefficients for most elements comparable to surface diffusion values due to the low density and porosity of these films(25).

The diffusion of Si, Al and Cu through the SiO_2 does not cause phase changes within the SiO_2. There was however a roughening of the interfaces and consumption of the oxide due to the initial diffusion of Si into the Al-.5Cu electrode. The specimen heat treated for 4 hours had an oxide thickness of 5.6nm and reaction layers 0.6nm thick. The reaction layer at the metal/SiO_2 interface is identical in thickness and contrast to the layer at the SiO_2/Si interface. The resolution of the microanalysis in this TEM/STEM would not permit the analysis of such small volumes of material to give a positive identification of the phase present in the layers or if the phases at the interfaces were the same.

The Al-.5Cu electrode on SiO_2 used as a test electrode for the gate oxide of a submicron MOSFET shows an advantage over Al-1Si by creating its own barrier layer and "stuffing" its grain boundaries with intermetallic to limit reaction with the oxide and limit low temperature grain boundary and dislocation diffusion of Si into the

electrode. The reduction of the diffusion of Si into the metallization by the interfacial barrier layer and stuffed grain boundaries will also keep resistivity of the electrode low during fabrication.(58) This Al-Cu intermetallic layer has a higher resistivity than the bulk Al-.5Cu, dependent upon Cu content, but the 0.6nm thickness does not add significantly to the electrode resistivity. The elimination of the barrier deposition step may be possible.

Al_2Cu, Ø, is a tetragonal compound in space group I4/mcm (140) a=.607, c=.487nm and is incoherent with the Al fcc structure, space group Fm3m(225) a=.405nm, in which it nucleates and grows. The hardness is 743 Knoop and the melting point is 591ºC. Pure Al with the same loading had a Knoop hardness of 28. See Appendix 2. The usefulness of a material as a diffusion barrier depends on these macroscopic properties. Melting point is a measure of the amount of energy necessary to break all the bonds in a crystal. Hardness is also an indicator of bond strength in the lattice as well as the ease or difficulty of dislocation glide and climb.

The nucleation and growth properties of Ø in sputter deposited Al can be manipulated by changing the substrate temperature. Examination of the Al-Cu phase diagram and positive lattice misfit suggests substrate temperatures that would encourage Ø precipitation at specific sites, produce a certain degree of growth and morpholgy. The sequence of transitions in low alloy Al-Cu is G.P.1 to G.P.2 to Ø ' to equilibrium Ø Al_2Cu. The structure and morphology of G.P. 1 is a plane of Cu atoms 3 to 5nm in diameter on

(100) type planes (loop). G.P. 2 (Ø ") has an ordered, coherent tetragonal structure a few atomic layers thick with a=.404, c=.768nm. Meta-stable Ø ' has a partially coherent tetragonal structure with a =.404 and c=.580nm. (59,60)

The mechanism observed in the Al-.5Cu gate electrode suggests a new class of diffusion barriers characterized by mono or bi-layers of intermetallic at grain boundaries and interfaces. These barrier layers can be induced to form by suitably designed sputter deposition of low alloy Al followed by controlled processing. Some of the candidates for alloying with the Al in addition to Cu which may also form these intermetallic barriers include W, Ag, Zr, Mo and Cr.

The performance of metallization systems as gate electrodes can be correlated with the diffusion distance of silicon into that metallization, $(Dt)^{1/2}$, in the first 2 hours of heat treatment. As deposited Al-1Si has the poorest performance with a 10% fail at 0.4 volts. Al and Si weight percents are equal in the Al-1Si at 40nm from the interface following heat treatment for 2hrs. at 400ºC, the largest diffusion distance for the metallizations tested. Al-.5Cu is used as an interconnect conductor in ULSI devices. The specific use investigated in this study is as a gate electrode deposited directly on extremely thin 6nm SiO_2. When Al-1Si or Al-.5Cu are used as gate electrodes or ohmic connections to sources or drains in a MOSFET a conducting barrier layer of TiN or heavily doped poly-Si is usually deposited between the Al alloys and the SiO_2 or Si . The addition of this relatively high resistivity barrier layer increases the power

consumption of a MOSFET constructed with this gate electrode, increases the operating voltage necessary and decreases the frequency at which the MOSFET can be switched.(58) The heavily doped poly-Si is susceptible to dopant depletion during processing and service which leads to an increase in resistivity.(4) If a high conductivity electrode can be deposited directly on the gate oxide without decreasing the breakdown voltage or causing microstructural changes during processing at 400ºC the reduction of processing steps can be accomplished and a more power efficient and faster MOSFET can be produced.

The Microstructural Effects of Si Diffusion on the SiO_2

Immediate failure of the gate oxide following deposition of the gate electrode is usually attributed to rapid diffusion of the metal through the oxide to the oxide/silicon interface. The much greater flux of Si atoms in the opposite direction is largely ignored. This failure of the gate electrode structure is assumed to be a metallic short across the gate oxide. In TEM examinations during this research no such "wires" were found in the Al-1Si specimens that failed with or without heat treatment. In the literature the mechanism of thin gate oxide degradation during service is described in terms of total charge passed by the oxide until the breakdown voltage drops precipitously. Charge passing through the oxide creates dangling bonds by collisions with valence electrons. Again Si diffusion is not considered as a mechanism of dangling bond generation and conductivity increase for the SiO_2.

The diffusion of oxygen through Si creates Si interstitials in this covalently bonded crystalline material. These interstitials coalesce on (1 1 0) type planes to form dislocation loops. The edges of these dislocation loops have a high density of dangling bonds producing a region of higher conductivity than the bulk semi-conductor and act as a "sink" for contaminants to further increase the conductivity there. The diffusion of Si through low density thermally grown vitreous SiO_2 at elevated temperatures by a similar mechanism can cause interstitials and dangling bonds to form. The excess Si can exist as interstitials, displace oxygen or Si, or bond with the Si or O on the inner surfaces of pores. The interstitials can form loops that extend entirely through the oxide or large fractions of the oxide thickness. These nearly one dimensional zones of high conductivity in addition to the inner surfaces of pores act as low resistivity current paths through the oxide to the Si substrate. As the ratio of Si/O increases the number of dangling bonds increases and the silica conducts more and more current. Metals with a high diffusion coefficient for Si cause the flux of Si through the oxide to be high since Si at the interface is immediately depleted by the bulk of the metal.

The use of polysilicon as an electrode eliminates the gradient of the Si concentration across the silica layer which eliminates the diffusion of Si through the oxide and the associated electronic damage. The Si concentration gradient in thermally grown thin oxide has been established by Rutherford backscatter (RBS) experiments which showed the O/Si atomic ratio to vary from 1.41 at 15.8nm from the SiO_2/Si interface to 0.4 at 1.3nm. (21) Metals with a low

diffusion coefficient for Si therefore are good candidates for deposition directly on gate oxide as electrodes.

Electrode Grain Growth and BVG Performance

As deposited grain morphology and size depends on the melting point of the metal being deposited, substrate temperature, microstructure and material. If a metal is deposited on a substrate at < .2 to.3T_m a fibrous-like narrow columnar structured thin film will result. The as deposited Cr and Ti thin films, relatively high melting point metals, had this small grain fibrous structure. See figures 15 and 18 pages 53 and 58. If the deposited metal was fcc and the substrate amorphous, the film will have <111> growth preference. The as deposited low melting point Al-1Si in contrast had large columnar grains. See figure 7, page 36.

Normal grain growth is proportional to the square root of time and is described by

$$(1) \qquad R^2_{mean}-R^2_{0\ mean} = Kt, \quad K=(4¥_{g.b.}\Omega M)/\partial$$

$¥_{g.b.}$ is the grain boundary surface energy. Ω is the atomic volume. M is atomic mobility and ∂ is the grain boundary width. The driving force for this growth is the reduction of grain boundary surface area per volume to reduce the free energy in the system. Normal grain growth can occur during deposition

Once the grains in a thin film have become columnar with an average size of at least the thickness of the film, growth stops. Secondary grain growth can occur in thin films where columnar grains with low interface and surface energy grow at the expense of grains with high energy interfaces and surfaces.
Grain growth in this mode is of the form;

$$(2) \qquad R_{mean}-R_{0\ mean}= (M(2(¥_{mean}-¥)+¥_{g.b.})/X)*(t-t_o) \ (61)$$

Secondary grain growth in thin films occurs at much lower temperatures, is inversely proportional to film thickness and is controlled by the surface microstructures and energy. Grain growth can occur at temperatures as low as $0.2T_m$.

In these experiments the film thicknesses increased with heat treatment time so that film thickness, X, was of the form;

$$(3) \qquad X=kt+X_o$$

X_o= the as deposited film thickness of the metal
k= constant determined experimentally for the metal
t= heat treatment time

k was determined from X and t data from several isothermal experiments. The X dependence on t was then used in the equation. Thin metallic films on the oxide in which there were no barriers to diffusion (i.e. Al-1wt%Si) equation (3) predicted the film thickness

increase exactly. Films in which barriers did form, thickness growth ceased once the diffusion activated barriers formed(Al-.5Cu).

(4) $dR/dt=M(2(¥_s^*-¥_s)+¥_{g.b.})/X$

for Al-1Si $X(t)=60t+90$ and upon integrating (4)

(5) $R(t)=R_0+[2M(¥_s^*-¥_s)+M¥_{g.b.})/60]*[\ \ln(60t+90)-\ln 90]$

Expression (5) is the time dependence of average grain size in an Al-1wt%Si thin film with a time dependent thickness. Thickness can be increasing or decreasing due to diffusion from or into the substrate, consumed by a reaction with the substrate at the interface or with layers above the Al-1Si. This equation can also be used to describe grain growth during deposition if growth is linear. Texture in the film increases during heat treatment since surfaces with low energy are favored. A comparison of diffraction patterns produced by the as deposited Cr and Al-.5wt%Cu films and films following a 2 hour heat treatment is in figure 38. Arcs of faint spots produced by the (111) planes of both metals collapse to a single intense spot following heat treatment. This confirms the established <111> texture preference of fcc metals deposited on amorphous substrates.

The resistivity and roughness of the interfaces of the metallization are a function of grain size. The largest step heights at the metal silica interface are at grain boundaries. This is of

importance since the interface roughness adds to the unwanted parasitic capacitance. Increased roughness adds to the capacitance by increasing the surface area of the electrode.

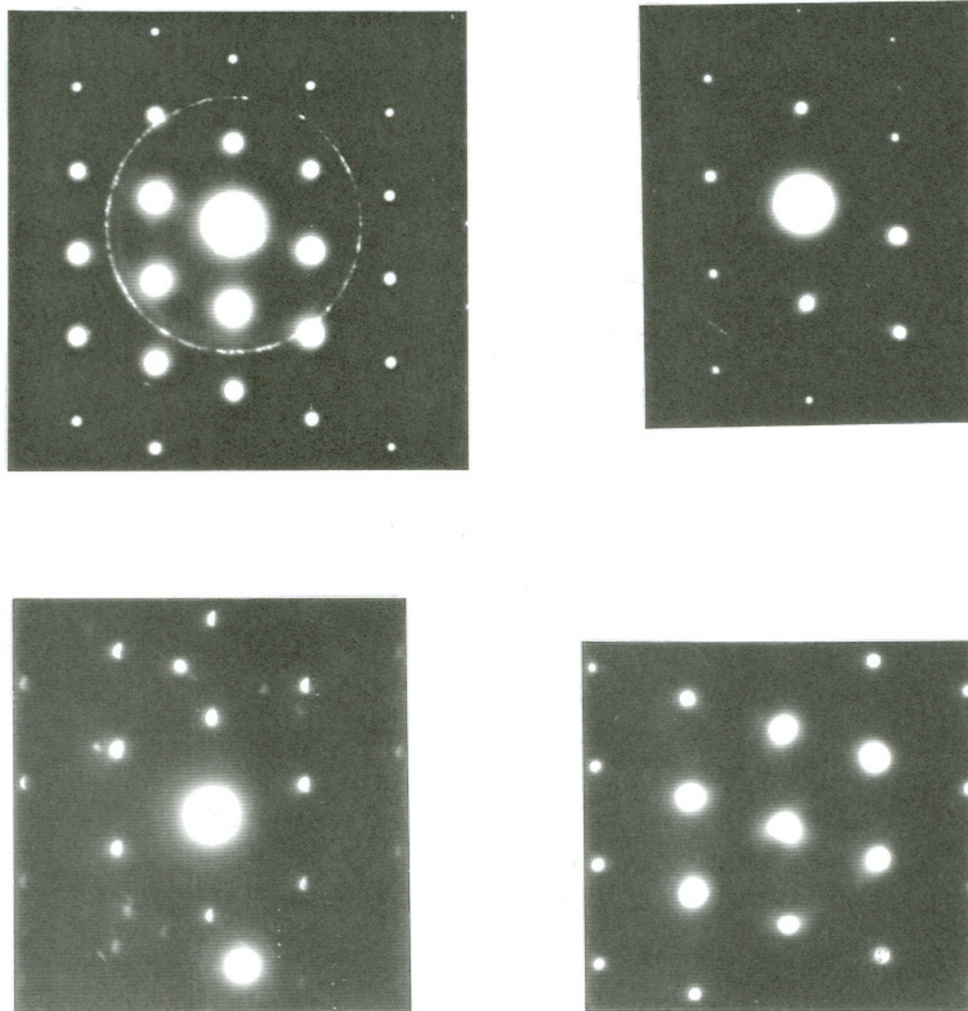


Figure 38. Selected area electron diffraction patterns showing increase in texture with heat treatment a. Cr as deposited and with 2hr of heat treatment b. Al-.5Cu as deposited and with 2hr of heat treatment

Dangling bonds at the surface of the oxide also increase due to the increase in surface area. These occupied traps add to the opposing dielectric field that diminishes the field at the Si surface. This reduction in field strength makes it necessary to operate the MOSFET at a higher voltage.

Grain growth in the Al-1Si electrode continues after 12 hours of heat treatment and is approximately 1.5 times the thickness of the growing electrode. The Al-.5Cu electrode in contrast has ceased grain growth and electrode growth at 4hrs. of heat treatment. Diffusion across grain boundaries is necessary for grain growth. The formation of an Al-Cu intermetallic diffusion barrier of sufficient thickness after 4hrs. at the grain boundaries has stopped grain growth. This intermetallic was detected during X-ray microanalysis as Cu enrichment at grain boundaries as mentioned previously.

Voids, Pores and Channels

Voids 0.6-1nm in diameter were present in the as deposited Cr grains. These voids act as scattering centers for conduction electrons, decreasing electron mobility and consequently conductivity. They are caused by vacancies or gas atoms trapped in the growing film that coalesce during sputter deposition. Coarsening of these structures to channels along grain boundaries occurs during the first two hours of heat treatment. Channels can increase resistivity and diffusion. The channels seeking minimum surface energy during subsequent heat treatments and grain growth form large pores 1-2nm in diameter within the enlarged grains.

The Effects of Si Diffusion on the Electrode

The diffusion of Si into the electrode affects several important characteristics of this thin film; the thickness of the electrode, the internal stress and the resistivity. These characteristics add to the series resistance of the MOSFET. The Al-1Si and Ti electrodes deposited directly on SiO_2 took on the greatest numbers of Si atoms. The most obvious change caused by the flow of Si into the electrodes was an increase in electrode thicknesses and these changes are compared in table 3. The high rate of growth of the Al-1Si(60nm/hr) does not appear to decrease at all even after 12 hours with a furnace cool. The Ti electrode possessed the same high growth rate. Al-.5Cu has a low growth rate of 10nm/hr for the first 4 hours and

decreases to 0 for the following 4 hours. Cr has the lowest growth rate of 5.25nm/hr but shows no indication of ceasing growth after 4 hours of heat treatment as did the Al-.5Cu.

The diffusion of Si into the Ti and Al-1Si electrodes was unimpeded since no diffusion barriers were deposited nor did any form in the electrode during heat treatment or deposition. Functions to describe the Si concentration profiles for Al-1Si and Ti electrodes presented in the results can be defined from characterization of electrode microstructure and derivations based on Fick's laws of diffusion. The complicating factors being; a thin film with an increasing thickness, increasing grain size and growth of a pure polycrystalline silicon layer on the Al-1Si electrode outer surface. Diffusion coefficients for Si in the thin SiO_2 can be determined by integrating the area under the concentration profiles to measure the total number of Si atoms that have diffused into the electrode during a given heat treatment.

Using Fick's first law and electrode thickness growth data from the isothermal experiments on Al-1Si a diffusion coefficient can be determined for the 7nm thick TCA SiO_2. The Si concentration profile for the Al-1Si electrode heat treated for 12 hours has a maximum of approximately 30wt% for 75% of the 810nm thickness and shows a SiO_2/Al interface concentration of 44wt%. The slope of the electrode thickness growth curve allows a flux to be calculated.

(6) $X_{Al\text{-}1Si} = \underline{60}t+90$ (nm, t in hours)

The volume added to the electrode /cm^2-hr is then $6x10^{-6}cm^3$ which is equivalent to a Si flux through the oxide of $2.33x10^{15}$ Si atoms/cm^2-sec or $3.89x10^{-9}$ mole/cm^2-sec and using Fick's first law.

(7) $D=-J/(dC/dx)_t$

(8) $D= 4.86x10^{-15}$ mole-cm^2/sec

The functional description of diffusion of the Si into the Al then becomes the solution for diffusion from two sources, the Si substrate via the oxide and the polycrystalline Si on the front surface of the Al-1Si electrode heat treated for 12 hours at 400ºC. Error function solutions to Fick's second law (9) with different boundary conditions predict the concentration variation with time and distance, equations 10, 11 and 12.

(9) $dC/dt=D(d^2C/dx^2)$

(10) $C(x,t)_s=C_s-(C_s-C_o)erf[x/2(Dt)^{1/2}]$ Si substrate source

(11) $C(x,t)_f=C_f-(C_f-C_{fo})erf[(X_{Al-1Si}-x\ )/2(Dt)^{1/2}]$

Al-1Si surface source

(12) $C(x,t)=C(x,t)_s+C(x,t)_f$

The Al-.5Cu and Cr electrodes, in contrast, both developed diffusion barriers, the Al-.5Cu during heat treatment and the Cr during deposition. The Al-.5Cu by the segregation of Cu to interfaces and grain boundaries formed an intermetallic barrier layer as previously described in detail. The Cr formed a dense 2nm thick Cr_2O_3 with the lowest diffusion coefficient for Si. The growth rate for the Cr electrode was 5.25 $\times 10^{-7}$cm/hr. This rate was the same for two isothermal heat treatments. The linear time dependence of thickness indicates a constant flux through the SiO_2 and Cr_2O_3. Assuming that the diffusion through the Cr_2O_3 is the slowest and controls the flux of Si into the electrode then the diffusion coefficient for the Cr_2O_3 can be determined from equation (7). The flux of Si into the Cr electrode is equivalent to 2.62×10^{16} Si atoms/cm^2-hr or 1.21×10^{-11}mole/cm^2-sec. The concentration gradient across the oxide is 1.14×10^6/cm. The diffusion coefficient then is 1.06×10^{-17} cm^2/sec. This value is two orders of magnitude smaller than the values for Al-1wt%Si and Ti.

In addition to causing changes in the metallization the flow of Si through the gate oxide causes microstructural defects that increase the conductivity of this oxide. These defects include composition change, interstitials, vacancies, disclinations and stress. This damage to the structure of the oxide increases the number density of dangling bonds which in turn increases conductivity at sites of high diffusion.

Microstructural Changes in the SiO_2 due to Heat Treatment

The effects of the 400ºC heat treatment on the oxide in an N_2 ambient included changes in thickness, short range order and composition. The oxide when heat treated without metallization more than doubled in thickness from 7nm to 15nm by continuation of the oxidation or by nitridation of the original oxide. The source of oxygen could be residual impurity oxygen in the N_2 ambient. The oxide with an Al-1Si metallization decreased from 8nm to 6.6nm following 2hrs. @ 400ºC and 6nm following 12 hours. Cr and Ti electrodes as deposited had an oxide thickness as deposited of 4.0nm indicating an immediate reaction during deposition or at room temperature post deposition that consumed nearly half the SiO_2. The Cr electrode reaction layer that formed proved stable and consumed no more oxide during subsequent heat treatments and maintained a high break down voltage. The reaction layer was a good diffusion barrier that gave the lowest electrode thickness growth rate. The Al-.5Cu electrode deposited directly on the oxide formed a reaction layer during heat treatment that limited diffusion and electrode growth. The as deposited oxide thickness of 6nm did not change following the 2hr. and 4hr. heat treatments. During the 11.25 hr. heat treatment the oxide thickness did decrease to 5nm. This also coincided with the electrode growth rate dropping to 0. The thickness of the oxide following heat treatment with metallizations decreased by a variety of mechanisms. Reaction layers consumed oxide at both the M/SiO_2 and the SiO_2/Si interfaces. Oxide only grew

when heat treated without a deposited metallization.

Short range order changed in the oxide heat treated without a metallization. In addition to the Si-O and O-O bond lengths of 0.182 and 0.306nm measured from diffraction patterns produced by the as deposited oxide, another amorphous ring was present which represented an atomic spacing of 0.082nm. This ring could represent a Si-N bond length. A planar section of the Al-.5Cu produced thin oxide from which electron diffraction patterns could be collected. This oxide was subjected to a low Si diffusion flux during room temperature periods and heat treatment temperature ramp before the intermetallic diffusion barrier transformation temperature. The oxide showed regions of damage or defects near the as deposited Al grain boundaries as previously described. There was also a change in short range order characterized by a decrease in nearest neighbor distances. The Si-O bond length decreased significantly to 0.112-0.123nm; the O-O bond length to 0.219-0.225nm. This oxide was found to be rich in Al and Cu which could explain the change in short range order and structure. The homogeneous structures visible in bright field TEM images of the ion milled as deposited and heat treated oxide without metallization is very different from the oxide heat treated with a metallization. These specimens did not eliminate Si diffusion through the oxide into the metal as is shown in figures. This diffusion was the principal agent of degradation of the oxide that caused a decrease in breakdown voltage in all but the Cr/SiO_2/Si specimen during heat treatment at 400ºC in N_2.

The structure of SiO_2 established by W.H.Zachariason (62) and confirmed experimentally by B. E. Warren (63) with X-ray diffraction was constructed of a randomly connected network (RCN) of tetrahedrons that did not fill space leaving inner surfaces and pores within the bulk of the material. In this research voids were not found to be common in these thermally grown oxides during high resolution imaging and atomic resolution imaging. The X-ray diffraction determined nearest neighbor distance was 0.162nm (Si-O bond) and 0.265nm (O-O bond) 2nd nearest neighbor distance. The as deposited silica had nearest neighbor distances comparable to this ideal structure, but after being heat treated and subjected to the diffusion of Si and metals, nearest neighbor distances decreased considerably. See table 11. This densification of the oxide increases internal stress, interstitials, structural defects and numbers of dangling bonds. These microstructural changes increase the space charge in the oxide and generally make the oxide more conductive by narrowing the bandgap and increasing the number of trapping states. Glass has a higher breakdown voltage than crystalline quartz. (55)

An attempt at measuring the magnitude of this stress caused by heat treatment and diffusion caused damage was done by measuring the deflection of the oxide film following removal of the Si substrate and metallization when producing planar sections of the 7nm oxide. Similar measurements were done on 300nm of oxide to determine stress levels by Jaccodine and Schegel.(52) See Appendix iii.

Increased stress decreases the resistivity of the oxide. As the

nearest neighbor distance decreases in a semiconductor the bandgap decreases when the Kronig-Penney approximation of the solution to Schrodinger's equation for a periodic square well potential representing a crystal lattice is applied. (38) The magnitude of this bandgap narrowing due to compressive stress $\Delta E_g=10.8x10^{-12}\Sigma_c$. Σ_c is the compressive uniaxial stress.(64) The extension of this principle to a vitreous solid such as SiO_2 with short range order and its band structure with a 9 volt band gap gives an explanation for increased conductivity in oxides in which the nearest neighbor distance has decreased. In this research oxides which were heat treated or subjected to the diffusion of Si and metal were proven to have increased stress, damage and decreased nearest neighbor distances which resulted in higher conductivity and a reduced breakdown voltage.

Interface Roughness

Sections of interface in cross-section 200nm in length were examined at high resolution to image Si lattice planes and interface with the SiO_2 to characterize roughness. The roughness dependence on scale was found to saturate above 100nm.(39) Heat treatment does not change step heights or frequency significantly for electrodes that performed well, Al-.5wt%Cu and Cr. The Al-1wt%Si had a frequency of 30/100nm following heat treatment. The Ti electrode decreased from 29 to 5 /100nm.

The metal/SiO_2 interface was also examined on this scale. The

interface with the metal was flat except at grain boundaries where 1nm ridges were measured. Each grain boundary created a step up and a step down. The frequency of such steps is determined by the grain size. See table 5 and figures.

Reaction Layers at the Interfaces

Reaction layers include diffusion zones, diffusion zones with precipitates and completely transformed continuous layers. The reaction layers are very important to the success of the oxide and metal thin films as a gate structure. Reactions on this scale must be self limiting and have products that are stable with low diffusion coefficients. Completely transformed continuous layers are most effective as diffusion barriers.

The Al-.5Cu and Cr electrodes formed reaction layers that acted as stable continuous diffusion barriers for up to 12 hrs. at 400ºC in N_2. The Cr formed a continuous Cr_2O_3 layer by reaction with the SiO_2 during deposition which changed very little during heat treatment without further reaction with the SiO_2. This reaction layer has a low diffusion coefficient for Si and Cr and maintained a high BVG with only 4nm of SiO_2 remaining. The Al-.5Cu did not react with SiO_2 but formed an Al-Cu intermetallic at interfaces. This layer was continuous and stable but did not form until heat treatment induced Cu segregation occurred at interfaces. Growth of this reaction film continued for up to 11.25hrs. when it was 1.0nm thick.

At this intermetallic barrier thickness, electrode thickness growth due to Si diffusion stopped.

The advantage of films formed by these solid state reactions dependent on solid state diffusion for mixing is that they are continuous with no pores or pin holes as is possible with vapor deposition techniques. The reactions in both cases are self limiting. The Cr + SiO_2 reaction product Cr_2O_3 eliminates the diffusion of Cr into the SiO_2 forming a barrier to the mixing of the reactants which stops any further reaction beyond a few atomic layers. The Al-.5Cu does not react with the SiO_2 to form any new crystalline phases. The oxide is not consumed but acts as a diffusion pathway since the intermetallic is forming at both SiO_2 interfaces. When the intermetallic layer reaches 0.8nm Si diffusion ceases. The limit to this slow reaction which does not stop at 11.25hrs. is the low wt% of Cu in the alloy so that there is a limit to the volume fraction that can be transformed.

In addition to regions that have actually changed crystal structure, diffusion zones where phase changes did not occur were also considered reaction layers. These diffusion zones are regions characterized by changed composition, increased point, line and planar defects, changed lattice parameters and increased stress. The electrical and mechanical properties of the oxide and metal are effected by these defects and changes. Examples of such zones included the 20nm precipitation zone in the Al-1wt%Si heat treated for 2hrs. and the entire oxide film.

Summary

Breakdown voltage measurements before and following heat treatment show that Cr and Al-.5wt%Cu provide the highest BVG for the metallizations deposited directly on the 7nm gate oxide in this research. Al-1wt%Si had the poorest performance with a BVG of 0.4V before and 0.2V following heat treatment. Comparisons of microstructures and BVG measurements of these electrodes for the 2hr. heat treatments and extended heat treatments provide the basis for proposed mechanisms of oxide degradation and diffusion barrier formation.

There were electrode thickness increases during heat treatment for all metals deposited directly on the oxide in this test matrix due to Si diffusion from the substrate through the oxide and into the electrode. Metals deposited on poly-Si performed well. A poly-silicon layer acts as a barrier layer which eliminates the Si concentration gradient across the gate oxide into the metal which consequently eliminates Si diffusion across the oxide.

Metal diffusion into the oxide occurs without destroying its insulating properties. The Al-.5wt%Cu electrode heat treated for 4hrs. showed high concentrations of Al and Cu in the oxide and an Al-Cu intermetallic at the SiO_2/Si interface but still maintained a BVG of 5.1V. The volume of metal diffusion into the substrate was much less than the diffusion of Si into the electrode. This eliminates metal diffusion as the most important mechanism of oxide

degradation and leaves the high flux of Si through the oxide as a major agent of damage and the reduction of resistivity during heat treatment.

The metallizations used in this research consumed the Si substrate when deposited directly on 7nm of oxide. The insoluble SiO_2 sinks into the substrate as mass is moved from the substrate side of the oxide to the metal side. This process, which at best changes operating characteristics of the device by changing junction depth was slowed by adding a diffusion barrier to the electrode. Diffusion barriers in this research included polysilicon, Cr_2O_3 which forms during Cr deposition and heat treatment produced Al_2Cu intermetallic.

This research proposes a new mechanism of diffusion barrier formation in low alloy metals. The diffusion barrier forms by segregation of the low alloy solute to the SiO_2/Si and the metal/SiO_2 interfaces. Al-.5wt%Cu formed an Al-Cu intermetallic diffusion barrier layers at grain boundaries and interfaces a few atomic layers thick during heat treatment. This is a self-limiting solid state reaction that produces a continuous film that reduces very little oxide. Between 2 and 4 hours of heat treatment in N_2 these intermetallic barriers are thick enough to eliminate diffusion between the Si substrate and the electrode so that electrode thickness growth stops. Diffusion of atoms between grains is also eliminated by the intermetallic grain boundary barriers so that grain growth stops.

In addition to changes in the electrodes there were significant

changes in the structure and composition of the oxide. Nearest neighbor distances decreased during heat treatment and the metal content increased. Regions of high damage were preferentially ion milled that coincided with the as deposited electrode grain boundaries. Increased stress in the oxide was detected following heat treatment. When the Si substrate and the electrode are removed leaving a planar section of just the oxide, the originally flat layer of SiO_2 on the now missing (100) Si extends to form a concave surface indicating a release of stress.

The problem of producing effective gate electrodes for sub-micron MOSFETS reduces to producing effective diffusion barriers to isolate and stabilize structures. The effectiveness and perfection of these barriers demanded by reduced dimensions and low melting point high conductivity metal electrodes requires that they be produced by a solid state reaction that eliminates all rapid diffusion paths. A metallization is desirable that forms its own diffusion barrier without the deposition of a high resistivity barrier layer by chemical or physical vapor deposition.

7. CONCLUSIONS

The goal of this work was to identify metallizations for direct deposition on 7nm of thermal SiO_2 without reduction of the BVG during heat treatment for use in thin film MOS gate oxide test electrodes during the fabrication of sub-micron MOSFETs. This requires a basic understanding of the mechanisms of resistivity reduction for the gate silica during heat treatment with a directly deposited electrode.

The major mechanisms of oxide break down voltage reduction during heat treatment are consumption of the oxide by a reaction with the electrode, the diffusion of substrate Si through the oxide into the electrode and the diffusion of metal into the oxide.

This research found that the diffusion of Si from the substrate into the metal electrode during thermal processing is a major agent of microstructural damage to the originally vitreous SiO_2. This damage; smaller nearest neighbor distances, increased numbers of dangling and weakened bonds, increased metal content and the formation of nanocrystallites of high quartz in the vitreous silica results in lower resistivity and therefore a lower BVG.

The elimination of Si diffusion through the silica so that a high BVG is maintained can be accomplished by the choice of a metal with a low diffusion coefficient for Si such as W or the deposition of a

diffusion barrier such as TiN. Sputtered low alloy metallizations such as Al-.5Cu which during heat treatment form intermetallic diffusion barriers by solute segregation at the sites of rapid diffusion such as interfaces and grain boundaries, maintain a high BVG during heat treatment. Soft low melting point metals such as Al with high conductivities (see table 1) that form hard ordered intermetallics with high melting metals such W or Cr can be used to form stable gate electrodes with low power requirements. The interfacial nanoscale intermetallic diffusion barriers can be synthesized by co-sputtered stoichiometry or caused to form by suitably designed heat treatment segregation.

The reaction of thin film metal with the oxide as predicted by the difference of the heats of reaction of the reactants and products can be misleading as an indicator of poor BVG performance. Cr, which was predicted to react with the SiO_2, did not consume the oxide to degrade the BVG but formed a diffusion barrier with the Cr_2O_3 product to eliminate further reaction by eliminating mixing. A self limiting reaction with the oxide that forms a diffusion barrier can be an advantage in a metallization system since this maintains a high BVG during heat treatment and provides good adhesion to the oxide. Possible gate electrodes should include those metals that have a limited reaction with the oxide to form a stable adherent product that acts as a nanoscale diffusion barrier.

REFERENCES

1. Pramanik D., Jain V., Solid State Technology **34**(5)(1991)p.97.

2. Brews J.R., Nicollian E.H., *MOS Physics and Technology* , Wiley N.Y.(1982).

3. Gibson J.M., Dong D.W., Solid State Science and Technology **127**(12)(1980)p.2722.

4. Downey S.W., et. al. , J. Vac. Science Tech. B **13**(2)(1995)p.167.

5. Natan M., J.Vac.Sci.Technol.B**4**(6)(1986)p.1404.

6. Pretorius R., Harris J.M., Nicolet M-A., Solid State Electronics **21**(1978) p.667.

7. Brown D.M. et al. , Solid State Electronics **11**(1968)p.1105.

8. Engeler W.E., IEEE Trans. on Electron Devices, ED-**19** No. 1 (1972)p.54.

9. Seichi Iwata et. al. ,IEEE Trans. on Electron Devices, ED-**31** no. 9(1994)p.1174.

10. Noguchi T. et. al. , Symp. on VLSI Techn. , Digest of Papers, Japan Soc. of Appl. Phy., San Diego (1986)p.19.

11. Naoki Kasai et. al. , IEDM Tech. Dig.(1988)p.242.

12. Hideaki Matsuhashi et. al., Extended Abstracts of the 21st Congress on Solid State Devices and Materials, Tokyo, (1989)p.17.

13. N.Yamamoto et. al., J.Electrochem. Soc. : Solid State Science and Technology, **133** no.2 (1986)p.401.

14. Shah P.L., IEEE Trans.on Electronic Devices, ED-**26**, no. 4 (1979)p.631.

15. Hillenius S.J. and Lynch W.T.,IEEE Intl. Conf. on Computer Design:VLSI in Computers, Port Chester N.Y., IEEE Computer Press (1985).

16. Wickersham C.E. et. al. ,J.Vac.Sci.Tech. B**4**(6), Nov/Dec(1986).

17. Irene E.A., CRC Critical Reviews in Solid State and Materials Sciences, **14**(2) (1988)p.175.

18. Schuegraf K., Chenming Hu, Semiconductor Science and Technology **9**(1994) p.989.

19. Gibson J.M., Dong D.W., J. Electrochem. Soc. :Solid State Sc. and Tech. **127** No.12(1980)p.2722.

20. Mackowiak J., Ellingham diagram provided by British Iron and Steel Research Association printed in *Physical Chemistry for Metallurgists* , George Allen and Unwin LTD, London (1966).

21. Sigmon T.W., Chu W.K. et al. ,Appl. Phys. Lett. **24** (1974)p.105.

22. Raider S.I. and Flitsch R., J. Vac. Technol. **13**(1976)p.58.

23. Helms C.R., J. Vac. Sci. Technol. **16**(1979)p.608.

24. Grunthaner P.J.et al., J.Vac. Sci. Technol. A**4**(1979) p.916.

25. Irene E.A., J. Electrochem. Soc. : Solid State Science and Tech., **125** No. 10(1978) p.1708.

26. Rosencher E., Straboni A., Rigo S. and Amsel G., Appl. Phys. Lett. **34**(1979) p.254.

27. Rigo S., Rochet F., Agius B. and Straboni A., J. Electrochem. Soc., **129**(1982)p.867 .

28. McBrayer J.D., "Diffusion of Metals in SiO_2" dissertation Stanford(1984).

29. Irene E.A., J. Appl. Phys. **54**(1983) p.5416.

30. Revesz A.G. and Evans R.J., J. Phys. Chem. Solids **30**(1969)p.551.

31. Pliskin W.A., IBM J. Res. Dev. **10**(1966)p.198.

32. Deal B.E. and Grove A.S., Appl. Phys. **36**(1965)p.3770. .

33. Nelson D.R., Phy. Rev. Lett. **50**(1983)p.982; Phy.Rev. B **28** (1983)p.5515.

34. Shewmon P.G., *Transformations in Metals* , McGraw-Hill, N.Y.(1969).

35. Borg R.J. and Dienes G.J., *Introduction to Solid State Diffusion* , Academic Press, N.Y., (1988)

36. Nicolet M-A.,Bartur M., J. Vac. Sci. Technol.**19**(3) Sept/Oct(1981).

37. Matare H.F., *Defect Electronics in Semiconductors* , Wiley Interscience, N.Y., (1971).

38. Bube R.H., *Electrons in Solids* , Academic Press, N.Y.(1981).

39. Tatsuo Yoshinobu et al. , Jpn. J. Appl. Phy. **33**(1993)p.383.

40. Maasaki Niwa et. al., JJAP series 4, Proceedings Intern. MicroProcess Conf. (1990).

41. Maasaki Niwa et. al., Jpn. J. Appl. Phys. **33**(1994)p.388.

42. Beyers R., Mat. Res. Soc. Proc. **47**(1985)p.143.

43. Condon and Odishaw, *Handbook of Physics* , Mcgraw-Hill, N.Y.,(1967).

44. Lenzlinger M. and Snow E.H., J. Appl. Phys. **40**(1969)p.278.

45. Welland M.E.,Murrell M.P., Scanning **15**(1993) p.256.

46. Williams D.B., *Practical Analytical Electron Microscopy In Materials Science* , Phillips Electronic Instruments Inc., Mahwah N.J.(1984).

47. Eddington J.W., *Practical Electron Microscopy* , N.V. Philips Gloeilampenfabrieken, Eindhoven (1976).

48. Buseck P.R., Cowley J.M., Eyring L. ,*High Resolution Transmission Electron Microscopy* , Oxford Press, N.Y.(1988).

49. Mc Carthy J.M. and Thomas L.E., Proc. of the 43rd Ann. Mtg. of EMSA, San Francisco Press, San Francisco, CA(1985)p.184.

50. Bassile D.P., Boylan R., et al, Mat. Res. Soc. Symp. Proc. **254**(1992)p.23 .

51. Frear D.R., Sanchez J.E., et.al., Metall. Trans. A **21**(1990)p.2449.

52. Jaccodine R.J., W.A.Schlegel, J.Appl.Phys. **37**(1966)p.2429.

53. EerNisse E.P., Appl. Phys. Lett. **35**(1979)p.8.

54. Murarka S.P., J. Appl.Phys. **54** (1983)p.2069.

55. Von Hippel A. and Maurer R.J. , Phy. Rev. **59**(1941) p.820.

56. Anthony T.R., *Diffusion in Solids: Recent Developments* , Academic Press, (1975) p.353 .

57. Park M. , Krause S.J., Appl. Phys. Lett. **64**(6)(1994) p.721 .

58. S.Kohyama, *Very High Speed MOS Devices* , Clarendon Press Oxford,1990.

59. Hatch J.E. , *Aluminum Properties and Physical Metallurgy* , ASM, p143.

60. Massalski T.B., *Binary Alloy Phase Diagrams,* ASM International, Al-Cu (1990) p141.

61. Thompson C.V., *Annual Review of Materials Science* (1990)p.245.

62. Zachariasen W.H., J.Am.Chem.Soc. **54**(1932) p384, J.Chem.Phys. **3**(1935) p.162, Glastech. Ber. **11**(1933)p.120.

63. B.E.Warren,Krutter H., Morningstar O., J.Am.Ceram.Soc **19**(1936) p.202.

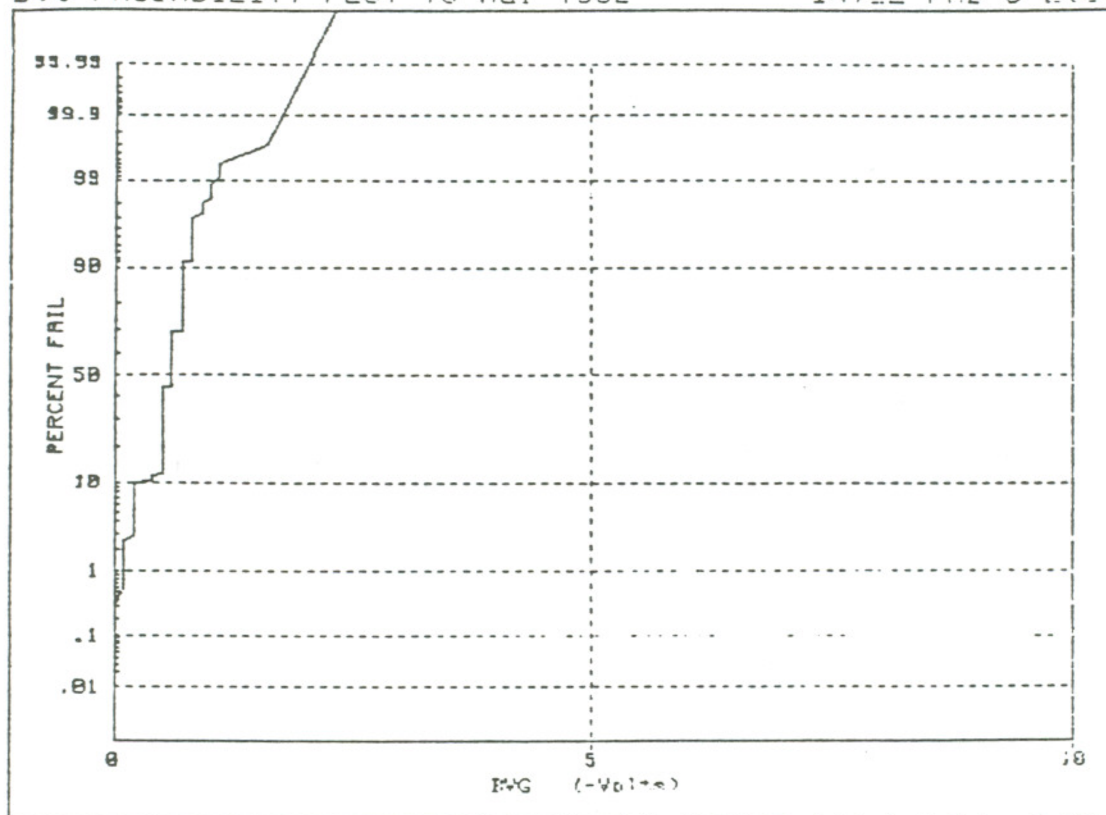
64. R.B.Fair, J.Appl.Phys. **50**(1979)p.860.

65. van Gurp, et. al. , J. Appl. Phys. **50**(11)(1979) p.6915 .

APPENDIX I

BREAKDOWN VOLTAGE GATE OXIDE MEASUREMENTS HISTOGRAMS , PROBABILITY PLOTS AND WAFER MAPS

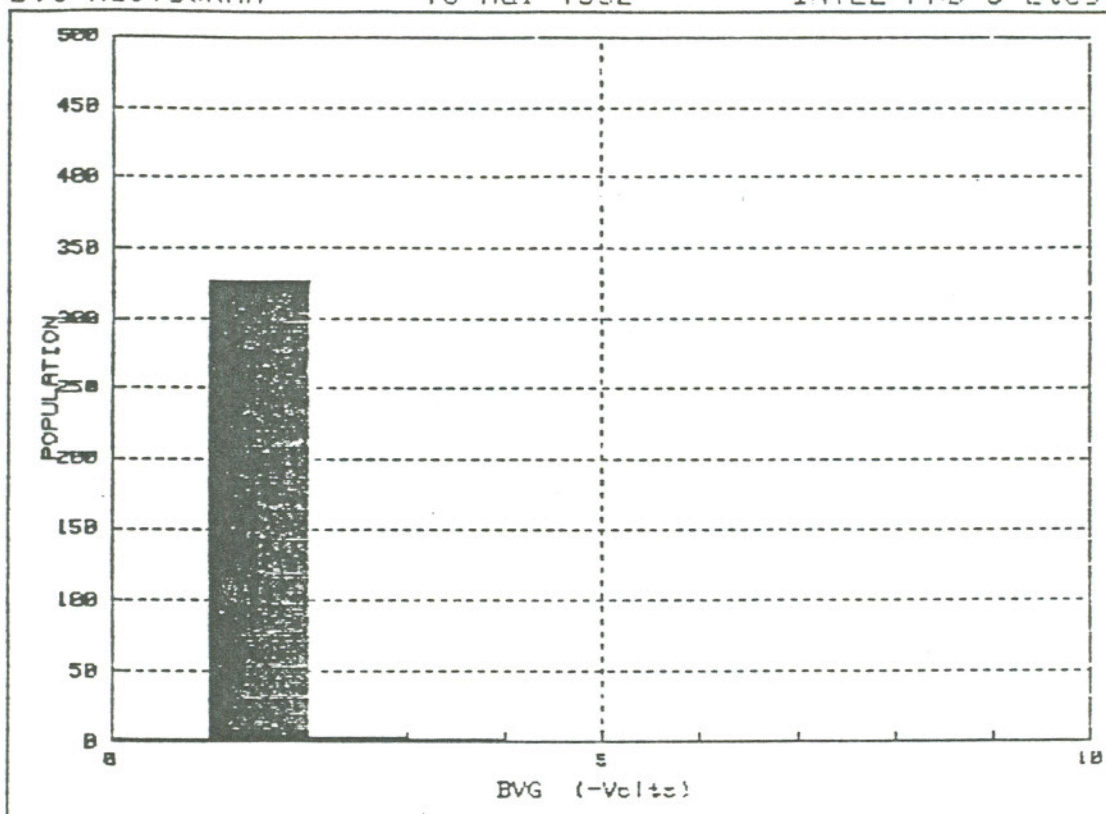
BVG PROBABILITY PLOT 18 Mar 1992 INTEL FAB 5 Etest



10%: .2
50%: .6
90%: .7

Lot#: 52108860 1 Wafers: 332 Points .2000 CM2

AlSi Dots Anneal



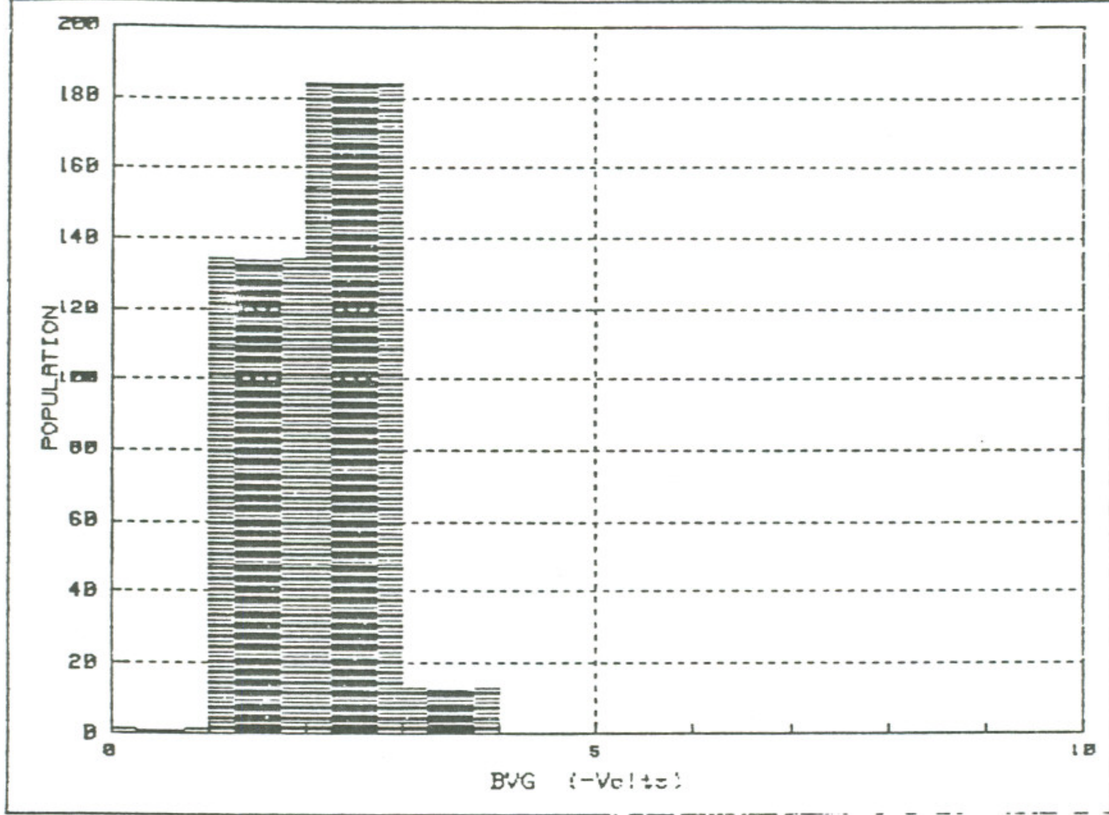
DEFECT DENSITY:
BVG < 1 : 22.09 cm.-2
BVG < 5.625 : 29.03 cm.-2

% TAILS:
.9036 %

Lot#: 52108860 332 Points 1 Wafers .2000 CM2

AlSi Dots Anneal

BVG HISTOGRAM 18 Mar 1992 INTEL FAB 5 Etest



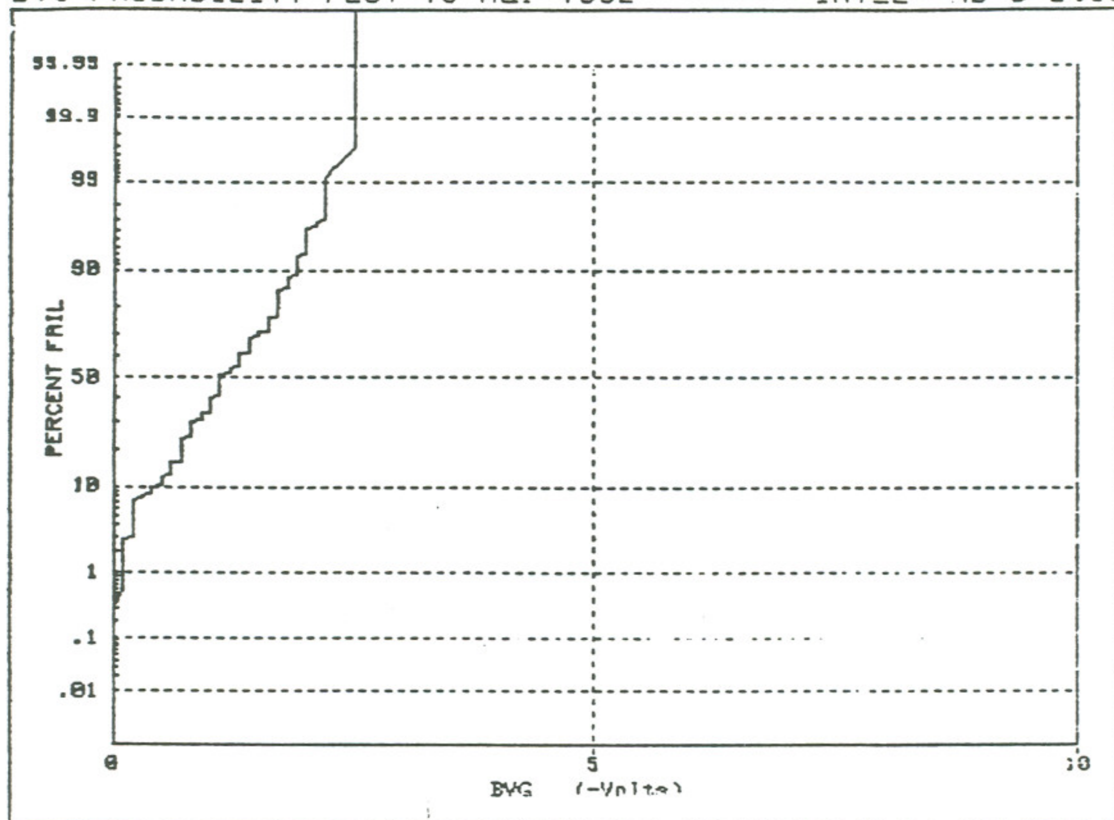
DEFECT DENSITY:
BVG < 1 : 2.61 cm.-2
BVG < 5.625 : 29.03 cm.-2

% TAILS:
59.04 %

Lot#: 52108860 332 Points 1 Wafers .2000 CM2

AlSi Dots

BVG PROBABILITY PLOT 18 Mar 1992 INTEL FAB 5 Etest

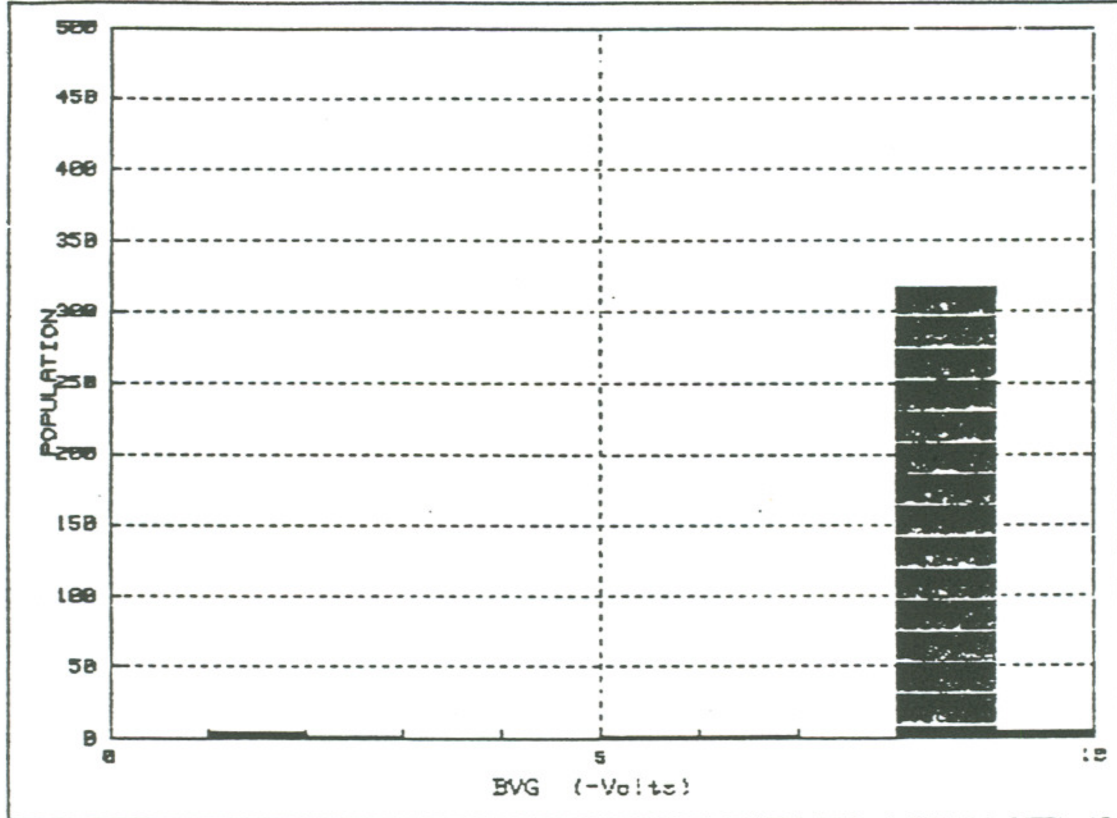


10%: .4
50%: 1.1
90%: 1.9

Lot#: 52108860 1 Wafers: 332 Points .2000 CM2

AlSi Dots

BVG HISTOGRAM 18 Mar 1992 INTEL FAB 5 Etest

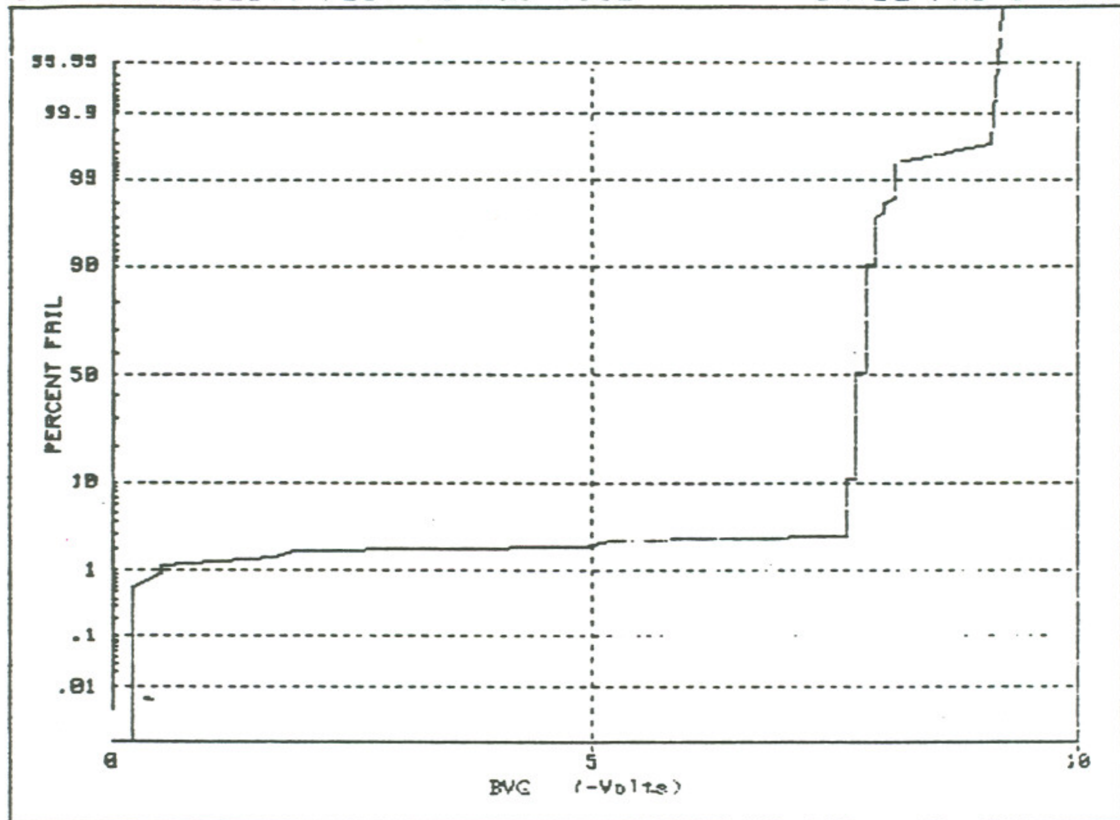


DEFECT DENSITY:
BVG < 1 : .06061 cm.-2
BVG < 5.625 : .122 cm.-2

% TAILS:
1.205 %

Lot#: 52108860 332 Points 1 Wafers .2000 CM2

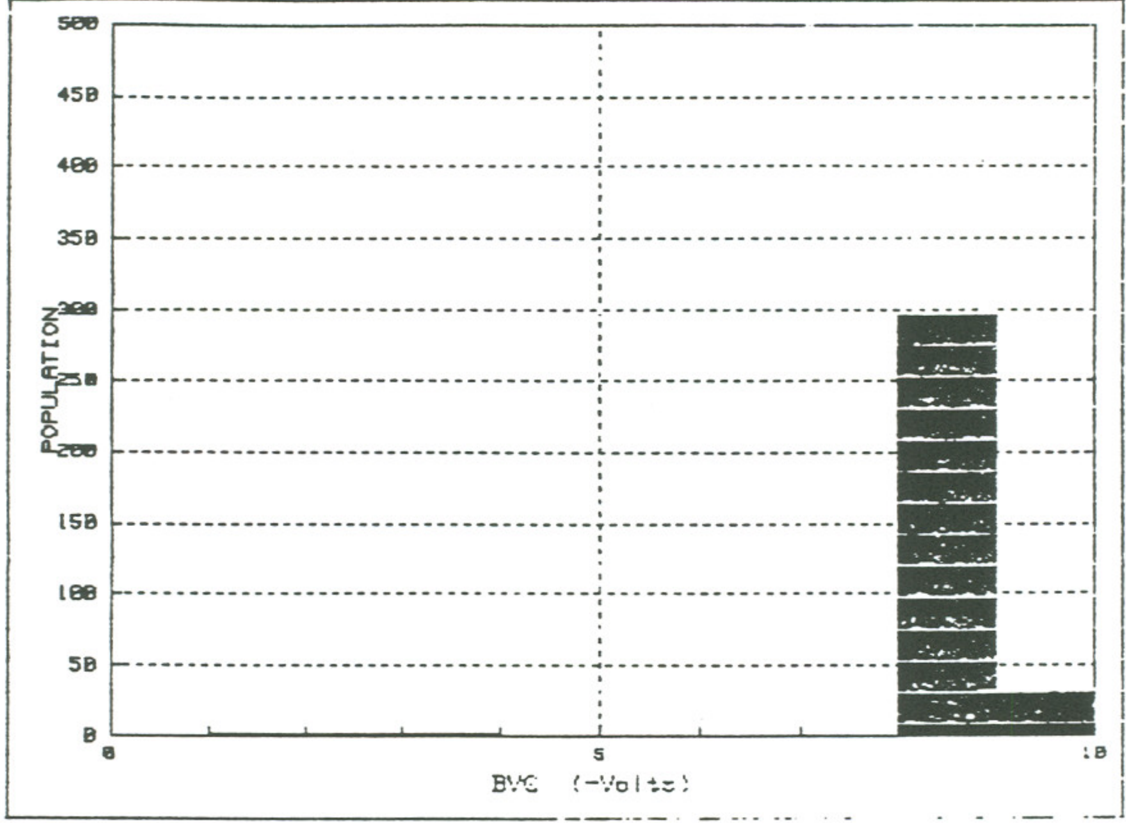
Poly AlSi Dots Anneal



10%: 7.6
50%: 7.7
90%: 7.8

Lot#: 52108860 1 Wafers: 332 Points .2000 CM2

Poly AlSi Dots Anneal



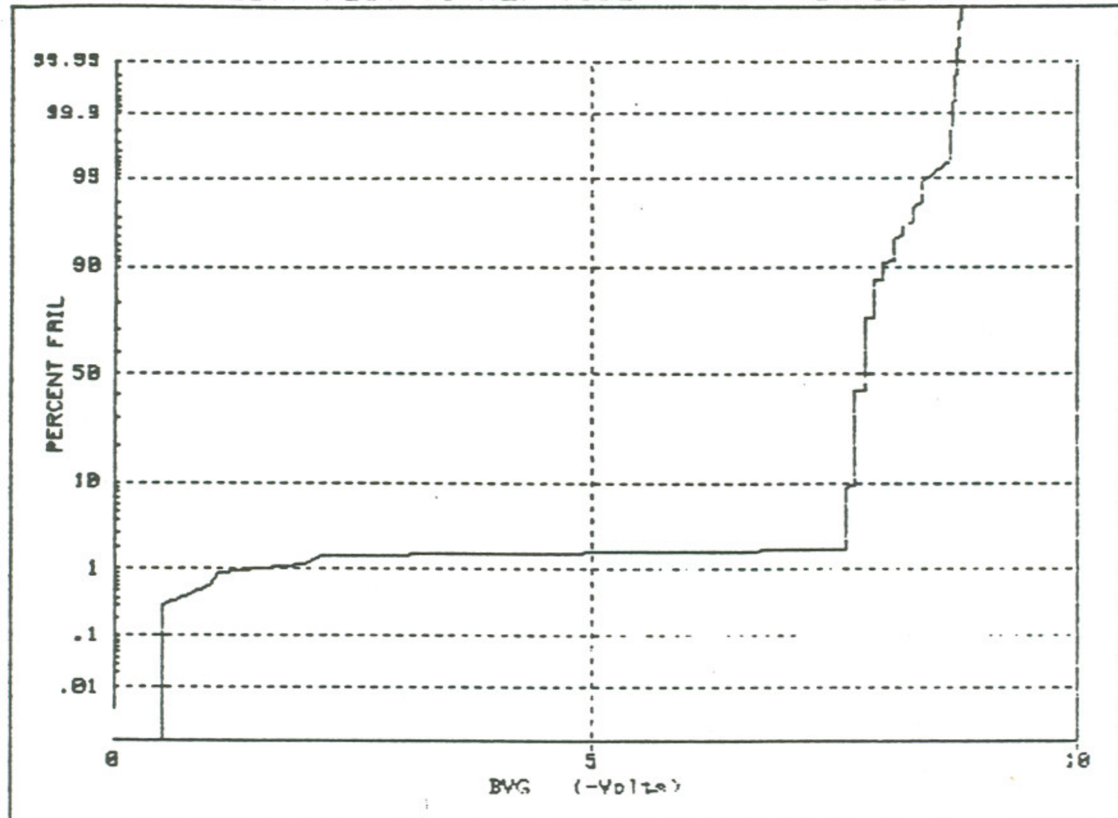
DEFECT DENSITY:
BVG < 1 : .03021 cm.-2
BVG < 5.625 : .07587 cm.-2

% TAILS:
.9036 %

Lot#: 52108860 332 Points 1 Wafers .2000 CM2

Poly AlSi Dots

BVG PROBABILITY PLOT 18 Mar 1992 INTEL FAB 5 Etest

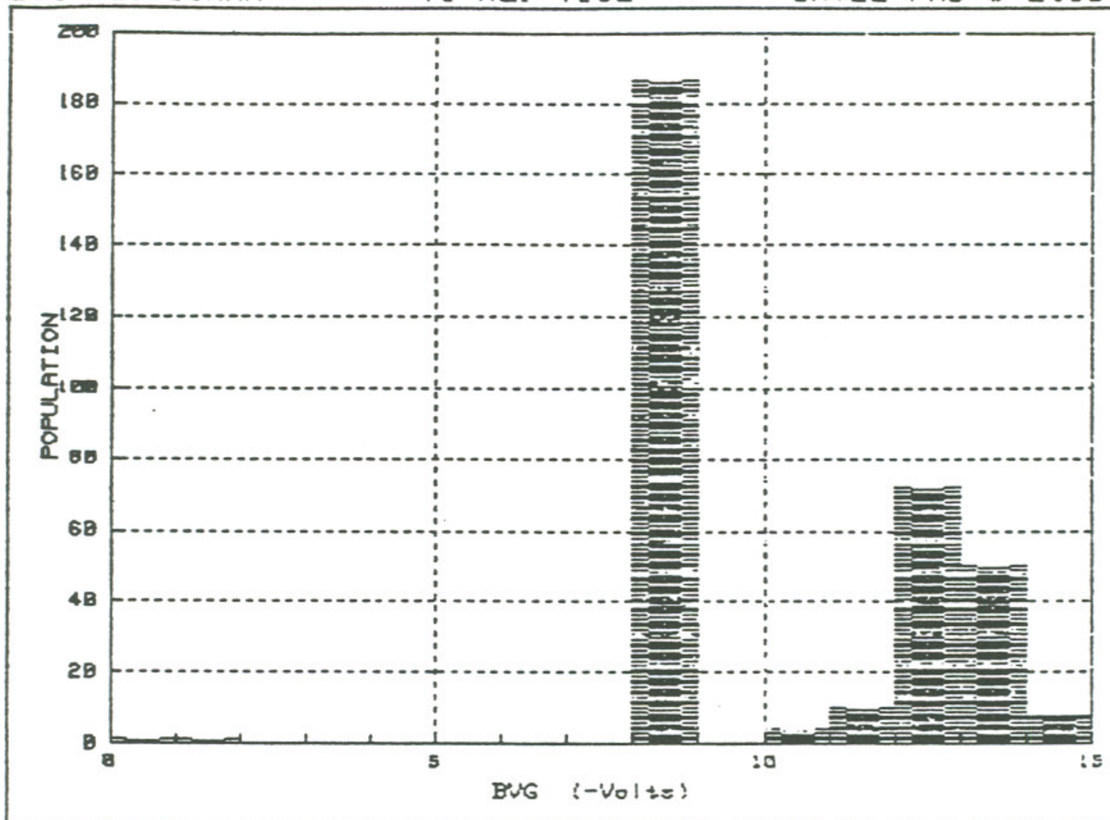


10%: 7.7
50%: 7.8
90%: 8

Lot#: 52108860 1 Wafers: 332 Points .2000 CM2

Poly AlSi Dots

BVG HISTOGRAM 18 Mar 1992 INTEL FAB 5 Etest



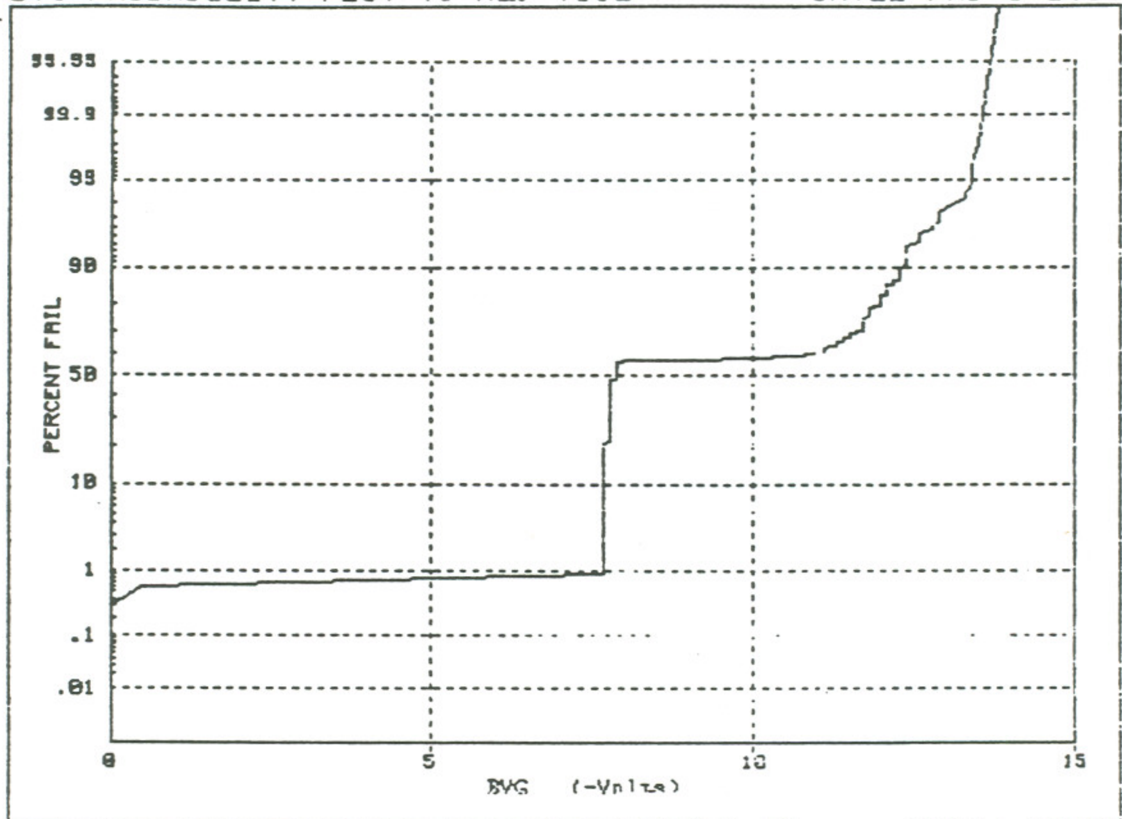
DEFECT DENSITY:
BVG < 1 : .03021 cm.-2
BVG < 5.625 : .03021 cm.-2

% TAILS:
0 %

Lot#: 52108860 332 Points 1 Wafers .2000 CM2

Poly AlCu Dots Anneal

BVG PROBABILITY PLOT 18 Mar 1992 INTEL FAB 5 Etest

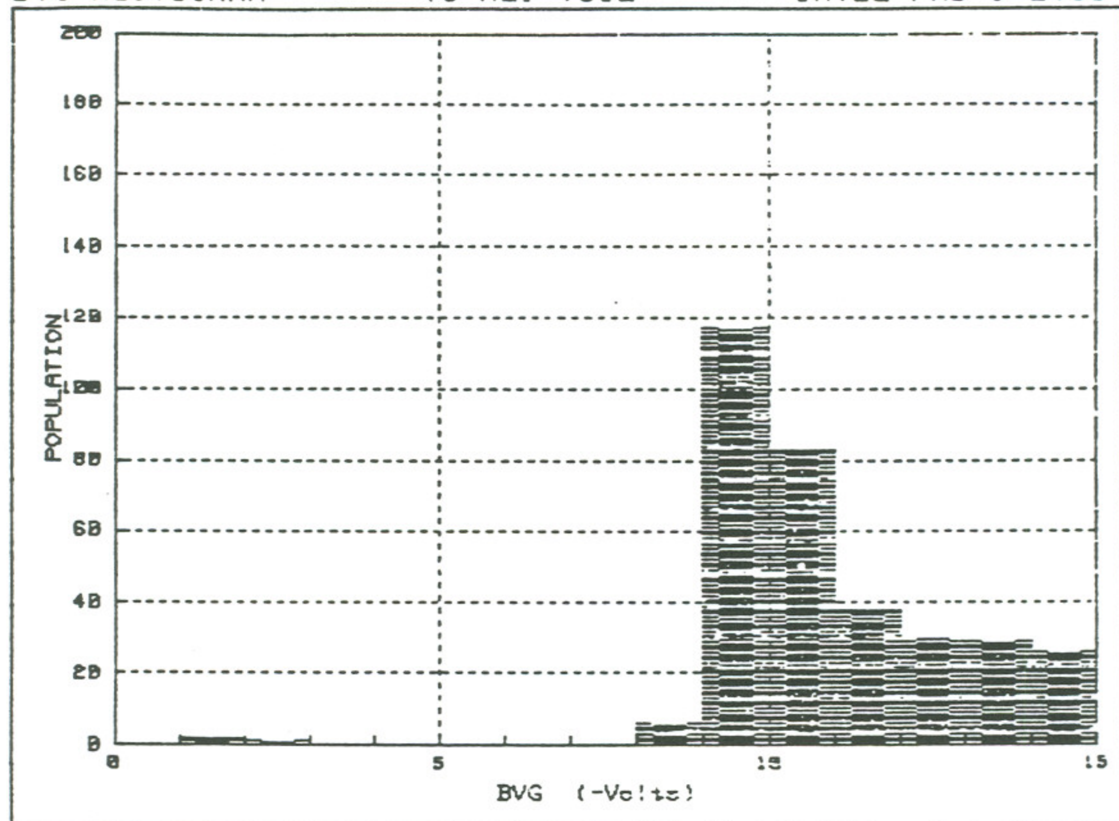


10%: 7.7
50%: 7.9
90%: 12.3

Lot#: 52108860 1 Wafers: 332 Points .2000 CM2

Poly AlCu Dots Anneal

BVG HISTOGRAM 18 Mar 1992 INTEL FAB 5 Etest



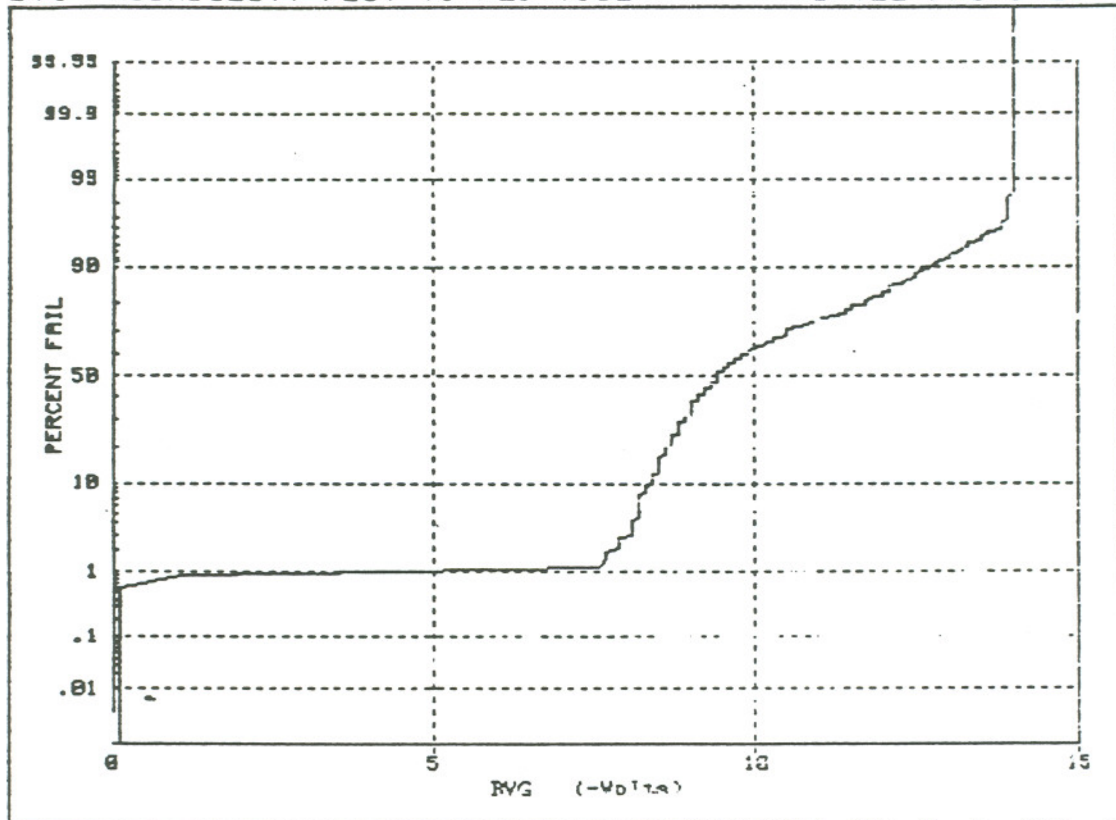
DEFECT DENSITY:
BVG < 1 : .03021 cm.-2
BVG < 5.625 : .04539 cm.-2

% TAILS:
.3012 %

Lot#: 52108860 332 Points 1 Wafers .2000 CM2

Poly AlCu Dots

BVG PROBABILITY PLOT 18 Mar 1992 INTEL FAB 5 Etest

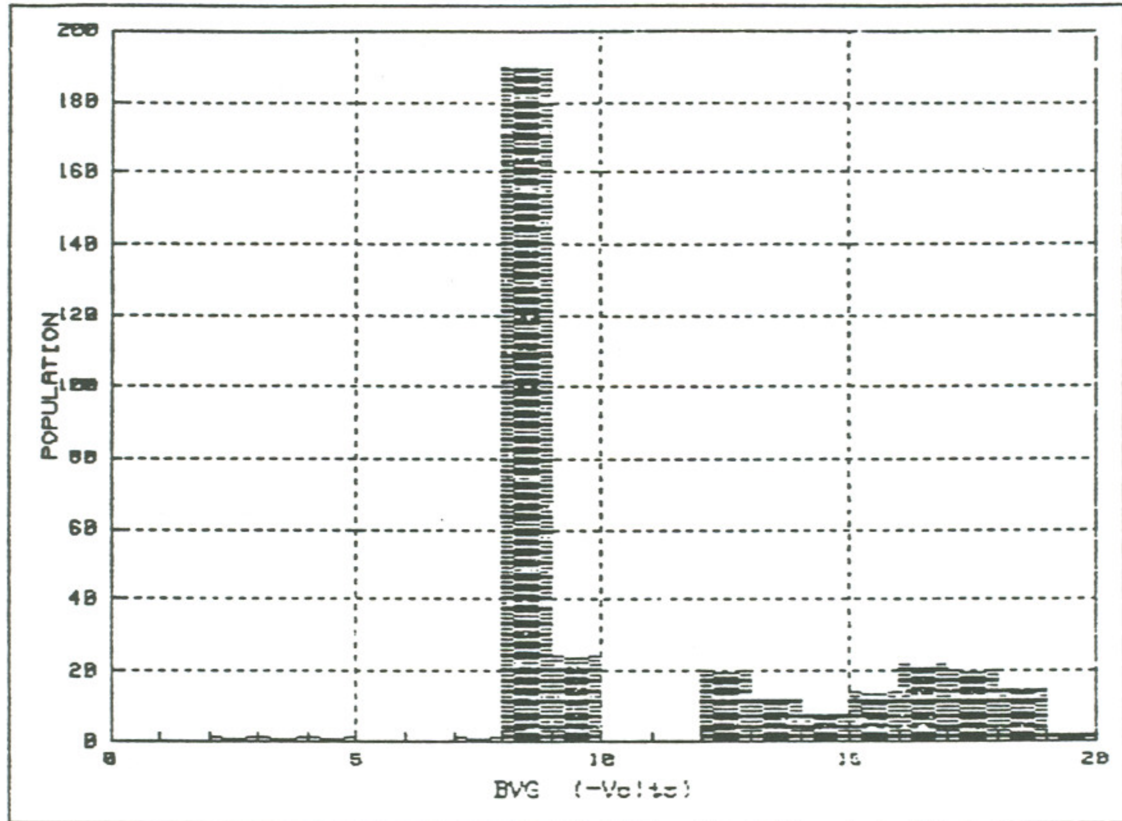


10%: 8.4
50%: 9.4
90%: 12.7

Lot#: 52108860 1 Wafers: 332 Points .2000 CM2

Poly AlCu Dots

BVG HISTOGRAM 18 Mar 1992 INTEL FAB 5 Etest

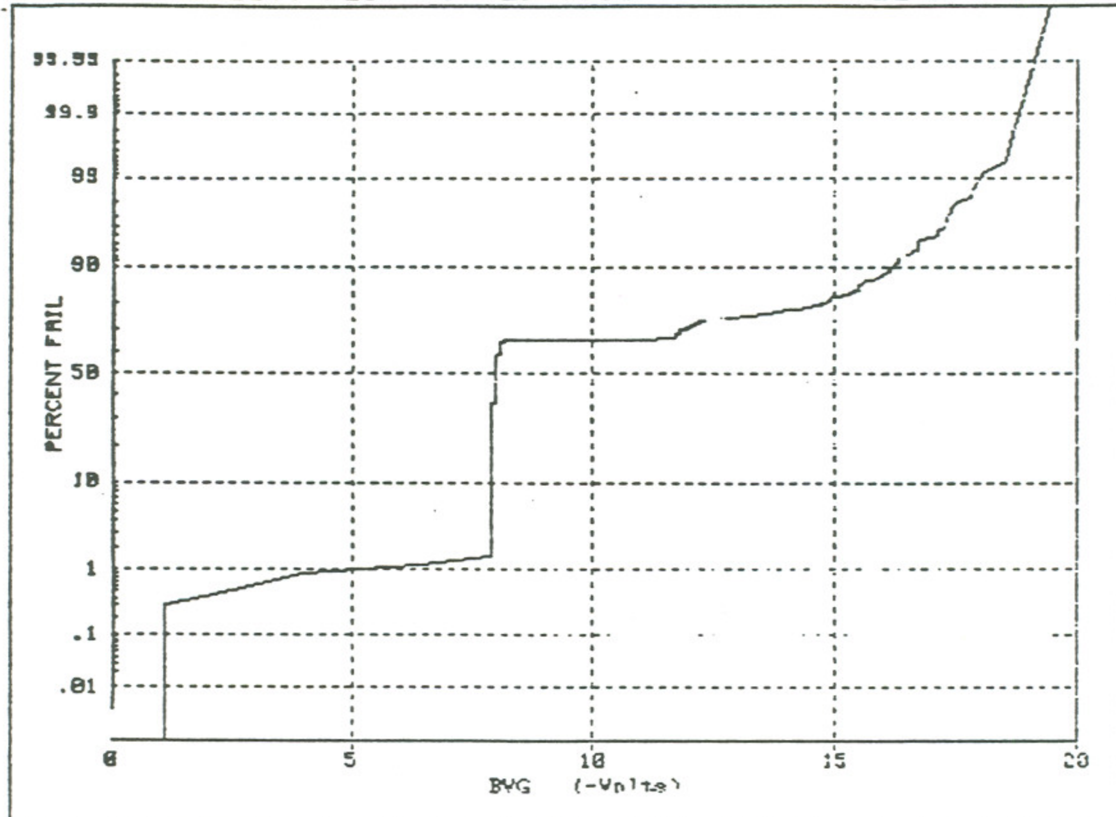


DEFECT DENSITY:
BVG < 1 : 0 cm.-2
BVG < 5.625 : .04539 cm.-2

% TAILS:
.9036 %

Lot#: 52108860 332 Points 1 Wafers .2000 CM2

Cr Dots Anneal

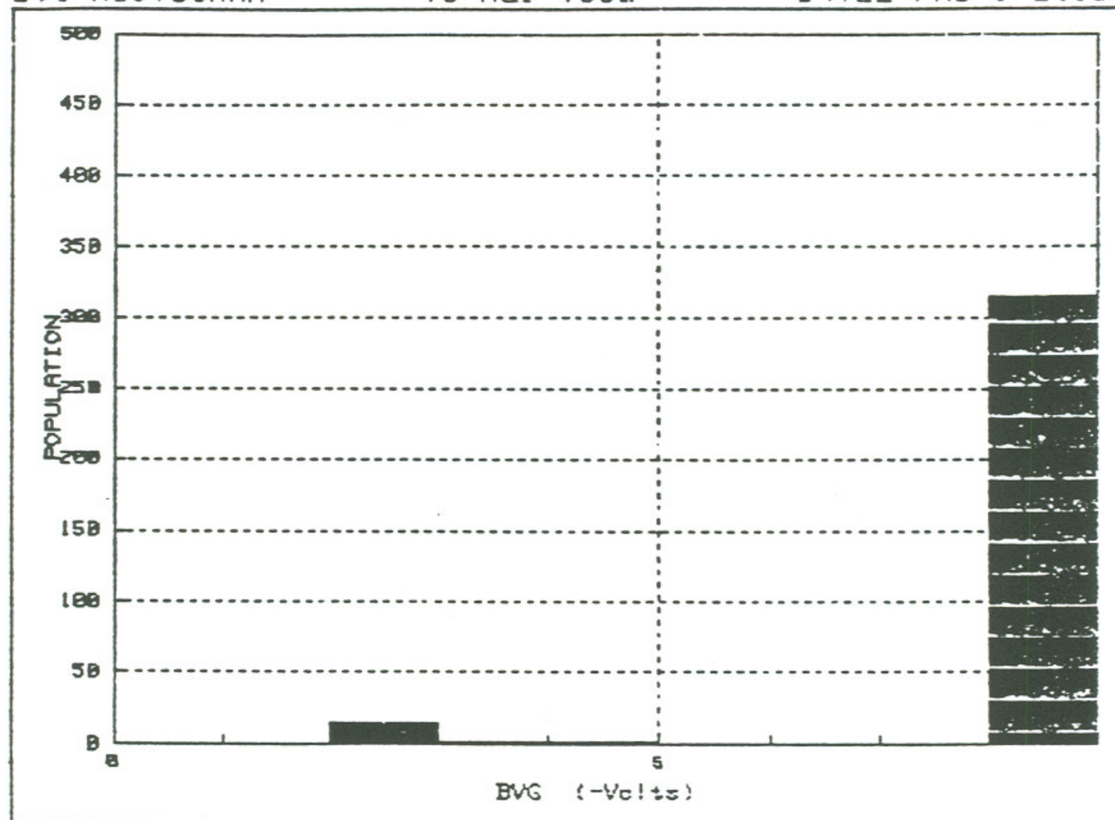


10%: 7.9
50%: 8
90%: 16.2

Lot#: 52108860 1 Wafers: 332 Points .2000 CM2

Cr Dots Anneal

BVG HISTOGRAM 18 Mar 1992 INTEL FAB 5 Etest

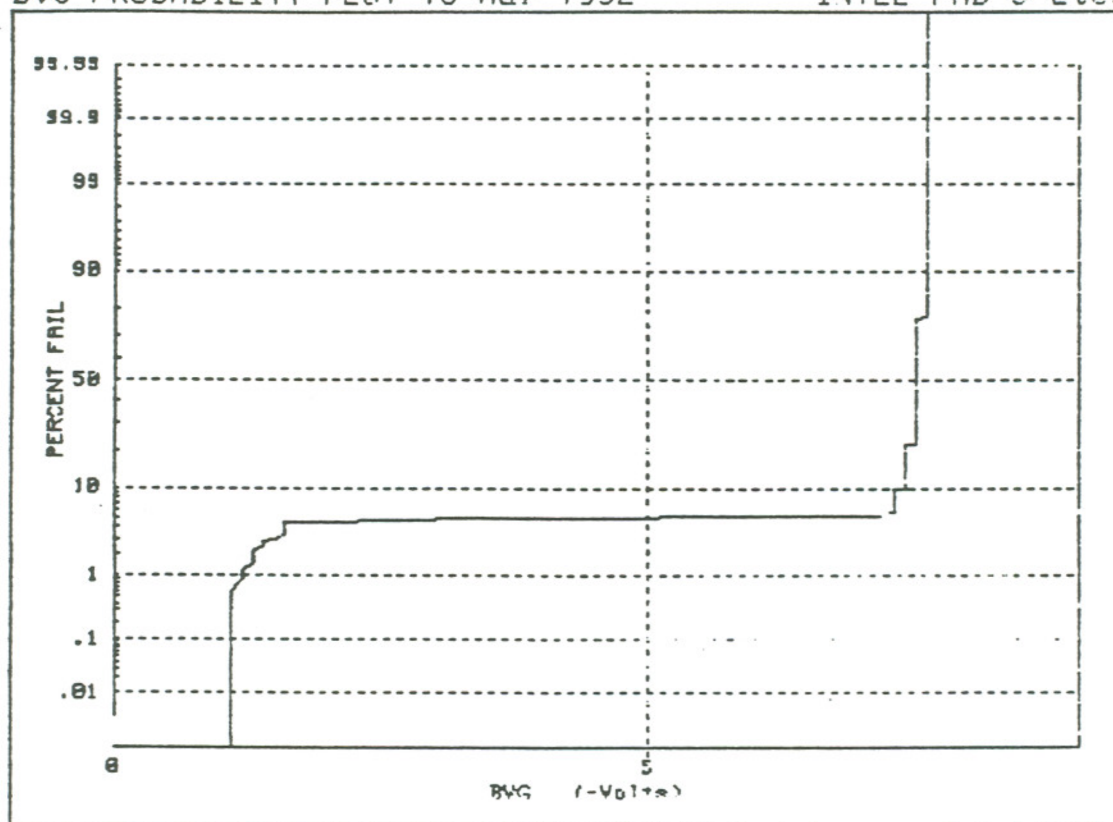


DEFECT DENSITY:
BVG < 1 : 0 cm.-2
BVG < 5.625 : .2628 cm.-2

% TAILS:
5.12 %

Lot#: 52108860 332 Points 1 Wafers .2000 CM2

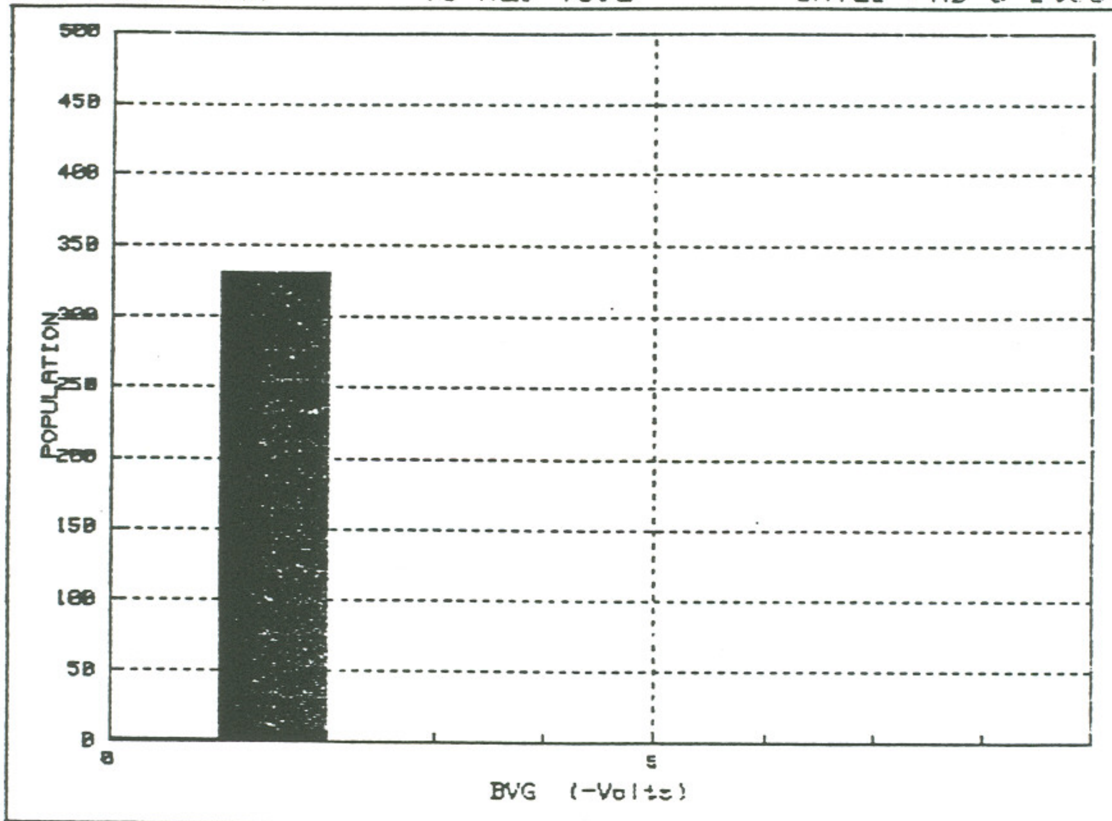
Cr Dots



10%: 7.4
50%: 7.5
90%: 7.6

Lot#: 52108860 1 Wafers: 332 Points .2000 CM2

Cr Dots



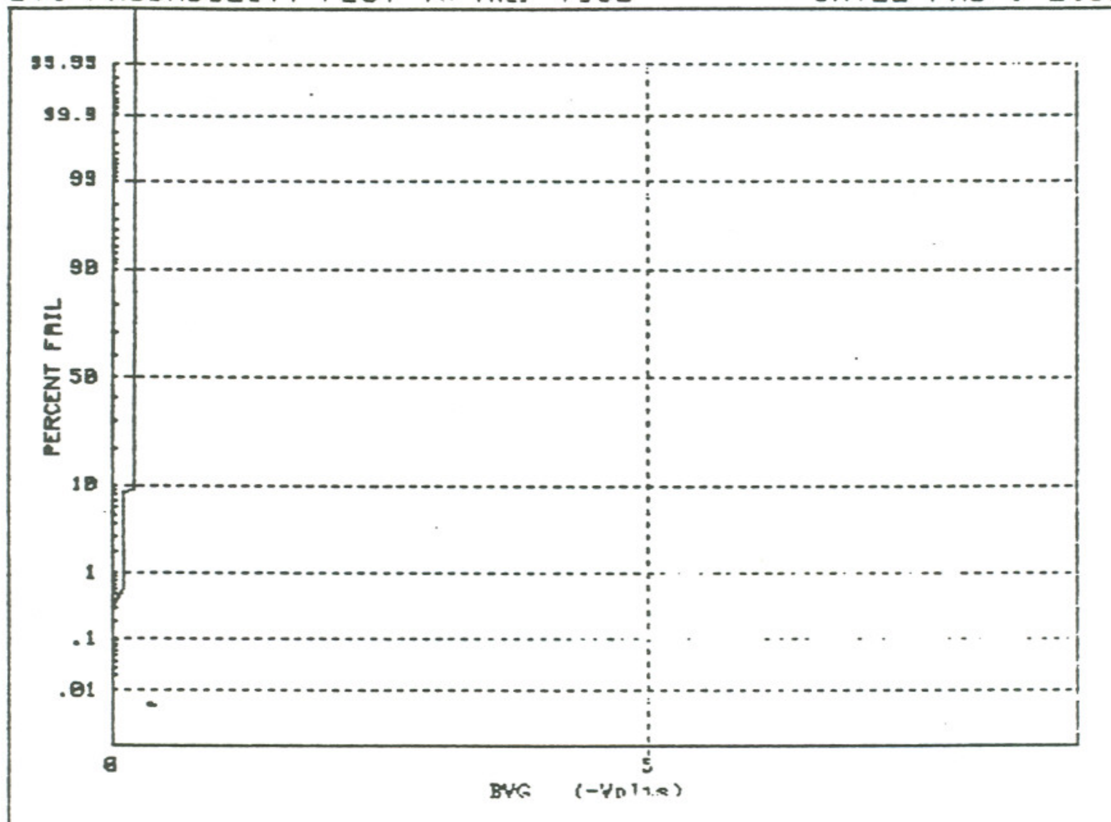
DEFECT DENSITY:
BVG < 1 : 29.03 cm.-2
BVG < 5.625 : 29.03 cm.-2

% TAILS:
0 %

Lot#: 52108860 332 Points 1 Wafers .2000 CM2

Ti Dots Anneal

BVG PROBABILITY PLOT 18 Mar 1992 INTEL FAB 5 Etest

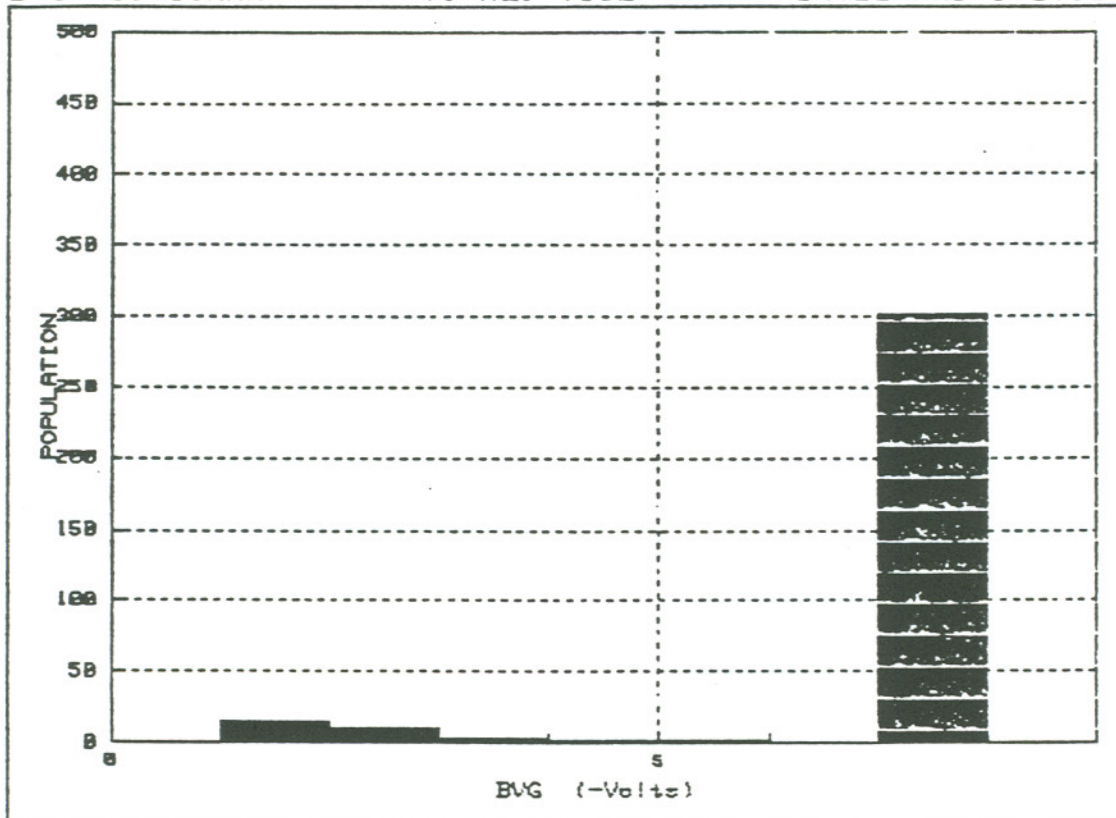


10%: .2
50%: .2
90%: .2

Lot#: 52108860 1 Wafers: 332 Points .2000 CM2

Ti Dots Anneal

BVG HISTOGRAM 18 Mar 1992 INTEL FAB 5 Etest

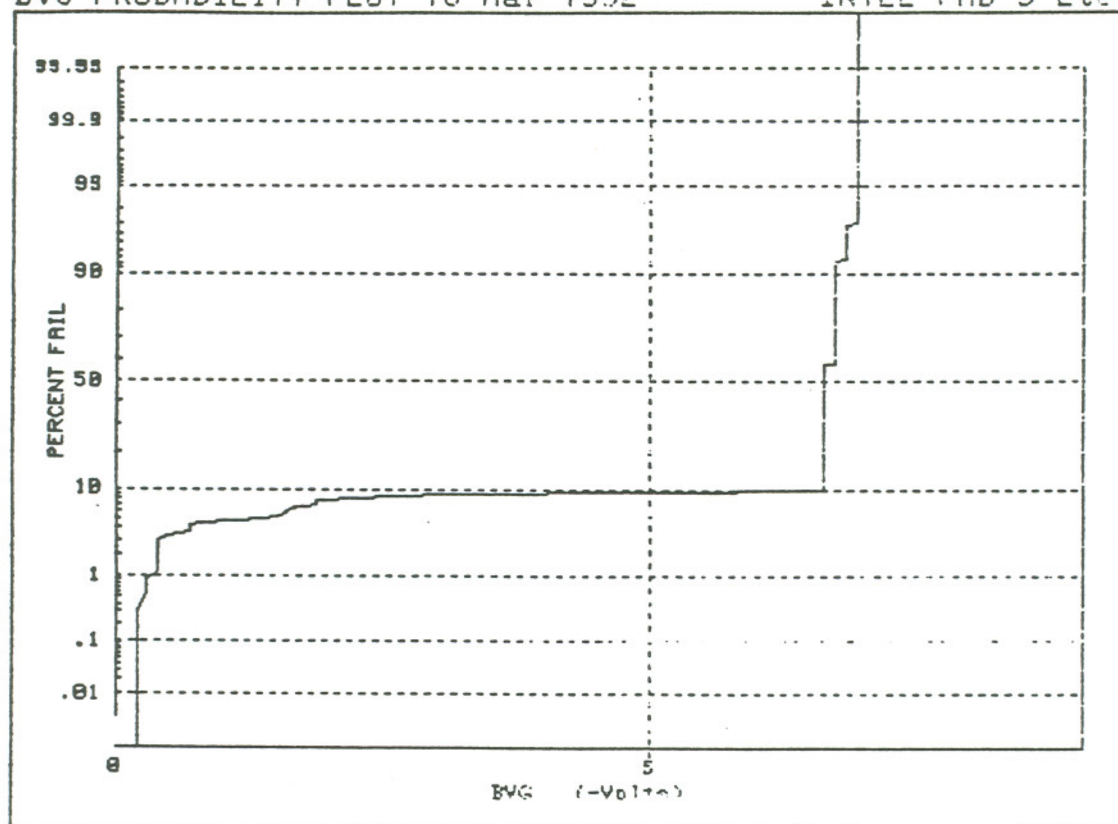


DEFECT DENSITY:
BVG < 1 : .2312 cm.-2
BVG < 5.625 : .4901 cm.-2

% TAILS:
4.819 %

Lot#: 52108860 332 Points 1 Wafers .2000 CM2

Ti Dots



10%: 6.6
50%: 6.6
90%: 6.7

Lot#: 52108860 1 Wafers: 332 Points .2000 CM2

Ti Dots

PROGRAM : FAB V BVG-INTEL REV: 5.01
COMMENTS : AlSi Dots Anneal
DEVICE : Large Dots
STRUCTURE: C/V Dot
AREA : .2
FILE : D_LAB/DATA_TEMP/2108860b03:REMOTE;LABEL MASTER
LOT : 52108860 DATE: 18 Mar 1992
WAFER : 03 TIME: 13:52:04
BY : ETHAN

WAFERMAP: (IBVGI for each tested die)
(* denotes A-mode (Short) OR B-mode (Tail) defect)
Wafer Tested with FLAT DOWN

						.7*	.7*	.9*	.8*	.7*	1.1*	.8*	.7*						
				.8*	.8*	.7*	.7*	1.5*	.7*	.8*	.7*	.7*	.7*	.7*	.8*				
			.7*	.7*	.7*	.6*	.7*	.7*	.7*	.7*	.7*	1.0*	.7*	1.0*	.8*	.5*			
		.6*	.7*	.7*	.7*	.7*	.7*	.6*	.7*	.7*	.7*	.6*	.8*	.5*	.8*	.8*	.7*		
	.6*	.7*	.6*	.6*	.6*	.7*	.7*	.6*	.7*	.7*	.7*	.7*	.7*	.5*	.7*	2.3*	.8*	.8*	
	.7*	.7*	.5*	.7*	.6*	.6*	.6*	.5*	.5*	.5*	.7*	.7*	.5*	1.1*	.7*	.7*	.9*	.8*	
.6*	.6*	.7*	.5*	.6*	.5*	.8*	.6*	.6*	.8*	.6*	.7*	.7*	.6*	.7*	.7*	1.0*	.7*	.5*	.7*
.6*	.7*	.6*	.6*	.6*	.6*	.7*	.6*	.6*	.6*	.6*	.7*	.7*	.6*	.6*	.6*	.8*	.7*	.8*	.8*
.5*	.6*	.6*	.7*	.6*	.7*	.6*	.6*	.6*	.5*	.7*	.1*	.6*	.6*	.6*	.6*	.7*	.7*	.5*	.6*
.6*	.6*	.6*	.5*	.7*	.6*	.7*	.5*	.8*	.6*	.6*	.5*	.5*	.6*	.6*	.9*	.7*	.6*	.6*	.2*
.5*	.6*	.6*	.5*	.5*	.6*	.6*	.7*	.6*	.5*	.6*	.5*	.5*	.5*	.5*	.7*	.2*	.2*	.2*	.5*
.5*	.5*	.6*	.7*	.7*	.8*	.5*	.6*	.6*	.6*	.5*	.2*	.6*	.2*	0.0*	.2*	.1*	.5*	.2*	.5*
.5*	.5*	.5*	.6*	.7*	.5*	.5*	.5*	.5*	.5*	.2*	.5*	.6*	.6*	.2*	.5*	.2*	.2*	.1*	.5*
.5*	.5*	.5*	.6*	.5*	.2*	.5*	.5*	.5*	.5*	.5*	.5*	.6*	.2*	.4*	.2*	.2*	.1*	.2*	.2*
	.5*	.5*	.5*	.5*	.5*	.5*	.2*	.5*	.5*	.5*	.5*	.5*	.5*	.2*	.5*	.4*	.2*	.5*	
	.4*	.5*	.5*	.5*	.1*	.5*	.5*	.5*	.5*	.2*	.2*	.5*	.4*	.2*	.5*	.5*	.5*	.4*	
		.5*	.5*	.5*	.5*	.5*	.5*	.5*	.5*	.5*	.5*	.5*	.1*	.2*	.5*	.5*	.4*		
			.5*	.5*	.5*	.5*	.1*	.5*	.5*	.5*	.5*	.7*	.7*	.6*	.6*	.6*			
				.5*	.5*	.5*	.5*	.5*	.6*	.5*	.5*	.6*	.5*	.5*	.5*				
						.5*	.5*	.5*	.5*	.7*	.5*	.5*	.6*						

TOTAL VALID DIE= 332

SHORTS DEFECT DENSITY (1V) : 19.3
TAILS DEFECT DENSITY : .1065
TOTAL DEFECT DENSITY (5.625V) : 10000

VOLTAGE	#FAIL	%FAIL	CUM % FAIL	DEFECT DENSITY
1	331	99.70	99.70	29.026
2	1	.30	100.00	10000.000

DESTRUCTIVE EVENTS = 332 = 100%
LIMIT VOLTAGE DIE 0
TEST COMPLETED 14:02:16

```
PROGRAM   : FAB V BVG-INTEL REV:  5.01
COMMENTS  : AlSi Dots
DEVICE    : Large Dots
STRUCTURE : C/V Dot
AREA      :  .2
FILE      : D_LAB/DATA_TEMP/2108860b04:REMOTE;LABEL MASTER
LOT       : 52108860                          DATE: 18 Mar 1992
WAFER     : 04                                TIME: 13:38:19
                                              BY  : ETHAN
-----------------------------------------------------------
WAFERMAP:      (IBVGI for each tested die)
               (* denotes A-mode (Short) OR B-mode (Tail) defect)
Wafer Tested with FLAT DOWN
```

```
                                    1.1*  1.2*  1.2*  1.1*  1.6*  1.1*  1.4*  1.4*
                        1.5*  1.5*  2.2*  1.3*  2.2*  1.5*  1.3*  2.0*  1.9*  1.7*  1.3*  1.3*
                  1.9*   .6*  1.7*  1.7*  2.2*  1.7*  1.6*  2.0*  1.0*  1.6*  1.4*  1.3*  1.1*  1.1*
            1.2*  1.8*  1.4*  1.7*  1.6*  1.9*  1.7*  1.3*  1.7*  1.0*  1.3*  1.9*  1.9*   .8*  1.0*   .9*
      1.4*  2.0*  1.9*  2.0*  1.7*  1.7*   .6*  1.3*  1.3*  1.7*  1.5*  2.0*  1.0*  1.4*  1.6*  1.7*  1.9*  1.7*
      1.3*  1.7*  1.7*  1.7*   .9*  1.8*  1.3*  1.5*  1.8*  1.8*  1.7*   .9*   .5*  1.4*  1.7*  1.8*  1.4*  1.8*
1.9*  1.1*  1.6*  1.9*  1.5*   .9*  2.1*  1.9*   .7*   .1*  1.1*  1.4*  1.7*  1.3*  2.0*  2.0*  1.4*  1.2*  1.1*   .2*
1.4*  2.0*  1.3*  1.7*  1.1*  1.1*  1.7*   .8*   .5*   .3*  2.0*  1.5*   .6*   .8*  1.7*  1.9*  2.2*   .5*  1.0*  1.0*
1.1*  1.5*  2.2*  1.2*  1.6*  1.1*   .8*   .9*   .5*   .8*   .8*   .7*   .7*   .8*  1.8*   .6*  1.0*  1.7*  1.1*  1.0*
1.7*  1.4*   .7*  2.0*  1.5*  1.5*  1.5*   .4*   .4*   .3*  1.1*  2.0*  2.3*  2.0*   .7*  1.2*  2.5*  2.5*   .2*   .8*
1.1*  1.4*  1.9*  1.5*  1.4*  1.4*  1.8*  1.7*  1.7*   .1*   .4*   .1*  1.1*   .7*  1.4*  1.0*  1.4*  1.8*   .7*   .1*
1.0*  1.4*  1.6*  1.3*  1.1*  1.1*  2.2*   .7*   .7*   .8*   .6*   .8*  1.7*   .7*   .9*   .5*   .7*   .2*   .7*   .2*
1.4*  1.0*  1.1*  1.0*   .5*  1.8*   .6*   .9*  1.1*   .7*   .2*   .1*   .8*   .6*   .7*   .7*   .7*   .2*   .5*   .1*
1.4*  1.6*  2.2*  1.0*   .7*  1.0*  1.1*  1.9*   .2*   .7*  1.1*   .2*   .4*   .2*   .6*   .7*   .8*   .4*   .2*  1.0*
      1.7*  1.3*   .7*  1.2*  1.0*   .2*  1.0*   .1*  1.1*   .2*  1.1*   .6*   .5*   .4*   .8*   .6*  1.0*  1.1*
      1.6*  1.7*  1.3*  2.1*  1.7*  1.4*  1.1*  1.1*   .8*   .9*  1.5*  1.2*   .6*   .2*  1.2*   .2*   .9*   .6*
            1.3*  1.6*  1.6*  1.1*   .7*  1.4*  1.4*   .2*   .8*  1.0*  1.0*  1.1*  1.3*  1.1*  1.1*  1.2*
                  1.3*  1.5*   .7*  1.3*  1.0*   .9*   .8*  1.1*   .8*  1.1*  1.3*  1.1*  2.2*  1.0*
                        1.4*  1.3*   .8*   .7*   .8*   .1*  0.0*   .2*   .8*  1.0*  1.3*   .8*
                                    1.1*   .7*   .7*   .8*  1.1*  1.3*   .7*  1.0*
```

```
     TOTAL VALID DIE= 332

     SHORTS DEFECT DENSITY ( 1V) :  2.035
     TAILS DEFECT DENSITY        :  5.478
     TOTAL DEFECT DENSITY ( 5.625V)  :  10000

VOLTAGE  #FAIL   %FAIL   CUM % FAIL   DEFECT DENSITY
   1      307    92.47     92.47           12.931
   2       25     7.53    100.00        10000.000

DESTRUCTIVE EVENTS = 332 = 100%
LIMIT VOLTAGE DIE  0
TEST COMPLETED  13:48:30
```

PROGRAM : FAB V BVG-INTEL REV: 5.01
COMMENTS : Poly AlSi Dots Anneal
DEVICE : Large Dots
STRUCTURE: C/V Dot
AREA : .2
FILE : D_LAB/DATA_TEMP/2108860b05:REMOTE;LABEL MASTER
LOT : 52108860 DATE: 18 Mar 1992
WAFER : 05 TIME: 13:25:14
BY : ETHAN

WAFERMAP: (|BVG| for each tested die)
(* denotes A-mode (Short) OR B-mode (Tail) defect)
Wafer Tested with FLAT DOWN

						7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8						
				.2*	1.7*	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.9				
			7.7	7.7	7.8	7.8	5.2*	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.9	7.9			
		7.7	7.7	7.7	7.7	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.9	7.9		
	7.7	7.7	7.7	7.7	7.7	7.8	7.7	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.9	7.9	
	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.9	
7.6	7.7	7.7	7.7	.2*	7.7	7.7	7.7	7.8	7.8	7.8	4.9*	7.8	7.8	7.8	7.8	7.8	7.9	7.9	7.9
7.6	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	.5*	7.8	7.8	7.8	7.8	7.8	7.8	7.9	7.8	7.9	8.0
7.6	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.8	7.7	7.8	7.8	7.8	7.8	7.9	7.8	8.1	7.9	7.9
7.6	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.8	7.8	7.8	7.8	8.1	7.8	7.8	7.8	7.9	7.8
7.5	7.6	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.8	7.9	7.8	7.8	7.8	7.9	7.8	7.9	7.8	8.1
7.6	7.6	7.7	7.7	7.7	7.7	7.7	7.7	7.8	7.7	7.7	7.7	7.8	7.8	9.2	7.8	8.1	7.8	7.8	7.8
7.5	7.6	7.6	7.7	7.7	7.7	7.7	7.7	7.7	8.0	7.7	7.7	7.7	7.9	7.7	7.8	7.8	7.8	7.8	7.8
7.6	7.6	7.6	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	8.1	8.0	7.8	7.8	7.8	7.8	7.8	7.8
	7.6	7.6	7.5	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.8	7.8	7.8	7.8	.5*	7.8	7.8	
	1.9*	7.6	7.6	7.6	7.7	7.7	7.8	7.7	7.7	7.7	7.7	9.1	7.7	7.8	7.8	7.8	7.8	7.9	
		7.6	7.6	7.6	7.7	7.7	7.7	7.7	7.7	7.7	7.8	7.8	7.8	7.7	7.8	7.8	7.8		
			7.5	7.6	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.8	7.7	7.9			
				7.6	7.7	7.7	7.7	7.7	7.8	7.7	7.7	7.8	7.7	7.7	7.8				
						7.5	7.7	7.7	7.7	7.8	7.7	7.7	7.7						

TOTAL VALID DIE= 332

SHORTS DEFECT DENSITY (1V) : .06061
TAILS DEFECT DENSITY : .06061
TOTAL DEFECT DENSITY (5.625V) : .122

VOLTAGE	#FAIL	%FAIL	CUM % FAIL	DEFECT DENSITY
1	6	1.81	1.81	.091
4	1	.30	2.11	.107
5	1	.30	2.41	.122
7	314	94.58	96.99	17.513
8	8	2.41	99.40	25.560
9	2	.60	100.00	10000.000

DESTRUCTIVE EVENTS = 8 = 2.41%
LIMIT VOLTAGE DIE 0
TEST COMPLETED 13:35:34

```
PROGRAM   : FAB V BVG-INTEL REV:  5.01
COMMENTS  : Poly AlSi Dots
DEVICE    : Large Dots
STRUCTURE: C/V Dot
AREA      :  .2
FILE      : D_LAB/DATA_TEMP/2108860b06:REMOTE;LABEL MASTER
LOT       : 52108860                            DATE: 18 Mar 1992
WAFER     : 06                                  TIME: 13:10:17
                                                BY  : ETHAN
-------------------------------------------------------------
WAFERMAP:      (IBVGI for each tested die)
               (* denotes A-mode (Short) OR B-mode (Tail) defect)
Wafer Tested with FLAT DOWN

                                    7.8   7.8   7.8   7.8   7.8   7.8   7.9   8.0
                        7.9   7.7   7.7   7.7   7.8   7.8   7.8   7.8   7.9   7.9   8.0   7.9
                  7.8   7.7   7.8   7.7   7.8   7.7   7.8   7.8   7.8   7.9   7.9   8.0   8.1   8.0   —
            7.8   7.7   7.7   7.7   7.8   7.8   7.7   7.8   7.8   7.8   7.9   7.8   8.2   8.3   8.1   7.9
      7.7   7.8   7.7   7.7   7.7   7.7   7.7   7.7   7.7   7.7   7.8   7.8   8.4   8.3   7.9   8.4   7.9   7.9
      7.7   7.7   7.7   7.8   7.7   7.7   7.7   7.7   7.7   7.7   7.9   7.9   7.8   8.0   8.4   7.8   7.9   7.9
7.8   7.7   7.7   7.7   7.8   7.7   7.7   7.8   7.8   7.9   7.8   7.8   7.9   8.5   8.7   7.8   1.1*  7.8   7.8   8.1
7.5   7.6   7.8   7.7   7.7   7.7   7.7   7.8   7.7   7.7   7.7   7.7   7.7   7.9   7.8   7.8   8.1   7.9   8.0   8.0
7.6   7.8   7.7   7.7   7.7   2.2*  2.0*  7.7   7.7   7.7   7.7   7.7   8.4   7.8   8.2   8.2   7.9   7.9   8.1   8.1
7.6   7.6   7.7   7.7   7.7   7.7   7.7   7.7   7.8   7.9   7.7   7.8   8.8   8.1   7.8   8.3   8.2   7.9   8.1   7.8
7.5   7.8   7.8   7.7   7.7   7.7   7.7   7.8   7.7   1.0*  7.7   7.8   8.7   8.1   8.1   8.1   7.9   7.8   8.0   8.0
7.6   7.8   7.7   7.7   7.8   7.7   7.7   7.7   7.8   7.7   7.7   8.3   8.2   8.0   8.1   8.0   7.8   7.8   7.8   7.8
7.6   7.8   7.8   7.6   7.7   7.7   7.7   7.7   7.9   7.7   8.1   8.0   8.3   7.8   7.9   7.9   7.9   7.8   7.8   7.8
7.6   7.7   7.7   7.7   7.7   7.7   7.7   7.7   7.7   7.7   7.8   7.9   8.0   7.9   7.9   7.8   7.9   7.8   7.8   7.8
      7.7   7.6   7.7   7.6   7.7   7.7   7.7   7.7   7.8   7.8   7.9   7.8   7.9   7.9   7.8   7.8   7.8   7.8
      7.7   7.6   7.6   7.7   7.7   7.6   7.7   7.7   7.8   7.8   7.9   7.8   7.8   7.8   7.8   7.8   7.8   7.8
            7.7   7.6   7.6   7.6   7.7   7.7   7.7   7.8   7.8   7.9   7.8   7.8   7.8   7.8   7.8   7.8
                  7.6   7.6   7.6   7.6   7.7   7.7   7.8   7.9   7.7   7.8   7.8   7.8   7.8   7.8
                        7.6   7.6   7.5   7.7   7.8   7.7   7.7   7.8   7.8   7.8   7.8   7.9
                                    .5*   7.7   7.8   7.7   7.8   7.7   7.8   7.7

          TOTAL VALID DIE= 332

          SHORTS DEFECT DENSITY ( 1V) :   .01508
          TAILS DEFECT DENSITY        :   .06061
          TOTAL DEFECT DENSITY ( 5.625V)  :   .07587

VOLTAGE  #FAIL    %FAIL  CUM %-FAIL    DEFECT DENSITY
   1        3       .90        .90             .045
   2        2       .60       1.51             .076
   7      283     85.24      86.75           10.105
   8       44     13.25     100.00        10000.000

DESTRUCTIVE EVENTS = 5 = 1.51%
LIMIT VOLTAGE DIE  0
TEST COMPLETED  13:20:28
```

```
PROGRAM   : FAB V BVG-INTEL REV:  5.01
COMMENTS  : Poly AlCu Dots Anneal
DEVICE    : Large Dots
STRUCTURE : C/V Dot
AREA      :  .2
FILE      : D_LAB/DATA_TEMP/2108860b09:REMOTE;LABEL MASTER
LOT       : 52108860                            DATE: 18 Mar 1992
WAFER     : 09                                  TIME: 11:48:35
                                                BY  : ETHAN
```

```
WAFERMAP:      (IBVGI for each tested die)
               (* denotes A-mode (Short) OR B-mode (Tail) defect)
Wafer Tested with FLAT DOWN

                                    12.4   7.8   7.8  12.1  12.0  11.4  11.8   7.9
                        7.8   7.8    7.8   7.8   7.8   7.8   7.8  11.9   7.9  12.4   7.9   7.9
                  7.8   7.8  10.3    7.8   7.8   7.8  12.1  12.0  11.1  12.3  12.3   7.9   7.9   7.9
            7.8   7.8   7.8  11.6   11.5   7.8  11.9   7.8  11.7  11.8   7.8   7.8   7.9   7.9   7.9   7.9
      7.7  11.3   7.8  12.3   7.8    7.8  11.8  11.7   7.8  11.7  11.1  12.3  10.8   7.9   7.9   8.0   7.9   7.9
      7.7   7.8  11.0  11.7   7.8    7.8  11.7  11.4  10.8  10.9  11.5  11.7  12.0  12.0  11.3   7.9   7.9   7.9
7.7   7.7  12.4  12.4  12.0  11.8   11.7  11.3   7.8  11.2  11.3  11.4  11.5  11.2  11.7  12.1   8.0   7.9   7.9   7.9
7.7  11.4  12.6   7.8  12.0  12.0   11.6  11.3  11.1  11.7  11.8  11.7  11.7  11.4  11.6   7.8  12.4   7.9   7.9   7.9
7.7   7.7   7.7  12.4   7.8  12.0    7.8  0.0*  11.1  12.2  13.3  12.5  12.3  11.8  11.4  11.8   7.8  11.7   7.9   7.9
7.7   7.7   7.7   7.8  11.7  12.4   11.7  11.0  11.1  12.1  13.4  13.2  12.9  12.1  11.8  12.0  12.2  12.1   7.8   7.8
7.7   7.7   7.7   7.7   7.7   7.8   12.1  11.3  11.1  12.5   9.9  13.8  12.9  12.3  11.8  11.8   9.3   7.8   7.8   7.8
7.7   7.7   7.7  11.8   7.7   7.8   12.1   7.8  11.2  12.4  13.0  13.5  10.7  12.3  12.1   7.8  11.7   7.8   7.8  10.2
7.7   7.7   7.7   7.7  12.3  12.4   12.6   7.8  11.7  12.0  12.9  12.7   7.8  12.3   7.8  11.7   7.8   7.8  13.3  11.7
7.7   .5*   7.7   7.7   7.7  11.1   12.6   7.8   7.8   7.8   7.8   7.8   7.8  12.4  12.1   7.8   7.8   7.8   7.8   7.8
      7.7   7.7   7.7   7.7   7.7    9.1   7.7  12.9  12.8   7.8   7.8   7.8  12.0   7.8   7.8   7.8  12.4   7.8
      7.7   7.7   7.7   7.7   7.7    7.7   7.7   7.8  12.8  12.2   7.8   7.8   7.8  10.8   7.8  12.4  13.4   7.8
            7.7   7.7   7.7   7.7    7.7   7.7  12.2   7.7   7.8  13.4  11.5   7.8   7.8   7.8  12.3   7.9
                  7.7   7.7   7.7    7.7   7.7  11.5   7.7   7.7   7.7   7.8   7.8   7.8   7.8   7.8
                        7.7   7.7    7.7   7.7   7.7   7.7   7.7   7.7   7.8   7.8   7.8   7.8
                                     9.7  12.4   7.7  10.3   7.7   7.7   7.8   7.8

     TOTAL VALID DIE= 190

     SHORTS DEFECT DENSITY ( 1V) :   .05291
     TAILS DEFECT DENSITY        :   0
     TOTAL DEFECT DENSITY ( 5.625V)  :   .05291
```

VOLTAGE	#FAIL	%FAIL	CUM % FAIL	DEFECT DENSITY
1	2	1.05	1.05	.053
7	184	96.84	97.89	19.304
8	2	1.05	98.95	22.769
9	4	2.11	101.05	10000.000
10	8	4.21	105.26	10000.000

DESTRUCTIVE EVENTS = 2 = 1.05%
LIMIT VOLTAGE DIE 142
TEST COMPLETED 11:58:48

PROGRAM : FAB V BVG-INTEL REV: 5.01
COMMENTS : Poly AlCu Dots
DEVICE : Large Dots
STRUCTURE: C/V Dot
AREA : .2
FILE : D_LAB/DATA_TEMP/2108860b10:REMOTE;LABEL MASTER
LOT : 52108860
WAFER : 10

DATE: 18 Mar 1992
TIME: 11:35:36
BY : ETHAN

WAFERMAP: (|BVG| for each tested die)
(* denotes A-mode (Short) OR B-mode (Tail) defect)
Wafer Tested with FLAT DOWN

						9.7	10.5	9.4	11.1	13.8	10.5	13.8	8.9						
				7.7	9.5	8.5	8.2	8.9	11.1	10.1	7.9	10.3	13.9	13.9	14.0				
			8.2	9.0	8.2	9.6	9.7	9.2	13.2	9.0	8.5	9.7	13.9	14.0	10.7	14.0			
		8.6	8.8	8.8	8.8	9.9	8.2	9.4	9.8	8.1	10.3	9.1	13.9	10.5	10.6	8.9	14.0		
	7.9	8.4	8.6	10.5	8.4	9.3	9.9	9.7	11.4	10.3	9.8	12.1	13.5	9.9	10.5	7.9	8.1	14.0	
	8.9	9.1	10.8	9.6	10.2	8.6	9.4	11.4	11.2	11.3	12.0	12.6	13.3	10.1	9.4	9.3	13.6	13.9	
9.3	9.0	9.2	9.8	9.4	9.4	9.5	11.5	11.3	11.3	11.7	8.7	12.3	13.1	10.9	13.5	12.9	8.8	8.2	14.0
9.7	9.3	9.6	9.4	9.1	9.6	9.4	8.6	10.5	9.8	12.4	10.9	12.1	12.4	9.5	12.0	9.0	9.2	8.6	13.9
13.8	10.0	10.1	8.5	9.0	9.2	11.5	9.0	11.1	11.4	.1*	12.5	12.1	11.4	9.4	9.6	10.6	8.5	9.1	10.2
13.2	9.0	9.1	8.6	9.1	9.1	9.1	7.6	10.9	11.7	12.0	12.1	12.1	8.5	9.0	11.5	9.2	9.3	9.5	10.8
9.5	9.2	8.2	8.3	12.9	12.5	12.3	11.7	11.7	11.7	12.0	12.3	10.2	12.1	9.3	12.5	13.0	8.4	9.0	8.6
9.4	9.7	8.8	8.5	13.0	12.8	10.9	12.5	12.7	1.1*	11.8	9.2	11.8	9.9	12.6	10.0	9.4	9.4	8.7	8.8
9.0	9.4	8.7	10.1	13.6	10.3	13.3	9.0	12.8	10.8	.1*	11.6	12.0	8.8	9.0	8.9	8.4	9.0	8.5	9.3
8.9	8.8	8.2	8.7	9.7	9.3	13.0	9.4	11.9	9.5	8.9	9.0	9.9	9.8	8.6	8.5	8.4	8.3	9.4	9.6
	8.1	8.9	9.2	13.2	9.7	9.9	10.2	12.5	11.5	9.3	8.8	9.4	10.9	9.0	8.6	8.3	8.2	8.3	
	8.5	8.1	10.5	8.7	7.7	10.3	10.5	11.5	12.2	9.0	8.2	8.7	8.5	8.2	8.4	9.0	8.1	9.0	
		8.5	9.3	9.2	8.8	9.5	10.3	8.4	10.5	9.3	8.8	8.7	8.8	8.5	8.5	8.5	8.7		
			8.8	9.0	9.0	8.8	9.9	9.9	10.5	8.7	8.8	8.9	8.7	8.7	8.5	8.5			
				8.4	8.6	8.2	8.7	13.3	8.7	9.1	8.2	8.3	8.5	8.7	8.4				
						9.0	9.1	10.3	10.4	12.7	12.8	10.6	10.0						

TOTAL VALID DIE= 185

SHORTS DEFECT DENSITY (1V) : .05435
TAILS DEFECT DENSITY : .0271
TOTAL DEFECT DENSITY (5.625V) : .08175

VOLTAGE	#FAIL	%FAIL	CUM % FAIL	DEFECT DENSITY
1	3	1.62	1.62	.082
7	6	3.24	4.86	.249
8	96	51.89	56.76	4.192
9	101	54.59	111.35	10000.000
10	41	22.16	133.51	10000.000

DESTRUCTIVE EVENTS = 3 = 1.62%
LIMIT VOLTAGE DIE 147
TEST COMPLETED 11:45:48

PROGRAM : FAB V BVG-INTEL REV: 5.01
COMMENTS : Cr Dots Anneal
DEVICE : Large Dots
STRUCTURE: C/V Dot
AREA : .2
FILE : D_LAB/DATA_TEMP/2108860b13:REMOTE;LABEL MASTER
LOT : 52108860 DATE: 18 Mar 1992
WAFER : 13 TIME: 11:19:42
BY : ETHAN

WAFERMAP: (|BVG| for each tested die)
(* denotes A-mode (Short) OR B-mode (Tail) defect)
Wafer Tested with FLAT DOWN

						11.7	11.7	11.8	11.8	11.7	11.8	11.7	11.7						
				4.0*	11.6	11.5	11.7	12.2	12.4	12.2	12.0	11.9	12.0	12.1	12.0				
			11.8	11.9	12.1	12.0	7.9	12.2	12.5	12.5	12.2	12.4	12.6	13.0	13.6	8.2			
		7.9	7.9	7.9	7.9	15.5	7.9	7.9	14.6	14.7	8.0	8.0	16.2	8.1	8.1	8.1	15.8		
	7.9	7.9	15.5	7.9	14.3	13.3	14.0	13.1	15.0	8.0	8.0	8.0	16.0	8.1	8.1	8.1	14.9	8.2	
	7.9	7.9	13.5	7.9	7.9	13.8	7.9	14.6	15.2	13.5	8.0	15.6	8.0	8.0	8.1	8.1	16.3	8.1	
14.8	11.1	16.3	16.1	16.2	16.1	7.9	14.9	17.3	8.0	17.3	17.2	8.0	8.0	8.0	17.1	8.1	8.1	8.1	13.9
7.9	7.9	7.9	7.9	7.9	16.7	14.9	7.9	16.2	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.1	8.1	8.1
7.9	15.5	7.9	15.1	17.4	16.0	7.9	17.4	7.9	17.1	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.1	8.1	8.1
7.9	15.9	7.9	16.4	16.7	15.5	7.9	7.9	7.9	7.9	7.9	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.1
7.9	15.6	7.9	15.3	7.9	14.2	7.9	16.8	7.9	17.5	8.0	8.0	8.0	8.0	8.0	8.0	7.9	8.0	8.0	8.1
6.4	7.9	16.7	14.9	18.5	16.5	7.9	7.9	7.9	7.9	7.9	9.0	16.0	8.0	17.3	8.0	7.9	8.0	8.0	8.0
7.9	15.6	2.9*	14.4	7.9	14.5	7.9	16.7	7.9	17.1	11.8	9.0	8.0	8.0	8.0	7.9	7.9	8.0	8.0	8.0
7.9	7.9	7.9	7.9	7.9	7.9	7.9	1.1*	8.0	17.8	8.0	8.0	8.0	19.4	7.9	7.9	7.9	8.0	8.0	8.1
	16.3	7.9	7.9	7.9	17.3	7.9	7.9	7.9	8.0	8.0	8.0	7.9	7.9	7.9	7.9	7.9	8.0	8.0	
	16.6	7.9	15.5	7.9	7.9	7.9	7.9	7.9	7.9	15.9	7.9	7.9	7.9	7.9	7.9	15.2	8.0	8.0	
		7.9	7.9	7.9	7.9	7.9	16.3	8.8	18.5	7.9	17.9	7.9	7.9	7.9	7.9	7.9	8.0		
			7.9	7.9	7.9	7.9	7.9	15.5	7.9	14.7	18.0	7.9	7.9	7.9	7.9	8.0			
				16.6	7.9	16.1	7.9	15.4	7.9	7.9	7.9	7.9	16.7	7.9	8.0				
						7.9	7.9	7.9	17.8	15.3	7.9	15.4	8.0						

TOTAL VALID DIE= 218

SHORTS DEFECT DENSITY (1V) : 0
TAILS DEFECT DENSITY : .06929
TOTAL DEFECT DENSITY (5.625V) : .06929

VOLTAGE	#FAIL	%FAIL	CUM % FAIL	DEFECT DENSITY
1	1	.46	.46	.023
2	1	.46	.92	.046
4	1	.46	1.38	.069
6	1	.46	1.83	.093
7	117	53.67	55.50	4.049
8	97	44.50	100.00	10000.000

DESTRUCTIVE EVENTS = 3 = 1.38%
LIMIT VOLTAGE DIE 114
TEST COMPLETED 11:29:55

```
PROGRAM   : FAB V BVG-INTEL REV:  5.01
COMMENTS  : Cr Dots
DEVICE    : Large Dots
STRUCTURE: C/V Dot
AREA      :  .2
FILE      : D_LAB/DATA_TEMP/2108860b14:REMOTE;LABEL MASTER
LOT       : 52108860                              DATE: 18 Mar 1992
WAFER     : 14                                    TIME: 11:03:53
                                                  BY  : ETHAN
```

```
WAFERMAP:     (|BVG| for each tested die)
              (* denotes A-mode (Short) OR B-mode (Tail) defect)
Wafer Tested with FLAT DOWN

                                    7.4   7.5   1.1*  7.5   7.5   7.5   7.5   7.6
                        1.1*  7.4   7.5   7.5   7.5   7.6   7.5   7.6   7.6   7.5   7.6   7.6
                  7.4   7.5   7.5   7.5   7.5   7.5   7.6   7.6   7.6   7.6   7.6   7.6   7.6   7.6
            7.4   7.5   7.5   7.5   7.5   7.5   7.6   7.6   7.6   7.6   1.2*  7.6   7.6   7.6   7.6   7.6
      7.4   7.4   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.6   7.6   7.6   7.6   7.6   7.6   7.6   7.6   7.5
      7.4   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.6   7.6   7.6   7.6   7.6   7.6   7.6   7.6
7.3   7.4   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.6   7.6   7.6   7.6   7.6   7.6   7.5
7.3   7.4   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.6   7.6   7.6   7.6   7.6   7.5   7.6
7.4   7.4   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.6   7.6   7.6   7.6   7.6   7.6   7.6
7.4   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.6   7.5   7.6   7.5   7.6   7.6   7.6
7.3   7.4   7.4   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.6   7.5   7.5   7.5   7.6   7.6   7.5
1.3*  7.4   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.6   7.6   7.6   7.5   7.6
7.3   7.4   1.5*  7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.6   7.5   7.5
7.3   7.4   7.4   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5
      7.3   7.4   7.4   7.5   7.5   7.5   7.5   1.6*  7.5   7.5   1.3*  3.1*  7.5   7.5   1.2*  7.5   7.5   7.5
      7.3   7.3   7.4   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   1.6*  7.5   7.5   1.4*  7.5   7.5
            7.3   7.4   7.4   7.4   1.3*  7.4   1.6*  7.5   7.5   1.4*  7.5   7.5   3.0*  7.5   7.5   7.4
                  7.3   7.3   7.4   7.4   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.5   7.4
                        7.3   7.3   7.4   7.4   7.4   7.4   7.4   7.5   7.1   7.5   7.4   7.4
                                    1.5*  7.3   7.4   7.4   7.4   7.4   7.4   1.5*

     TOTAL VALID DIE= 332

     SHORTS DEFECT DENSITY ( 1V) :  0
     TAILS DEFECT DENSITY        :  .2628
     TOTAL DEFECT DENSITY ( 5.625V)  :  .2628
```

VOLTAGE	#FAIL	%FAIL	CUM % FAIL	DEFECT DENSITY
1	15	4.52	4.52	.231
3	2	.60	5.12	.263
7	315	94.88	100.00	10000.000

DESTRUCTIVE EVENTS = 17 = 5.12%
LIMIT VOLTAGE DIE 0
TEST COMPLETED 11:18:43

```
PROGRAM   : FAB V BVG-INTEL REV:  5.01
COMMENTS  : Ti Dots Anneal
DEVICE    : Large Dots
STRUCTURE: C/V Dot
AREA      :  .2
FILE      : D_LAB/DATA_TEMP/2108860b17:REMOTE;LABEL MASTER
LOT       : 52108860                                DATE: 18 Mar 1992
WAFER     : 17                                      TIME: 10:50:35
                                                    BY  : ETHAN
-------------------------------------------------------------------
WAFERMAP:     (|BVG| for each tested die)
              (* denotes A-mode (Short) OR B-mode (Tail) defect)
Wafer Tested with FLAT DOWN

                                    .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
                        .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
                  .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
            .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
      .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
      .2*   .2*   .2*   .2*   .2*   .2*   .2*   .1*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
.2*   .2*   .2*   .2*   .2*   .2*   .2*   .1*   .2*   .1*   .2*   .1*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
.2*   .2*   .2*   .2*   .2*   .1*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .1*   .2*
.1*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .1*   .1*   .1*   .2*   .2*   .2*   .2*   .1*   .2*   .2*   .2*   .2*
.2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .1*   .2*   .2*   .2*   .2*   .2*   .2*   .1*   .2*   .2*   .2*
.2*   .2*   .1*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .1*   .1*   .1*
.1*   .2*   .1*   .2*   .2*   0.0*  .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
.2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .1*
.2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
      .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .1*
      .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
            .2*   .1*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
                  .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
                        .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*   .2*
                                    .2*   .1*   .1*   .1*   .1*   .1*   .1*   .2*

     TOTAL VALID DIE= 332

     SHORTS DEFECT DENSITY ( 1V) :   10000
     TAILS DEFECT DENSITY          :   0
     TOTAL DEFECT DENSITY ( 5.625V)  :    10000

VOLTAGE   #FAIL    %FAIL   CUM % FAIL    DEFECT DENSITY
   1        332    100.00     100.00          10000.000

DESTRUCTIVE EVENTS = 332 = 100%
LIMIT VOLTAGE DIE  0
TEST COMPLETED  11:00:48
```

```
PROGRAM   : FAB V BVG-INTEL REV:  5.01
COMMENTS  : Ti Dots
DEVICE    : Large Dots
STRUCTURE : C/V Dot
AREA      :  .2
FILE      : D_LAB/DATA_TEMP/2108860b18:REMOTE;LABEL MASTER
LOT       : 52108860                               DATE: 18 Mar 1992
WAFER     : 18                                     TIME: 10:35:07
                                                   BY  : ETHAN
---------------------------------------------------------------
WAFERMAP:     (|BVG| for each tested die)
              (* denotes A-mode (Short) OR B-mode (Tail) defect)
Wafer Tested with FLAT DOWN

                         6.7  6.7  6.7  6.7  6.7  6.7  6.8  6.9
               1.9* 6.7  6.7  6.7  6.7  6.7  6.7  6.7  6.8  6.8  6.9  6.9
          6.6  6.7  6.7  6.7  6.7  6.7  6.7  6.7  6.7  6.7  6.8  6.8  6.9  6.9
     6.6  6.6  6.7  6.7  6.7  6.7  6.7   .7* 6.7  6.7  6.7  6.7  6.8  6.8  6.9  6.9
6.6  6.6  6.6  6.6  6.7  6.6  6.7  6.7  6.7  6.7  6.7  6.7  6.7  6.7  6.8  6.8  6.9  6.9
6.6  6.6  6.6  6.6  6.6  5.7  6.7  6.7  6.7  5.7  6.7  6.7  6.7  5.7  6.7  6.8  6.8  6.9
5.6  3.1* 6.5  6.6  6.6  6.6  6.6  6.5  6.6  6.7  6.7  6.7  6.7  6.7  6.7  6.7  5.7  6.8  6.8  6.9
6.5  6.6  1.6* 6.6  6.6  6.6  6.6  6.6  6.7  6.6  6.7  5.7   .7* 6.7  6.7  6.7  6.7  6.7  6.8  6.8
6.5   .4* 6.6  1.7* 6.6  6.6  6.6  6.6  6.6  6.6  2.3* 6.7  6.7  6.7  6.7  6.7  6.7  6.7  6.7  1.1*
6.5  6.6  6.5  6.6  6.6  6.5  6.6  6.5  6.6   .4* 6.6   .8* 6.7  6.7  6.7  6.7  6.7  6.7  6.7  6.7
6.5   .4*  .3* 6.6  6.6  6.6   .5* 6.6  6.6  6.6  6.7  2.5* 6.7  6.7   .4* 6.7  6.7  6.7  6.7  6.7
1.4* 6.6  6.5  6.5  6.5  1.9* 6.5  1.6* 6.6  6.6   .7* 6.6  6.7  2.7* 6.7  6.7  6.7  5.7  6.7  5.7
6.6   .4* 6.6   .3* 6.6  6.5  6.6  6.6  6.6  6.6  1.7* 6.7  1.9* 6.7   .4* 5.7  6.7  6.7  6.7  6.7
 .2* 6.5  6.6  6.5  6.5  6.6  6.5  6.5  6.6  6.6  6.5  6.7  6.6  6.7  6.6  6.7  6.7  6.7  5.0* 6.7
     6.5  6.5   .4* 6.6  6.5  6.5  6.6  6.5  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.7  6.7  6.7
     6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.5  6.6  6.7
          5.5  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.5  6.7
               6.5  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6
                    6.5  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  6.6  1.5*
                              1.8* 6.6  6.6  6.6  6.6  6.6  6.6  6.6

    TOTAL VALID DIE= 332

    SHORTS DEFECT DENSITY ( 1V)  :  .2312
    TAILS DEFECT DENSITY         :  .247
    TOTAL DEFECT DENSITY ( 5.625V)  :  .4901

VOLTAGE  #FAIL   %FAIL   CUM % FAIL   DEFECT DENSITY
   1      - 26    7.83       7.83            .408
   2         3     .90       8.73            .457
   3         1     .30       9.04            .474
   5         1     .30       9.34            .490
   6       301   90.66     100.00       10000.000

DESTRUCTIVE EVENTS = 31 = 9.34%
LIMIT VOLTAGE DIE  0
TEST COMPLETED  10:45:27
```

APPENDIX II

HARDNESS MEASUREMENTS FOR Al, Al-Cu and Al-W

Al and Cu were weighed out to give the correct Al/Cu atomic ratio and were then melted at $5x10^{-6}$ torr in a conical W coil to produce a micro-ingot of Al_2Cu for Knoop micro-hardness measurements. The same type of micro-ingot of Al was also prepared. Unexpected phases formed in each case. The Al-Cu showed 2 phases to be present both with hardnesses much greater than Al, 759 and 474. See figure 1. The molten pure Al caused some of the W to melt or diffuse into the melt to form Al-W intermetallic needles with a hardness of 700 compared to 47.7 for the pure Al between needles.(65)

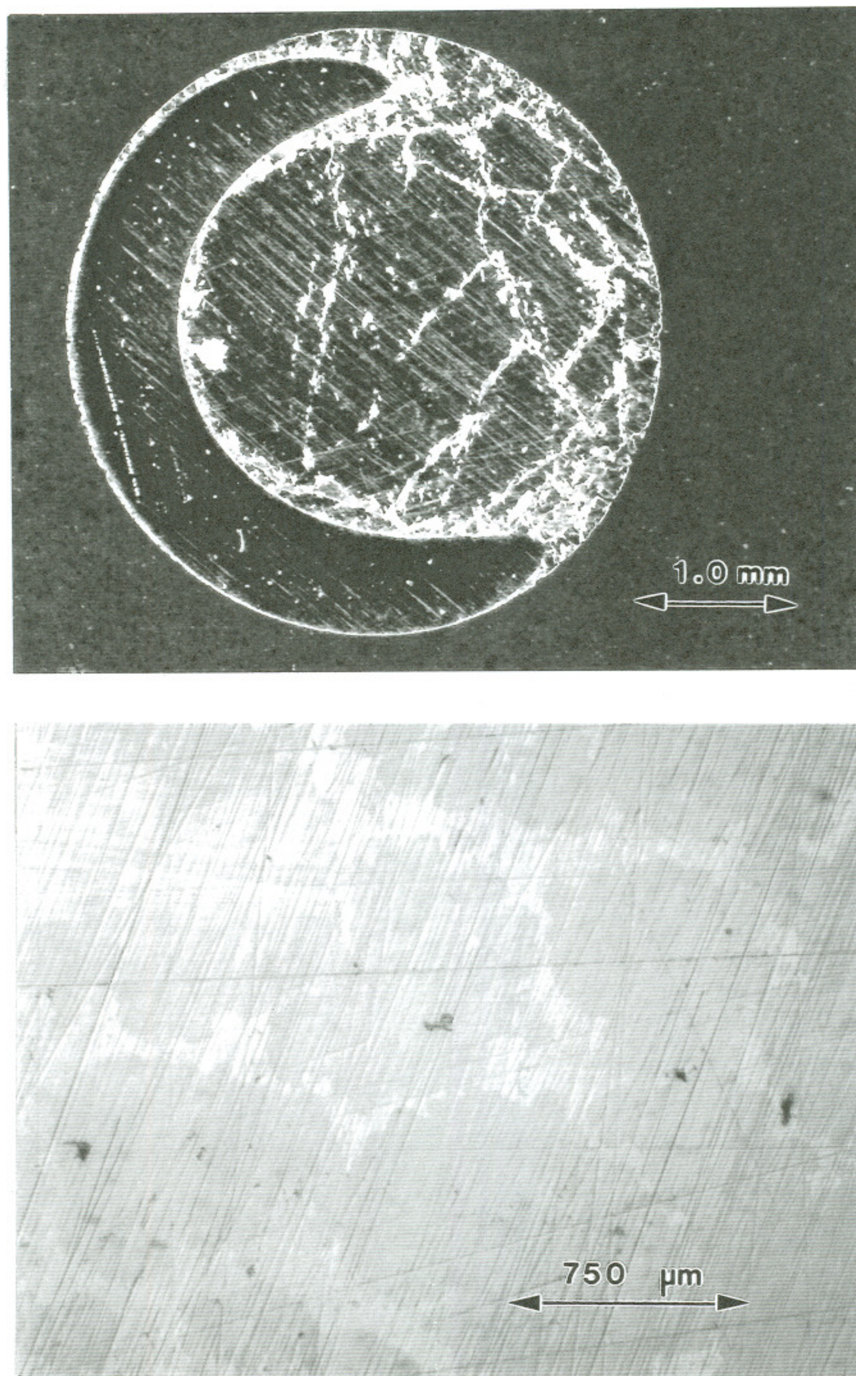


Figure1. Optical images of cross-section of W crucible containing Al-Cu intermetallic. Atomic ratio for Al/Cu is 2/1. The hardness measurements for the large grains is 759 Knoop and 474 between the large grains.

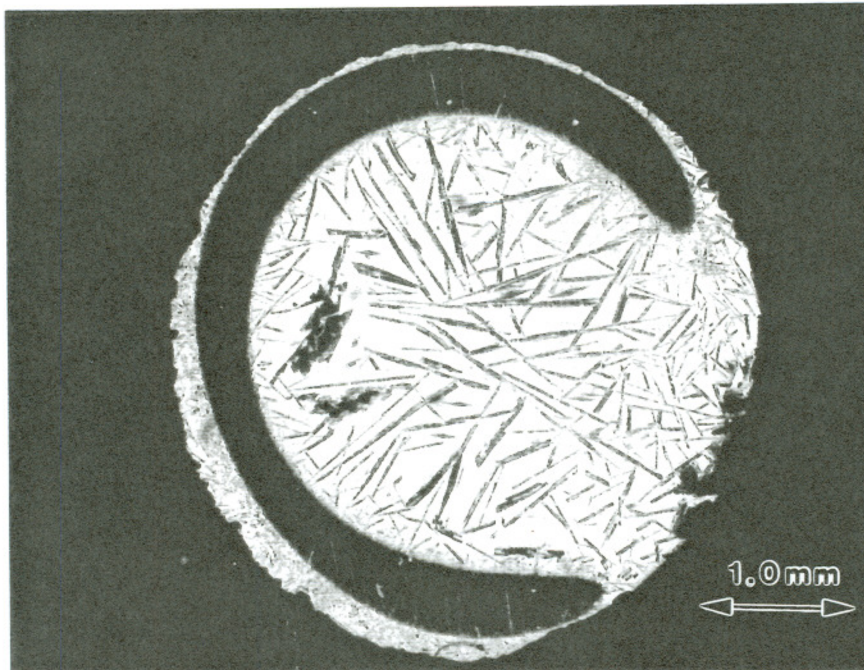


Figure 2. Optical images of cross-section of pure Al in W crucible. Knoop hardness measurements for pure Al, pt1, and the unexpected Al-W intermetallic were 47.7 and 700, respectively.

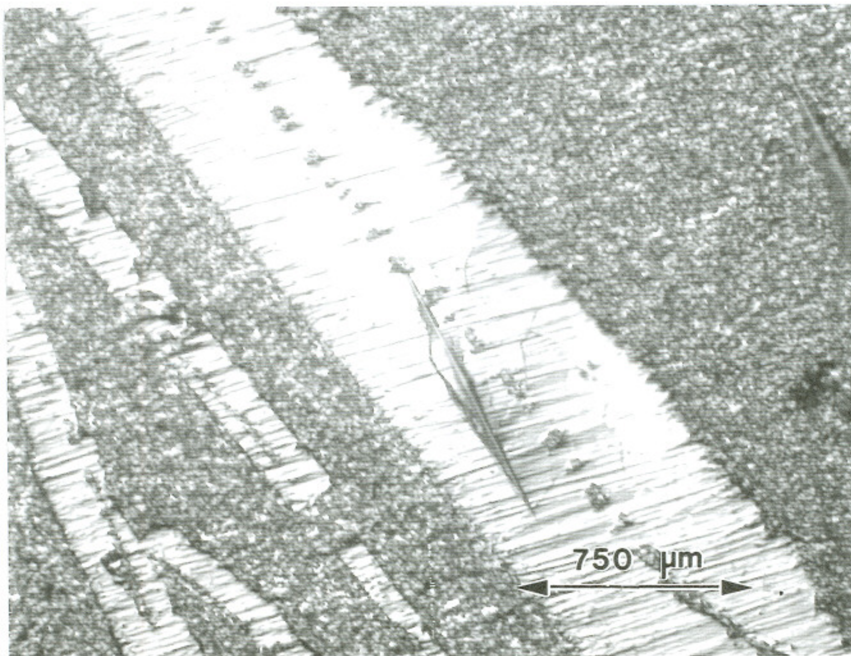


Figure 3. Shattered Al-W intermetallic needle subjected to a 100gm load during Knoop measurements. Conseqently a 10gm load was used.

APPENDIX III

DETERMINATION OF THE STRESS IN THE SiO_2 HEAT TREATED FOR 4 HRS WITH A DIRECTLY DEPOSITED Al-.5WT%Cu ELECTRODE

When the Al-.5Cu layer and Si substrate were removed to produce a planar section of the 7nm thick oxide a concave surface toward the Si substrate was observed. The compression of this thin film is caused by differences in the linear coefficients of expansion for Si and SiO_2 and excess Si, Al and Cu in the film. Measuring the depth of this concave surface would permit the measurement of compression in the film to permit the determination of stress in the film. Similar work was done by Jaccodine and Schlegel. (52)

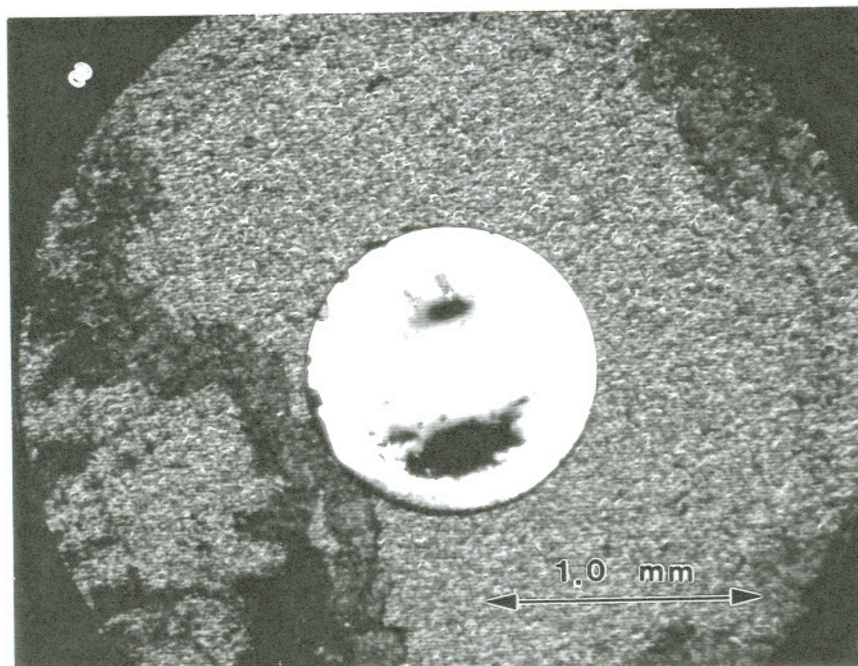


Figure 1. Optical image of concave surface produced by 7nm thick silica after 4 hrs of heat treatment at 400ºC in N_2 and removal of the metallization and Si substrate.

The depth of the concave surface of the oxide below the original surface of the substrate when the film was held in compression was measured by using an optical microscope to first focus on an area adjacent to the planar section of the 7nm oxide where substrate is still present and then focusing on the bottom of the concave surface. The relaxed oxide film is considered to be the surface of a balloon and the hoop stress is then calculated for the oxide film using the technique of Jaccodine and Schlegel.

(1) $R= (L/4)(L/2h+2h/L)$ R=radius of the oxide balloon
L= diameter of concave surface=550μm
h= depth of concave surface=11.2μm

Assuming the film to have linear elasticity and to be isotropic

(2) stress = Ee/(1-v) — E= Young's modulus for SiO_2; e= strain for the oxide film =ΔL/L=.0011

(3) ΔL=(2Ø/360)(2πR)-L — Ø= 1/2 angle subtended by the arc of oxide =4.66º

(4) stress= 8.9×10^8 dynes/cm^2 from equation (2)

Biographical Note

Born June 1, 1947 in Troy, New York. Married, wife Karen and son Justin.

Education

Received Bachelors degree in Physics from S.U.N.Y. at Stony Brook,L.I. in 1969 and Masters degree in Materials Science and Engineering from Washington State University at Pullman in 1987.

Employment

Worked as an electron microscopy technician and associate engineer for Westinghouse-Hanford 1976-88, then as a research scientist for Battelle PNL 1988-90 and presently employed at OGI as a senior research engineer.

Research Interests

Mechanisms of microstructural change in metallization and insulator nanometer scale thin films for micro-electronic applications, melt-shell reactions during casting, manipulation of Zirconium alloy microstructures to produce highly corrosion resistant alloys, the development of Focused Ion Beam(FIB) processes for the fabrication of micro-sensors and sub-micron structures and the development of materials characterization techniques using analytical electron microscopy and focused ion beam technology.

Representative Publications

J.M. McCarthy, "Microstructural Characterization of Al-.5Cu and Al-1Si on 0.6nm TCA-SiO_2/Si Following Heat Treatment at 400ºC in N_2- Mechanisms Providing Stability and a High Break Down Voltage for the Al-.5Cu MOS Device" MRS Spring Meeting Proceedings,(1995)

B.J.Herb, J.M.McCarthy, C.T.Wang and H.Ruhman "Correlation of Transmission Electron Microscopy Microstructure Analysis and

Texture with Nodular Corrosion Behavior for Zircaloy-2", Zirconium in the Nuclear Industry : Tenth International Symposium, (1994), ASTM STP1245 p.419.

F.A.Garner, J.M.McCarthy, K.C.Russel and J.J.Hoyt, "Spinodal-like Decomposition of Fe-35Ni and Fe-Cr-35Ni Alloys during Irradiation or Thermal Aging" Journal of Nuclear Materials" , **205**(1993)p.411.

J.M.McCarthy, "Phase Evolution during Neutron Irradiation of Commercial Fe-Cr-Mn Alloys", Journal Nuclear Materials **179-181**(1991)p.626.

J.M.McCarthy, L.E.Thomas, W.T.Pawlewicz, W.S.Frydrych and G.J.Exarhos, "Deposition of Dielectric Optical Coatings: A Microstructural Study of the Deposited Layers and Interfaces" MRS Symposium Proceedings **152**(1989)p.201.