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# **Pd-Ge Ohmic Contact on to GaAs Formed by the Solid Phase Epitaxy of Ge: A Microstructure Study**

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## **Dedication**

In memory of my grandfather Florea Radulescu

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# **Abstract**

## **Pd-Ge Ohmic Contact on to GaAs Formed by the Solid Phase Epitaxy of Ge: A Microstructure Study**

**by Fabian Radulescu, M.S.**

**Thesis Research Adviser: Dr. John M. McCarthy**

Driven by the remarkable growth in the telecommunication market, the demand for more complex GaAs circuitry continued to increase in the last decade. As a result, the GaAs industry is faced with new challenges in its efforts to fabricate devices with smaller dimensions that would permit higher integration levels. One of the limiting factors is the ohmic contact metallurgy of the metal semiconductor field effect transistor (MESFET), which, during annealing, induces a high degree of lateral diffusion into the substrate. Because of its limited reaction with the substrate, the Pd-Ge contact seems to be the most promising candidate to be used in the next generation of MESFET's. The Pd-Ge system belongs to a new class of ohmic contacts to compound semiconductors, part of an alloying strategy developed only recently, which relies on solid phase epitaxy (SPE) and solid phase regrowth to "un-pin" the Fermi level at the surface of the compound semiconductor. However, implementing this alloy into an integrated process flow proved to be difficult due to our incomplete understanding of the microstructure evolution during annealing and its implications on the electrical properties of the contact.

The microstructure evolution and the corresponding solid state reactions that take place during annealing of the Pd-Ge thin films on to GaAs were studied in connection with their effects on the electrical properties of the ohmic contact. The phase transformations sequence, transition temperatures and activation energies were determined by combining differential scanning calorimetry (DSC) for thermal analysis with transmission electron microscopy (TEM) for microstructure identification. In-situ TEM annealing experiments on the Pd/Ge/Pd/GaAs ohmic contact system have permitted real time determination of the evolution of contact microstructure. The kinetics of the solid state reactions, which occur during ohmic contact formation, were determined by measuring the grain growth rates associated with each phase from the videotape recordings. With the exception of the Pd-GaAs interactions, it was found that four phase transformations occur during annealing of the Pd:Ge thin films on top of GaAs. The microstructural information was correlated with specific ohmic contact resistivity measurements performed in accordance with the transmission line method (TLM) and these results demonstrated that the Ge SPE growth on top of GaAs renders the optimal electrical properties for the contact. By using the focused ion beam (FIB) method to

produce microcantilever beams, the residual stress present in the thin film system was studied in connection with the microstructure.

Although, the PdGe/epi-Ge/GaAs seemed to be the optimal microstructural configuration, the presence of PdGe at the interface with GaAs did not damage the contact resistivity significantly. These results made it difficult to establish a charge transport mechanism across the interface but they explained the wide processing window associated with this contact.

# Contents

<b>Dedication</b> .....	iii
<b>Acknowledgments</b> .....	iv
<b>Abstract</b> .....	v
<b>List of figures</b> .....	ix
<b>List of tables</b> .....	xii
<b>1. Introduction</b> .....	1
1.1 Background .....	1
1.2 Objective and thesis outline .....	2
<b>2. Theoretical considerations</b> .....	6
2.1 Introduction .....	6
2.2 Interfacial phenomena: thermodynamic and kinetic aspects .....	7
2.3 Electronic aspects of the metal/semiconductor interface .....	15
<b>3. Ohmic contacts to semiconductors</b> .....	23
3.1 The Schottky barrier formation .....	23
3.2 Ohmic contacts to GaAs .....	25
3.2.1 Ge-based ohmic contacts .....	27
3.2.2 SPE and SPR-based ohmic contacts .....	33
3.2.3 Basic GaAs device applications .....	41
<b>4. Experimental procedures and analysis</b> .....	53
4.1 Deposition of thin films .....	53
4.2 Calorimetry .....	54
4.3 Analysis of calorimetric data: determining the activation energies .....	55
4.4 Transmission electron microscopy .....	58
4.4.1 Analytical electron microscopy .....	58

4.4.2 High resolution electron microscopy.....	60
4.4.3 In-situ transmission electron microscopy .....	60
4.5 TEM sample preparation .....	60
4.5.1 Cross-sectional specimen preparation by focused ion beam .....	61
4.5.2 Planar section TEM sample preparation .....	64
4.6 Contact resistivity measurements by the transmission line model .....	64
<b>5. Phase formation sequence in the Ge/Pd/GaAs system.....</b>	<b>70</b>
5.1 Introduction .....	70
5.2 Microstructure evolution of the Pd-Ge ohmic contact on GaAs .....	72
5.3 In-situ annealing TEM study of the Ge/Pd/GaAs interfacial reactions.....	81
<b>6. The effect of stress on the Ge solid phase epitaxial growth .....</b>	<b>101</b>
<b>7. The microstructure effect on the ohmic contact performance .....</b>	<b>112</b>
7.1 Constant-heating-rate annealing experiments .....	113
7.2 Isochronal annealing experiments .....	116
<b>8. Summary and future work .....</b>	<b>133</b>

## List of Figures

2.1.	Several examples of M-GaAs isothermal phase equilibria .....	10
2.2.	Ga-As phase diagrams a) M-Ga-As with little solubility b) M-Ga-As with extensive solubility and c) M-Ga-As with ternary phase.....	11
2.3.	GaAs interface morphology as determined by the phase growth kinetics a) Ga diffuses first b) metal M diffuses first.....	14
2.4.	Metal-semiconductor charge transport mechanisms. a) Thermionic emission b) Thermionic field emission c) Field emission.....	17
2.5	Theoretical dependence of contact resistance on the doping concentration .....	19
3.1.	Solid phase fabrication methods for ohmic contacts to GaAs as suggested by Murakami.....	31
3.2	Schematic illustration of SPE with transport medium .....	35
3.3.	Schematic illustration of the SPR mechanism .....	37
3.4.	SPR mechanism scheme for GaAs.....	38
3.5.	Typical GaAs MESFET configuration .....	43
3.6	The $I_{DS}$ versus $V_{GS}$ dependance determines the MESFET's mode of operation.....	43
3.7	Illustration of a HEMT device structure.....	48
4.1.	Typical as-deposited Pd/Ge/Pd thin film stack used in this thesis .....	53
4.2.	GaAs piece of wafer attached to half Mo washer.....	62
4.3.	SEM images of typical TEM cross sections as prepared by FIB milling .....	63
4.4.	Ohmic contacts on a GaAs conductive channel where the current flow is parallel with the surface .....	66
4.5.	a) Schematic picture of a typical TLM structure used in measuring the specific ohmic contact resistivity b) Actual image of a TLM structure.....	67
4.6.	Obtaining various ohmic contact parameters by TLM plots .....	68
5.1.	DSC trace of Pd/Ge/Pd multilayer film heated at 10 °C/min. and the peak temperature associated with each solid state reaction.....	74
5.2.	Cross sectional view of an as-deposited specimen.....	74
5.3.	Cross-sectional micrograph of a sample annealed at 161 °C and quenched in He atmosphere. The arrows indicate the Ge depleted layer .....	75
5.4.	Cross-sectional micrograph of a sample annealed at 214 °C and quenched in He atmosphere .....	75

5.5.	Cross-sectional TEM image of a sample annealed at 269 °C and quenched in He atmosphere .....	77
5.6.	Cross-sectional image of a sample annealed at 322 °C and quenched in He atmosphere .....	77
5.7.	Cross sectional micrograph of the final microstructure resulted from annealing at 380 °C followed by slow cooling in a forming gas atmosphere .....	78
5.8.	High resolution TEM image of the PdGe/epi-Ge/GaAs interface.....	78
5.9.	DSC traces for Pd(20 nm)/Ge(150 nm)/Pd(50 nm) multiple thin film stacks heated from 10 to 100 °C/min.....	80
5.10.	Kissinger plots and the activation energies associated with each solid state reaction .....	80
5.11.	Video-captured TEM image of a sample subjected to rapid thermal annealing at 182 °C .....	84
5.12.	Video-captured TEM image of a sample subjected to rapid thermal annealing at 241 °C .....	84
5.13.	Video-captured TEM image of a sample subjected to rapid thermal annealing at 273 °C .....	85
5.14.	Video-captured TEM image of a sample subjected to rapid thermal annealing at 293 °C .....	85
5.15.	Video-captured TEM image of a sample subjected to rapid thermal annealing at 307 °C .....	86
5.16.	Video-captured TEM image of a sample subjected to rapid thermal annealing to 315 °C at the start of the holding period.....	86
5.17.	Video-captured TEM image of a sample subjected to rapid thermal annealing followed by holding at 318 °C for 3 min. ....	87
5.18.	Video-captured TEM image of a sample subjected to rapid thermal annealing followed by holding at 318 °C for 10 min. ....	87
5.19.	DSC scan of Pd/Ge/Pd multilayer film heated at 12 °C/min.....	89
5.20.	Temperature correction plot as established by table 5-I.....	90
5.21.	Pd <sub>2</sub> Ge isothermal growth as measured from the in-situ TEM recordings .....	91
5.22.	PdGe isothermal growth as measured from the in-situ TEM recordings .....	91
5.23.	Arrhenius plot derived from the Pd <sub>2</sub> Ge growth measurements.....	93
5.24.	Arrhenius plot derived from the PdGe growth measurements .....	93
5.25.	Video-captured TEM image of a sample annealed at 210 °C for 5 min. followed by a second holding period at 320 °C for 5 min.....	95
5.26.	Video-captured TEM image of a sample subjected to rapid thermal annealing to 318 °C followed by a holding period of 5 min. ....	95
5.27.	Dislocation along the [111] plane in the GaAs substrate that was formed as a result of a higher annealing temperatures .....	96

6.1.	Microcantilever beam structure aligned along the $\langle 011 \rangle$ direction.....	103
6.2.	Cross-Sectional TEM image of a sample annealed at 325 °C for 5 min .....	105
6.3.	Cross-Sectional TEM image of a sample annealed at 400 °C for 5 min. The arrow indicates stacking faults present in the Ge epitaxial layer .....	105
6.4.	SEM 45° tilt view of FIB produced microcantilever beams (GaAs up), deflected under the residual tensile stress present. a) Specimen heated at 269 °C and quenched in He atmosphere. b) Specimen heated at 322 °C and quenched in He atmosphere. c) Specimen heated at 325 °C for 5 min. and cooled in forming gas atmosphere. d) Specimen heated at 400 °C for 5 min. and cooled in forming gas atmosphere.....	106
7.1.	Specific contact resistivities as a function of annealing temperature. The annealing time was 5 min. for all specimens .....	117
7.2.	Cross-sectional micrograph of a sample annealed at 250 °C for 5 min. Part of Ge that was not transported to the GaAs interface remained trapped between the PdGe layers.....	120
7.3.	Cross-sectional micrograph of a sample annealed at 300 °C for 5 min .....	120
7.4.	Cross-sectional micrograph of a sample annealed at 350 °C for 5 min. ....	121
7.5.	Cross-sectional image of a sample annealed at 375 °C for 5 min. The arrows indicate stacking faults present in the Ge epitaxial layer. ....	121
7.6.	a) Cross-sectional micrograph of a sample annealed at 400 °C for 5 min. The arrow points to an area with high density of stacking faults in the Ge layer b) Magnified view of the stacking faults along the [111] planes in the Ge epitaxial layer .....	123
7.7	Three basic thin film growth modes on a substrate. a) Frank-van der Merwe or layer-by-layer growth mode, b) Stranski-Krastanov mode and c) Volmer-Weber or island growth mode .....	125
7.8.	Surface tension equilibrium at the thin film-substrate interface .....	126

## List of Tables

5-I	In-situ TEM temperature correction determination. The heating rate for both, DSC and in-situ TEM was 12 °C/min .....	89
6-I	Calculated residual stress based on the measured micro – cantilever beam deflection .....	107
7-I	Specific contact resistivity as a function of the annealing method. Three TLM structures were measured for each annealing temperature and the average values were recorded .....	114
7-II	Microstructural parameters and specific contact resistivity as a function of annealing temperature. The average values were determined by observing a minimum of 4 μm in each specimen .....	127

# **1. Introduction**

## **1.1 Background**

Understanding the ohmic contact behavior of a metal-semiconductor interface is one of the great scientific challenges still faced by the electronic materials science. The metal-semiconductor structure is a subclass of a more general scientific topic described as interface phenomena. Typically, the focus of interface research is on the unique properties present at the transition region between two materials and on understanding how these properties differ from those of the bulk solids on either side. The complex nature of the interfaces makes this subject an essentially interdisciplinary topic. For example, the properties of the interface region are influenced by various factors such as defects, formation of compounds, kinetics, anisotropy and inhomogeneities. In particular, the metal-semiconductor contacts exhibit considerable diffusion or chemical reactions at the interface. Another difficulty in characterizing them is the non-equilibrium nature of such structures as their electrical and microstructural properties depend upon how they are formed.

Ohmic contacts to semiconductors serve the key function of connecting the device to the other circuit components. In general, an ideal ohmic contact should pass current through the metal/semiconductor interface with negligible resistance, this way preserving the intrinsic electrical characteristics of the device. The electrical and metallurgical characteristics of the ohmic contacts are key issues that determine the performance of any electronic or optoelectronic semiconductor device. Over the last decades, researchers focused their attention on the metal-silicon interface study given the technological importance of this system. However, in the last decade the telecommunications market

sector continued to expand and the need for integrated circuits operating at high frequencies increased significantly. Since the silicon-based devices cannot satisfy the new high frequency needs of this market, the attention has shifted toward compound semiconductors, especially GaAs. Integrated circuits built on GaAs substrates can operate at speeds beyond the capability of Si-based ones. As the design complexity of the GaAs circuits increases, the efforts for achieving higher integration levels and more performant devices have intensified. As far as the ohmic contacts are concerned, this translates into a need for structures that are thermally stable during device fabrication process, exhibit a shallow diffusion depth of the metals into the GaAs and provide a smooth surface morphology, as well as rendering good electrical properties.

The ohmic contacts employed by most of the GaAs industry today are based on the Au-Ni-Ge thin film alloys. One of the drawbacks of this contact is the melting that takes place during annealing as Au and Ge form a low temperature eutectic system. To address this problem, research studies have sought a new ohmic metallization alloy that reacts in solid state only without the spiking apparent in the Au-Ni-Ge contact. One such non-spiking contact is the Pd-Ge thin film system. In spite of some early promising results, implementing this contact into a fabrication line proved to be rather difficult because of our incomplete understanding of the microstructure evolution and its effects on the electrical properties.

In this thesis, evaporated Pd/Ge/Pd thin films on GaAs substrates were investigated in connection with their microstructural evolution during annealing and the resulting electrical properties.

## **1.2 Objective and Outline of the Thesis**

The purpose of this thesis is to perform a microstructural study of the Pd-Ge ohmic contact on GaAs and correlate this information with its electrical properties. The Pd-Ge/GaAs system belongs to a new class of ohmic contacts to compound semiconductors, part of an alloying strategy developed only recently. This novel approach relies on two

solid state mechanisms to “un-pin” the Fermi level at the surface of the compound semiconductor. First, the solid phase epitaxy (SPE), consists of growing a closely lattice-matched material onto the substrate single crystal. The second mechanism, solid phase regrowth (SPR), takes place in two stages. In the initial stage, the substrate material forms an intermediary phase with reacting alloying elements and in the second stage, the intermediary phase decomposes into several by-products. One of them is the substrate material, which regrows epitaxially onto the unreacted substrate. The outcome of both of these mechanisms (SPE and SPR) is an epitaxial heterostructure, which modifies the electronic band structure of the original substrate surface.

The objective of this thesis is two fold. One is to gain a more complete insight into the intricacies of these two mechanisms and it is expected that understanding them would provide us with the necessary knowledge to create more accurate models. This would lead to new, more rational materials selection procedures and better ohmic contact design. Secondly, it is hoped that these results would help advance the compound semiconductor ohmic contact technology and open the path towards better devices.

Chapter 2 of this thesis describes several theoretical aspects of the metal/compound semiconductor interface. These include microstructural characteristics (e.g. phase formation sequence, interface morphology, phase equilibria) and the electrical properties (such as the basic charge transport mechanisms) present at such an interface. Several issues related to the ohmic contacts to semiconductors are discussed in chapter 3. In general, the ohmic contact behavior is influenced by the Schottky barrier present at the metal/semiconductor interface. The details of this phenomenon are still surrounded by controversy and the various models that describe the Schottky barrier formation are presented in the first part of this chapter. Then, a literature review regarding various types of ohmic contacts to GaAs is described. This leads to a framework for the materials selection needed in order to design a SPR and/or SPE based ohmic contact to GaAs, which could be further extended to other compound semiconductors. The principles derived from this analysis provide a rationale for the choice of the Pd-Ge ohmic contact

system as a replacement for the Au-Ni-Ge. In the last part of the chapter, the most common applications of the ohmic contacts to GaAs devices are illustrated.

The experimental procedures and analysis employed in this thesis are described in chapter 4. These include thin film deposition, thermal analysis, electron microscopy, focused ion beam and contact resistivity measurements.

In chapter 5, the phase formation sequence of the Pd/Ge/Pd/GaAs system is studied by combining analytical TEM with thermal analysis and *in-situ* TEM annealing experiments, which allowed for a continuous record of the dynamics of the phase transitions. Two methods are employed in order to determine the solid state reaction kinetics parameters. One involves thermal analysis and the other consists of measuring the reaction rates from the *in-situ* TEM video recordings. Both procedures provided results that were in very close agreement.

The work presented in chapter 6 examines the residual stress associated with the microstructure present in the final stages of the Pd-Ge ohmic contact formation. These results indicate that Ge solid phase epitaxial growth on to GaAs is strongly affected by the tensile stress set in the thin film system. Also, a new model that suggests that the tensile stress induced by the PdGe intermediate layer plays an important role in the Ge SPE growth was proposed. This model seems to agree with other SPE systems and provides a new view of the possible role played by the transport medium layer.

The correlation between the microstructure and the electrical properties of the contact is treated in chapter 7. In the first part of the chapter, specific ohmic contact measurements were performed in relation with the microstructural evolution observed in chapter 5. Then, the focus shifted towards the final stages of the ohmic contact formation. Isochronal annealing experiments at temperatures that correspond to the start of the ohmic behavior were performed and, once again, the microstructure information was correlated with the contact resistivity data. These correlations provided new evidence that permitted to draw original conclusions regarding the charge transport mechanism across the interface.

A summary of the entire thesis will be presented in chapter 8. Also, the possible impact of these new results on future ohmic contacts to compound semiconductor will be discussed.

## **2. Theoretical Considerations**

The ohmic contact behavior is part of a more general scientific topic which encircles the metal-semiconductor interface phenomena. In order to understand these structures, several viewpoints should be considered. In this chapter, various theoretical aspects of the metal-semiconductor interface will be analyzed. These include, electronic aspects, phase formation sequence, interface morphology and microstructure effects on the electrical properties.

### **2.1 Introduction**

The contact between metal and semiconductor involves a number of complex issues which concern the bulk and interfacial structure, composition, morphological and electrical characteristics of the metal and semiconductors. One of the goals of past and current studies concerned with these issues is the development of unambiguous, realistic models of such contacts in terms of first principles. Another goal of such research is that of obtaining better technological control of electronic devices and integrated circuits.

Electronic properties of a metal-semiconductor interface can often be predicted by the energy band diagrams. The thermal energy necessary for an electron to cross the potential barrier present at the metal-semiconductor interface is referred to as the Schottky barrier. Although it is recognized that the microstructure of a metal-semiconductor interface should influence the Schottky barrier height, this relationship has not been well established yet. One of the reasons is the complexity of the reactions that take place at such interfaces. Anisotropic and inhomogeneous effects are in place due to the polycrystalline nature of the metals and it seems obvious that any study that describes the

electrical properties of the interfaces should first characterize the microstructure. However, existing Schottky barrier models often rely on mechanisms that are not directly linked to the interface structure because such studies are difficult to perform.

The phase formation sequence and stability of bulk mixtures of materials could be predicted by using the available phase diagrams and kinetics data. However, there are no general models that would describe the microstructure evolution for the case of a thin metal film deposited on a substrate. Although considerable progress has been made in the last decade, predicting the microstructure of the relative simple metal-Si binary system is still difficult, not to mention the metallization of compound substrates. On one hand, the metal-GaAs system is more complex due to the compound nature of the substrate, and, on the other hand, it is more complex due to the fact that the metal films usually consist of two or three elements (e.g. Au-Ni-Ge the most used ohmic contact by today's GaAs technology).

This chapter will describe the basic theoretical issues regarding both the electronic aspects and the materials science of the metal-GaAs interface. Also, a literature review of the current technological status of the ohmic contacts to semiconductors, with emphasis on GaAs contacts, will be presented.

## **2.2 Interfacial Phenomena. Thermodynamic and Kinetic Aspects**

The stability of metal/GaAs interfaces is a problem of great technological importance as most common devices need metal contacts to form an active Schottky barrier or an ohmic contact. The electrical performance and operational stability of GaAs thin-film electronic devices rely on the interfacial phenomena of Metal/GaAs heterostructures. The trend toward miniaturization and integration of GaAs devices in modern microelectronics applications has imposed new requirements upon the contact metallization of GaAs. One of the limiting criteria is that GaAs contacts must exhibit appropriate and reproducible electrical properties when exposed to high temperature processing steps which are necessary for the fabrication of the GaAs circuits. While the

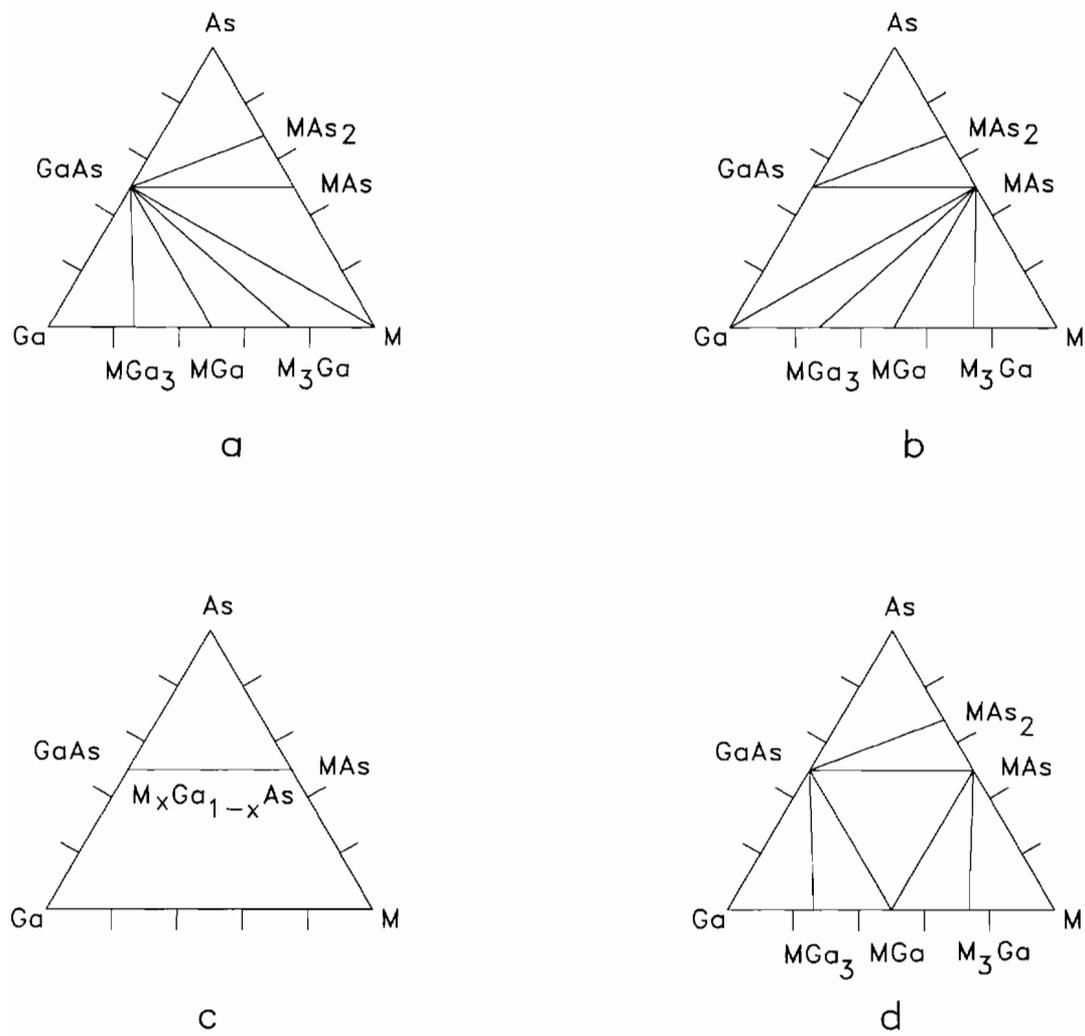
electrical functions are determined by electronic factors such as band structures, the thermal stability is governed by material factors which include thermodynamics, reaction kinetics and the interface morphology between the metallizing elements and the compound semiconductor. Specifically, the thermal stability may be achieved either by choosing a metallizing agent that is chemically stable to the semiconductor or by reducing and controlling the interfacial interaction between the metallizing agent and the semiconductor substrate. In past years, most of the research pertaining to interfacial reactions of GaAs metallization systems has concentrated on the identification of the phases formed and to some extent the resulting morphologies when elemental or multi-component metallic contacts to GaAs are exposed to specific environments. These results give only piecewise information, some of which is contradictory, and is very difficult to rationalize. They provide little basis for solving actual processing problems and have no predictive capability. The studies by Williams et al. <sup>1,2,3</sup>, Beyers <sup>4</sup>, Sands <sup>5,6</sup>, Schmid-Fetzer <sup>7</sup> and Lin et al. <sup>8</sup> have demonstrated the importance of ternary M/Ga-As phase equilibria to rationalize interfacial reactions in M/GaAs contacts and to provide some basis for choosing which elemental metal systems would make suitable contacts. However, no effort has been made to utilize quaternary or higher order phase equilibria to evaluate and predict the interfacial interactions of multi-component contacts to GaAs. This situation is unfortunate since the most common GaAs contact metallization schemes used by today's technology consist of two to three component metal alloys (e.g. Au-Ni-Ge ohmic contact).

The kinetics of binary systems, specifically those for the metallization of silicon, are not even well understood, not to mention the metallization of compound semiconductors, which involves ternary and higher order systems. Even though Kirkaldy<sup>9</sup> has solved the basic diffusion equations for ternary systems, these solutions have not been applied to tackle the Metal/GaAs systems. In fact, very few systems in the metallurgical literature have been tackled using ternary diffusion theories, due to the high complexity of the diffusion theories and the lack of availability of sufficient thermodynamic and kinetic data. For multi-component contacts to GaAs, the situation is even worse since there has

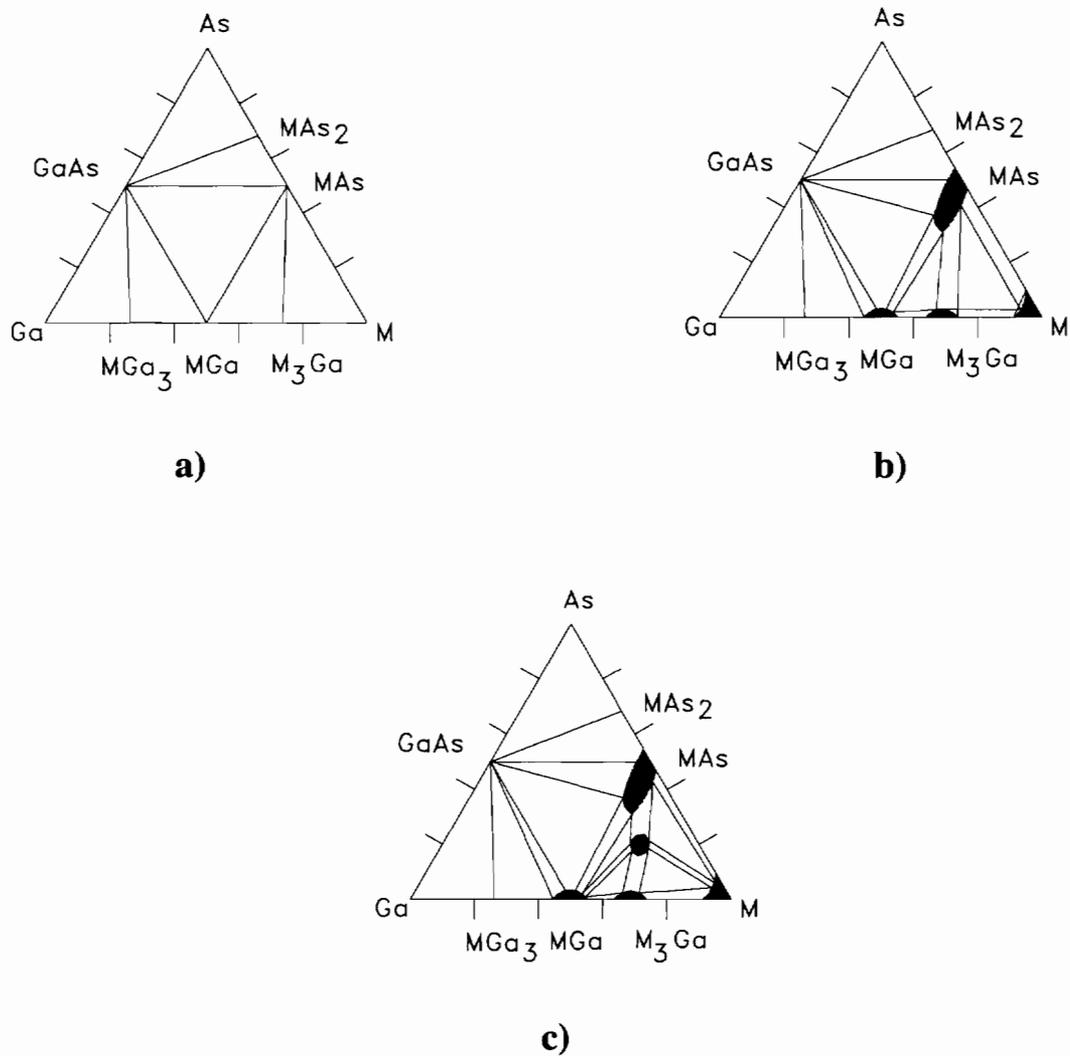
been no effort to solve the diffusion equations which are even more complicated due to the great number of component elements involved.

Beyers et al.<sup>10</sup> have given a scheme that classifies isothermal M/GaAs phase equilibria to seven basic types according to the probable phase equilibrium relationships of intermetallic phases and GaAs while neglecting the solubilities of the intermetallic phases. As far as the present understanding, only three types were identified in experimentally determined M-Ga-As phase diagrams. These three types, as well as the one that has been identified in other III-V compound systems, are depicted in Fig. 2.1. Fig. 2.1(a) shows the type where GaAs is the most stable phase, and all other phases are in equilibrium with it. Au-Ga-As, Ag-Ga-As and W-Ga-As are examples of this type of M-Ga-As systems. Phase equilibria shown in Fig. 2.1(b) has not been identified in M-Ga-As systems, where the MAs phase is the most stable phase and all other phases, including the GaAs phase, are in equilibrium with it. However, this type of phase equilibria was found in other M-III-V systems such as Ni-In-As. Fig. 2.1(c) shows a type where MAs and GaAs form a continuous solid solution, which occurs only if the component element M is a Group III element such as Al or In. Fig. 2.1(d) illustrates the type of phase equilibria which is the most common case occurring in the M-Ga-As systems. In this type of phase diagram, no single phase dominates the phase equilibrium relationships. Instead, a three-phase region is constituted among GaAs and two intermetallic phases from the M-Ga binary and the M-As binary, respectively.

Lin and Chang<sup>11</sup> classified the latter type of M-Ga-As phase diagrams into three categories, depending upon the solution behaviors of the binary phases. Fig. 2.2(a) depicts the case where the binary phases exhibit limited solubilities of the third component elements. Cr, Nb, Ir and Pt-Ga-As phase diagrams belong to this category. The diagram in Fig. 2.2(b) shows the case where the binary phase MAs dissolves a considerable amount of the counter phase "MGa". The symbol "MGa" denotes an unstable phase MGa which exhibits the MAs structure. Ni-Ga-As and Co-Ga-As phase diagrams belong to this category.



**Figure 2.1. Several examples of M-GaAs isothermal phase equilibria**



**Figure 2.2.** M-Ga-As phase diagrams a) M-Ga-As with little solubility b) M-Ga-As with extensive solubility and c) M-Ga-As with ternary phase

Fig. 2.2(c) describes another case where, in addition to extensive solubilities of MAs, MGa,  $M_3Ga$  and M, there exists a ternary phase T with a composition lying along the GaAs-M join. The Pd-Ga-As system falls into this category.

The appearances of the three types of phase diagrams depend upon the relative stabilities of the competitive phases, the phase stabilities of the component elements and the intermetallic phases, and the thermodynamic solution behaviors of the solution phases. In order to predict the phase diagrams of M-Ga-As accurately, it is necessary to know the Gibbs free energies of the binary phases and the solution behaviors of the phases with extensive solubilities. Schmid-Fetzer <sup>7</sup> has calculated several M-Ga-As phase diagrams based upon estimated enthalpies of formation of intermetallic phases by Miedema's model. However, for those systems in which the binary phases exhibit complex solution behavior, phase diagrams must be determined experimentally. It is obvious from Fig 2.2 that in all the cases, the M/GaAs contacts will undergo chemical reactions when subjected to sufficiently high temperatures. In some cases, a sufficiently high temperature may be only 100 °C or even lower. However, in view of the many types of phase equilibria exhibited by M-Ga-As systems, the kinetics of the reactions in M/GaAs couples are often quite different.

Thermodynamics tells us about what will happen when equilibrium conditions are achieved but does not tell us how the intermediate phases are configured. It is difficult to tell from the phase diagrams what phases will form when M is in contact with GaAs. While only one arrangement of the phases is possible in a binary couple, this is not true for a ternary or higher order couple. To rationalize this problem, several viewpoints should be considered. These include diffusion path, phase formation sequence and interface morphology.

The diffusion path is defined as the arrangement of phases in a diffusion couple where the primary concern is the configuration of the intermetallic phases between M metal film and GaAs. According to Kirkaldy and Brown <sup>12</sup>, a semi-infinite diffusion couple of a ternary systems has only one diffusion path. Although it is possible in principle to calculate the diffusion path, it is practically impossible to accomplish this,

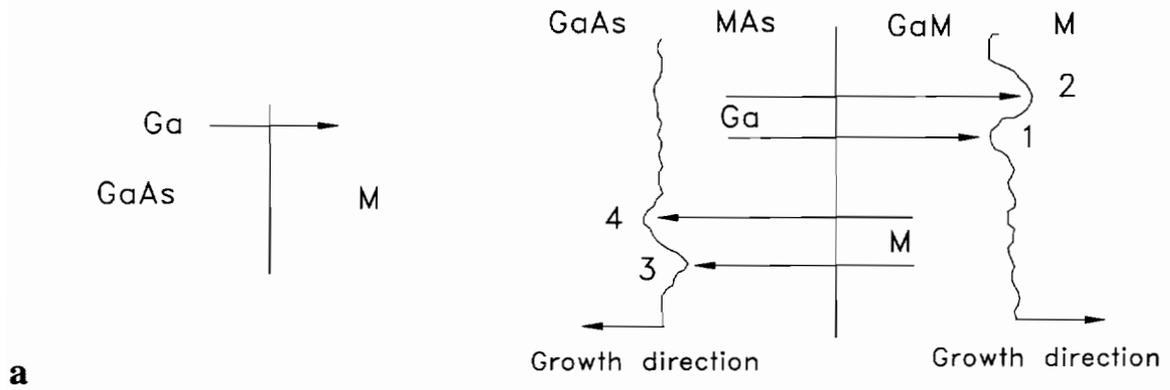
given the current state of our understanding of ternaries such as M-Ga-As. For bimetallic contacts to GaAs, where two metals are going to be deposited on GaAs, the possible diffusion paths become even more complicated. Experiments must be done to determine the diffusion path for a GaAs-M couple. From a device point of view, it is important to know which of these phases is in contact with GaAs under equilibrium conditions.

The initial and transient phase configuration for bulk and thin-film diffusion couples have been argued to be different in the literature<sup>13,14</sup>. The intermediate phase growth in the bulk has been reported to be parabolic and simultaneous ( for those systems involving only equilibrium phases ). On the other hand, sequential growth is observed in the thin-film case, i.e., the intermediate phases grow one by one. This discrepancy has been attributed to nucleation barriers<sup>15</sup>, interfacial reactions<sup>16</sup>, strain energy (lattice mismatch) in the case of thin-films and difference in the diffusion mechanisms. In bulk diffusion couples, an infinite supply of the two end phases is realized. This is not the case for a thin metal film deposited on a substrate. The metal thin-film may be consumed during the growth of the first phase. The diffusion controlled mechanism explanation is that all the equilibrium phases exist initially and the diffusivities and large homogeneity ranges account for the different initial thicknesses of all the phases. The thicknesses of some phases are so small that they cannot be detected by regular analytical means. After the consumption of the metal film, the diffusion flux in the phase next to the metal is suppressed, and the phase next to it has a chance to grow. Sequential phase growth is then observed.

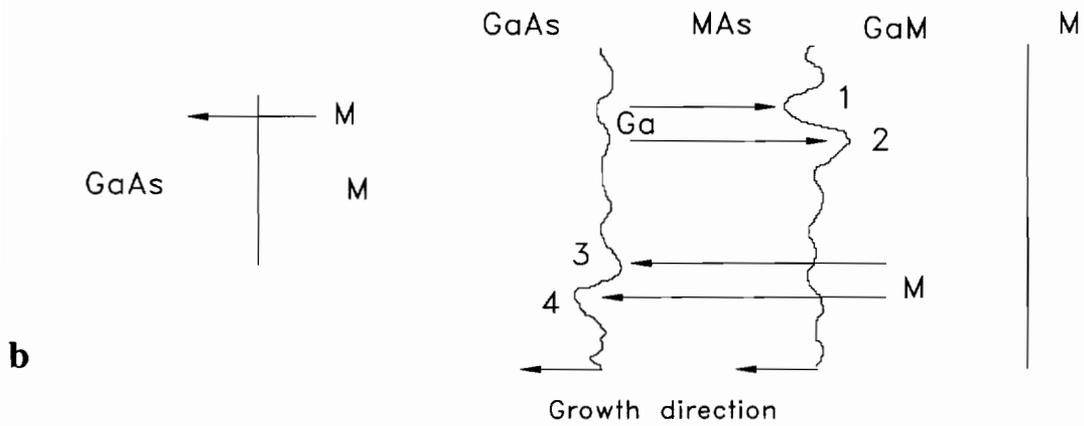
The interface morphology is determined by the growth kinetics of the phases in a couple. Wagner<sup>17</sup> has considered the morphological and kinetics aspects of displacement reactions in the solid state and established the criteria for the stability of a flatly grown interface. Rapp<sup>18</sup> and co-workers have utilized this concept to study reactions in M/oxide and M/sulfide couples. These rules were applied to M/GaAs diffusion couples by Lin et al.<sup>19</sup> and are discussed below.

In Fig. 2.3(a), assuming that the initially predominant moving species is Ga and that As diffuses the slowest, the growth of MGa and MAs would necessarily occur at the

Case I: Ga diffuses initially



Case II: M diffuses initially



**Figure 2.3. M-GaAs interface morphology as determined by the phase growth kinetics a) Ga diffuses first b) metal M diffuses first**

MGa/M and GaAs/MAs interfaces, respectively. A moving interface is referred to as a growth front. The growth of MGa and MAs is controlled by the diffusion of Ga and M, respectively. The flux of Ga arriving at position 1 exceeds that at position 2 resulting in the formation of a planar MGa/M interface. Similarly, the flux of M arriving at position 3 exceeds that at position 4, again resulting in the formation of a planar GaAs/MAs interface. On the other hand, in case II, as is shown in Fig. 2.3(b), the species M is the predominant moving element for the growth of MGa and MAs. In this case, the growth fronts of MGa and MAs are at the MAs/MGa and GaAs/MAs interfaces, respectively. If the rate-controlling step for the growth of MGa is the diffusion of Ga, then the growth rate at position 1 is higher than that at position 2. Under these circumstances, a planar MAs/MGa interface would be unstable. The situation for the GaAs/MAs interface is the same as that in Fig. 2.3(a) and therefore the interface remains planar. If As is the predominant moving element, the evolution of the interfaces would be similar to the first case where Ga is the prevailing diffusion specie. However, in practice, it was noted that Ga tends to be the first element to outdiffuse.

From the above discussion, it may readily be seen that a knowledge of the predominant moving element and the rate controlling steps to phase growth are the key points to understanding and predicting interface morphologies.

In this section, several features that determine the microstructural characteristics of the metal-GaAs interface were discussed. Models that describe the interaction between a metal and GaAs in an attempt to predict the interface thermodynamics, kinetics and morphology were reviewed.

### **2.3 Electronic Aspects of the Metal/Semiconductor Interface.**

When a metal contacts directly onto n-type GaAs, the valence and conduction bands of the semiconductor bend to make the Fermi levels in the metal and the semiconductor equal <sup>20</sup>. The carrier transport mechanisms through this M-S interface are strongly influenced by the donor concentration in the semiconductor and the temperature.

Three typical cases are shown in Fig. 2.4, for n-type GaAs.  $\phi_b$  is the energy difference between the Fermi level in the metal and the bottom of the conduction band of GaAs at the interface. Fig. 2.4(a) shows the situation where GaAs is lightly doped ( $N_d < 10^{17} \text{ cm}^{-3}$ ). In this case the depletion width is very wide and the electrons cannot tunnel through the GaAs interface. The only way the electron can transport between the GaAs and the metal is by thermionic emission (TE) over the potential barrier  $\phi_b$ . Fig.2.4(b) illustrates the band diagram of the metal contacting GaAs doped at an intermediate level of  $10^{17}$ - $10^{18} \text{ cm}^{-3}$ . In this case, the electrons can partially tunnel through the interface and both the thermionic and tunneling processes are equally important. The current flow is controlled by electrons with some thermal energy tunneling through the mid-section of the potential barrier. This is called thermionic-field emission (TFE). When the semiconductor is extremely heavily doped ( $> 10^{18} \text{ cm}^{-3}$ ), the electrons can tunnel through from the Fermi level in the metal into the semiconductor. This process is called field - emission (FE), which is shown in Fig 2.4(c).

A useful parameter indicative of the electron tunneling probability is  $kT/E_{00}$ , where  $E_{00}$  is a characteristic energy. This is defined by:

$$E_{00} = (qh/4\pi)(N_d/m^*\epsilon)^{1/2}$$

where:

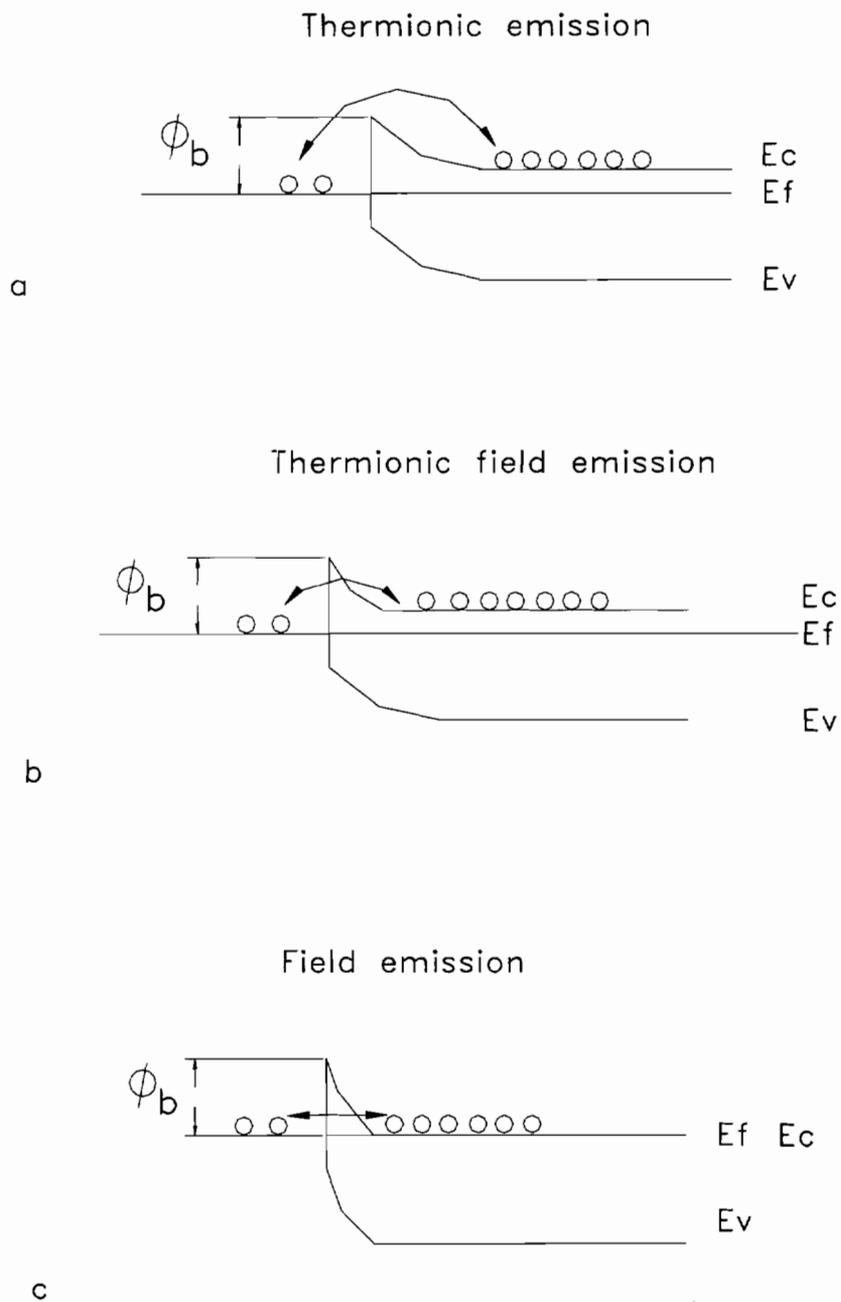
q is electron's charge

h is Planck's constant

$m^*$  is the effective mass of tunneling electron

$\epsilon$  is the dielectric constant of the semiconductor.

It can be noted that when  $E_{00}$  is high relative to thermal energy  $kT$ , the probability of electron transport by tunneling increases. Therefore, the ratio  $kT/E_{00}$  is a useful measure of the relative importance of the thermionic process to the tunneling process. For low doping levels,  $kT/E_{00} \gg 1$ , thermionic emission is the dominant current flow



**Figure 2.4. Metal-semiconductor charge transport mechanisms. a) Thermionic emission b) Thermionic field emission c) Field emission**

mechanism. For  $kT/E_{00} = 1$ , both thermionic and tunneling current flow take place. For  $kT/E_{00} \ll 1$ , the tunneling mechanism dominates the current flow.

The specific contact resistance  $\rho_c$  is given by the reciprocal of the derivative of current density with respect to voltage:

$$\rho_c = (\delta J / \delta V)^{-1} |_{V=0}$$

The current-voltage relationships could be approximated and the following expressions for  $\rho_c$  are derived:

$$\rho_c = C_1 \exp(q\phi_b/kT) \text{ for TE,}$$

where:

$$C_1 = (k/qA^*)T, A^* \text{ being the Richardson constant}$$

For contacts with heavy doping in which the tunneling process is the dominant current transport mechanism,  $\rho_c$  is given by <sup>20</sup> :

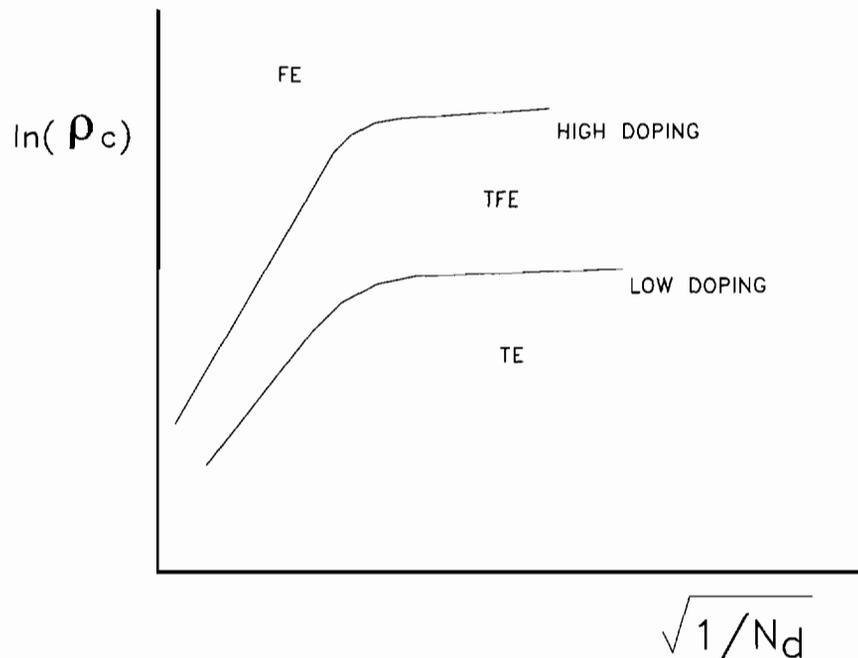
$$\rho_c = C_2 \exp(q\phi_b/E_{00})$$

where  $C_2$  has a weak temperature dependence.

For contacts in which thermionic-field-emission is the dominant transport mechanism,  $\rho_c$  is given by <sup>20</sup> :

$$\rho_c = C_3 \exp[\phi_b/N_d \coth(E_{00}/kT)]$$

where  $C_3$  is a function of  $\phi_b$  and  $T$ .



**Fig. 2.5 Theoretical dependence of contact resistance on the doping concentration**

In order to show the dependence of  $\rho_c$  on doping level,  $N_d$ , and barrier energy,  $\phi_b$ , the expected  $\rho_c$  values are plotted in Fig. 2.5 as a function of  $(1/N_d)^{1/2}$  for two  $\phi_b$  values. In the FE region,  $\ln(\rho_c)$  depends linearly on  $(1/N_d)^{1/2}$  with slope  $4\pi(\epsilon m^*)^{1/2} \phi_b / h$ . In the TE region  $\rho_c$  is independent of the doping concentration and is equal to  $(kT/qA^*)\exp(\phi_b/kT)$ . The TFE region bridges the two. For contacts with lower  $\phi_b$ , the  $\rho_c$  values become smaller in the entire  $N_d$  range. Excellent agreement of contact resistances predicted by the above theory and experiments was observed for contacts to n-type Si<sup>21</sup>. In typical device applications employing ohmic contacts to GaAs, the substrate was doped at levels higher than  $10^{17} \text{ cm}^{-3}$ . For these contacts, TFE and FE are the dominant current transport mechanisms. To prepare low-resistance Ohmic contacts, the reduction of the barrier height ( $\phi_b$ ) and an increase of the doping level ( $N_d$ ) in the GaAs are essential. As a

corollary, it can be pointed out that there are three approaches to reduce the  $\rho_c$  values of the contact:

- 1) by increasing the doping level ( $N_d$ )
- 2) by reducing the barrier height ( $\phi_b$ )
- 3) by combining the two above.

These choices have great implications in the new GaAs ohmic contact materials selection process as it will be further explained in the following chapter.

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## 3. Ohmic Contacts to Semiconductors

### 3.1 The Schottky Barrier Formation

The fundamental understanding of the Schottky barrier formation at the interface between two materials is still an area of intensive investigation. This is fueled by the fundamental interest in the problem and by the technological needs for reliable contacts to semiconductors as a part of electronic or optoelectronic devices. Two distinct types of contacts are fundamental components of many devices:

- 1) Ohmic, low resistance contacts that exhibit a linear I-V dependence.
- 2) Schottky, rectifying contacts that exhibit a non-linear I-V behavior.

The performance characteristics of the device are strongly influenced by the properties of both types of contacts. In spite of numerous studies performed in the last decades, two important issues remain to be solved: the basic mechanism responsible for the Schottky barrier formation and the reproducibility and stability of the electrical properties during annealing or aging.

According to the Schottky model, the barrier height is simply the difference between the Fermi level in the metal and the minimum of the conduction band in the semiconductor at the interface. This model predicts that the Schottky barrier is proportional to the work function of the metal. Thus, by choosing different metals, one may obtain contact behavior ranging from ohmic to rectifying. Although the Schottky model was somehow successful in predicting the characteristics of the metal/Si contacts, it was not the case for the metal/GaAs contacts. It was found that for most metal/GaAs

contacts, the barrier height is independent of the metals, a phenomenon described as the Fermi level “pinning”.

The Bardeen model attributed the Fermi level pinning to the existence of a large number of surface states at the metal-semiconductor interface. It was assumed that a thin insulating layer separates the metal and semiconductor, this way, the barrier height would be independent of the work function of the metal.

A wide variety of semiempirical models seek to estimate the Schottky barrier height on the basis of phenomenological correlations. Kurtin et al.<sup>1</sup> proposed that the barrier height is proportional to the electronegativity of the metal, rather than the work function of the metal. Mead and Spitzer<sup>2</sup> proposed a rule that the barrier height was about two thirds of the semiconductor’s band gap, which was found valid for GaAs, GaP and AlAs. However this rule did not hold for InP, InAs and GaSb. Another model was proposed by McCaldin and McGill<sup>3</sup>, known as the “common anion rule”. They showed that Schottky barrier height was inversely proportional to the electronegativity of the anion of the semiconductor. Another model in this category was described by Tersoff<sup>4</sup> and known as the charge neutrality model. Various studies applied these models either singly or in combinations in order to analyze experimental measurements of the Schottky barrier height.

The theoretical models developed in the more recent years could be divided into two categories: models that assume the existence of lattice defects near the interface and models that include only the properties of the ideal metal/semiconductor interfaces. The later are also known as metal-induced gap states (MIGS) models<sup>5</sup>, which argue that electronic interactions between metal and semiconductor take place, even if no metallurgical reactions occur at the interface. The defect models<sup>6</sup>, on the other hand, suggest that the Fermi level pinning is generated by the near surface charged lattice defects (e.g. anion vacancies, and antisite defects), which are screened by their associated “image” charges in the metal.

Despite the large effort made so far in this research area, a model that would derive the metal-semiconductor Schottky barrier height from the first principles, has not

been yet universally accepted. More studies that would correlate the microstructure with the electrical properties of the metal-semiconductor interfaces are required in order to achieve this goal. Recently, a new experimental approach to study the Schottky barrier formation was demonstrated by Monch<sup>7</sup>. He used an ultrahigh vacuum system to build a metal-semiconductor contact atom-by-atom. This method allowed observing the role of the kinetics of the metal film growth on the value of barrier height and the non-equilibrium character of the metal-semiconductor interface. Also, the relatively new atomic force microscopy (AFM) studies regarding the surface materials science is expected to make new inroads in the fundamental understanding of the interfaces.

### 3.2 Ohmic Contacts to GaAs

The problem of the ohmic contacts to GaAs and other III-V semiconductor compounds is a long-standing electronic materials issue. In fact it was one of the reasons that prevented some of the compounds from becoming main stream substrate materials for IC fabrication. In contrast with the elemental semiconductors, the III-V compounds are more likely to be damaged during processing. Thermal instability and surface dissociation at relatively low temperature are the main drawbacks of the III-V compounds in comparison with the elemental semiconductors. Moreover, the increased number of chemical species present at the interface enlarges the complexity of the problem. The early attempts to rationalize the reactions that take place during ohmic contact formation on to III-V compounds and their effect on the electrical properties produced many controversial results. The sense of frustration present among scientists was expressed by Rideout<sup>8</sup> in his review article who said: “the ohmic contact technology had developed thus far more as a technical art than as a science”. A lot of progress was made since Rideout’s statement but some fundamental questions still remain unanswered. Good review articles were written in the past<sup>9</sup> and they all point out the wide mixed diversity of materials used in an attempt to provide a more acceptable ohmic contact. At the same time, a multitude of mechanisms were reported to be responsible for the ohmic behavior

of the contacts which reflects the lack of an unified model capable of describing these phenomena.

As described in section 2, according to the Schottky model, there are three means to reduce the specific contact resistance:

- 1) by increasing the doping level ( $N_d$ )
- 2) by reducing the barrier height ( $\phi_b$ )
- 3) by combining the two above.

The ohmic contacts can also be classified by the fabrication method employed in producing the ohmic contacts. The two methods used are: atomic epitaxial growth - Molecular Beam Epitaxy (MBE) and Metalorganic Vapor Phase Epitaxy (MOVPE) - and common thin film depositions followed by alloying at an elevated temperature. The first method allows for a very tight control of the grown films as far as the thickness, composition and type of doping used. The second method is the one mainly used in production, the main disadvantage is the fact that heat has to be applied in order to alloy the deposited metals. Far better results are obtained by using MBE and MOVPE but these techniques are very expensive and, so far, they have been used in research only. On one hand this alloying process produces phases and microstructures that are not predictable and reproducible but on the other hand the process is simple and inexpensive.

Based on the electron transport mechanisms listed above, and the fabrication methods, the Ge based ohmic contacts reported in the literature will be discussed in the following section.

### 3.2.1 Ge-Based Ohmic Contacts to GaAs

In order to better understand the Pd-Ge ohmic contact to GaAs, in this chapter, the more general Ge based ohmic contacts will be reviewed. Various aspects concerning the quality of these contacts will be treated.

One way of facilitating the electron transport across the contact is by increasing the tunneling probability. This can be achieved by doping the GaAs as heavily as possible close to the metal/GaAs interface. However, doping the GaAs substrate is not a trivial matter. The most common dopants are Si, Sn and Te and they were proven unable to dope GaAs to high levels. The dopants segregate to form clusters and are not electrically active as carriers in GaAs. MOVPE and MBE techniques have the advantages of permitting the doping of GaAs with dopants higher than their solubility limits and controlling the site (n or p) during deposition.

The most successful technique for obtaining increased doping levels was MBE, which produced low resistivity contacts to GaAs. Si seems to be the most suitable dopant for MBE grown ohmic contacts. It was proven to be insensitive to the growing conditions, it is less amphoteric than other dopants and it allowed for doping concentrations of up to  $10^{20} \text{ cm}^{-3}$ .

Germanium also was used as a dopant in MBE grown ohmic contacts. Ge was found to have a strong amphoteric behavior<sup>10</sup> in ion-implanted GaAs substrates, and GaAs layers with opposite polarities (n- or p-type) were produced depending on ion dose and annealing temperature. Similar behavior was observed in MBE grown GaAs layers; n- and p-type GaAs layers were grown with Ge on the same substrate simply by changing the substrate temperature and/or the As to Ga flux ratio during growth<sup>11</sup>.

Another technique to dope GaAs heavily with donors, by pulsed annealing using laser or electron beams, has been reviewed by Palmstrom and Morgan<sup>12</sup>. High doping concentrations of  $1 \times 10^{19} \text{ cm}^{-3}$  were achieved by depositing a thin film containing dopants on the GaAs surface prior to pulsed annealing<sup>13</sup>. However, this technique

produced a high density of crystalline defects in GaAs<sup>14</sup> making this technique impractical for device applications.

Another approach to lowering the contact resistivity is to reduce the barrier height present at the metal/GaAs interface as illustrated in Fig 2.4. However, taking advantage of this transport mechanism in the case of GaAs proved to be difficult due to the Fermi level pinning phenomenon mentioned in chapter 3.1. When a metal thin film is deposited on GaAs and then annealed, it was found that the Fermi level of the GaAs is pinned at the middle of the energy gap<sup>15</sup>, independently of the metal's work function.

Atomic epitaxially-grown ohmic contacts with intermediate Ge layers doped heavily with donors were first prepared by Stall et al.<sup>16</sup> by MBE. Ge was chosen as an intermediate layer, because Ge has not only a low energy gap but also Ge can be doped to higher levels than GaAs. Also, the lattice parameter of Ge is close to that of GaAs and density of crystalline defects such as misfit dislocations is expected to be extremely small. The small electron affinity difference between Ge and GaAs (approx. 60 mV) does not act as a significant barrier to electron flow. Ge layers doped with As at levels as high as  $1.4 \times 10^{20} \text{ cm}^{-3}$  were grown on the GaAs substrate which was doped with Se to the level of  $1.5 \times 10^{18} \text{ cm}^{-3}$ . Then, Au metal was deposited onto Ge layers to measure the contact resistivity values by TLM. The barrier height at the metal/Ge interface was assumed to be about 0.5 eV. This contact provided an extremely low contact resistivity of  $1 \times 10^{-7} \Omega \text{ cm}^2$ . Similar contacts with intermediate Ge layers were prepared by MOVPE where the Ge layers were doped with P at a level of  $1 \times 10^{19} \text{ cm}^{-3}$ <sup>17</sup>. TiPtAu metals were deposited onto Ge/GaAs and the contact resistivity values were measured to be  $1 \times 10^{-5} \Omega \text{ cm}^2$ . One of the big advantages of preparing ohmic contacts by MOVPE is that the Ge layers can be selectively grown in SiO<sub>2</sub> windows, providing a simple fabrication process for GaAs devices.

The MBE or MOVPE grown contacts satisfy most requirements for integrated circuits but their major disadvantage is the high cost associated with the MBE and MOVPE reactors. In spite of some efforts to cut these costs down by building larger reactors, these methods do not seem to be a viable solution for producing commercial

GaAs integrated circuits in the near future. That is the reason the vast majority of research related to the GaAs ohmic contacts is focused on using more cost effective and simple fabrication methods.

The “alloying” method is a more conventional technique in which contact materials are deposited on GaAs and subsequently annealed. However, the control over this process is poor due to the complex metallurgy of the contact elements. The doping level and formation of phases with low energy gap are very sensitive to dopants in the metals, deposition methods, GaAs surface cleanliness, metallurgical systems, deposition sequence, annealing method, temperature, time, etc. In addition, these contacts are far from the ideal ohmic contact, because reaction between the contact metal and the GaAs substrate during annealing is extremely complicated.

The Au-Ni-Ge ohmic contact was introduced about three decades ago and, at that time, the addition of Ni to the Au-Ge alloy represented a major improvement in reducing the surface roughness. Furthermore, several other advantages were noted: improvement of adhesion by depositing a thin first layer of Ni, improvement of reproducibility and improvement of device reliability. These contacts had a wide process window and could be prepared by various annealing methods such as conventional furnace anneal, laser anneal, or pulse lamp anneal. Therefore, these contacts had become the industry standard and they are still extensively used by the current GaAs technology. The devices used in that period demanded a simple process to fabricate ohmic contacts, which was more important than other requirements. In the recent years however, the situation has changed. The GaAs based circuits are integrated on a larger scale and the control over the device dimensions became very important.

By examining the Au-Ge phase diagram, one notices the melting point of Au decreases from 1063 °C to 356 °C by adding Ge up to 12 wt.%. The optimum contacts were obtained by annealing at temperatures between 440 °C and 550 °C which rendered contacts with resistivities in the mid  $10^{-7} \Omega \text{ cm}^2$ <sup>18</sup>. However, lateral diffusion of the contacts was observed in as-prepared Au-Ge-Ni contacts and the contact materials diffused into the GaAs substrate to a measured depth of about 0.2  $\mu\text{m}$ . These large

vertical and horizontal diffusions were due to melting of the contact metals and dissolution of the GaAs during annealing at temperatures above 360 °C. The Au-Ge-Ni contacts were thermally unstable at temperatures above 350 °C (after contact formation) even though the contacts were prepared at temperatures higher than 400 °C<sup>18</sup>. Moreover, Au reacted with GaAs forming low-melting-point phases, which caused the thermal instability.

Germanium-based ohmic contacts prepared by a conventional technique have been most extensively used in the research of GaAs devices. Even though the current transport mechanisms across these Ge-based ohmic contacts are not clearly understood at the moment, it seems that Ge plays two roles in reducing the contact resistance: increases the doping concentration at the metal/GaAs interface and reduces the barrier height of the interface by forming an intermediate thin Ge layer between the metal and GaAs. It appears that the presence of Ge is beneficial for the electrical properties of ohmic contacts prepared by the alloying method. However, in designing new Ge-based ohmic contact schemes, one should exclude the use of gold. This would improve the thermal stability of the structure and contact morphology as long as the new component doesn't form a low melting eutectic with Ge.

Several attempts were made in replacing Au with other metals (refs) (e.g. Al, Ag) that exhibit higher melting temperature in the eutectic mixture with Ge but no conclusive experimental data for improved thermal stability were yet presented. This situation pointed toward considering new alloying strategies that would lead to ohmic contact formation through solid phase interactions. It would also be preferable if the reaction with the GaAs substrate would be as limited as possible. In his review article<sup>19</sup>, Murakami indicated three strategies for developing new GaAs ohmic contacts by solid state reactions and they are represented in Fig. 3.1. Method A was first demonstrated by Fukada et al. which used As, P and Si ions to implant the Ge layer and Au as the cap metal. The structure had to be annealed at 800 °C, in order to activate the implants, which is high for a typical GaAs integrated circuit thermal budget. Moreover, the minimum contact resistance obtained was in the  $10^{-4} \Omega \text{ cm}^2$  range. The other two methods are

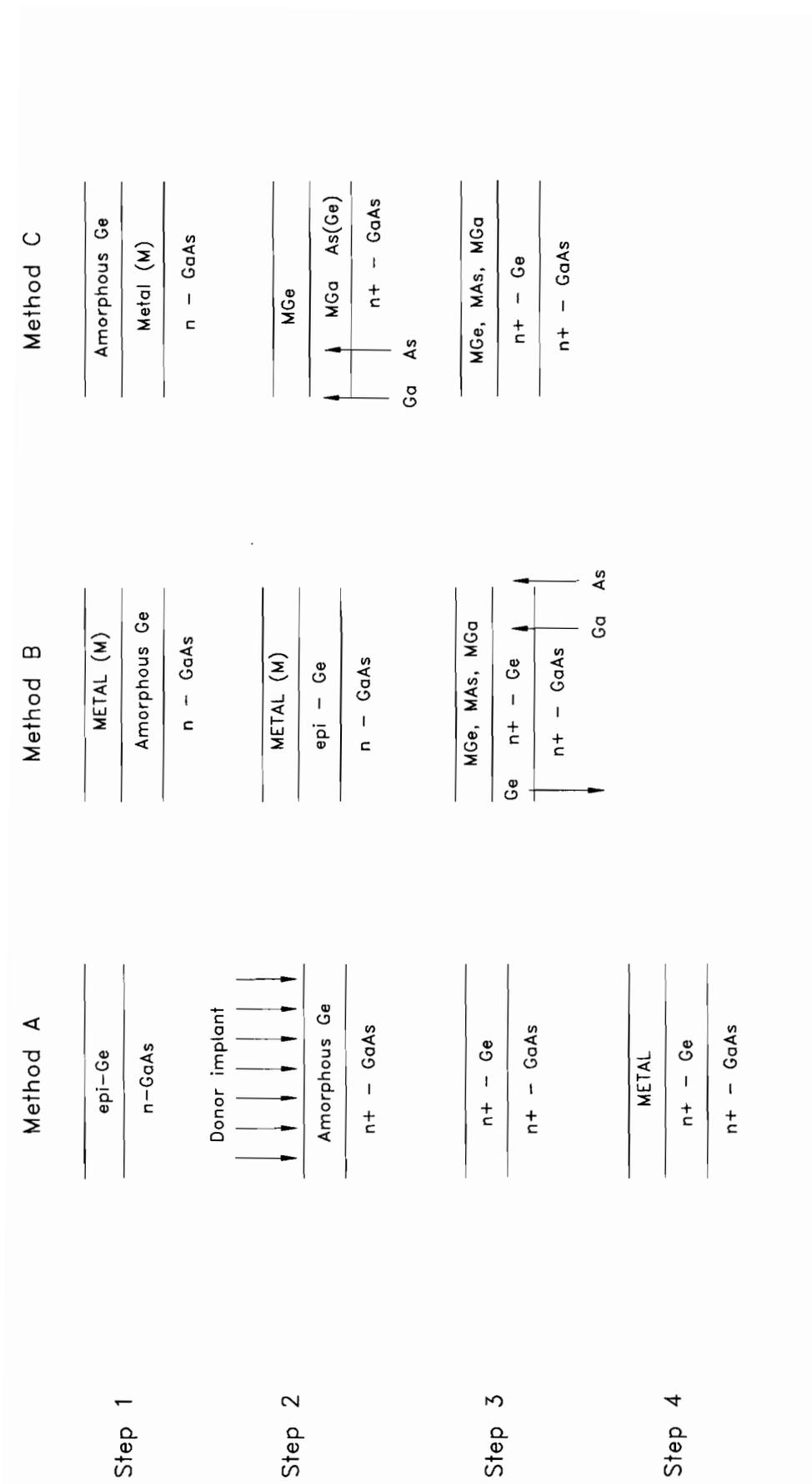


Figure 3. 1. Solid phase fabrication methods for ohmic contacts to GaAs as suggested by Murakami.

similar with only one difference that is the initial deposition sequence. In method B a-Ge was deposited first followed by the metal whereas in method C the metal is initially in direct contact with the GaAs substrate. However, after annealing, the final microstructure would be identical, metal compound/n<sup>+</sup> epi-Ge/n<sup>+</sup>-GaAs. From this class of ohmic contacts, Ni and Pd were the metals that received most of the attention in regard with using the fabrication method B and C. Several attempts to develop a better quality contact were described in the literature and some common features were noted. There was no evidence of melting taking place even though some annealing procedures used relatively high temperatures. It appears that their thermal stability is higher than Au-Ni-Ge contacts. These first promising findings fueled more research activity around these structures in spite of the fact that earlier studies reported relatively high contact resistivities. Both contacts appear to perform better if method C is employed, the metal has to be initially in contact with the GaAs.

Anderson et al.<sup>20</sup> prepared Ni-Ge contacts by method B. In order to form epitaxial Ge layers during deposition, the substrate was kept at temperatures higher than 425 °C, and Ni layers were deposited onto the epitaxial Ge layers. These contacts showed Schottky behavior in the as-deposited state. Ohmic behavior with a contact resistivity value of  $3 \times 10^{-5} \Omega \text{ cm}^2$  was obtained after annealing at 550 °C. These contacts were stable at 350 °C for 6 h. A more complex contact system was demonstrated by Wurfl et al.<sup>21</sup> who prepared Ge/Ni/WSi/Au contacts by e-beam evaporation and annealing using method B. The minimum contact resistivity of these contacts was  $4 \times 10^{-5} \Omega \text{ cm}^2$  which was obtained after annealing at 635 °C. The dominant phases detected were NiGe compounds. NiGa, NiAs, and NiGe compounds, which are expected to form in the Ni-Ge ohmic contacts, have high melting points. The excellent thermal stability observed in these NiGe contacts was believed to be due to the lack of low-melting-point compound formation. Microstructural analysis of these contacts showed that intermixing of Ge/GaAs and out-diffusion of Ga and As toward the contact surface occurred after annealing. The authors believed that transition from Schottky to ohmic behavior after annealing is due to

heavy doping of As of the Ge layer and Ge doping of the GaAs interface, forming the n+ regions.

Pd-Ge contacts were first developed by Sinha et al. <sup>22</sup> by using method B. They deposited sequentially Ge and Pd with a thickness of 50 nm each by e-beam evaporation and annealed the Pd-Ge contacts at 500 °C. The contacts provided contact resistivity values of  $3.5 \times 10^{-5} \Omega \text{ cm}^2$  to n-GaAs. Although the resistivity values were higher than those of the Au-Ge-Ni contacts, the surface morphology was very smooth. Grinolds and Robinson <sup>23</sup> used a similar method to obtain comparable Pd-Ge contacts.

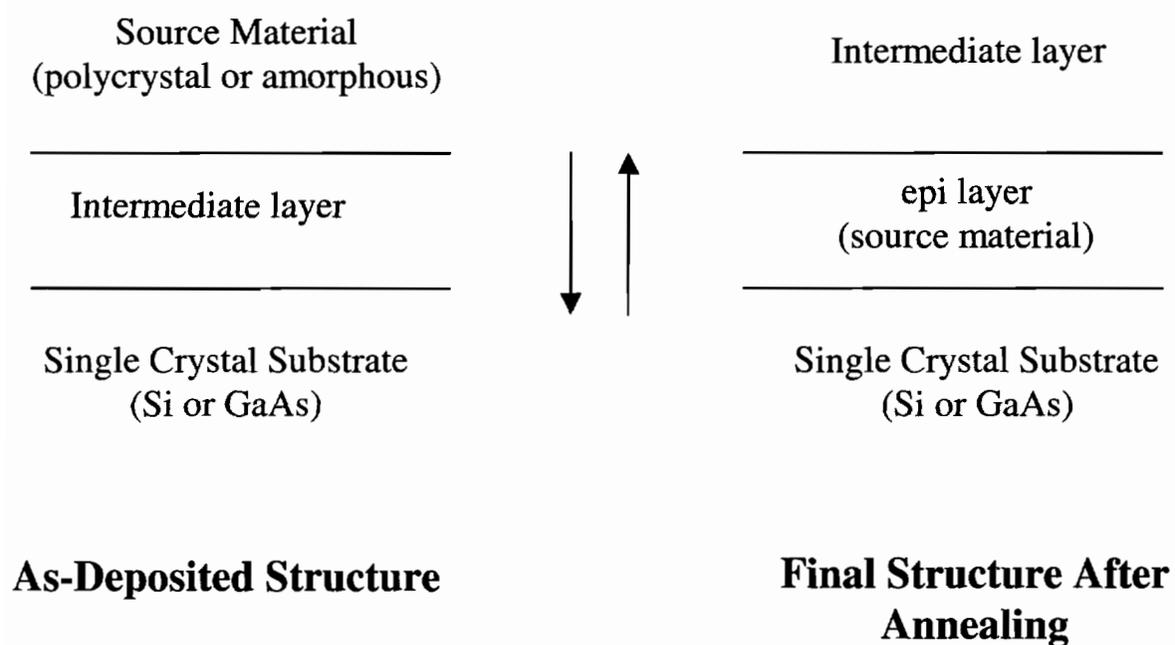
The most promising ohmic contacts prepared according to method C were the ones that used Pd and Ni as the intermediary metal between Ge and GaAs. This may be due to the fact that Pd and Ni are the only known metals to form ternary phases with GaAs <sup>24</sup>. The effect of this early interaction in forming the contact is not yet clearly understood but several hypotheses will be discussed in chapter 6. The beneficial effects of having Ni and Pd in direct contact with the GaAs substrate was demonstrated for other contact systems like Si-Ni, In-Pd, Si-Pd and Sb-Pd. It was clearly shown for the Si-Ni system that a solid phase GaAs regrowth (SPR) mechanism takes place as the  $\text{Ni}_x\text{GaAs}$  ternary phase forms in the early stages of the reaction and then decomposes at higher temperatures. This concept of ohmic contact formation was demonstrated by Sands et al. <sup>25</sup> for the Ni-Si contact and, by analogy, its validity was extended to the rest of the Ni and Pd based systems although clear analytical proof was not yet provided <sup>26</sup>. The SPR of GaAs and the solid phase epitaxy (SPE) of Ge on top of GaAs are two mechanisms that, currently, are at the heart of a new ohmic contact paradigm. This new class of ohmic contacts will be treated as a separate group in the following section.

### **3.2.2 SPE and SPR Based Ohmic Contacts to GaAs**

Starting several decades ago, the solid phase epitaxial (SPE) growth phenomenon was mostly studied in connection with the re-crystallization of the post-implanted amorphized semiconductor materials like Si, Ge and to less extent GaAs. Other studies

attempted to use this mechanism as an alternative method for growing epitaxial films. This approach was attractive because of its simplicity as opposed to more expensive techniques such as MBE, MOCVD and even the lower vacuum CVD method. Some degree of success was demonstrated in case of growing homoepitaxial systems like Si/Si and Ge/Ge. However, this method had not reached a production status and its use was mainly scientific. Excellent reviews<sup>27,28</sup> treating the SPE growth in general, were written in the past which, mainly, described cases of homoepitaxial growth on elemental semiconductors. One special class of SPE growth is represented by the SPE processes that involve transport media, which are illustrated by Fig.3.2. This form of SPE was demonstrated for the homoepitaxial growth of elemental semiconductors (Si and Ge) with metals as transport media. The metals employed fall into two fundamentally different categories: simple eutectic forming systems (e.g. Au, Al, Ag) and systems that formed compounds like Pd<sub>2</sub>Si and PdGe. In the first category of metals the source material would grow epitaxially on to the substrate by a dissolution-precipitation mechanism. For the later type of metals, the source material was probably transported to the substrate interface by grain boundary diffusion. The exact role played by the transport medium is not yet understood and a new model will be proposed in chapter 6 of this thesis.

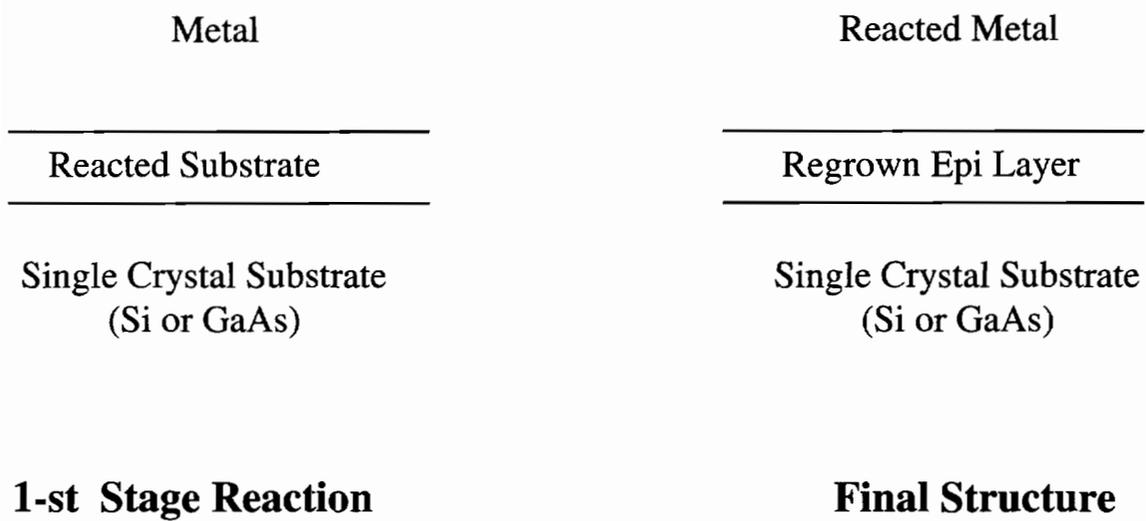
It wasn't until the last decade that cases of technologically important solid phase heteroepitaxy with transport medium were reported. Renewed interest in the method was generated by the new processing requirements imposed on the ohmic contacts to Si and GaAs substrates. In the recent years, promising results were reported in regard to CoSi<sub>2</sub> epitaxial growth on Si through different transport media –the titanium mediated epitaxy (TIME)<sup>29</sup> and the oxide mediated epitaxy (OME)<sup>30</sup> methods- and these SPE systems are currently under intensive research. But the first reported case of solid phase heteroepitaxial growth with transport medium and probably the most studied such system, was the Ge/Pd/GaAs<sup>31</sup>. The motivation for studying these systems is two fold. On one hand, they would provide a more uniform and stable ohmic contact. On the other hand one may fabricate new types of devices (e.g. metal base heterostructure bipolar transistors) without the expense of using MBE deposited heterostructure



**Figure 3.2 Schematic illustration of SPE with transport medium.**

If SPE describes a set of reactions that do not include the substrate, the SPR mechanism refers to the epitaxial redeposition of a modified layer of the top substrate material. The principle of the method is illustrated in Fig.3.3. In stage I, the substrate uniformly interacts with the metal either by forming an intermetallic or by simply dissolving in a solid solution. In stage II, the interlayer phase (solution), formed in stage I, decomposes and one of the byproducts is the substrate material, which regrows epitaxially on top of the unreacted substrate. This newly regrown layer would exhibit slightly different electrical properties mainly due to the inclusion of dopants. One of the requirements that the SPR system would have a practical importance in device fabrication is the uniformity of the reaction layer. The interaction between metal and semiconductor should be isotropic in both stage I and II. For example, at the Al/Si interface, it would not be practical to make use of the SPR mechanism because Al dissolves Si preferentially along the  $\langle 111 \rangle$  planes which leads to the formation of “spikes” into the substrate. On the other hand, Au dissolves Si more uniformly and this property was exploited by Ma et al.<sup>32</sup> who used the Ge/Au/Si SPR system to grow a SiGe/Si heterostructure. The choice of the metal in a GaAs SPR system is dictated by the same interface uniformity needs. In this case, selecting a metal that would dissolve both As and Ga would be more difficult. It was speculated the role of Au in the Au-Ge-Ni contact is to dissolve both As and Ga and to create a GaAs regrown layer nevertheless however, there was no clear analytical proof to support this prediction. One other way of achieving this goal is to use a metal that would react uniformly with Ga and As by forming a ternary phase,  $M_x\text{GaAs}$ . The decomposition of this ternary phase would be driven by the addition of a fourth element D. Fig. 3. 4 illustrates the principle of the SPR mechanism for compound semiconductors. This element would play two roles in the SPR based contacts. Firstly, it would form a stable  $M_x\text{D}$  compound to extract the GaAs from the ternary phase according to the reaction:





**Figure 3.3. Schematic illustration of the SPR mechanism**

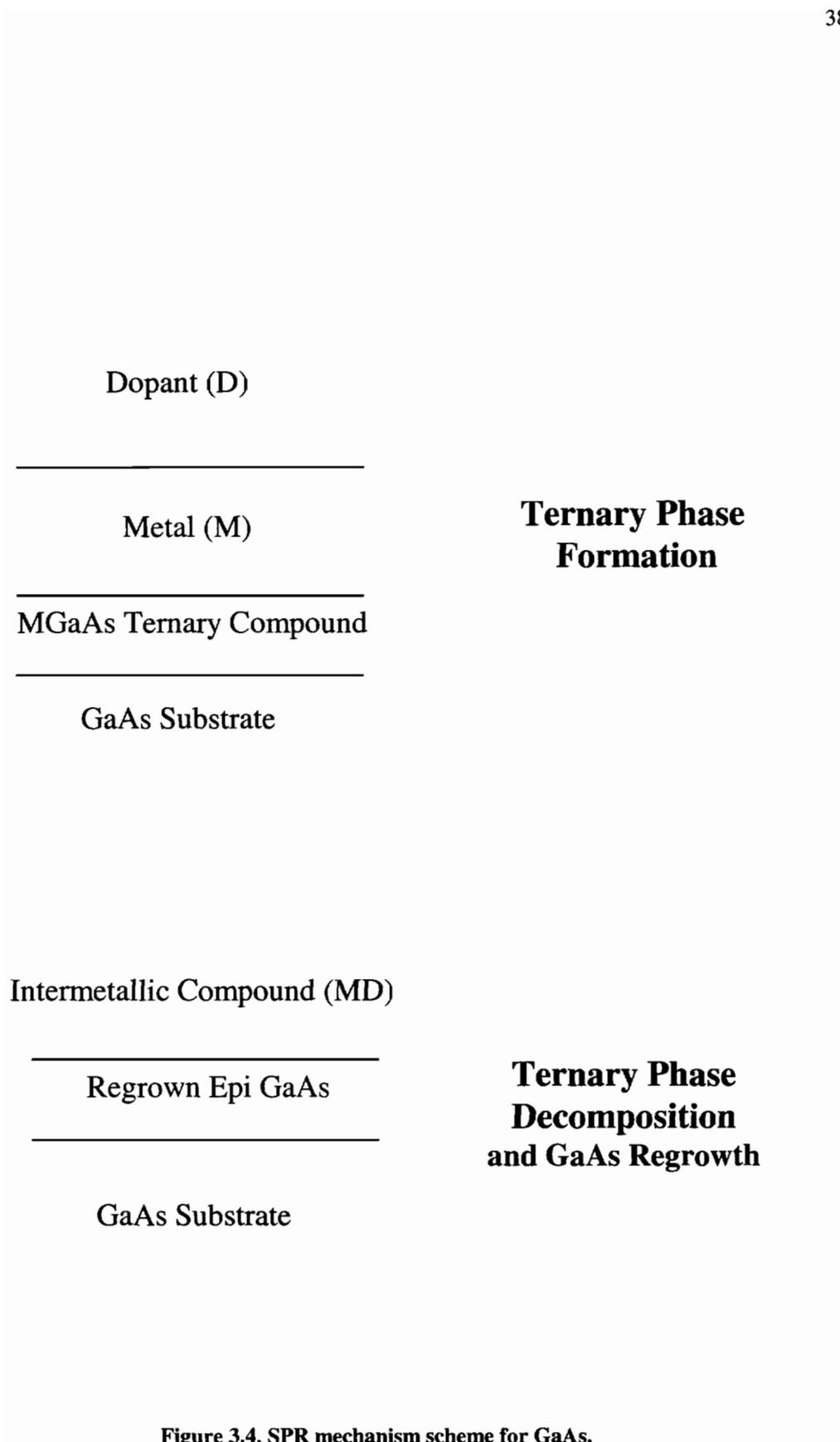


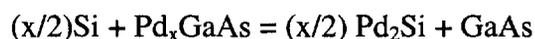
Figure 3.4. SPR mechanism scheme for GaAs.

Secondly, it would act as dopant for the GaAs regrown layer. The only metals that are known to form ternaries with GaAs are Pd and Ni and the choice of the dopant D would be Si and/or Ge. When Ge is used as dopant, then the SPE mechanism may also become possible due to the close lattice match between Ge and GaAs. On the contrary, it is very unlikely that Si would grow epitaxially on GaAs because of the large lattice mismatch set at such an interface. Based on the experimental evidence presented so far, the M-Si systems seemed to depend solely on the SPR mechanism to form ohmic contacts on GaAs whereas the M-Ge systems may rely on a combination of both SPE and SPR. The extent of SPE versus SPR and the importance of each mechanism in determining the ohmic behavior of the M-Ge contacts is still under scientific debate. For example, the charge transport mechanism seen across the Pd-Ge ohmic contact is still surrounded by controversy<sup>33</sup>. The focal point of the argument is whether the ohmic behavior of the contact can be explained by an enhanced Ge doping of the regrown GaAs – the doping model – and/or by As doping of the Ge epitaxially grown layer – the heterojunction model.

The Pd-Si contacts were studied by Wang et al.<sup>26</sup> who suggested a SPR mechanism is responsible for the ohmic behavior of the contact. According to their conclusions, Pd reacts with GaAs to form the ternary phase:



Then, the ternary intermetallic decomposes in the presence of Si according to:



The Pd<sub>2</sub>Si forms at the Pd/Si interface which renders the final microstructure, Pd<sub>2</sub>Si/n<sup>+</sup>-GaAs (Si-doped)/GaAs. A similar SPR mechanism was demonstrated by Sands et al.<sup>25</sup> for the Ni-Si contact. The final microstructure was identified by TEM and RBS analysis to contain the NiSi/n<sup>+</sup>-GaAs (Si doped)/GaAs stack.

For the Ge based contacts that form this category, the extent of SPE and/or SPR was not yet clarified. Kolawa et al.<sup>34</sup> prepared Ni-Ge contacts by using sputter-deposition techniques where Ni was directly deposited onto the GaAs substrates (method C). They deposited Ni/Ge/WN/Au onto GaAs and annealed at 500 °C for 10 min. A contact resistivity value of  $2 \times 10^{-6} \Omega \text{ cm}^2$  was obtained and this contact was stable at 500 °C for 1h. Although the detailed microstructure analysis of the Ni-Ge contacts has not been carried out, the Ge/Ni/GaAs reaction is believed to be similar to that shown in Fig. 3.1 (method C), which was assembled based on microstructure analysis of Ni/GaAs contacts and preliminary X-ray diffraction study of a Ge/Ni/GaAs contact. First, an intermediate phase of  $\text{Ni}_x\text{GaAs}$  containing Ge and NiGe will be observed at the initial stages of annealing when excess Ni over that necessary for NiGe compound formation exists. At the later stages, this  $\text{Ni}_x\text{GaAs}$  phase will decompose into NiGe and GaAs. The low resistance observed in this Ni-Ge contact is believed to be due to reduction of the barrier height by forming an As-doped Ge SPE grown layer between the compound and GaAs. Other, more recent studies showed the final contact is thermally stable at high temperatures, which makes it very attractive for device application. These studies, however, suggest the SPR is the key mechanism responsible for good ohmic behavior of the contact.

The most promising solid state contact to replace the Au-Ni-Ge appears to be Pd-Ge. These contacts tend to have lower resistivities than other SPR (or SPE)-based contacts and the process window appears to be wider. Another advantage is that the Pd reaction with the GaAs substrate is very limited whereas the formation of the ternary  $\text{Ni}_x\text{GaAs}$  consumes a large amount of GaAs. This feature makes the Pd-Ge contact a very attractive choice for heterostructure based devices such as HEMT's and HBT's.

Marshall et al.<sup>31</sup> studied systematically the effects of deposition sequence and thicknesses of Ge and Pd layers on the contact resistance. They found that the fabrication process influenced strongly the contact resistance and that deposition of Pd directly onto the GaAs substrates and excess Ge over that necessary for PdGe formation were essential to prepare low-resistance contacts. They prepared PdGe contacts with low resistivities,

approximate  $2 \times 10^{-6} \Omega \text{ cm}^2$ , which was an order of magnitude lower than those reported by previous Pd-Ge contact studies. It was concluded that the dominant current transport mechanism is tunneling. Grinolds and Robinson<sup>23</sup> also reached the same conclusion from their own measurements. These contacts had not only a very smooth surface, but also shallow vertical diffusion depth, which makes them attractive for VLSI devices.

Although there are some important issues that still need to be addressed, the SPR and SPE mechanisms show potential for providing a better quality ohmic contact to GaAs. Their main advantages stem from the fact that no melting occurs during the contact formation process. A framework for the materials selection that would be needed in order to design a SPR and/or SPE ohmic contact system was provided in this section.

### 3.2.3 Basic GaAs Device Applications

This section will briefly describe the geometry and the operation of the most important GaAs devices.

In most cases, a Schottky barrier results when a metal is placed in intimate contact with a semiconductor, in our case n-type GaAs. From an electrical point of view, the Schottky barrier is equivalent with a diode. At the M/S interface there exists a region depleted of carriers (electrons in our case). This area is called a depletion region and its thickness is a function of the voltage applied between the metal and the semiconductor<sup>35</sup>. Since there are no mobile carriers in the depletion region, this area acts as a voltage-modulated capacitor between metal and the undepleted part of GaAs. The boundary between the depleted area and the undepleted area is assumed sharp and in this case, the depletion thickness is given by:

$$\omega = 2\epsilon (V+V_{bi})/qN$$

where:

$\omega$  is the thickness of the depletion region

$q$  is the electron charge

$\epsilon$  is the dielectric constant of the semiconductor

$N$  is the doping concentration

$V$  is the applied voltage

$V_{bi}$  is the "Built in" voltage

The presence of  $V_{bi}$  means that a depletion region exists even in the absence of an applied voltage. A negative voltage will expand the depletion region whereas a positive voltage will decrease the thickness of the region. Breakdown will occur if we apply a voltage too large in the positive direction (forward) or in the negative direction (reverse). For voltages between the forward and reverse breakdown, the thickness of the depletion layer may be controlled by the applied voltage.

The field-effect transistor is the main GaAs device for analog circuits and digital logic. Several types of FET's were developed and used in IC production starting with 1952. The metal-semiconductor field effect transistor (MESFET), illustrated in Fig. 3.5, consists of two ohmic contacts called the "source" and the "drain" that allow the current to flow into and out of the substrate. Between the source and the drain, there is a rectifying contact called the "gate". The MESFET relies upon the use of a metal-semiconductor Schottky barrier to form the gate structure. The substrate under the contacts consists of two layers: a conductive GaAs layer and a semi-insulating GaAs layer. The conductive layer is called the "channel" and is made by doping the semi-insulating substrate. In any FET device, it is only the channel underneath the gate electrode which is modulated by the gate bias, and strictly speaking it is only this "intrinsic" portion of the FET that behaves ideally, according to the models. The regions either side of the gate form parasitic resistances connecting the intrinsic FET to the outside world.

The MESFET lies at the heart of GaAs IC technology today and its performance determines the final quality of the IC's both analog and digital. This is the motivation of studying its functions and the need of improving its properties.

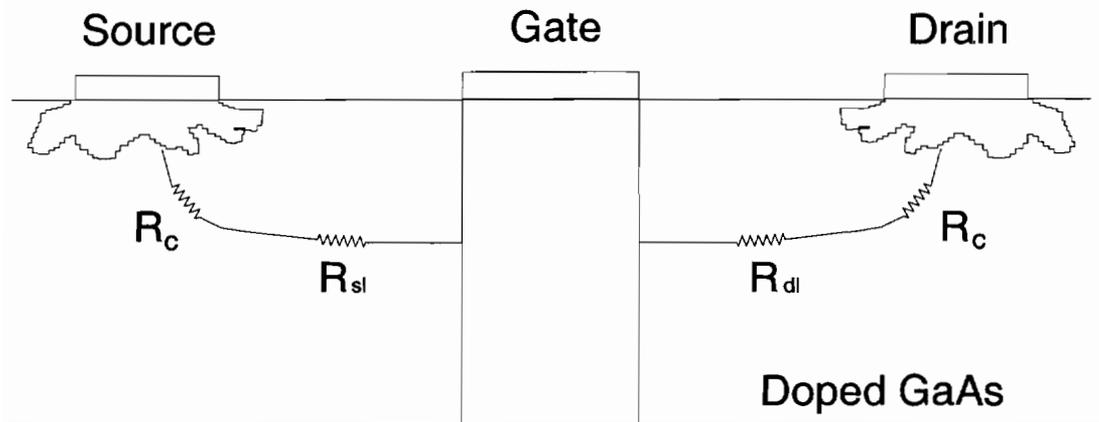


Figure 3.5. Typical GaAs MESFET configuration

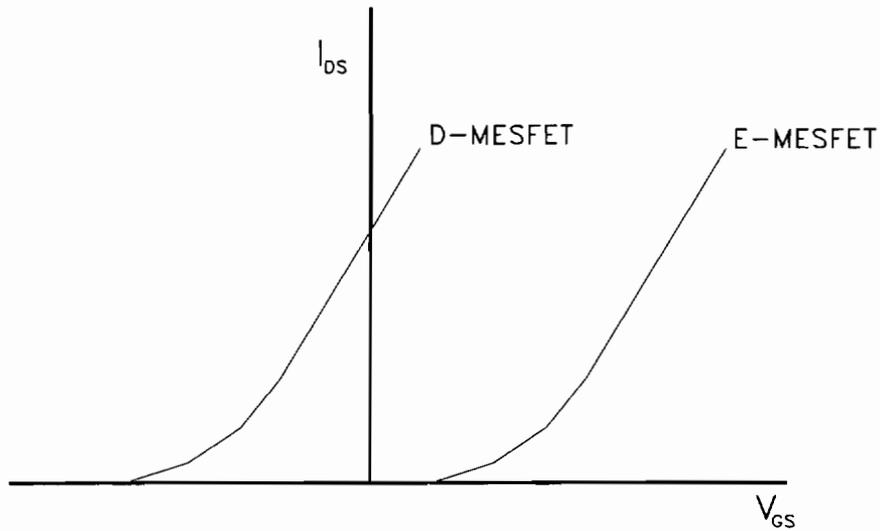


Figure 3.6. The  $I_{DS}$  versus  $V_{GS}$  dependence determines the MESFET's mode of operation

If no voltage is applied to the gate contact ( $V_G=0$ ), then at small source-drain voltages ( $V_{DS}$ ) the channel current ( $I_{DS}$ ) is linearly dependent on  $V_{DS}$  as given by:

$$I_{DS}=V_{DS}/R_{DS}$$

where  $R_{DS}$  is the total drain-source resistance and equals  $2(r_c+r_{channel})$ ,  $r_c$  is the contact resistance.  $r_{channel}$  is given by:

$$r_{channel}=L_{DS}/q\mu_n n a W$$

where:

$n$  = carrier density

$\mu_n$  = drift mobility of carriers

$a$  = channel thickness (doping depth minus the surface depletion layer)

$W$  = device width

$L_{DS}$  = drain-source separation

$q$  = electron charge

At large  $V_{DS}$ , this linear relationship stops reflecting the dependence of the electron velocity on electric field strength.

The current through the rectifying (Schottky) contact is given by <sup>36</sup> :

$$I_G = A T^2 L W \exp(-qV_{bi}/kT) \exp(qV_G/nkT)$$

where:

$A$  = the effective Richardson constant =  $8.8 \text{ cmK}^{-1}$  at 300 °K

$T$  = the temperature

$L$  = contact length

$W$  = contact width and

$n$  = ideality factor (usually in the range 1.1 - 1.2)

The equation is often approximated to:

$$I_G = I_S \exp(qV_G/kT)$$

$I_S$  is the saturation current and indicates the magnitude of the gate leakage current under reverse-bias conditions ( $V_G$  negative).  $V_{bi}$  is a constant known as the "built-in" voltage of the diode, and is dependent on the materials used.  $V_G$  is the bias applied to the metal side of the Schottky diode.  $V_G$  must be positive to forward bias the diode. As  $V_G$  approaches  $V_{bi}$ , the resistance of the contact drops rapidly and appreciable conduction can occur. For negative bias, Schottky diodes on n-type GaAs generally have  $V_{bi}$  in the range 0.7 - 0.8 V versus 0.4 - 0.6 V for Si devices. This is an advantage exploited in some digital ICs as  $V_{bi}$  limits the noise margin in this circuits. If a Schottky diode is placed in between two ohmic contacts, then it is possible to modulate the thickness of the diode depletion layer by varying the bias on the Schottky contact and thus the resistance of the channel between the ohmic contacts. This is the basis of operation of the MESFET structure. It is only in the region directly under the gate that resistance is modulated; this area is known as the active region of the MESFET.

It is possible to control the drain-source current ( $I_{DS}$ ) by varying  $V_{DS}$  and  $V_{GS}$  in this structure. Two types of MESFET operations can be defined depending on whether or not the device is conducting at zero gate bias, which in turn depends upon the relative thicknesses of the doped region under the gate and the depletion layer at zero bias. If the depletion layer is thicker than the doped region, the channel will be cut-off with zero gate bias and no drain-source current can flow. The device is normally off and positive gate biases must be applied to reduce the depletion layer and a conduction channel can be formed. This is the enhancement mode MESFET or E-MESFET. On the other hand, if the depletion layer is thinner than the doped region, then the device is normally-on at zero bias and is called depletion mode MESFET or D-MESFET. Fig. 3.6 shows the  $I_{DS}$  vs.  $V_{GS}$  for E-MESFET and D-MESFET. The  $V_T$ , threshold voltage is defined as the gate voltage that makes the depletion layer and the channel equal in thickness. The sign of  $V_T$

determines the mode FET structure. A positive  $V_T$  indicates a E-FET whereas a negative value indicates a D-FET. As  $V_{DS}$  increases, the depletion layer width at the drain end will increase until it is the same width as the channel. In this situation we reached the “saturation” limit. A measure of this phenomenon is the pinch-off voltage,  $V_P$  which is defined as the drain-source voltage which extends the depletion layer across the channel at the drain end of the gate.  $V_P = V_{GS} - V_T$ .

To a good approximation the I-V characteristics of a GaAs MESFET can be described by the following equations:

$$I_{DS} = \beta(2[V_{GS}-V_T]- V_{DS})V_{DS}(1+\lambda V_{DS}) \text{ in the linear region and}$$

$$I_{DS} = \beta(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \text{ in the saturation region, where:}$$

$\beta$  is a constant proportional with  $\mu_n W/L$ ,  $\mu_n$  being electron mobility,  $L$  the gate length and  $W$  is the gate width.  $\lambda$  is a measure of the output conductance  $g_0$  of the MESFET. The I-V characteristic in saturation mode is not flat due to the combined effects of various leakage currents and  $\lambda$  is a measure of the magnitude of these currents. From the variation of  $I_{DS}$  with  $V_{DS}$  and  $V_{GS}$  it is possible to define two conductances given by :

$$g_0 = \delta I_{DS} / \delta V_{DS} \text{ at constant } V_{GS}, \text{ the drain (or output) conductance}$$

and

$$g_m = \delta I_{DS} / \delta V_{GS} \text{ at constant } V_{DS}, \text{ the transconductance}$$

The conductance ratio  $g_m/g_0$  is a common factor in determining the performance of many analog circuits; typically, this ratio is in the range 15-25.

Any current flowing through the device will produce a voltage drop so the values of  $V_{GS}$  and  $V_{DS}$  present in the intrinsic device will be actually less than those applied at the contacts. The value of  $I_{DS}$  produced by an applied  $V_{GS}$  and  $V_{DS}$  will be degraded by the parasitic voltages. Any degradation in  $I_{DS}$  and  $g_m$  will have an effect on the speed of

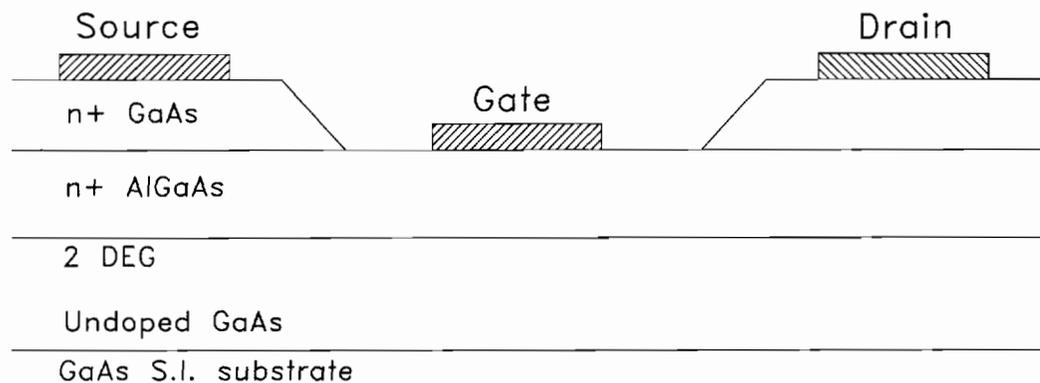
the IC so one of the main goals of the GaAs technology is to minimize the parasitic resistances present in MESFET's. One possibility is reducing the  $r_c$ , contact resistance and another one is reducing the spacing between the ohmic contacts and the gate. Both of these alternatives will rely on the characteristics of the new ohmic contacts to be developed.

The high electron mobility transistor (HEMT) is a relatively new GaAs technology device structure. The advantage of GaAs transistors over silicon devices depends mainly upon the higher electron mobility in GaAs. If maximum speed is required, the fast solution is to use a high doping level as to minimize the resistances in the transistor. This solution, however, has limited use for several reasons:

- 1) the capacitances in the IC will increase, thus decreasing the speed of the circuit.
- 2) the electron mobility decreases due to increase scattering by the dopants.
- 3) there are practical limitations to the maximum doping level which can be used since high doping levels will introduce a large number of dislocations into the crystal lattice.

In the HEMT structure, a highly doped layer of  $\text{Al}_{1-x}\text{Ga}_x\text{As}$  is grown on top of a high purity, undoped layer of GaAs. The ternary compound  $\text{Al}_{1-x}\text{Ga}_x\text{As}$  is formed from a mixture of GaAs and AlAs in the ratio  $x$  to  $(1-x)$ ;  $x$  is typically around 0.3. See Fig. 3.7. Typically, HEMT fabrication techniques involve molecular beam epitaxy (MBE) which allows a good control of the composition and of the thickness layer. The band structure of the interface between these two layers is such that electrons from the doped AlGaAs layer will diffuse into the undoped GaAs to sit in a very thin layer at the interface. In the ideal device this layer actually has no thickness and so is referred to as a "two-dimensional electron gas". (2DEG)

The conductivity of the high mobility electron layer can be modulated in a similar way as a MESFET, by varying the depth of the depletion layer formed by a Schottky contact. The Schottky gate contact to AlGaAs has a higher built-in voltage than the same contact on GaAs, allowing for a better noise margin than in a MESFET.



**Figure 3.7 Illustration of a HEMT device structure**

Ohmic contacts are usually made via a doped layer of GaAs grown on top of the AlGaAs layer. This layer gives a lower parasitic contact resistance than contacts made directly to AlGaAs due to the smaller band gap of GaAs.

The main disadvantage of HEMT technology is the high processing cost associated with the complex processing techniques, MBE and metal-organic chemical vapor deposition (MOCVD).

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## 4. Experimental Procedures and Analysis

### 4.1 Deposition of Thin Films

In this thesis, one ohmic contact system consisting of a three-layer thin film stack on GaAs substrate was examined. 50 nm thick polycrystalline palladium, 150 nm thick amorphous germanium and 20 nm thick polycrystalline palladium were deposited by alternate electron beam evaporation onto <100> oriented GaAs substrates. The evaporation took place at a vacuum pressure of  $2 \times 10^{-6}$  Torr. Prior to evaporation, the wafers were cleaned by dipping in a 10:1 HCl solution for 30 sec. and then rinsed in deionized water. Fig. 4.1 shows a TEM cross-sectional view of the as-deposited Pd(20 nm)/Ge(150 nm)/Pd(50 nm)/GaAs thin film stack that was used throughout this thesis.

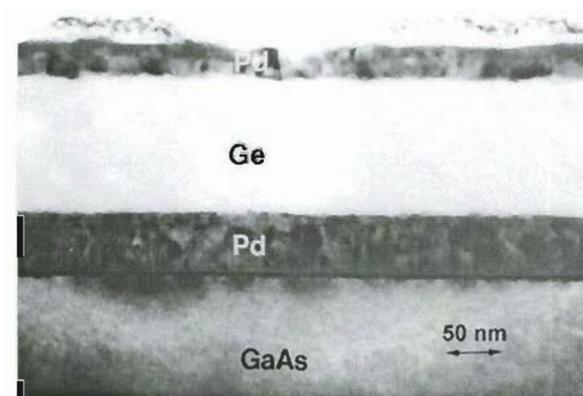


Figure 4.1. Typical as-deposited Pd/Ge/Pd thin film stack used in this thesis.

During cross-sectional Transmission Electron Microscope (TEM) sample preparation, an extra thin film layer consisting of approximate 1  $\mu\text{m}$  of platinum was deposited by Ion Beam Enhanced Chemical Vapor Deposition (CVD) prior to Focused

Ion Beam (FIB) milling. This deposition took place after heat treatments and its only purpose was to protect the final microstructure of the contact during FIB milling.

Free standing palladium/amorphous-germanium/palladium multilayer thin films were prepared by first coating the GaAs substrate with a 1  $\mu\text{m}$  thick photoresist film. Palladium, germanium and again palladium were then alternately evaporated at room temperature with the same thicknesses as described above. After the deposition, the substrates were soaked in high purity methanol for 1 to 3 hours to dissolve away the photoresist and remove the multilayered films. The films were then collected into DSC pans and dried under vacuum with base pressure of  $1 \times 10^{-6}$  Torr for 5-7 hours.

## 4.2 Calorimetry

Heat-flux differential scanning calorimetry (DSC) was used in the present work to measure the heat evolved from the reacting Pd/Ge/Pd multilayers. This technique permitted to identify the phase transformations that unfold during heat treatment, determine their sequence, the temperature range within which they occur and measure their activation energies. In heat-flux DSC, a single furnace is used to heat both sample and reference materials, and the temperature difference is measured. This method differs from differential thermal analysis (DTA) in two significant aspects. Firstly, the heat flow path from the furnace to the sample and reference is of low resistance so large heat flow differences give rise only to small temperature differences and the accuracy and similarity of the sample and reference temperature programmes is maintained. Secondly, the heat flow paths from the furnace to the sample and reference thermocouples are made identical and independent of the sample and reference materials; thus the temperature difference is directly proportional to the difference in heat flow to the sample and reference. The principles described above are used by the Du Pont 9900 DSC instrument<sup>1</sup>, which was employed in this work. The reference, which does not go through any transitions, and a sample are heated at a constant heating rate and the difference in power flow is recorded as function of temperature.

The starting temperature was 30 °C, heating rates were varied from 10 °C/min. to 100 °C/min. and the final temperature was 450 °C. After the initial run, the samples were quickly cooled, and a second run was made without disturbing the sample at the same heating rate as the first one. The second DSC trace was used as a baseline and subtracted from the first trace. This entire task was accomplished in a spreadsheet software with data imported from the DSC analysis system.

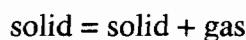
Freestanding multilayer films were collected in the pans as described in the previous section. Their weight was measured using a Mettler AE 240 balance with a +/- 0.1 mg sensitivity. The sample weight ranged from 1.5 to 2.5 mg., which rendered a sufficiently large signal-to-noise ratio in the Du Pont 9900 DSC instrument.

Heating the samples both for annealing and DSC was performed under forming gas atmosphere that consisted of 4% $H_2$ -96% $N_2$ . For the samples used in TEM phase identification studies, at the end of the heating cycle, the ambient gas atmosphere was switched to He in order to maximize the heat transfer during quenching.

### **4.3 Analysis of Calorimetric Data. Determining Activation Energies**

Although DSC is commonly used to determine enthalpies and temperatures of reactions and specific heats, its use for obtaining kinetic data on solid state transformations was limited. It was shown that reaction kinetics could be evaluated by analyzing the shape of the transformation peaks as well as the shift in the transformation temperatures with scanning rate <sup>2,3</sup>. Clevenger et al. <sup>4</sup> has demonstrated the use of this method in studying kinetics of reactions for metal-silicon thin films, which were similar with the metal-germanium system presented in this study.

The method we employed in determining the activation energies associated with the solid state reactions that take place during ohmic contact formation was first demonstrated by Kissinger <sup>2</sup>. He initially restricted its use to reactions of the type:



Later, Henderson <sup>3</sup> and Boswell <sup>5</sup> demonstrated the method could be extended for calculating activation energies for other solid state reactions (e.g. nucleation and growth) as long as the following separation of variable could be assumed:

$$\frac{dX}{dt} = f(X) \cdot g(T) \quad (1)$$

where  $dX/dt$  is the reaction rate and  $T$  is the temperature. If the temperature function follows the Arrhenius dependence, then:

$$g(T) = C_0 \cdot e^{-\left(\frac{Q}{kT}\right)} \quad (2)$$

and by combining (1) and (2) we obtain:

$$\frac{dX}{f(X)} = \frac{C_0}{R} \cdot e^{-\left(\frac{Q}{kT}\right)} \cdot dT \quad (3)$$

where  $R$  is the constant scan rate and is equal to  $dT/dt$ ,  $T$  is temperature and  $t$  is time. Integrating the left side of equation (3) from  $X = 0$  to  $X = X_p$ , and the right side of the equation from  $T = T_0$  to  $T = T_p$  where:

$X_p$  is the fraction transformed at the peak temperature

$T_0$  is the temperature at which the reaction starts

$T_p$  is the peak temperature,

we obtain:

$$\int_0^{X_p} \frac{dX}{f(X)} = \int_{T_0}^{T_p} \frac{C_0}{R} \cdot e^{-\left(\frac{Q}{kT}\right)} \cdot dT \quad (4)$$

According to Boswell <sup>5</sup>, the integral from the left side of (4) is a constant whose value does not depend on the heating rate but depends only on  $X_p$  and the form of  $f(X)$ .

Assuming that the fraction transformed at the peak temperature  $X_p$  does not depend on the scan rate, then:

$$\mathbf{R} \cdot \mathbf{C}_1 = \int_{T_0}^{T_p} e^{-\left(\frac{Q}{kT}\right)} dT \quad (5)$$

where:

$$\mathbf{C}_1 = \frac{\int_0^{X_p} \frac{dX}{f(X)}}{\mathbf{C}_0}$$

By integrating the right side of equation (5) and assuming  $T_p \gg T_0$  and  $Q/kT \gg 1$ , we get:

$$\int_{T_0}^{T_p} \frac{C_0}{R} \cdot e^{-\left(\frac{Q}{kT}\right)} \cdot dT = \frac{kT_p^2}{Q} \cdot e^{-\left(\frac{Q}{kT}\right)}$$

then,

$$\ln \frac{R}{T_p^2} = C_2 - \frac{Q}{kT_p} \quad (6)$$

where:

$$C_2 = \frac{K}{Q \cdot C_1} \text{ is a constant.}$$

Equation (6) can then be used to calculate the activation energy for a reaction which DSC peak was identified by plotting  $\ln ( R/T_p^2)$  versus  $1/kT_p$  at different heating rates and taking the slope of the straight line to be  $Q$ .

## **4.4 Transmission Electron Microscopy**

In transmission electron microscope (TEM), a thin solid specimen (<200 nm) is bombarded in vacuum with a parallel beam of electrons and the beam is of sufficient energy to pass through the specimen. A series of electromagnetic lenses then magnifies this transmitted electron beam and diffracted electrons are observed in the form of a diffraction pattern beneath the specimen. This information is used to determine the crystal structure of the material examined. Transmitted electrons form images from small regions of the specimen and produce contrast due to various scattering mechanisms given by the interactions between the electrons and the atomic constituents of the sample.

### **4.4.1 Analytical Electron Microscopy (AEM)**

The AEM system used throughout this work consisted of a JEOL 2000FX TEM/STEM unit operating at 200 KeV accelerating voltage which was equipped with a KeVex Quantum EDS X-ray detector capable of detecting nitrogen and elements higher in atomic number than nitrogen. This unit permitted to investigate microstructural changes that occur during Pd-Ge ohmic contact annealing process by combining its various capabilities. Bright field and dark field imaging, selected area diffraction (SAD), micro-diffraction and energy dispersive X-ray spectrometry were the techniques employed to characterize the ohmic contact microstructure.

EDS X-ray chemical identification was performed in the STEM imaging mode where a 10 nm electron beam probe produced a sufficiently large X-ray signal-to-noise ratio in the detector. Semi-quantitative analysis of the EDS X-ray spectra was carried out

using the Standardless Metal Thin Film (SMTF) program that is part of the Tracor Northern analysis software system.

Microdiffraction patterns were taken from various grains and at different zone axes, typically 1-3 zones per grain. The limit was imposed by the grain size and the geometry of the samples, in the case of FIB prepared specimens, where the maximum tilt angle was given by the width and depth of the canyon. EDS X-ray analysis was also performed on each grain from which microdiffraction patterns were recorded.

Bright field, dark field analysis indicated which grains were generating a specific diffracted electron beam.

The various compounds present in the microstructure of the Pd-Ge ohmic contacts studied in this thesis were identified on the basis of the best match found in the published literature for d-spacings measured from microdiffraction patterns. A list of potential phases which best fitted the experimentally calculated d-spacings was assembled by searching the database for the crystals, using the computer program Desktop Microscopist. The chemical analysis data obtained from the EDS X-ray studies was used to narrow down the list of possible compounds. The lattice parameters and the Wyckoff positions of the atoms in the crystal whose d-spacings best fitted the experimental data, were entered into the Desktop Microscopist software and the electron diffraction patterns were simulated for various zone axes<sup>6</sup>. Additional evidence was gathered by comparing the experimentally determined interplanar angles with the computer simulated ones.

The camera constant for the diffraction patterns was calibrated by measuring the patterns produced by the adjacent GaAs substrate.

#### **4.4.2 High Resolution Electron Microscopy**

High-resolution electron microscopy was employed to study the epitaxial nature of the Ge/GaAs interface, which is the key element in forming ohmic contacts with low specific resistivity. This work was completed at Lawrence Berkeley National Laboratory, National Center for Electron Microscopy (NCEM).

The basic instrument was a Philips CM300FEG/UT, a TEM with a field-emission electron source, and an ultra-twin objective lens with low spherical aberration ( $C_s = 0.65\text{mm}$ ) and a native resolution of  $1.7\text{\AA}$ . High-resolution images were produced at 300 KeV accelerating voltage and were recorded digitally with a Gatan CCD (charge-coupled device) camera.

#### **4.4.3 In-Situ Transmission Electron Microscopy**

In-Situ TEM experiments were carried out at Lawrence Berkeley National Laboratory, NCEM and they allowed to visualize the dynamics of the solid state phase transformations that take place during ohmic contact annealing. The instrument used was a JEOL 200CX TEM equipped with a Gatan double tilt-heating holder. Its spacial resolution ( $2.8\text{\AA}$ ) was higher than the other TEM instruments described above. In addition to a standard film camera, a Gatan 622 intensified TV camera and VCR were employed in recording the heating experiments at video rates. The temperature was recorded live on the videotape by using an Amiga computer specialized software.

#### **4.5 TEM Sample Preparation**

In order to be able to perform TEM on a specimen, the area of interest has to be electron transparent. The TEM also requires that the completed sample fit within a 3-mm disc, with the thinned area close to the center. This means a certain amount of sample preparation is necessary to go from the wafer as-deposited films to a TEM-ready sample.

The ohmic contact microstructure was studied using cross-sectional and planar specimens. Each type of specimen required different preparation techniques, which will be described in the following sections.

#### **4.5.1 Cross-Sectional Specimen Preparation by Focused Ion Beam (FIB)**

TEM specimen preparation using FIB is a relatively new method, being first demonstrated only a decade ago. Since then, there have been dramatic improvements in the ultimate resolution and milling characteristics of the commercially available ion columns which has led to an overall reduction in the FIB preparation time as larger current densities have allowed the same volume of material to be removed faster without loss of precision <sup>7</sup>.

In this approach, the site to be analyzed is identified and then a combination of sawing, cleaving, and grinding is used to extract a sample that is small enough (1x2x.5 mm) to fit into the TEM. This sample also has to be thin enough in the region of interest to allow the subsequent FIB thinning to be achieved in a reasonable time.

First, a 1x2-mm piece of the GaAs substrate that contained the ohmic contact thin film system was cut from the wafer with an IsoMet low speed diamond saw. The cut sample was attached with low melting temperature Crystalbond wax on a metal stub and manually ground on lapping discs. Thinner samples take less preparation time in the FIB, however due to the GaAs brittleness, their thickness ranged from 60 to 120  $\mu\text{m}$ . This remaining piece was glued on half molybdenum washer as shown in Fig. 4.2.

The metallized surface of the sample was positioned perpendicular to the  $\text{Ga}^+$  beam direction, which milled 20-30  $\mu\text{m}$  wide and 3-4  $\mu\text{m}$  deep canyons, leaving an electron transparent foil in the middle (see Fig.4.3) . Prior to FIB thinning, a platinum protective layer was deposited in-situ by Ion Beam Enhanced Chemical Vapor Deposition (CVD) at the location of the final electron transparent region. This platinum deposition capability was available in the FEI 610 FIB workstation, which was used during this

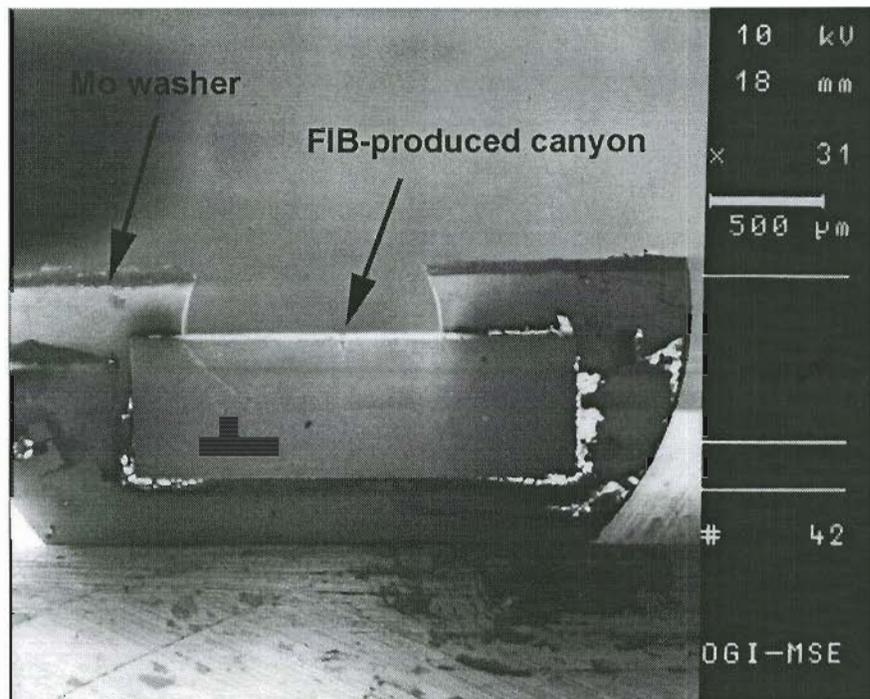
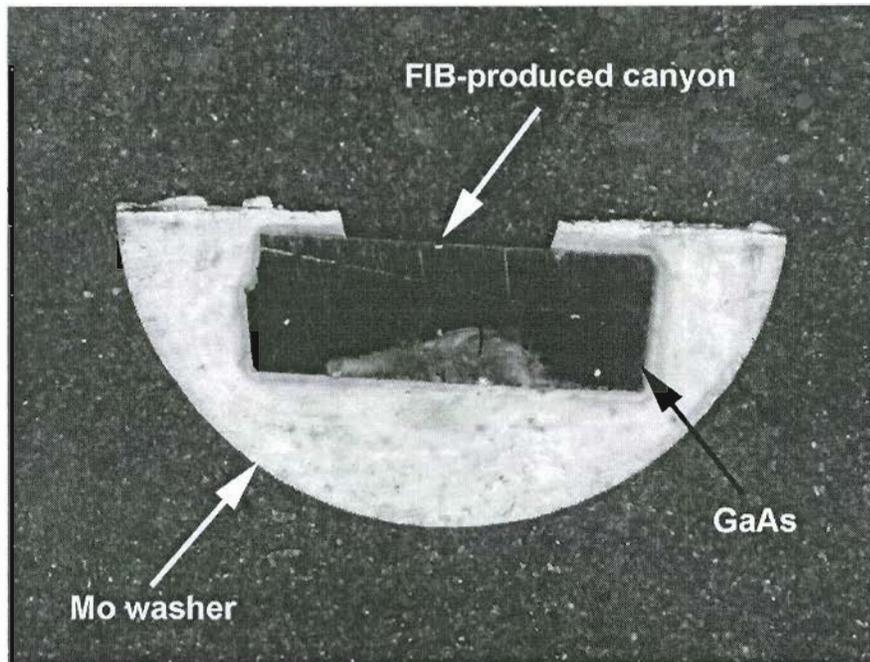


Figure 4.2. GaAs piece of wafer attached to half Mo washer

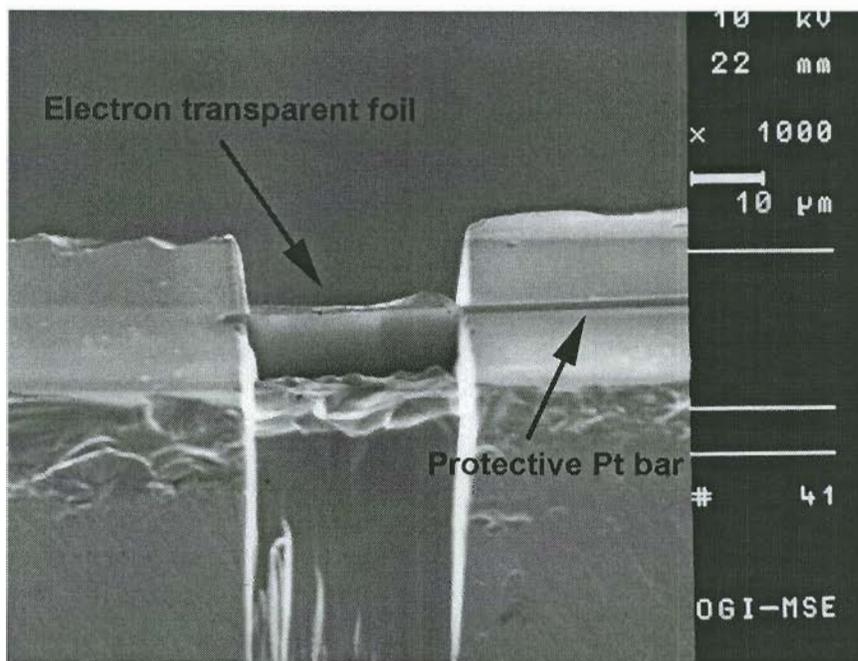
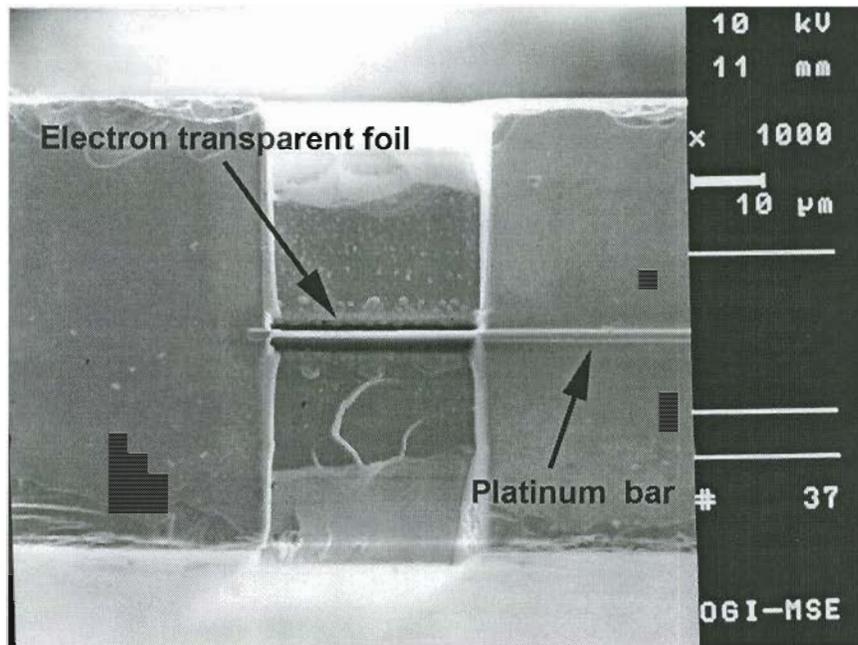


Figure 4.3. SEM images of typical TEM cross sections as prepared by FIB milling.

study. Once the FIB milling is complete, the sample attached to the washer can be transferred directly to the TEM for analysis.

#### **4.5.2 Planar Section TEM Specimen Preparation**

Planar sections were used to provide information about the Pd/Ge/Pd thin film system and the microstructural changes that take place during heating. Freestanding Pd/Ge/Pd films were studied before and after DSC analysis. After depositing the ohmic contact thin film system on top of the photoresist layer, the substrates were soaked in high purity methanol for 1 to 3 hours. This step dissolved away the photoresist and removed the multilayer films which were, then, collected into DSC pans and dried under vacuum with base pressure of  $1 \times 10^{-6}$  Torr for 5-7 hours. The films were carefully removed from the DSC pans after they were annealed in the DSC cell, and placed on a copper/carbon grid holder for TEM analysis.

#### **4.6 Contact Resistivity Measurements by the Transmission Line Model (TLM)**

In order to correlate the effects of the microstructure with the most important electrical property of the ohmic contacts, throughout this research work, the Transmission Line Model (TLM) method was employed for measuring the contact resistivity. The motivation of this choice was the need for consistency and the fact that most of the ohmic contact on GaAs resistivity data reported in the literature so far was gathered by using the TLM method. Other reasons for its use will become more evident from the brief description below.

The specific resistivity,  $\rho_c$ , of a metal/semiconductor contact is defined as <sup>8</sup> :

$$\rho_c = (\delta V / \delta J)_{V=0}$$

where  $V$  is the voltage and  $J$  is the current density that passes through the contact. The total contact resistance,  $R_c$ , of an ohmic contact is:

$$R_c = \rho_c / A \quad (7)$$

where  $A$  is the contact area and assuming that the current flow is vertical across the interface and uniform over the entire area. Therefore, the measured total resistance,  $R_T$  of two identical ohmic contacts on opposite sides of a homogeneous semiconductor bar can be express as:

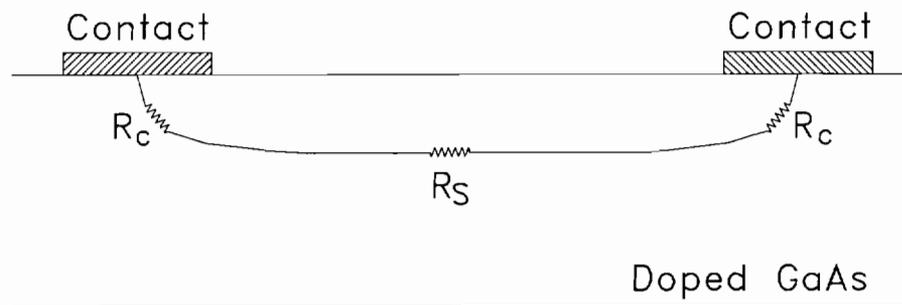
$$R_{tot} = 2R_c + \rho_b L/A = 2 \rho_c / A + \rho_b L/A \quad (8)$$

where  $A$  is the area of the contact,  $\rho_b$  the bulk resistivity of the semiconductor,  $L$  the length of the semiconductor bar. In principle, the contact resistance  $R_c$  and specific contact resistivity  $\rho_c$  could be calculated from the above equation, but this method would produce large errors because  $\rho_b$  is much higher than  $\rho_c$ . Another problem is the exact alignment of the contact areas on the opposite sides of the wafer which, if not accurate, could induce anomalous current flow and generate additional resistance. Moreover, this structure is not compatible with the integrated circuit technology.

Ohmic contacts are commonly applied to devices on thin active layers such as MESFETs and HEMTs. For contacts on this type of lateral structures, the current distribution across the contact is not uniform, making equation (7) unusable for determining the specific contact resistivity. The analysis is more complex due to lateral current flow, current crowding and the sample geometry. One theoretical method that takes into account the current crowding and makes it possible to extract the specific contact resistivity, is based on the Transmission Line Model (TLM)<sup>8,9</sup>. For the contact configuration shown in Fig. 4.4, it was demonstrated that  $R_c$  contact resistance is given by:

$$R_c = [\rho_c / (L_T Z)] \coth(L/L_T)$$

where  $L$  is the length of the contact,  $Z$  is the width of the conductive channel region, and  $L_T$  is defined as the transfer length where the voltage due to the current from the semiconductor to the metal or from the metal to the semiconductor has dropped to  $1/e$  of its maximum value.



**Figure 4.4. Ohmic contacts on a GaAs conductive channel where the current flow is parallel with the surface.**

It was also shown that:

$$L_T = \sqrt{\frac{\rho_c}{\rho_s}}$$

where  $\rho_s$  is the sheet resistance of the conductive channel. Fig. 4.5 illustrates a sketch and an actual optical image of the TLM structures used throughout this thesis. For contacts with  $L > 1.5L_T$  we can approximate  $\coth(L/L_T) \approx 1$  and contact resistance become:

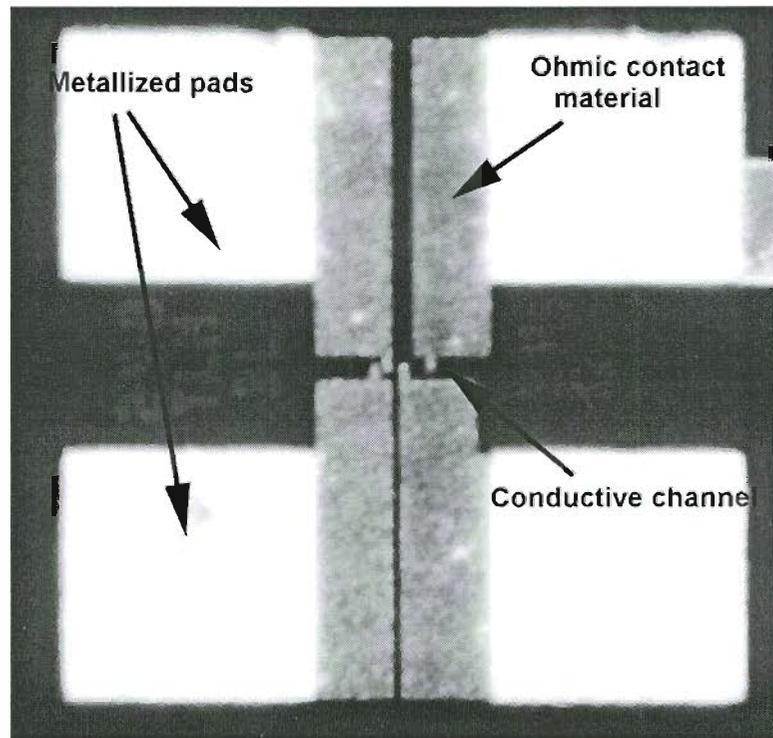
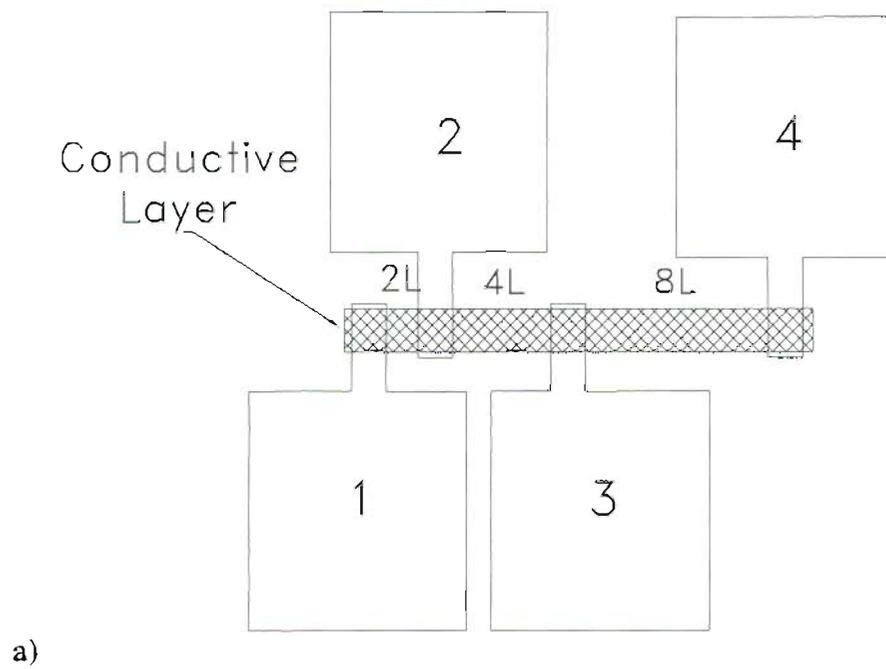


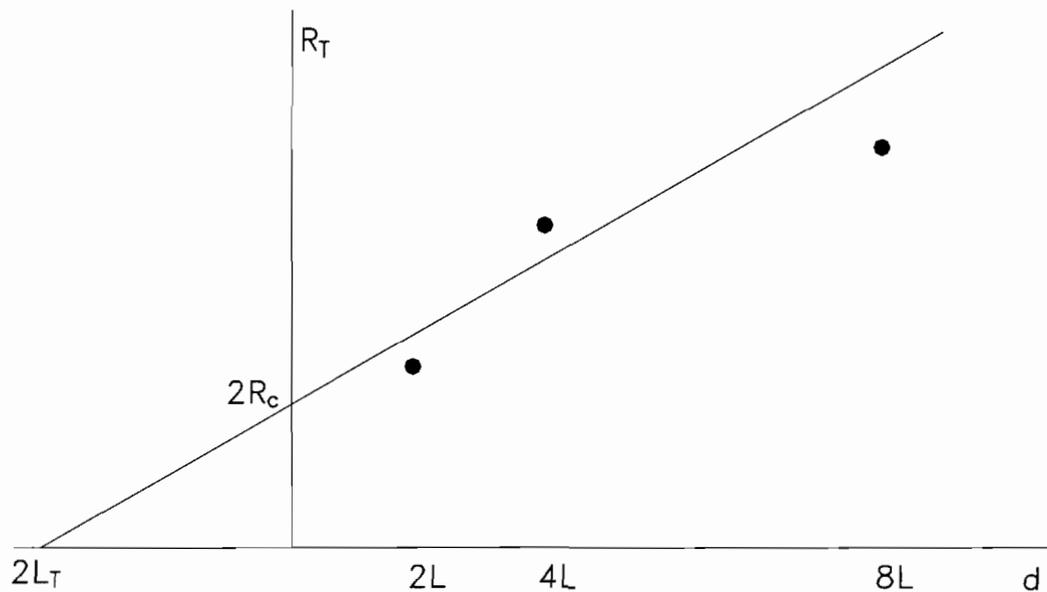
Figure 4.5. a) Schematic picture of a typical TLM structure used in measuring the specific ohmic contact resistivity b) Actual image of a TLM structure.

$$R_c = \rho_c / (L_T Z)$$

The total resistance between any two contacts is given by:

$$R_T = \rho_s d / Z + 2R_c = \rho_s d / Z + 2\rho_c / (L_T Z)$$

Typical TLM test structures consist of a series of ohmic contact pads separated by different  $d$  gap spacings along a conductive channel, as shown in Fig. 4.5(b). By plotting the total resistance as a function of  $d$ , three parameters can be extracted. The measured slope is  $\rho_s / Z$  which gives sheet resistance  $\rho_s$ , the intercept at  $d = 0$  is  $R_T = 2R_c$  and the intercept at  $R_c = 0$  is  $d = 2L_T$  which can be used to calculate the specific contact resistance,  $\rho_c$ . A generic TLM plot is represented in Fig. 4.6.



**Figure 4.6. Obtaining various ohmic contact parameters by TLM plots.**

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## **5. Phase Formation Sequence in the Ge/Pd/GaAs System**

The compound semiconductor contact metallization schemes are usually comprised of multiple elements thin film systems that, when annealed, undergo a series of phase transformations. As opposed to elemental semiconductor contacts, this added complexity requires a better and more accurate understanding of the microstructure evolution sequence, which determines the final phase configuration and interface morphology. It is generally believed that the electrical parameters of these contacts are influenced by the microstructure characteristics, and being able to control its final configuration is a key element for better devices. Studying the contact phase formation sequence provides us with the necessary knowledge to control the annealing process of the system and to understand the charge transport mechanisms across the metal/compound semiconductor interface.

### **5.1 Introduction**

As the demand for more complex GaAs integrated circuits is growing, major efforts are made in the direction of scaling down the device dimensions. One of the limiting factors is the size of the metal-semiconductor field effect transistor (MESFET) which depends on the ohmic contact characteristics. In the last decade, the Pd-Ge contact system emerged as the most promising replacement of the Au-Ni-Ge alloy, still used by most of today's GaAs technology. Its better electrical properties stem from the fact that contact formation is based on a series of solid state reactions and no melting of the metal thin films and GaAs substrate take place during annealing. Research studies by Marshall et al.<sup>1</sup> demonstrated that thermally stable contacts with low resistivities could be achieved

by low temperature annealing of Pd and Ge thin films. Their studies also revealed that the excess Ge is regrown on top of the GaAs substrate by a solid state epitaxy mechanism.

However, implementing this type of contact into a device fabrication line proved to be difficult due to our incomplete understanding of the solid state reactions that take place during contact formation. Furthermore, similar Pd/Ge based contact systems were reported to lack a good adhesion to the substrate and it was found that their resistance increases rapidly with temperature<sup>2</sup>. So far, good ohmic contacts were obtained by using "recipes" derived from trial and error experiments, and it has been recognized that there is a need for a better understanding and well derived models if control over microstructure and ohmic contact performance is to be accomplished.

The behavior of the Pd-GaAs interface, when subjected to annealing temperatures lower than 400 °C, was studied in great detail by Sands et al.<sup>3</sup>. They showed that two Pd<sub>x</sub>GaAs ternary phases, labeled as "phase I and phase II" form successively at the interface and the transition temperature is around 250 °C. Ottaviani's et al.<sup>4</sup> study on the Pd-Ge thin film system demonstrated that, at low temperatures, Pd<sub>2</sub>Ge forms first, followed by PdGe transformation at higher annealing temperatures. The microstructure of the entire contact system, Ge/Pd/GaAs, was investigated by Marshall et al.<sup>5</sup>, which showed the predominant reaction takes place between Pd and Ge to first form Pd<sub>2</sub>Ge and then PdGe.

The purpose of this work is to characterize the kinetics of the solid state reactions as they evolve during the annealing process and to identify the mechanisms that contribute to (or hinder) the formation of good ohmic contacts.

The interactions that take place between Pd/Ge thin films evaporated on to a GaAs substrate were examined by transmission electron microscopy (TEM) and constant-heating-rate differential scanning calorimetry (DSC). Metal silicide formation studies by Clevenger et al.<sup>6</sup> have demonstrated that combining DSC for thermal analysis with TEM for phase identification and microstructural information is an effective way to study the kinetics of thin film reactions. Results of this examination as they are applied to Pd-Ge on GaAs ohmic contact formation, are reported in this chapter.

The microstructure evolution and the corresponding solid state reactions that take place during the formation of the Pd-Ge ohmic contacts on GaAs were studied using constant-heating-rate differential calorimetry (DSC) and cross-sectional transmission electron microscopy (XTEM). DSC analysis at different heating rates was performed on Pd(20 nm)/ Ge(150 nm)/Pd(50 nm) thin film stacks that were lifted from the substrate. Specimens heated at temperatures that coincide with the DSC peaks were quenched in a He atmosphere and the resulting microstructure was characterized by XTEM. Variable constant-heating-rate DSC experiments allowed to determine the activation energy associated with each solid state reaction by the Kissinger plot method.

As an extension of the method described earlier, the phase formation sequence and the evolution of microstructure during ohmic contact alloying were investigated by *in-situ* annealing TEM. By using this technique, it is possible to directly observe both palladium germanide phase formation and Ge SPE growth on GaAs. This method also allows kinetic and microstructural information to be observed during annealing and provides a continuous and complete record of phase and microstructure evolution.

## **5.2 Microstructure Evolution of the Pd/Ge/Pd/GaAs Ohmic Contact on GaAs.**

In this study, Pd(20 nm)/Ge(150 nm)/Pd(50 nm) layers were used as free standing films for DSC experiments and on <100> oriented n-type GaAs substrates for TEM microscopy. The free standing films were prepared by alternate electron beam evaporation of Pd and Ge onto GaAs substrates coated with about 1  $\mu\text{m}$  of photoresist. More details regarding this procedures were provided in section 4.1. The DSC samples were prepared by soaking the wafers in methanol to dissolve the photoresist and the remaining Pd/Ge/Pd thin films were collected and dried under vacuum.

Heating the samples both for annealing and DSC was performed under a forming gas atmosphere that consisted of 4% $\text{H}_2$ -96% $\text{N}_2$ . At the end of the heating cycle, the

ambient gas atmosphere was switched to He to maximize the heat transfer during quenching of the TEM samples.

Electron transparent TEM cross-sections were produced by the FIB method as described in section 4.5.1. The specimens were then examined with a JEOL 2000FX analytical TEM/STEM equipped with a KeVex Quantum window EDS X-ray detector (O and N sensitive). The phases were identified by measuring d-spacings from TEM microdiffraction patterns recorded from several grains of each of the existing layers and searching a diffraction data base. The results were confirmed by simulating the zone axis patterns with Desktop Microscopist electron diffraction software. The camera constant for the diffraction patterns was measured from patterns produced by the adjacent GaAs substrate.

Fig. 5.1 shows the DSC trace for Pd/Ge/Pd thin film multilayers heated at a constant rate of 10 °C/min. XTEM was performed to correlate the thermal changes with microstructural transitions, this time using specimens which included the GaAs substrate. The samples were heated in the forming gas ambient at the same constant rate of 10 °C/min to the peak temperatures and quenched in a He atmosphere to room temperature with a rate of cooling of about 400 °C/min in the DSC cell. The purpose of this high rate of cooling step was to preserve the microstructure present at the peak of reaction. Fig. 5.2 shows the as-deposited thin film stack prior to any heat treatment. The 3 nm thick Pd/GaAs reaction layer was identified by Sands et al.<sup>3,7</sup> as being Pd<sub>x</sub>GaAs which forms at room temperature.

Fig. 5.3 is a cross-sectional image of the sample heated at 161 °C and represents the first stage of Pd:Ge thin film alloying. An amorphous 18 nm thick Ge depleted layer is noted at the lower Pd-Ge interface which is formed due to fast Ge diffusion into the Pd layer. The microdiffraction patterns recorded suggest that no new phases are formed at this point.

The micrograph presented in Fig. 5.4 represents the structure resulting from an anneal at 214 °C, which corresponds to the second DSC peak. Both Pd layers are reacted and the newly formed phase identified by TEM microdiffraction is hexagonal Pd<sub>2</sub>Ge.

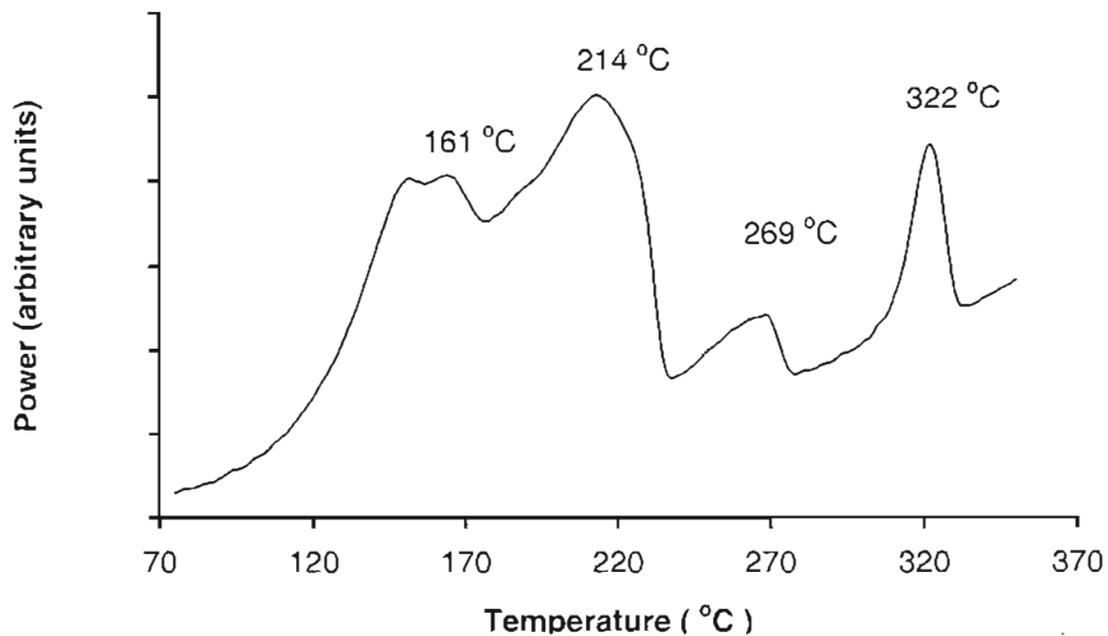


Figure 5.1. DSC trace of Pd/Ge/Pd multilayer film heated at 10 °C/min. and the peak temperature associated with each solid state reaction.

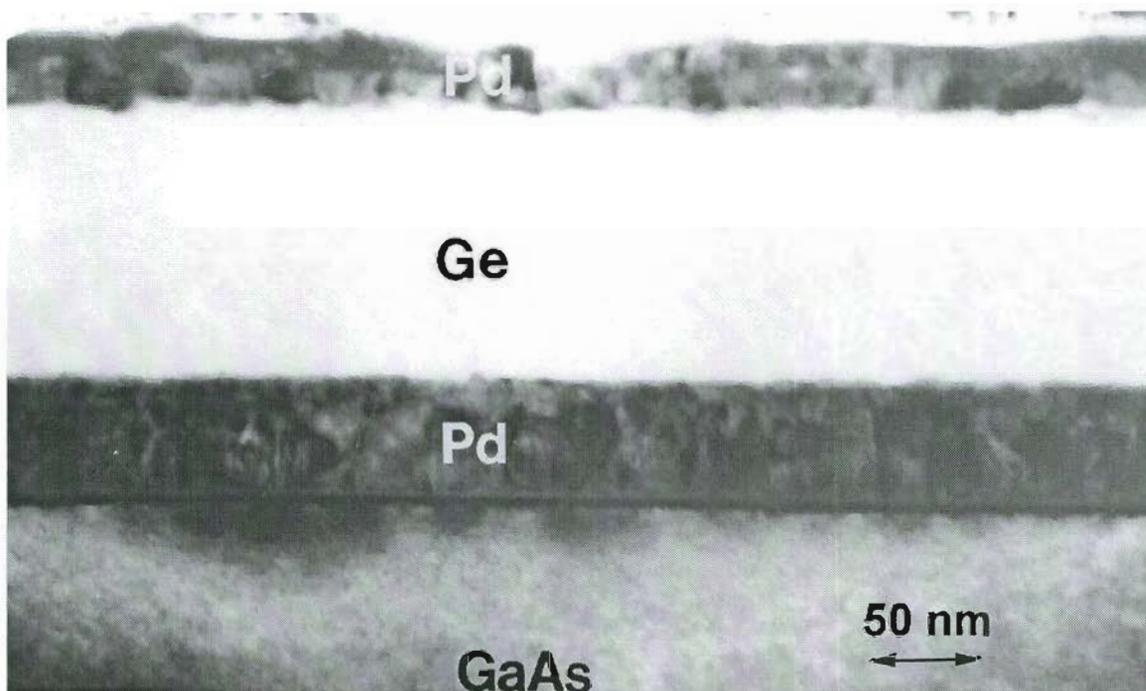


Figure 5.2. Cross sectional view of an as-deposited specimen.

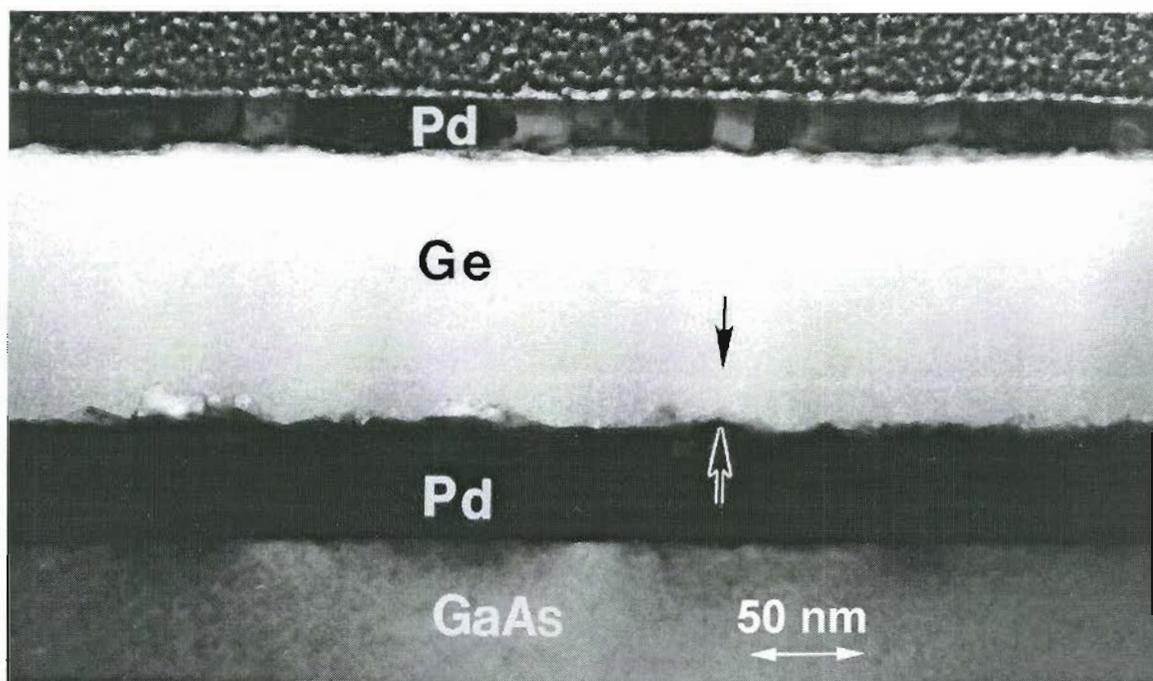


Figure 5.3. Cross-sectional micrograph of a sample annealed at 161 °C and quenched in He atmosphere. The arrows indicate the Ge depleted layer.

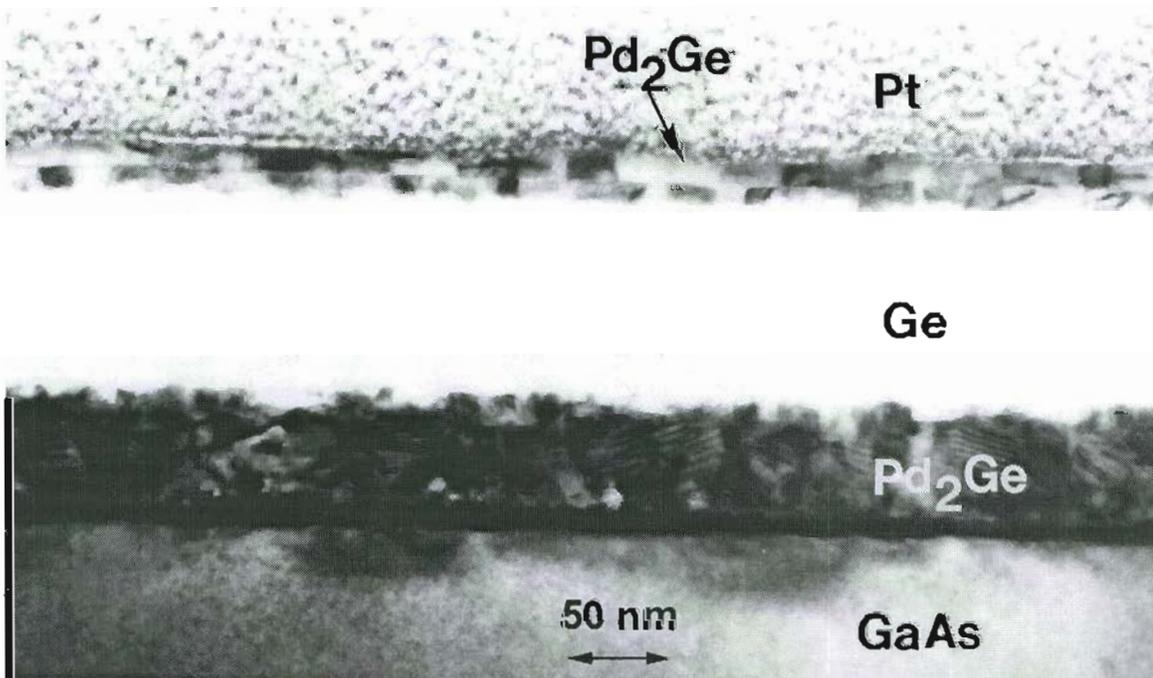


Figure 5.4. Cross-sectional micrograph of a sample annealed at 214 °C and quenched in He atmosphere.

The thickness of the lower Pd<sub>2</sub>Ge layer is 65 nm, about the thickness of the initial Pd layer plus the thickness of the Ge depleted area. At the Pd:GaAs interface, the reaction layer grows to 8 nm.

As shown in Fig. 5.5, the Pd:Ge reaction has continued though the amorphous Ge (a-Ge) layer remained unreacted after annealing at 269 °C. TEM microdiffraction results suggest that a new phase, an orthorhombic PdGe compound, nucleates and grows at the Ge-Pd<sub>2</sub>Ge interface consuming a-Ge and Pd<sub>2</sub>Ge according to:



This reaction requires that Ge diffuses through the PdGe layer and reacts with Pd<sub>2</sub>Ge. The image shows some Ge that gets trapped at the PdGe-Pd<sub>2</sub>Ge interface without being consumed by the reaction, which may suggest that PdGe formation is both diffusion and reaction controlled. At the interface with GaAs, the ternary compound can still be noticed at this temperature although its thickness decreases, probably due to the consumption of Pd.

After annealing at 322 °C, some residual Pd<sub>2</sub>Ge is still present although the predominant phase is PdGe. Part of the unreacted a-Ge crystallized between the compound layers although a-Ge is still present. The ternary compound is not present at the interface with GaAs as the PdGe compound is in direct contact with the substrate. Fig. 5.6 provides a cross-sectional view of a sample annealed at this temperature.

The final microstructure resulted from annealing at 380 °C, as shown in Fig. 5.7, reveals that the excess Ge was transported through the PdGe layer and then grew epitaxially on top of the substrate. In comparison with the sample annealed at 322 °C, it can be noticed that a certain degree of PdGe grain growth took place. Also, at this temperature, no Pd<sub>2</sub>Ge was detected. Fig. 5.8 shows, in greater detail, the epitaxial nature of the Ge layer.

It is concluded the first DSC peak represents Pd-Ge interdiffusion and the subsequent formation of an amorphous Pd<sub>2</sub>Ge layer, the second DSC peak is associated

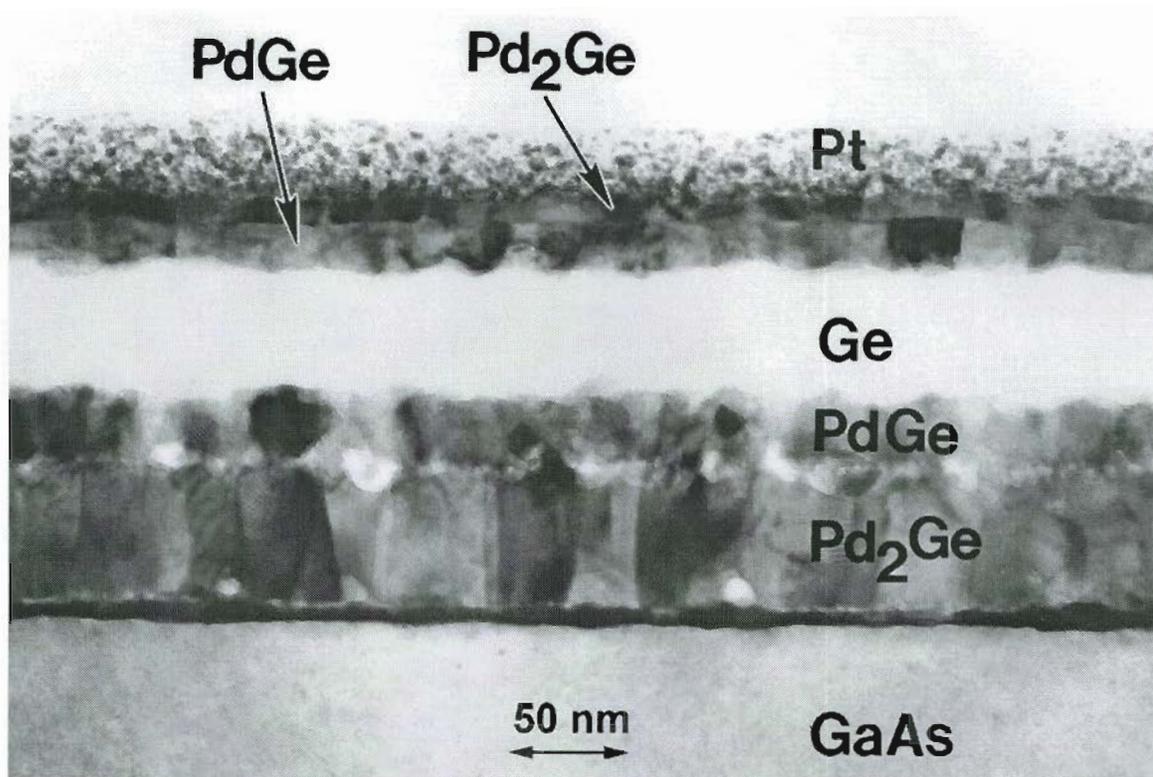


Figure 5.5. Cross-sectional TEM image of a sample annealed at 269 °C and quenched in He atmosphere

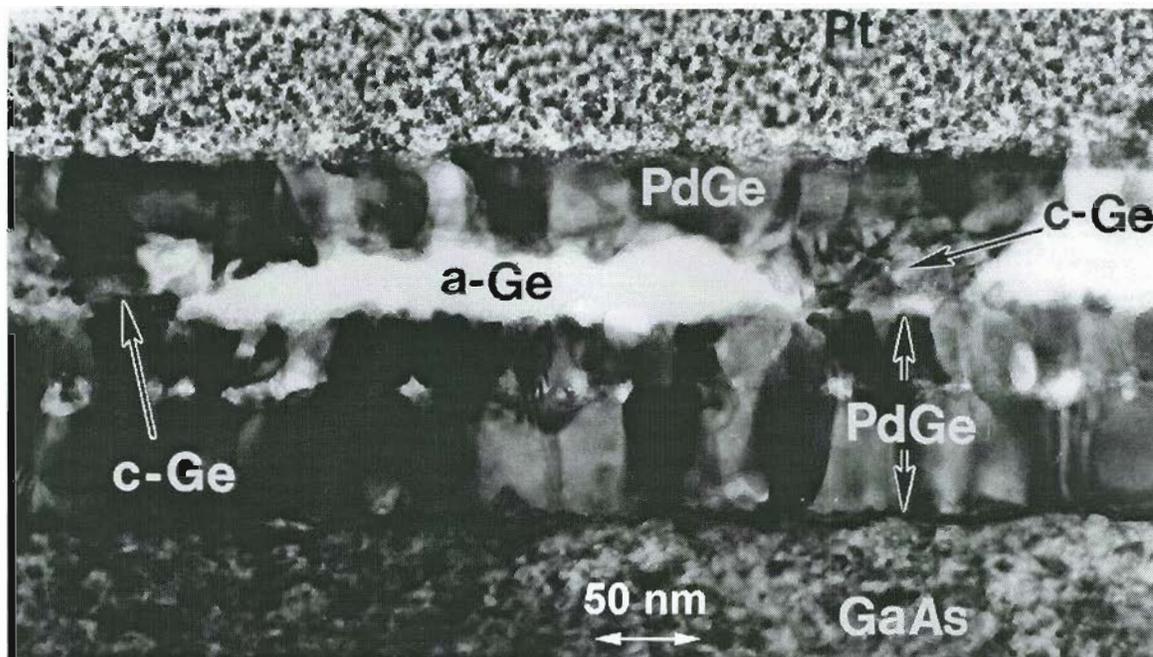


Figure 5.6. Cross-sectional image of a sample annealed at 322 °C and quenched in He atmosphere

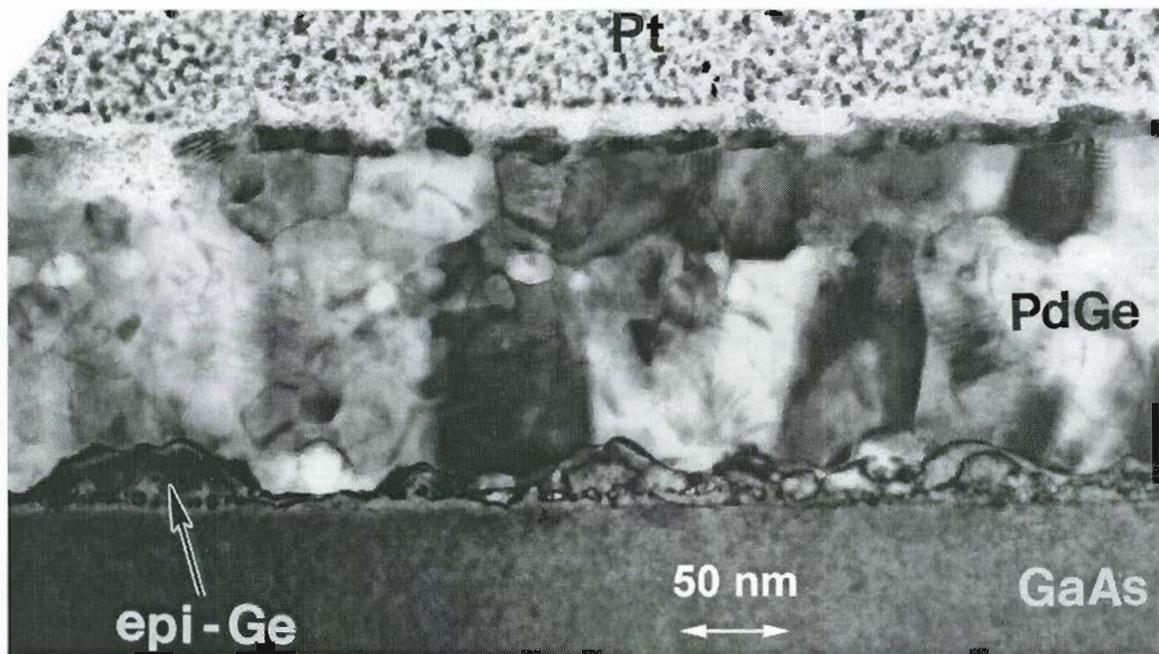


Figure 5.7. Cross sectional micrograph of the final microstructure resulted from annealing at 380 °C followed by slow cooling in a forming gas atmosphere.

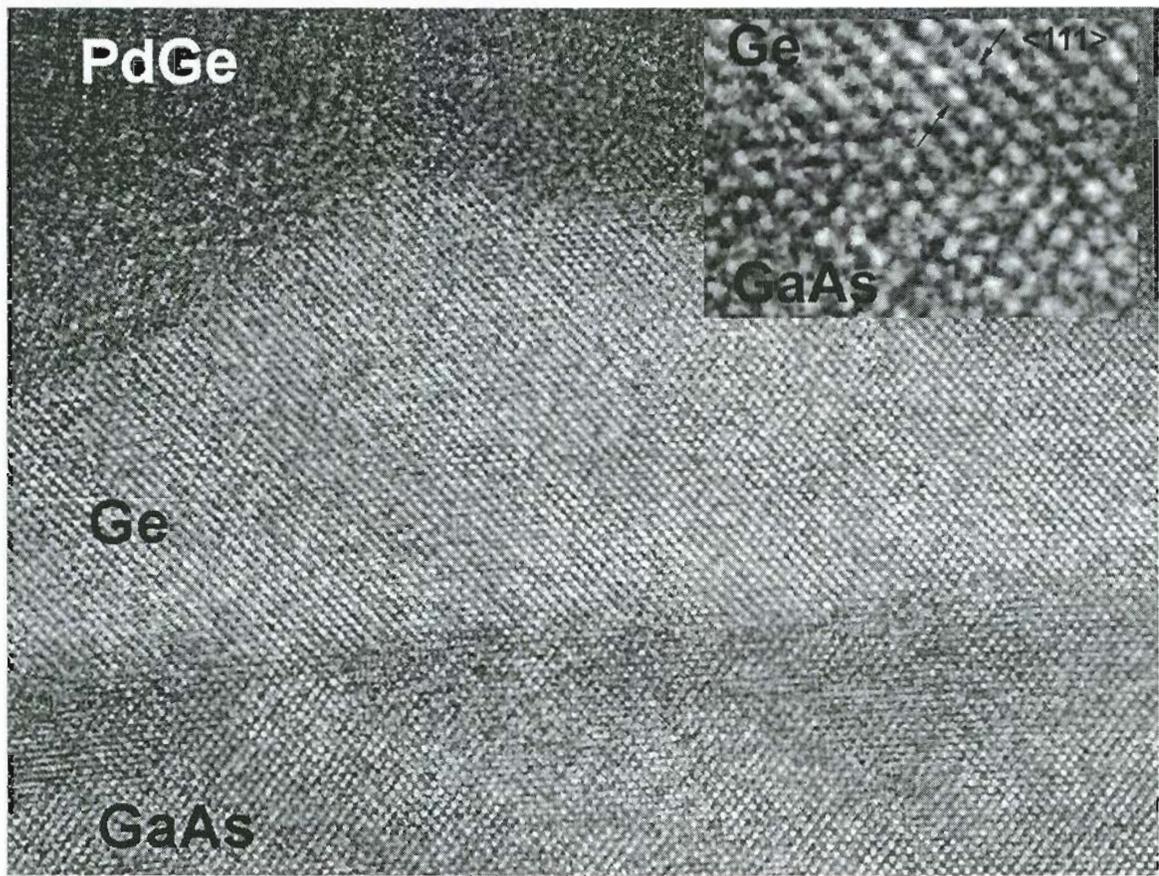


Figure 5.8. High resolution TEM image of the PdGe/epi-Ge/GaAs interface

with Pd<sub>2</sub>Ge formation, the third peak is related to PdGe phase transformation and the fourth DSC peak describes the excess Ge crystallization. Since the thin film stack subjected to DSC did not contain any substrate, the significance of the fourth peak is not entirely relevant for the Ge solid state epitaxy on GaAs. However, as it can be recognized from the correlated DSC data with TEM studies, the rest of the Pd:Ge reaction is identical in both situations, with or without the GaAs substrate. In the final stages of ohmic contact formation there are two competing reactions that determine the extent of Ge transport to the GaAs surface - PdGe formation and Ge crystallization. They both consume a-Ge and, as shown by previous studies <sup>1,8</sup>, the presence of Ge at the GaAs interface is essential for a good ohmic contact formation. This behavior is consistent with earlier research on similar Pd:Ge thin film systems <sup>9,10</sup> which showed that c-Ge and both germanide phases can coexist. Nevertheless, the role of the Ge epitaxial layer in forming a low resistance ohmic contact is surrounded by controversy. Marshall et al. <sup>1</sup> proposed a model based on the Ge/GaAs low barrier heterojunction while studies by Palmstrom et al. <sup>8</sup> and Jones et al. <sup>2</sup> suggested that Ge diffuses into the GaAs substrate and occupies Ga sites created by Ga outdiffusion.

Fig. 5.9 shows the DSC traces obtained for five scan rates of 10-100 °C/min and it can be noticed that as the heating rate is increased, the peaks shift to higher temperatures. Kissinger <sup>8</sup> demonstrated that this peak temperature shift is determined by the activation energy of each reaction and Clevenger et al. <sup>6</sup> showed that we can apply this type of analysis to thin film solid state reactions. According to Kissinger's equation:

$$\ln(H/T_p^2) = C - Q/kT_p$$

where H is the heating rate, C is a constant, T<sub>p</sub> is the peak temperature, Q is the activation energy of the reaction associated with the peak, and k is the Boltzmann constant. The activation energy, Q was obtained by plotting  $\ln(H/T_p^2)$  vs.  $-(1/T_p)$  for the heating rates and peak temperatures shown in Fig. 5.10.

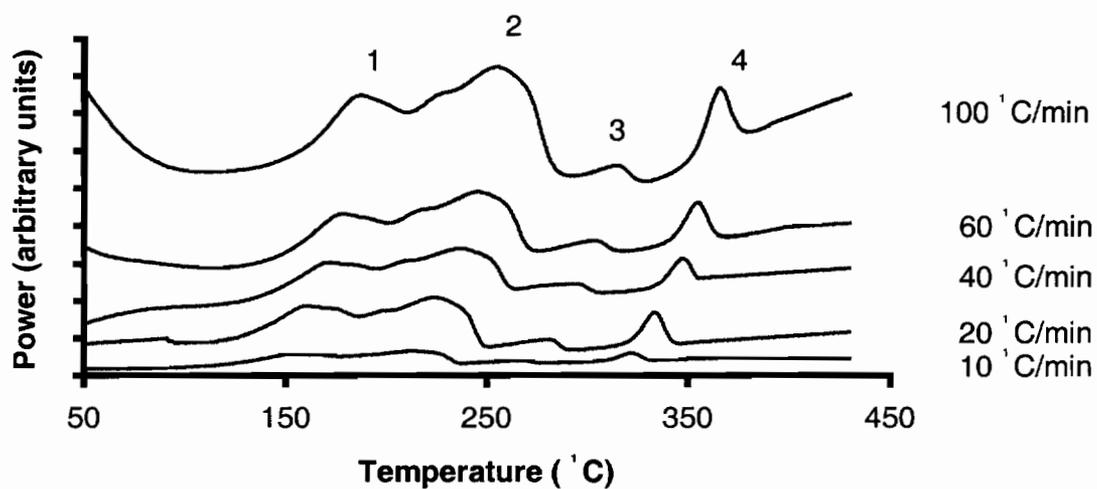


Figure 5.9. DSC traces for Pd(20 nm)/Ge(150 nm)/Pd(50 nm) multiple thin film stacks heated from 10 to 100  $^{\circ}\text{C}/\text{min}$ .

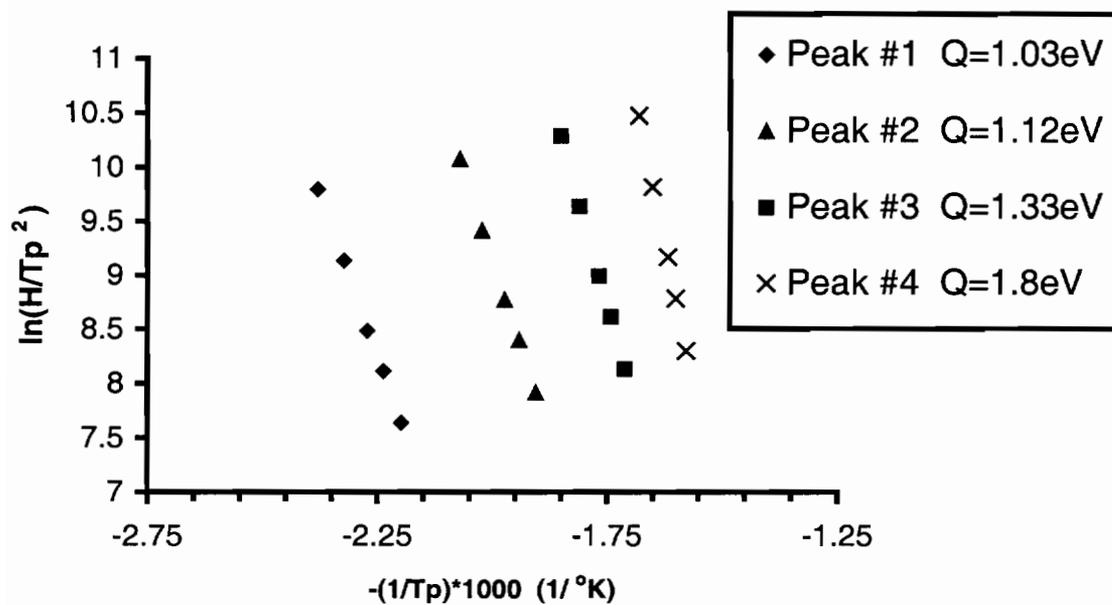


Figure 5.10. Kissinger plots and the activation energies associated with each solid state reaction.

Based on the analysis presented in section 4.3, the activation energy of Pd<sub>2</sub>Ge formation was found to be 1.12 eV. Ottaviani et al.<sup>9</sup> calculated an activation energy of 1.5 eV for the same thin film system by using backscattering spectroscopy and X-ray diffraction. Their study included a-Ge and c-Ge and the same activation energy was observed for both PdGe and Pd<sub>2</sub>Ge. The result for PdGe formation is 1.33 eV, which slightly underestimates their value. Numerous bulk Ge crystallization kinetics studies have been done in the past and a wide range of values were found<sup>11</sup>. The most recent study by Edelman et al.<sup>12</sup> estimated an average activation energy of 2 eV for bulk Ge crystallization and they have also shown that enhanced kinetics could take place due to metallization which results in lower activation energies. In this work, the finding for the activation energy of Ge crystallization at the interface with PdGe is 1.8 eV, which is in good agreement with previous research.

In this section, DSC was correlated with TEM to identify and analyze the solid state reactions that take place during Pd-Ge on GaAs ohmic contact formation. With the exception of Pd-GaAs interactions, it was found that four solid state reactions take place during the annealing of Pd:Ge thin films on top of GaAs and they are as follows: initial Pd-Ge interdiffusion, followed by Pd<sub>2</sub>Ge formation which transforms into PdGe and, at last, Ge solid state epitaxial regrowth on top of GaAs. This study determined the approximate temperature ranges in which the reactions take place and the activation energy associated with each. The results were in reasonable agreement with previous studies performed on similar systems.

### **5.3 *In-Situ* Annealing Transmission Electron Microscopy Study of the Pd/Ge/Pd/GaAs Interfacial Reactions**

In the previous section, the solid state reactions that take place during the formation of the Pd/Ge/Pd ohmic contact to GaAs were analyzed by using a combination of analytical TEM/STEM with energy dispersive x-ray spectroscopy (EDAX) and DSC. It was demonstrated that the majority of the reactions take place at the Pd:Ge interface

whereas the interaction between the Pd and the GaAs substrate is limited to the formation a thin interlayer, not thicker than 8 nm. The results presented in section 5.2 also established the transition temperature associated with each solid phase transformation. These transitions were determined by “freezing” the microstructure present at the DSC peak temperature through a fast cooling rate quench in He atmosphere. In this chapter, as an extension of the previously reported results, the phase formation sequence and the evolution of microstructure during ohmic contact alloying will be investigated by utilizing the in-situ annealing TEM technique. By using this method, it is possible to directly observe both germanide phase formation and Ge SPE growth on GaAs. This technique also allows kinetic and microstructural information to be observed during annealing and provides a continuous and complete record of phase and microstructure evolution.

As-deposited Pd (20 nm) / a-Ge (150 nm) / Pd (50 nm)/ GaAs cross-sectional samples of equal thickness were produced by using a focused ion beam (FIB) method that was described in section 4.5.1. The advantage of using this sample preparation technique for in-situ TEM experiments is two fold. Firstly, it provides a larger cross-sectional electron transparent area which renders a more extended view of the thin films stack. Secondly, it could answer a concern regarding the accuracy of all in-situ TEM experiments in general which is the thin foil surface effects. The thickness of the transparent foil could be somewhat controlled, thus one would be able to determine the surface effects on the observed experiments by analyzing the same reaction on foils with different thickness.

A set of ten TEM samples was prepared from the same as-deposited wafer. These samples were loaded into a Gatan double tilt heating holder and then annealed in-situ in a JEOL CX-200 TEM equipped with a Gatan intensified video camera. Isothermal as well as constant heating rate annealing between 130 °C and 400 °C was performed on this set of samples. The recorded temperature correction varied from -9 °C to -24 °C and was established by direct comparison with a DSC scan of equal heating rate.

The kinetics of the solid state reactions that occur during ohmic contact formation were determined by measuring the grain growth rates associated with each phase from the videotape observations. Images captured from the videotape provided a suitable way of performing these measurements.

Figures 5.11 through 5.18 represent a sequence of video captured images of an ohmic contact structure subjected to 100 °C/min. heating ramp rate followed by a 10 min. holding time at 318 °C. This procedure resembles rapid thermal annealing (RTA) which is compatible with typical integrated circuits processing requirements.

The first phase transformation that takes place during annealing is shown in Fig.'s 5.11 and 5.12 where the nucleation and growth of hexagonal Pd<sub>2</sub>Ge proceeded until the whole initial Pd layer is consumed. Both Pd layers reacted with the a-Ge and the newly formed germanide phase was identified by TEM microdiffraction.

The orthorhombic PdGe phase nucleates at the Ge-Pd<sub>2</sub>Ge interface, as demonstrated by Fig. 5.13 and, afterwards, grows, consuming a-Ge and Pd<sub>2</sub>Ge according to:



This reaction requires that Ge diffuses through the PdGe layer and reacts with Pd<sub>2</sub>Ge as shown in Fig. 5.14 and 5.15. At 307 °C, a small amount of Pd<sub>2</sub>Ge is still present at the interface with GaAs, see Fig. 5.15. As the temperature increases, the Pd<sub>2</sub>Ge is consumed and the PdGe surface makes direct contact with the GaAs substrate. In the next stage, the excess a-Ge diffuses through the PdGe grain boundaries and grows on top of the GaAs substrate by a solid phase epitaxy mechanism. This is clearly illustrated in Fig. 5.16, 5.17 and 5.18.

The evidence presented so far, in regard to the microstructure evolution of the Pd-Ge ohmic contact on GaAs, demonstrates the first phase change is the Pd<sub>2</sub>Ge formation. This hexagonal phase then transforms into orthorhombic PdGe followed by solid phase epitaxial growth of Ge at the GaAs interface. In the final stages of ohmic contact

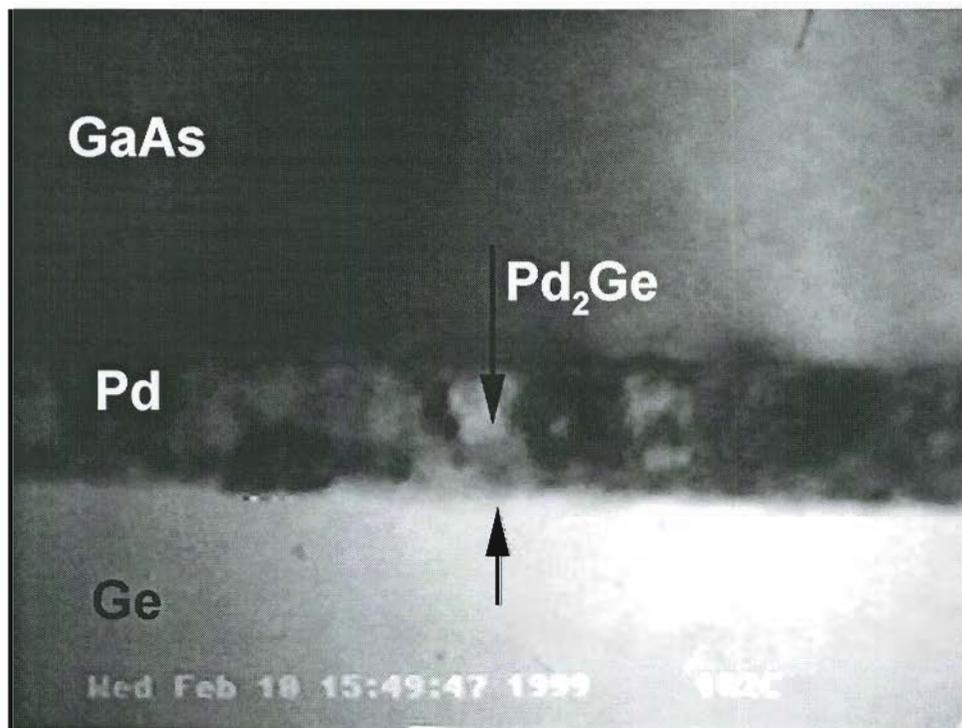


Figure 5.11. Video-captured TEM image of a sample subjected to rapid thermal annealing at 182 °C.

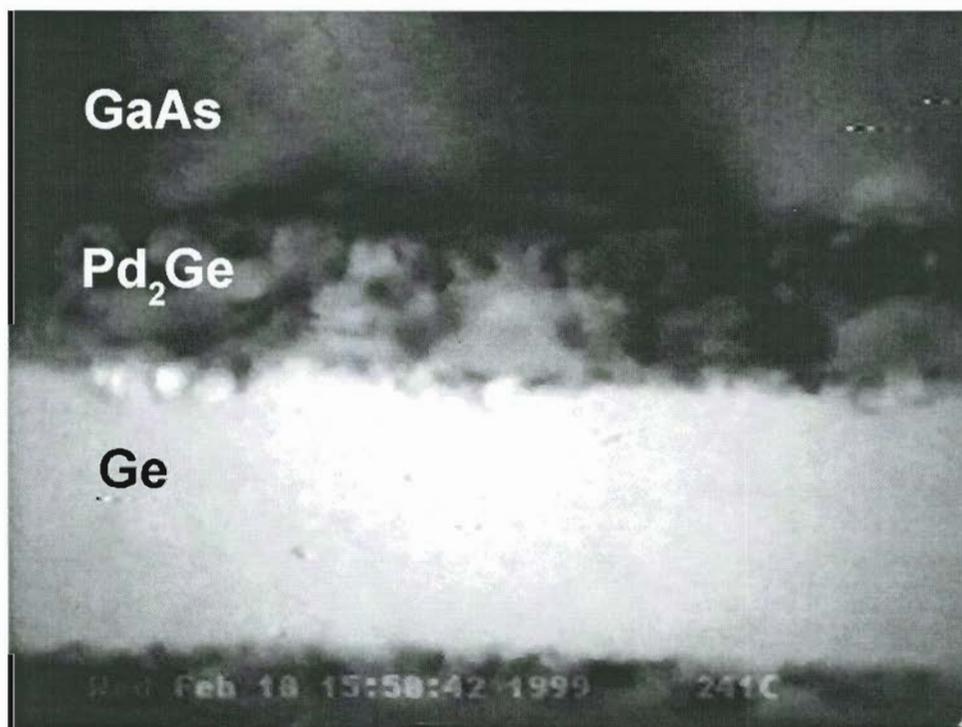


Figure 5.12. Video-captured TEM image of a sample subjected to rapid thermal annealing at 241 °C.

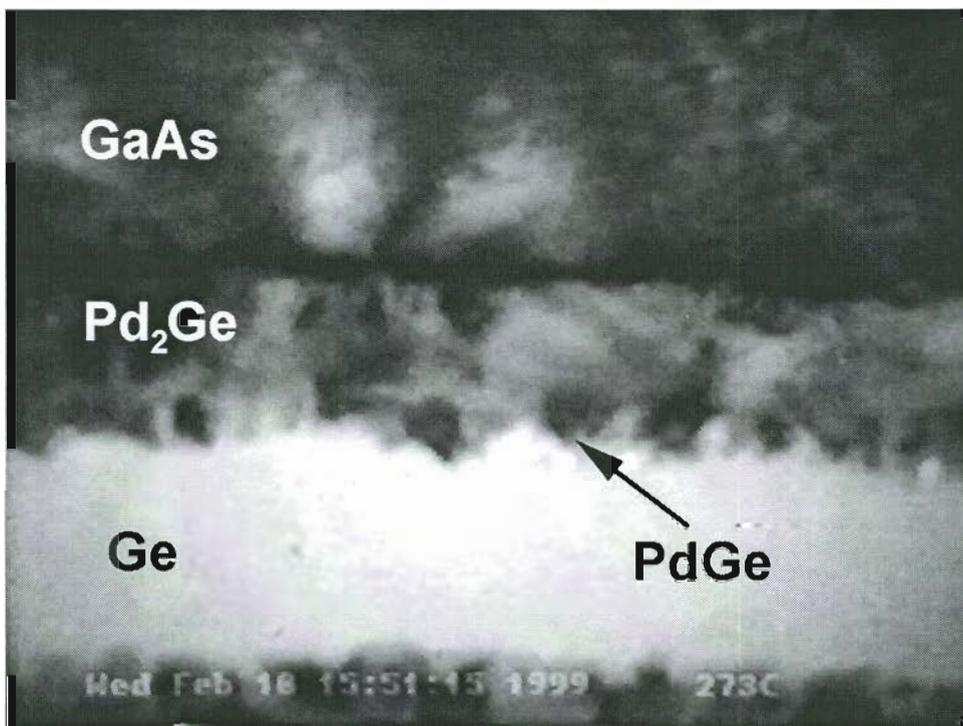


Figure 5.13. Video-captured TEM image of a sample subjected to rapid thermal annealing at 273 °C.



Figure 5.14. Video-captured TEM image of a sample subjected to rapid thermal annealing at 293 °C.

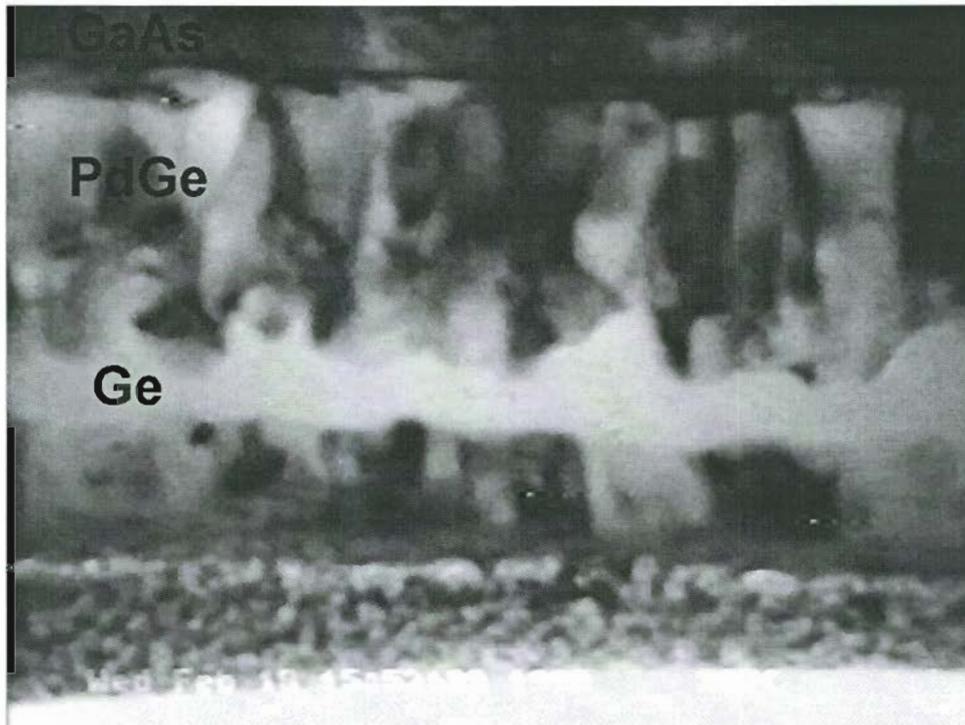


Figure 5.15. Video-captured TEM image of a sample subjected to rapid thermal annealing at 307 °C.

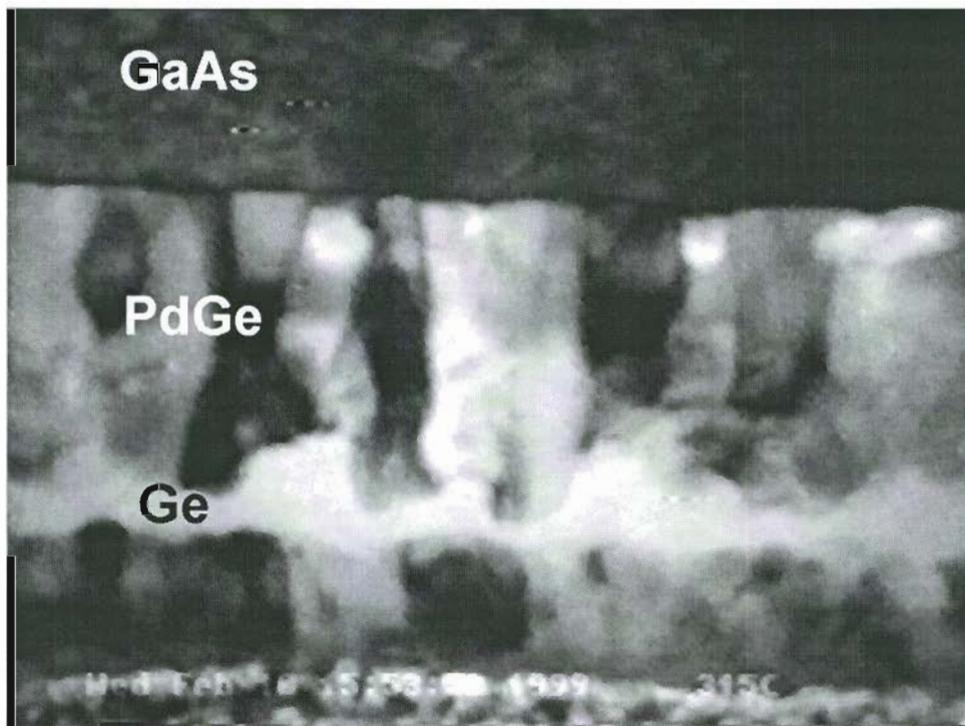


Figure 5.16. Video-captured TEM image of a sample subjected to rapid thermal annealing to 315 °C at the start of the holding period.

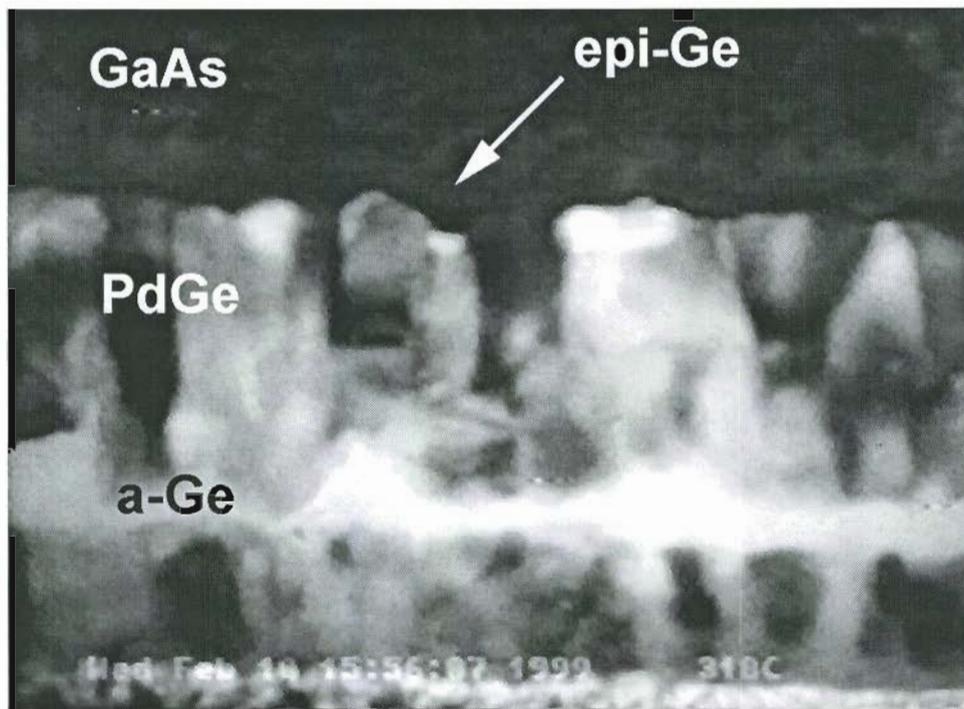


Figure 5.17. Video-captured TEM image of a sample subjected to rapid thermal annealing followed by holding at 318 °C for 3 min.

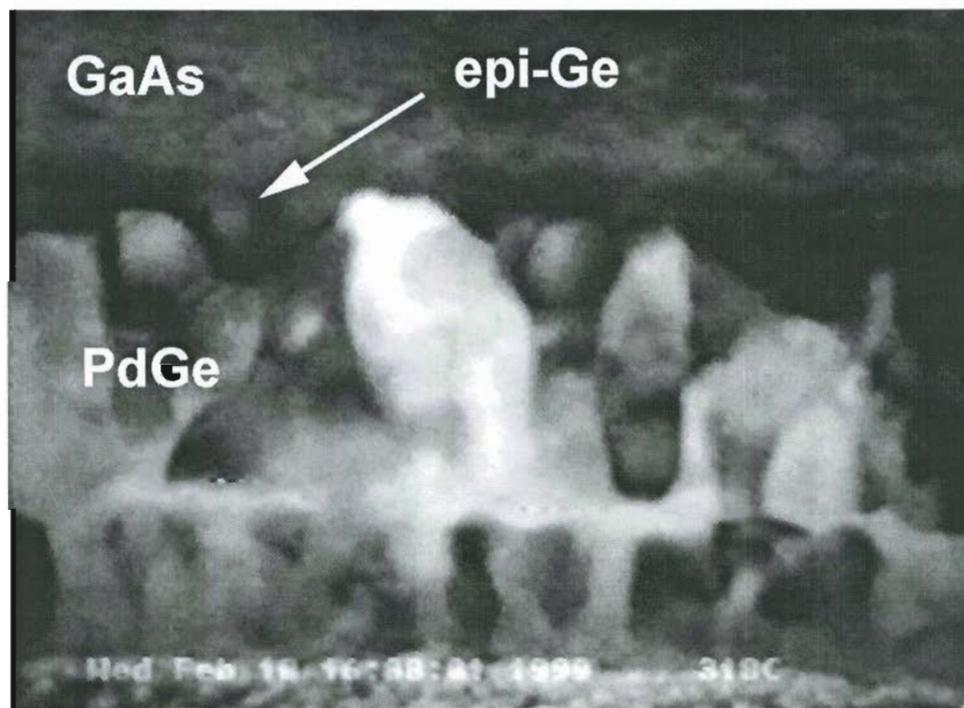


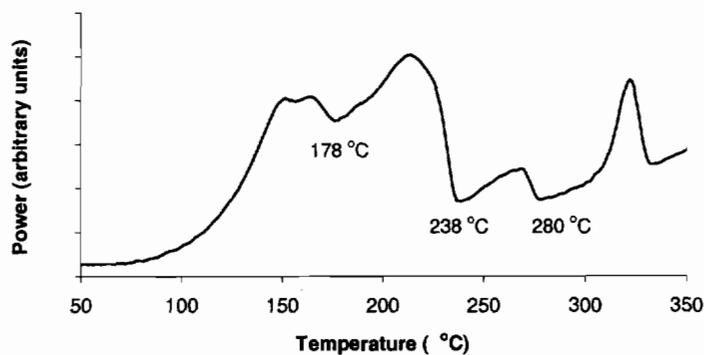
Figure 5.18. Video-captured TEM image of a sample subjected to rapid thermal annealing followed by holding at 318 °C for 10 min.

formation there are two competing reactions that determine the extent of Ge epitaxial growth on GaAs - PdGe formation and Ge crystallization. They both require excess a-Ge and, as shown by the recorded videotapes, the Pd<sub>2</sub>Ge has to be consumed entirely before Ge SPE growth on GaAs would occur.

These findings agreed with the results presented earlier in this chapter that determined the phase formation by combining TEM with the differential scanning calorimetry (DSC) method. They also indicate that, in the overall thin film stack system, the dominant solid state reactions take place between Pd and Ge. The consumption of the GaAs is very limited and its dimensions did not permit a complete microstructural characterization of this reaction layer as the electron probe size was larger than the thickness of the layer. Moreover, as a consequence of the videotape recordings limited resolution, the continuous detection of this layer was disrupted. However, a previous study of the Pd-GaAs system by Sands et al. <sup>3</sup>, showed that this layer consists of a ternary phase, Pd<sub>x</sub>GaAs and it is very probable the same phase would form in the Ge/Pd/GaAs system.

In order to analyze the kinetic parameters that describe the formation of Pd<sub>2</sub>Ge and PdGe, an Arrhenius temperature dependence was assumed. For this type of analysis, the accuracy of the results relies on the precise temperature measurements. Since the thermocouple configuration of the typical TEM heating holders does not allow recording the actual temperature at the specimen surface, one needs to calibrate the system. This is a common problem associated with any TEM in-situ heating experiment and, so far, a unique fit-for-all temperature calibration procedure has not been yet developed. In this study, the temperature was calibrated by comparing the DSC analysis results with the real-time videotape recordings. The same heating rate was used in both experiments to measure the temperature associated with three distinctive events in the microstructure evolution of the contact. In the DSC scan presented in Fig. 5.19 the start and the end of Pd<sub>2</sub>Ge formation are measured at 178 °C and 238 °C, respectively. In addition to these two data points, the end of PdGe formation, measured at 270 °C could also be used as

good indicator because it is a well-defined stage in the microstructure evolution of the contact.



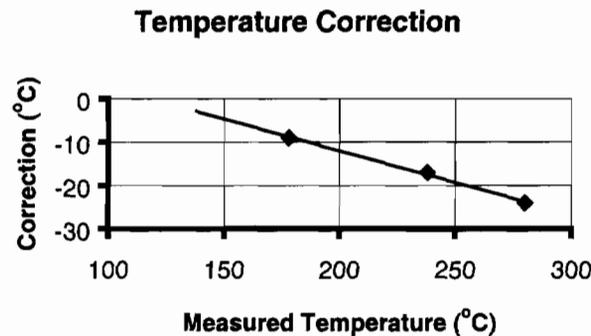
**Figure 5.19. DSC scan of Pd/Ge/Pd multilayer film heated at 12 °C/min.**

Table 5-I shows two sets of temperature values associated with these three data points, one determined by DSC and the other by in-situ TEM. Both sets of measurements were performed under the same heating rate, 12 °C/min.

**Table 5-I. In-situ TEM temperature correction determination. The heating rate for both, DSC and in-situ TEM was 12 °C/min.**

	In-Situ TEM video tape recording (°C)	DSC temperature measurement (°C)	Correction (°C)
Pd <sub>2</sub> Ge start	187	178	-9
Pd <sub>2</sub> Ge end	255	238	-17
PdGe end	304	280	-24

Assuming the same linear tendency, the temperature correction was extrapolated to lower temperatures, as demonstrated in Fig. 5.20



**Figure 5.20. Temperature correction plot as established by table 5-I.**

The growth of both germanide phases is noted to be proportional to the square root of the annealing time, as shown by Fig.5.21 and Fig. 5.22. This time dependence indicates a diffusion controlled mechanism as described by:

$$X^2 = 4 \cdot D(T) \cdot t \quad \text{where:} \quad (1)$$

X is the thickness of the germanide phase, t is the annealing time and D(T) is the temperature dependent velocity constant which may be expressed as :

$$D(T) = D_0 \cdot e^{-E_a/kT} \quad \text{where :} \quad (2)$$

$E_a$  is the activation energy,  $D_0$  is a temperature independent coefficient, T is the temperature and k is the Boltzmann constant.

By taking the 1-st derivative with respect to t at both sides of equation (1), we obtain:

$$X \frac{dX}{dt} = 2 \cdot D_0 \cdot e^{-E_a/kT} \quad \text{and}$$

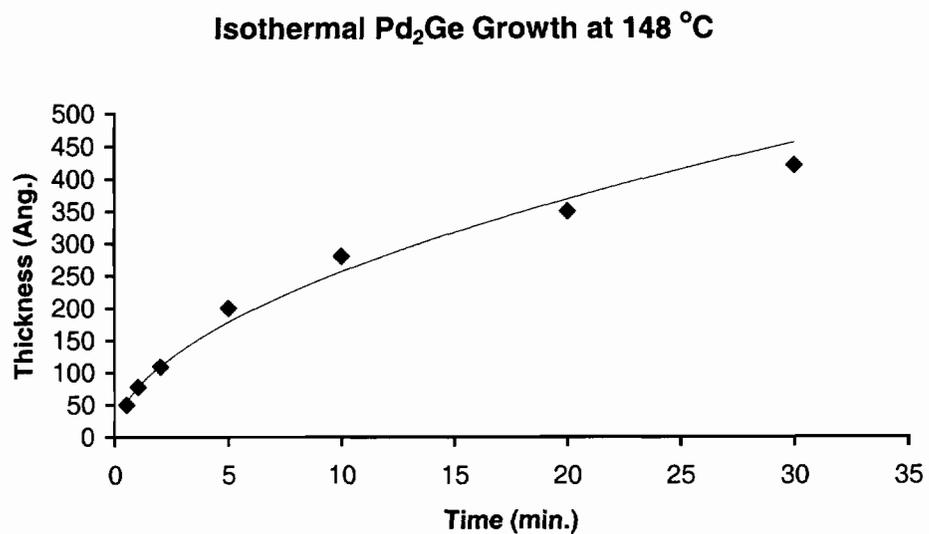


Figure 5.21. Pd<sub>2</sub>Ge isothermal growth as measured from the in-situ TEM recordings

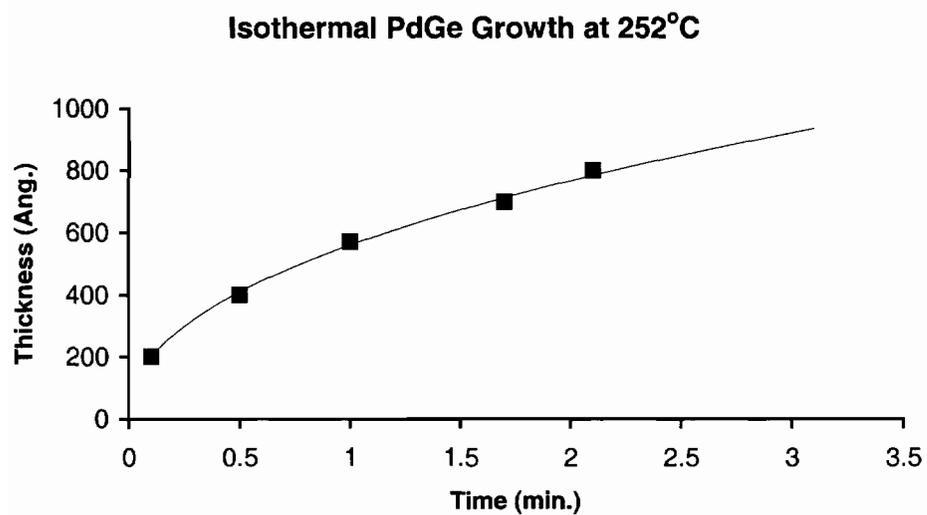


Figure 5.22. PdGe isothermal growth as measured from the in-situ TEM recordings

$$\ln\left(X \frac{dX}{dt}\right) = \ln(2 \cdot D_0) - \frac{E_a}{kT} \quad (3)$$

It could be noticed that by plotting  $\ln[X(dX/dt)]$  vs.  $-1/kT$  one could obtain  $D_0$  and  $E_a$  by measuring the intercept to the y axis and the slope, respectively. Figures 5.23 and 5.24 show the Arrhenius plots associated with the evolution of both germanide phases. Based on the analysis presented above, the activation energy of  $\text{Pd}_2\text{Ge}$  formation was found to be 0.98 eV. In the previous chapter, a 1.12eV was calculated by using the DSC Kissinger plot method. Scott et al.<sup>13</sup> studied the kinetics of the Pd/c-Ge interactions and they obtained a 1.08 eV activation energy for the growth of the  $\text{Pd}_2\text{Ge}$  hexagonal phase. Although, their analysis started with an initial single crystal Ge phase as opposed to amorphous Ge used in this study, the results show a very close agreement. Ottaviani et al.<sup>4</sup> calculated an activation energy of 1.5 eV for the same thin film system by using backscattering spectroscopy and X-ray diffraction. Their study included a-Ge and c-Ge and the same activation energy was observed for both PdGe and  $\text{Pd}_2\text{Ge}$ . Our in-situ TEM findings for PdGe formation is 1.29 eV which slightly underestimates their value. The DSC analysis, presented in section 5.2 of this chapter, revealed a 1.33 eV activation energy for this phase growth which agrees well with the in-situ TEM results.

In addition to the growth of both germanide phases kinetic analysis, these in-situ TEM experiments allowed us to observe several other features of the ohmic contact microstructure evolution. In the final stages of the ohmic contact formation, the Ge diffuses through the PdGe grain boundaries and grows epitaxially on top of the GaAs substrate. Although the exact role played by this Ge layer in the charge transport mechanism is not yet clearly established, it seems there is some consensus over the fact that Ge transport to the GaAs surface provides an ohmic contact with low resistivity<sup>1,8</sup>. Since the Ge transport to the GaAs surface is achieved by grain boundary diffusion through the PdGe layer, it implies that PdGe grain size would affect this transport mechanism. One way of controlling the shape and size of the PdGe grains is by modifying the annealing procedure of the ohmic contact. The videotape recordings

demonstrated that the PdGe nucleates at the a-Ge:Pd<sub>2</sub>Ge interface and then grows, mainly, in one direction until the whole Pd<sub>2</sub>Ge phase is consumed. In the first stage of the PdGe formation, mainly nucleation takes place at the interface. The second stage is represented by a columnar grain growth and finally, in the third stage, PdGe coarsening combined with the formation of an equiaxial grain structure. Clearly, the most favorable configuration for the Ge transport is given by the columnar grain structure because of the high grain boundary density. It is well known that grain boundary diffusion is faster than intergrain diffusion. However, the large difference in diffusion volumes for these two mechanisms limits the effectiveness of grain boundary diffusion in controlling the overall rate of diffusion in polycrystalline materials. For compounds, the grain boundary diffusion is expected to prevail under a large temperature range due to the atom-type-site-specific mechanisms that are generally associated with these materials. One way to achieve the columnar grain microstructure is by a two step annealing process and Fig. 5.25 clearly illustrates just that. The microstructure in Fig. 5.26 was obtained by a fast ramp rate followed by holding at 318 °C for 5 min., typical annealing method employed in the IC fabrication line. In Fig. 5.25 the columnar PdGe grain microstructure resulted from a two step annealing procedure that consisted of fast ramping to 210 °C and holding for 5 min. at this temperature, followed by a second holding period at 320 °C for 5 min. The low temperature isothermal provided a high density of PdGe nuclei at the a-Ge:Pd<sub>2</sub>Ge interface without 2D coarsening while the second rapid ramp rate step contributed to the columnar growth of these nuclei. A rapid ramp rate anneal through the PdGe nucleation period renders a lower nuclei density which, in turn, favors the subsequential lateral grain growth. This translates into a lower density of PdGe grain boundaries and a non-uniform Ge transport to the GaAs surface.

At higher annealing temperatures, the formation of dislocations in the GaAs substrate starts to be noticed. Their presence is probably due to the relief of the high level of stress present at the interface. In the following chapter, measurements of the residual stress induced by the Pd-Ge ohmic contact formation on GaAs will be presented and the

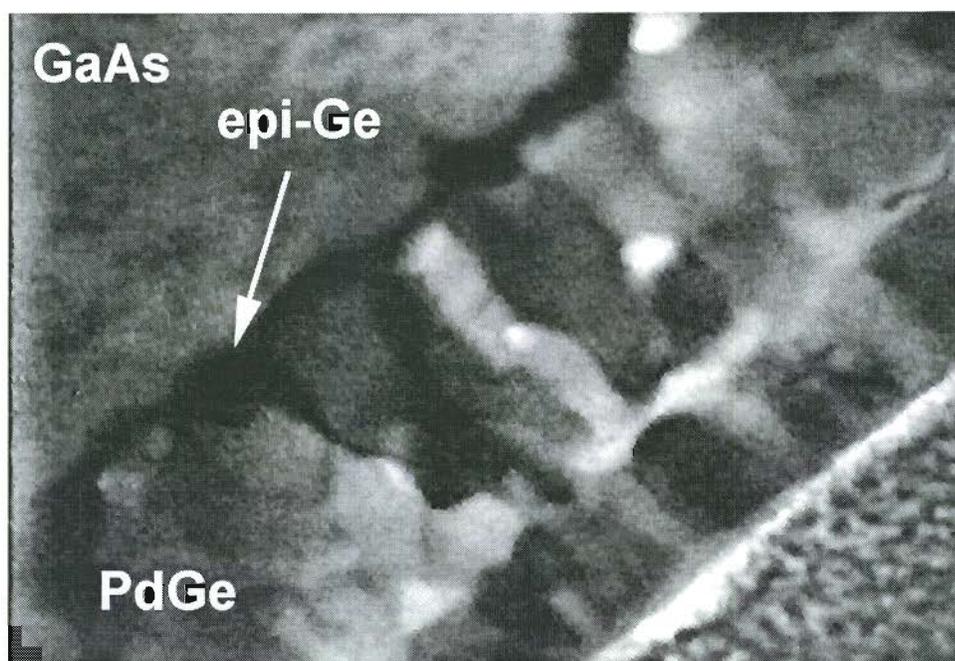


Figure 5.25. Video-captured TEM image of a sample annealed at 210 °C for 5 min, followed by a second holding period at 320 °C for 5 min.

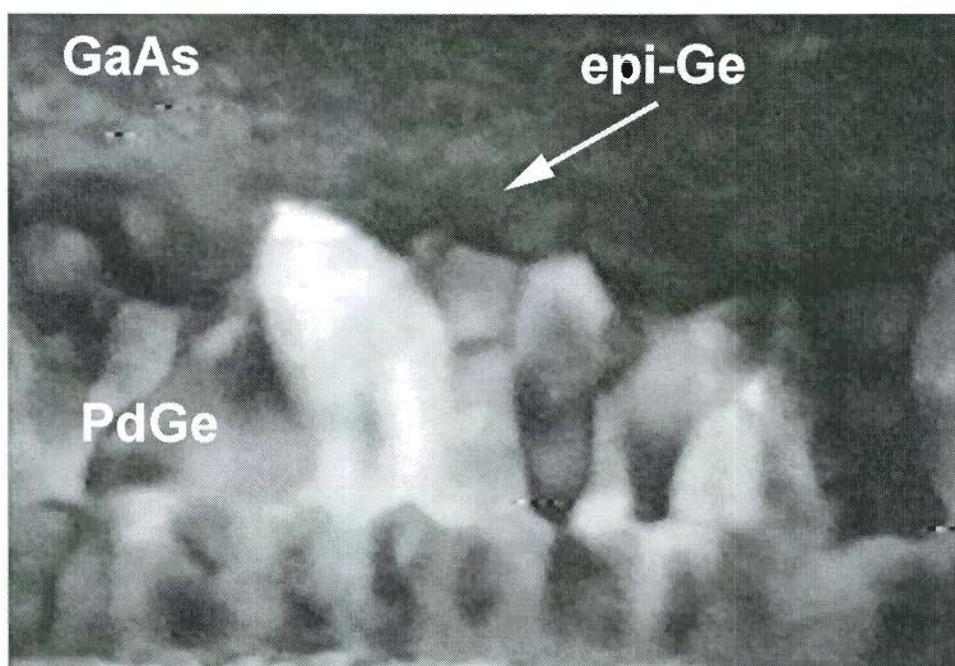


Figure 5.26. Video-captured TEM image of a sample subjected to rapid thermal annealing to 318 °C followed by a holding period of 5 min.

issue will be discussed in greater detail. Fig. 5. 27 demonstrates an example of such a dislocation.

In this section, the solid state reactions that occur during the Pd-Ge ohmic contact formation on GaAs were studied by *in-situ* TEM analysis.



Figure 5.27. Dislocation along the [111] plane in the GaAs substrate that was formed as a result of a higher annealing temperatures

The results agreed with the findings presented in section 5.2 of this chapter where it was demonstrated that, excluding the Pd-GaAs interactions, four phase transitions take place during annealing:

1. Pd-Ge interdiffusion and formation of a Pd<sub>2</sub>Ge amorphous mixture.
2. Hexagonal Pd<sub>2</sub>Ge formation.
3. Orthorhombic PdGe transformation.
4. Excess Ge crystallization.

The kinetics of the solid state reactions, which occur during ohmic contact formation, were determined by measuring the grain growth rates associated with each phase from the videotape observations. It was established that the growth of both germanide phases is diffusion controlled and it could be described by the following relationship:

$$X^2 = 4 \cdot D_0 \cdot e^{-E_a/kT} \cdot t \quad \text{where:}$$

X is the thickness, t is the annealing time,  $E_a$  is the activation energy,  $D_0$  is a temperature independent coefficient, T is the temperature and k is the Boltzmann constant. For both germanide phases, all the kinetic parameters were calculated from the Arrhenius plots presented earlier and it was found that:

$$X^2 = 2.94 \cdot 10^{15} \cdot e^{-0.98\text{eV}/kT} \cdot t$$

describes the  $\text{Pd}_2\text{Ge}$  growth and

$$X^2 = 6.89 \cdot 10^{17} \cdot e^{-1.28\text{eV}/kT} \cdot t$$

describes the  $\text{PdGe}$  growth, where X is the thickness in angstroms, T is the temperature in  $^\circ\text{K}$ , k is the Boltzmann constant and t is the time measured in minutes.

The values found for the activation energies were in very close agreement with the ones determined in the previous section. Furthermore, this data agreed with other studies presented in the literature that measured the activation energies through other indirect methods such as backscattering and x-ray techniques.

A new temperature calibration method for the in-situ TEM measurements was also presented in this section. The DSC information was correlated with distinct events that were easily observed in the in-situ TEM experiments. Because the temperature could

be determined very accurately in the DSC cell, this technique provides a relatively precise method of calibration that could easily be adapted to study other systems by in-situ TEM.

In this chapter, the phase formation sequence of the Pd/Ge/Pd thin film system on GaAs was determined. This information opens the way for a better understanding of the electronic behavior of the contact that will be further discussed in chapter 8.

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## 6. The Effect of Stress on the Ge Solid Phase Epitaxial Growth

Solid phase epitaxial (SPE) growth with a transport medium is a fascinating yet not completely understood phenomenon with many potential applications in the semiconductor industry. A general description of the SPE mechanism was made in chapter 3.2.2. Good reviews <sup>1,2</sup> treating the SPE growth in general were written in the past which, mainly, described homoepitaxial growth, with or without the transport medium. However, only a few cases of technologically important solid phase heteroepitaxy with transport medium were reported in the literature. Ma et al. <sup>3</sup> demonstrated SiGe SPE growth on Si through a Au layer. More recently, two systems relating to CoSi<sub>2</sub> epitaxial growth on Si through different transport media were reported. Dass et al. <sup>4</sup> and Hsia et al. <sup>5</sup> showed CoSi<sub>2</sub> SPE growth through a Ti layer by the titanium mediated epitaxy (TIME) method whereas Tung <sup>6</sup> demonstrated CoSi<sub>2</sub> SPE growth through an oxide layer, the oxide mediated epitaxy (OME) method. But the first case of solid phase heteroepitaxial growth with transport medium and probably the most studied such system was, to the best of my knowledge, reported by Marshall et al. <sup>7</sup>, in connection with the Pd-Ge ohmic contact formation on GaAs. Their studies revealed that Ge in excess of the amount needed to form the PdGe compound is necessary in order to obtain a low resistance ohmic contact on GaAs. They have also demonstrated that during annealing of a Pd:Ge bylayer on GaAs, the Ge is transported to the GaAs interface where it grows by a SPE mechanism.

If the source material is deposited directly on the substrate, without intermediate medium, and then annealed, the quality of the epitaxially-grown layer suffers or, in some cases, epitaxy doesn't occur at all. The exact role played by the intermediate layer is not yet entirely understood even though few common features could be noted in some of the

SPE systems mentioned earlier. It was suggested that a “cleaning” effect takes place as the intermediate layer reacts with the substrate or reduces the oxides present at the surface, this way creating an ideal surface for epitaxy. This explanation could be valid for the Ge/Pd/GaAs and Co/Ti/Si systems. Pd reacts with GaAs at room temperature to form a very uniform layer of ternary  $\text{Pd}_x\text{GaAs}$ <sup>8</sup> and Ti reduces the  $\text{SiO}_2$  or reacts with Si to form a silicide phase. A similar argument could be made for the SiGe/Au/Si where Au acts as a solvent for Si during annealing, modifying the surface of the substrate and hence, promoting a precipitation of SiGe through SPE growth. However, this “cleaning” effect cannot explain the OME of  $\text{CoSi}_2$  where the initial interface consists of  $\text{SiO}_x/\text{Si}$ . In fact, a previous study by Tung<sup>6</sup> recognizes that the role of the oxide is not a chemical one and he extended the same argument to TIME systems. According to his interpretation, the intermediate layer plays the role of a diffusion barrier, which alters the silicide phase formation sequence and promotes the epitaxial growth of  $\text{CoSi}_2$ .

The work of Aziz et al.<sup>9</sup> demonstrated the effect of stress on a heteroepitaxial SPE system without an intermediate layer. They started with a-SiGe/Si and showed that externally applied tensile stress increases the growth rate of SiGe on Si whereas the compressive stress doesn't affect the epitaxial growth as much. The intensity of tensile stress at the wafer surface necessary to change the kinetics of epitaxial growth significantly was 6 kbar, which is commonly attained at a metal/Si interface during annealing steps. This implies that an intermediate layer could affect the kinetics of SPE growth by a stress-induced mechanism. In this chapter, it will be demonstrated how several microstructural configurations of the Ge/Pd/GaAs relate to the residual stress induced by various annealing procedures.

Pd (20 nm)/Ge (150 nm)/Pd (50 nm) layers were deposited on <100> oriented GaAs substrates by alternate electron beam evaporation. Prior to evaporation, the wafers were cleaned by dipping in a 10:1 HCl solution for 30 sec. and then rinsed in deionized water. Various ohmic contact microstructures were obtained by annealing the samples under forming gas atmosphere that consisted of 4% $\text{H}_2$ -96% $\text{N}_2$ . A micro-cantilever beam bending technique was employed to measure the residual stress induced by the different

microstructure configurations present in the contact system. Precise geometry cantilever beam structures were produced by focused ion beam (FIB) milling. Each sample was glued to a Mo washer and then mechanically ground on lapping discs from the substrate side. A second stage, more precise thinning was carried out in the FIB system by milling  $50 \times 100 \mu\text{m}$  large areas. The final thickness in these areas ranged from 1.25 to 1.4  $\mu\text{m}$ , including both the GaAs substrate and the Pd/Ge ohmic contact thin film stack. Finally, micro-cantilever beam structures were produced by FIB milling and then its dimensions and the beam deflection under stress were measured in the scanning electron microscope. The FIB prepared TEM specimens were produced from detached areas of the wafer in close proximity to the cantilever beam structures. Fig. 6.1 illustrates a structure produced by this technique.

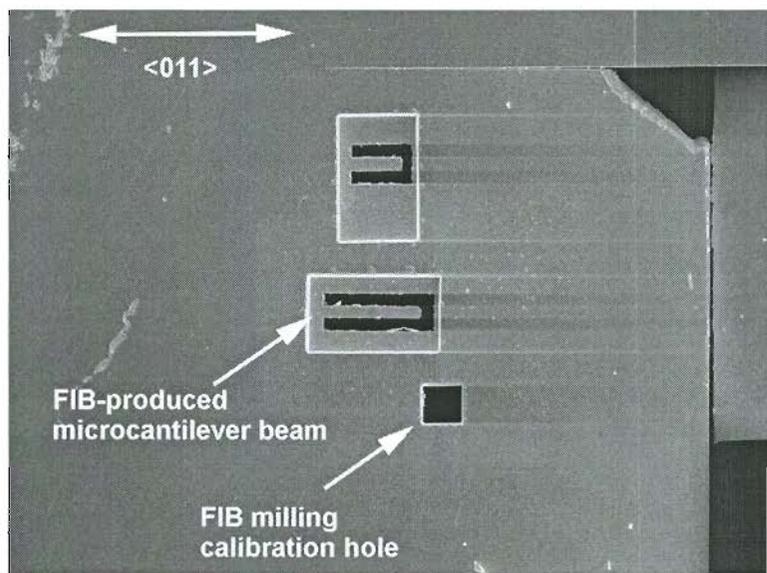


Figure 6.1. Microcantilever beam structure aligned along the  $\langle 011 \rangle$  direction.

The microstructure evolution study presented in chapter 5 showed that several solid state reactions take place during the annealing of Pd:Ge thin films on top of GaAs and they are as follows: initial as deposited Pd-GaAs reaction to form the ternary  $\text{Pd}_x\text{GaAs}$  phase, followed by  $\text{Pd}_2\text{Ge}$  formation which transforms into PdGe and at last, Ge solid state epitaxial growth on top of GaAs. The ternary phase decomposes before Ge

solid state epitaxial growth would take place. Fig. 5.5 demonstrates that, after annealing at 269 °C and cooling by quenching in He atmosphere, Pd<sub>2</sub>Ge hexagonal phase consumed all the initially deposited Pd. At the Ge - Pd<sub>2</sub>Ge interface, Ge rich PdGe orthorhombic phase was identified and the GaAs substrate is separated from the Pd<sub>2</sub>Ge layer by a thin ternary compound, Pd<sub>x</sub>GaAs.

After annealing at 322 °C followed by quenching, the predominant phase present is the PdGe compound. Part of the unreacted Ge crystallized between the compound layers although a-Ge is still present. The Pd<sub>x</sub>GaAs ternary compound is not present and the PdGe layer is in direct contact with the GaAs substrate. Fig. 5.6 provides a cross-sectional view of a sample annealed at this temperature.

Fig. 6.2 reveals that after annealing at 325 °C for 5 min., Ge solid phase epitaxial growth on GaAs takes place. As the annealing temperature was increased to 400 °C, the integrity of the Ge epitaxial layer suffered. This aspect of the microstructure evolution and its effects on the contact resistivity will be discussed in chapter 7. Fig. 6.3 provides evidence for 3D islanding and the presence of dislocations along the {111} planes.

The residual stress associated with each microstructure presented above was calculated by measuring the micro-cantilever beam deflection as shown in Fig. 6.4. A modified Stoney's equation for determining the uniaxial stress in a cantilever beam was employed, as suggested by Berry and Pritchett<sup>10</sup>.

$$\sigma = \frac{E_s}{(1-\nu^2)} \frac{t^2}{6b} \frac{1}{R}$$

$E_s$  and  $\nu$  are the substrate Young's modulus and Poisson's ratio,  $t$  is the thickness of the substrate,  $b$  is the thin film thickness and  $R$  is the curvature of the deflection which can be approximated by  $1/R = 2\delta/L^2$ , where  $\delta$  is the deflection of the cantilever beam at a distance  $L$  from the fixed end. All of the micro-cantilever beams were milled in the {100} plane along <011> directions. Brantley's<sup>11</sup> calculated values for the Young's modulus and Poisson's ratio associated with this plane and directions were used.

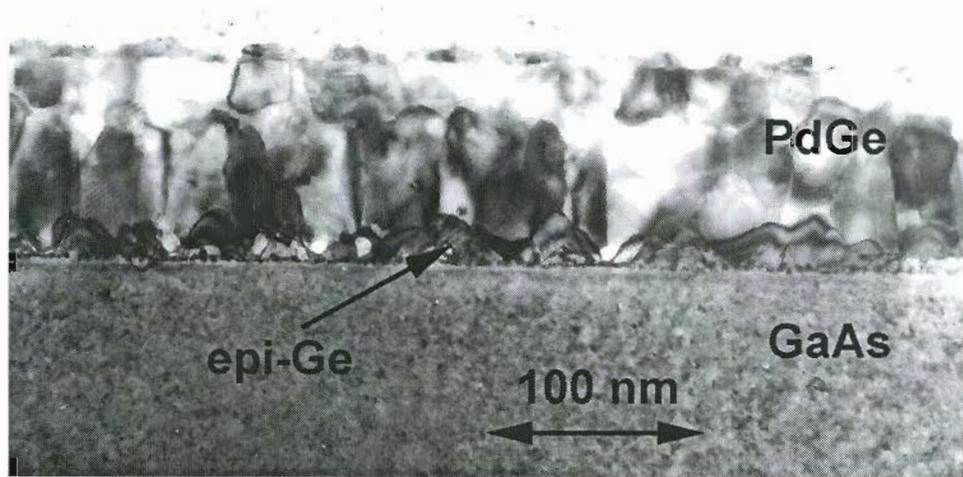


Figure 6.2. Cross-sectional TEM image of a sample annealed at 325 °C for 5 min.

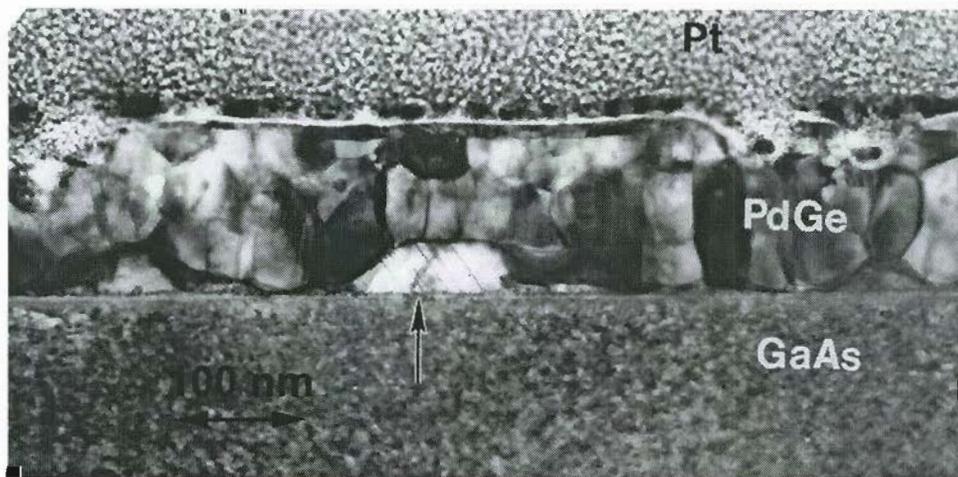


Figure 6.3. Cross-sectional TEM image of a sample annealed at 400 °C for 5 min. The arrow indicates stacking faults present in the Ge epitaxial layer.

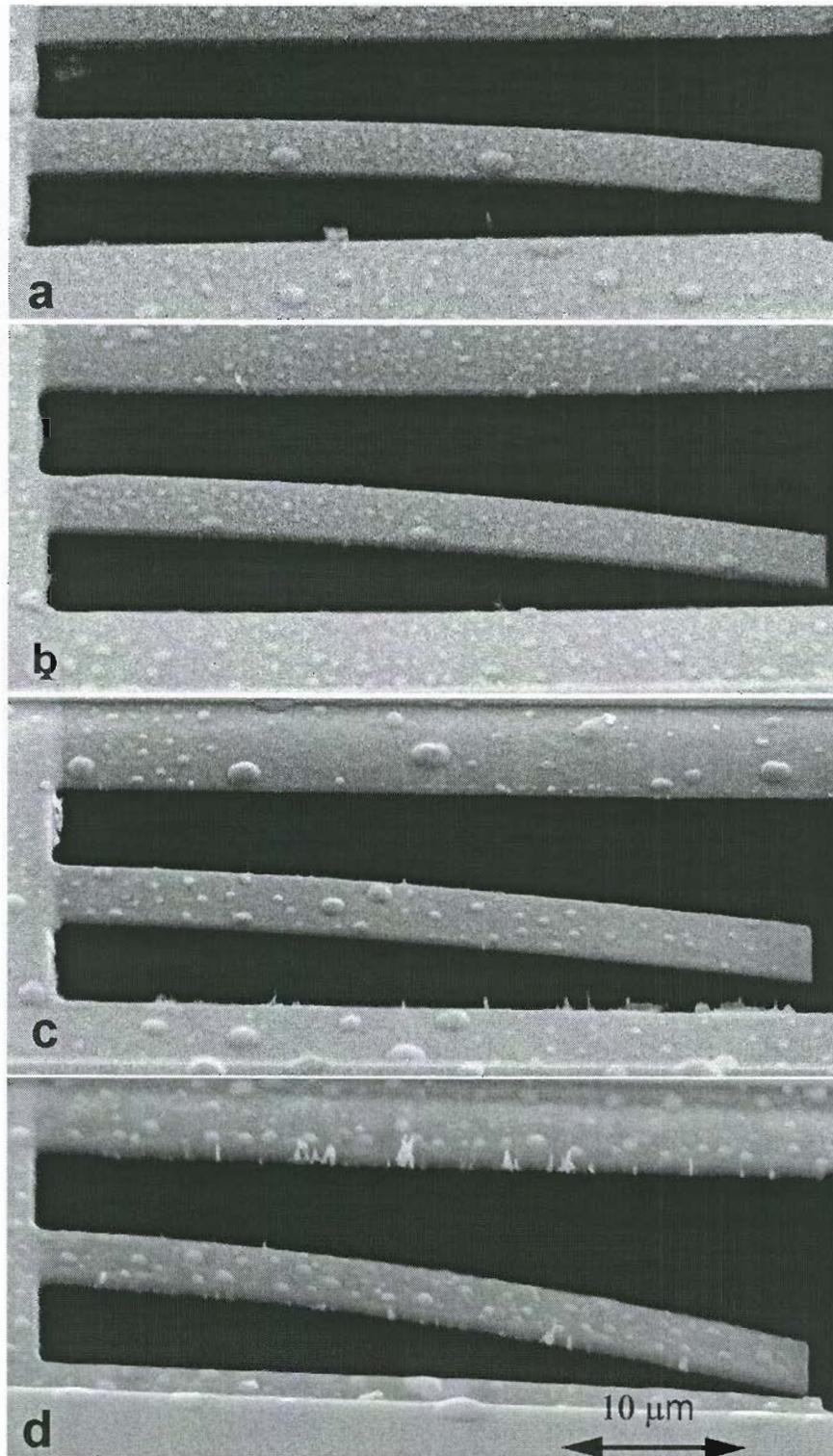


Figure 6.4. SEM 45° tilt view of FIB produced microcantilever beams (GaAs up), deflected under the residual tensile stress present. a) Specimen heated at 269 °C and quenched in He atmosphere. b) Specimen heated at 322 °C and quenched in He atmosphere. c) Specimen heated at 325 °C for 5 min. and cooled in forming gas atmosphere. d) Specimen heated at 400 °C for 5 min. and cooled in forming gas atmosphere.

Table I. summarizes the residual stress measurement results. It can be noticed that a stress reduction takes place between the sample annealed to 322 °C with no holding time and the sample annealed to 325 °C for 5 min. The TEM analysis shows no evidence of Ge epitaxial growth for a sample annealed at 322 °C with no holding time (see Fig. 5.6).

**Table 6-I. Calculated residual stress based on the measured micro – cantilever beam deflection.**

Specimen annealing method	Thickness of the Pd-Ge thin film stack ( $\mu\text{m}$ )	GaAs substrate thickness ( $\mu\text{m}$ )	Micro-beam deflection ( $\mu\text{m}$ ) at $L = 40 \mu\text{m}$	Thin film residual stress (kbar)
269 °C and quenched	0.156	1.11	.98	1.97
322 °C and quenched	0.182	1.20	4.10	8.26
325 °C and hold for 5 min.	0.182	1.10	3.29	5.58
400 °C and hold for 5 min.	0.182	1.10	5.71	9.69

By increasing the annealing time to 5 min. at 325 °C, Fig. 6.2 demonstrates the Ge transport across the PdGe layer followed by SPE growth on GaAs. This indicates a strong correlation between the stress relaxation and the Ge SPE growth on GaAs. As a result of increasing the annealing temperature to 400 °C, the tensile stress present in the film increases considerably and stacking faults in the Ge epitaxial layer are revealed by the TEM microanalysis (see Fig. 6.3).

The residual stresses associated with the microstructural changes that take place during the final stages of Ge/Pd ohmic contact formation were measured. It was found that Ge SPE growth on GaAs is associated with a slight tensile stress reduction. There are two arguments that can explain the effect of stress on the Ge SPE growth. From a thermodynamic point of view, the Ge SPE growth tends to relax the system, this way minimizing the residual tensile stress energy stored in the thin film stack. Secondly, the SPE growth of Ge could be explained by the change in kinetics associated with the presence of tensile stress induced by the PdGe intermediate layer, formed prior to the Ge transport to the GaAs surface. This effect is related to the one demonstrated by Aziz et al.<sup>9</sup> which showed that an externally applied tensile stress could lower the SPE activation energy. A similar argument could be made for the other solid phase heteroepitaxial systems discussed earlier. Ti and Au have higher thermal expansion coefficient than Si and they are expected to induce tensile stress during annealing. For the OME system, Tung<sup>6</sup> pointed out the importance of using non-stoichiometric  $\text{SiO}_x$  ( $x < 2$ ) oxide as an intermediate layer. According to his study, the use of stoichiometric  $\text{SiO}_2$  thermal oxide as an intermediate layer results in polycrystalline  $\text{CoSi}_2$  growth. Generally, a thermal oxide induces a compressive stress on the Si substrate, however this stress could be reversed to tensile if the content of oxygen is reduced<sup>12</sup>. These findings suggest that tensile stress may be an important ingredient in the SPE growth and the intermediate layer may play a physical role rather than a chemical one. Moreover, from a technological perspective, these results may lead to new methods of using controlled stress in engineering novel SPE systems.

The results presented in connection with other SPE systems indicate that this effect was found for tension stress but not for compressive stress. The reason for increased kinetics cannot be simply attributed only to an added internal energy component because this would be expected to be the same whether a tensile or compressive stress was applied. It is proposed that the accelerating effect of the tensile stress alone was due to the microstructure modification of the interface between the substrate and nucleating phases.

Although the use of lithographically defined micro-cantilever beam bending techniques for stress measurements were previously reported <sup>13</sup>, this study demonstrates a new and more flexible method of fabrication based on FIB milling.

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## **7. The Microstructure Effect on the Ohmic Contact Performance**

Integrated circuits (IC) based on Metal Semiconductor Field Effect Transistor (MESFET) technology and operating at high frequencies are one of the important commercial applications of GaAs. Under high frequency operating conditions, the ohmic contact resistance becomes an important device parameter and affects the performance of the MESFET. Thermally stable, low resistance ohmic contacts to n-type GaAs are necessary in order to be able to fabricate optimal integrated circuits. To develop such ohmic contacts, an investigation of the metal/GaAs interfaces, which strongly affect the electrical properties, is extremely important. As described in chapter 5, when the metal/GaAs system is annealed to form the contact, the reaction between the Pd-Ge and GaAs substrate is complicated. In spite of several previously proposed models, the mechanism that leads to ohmic contact behavior was not yet established.

In chapter 2, the basic charge transport mechanisms were described. The net carrier concentration in the semiconductor surface near the interface with the contact could be altered by the interdiffusion of dopants (in this case Ge) from the metal combined with the formation of lattice defects in GaAs due to outdiffusion of Ga and As to the contact metal. Regions in which carrier concentration is high could have a narrow depletion region and conduct by electron tunneling. The degree to which a high doping level is achieved may depend on the phase and composition of the material in contact with the unreacted GaAs. Alternatively, interfaces that have a low barrier height for conduction could form between certain phases and the GaAs. The extent to which the low contact regions form would depend on the details of the annealing process and the microstructure of the resulting ohmic contact.

When used in integrated circuits, ohmic contacts must, in addition to having a low resistance, also be uniform across a wafer. A further requirement for such contacts is the thermal stability at elevated temperature after the contacts are formed, as the devices are subjected to the subsequential processing steps.

In this chapter, analytical cross-sectional Transmission Electron Microscopy (XTEM) was used to study the interfacial microstructures of Pd-Ge on GaAs. The objective was to correlate the microstructures and the contact resistances measured by the Transmission Line Method (TLM). The main advantages of using XTEM in combination with Energy Dispersive Analytical X-ray (EDAX) for this interface study are that a direct observation of the interfacial microstructure can be made with a high spatial resolution, and that the information on the chemical compositions and the crystallographic structures at the particular area of interest are obtained at the same time. By comparing the differences in the interface morphologies, the chemical compositions, and the crystal structures of the phases formed in these ohmic contacts after they were subjected to various annealing procedures, the variation in the measured contact resistivities can be reasonably explained in terms of microstructure changes. The primary purpose of this chapter was to search for a microstructure which produces the lowest contact resistivity by varying the annealing parameters (temperature and time). In this search, the results obtained in chapter 5 regarding the phase formation sequence were very important.

## **7.1 Constant-Heating-Rate Annealing Experiments**

In this section, the microstructures obtained by annealing under the same conditions as the ones described in chapter 5.1 were correlated with the TLM measurements. Specimens that were annealed by using a constant-heating ramp rate to temperatures that coincided with the DSC peaks (see Fig. 5.1) were quenched in He atmosphere and the resulting ohmic contacts were characterized by specific ohmic contact resistivity measurements. Ohmic contacts with TLM structures were lithographically

defined and then annealed in the DSC cell, the same way as the TEM specimens. After annealing, the specific contact resistivity was determined by TLM measurements.

**Table 7-I. Specific contact resistivity as a function of the annealing method. Three TLM structures were measured for each annealing temperature and the average values were recorded.**

Annealing temperature (°C)	Specific contact resistivity ( $10^{-6} * \Omega\text{-cm}^2$ )
161 °C and quenched	Not ohmic
214 °C and quenched	Not ohmic
269 °C and quenched	88.5
322 °C and quenched	4.34
380 °C and slowly cooled	3.64

Table 7-I summarizes the TLM measurements obtained. The as deposited samples as well as the samples annealed at 161 °C and 214 °C showed no ohmic behavior. A relatively high resistivity ohmic contact was obtained after annealing at 269 °C. Figure 5.5 provided a cross-sectional TEM image of a sample annealed at this temperature. In studying the Pd/GaAs system, Sands et al. <sup>1</sup> demonstrated that around 250 °C, a phase transition takes place as the Pd<sub>x</sub>GaAs ternary compound transforms from “phase I” to “phase II”. Although the large size of the electron beam probe did not allow to characterize this thin interfacial layer, it is very possible that the same phase transformation would take place at the Pd<sub>2</sub>Ge-GaAs interface. The onset of the contact behavior may be associated with the transition from “phase I” to “phase II”. A much lower ohmic contact resistivity is obtained after annealing at 322 °C. Fig. 5.6 shows no

$\text{Pd}_x\text{GaAs}$  ternary phase present at the interface which suggests the sharp decrease in the contact resistivity can be attributed to the decomposition of the ternary compound.

The lowest specific ohmic contact resistivity was obtained after annealing at 380 °C followed by a slower cooling in the forming gas atmosphere. This annealing procedure provided a slight decrease in the contact resistivity, which is associated with the Ge transport to the PdGe-GaAs interface. Although a good ohmic contact can be obtained when PdGe is in direct contact with the GaAs substrate (as the Ge/PdGe/GaAs configuration presented in Fig. 5.6), the optimal electrical properties were attained after Ge solid phase epitaxial (SPE) growth took place, as demonstrated by Fig. 5.7.

These findings suggest the Ge transport to the GaAs interface is not essential for the ohmic behavior of the contact, nevertheless, the growth of the epitaxial Ge on to GaAs lowers the resistivity and optimizes the ohmic contact. These results suggest that two different interfacial microstructural configurations (Ge/PdGe/GaAs and PdGe/epi-Ge/GaAs) provided ohmic contacts with close resistivity values, which implies that at least two different charge transport mechanisms could occur. This experimental evidence and the work of others on this ohmic contact make it difficult to establish a model that would explain the charge transport across the interface. In order to propose a charge transport mechanism across the interface one has to consider the evidence provided by Marshall et al. <sup>2</sup> which showed that GaAs solid phase regrowth (SPR) takes place subsequently to the  $\text{Pd}_x\text{GaAs}$  decomposition. This would create a PdGe/epi-Ge/ $n^{++}$ -GaAs/GaAs structure and the electrical charges would tunnel through the thin Ge doped GaAs regrown layer. Even though this model seems to be the most accepted one, there are still some unanswered questions in regard to the exact role played by the Ge epitaxial layer. If the GaAs SPR combined with the Ge doping of this layer could account for the ohmic behavior at the Ge/GaAs interface, there is no explanation for the charge transport at the PdGe/Ge interface. A study <sup>3</sup> of the metal contacts to Ge substrates revealed a 0.61eV Schottky-barrier height at the PdGe/Ge interface. If this barrier height were still present at the PdGe/Ge interface as part of the PdGe/epi-Ge/ $n^{++}$ -GaAs/GaAs structure, the contact would not be ohmic, unless a high level doping would be present in the Ge

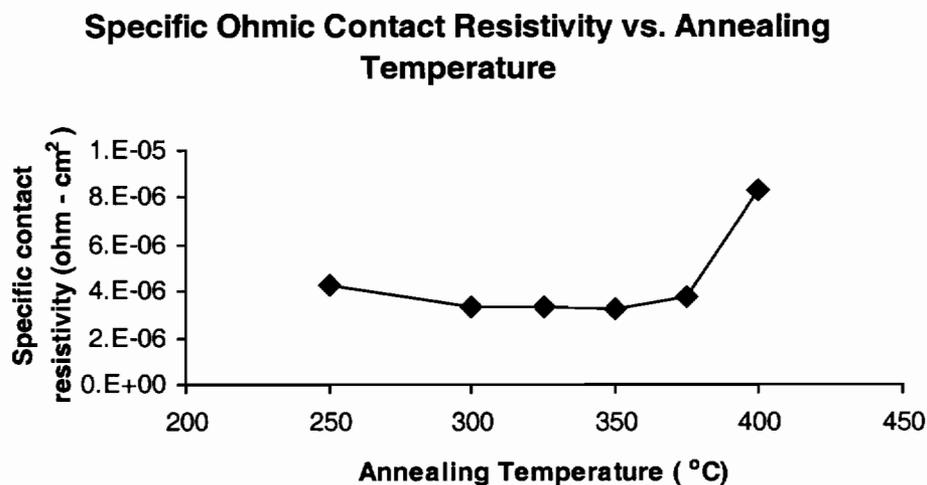
epitaxial layer. However, there is no evidence presented in the literature that indicates the nature of such doping. In fact, most of the studies performed on this contact are lacking a complete treatment of the electronic nature of the PdGe/epi-Ge/GaAs system that would include the PdGe/Ge interface.

The TLM measurements showed new evidence that PdGe in direct contact with the GaAs could form an ohmic contact with a relatively low resistivity. However, the presence of the epitaxial Ge layer at the interface provides the GaAs ohmic contact with minimum resistivity. Although, this study shows the importance of the Ge/GaAs interface for a good ohmic contact behavior, a model that would explain the charge transport mechanism across the ohmic contact was difficult to establish.

The key element in obtaining a good ohmic contact is the Ge transport to the interface with GaAs. Two competing reactions that consume the initial amorphous Ge layer and affect the integrity of the Ge epitaxial layer were found. One is the solid state phase transformation from Pd<sub>2</sub>Ge to PdGe and the other is Ge crystallization by solid state epitaxy on GaAs. Knowing how to control each of them is necessary in order to design better annealing processes which would produce a more stable structure with lower ohmic contact resistivity.

## **7.2 Isochronal Annealing Experiments**

In order to develop a fabrication process for reproducible, low resistance ohmic contacts, one should focus on the parameters in that process that affect the microstructure at the metal/GaAs interface and one such parameter is the annealing temperature. In this set of experiments, microstructure analysis and contact resistance measurements of isochronally annealed Pd-Ge contacts to GaAs were performed. The TLM measurements presented in the previous section demonstrated that annealing temperatures greater than



**Figure 7.1. Specific contact resistivities as a function of annealing temperature. The annealing time was 5 min. for all specimens**

214 °C are needed for the onset of the ohmic behavior of the contact. In this section, evaporated Pd/Ge/Pd thin film stacks on GaAs were subjected to isochronal annealing at temperatures between 250 °C to 400 °C, where the ohmic behavior was noticed. The characteristics of the ideal Pd-Ge ohmic contact on GaAs were established by correlating their electrical performance with cross-sectional transmission electron microscopy (XTEM) images.

Typical TEM cross-sectional specimen preparation techniques limit the electron transparent area and make the global characterization of the contact difficult. The XTEM sample preparation was performed by using a Focused Ion Beam (FIB) method that permitted observation of a minimum of 4 μm of the interface cross section in each of the specimens examined. This made it possible to study the full microstructural impact on the electrical performance of the contact and provide some new evidence concerning the importance of the Ge/GaAs interface in the charge transport mechanism. Heating the samples was performed under forming gas atmosphere that consisted of 4%H<sub>2</sub>-96%N<sub>2</sub> and the contact resistances were then measured by an automatic tester using the TLM

method, providing a direct link between the microstructure and the electrical properties of the contacts.

The samples were annealed by using a ramp rate of 2 °C/sec. and holding for 5 minutes at temperatures ranging from 250 °C to 400 °C. Fig. 7.1 shows the variation of the specific contact resistivity with the annealing temperature. This “U” shape type of variation is similar with ones determined for other metal/GaAs ohmic contact systems<sup>4,5,6</sup>. The minimum specific ohmic contact resistivity was obtained in the 300 °C to 350 °C annealing temperature range.

In chapter 5, it was shown that, at 250 °C, the Pd<sub>2</sub>Ge phase formation consumed all the Pd. At temperatures higher than 250 °C there are three solid state reactions that are essential in the ohmic contact formation:

1. Pd<sub>2</sub>Ge phase transformation to PdGe
2. Ge crystallization as a solid state epitaxial layer on GaAs or as a polycrystalline phase between the PdGe layers
3. Ternary Pd<sub>x</sub>GaAs<sup>1</sup> phase decomposition

The first and second reactions are competitive as they both consume the amorphous Ge (a-Ge) and they take place in the same temperature range. Two possible mechanisms could lead to Ge crystallization. One is nucleation and growth of multiple grains between the two PdGe layers or, if the annealing time is increased, Ge crystallizes through a solid state epitaxial growth mechanism. The third reaction unfolds before Ge solid state epitaxial growth would take place, this way creating a clean GaAs surface, ideal for the Ge epitaxy. Another mechanism that may contribute to the Ge SPE growth was described in chapter 6 and is based on the tensile stress induced by the presence of the PdGe layer.

Fig. 7. 2 shows the microstructure that resulted from annealing at 250 °C for 5 min. Poly-crystalline PdGe compound is the predominant phase present and resembles a columnar grain structure. The average PdGe grain size measured on a direction parallel to the substrate interface is 75.5 nm. At higher annealing temperatures, PdGe grain coarsening takes place, which would produce equiaxially shaped grains. The STEM /EDX analysis identified some Ge pockets “trapped” between the PdGe compound layers and

the amount of Ge transported to the GaAs interface is relatively low due to the small diffusion coefficients associated with this annealing temperature. However, the Ge epitaxial layer, with an average thickness of 16.6 nm, covers 93% of the interface with the GaAs substrate. The remaining 7% of the interface represents the area where PdGe is in direct contact with the substrate.

The characteristics of the ohmic contact microstructure resulted from annealing to 300 °C for 5 min. are presented in Fig. 7.3. More Ge was transported to the GaAs interface, which resulted in a Ge epitaxial layer with an average thickness of 26.1 nm. Moreover, this epitaxial Ge covered a higher percentage of the GaAs interface, 97.8%. The PdGe grains exhibit the same columnar feature as the ones resulted from annealing to 250 °C. In particular, the average PdGe grain size in the direction parallel to the substrate interface is 76.8 nm, not significantly different than the previous annealing temperature.

The micrograph presented in Fig. 7.4 represents the ohmic contact microstructure that evolved from annealing at 350 °C for 5 min. In this case, the average thickness of the Ge epitaxial layer is 31 nm and its substrate coverage extends to 98.5% of the substrate interface. The PdGe grains lost their columnar feature and a certain degree of coarsening took place at this annealing temperature. In fact, the average grain size in the direction parallel to the GaAs interface is 84 nm, an increase from the grain size given by annealing at 300 °C.

Fig. 7.5 reveals the features of the ohmic contact thin film system after annealing at 375 °C for 5 min. The Ge epitaxial layer exhibits a slight increase in the average thickness (to about 32 nm) and some degree of islanding which increases the percentage of PdGe in direct contact with GaAs to 7 % (or 93% Ge in contact with the substrate). Moreover, some stacking faults along the [111] plane could be noticed in this Ge layer as indicated by the arrows in Fig. 7.5. The effect of the PdGe grain coarsening increased as the average grain size along the GaAs surface is 87 nm.

By raising the annealing temperature to 400 °C, one notices the degradation in the Ge epitaxial layer as the islanding effect is more evident and the stacking fault density increases. An area with a high density of stacking faults is indicated by the arrow in

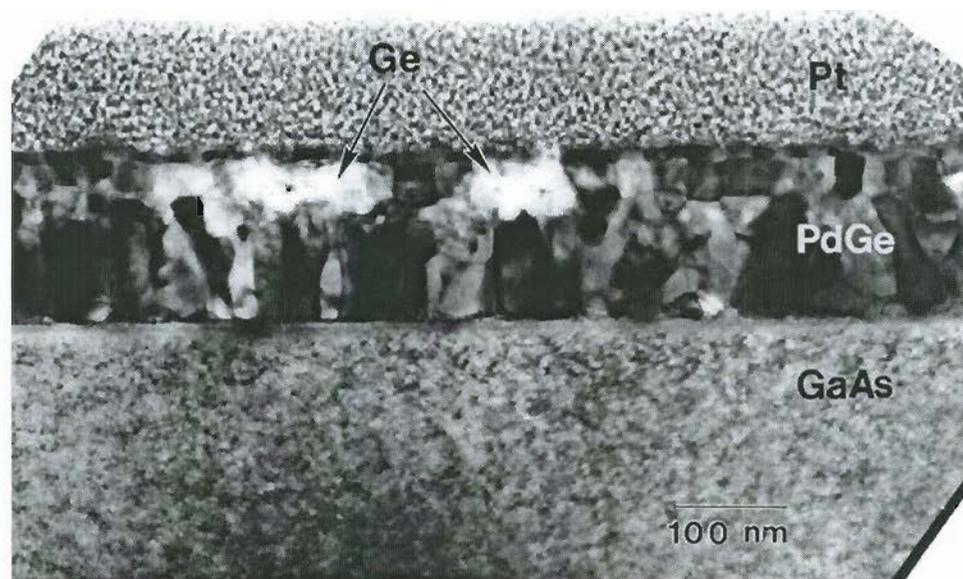


Figure 7.2. Cross-sectional micrograph of a sample annealed at 250 °C for 5 min. Part of Ge that was not transported to the GaAs interface remained trapped between the PdGe layers.

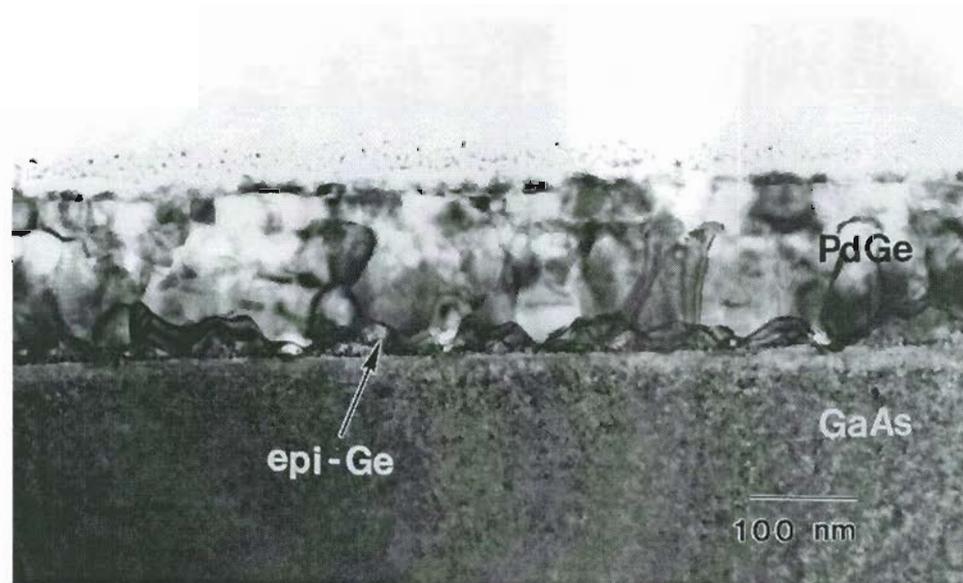


Figure 7.3. Cross-sectional micrograph of a sample annealed at 300 °C for 5 min.

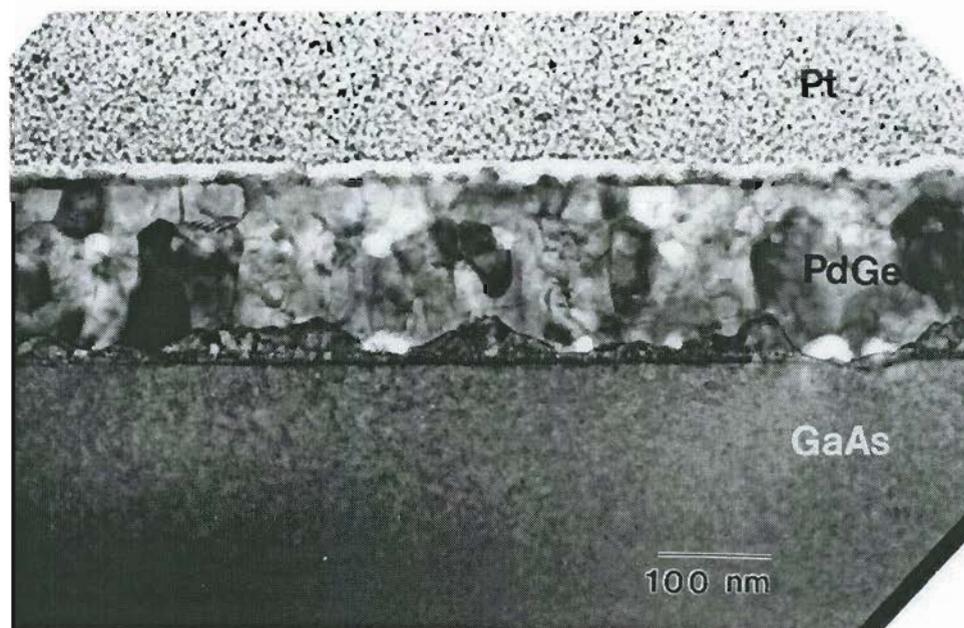


Figure 7.4. Cross-sectional micrograph of a sample annealed at 350 °C for 5 min.

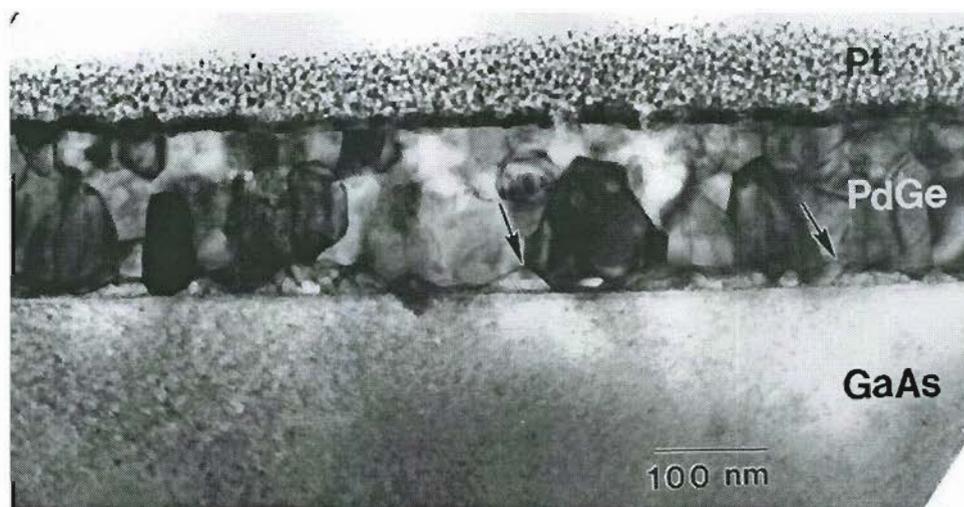
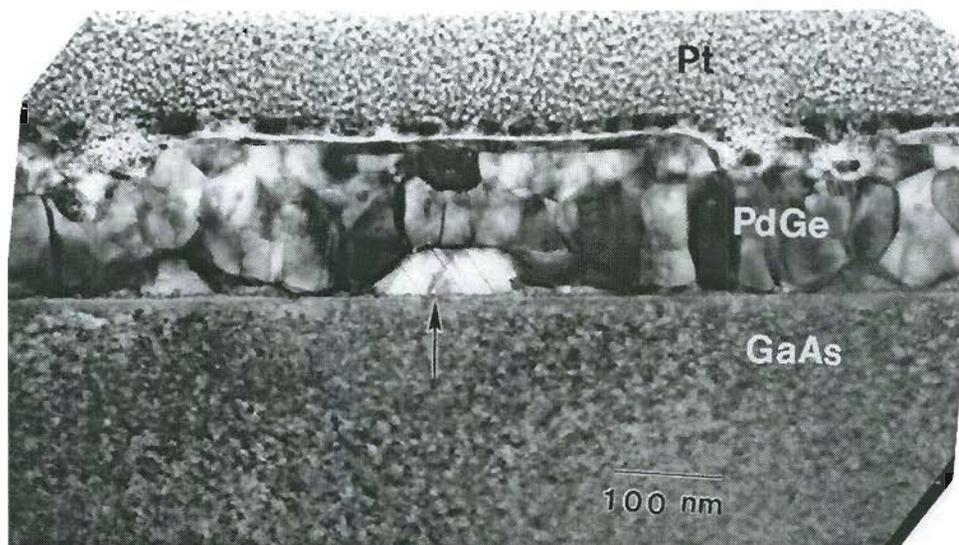


Figure 7.5. Cross-sectional image of a sample annealed at 375 °C for 5 min. The arrows indicate stacking faults present in the Ge epitaxial layer.

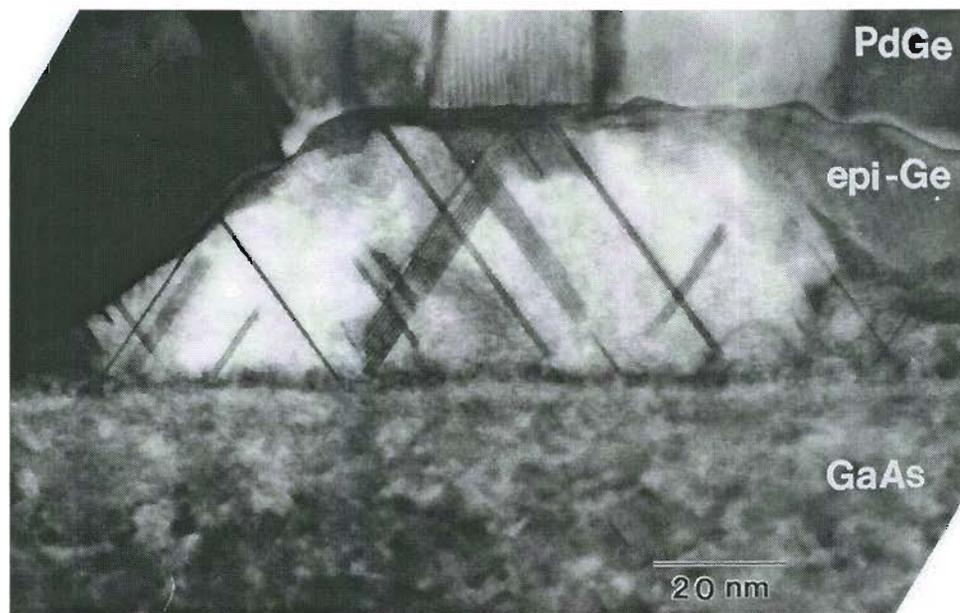
Fig. 7.6(a). Figure 6(b) shows a higher magnification of this feature. The epitaxial Ge in contact with the GaAs substrate is reduced to 90.5% of the interface and the average Ge thickness is 32.3 nm. Further PdGe grain growth took place laterally, along the GaAs interface, and the average grain size in this direction is 90.2 nm.

The differential scanning calorimetry (DSC) experiments described in chapter 5 demonstrated that two solid state reactions take place in the final stages of the ohmic contact formation when the contact is annealed at temperatures between 250 °C to 400 °C. One is Pd<sub>2</sub>Ge transformation to PdGe and the other is Ge crystallization. They are competitive reactions as they both consume a-Ge but the former one dominates at lower temperatures (its peak was measured by DSC to be 269 °C) and the latter one prevails at higher temperatures (DSC peak temperature measured at 322 °C). In that case, the annealing temperature actually determines which reaction will prevail. At 250 °C, PdGe nucleation and growth predominate, which lead to large PdGe grains before the Ge transport to the GaAs interface takes place. This way, the Ge epitaxial growth is limited due to the reduced density of grain boundaries – fast diffusion paths through the PdGe layer- and due to the relatively low temperature diffusivity. These two effects, large PdGe grains and small diffusion coefficients associated with the low annealing temperature, influence the Ge transport to the GaAs interface. Ge “trapped” in between the PdGe layers could be noticed in Fig. 7.2 as identified by EDX analysis. Annealing at higher temperatures, 300 °C and 350 °C, appears to provide the right balance between the kinetics of the two solid state reactions described above. In this way, sufficient Ge is transported to the substrate interface before the PdGe grains size increase and grain boundaries density reduction occurs. Higher annealing temperatures, 375 °C and 400 °C, provide the appropriate conditions for Ge transport to the interface, however the integrity of the Ge epitaxial layer suffers as the critical thickness is reached. Fig. 7.6 provides evidence for 3D islanding and stacking fault formation along the [111] planes.

A large number of studies<sup>7</sup> performed on thin film formation on a substrate indicate three basic growth modes: Frank – van der Merwe or layer-by-layer



a.



b.

Figure 7.6. a) Cross-sectional micrograph of a sample annealed at 400 °C for 5 min. The arrow points to an area with high density of stacking faults in the Ge layer b) Magnified view of the stacking faults along the [111] planes in the Ge epitaxial layer.

Volmer-Weber or island and Stranski-Krastanov which are illustrated in Fig. 7.7. The layer growth generally produces planar epitaxial structures especially when the substrate and film both have the same crystal configuration. In the opposite case, the island growth occurs when the film material nucleates on the substrate and grows in three dimensions to form islands. Stranski-Krastanov growth combines the layer and the island modes. This mode starts with a layer-by-layer growth and then, as the interaction between the deposited atoms and the substrate weakens, continues with the island growth. Although some of the aspects of the thin film growth mechanisms are not yet completely understood, the three modes described above can be rationalized by using a very simple thermodynamic model. As illustrated in Fig. 7.8, at equilibrium, the surface tensions at the interface should satisfy the following relationship:

$$\gamma_{sm} = \gamma_{sf} + \gamma_{fm} \cdot \cos \alpha$$

where:

$\gamma_{sm}$  is the surface tension at the interface between the substrate and the surrounding medium,  $\gamma_{fm}$  is the surface tension at the interface between the film and the surrounding medium,  $\gamma_{sf}$  is the surface tension at the substrate-film interface and  $\alpha$  is the contact angle. For island growth,  $\alpha < 0$  and then:

$$\gamma_{sm} < \gamma_{sf} + \gamma_{fm}$$

For layer-by-layer growth, the film “wets” the substrate and  $\alpha = 0$ , then:

$$\gamma_{sm} = \gamma_{sf} + \gamma_{fm}$$

For Stranski-Krastanov growth,

$$\gamma_{sm} > \gamma_{sf} + \gamma_{fm}$$

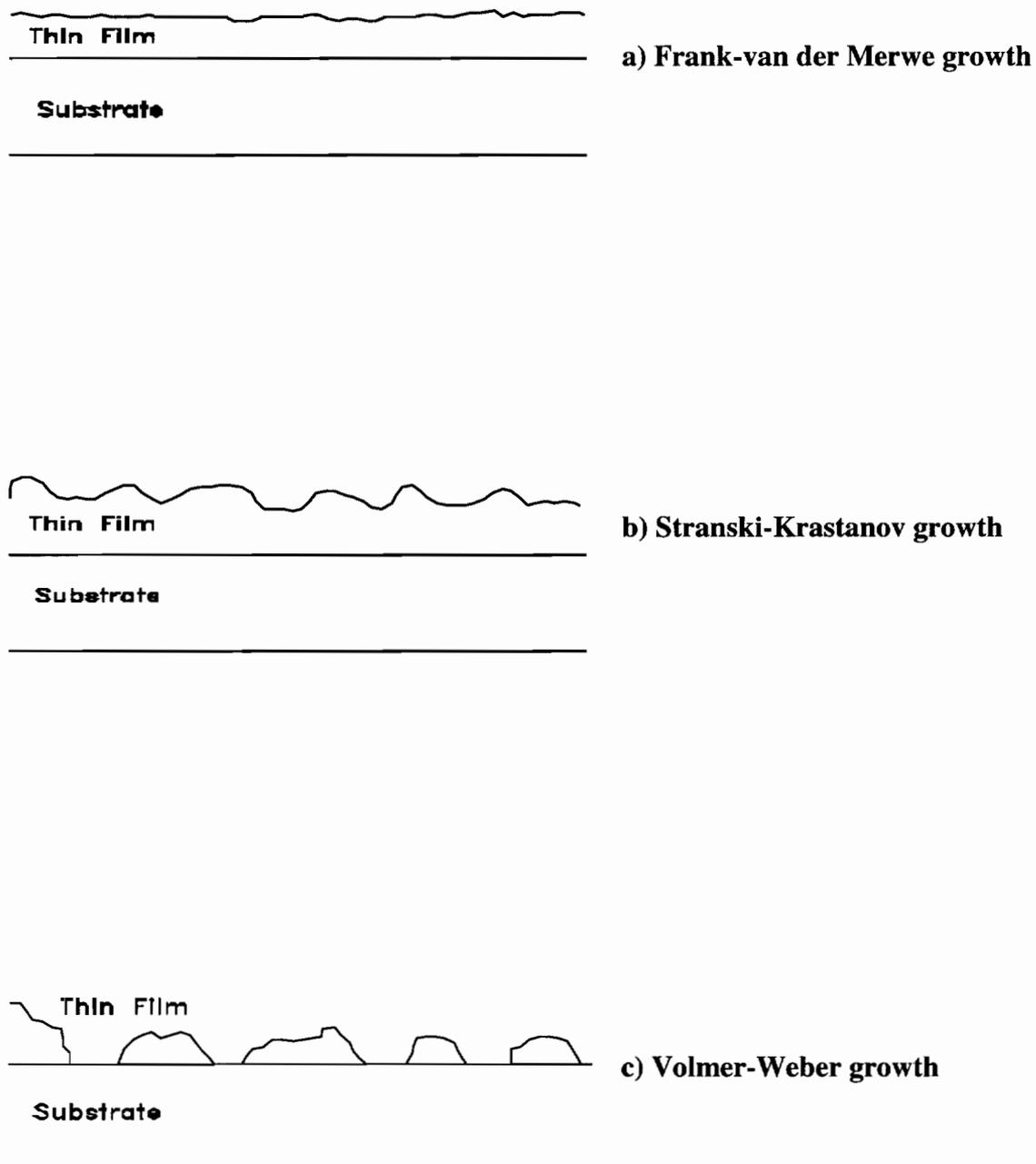
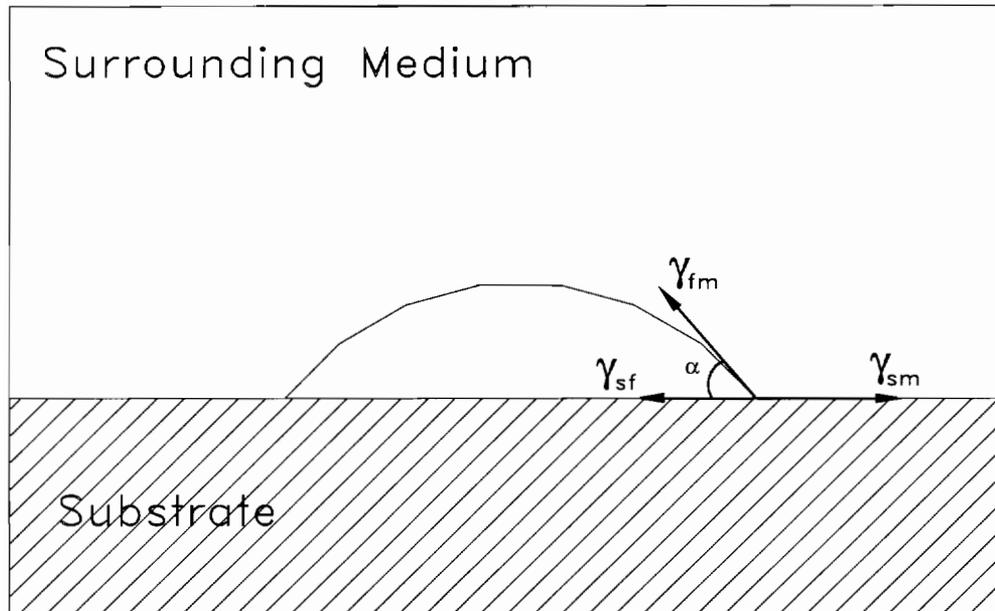


Figure 7.7. Three basic thin film growth modes on a substrate. a) Frank-van der Merwe or layer-by-layer growth mode, b) Stranski-Krastanov mode and c) Volmer-Weber or island growth mode.



**Figure 7.8. Surface tension equilibrium at the thin film-substrate interface.**

The growth mode and the thermodynamic analysis presented above assume an uniform and isotropic surrounding medium. That's why this type of analysis was usually employed in situations where the surrounding medium was a vapor phase or vacuum. The same definitions that describe the three growth modes could be extended to cases where the surrounding medium is a solid phase and, clearly, the SPE growth with transport medium represents such a case. However, when the transport medium is a poly-crystalline phase, the assumptions of uniformity and isotropy do not hold, therefore, the thermodynamic equilibrium at the interface would be described by more complex equations. Nevertheless, the nomenclature related to the growth modes defined earlier, could still be used in analyzing the PdGe mediated Ge SPE growth on GaAs.

Various microstructural parameters were measured from TEM images in addition to the ones presented in Fig. 7.2 through 7.6. At least 4  $\mu\text{m}$  of the contact cross-sectional length was analyzed in each specimen, and a summary is presented in Table 7-II.

**Table 7-II. Microstructural parameters and specific contact resistivity as a function of annealing temperature. The average values were determined by observing a minimum of 4  $\mu\text{m}$  in each specimen.**

Annealing temperature (°C)	Average PdGe grain size (nm)	Epitaxial Ge average thickness (nm)	Epitaxial Ge interface coverage ( % )	Specific contact resistivity ( $\Omega\text{-cm}^2 * 10^{-6}$ )
250	75.5	16.6	93.2	4.25
300	76.8	26.1	97.8	3.32
350	83.9	30.9	98.5	3.29
375	86.8	31.8	92.7	3.77
400	90.2	32.3	90.5	8.28

The PdGe grain size in the direction parallel to the GaAs surface grows with increasing annealing temperature. Another measured parameter that increases with annealing temperature is the average thickness of the Ge epitaxial layer whose role in the charge transport mechanism is still surrounded by controversy. The focal point of the argument is whether the ohmic behavior of the contact can be explained by an enhanced Ge doping of the regrown GaAs – the doping model – and/or by As doping of the Ge epitaxially grown layer – the heterojunction model. According to the results presented in Table I, it can be noticed that one parameter that correlates well with the electrical performance of the contact is the Ge coverage of the GaAs interface. The best ohmic contacts were formed by annealing between 300 °C and 350 °C, which resulted in about 98% Ge coverage of the GaAs interface. It appears that less epitaxial Ge in direct contact with the substrate may be detrimental to the specific ohmic contact resistivity. However, it was shown in the previous section of this chapter that the presence of PdGe at the GaAs surface still renders an ohmic contact with good ohmic contact. This implies that conduction occurs in both areas where Ge or PdGe is in direct contact with the GaAs, even though the PdGe/epi-Ge/GaAs configuration seems to be the optimal contact microstructure. Based on the electrical data presented in this section, one can notice the large processing window of this Pd-Ge ohmic contact as annealing temperatures from 250 °C through 375 °C provided ohmic contacts with relatively low resistivity. This behavior can be very well justified by the fact that two microstructural configurations Ge/PdGe/GaAs and PdGe/epi-Ge/GaAs formed low resistivity ohmic contacts.

The electrical measurements presented in this chapter in conjunction with the TEM studies for both constant heating rate and isochronal experiments, indicated that the optimal ohmic contact is given by the PdGe/epi-Ge/GaAs arrangement. In other words, the larger epi-Ge interface coverage, the lower the ohmic contact resistivity is. However, a discrepancy can be noticed in regard with the Ge coverage of the sample annealed at 250 °C when compared with the one annealed at 375 °C. The resistivity of the samples annealed at 375 °C are lower than the ones of the samples annealed at 250 °C even though their GaAs interface is covered with less epitaxial Ge. Another surprising result is the

close resistivity values between the samples quenched from 322 °C (see section 7.1) and the ones that were held at 250 °C for 5 min. Figure 5.6 showed that no observable Ge was transported to the GaAs interface whereas in Fig. 7.2 some epitaxial Ge can be noticed between GaAs and the PdGe layer.

This anomaly could be attributed to the difference in the Ge layer thickness although a clear proof to support this argument could not be established. In determining the electrical properties of these contacts, previous studies<sup>8</sup> suggested tunneling is the dominant charge transport mechanism. If the tunneling effect takes place across the epi-Ge layer, then different epi-Ge thicknesses would affect the charge current flow as the areas with a thinner Ge layer would exhibit less contact resistance.

In the case of the sample annealed at 400 °C, the sharp increase in contact resistivity represents the onset of another degrading mechanism, which cannot be explained only by the Ge coverage of the GaAs interface. Fig. 7.6 revealed the presence of stacking faults in the Ge epitaxial layer which were hardly noticed in the sample annealed at 375 °C (see Fig. 7.5) and were not found at all in the samples annealed at lower temperatures. Therefore, besides the epitaxial Ge coverage of the interface, its crystallinity is also important.

The evidence showed in this section proves the Ge epitaxial layer plays an important role in the charge transport mechanism across the contact. However, it was also demonstrated that the presence of PdGe at the GaAs interface provides a good ohmic contact structure and it may explain the large processing window exhibited by these contacts.

Microstructure analysis and contact resistance measurements were carried out for the Pd-Ge ohmic contact system on GaAs. The specific contact resistivity was found to be influenced by the epitaxial Ge layer coverage of the GaAs interface and by its crystalline integrity. Although, this study shows the importance of the Ge/GaAs interface for a good ohmic contact behavior and supports the heterojunction model, there is not enough evidence to rule out the doping model. This debate will not be concluded as long as we

are lacking convenient analytical methods necessary to characterize the interfacial microstructure at atomic resolution.

Also, a new argument was made in explaining the specific contact resistivity “U” shape dependence on the annealing temperature. In case of the lower annealing temperature, insufficient Ge present at the interface limits the coverage of the substrate whereas the higher annealing temperatures provide enough Ge transport but the GaAs coverage is poor due to the Ge island formation. At high annealing temperatures, Ge forms islands that characterize the Volmer-Weber type of growth as demonstrated in Fig. 7.6 for a 400 °C anneal. The best ohmic contact resistivity is obtained when the Ge epitaxial layer growth follows the Stranski-Krastanov mode. Epitaxial thin films formed this way start with a layer-by-layer type of growth and then, beyond a critical thickness, the island formation takes place. This study showed that Stranski-Krastanov epitaxial Ge thin film growth occurs when annealing is performed between 300 °C and 350 °C, which resulted in maximum Ge coverage of the GaAs interface.

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## 8. Summary and Future Work

In order to fabricate improved GaAs devices, new materials need to be explored for the ohmic contact structures. A wide variety of ohmic contact materials were investigated in the past but the Ge-based alloys seemed to be the most successful ones. In particular, the Au-Ni-Ge alloy was at the center of the GaAs ohmic contact technology for the last three decades. One of the major disadvantages of this contact is the low temperature melting point associated with it, which is given by the Au-Ge eutectic mixture. It became clear that, during the annealing step, an improved alloy would react in solid state only, without melting, and one such contact proved to be the Pd-Ge thin film system. The purpose of this thesis was to perform an analysis of the mechanisms that contribute to (or hinder) the formation of the Pd-Ge ohmic contact.

This thesis described the microstructure evolution of this ohmic contact alloy and showed how the various phases and interface morphologies correlate with the electrical properties of the contact. Chapter 2 treated several theoretical aspects of the metal/compound semiconductor interface that included microstructural (e.g. phase formation sequence, interface morphology, phase equilibria) and electrical (such as the basic charge transport mechanisms) considerations. Chapter 3 presented a literature review of various topics considered necessary in understanding the ohmic contacts to semiconductors. Along these lines, the Schottky barrier formation models, ohmic metallization schemes to GaAs, the phenomena of solid phase epitaxy (SPE) and solid phase regrowth (SPR) were discussed. Also, the most common applications to electronic devices were presented. Chapter 4 described the experimental techniques employed in this research. In chapter 5, the phase formation sequence of the Pd/Ge/Pd thin film system on GaAs during annealing was analyzed. The effects of tensile stress on the Ge SPE

growth were studied in chapter 6 whereas the correlation between the electrical properties and the microstructure of the contact was done in chapter 7.

Numerous attempts were made in the past to develop new ohmic contact metallizations on GaAs<sup>1</sup>. In spite of this great research effort, a clear materials selection procedure does not seem to be followed and the choice of elements present in the metallization alloys appears to be arbitrary. The Pd-Ge ohmic contact to GaAs belongs to a new category of metallization schemes that rely on the formation of an epitaxial heterostructure at the metal/semiconductor interface. Chapter 3 introduced the concept of solid phase epitaxy (SPE) and solid phase regrowth (SPR) and described the way one could use these two mechanisms to design new contact metallization alloys. This led to a framework for the materials selection needed in order to design a SPR and/or SPE-based ohmic contact to GaAs, which could be further extended to other compound semiconductors. The principles derived from this analysis provided a rationale for the choice of the Pd-Ge solid state ohmic contact system as a replacement for the Au-Ni-Ge. By following the same materials selection criteria for an SPE/SPR-based contact, one could find other candidate systems such as Ni-Ge. This alloy received some attention in the literature but produced very mixed results so far, probably due to the fact that Ni consumes a greater amount of GaAs than Pd during the initial stages of ohmic contact formation. Further research could find ways of limiting this interaction (e.g. depositing less Ni in direct contact with GaAs) which may lead to a more thermally stable contact. Also, other solid state reactions (e.g. dissolution-precipitation) aside from the ternary compound formation-decomposition may lead to the SPR of GaAs. By exploring materials that would dissolve both Ga and As uniformly, one may extend the choices of possible SPR-based contacts to GaAs.

The phase formation sequence of the Pd/Ge/Pd/GaAs system was studied in chapter 5. By combining analytical TEM with thermal analysis, the solid state transition temperatures were accurately determined. The microstructure evolution and the corresponding solid state reactions that take place during the formation of the Pd-Ge ohmic contacts on GaAs were studied using constant-heating-rate differential calorimetry

(DSC) and cross-sectional TEM. Specimens heated at temperatures that coincided with the DSC peaks were quenched in a He atmosphere and the resulting microstructure was characterized by TEM. The variable constant-heating-rate DSC experiments led to the activation energy values associated with each solid state reaction. As an extension to this study, in the second part of chapter 5, the phase formation sequence and the evolution of the microstructure were studied by in-situ TEM annealing. These experiments provided a continuous record of the phase transitions that take place during ohmic contact formation. A novel temperature calibration technique, which relied on DSC to correct the temperature readout, was presented. Measuring the temperature is an inherent problem for any in-situ TEM experiment and this technique could be used successfully in analyzing other systems. From a technological point of view, the results presented in this chapter showed that at temperatures higher than 250 °C there are three solid state reactions that are essential in the ohmic contact formation:

1. Pd<sub>2</sub>Ge phase transformation to PdGe
2. Ge crystallization as a solid state epitaxial layer on GaAs
3. Ternary Pd<sub>x</sub>GaAs phase decomposition

Based on the thermal analysis and in-situ TEM observations, the kinetic parameters of both germanide phases were determined. It was shown that their growth is described by the following relationships:

$$X^2 = 2.94 \cdot 10^{15} \cdot e^{-0.98\text{eV}/kT} \cdot t \quad \text{for the Pd}_2\text{Ge growth and}$$

$$X^2 = 6.89 \cdot 10^{17} \cdot e^{-1.28\text{eV}/kT} \cdot t \quad \text{for the PdGe growth,}$$

where X is the thickness in angstroms, T is the temperature in °K, k is the Boltzmann constant and t is the time measured in minutes. These equations represent complete solutions to the growth kinetics of these two phases. As a result, it will be possible to model the formation of this ohmic contact with “Virtual Fab” type of software tools (e.g. Silvaco’s Athena). This will increase the flexibility of a modern fabrication line in regard

with changing the annealing process. For example, quite often in a lift-off patterning step it is necessary to change the thickness of the contact which implies that new annealing parameters would need to be established. By knowing the kinetics of the reactions that lead to a good contact, one would avoid the expenses of these experimental evaluations.

The work presented in chapter 6 examined the residual stress associated with the microstructure present in the final stages of the Pd-Ge ohmic contact formation. These results indicated that Ge solid phase epitaxial growth on to GaAs was strongly affected by the tensile stress set in the thin film system. These findings suggest that tensile stress may be an important ingredient in the SPE growth and the intermediate layer may play a physical role rather than a chemical one. From a technological perspective, these results may lead to new methods of using controlled stress in engineering novel SPE systems. Moreover, it was shown in past studies that the role of stress could also be extended to modifying the electrical properties of the heterostructure (e.g. energy bandgap structure). Future thin film stress studies should be motivated by the fact that inducing controlled stress at an interface is a relatively trivial technological matter. Consistent amount of stress could be induced by depositing materials on either side of the wafer provided the new elements would not chemically disturb the ohmic contact formation. Modeling the thin film stress reached scientific maturity to some extent but several issues still need to be studied further. One of these issues is measuring the stress present in patterned device structures as opposed to uniformly deposited blanket thin films. Although the use of lithographically defined micro-cantilever beam bending techniques for stress measurements was previously reported, chapter 6 demonstrated a new and more flexible method of fabrication based on FIB milling.

The effect microstructure has on the electrical performance of the contact was studied in chapter 7. In the first part of the chapter, specific ohmic contact measurements were performed in relation to the microstructural evolution observed in chapter 5. Then, the focus shifted towards the final stages of the ohmic contact formation. Isochronal annealing experiments at temperatures that correspond to the start of the ohmic behavior were performed and, once again, the microstructure information was correlated with the

contact resistivity data. For the Pd/Ge thickness ratio employed in this study, it was determined that the lowest ohmic contact resistivities were obtained after annealing for 5 minutes at temperatures between 300 °C and 350 °C. It also was shown that PdGe in direct contact with GaAs could contribute to the formation of a low resistivity ohmic contact. This is a new element that needs to be considered when describing the charge transport mechanisms across the interface. However, the minimum contact resistivity was obtained after Ge SPE growth took place and this result is somewhat consistent with previous studies. Based on this evidence, it was concluded that at least two charge transport mechanisms contribute to the low resistivity of the contact as given by a-Ge/PdGe/GaAs and PdGe/epi-Ge/GaAs microstructural configurations. In the first case, the contact would conduct through a low Schottky barrier interface given by the PdGe/GaAs heterostructure. For the second case, it was shown that the epi-Ge/GaAs interface is also a low barrier height interface <sup>2</sup> (approx. 60 mV) and, since considerable Ga outdiffusion was demonstrated to occur, one can assume that excess As at the interface could increase the tunneling probability by providing a heavily n-doped epi-Ge layer. In fact, for the first microstructural configuration case given by a-Ge/PdGe/GaAs one could argue that a few monolayers of Ge could be present between PdGe and GaAs so the tunneling mechanism would be responsible for the low contact resistivity but there was no analytical evidence to support this view. However, this hypothesis may have its merit since the size of the Ge monolayers necessary for tunneling to take place is smaller than the resolution limit of the analytical instruments employed.

Another view that needs to be explored when proposing a charge transport mechanism across this contact is the role played by the GaAs solid phase regrowth (SPR). This would create a PdGe/epi-Ge/n-doped regrown GaAs/GaAs configuration which, would conduct through tunneling set by the highly doped thin GaAs regrown layer. Although the experimental evidence for SPR in the Pd-Ge contacts is not very clear, this seems to be the most accepted model. In this thesis, no evidence for GaAs SPR was found but the analytical resolution limits and the lack of substrates with a buried marker structure made it difficult to observe this reaction. In chapter 5 it was shown that during

annealing of the contact, no more than 8-nm ternary compound was detected at the Pd-GaAs interface. The decomposition of this phase would render only a very small amount of GaAs for SPR, which would be difficult to measure. Furthermore, previous studies showed that considerable Ga outdiffusion takes place during annealing, which would imply that even less GaAs material would be available for regrowth.

Although the presence of PdGe at the interface with GaAs does not seem to damage the electrical properties of the contact, the evidence presented in this chapter showed that the SPE growth of Ge on to GaAs provided the lowest resistivity interface. Based on the measurements of the Ge coverage of the interface, a new argument was made in explaining the specific contact resistivity “U” shape dependence on the annealing temperature. In the case of the lower annealing temperature, insufficient Ge present at the interface limits the coverage of the substrate whereas the higher annealing temperatures provide enough Ge transport but the GaAs coverage is poor due to the Ge island formation.

The analysis presented in this thesis reveals the importance of the epi-Ge/GaAs interface for a good ohmic contact behavior and to a certain degree supports the heterojunction model. However, the significance of the possible GaAs SPR and the possible implications of this mechanism in establishing a charge transport mechanism across the contact could not be determined. Based on the work presented in this thesis only, there is not enough evidence to rule out the doping model. This debate will not be concluded as long as we are lacking convenient analytical methods necessary to characterize the interfacial microstructure at atomic resolution. It is expected that new developments in high resolution quantitative TEM or other analytical instruments may answer these questions in the future.

For future work, there are a number of areas to be investigated. For SPE and SPR phenomena, it would be appealing to investigate the possibility of applying the materials selection criteria presented in chapter 3 to other semiconductor compound materials of great interest today, such as InP, GaN or CdZnTe. Also, more studies of the Ni-Ge or Ni-Pd-Ge ohmic contacts on to GaAs would probably produce more insights into the SPE

and SPR phenomena and hopefully extend the choice of contact materials. Another area of future research would be the study of the role of stress in the thin film solid state reactions and also its effects on the electrical properties of the interfaces. The possibility of using stress to control the final microstructure of a contact would be very appealing and more studies in this direction would be beneficial not only for compound semiconductor industry but for the Si-based technology also. Research work in all these areas should contribute to a deeper understanding of the metal-semiconductor interface phenomena.

## References

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