NUMERICAL SIMULATION OF CTE MISMATCH AND THERMAL-STRUCTURAL STRESSES IN THE DESIGN OF INTERCONNECTS

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A dissertation presented to the faculty of the
OGI School of Science and Engineering at OHSU
In partial fulfillment of the requirements for the degree of
Doctor of Philosophy
In Materials Science and Engineering

July, 2001

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ACKNOWLEDGEMENTS

I would like to acknowledge the support, supervision, guidance, and encouragement of my advisor, Dr. Milton Scholl. I would like to thank him specially for taking me as a long distance student living in the East Coast, for the latter half of this project.

Many thanks are also due to Dr. Lemmy Meekisho, for his patient supervision and valuable suggestions given to me both as my initial advisor and as my thesis committee member. I also greatly appreciate the time and effort of my thesis committee members, Dr. Anthony Bell, Dr. Jack McCarthy, and Dr. Lemmy Meekisho. I thank all of them for reviewing this dissertation and for the valuable suggestions they made.

I am also grateful to Mr. Jorge Ivaldi, my supervisor at ASML, for encouragement and his unconditional commitment to see me complete this dissertation. Without Mr. Ivaldi's support I would have never completed this dissertation. I also thank ASML for their financial support and time off from work given to visit OGI to complete this project.

I would also like to extend my thanks and appreciation to Ms. Julianne Williams and other librarians at OGI School of Science and Engineering at OHSU for their help with the references and for getting this dissertation in compliance with required specifications.

Finally I would like to thank my friend Ms. Lenka Casey for her understanding, encouragement and support during periods of discouragement to make this project a success.

DEDICATION

Dedicated to my late parents,

Rose Yesudial Peter

And

Gurubatham Selvaraj Peter

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PREFACE

The objective of this dissertation was to show by mathematical modeling the reduction in thermal stress obtained by inserting a wire bundle (wire interconnect) between the chip and the board, instead of soldering the chip directly to the board (solder interconnect). Thermal stresses are created due to the mismatch in coefficient of thermal expansion (CTE) between the chip, board, solder joint and lead wires. This approach is based on the fact that each wire or fiber has a very small contact with the chip. Hence with the chip having a very small CTE, each fiber will separate at the chip, reducing the stress on the chip.

When a system containing chips soldered directly to the circuit board are cycled on and off causing cyclic stress, minute fractures are initiated and the module is prone to fatigue failure. Vibration analysis (fatigue failure analysis) was performed to show the reduction in stress in the wire interconnect compared to solder interconnect.

To emphasize the practical aspects and the potential of wire bundle interconnects, a non-functioning interconnect was made. To validate the mathematical model, the solder interconnect results were compared with the published results of other researchers. In addition the results obtained for the solder interconnect using the ANSYS program was cross checked with the results obtained using the IDEAS program.

ABSTRACT

NUMERICAL SIMULATION OF CTE MISMATCH AND THERMAL - STRUCTURAL STRESSES IN THE DESIGN OF INTERCONNECTS

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With the ever-increasing chip complexity, interconnects have to be designed to meet the new challenges. Advances in optical lithography have made chip feature sizes available today at 70 nm dimensions. With advances in Extreme Ultraviolet Lithography, X-ray Lithography, and Ion Projection Lithography it is expected that the line width will further decrease to 20 nm or less. With the decrease in feature size, the number of active devices on the chip increases. With higher levels of circuit integration, the challenge is to dissipate the increased heat flux from the chip surface area. Thermal management considerations include coefficient of thermal expansion (CTE) matching to prevent failure between the chip and the board. This in turn calls for improved system performance and reliability of the electronic structural systems. Experience has shown that in most electronic systems, failures are mostly due to CTE mismatch between the chip, board, and the solder joint (solder interconnect). The resulting high thermal-structural stress and strain due to CTE mismatch produces cracks in the solder joints with eventual failure of the electronic component.

In order to reduce the thermal stress between the chip, board, and the solder joint, this dissertation examines the effect of inserting wire bundle (wire interconnect) between the chip and the board. The flexibility of the wires or fibers would reduce the stress at the rigid joints. Numerical simulations of two, and three-dimensional models of the solder and wire interconnects are examined. The numerical simulation is linear in nature and is based on linear isotropic material properties. The effect of different wire material properties is examined. The effect of varying the wire diameter is studied by changing the wire diameter.

A major cause of electronic equipment failure is due to fatigue failure caused by thermal cycling, and vibrations. A two-dimensional modal and harmonic analysis was simulated for the wire interconnect and the solder interconnect. The numerical model simulated using ANSYS program was validated with the numerical/experimental results of other published researchers. In addition the results were cross-checked by IDEAS program. A prototype non-working wire interconnect is proposed to emphasize practical application. The numerical analysis, in this dissertation is based on a U.S. Patent granted to G. Peter [42].

CHAPTER 1

RESEARCH SIGNIFICANCE AND LITERATURE REVIEW

1.1 RESEARCH BACKGROUND

The current trend in the semiconductor industry is the development of sub-micrometer scale integrated circuits (IC). The signal propagation time is reduced by shorter lengths between chips, resulting in faster system speed. The personal computer purchased in the year 1995 had an Intel 133 MHz microprocessor chip, which was the top speed of a fast computer at that time. However today (2001) the fastest personal computer available uses an Intel 1.5 GHz microprocessor. It is now predicted that in five years time the chips will be 30 times faster than the chips which are in use today. These super microchips are predicted to perform four hundred million calculations in a fiftieth of a second. The ever-increasing clock speed, with IC devices shrinking to sub-micron level, demand reliable electronic assemblies with better technologies in wafer processing, die packaging, and properties of materials.

All levels of packaging involve interconnects. Interconnects can be defined at six different levels. Level one describes the silicon chip connection between chip and lead frame or board; Level two describes the printed wiring connecting individual components to each other. At level three, printed wiring boards are connected to each other. Levels four, five, and six deal with subsystem, cabinets, and other large system connections. Of these, chip to board failure is the cause of majority of electronic package failure, according to Pecht [41]. It is seen from Figure 1-1 [21], that solder related (interconnect) failures are the largest contributors to electronic package failure.

Interconnects provide mechanical, thermal, and electrical functions in the electronic package. Various technologies have been developed to solve this problem of interconnects between chips and the chip and the circuit board. The pin-in-hole or pin-through hole was the traditional method until the late 1980s when the surface mount

technology was introduced. The introduction of the surface mount technology revolutionized the electronic packaging industry. Surface mount technology includes flip chip, chip-on-chip, tape-automated bonding, and ball grid array and multi-chip module. However each of these techniques differ in its circuitry design and interconnections.

Solders have been successfully used for interconnects. Solder fluxes and solder powders have been combined into paste and are easily applied to component foot print areas. Various interconnect soldering methodologies such as vapor phase, convection infrared, hot-bar re-flow are in use today. With the surface mount technology, solder interconnect will continue to be the most reliable technology, with ease of interconnect and cost effectiveness. However, failure in solder interconnect can be due to mechanical failure due to weakness in material strength, surface tension effects, high temperature creep and plastic deformation, excessive voids, inter-metallic compound formation at interfaces, development of damaging microstructures, fatigue failure due to corrosion, and mismatch in coefficient of thermal expansion (CTE).

The joint material causes serious failure due to stress as a result of CTE mismatch when the temperature changes. The CTE of plastic/ceramic is approximately 20 times the CTE of the silicon chip. One solution is to use strain buffers between the low CTE silicon and the high CTE metal. At present, solders with strain buffers such as copper and molybdenum are in use. The strain at the solder joints due to temperature change and fatigue failure of solder interconnects are still high. This dissertation proposes an alternative design aimed at reducing stress due to CTE mismatch.

The electronic packaging problem involves the devising of packaging schemes and the use of advanced materials. Both are important aspects and should take place in a manner that is mutually beneficial. Certain packaging schemes may not be possible unless advanced materials are available. Typically a packaging scheme may require high heat extraction, combined with low stress at the interconnection. Thus the interconnect materials should have high thermal conductivity to dissipate heat produced by the chips, with close match between the CTE of the chip and the substrate to minimize thermal stress. Most of the work in electronic packaging is concerned with packaging schemes rather than materials. Figure 1- 2 [60], shows the hierarchy of packaging schemes. The chip or die is attached to the substrate or printed circuit board (PCB) on which

interconnect lines have been written (usually by screen printing) on each layer of multilayer substrate or board. In the first level, the chip (or chips) packaging may be attached to substrate via soldered joints and the substrate attached to the PCB via soldered joints. In the direct chip attach module (DCAM), the chip is attached directly to the PCB. In the multi chip module laminate (MCML), the chip is attached via cardlet, with one or many cards attached to a large card. The MCML allows for denser packaging. In surface mount technology (SMT) the surface patterns of conductors are connected electrically without employing holes. Solder is used to make electrical connection between the surface mount package (leaded or leadless) and a circuit board. Figure 1-3 (a & b)[56] shows integrated circuit package types. Figure 1- 4 (a & b) [15] shows the conventional pin-through-hole (PTH) technology and the high density packaging based on surface mount technology (SMT). Table 1-1 [60] compares the PTH and SMT technology and provides clues as to the failure mechanism.

As the chip size and complexity increases, the main challenge shifts to interconnect design to maximize circuit performance. Circuit performance is increased by minimizing propagation delays and optimizing interconnect line layout on the die [46] . In advanced chips as interconnect dimensions are scaled down, parasitic capacitance increases with an increase in propagation delays, thus effecting the speed performance of the electronic device. Further, the increase in chip size and longer interconnect increases the interconnect resistance and the resistive capacitance (RC) time constant is increased, contributing to the propagation delay. Thus for electrical performance, electrically superior interconnect and dielectric materials are needed to reduce signal propagation time. Every additional interconnection imposes a signal propagation delay, which is in turn directly proportional to the square of the dielectric constant of the substrate material, according to Hwang [21]. Table 1-2,[21] lists the dielectric constants of die-level substrate. The signal noise is reduced by multiple chip module, where the distance between the chips is reduced due to increase in package density, thus reducing parasitic capacitance. The combination of shorter signal length and lower die electric constant of the substrate aids the fast clock rate.

1.2 PRIOR ART AND FUTURE TRENDS FOR SOLUTIONS

In an effort to provide reliable cost-effective interconnection, different approaches have been examined for the last twenty-five years. One of the best examples related to this effort is by Purinton [44]. The following reproduced from the Purinton patent [44].

> "The research deals with interconnection using a non-conductive, nonporous film having metal filled pores extending throughout the thickness of the film, such that each device is contacted by metal in at least several pores, where film comprises liquid crystal or rigid rod polymer films. Figure 1-5 (a)[44], shows nanoscopic metal fibrils 26 within polymer film 27 have a diameter of only 25 nanometers, such that the tips are readily capable of entering each of valleys 27 in the surface of pad 28. This intimate contact, in combination with the larger number of fibrils that contact each pad, provides an lower resistance contact comparable with the resistance characteristic of an alloyed wire bond. Figure 1-5 (b)[44], show this device, with the film capable of deforming under pressure to fill the entire space between circuit parts. Consequently, nanoscopic fibrils 31 readily deform as a result of film compression between pads 32 and 33. Similarly fibrils 34 readily deform, as a result of film compression between pads 35 and 36. The remaining fibrils 37 are not compressed, and they make no electrical contact, but they do serve to conduct heat."

The preceding example deals with connecting and interconnect medium to an electronic part using a film and pores filled used as interconnect medium. The concept does not deal with reducing stress as a mechanical interconnect. It involves completely different materials for pore filling for the thermal properties and electrical conductivity aspect of the interconnect. The interconnect itself is pores filled with either thermally conducting or electrically conducting materials.

Another example is Meda, [30], and the following is reproduced from the Meda et al patent.[30]

> "In this devise as shown in Figures 1-6 (a,b,c,d,e) [30], copper coil 2 is bonded on both sides to an electrical insulating film 3. Holes are formed in the copper foil 2 by etching, and through-holes 5 are formed in the aforesaid electrical insulating film 3, using copper foil 2 as a mask for etching. Next, the through-holes 5 are

> filled with a conductive elastomer 6, and hardened. The copper foil 2 is then etched to form protuberances 4 of elastomer 6 having the same viscosity. The conducting elastomer 6 protuberance 4 on one side makes contact with the semiconductor device pad. While the protuberance 4 on the other side makes contact with the substrate-side pad. Pressing both together makes a conductive connection."

In the above method a metallic film is used instead of soldering. It uses silicone resin and a process of etching, to extrude portions, which are then plated (a form of electro plating), which forms as a sheath.

In other research Peterson [43] discloses interconnection using conductive films and metal-filled pores. Mahmoud [31] used a fusible conductive adhesive for making electrical and mechanical contact. Naylor [39] discloses a method of forming an anistropic electrical connection between conductive elements having an oxide layer by using an adhesive including carbon fibers and metallic particles. Ishii, Kataoka, Tanaka [26] proposed a mounting substrate onto which components are mounted wherein metal nodules are formed on conductors of connection portions by electrodeposition. Hanrahan et al. [16] used an electrical interconnect which is a structure comprising polymer matrix of microstructure nodes separated by void spaces and being interconnected by fibrils. Hinrichsmeyer, Stadler [18] and IBM Corporation [22] describe a process for making a connection using metal-filled capillaries and solder-filled elastomeric spacer which permits soldering semiconductor chips to substrates having a thermal coefficient of expansion differing from that of the semiconductor material. These processes are shown in Figures.1-7 [22] & 1-8 [18].

In recent years the number of different technologies available to resolve the interconnect problem has increased significantly. These include surface mount, through hole, array packaging, thick and thin film hybrids, multi-chip modules and fiber optics. Though interconnects on silicon ships are originally the best electrical interconnects there are, International Technology Roadmap for Semiconductors [25] predicts that after 2006 no known physical solution will be able to scale to keep up with the speed and integration level of the chips required at that time. This scaling barrier is the under lying reason why even those on-chip interconnects are starting to run into serious limits.

Hence we may need to consider short distance optical interconnects much sooner than we would have guessed. Optical interconnects are not bound by the electronic scaling limit because the physics of the two approaches are completely different. Thus off-chip interconnects are thus likely to be an attractive first implementation of optical interconnects to silicon chips.

The use of fiber-optics for long distance communication is based on the fact digital optical signals can be propagated over long distance inexpensively with very high data transmission rate with low attenuation and signal degradation. But recently the use of a multiplicity of spectral bands in a single fiber for signal transmission (through wavelength-division multiplexing) to provide even higher bandwidths, has sparked a natural interest in extending the optical techniques to shorter–and shorter distance, according to Li, Towe, Haney [29]. Fig 1-9 reproduced from Li, Towe, Haney[29], shows the optical interconnection hierarchy. The spatial density of the optoelectronic (OE) elements and channels must match the interconnect requirements of modern high-density integrated circuits in order to achieve clear competitive advantages over traditional wire interconnections. Hence spatial parallelism plays a more important role at the shorter distance than it does at the longer distance. This has created interest in developing opto-electronic technologies that could be used in microelectronic interconnects. As the clock speed in chips exceed 2.0 GHz, the internal computational bandwidths of these chips increases greatly. However, the communication bandwidths between chips and other components in a system is severely limited by metallic interconnections. As mentioned previously, these physical constraints are due to RC time constant, cross talk between conductors, and ohm losses. At present the two main techniques being developed are guided-wave approaches and free-space concepts. Both techniques could make use of the smart pixel technology now being developed. Hence future interconnections for chip to chip, or chip to board etc., could be in the form of optical interconnection. However, this technology is not readily available at present to solve the chip to chip, or chip to board bottlenecks. A good account of all recent developments in optoelectronics is given by Li, Towe, Haney [29].

None of the above prior art, and optoelectronic technology have the overall structural and electrical combination and configurations of an interconnection bundle analyzed in this dissertation, thus the proposed approach is unique.

1.3 COMPOSITE MATERIALS

One approach to meet the requirements of advanced materials in electronic packaging is to create new composite materials according to Chung [8] and Brinson, Reinhart [6] . Composite materials consist of two or more constituents with each constituent maintaining distinct properties and regions. Accordingly alloys are not composites. The most common composites consists of a matrix reinforced with continuous or discontinuous fiber whiskers, or particles. The four key classes of composites are polymer-matrix composites (PMC's), metal matrix composites (MMC's), ceramic-matrix composites (CMC's) and carbon/carbon (C/C) composites. In addition, there are composites in which the phases have amorphous geometry's. For example, some circuit breaker contacts are made by infiltrating silver into a porous pre-form made by sintering tungsten particles, in essence a metal/metal composite.

One of the well-established composites is the glass fiber reinforced polymer (GFRP) for printed circuit boards. Recent advanced composites provide unique advantages by being able to tailor their CTE, with high thermal conductivity, low density, and with high strength, and stiffness. At present, the leading composites of interest for applications such as heat sinks and packages are carbon fiber reinforced epoxy (CFR/Ep), carbon fiber reinforced aluminum (C/Al), carbon fiber reinforced copper (C/Cu), boron fiber reinforced aluminum (B/ AI) and silicon carbide particle reinforced aluminum (SiC)p/ AI), according to Brinson, Reinhart [6] and Harper, Sampson [17]. Fiber reinforced composites are strongly anistropic; their properties depend strongly on fiber direction. In contrast, monolithic and particle reinforced metals tend to be isotropic; their properties are the same in every direction. Mechanical and physical properties of fiber reinforced materials can be tailored over wide ranges by selection of fiber, matrix, fiber volume fraction, and fiber orientations. Figure 1- 10 [8], shows how the isotropic in-plane CTE of copper reinforced with a variety of pitch-based carbon fibers varies with fiber volume fraction. Note that by varying fiber volume fraction, V_f, it is possible to match the

CTE of virtually all materials of interest, including silicon, gallium arsenide, alumina, beryllia and aluminum nitride. Figure 1-11 [8], shows the in-plane thermal conductivity of C/Cu composites vary with V_f, and the CTE's are much higher than those of conventional packaging materials with low CTE's. Through-thickness conductivity's are also high. Figures.1-12 [8] & 1-13 [8], show the CTE and thermal conductivity of carbon fiber reinforced aluminum vary with fiber volume fraction. Another important composite materials is SiC reinforced aluminum alloys. The purity of SiC plays an important role here, and high purity particles have higher thermal conductivities.

Problems associated with brazes and solders can be alleviated by the use of composites brazes or solders which contain a filler of low CTE. Graphite is a suitable filler for alloys typically used for brazing and soldering such as the silver-based braze alloys and tin-based solder alloys. Carbon fibers have been successfully used as a filler for both brazes, according to Cao, Chung [7] and Zhu, Chung [62] and solders according to Ho, Chung [19]. Either short or continuous carbon fibers can be used. Short fibers are needed if the solder or braze is to be applied in the form of a paste.
Continuous fibers are more effective than short fibers in decreasing the CTE, but they cannot be in a paste form and are the limited to applications in solder/braze preforms.

Polymers are used as adhesives for attaching a die to a substrate. Due to the low CTE of the die and the substrate, a low CTE is desired for the adhesive. A filler of low CTE can be added to the polymer for this purpose. Because of the need to dissipate heat from the die and because polymers are in general thermal insulators, the filler is preferably a thermal conductor. Graphite and AIN are thus suitable fillers.

Solders in the form of solder paste, according to Shi, Saraf, Huang [47] compete with polymer adhesives for use as screen printable die attach. The attraction of solders lies in their high thermal conductivity. Like polymeric adhesives, solders suffer from a high CTE. Solders suffer in particular because they are fatigued by thermal stresses arising from CTE mismatches. Use of an active (titanium-containing) solder together with a low CTE filler (such as molybdenum particles) alleviates CTE mismatch but makes the solder less ductile.

1.4 PROBLEM DEFINITION

In industry today two types of solders are used, according to Viswandher [60] : soft solder and hard solder. Hard solder alloys are based on Au-Sn, Au-Ge, and Au-Si. Hard solder has a low melting point, with a relatively long fatigue life. However hard solder is expensive and it is typically only used for chip sizes smaller than 0.25 in. Since the chip is small the differential expansion between the copper and the silicon is small and thus the stress is reduced, with relatively long fatigue life. Due to the cost, even in this case soft solder is often used. Soft solder alloys are based on Pb, Sn, In, Ag, Bi, and Cd. They are low cost and also have a low yield stress at low temperature. They plastically deform and have a low fatigue life. Soft solder is normally used for chip sizes between 0.25 in and 1.00 in. If chip sizes are greater than 1.00, then there are other approaches. One is to parallel two chips of half the size, which reduces the thermal expansion stress. However due to close proximity of many joints and power cycling, electrical failures are not uncommon. Other approach is in the use of low expansion materials such as W, or Mo. However the surfaces still rub against each other due to CTE mismatch, and fatigue failure occurs.

It is well understood that the elements of an electronic package are fabricated from materials that are mechanically joined at one temperature and then exposed to different temperature in use, according to Viswandher [60]. Owing to the differing CTE, the joined materials are subjected to thermal stresses that can fracture component to carrier interface joints causing mechanical and electrical failure. From Table 1- 3 [21], it can be seen that silicon has a low CTE compared to the CTE of other packaging materials. During manufacture the temperature is normally raised to 400 F for solder reflow and then cooled to room temperature. This temperature change introduces strain at the solder joints and stress in the components before being used.

The rigidity of the package clamped to the heat sink determines the type of strain induced in the solder joints due to the temperature gradient. In Figure 1-14 (a), the package is rigidly clamped, and the solder joint is subjected to a shear dominance strain field. In Figure 1-14 (b), the package is not rigidly clamped, hence the solder joint is subjected to a perpendicular force in addition to the in plane shear strain. This results in

bowing of the electronic component. Note that Figures.1-14 (a) & (b) are highly magnified.

In this dissertation, a unique strain accommodation is explored, based on the fact that the strain buffer between the chip and the board can be made of individual fibers. Each individual fiber has a very small contact with the chip. Hence with the chip having a very small CTE, each fiber will separate at the chip, reducing the stress at the chip. Figure 1-15, shows how the fibers are anticipated to be flexible due to a large temperature difference. This allows the chip size to be increased. The materials for the fibers could be copper, titanium, or silver, based on cost considerations.

1.5 APPROACHES AND STRATEGIES

The numerical simulation and design of a solution to a practical problem such as joint failure in electronic components is quite far reaching. The benefits of this are the availability of reliable, more robust, and cost effective component for electronic packaging. The actual prototype production and testing of a component during the design and development phase is more expensive and time consuming. Thus the computer model could be used to optimize the chip, interconnection, and the board for thickness, material selection, percentage of fiber in the composite for interconnection; all before actual component production. This would result in a component being designed with minimum cost and in use; for minimum thermal stress despite greater temperature changes, and thus higher reliability of the electronic component.

Using pure conduction theory and numerical modeling the CTE effect on first level interconnect (chip to lead frame or board) is studied. In this research the structural static analysis capabilities of the ANSYS [(2)] program are used to determine the displacements and stresses that occur due to thermal loading. Static analysis is appropriate for solving problems in which the time-dependent effects of inertia and damping do not significantly effect the component's response. Static analysis can be used to predict the stress in the component resulting from a temperature distribution in the chip. In the real world the temperature distribution in a chip is not uniform as prescribed in this study; as the heat generation rate inside the chip is not uniform. In order to keep the chips working at a relatively stable temperature range many semi-conductor devices

have thermal compensation systems to lock the thermal load. This keeps the chip work at relatively stable temperature range.

There are many reasons for combining testing and analysis, including validating results. These could confirm or determine material properties, wire or fiber diameters, number of fibers or wires in the flexible inter-connect, their spacing, and the solder thickness. The model studied in this dissertation is to highlight the advantages and feasibility of using discrete contacts between the silicon chip and the board.

Typical semi-conductor device design and operation consists of different combination of components including chip, circuit board, substrate, adhesive layers, heat sink, thermal vias of different sizes, and material. Detailed modeling for this study is unwarranted, as it would require a significant amount of computational resources, making the problem solving process practically impossible. Hence, in this dissertation the approach is to model only the chip, the wires or fibers, the circuit board, and the solders.

Two basic models are analyzed. In the first model the chip is attached to the board by means of wires, wire interconnect. In the second model the chip is directly soldered to the board: solder interconnect. As a general rule, finite element modeling should start with a simple model. Once the mathematical model has been solved accurately and the result has been interpreted, it is feasible to consider a more refined model in order to increase the accuracy. In this study a simple two-dimensional model is developed to obtain an idea of the thermal loading, boundary conditions, and the appropriate locations to apply them. Based on the results of the two-dimensional model, the three-dimensional model is developed to obtain more accurate results.

Materials of electronic assemblies can fracture when they are subjected to repeated stress that are considerably less than their ultimate static strength. This failure appears to be due to submicroscopic cracks that grow into visible cracks, which then leads to a complete rupture under repeated loading. Every stress cycle experienced by the electronic system will use up a small part of its total life. When enough stress cycles have been experienced, the fatigue life will be used up and cracks will develop in structural elements such as solder joints, plated-through holes, and electrical lead wires, resulting in failure.

Fatigue can also be generated in electronic system by shock and vibration. It is probably safe to say that all electronic equipment will be subjected to some type of vibration at some time in its life. Vibration can be associated with the end use of the product or due to transportation of the product from the manufacturer to the consumer. Thermal stress can develop in an electronic assembly while it is stored or sitting on a shelf, with no electrical operation. The combined thermal cycle fatigue, and vibration cycling fatigue is common in moving vehicles or machinery such as airplanes and washing machines. Small fractures may be initiated during the thermal cycling environment, but they do not propagate rapidly since the thermal cycling rate is very low (1 to 10 cycles per day). Vibration environments, on the other hand, often produce several hundred cycles per second, so small cracks can grow more rapidly in vibration until a full fracture occurs. Field experience with military types of electronic equipment shows that the greatest number of failures typically occur in the electrical interconnect system, according to Pecht [41]. In this study modal and harmonic analysis is done on the two-dimensional models. In the three-dimensional models, modal analysis is performed, with the solder- only model. The mathematical model is presented in chapter 2 and the numerical simulation results are presented in chapter 3.

Test validation of essential aspects of the model response is helpful in many ways. Comparison of experimental data with analysis data for solution confirmation is a separate activity from verification of the Finite Element model. The model could be conceptually incorrect, and yet produce the desired results. The model could be incorrect for several reasons; wrong assumptions, wrong numerical procedures and errors in post processing of results. Experimental measurement and validation could be very difficult and costly. It should be emphasized that though computer simulation is considered to be inexpensive, it may not be so, if the model is sophisticated and requires expensive validation. In this study, the numerical simulation model is cross- checked by simulating the same geometry of the model, with the same property etc., using two different computer codes. In addition the results of the numerical simulation is validated with the numerical/experimental results of other published researchers.

In this study the experimental approach is to emphasize the practical applications of the proposed design. The experimental approach was not to verify the numerical model. The questions to be asked are:

1. How well can the interconnect wires or fibers be confined in a bundle
2. What type of manufacturing process can be used.
3. What type of material can be used for this process.
4. For electrical transmission can the wires or fibers be insulated.
5. How uniform and consistent are the wires

For this experiment a sample interconnection is made out of super conducting material. The wires were manufactured from multi-filamentary internal tin, Nb_3Sn wire using a patented modified jelly roll (MJR) process. The MJR method produces uniform and consistent super-conducting wire. Discussions of the feasibility of this approach, and the details of the sample interconnect are described in chapter 4. Discussions of results and future research are presented in chapter 5.

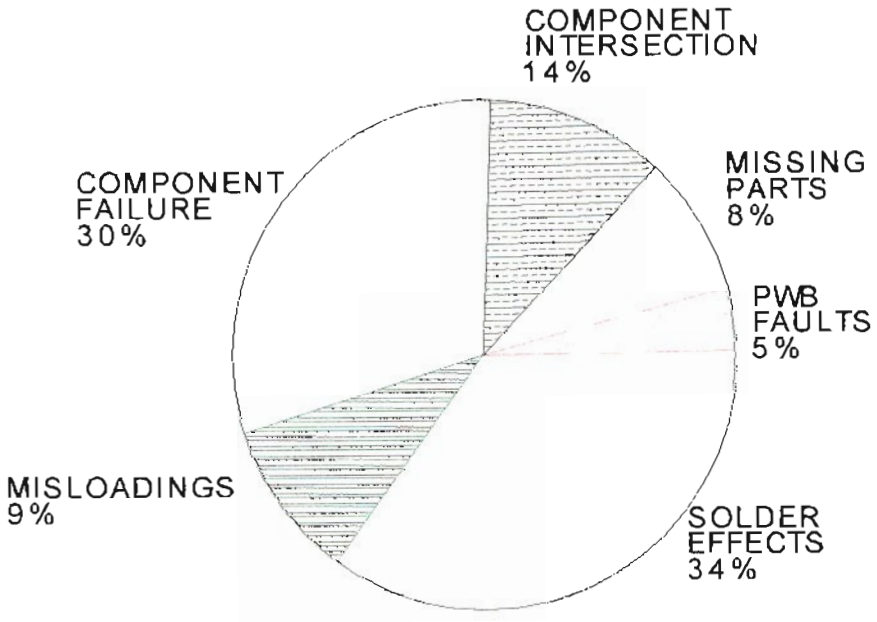
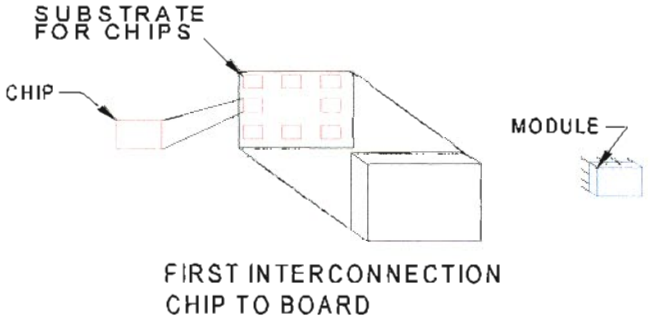
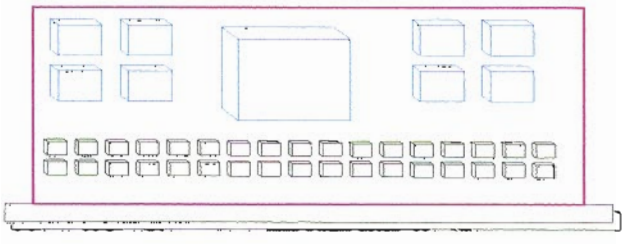


Figure 1-1 Distribution of Surface Mount Manufacturing Defects
(Adapted From Reference 21)





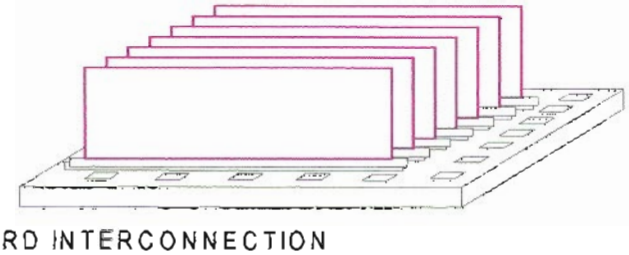


Figure 1-2 Levels of Electronic Packaging
(Adapted From Reference 60)

NAME		APPEARANCE	REMARKS	
			MATERIAL	LEAD PITCH, ETC
LCC	LEADLESS CHIP CARRIER		C	1.27mm(50mil) 1.00mm(40mil) 0.975mm(30mil) CONTACT No. 16~36 PIN
PGA	PIN GRID ARRAY		C P	1.27mm LEAD PIN No. 100~500 PIN
SOP	SMALL OUTLINE PACKAGE		P	1.27mm(50mil) TWO-WAY LEAD 16~36 PIN
PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm(50mil) J-SHAPED LEAD 16~124 PIN
SOJ	JBEND SOIC		P	1.27mm(50mil) TWO-WAY LEAD 16~124 PIN
QFP	QUAD FLAT PACKAGE		P C	1.00mm 0.8mm .065mm FOUR-WAY LEAD 20~128 PIN

NOTE P: PLASTICS C: CERAMICS

(a)

NAME		APPEARANCE	REMARKS	
			MATERIAL	LEAD PITCH, ETC
S-DIP	SHRINK DIP		P	1.778mm(70mil) LEAD PIN No. 4~64 PIN
DIP	DUAL INLINE PACKAGE		P C	2.54mm (mil) LEAD PIN No. 4~64 PIN
PGA	PIN GRID ARRAY		C P	3.54mm/1.27mm (100mil)/(50mil) LEAD PIN No. 64~240 PIN
SKINNY	SKINNY DIP		P	2.54mm(70mil) WIDTHWISE PITCH 1/2 SIZE LEAD PIN No. 8~28 PIN

(b)

Figure 1-3 Integrated Circuit Package Types:
(a) Pin Inserting-Type Package
(b) Surface-Mounting Type Package
(Adapted From Reference 56, © 2000 IEEE)

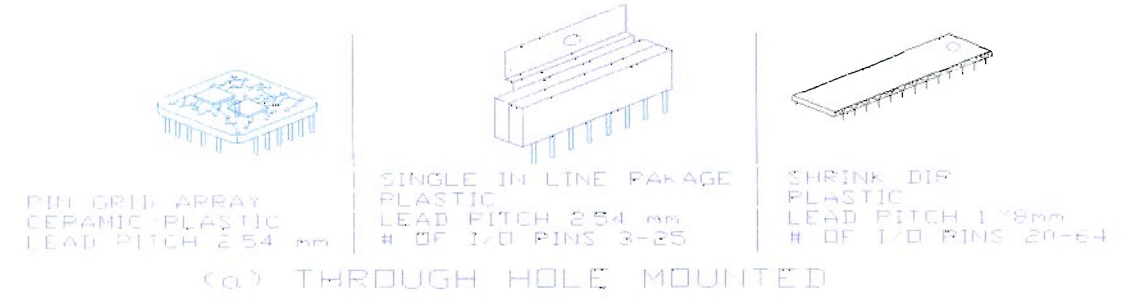
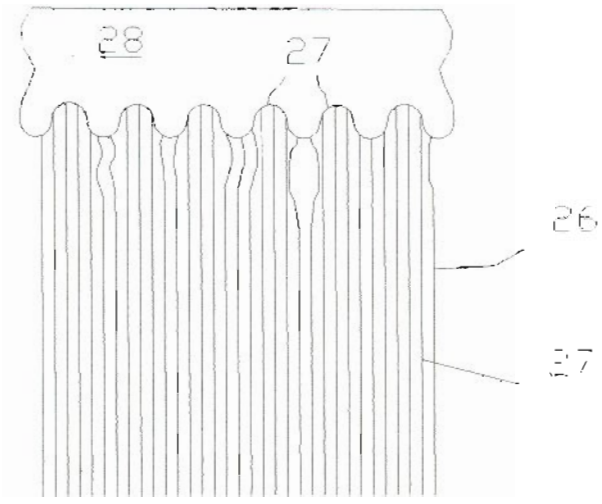
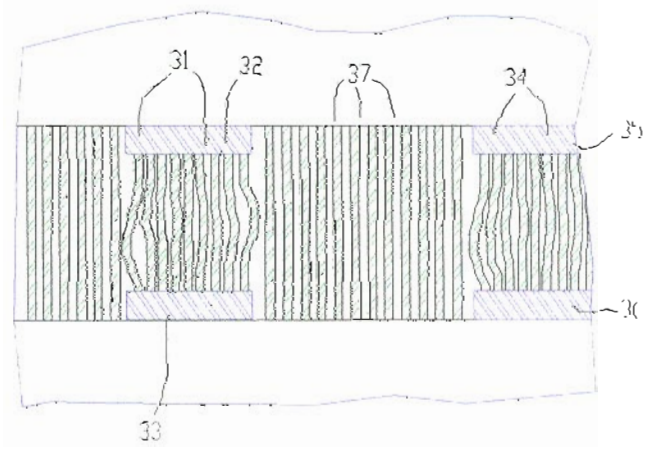


Figure 1-4 (a) Conventional Pin through Hole Components
(b) High Density Surface Mount Technology
(Adapted From Reference 15)



(a)



(b)

Figure 1-5 (a,b) Nanoscopic Metal Fibrils)
(Adapted From Reference 44)

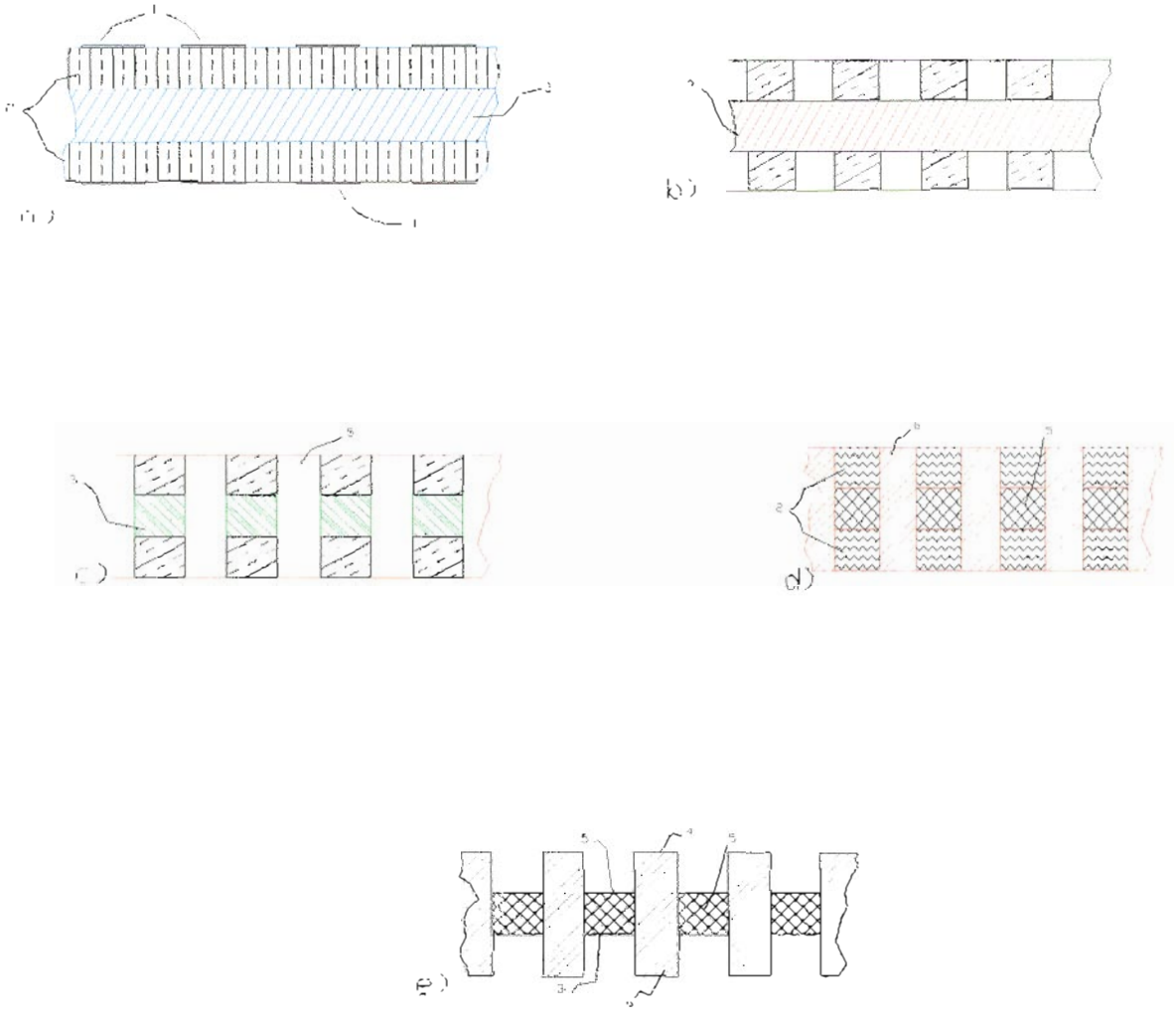


Figure 1-6 (a,b,c,d,e) Copper Coil Bonded with Electrical Insulating Film
(Adapted From Reference 30)

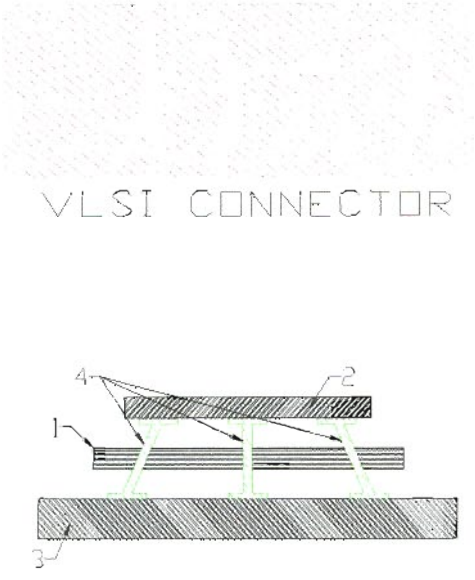


Figure 1-7 Metal Filled Capillaries
(Adapted From Reference 22)

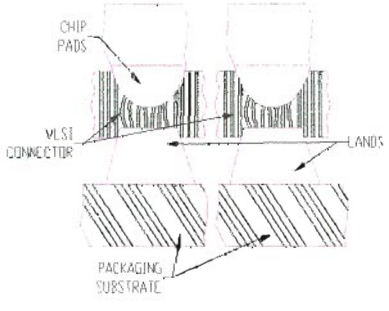


Figure 1-8 Solder-Filled Elastomeric Spacer
(Adapted From Reference 18)

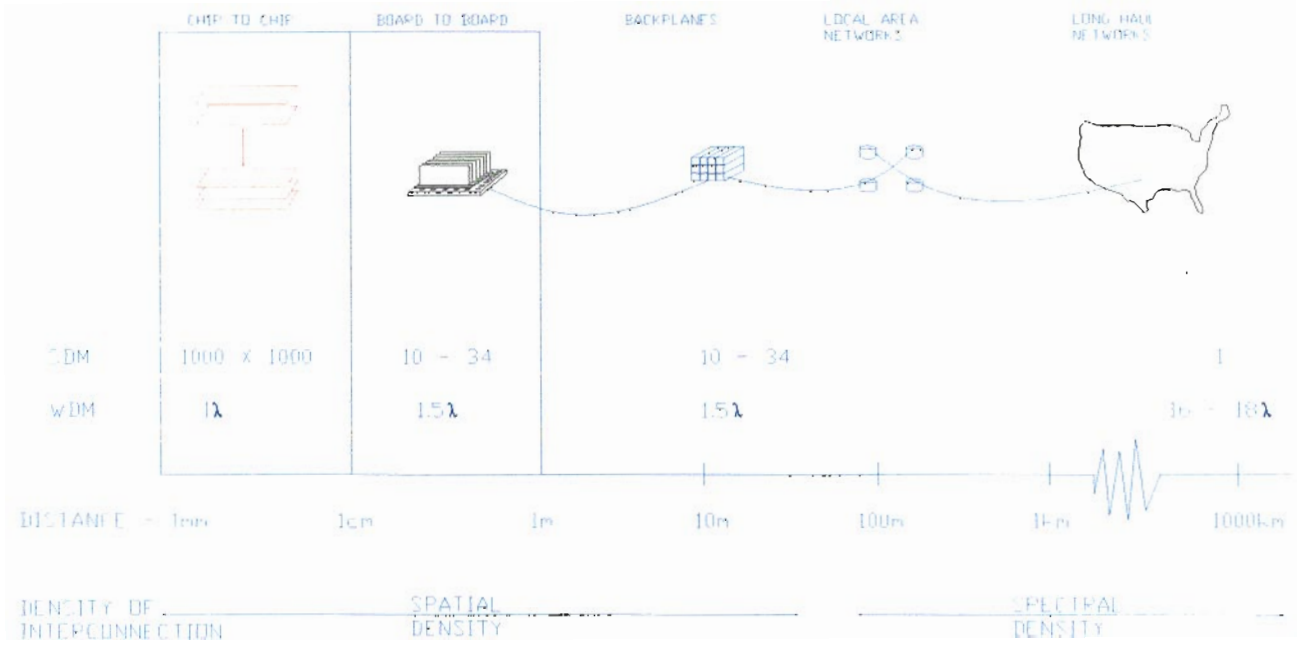


Figure 1-9 Optical Interconnection Hierachy
(Adapted From Reference 29, © 2000 IEEE)

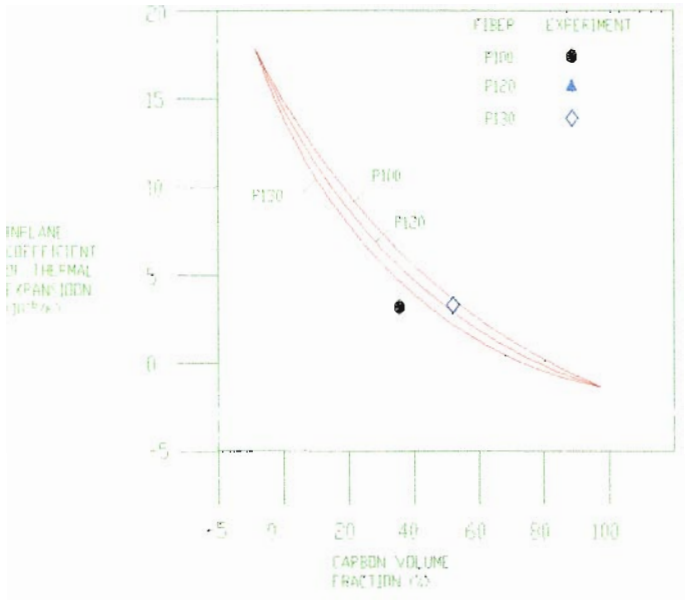


Figure 1-10 Variation of Inplane (isotropic) Coefficient of Thermal Expansion With Fiber Volume Fraction for Carbon Fiber Reinforced Copper (0/90) Laminates
(Adapted From Reference 8)

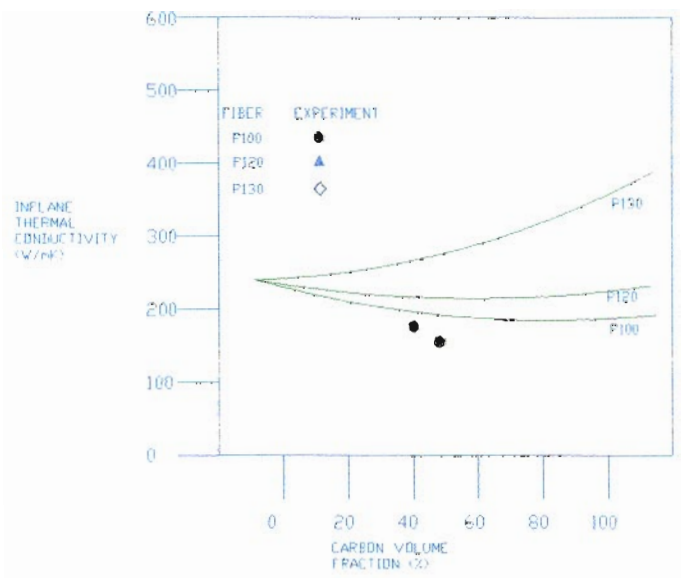


Figure 1-11 Variation of Inplane (isotropic) Thermal Conductivity With Fiber Volume Fraction for Carbon Fiber Reinforced Copper (0/90) Laminates
(Adapted From Reference 8)

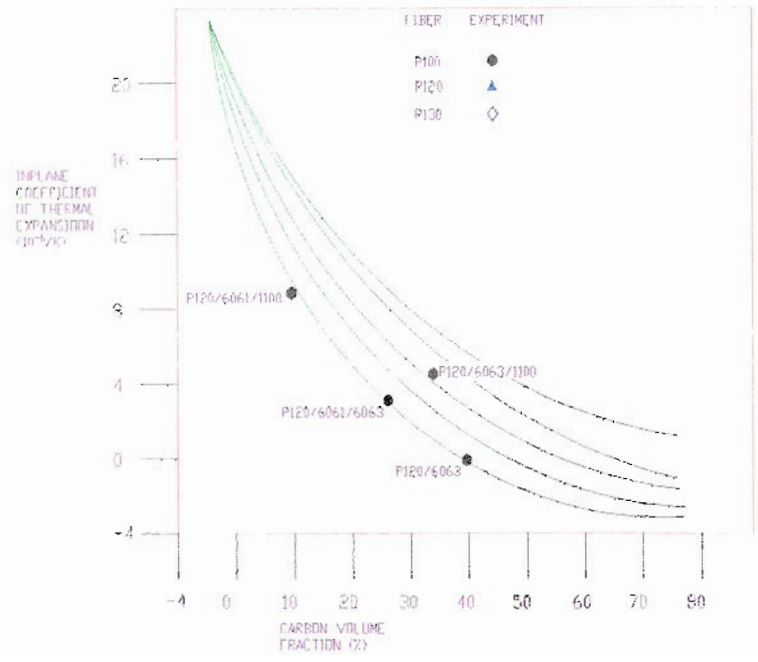


Figure 1-12 Variation of Inplane (isotropic) Coefficient of Thermal Expansion With Fiber Volume Fraction for Carbon Fiber Reinforced Aluminum (0/90) Laminates (Adapted From Reference 8)

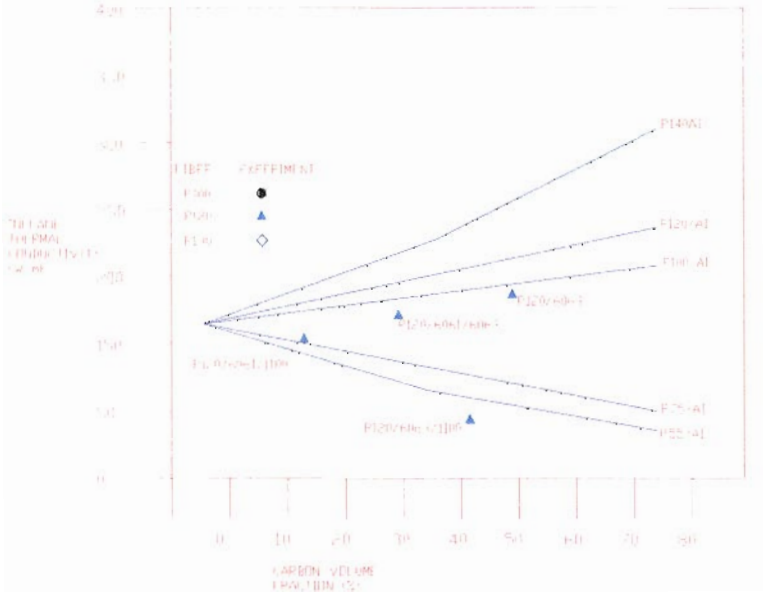
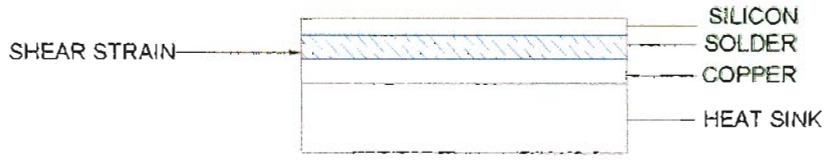
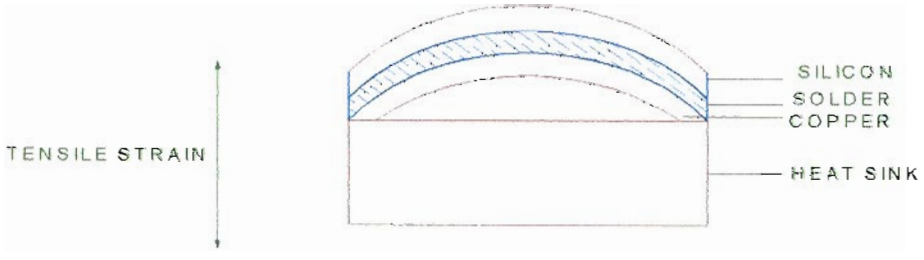


Figure 1-13 Variation of Inplane (isotropic) Thermal Conductivity With Fiber Volume Fraction for Carbon Fiber Reinforced Aluminum (0/90) Laminates (Adapted From Reference 8)



(a)



(b)

Figure 1-14 (a) Package Rigidly Clamped
(b) Package Not Rigidly Clamped

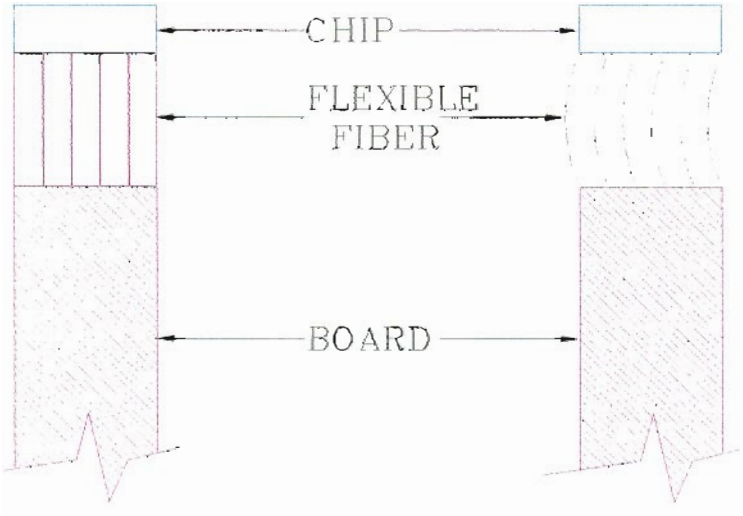


Figure 1-15 Anticipated Flexibility in Fibers due to Large Temperature Difference

Table 1-1 PTH and SMT Component Technology Comparison
Adapted from Reference Viswandher [60]

Item Description	**PTH Components**	**SMT Components**
Carrier CTE mismatch	No concerns except for very large components (>50 mm)	CTE mismatch is a reliability issue
Package types	Single inline package (SIP), Dual inline package (DIP), Pin grid array (PGA)	J-Leaded and gull wing, Leadless carrier (LCC), Quad flat pack (QFP), Tape automated bond (TAB), Pad grid array (PGA), Ball grid array (BGA)
Assembly method	Hard solder, Solder fountain, Wave solder	Hard solder, Vapor phase reflow, Laser reflow
Solder joint reliability	Affected by lead contamination and hole plating quality	Affected by terminal metal quality, Placement accuracy, and Solder paste volume

Table 1-2 Dielectric Constants of Common Substrate Materials
Adapted from Reference Hwang [21]

MATERIAL	Dielectric constant, Room temperature, 1 MHz
FR-4	4.8
Polyimide	3.5 – 4.5
BT Epoxy	4.2
Cyanate ester	4.5
AL_2O_3 (99%)	9.2
AL_2O_3 (96%)	9.0
B_eO	6.7
AIN	6.0 – 8.5
SiC	40.0 – 45.0
GaAs	12.8
Si	11.7
Diamond (Chemical Vapor Deposition-CVD)	5.5 – 5.9

Table 1-3 CTE of Solders and Substrates
Adapted from Reference Hwang [21]

Material	**CTE, 10^{-6}/°C at 293 K**
Diamond	0.8 – 1.7
Si	3.0
SiC	3.7 – 3.8
AIN	4.1 – 4.6
GeAs	5.9
ALO_3	6.4
BeO	8.0
Kovar	3.3 – 5.8
Alloy 42	5.3
FR-4	16
Cu	16 - 17
Polymide	13
Epoxy/Kevlar	3 - 8
Kevlar/Cyanate Easter	1 - 3
Cynate easter	15
BT Epoxy	14 (XY)
Moulding compound	15
Ag-filled die attach	52
75 Sn/25 Pb	23.8
65Sn/35 Pb	24
60Sn/40 Pb	24.1
30 Sn/70 Pb	26.8
20 Sn/80 Pb	27.9
62 Sn/36 Pb/2Ag	21.0
40 Sn/60Bi	17.5

CHAPTER 2

MATHEMATICAL MODELING

The analysis of an engineering problem requires the idealization of the problem into a mathematical model. It is clear that we can only analyze the selected mathematical model and that all the assumptions in this model will be reflected in the predicted results. We cannot expect any more information in the prediction of the result than the information contained in the model. Therefore it is crucial to select an appropriate mathematical model that will most closely represent the actual situation. It is also important to realize that we cannot predict the response exactly, because it is impossible to formulate a mathematical model that will represent all the information contained in an actual system.

As a general rule, the mathematical modeling should start with a simple model. Once the mathematical model has been solved accurately and the result has been interpreted, it is feasible to consider a more refined model in order to increase the accuracy of the prediction of the actual system. For example, in a structural analysis, the formulation of the actual loads into appropriate models can drastically change the results of the analysis. The results from the simple model combined with an understanding of the behavior of the system will assist in deciding whether and at which part of the model further refinement is needed. Clearly, the more complicated models will include more complex response effects but it will also be more costly and sometimes more difficult to interpret the solutions.

Modeling requires that the physical action of the problem be understood well enough to choose suitable kinds of elements. The object is to avoid waste of time and computer resources with over-refinement and badly shaped elements. Once the results are calculated, it is imperative to check the results to see if they are reasonable. Checking is very important because it is easy to make mistakes when we rely on mathematical software to solve complicated systems.

2.1 NUMERICAL APPROACHES

There are many tools available to study thermo-mechanical effects of new electronic packages. Designs can be optimized for different materials properties, temperature changes, environmental effects etc. Once meaningful analytical results are obtained, then a prototype is built and tested under laboratory conditions to confirm the analytical results. Finding an appropriate way of implementing the model and achieving meaningful results is another major task of modeling analysts. The three most popular analytical methods available to engineers and designers to day are hand calculations (closed form solutions), finite difference method (FDM), and finite element methods (FEM). Boundary elements (BEM) are becoming more popular these days for larger models. BEM is supposed to be 10 to 25 times faster than FEM, however it is not believed to replace FEM, but rather to complement FEM, according to Trevelyan [58].

Hand Calculations/Closed Form Solutions: Hand calculations are normally effective for small problems, and to get a rough estimate of a large problem. They are also used to check larger computer runs. Closed form solutions are possible if the problems are linear, moderate on size and the geometry is not very complex. Closed form solutions give more accurate results than numerical solutions.

Finite Difference Method (FDM): The evolution of numerical method, specifically FDM for solving ordinary and partial differential equations, began around the turn of the century, according to Anderson, Tannehill, Pletcher[1]. FDM is based on directly discretizing the governing equations using Taylor series, or directly establishing discrete finite difference equations through energy conservation. It is a very powerful and convenient method to use. It gives a "pointwise" approximation to the governing equations, which discritizes the domain into a finite difference grid with nodes at intersections of the grid. Finite difference equations need to be established for every node, both inside and on the boundaries of domain, and this set of equations must be solved simultaneously to get the solution of interest at the nodes. The solutions obtained are only at the nodes in the domain, and for values elsewhere in the domain interpolation by an appropriate order polynomial function is required. When this method is applied to solutions of thermal problem in electronic packaging, two-dimensional and three -

dimensional thermal analog resistor networks are usually developed to accurately simulate the characteristics of the model for steady state or transient solutions, according to Steinberg [55]. The model will typically be made up of nodes that are interconnected with thermal resistors those represent the heat flow in the system. Transient solutions to complex problems can be obtained by making a variable for one area or element is dependable of another area or element. One of the disadvantages of FDM is its inability to handle irregular geometries. However, through proper grid generation solutions to irregular shapes have been accomplished, according to Patankar [40], Nakamura [38] and Sorenson [52]. Well known codes like FLUENT (ICEPAK), FLOW3D use finite volume methods, which is regarded as the simplest of a more general set of methods called finite element methods FEM, according to Ferziger [14].

Finite Element Method (FEM): The importance of the finite volume method lies in the fact that approximating the equations by integration makes it easier to assure that the integrated (or global) form of conservation laws are accurately reproduced. One version of the FEM consists of multiplying the equation by a "weight" function (which may be a known function or the solution itself) and integrating the result over a finite region of the solution domain. Both the solution and the weight function are then approximated by polynomials in order to make quadrature possible and one obtains a system of equations for the coefficient of the polynomials, according to Ferzier [14], Kardestuncer[27] and Zienkiewicz [63]. There are a great variety of FEMs. Their principal advantages are that (1) the spacing of the grid points can be made arbitrary with no increase in complication, and (2) the accuracy of the approximation can be increased by using higher order polynomials without much difficulty other than an increase in the amount of calculation to be done. In dealing with partial differential equations in two and three dimensions, the first advantage becomes the very powerful one that the computational points need not be arranged on a rectangular grid (triangles are used quite commonly), allowing the method to deal with irregular boundaries very effectively, and the second advantage is retained as well. In the application of FEM for electronic packaging modeling, the major advantage is that the model can be used for both thermal and structural analysis. This aspect is explained in greater detail in Section 3.1. The major disadvantage of finite element

methods are that they require more work to derive and the systems of equations are not quite as regular as those produced by finite difference methods.

Boundary Element Method (BEM): There are number of applications in which Laplace's equation needs to be solved in an irregular region but results are needed only on the boundary. For example, one might have a problem in which a potential is given on the boundary and the desired information are the gradient of the potential on the boundary. No interior information is necessary, and if computation of the interior solution can be avoided, so much the better, according to Ferziger [14]. BEM can be derived by the use of Green's formula for Laplace's equations. The BEM discretizes the boundary into elements and solves for values on the boundary. The method is supposed to be more accurate for boundary intensive variations. In addition, the BEM uses a lower dimension computational domain with regard to the problem domain, since the boundary of a three dimensional domain is a surface (2-D) and a two dimensional domain is a curve (1-D). Therefore, the meshing can be much fine with a given computational capacity. Although discretization of the interior domain may be necessary for the non-homogeneous governing equations, e.g. involving body loads, etc., the interior can be fairly coarse without significant influence on the accuracy. The results of the BEM are not limited on the boundary only, since the interior values can be derived after the values on the boundary are obtained. The modeling techniques are similar to FEM where relatively small elements are used and where conditions change rapidly. In electronic packaging studies this is very important at stress concentrations or at hot spots in thermal analysis, because of the sharply peaking stress patterns that are generally not predicted by FEM.

In this study FEM using ANSYS [2] computer code was selected to perform all numerical analyses. The numerical model simulated using ANSYS program was cross-checked by using another FEM code, IDEAS.

2.2 MODEL REVIEW

Computer aided measurements of thermal properties in composites and electrical modeling and simulation of interconnects are discussed by Morris [36] . The thermal, stress, and strain are a coupled process. The model has to take into account the heat flow paths and the structural load paths through the system. Modeling of solder joints, lead wires, and plated-through holes are discussed by Aung[3]. Since the dimension of the chip, interconnects, board, and solder joints are really small, the element thickness becomes very small. This could produce numerical instability, due to point load, sudden changes in the boundary, or sharp corners in the structure. One way to avoid this is to spreading the load over a closely clustered group of node points. In this study the thermal load is applied to all nodal points on the chip. Further, two and three-dimensional models are simulated. Three-dimensional models use solid elements, to obtain full three-dimensional characteristics. Symmetry conditions used to reduce computer time, resources and cost. In order to check the accuracy of the model the results of a full three-dimensional model is compared with that of the symmetrical model.

The derivation and mathematical modeling of a typical heat conduction problem is discussed in many references, and the following is based on Zienkiewicz[63], Huebner[20], Cook [10] , Desai [12] and Boresi [5]. The mathematical equations describing the deformation of solids are very similar in form to those for the flow of fluids. The principal difference is that while solid behavior is formulated in terms of displacements and strains, the equivalent variables for fluids are velocities and strain rates. Another distinction is that the co-ordinate systems used are usually fixed relative to the material in the case of solids (Lagrangian method of description), but are fixed in space in the case of fluids (Eulerian method of description). This means that the equations are only applicable to small strains in solid bodies such that their overall geometries are not significantly affected. No such restriction applies to strain rates in fluids.

Using the symbols σ for stress and e for strain; individual components of stress are indicated by double subscripts as follows:

direct stress: σ_{xx} , σ_{yy} , σ_{zz}

shear stress: σ_{xy} , σ_{yz} , σ_{zx} , σ_{yz} , σ_{zy} , σ_{xz}

The first subscript defines the direction of the stress and the second one denotes the direction of the outward normal to the surface on which it acts, as shown in Fig. 2-1. According to this convention tensile stresses are positive. For rotational equilibrium to be maintained the shear stresses must be complementary.

$$\sigma_{xy} = \sigma_{yx} , \sigma_{yz} = \sigma_{zy} , \sigma_{zx} = \sigma_{xz} \qquad (2.1)$$

The components of displacements (for solids) or velocity (for fluids) in the coordinate directions x,y,z are denoted by u,v,w respectively. The direct and shear components of strain or strain rate may be defined as follows:

$$\varepsilon_{xx} = \frac{\partial u}{\partial x} , \quad \varepsilon_{yy} = \frac{\partial v}{\partial y} , \quad \varepsilon_{zz} = \frac{\partial w}{\partial z} \qquad (2.2)$$

$$\varepsilon_{xy} = \varepsilon_{yx} = \frac{\partial u}{\partial y} + \frac{\partial v}{\partial x} \qquad (2.3)$$

$$\varepsilon_{yz} = \varepsilon_{zy} = \frac{\partial v}{\partial z} + \frac{\partial w}{\partial y} \qquad (2.4)$$

$$\varepsilon_{zx} = \varepsilon_{xz} = \frac{\partial w}{\partial x} + \frac{\partial u}{\partial z} \qquad (2.5)$$

If inertia forces are negligibly small the differential equations of equilibrium for the three co-ordiante directions can be expressed as follows:

$$\frac{\partial \sigma_{xx}}{\partial x} \quad \frac{\partial \sigma_{xy}}{\partial y} \quad \frac{\partial \sigma_{xz}}{\partial z} + \bar{X} = 0 \qquad (2.6)$$

$$\frac{\partial \sigma_{yx}}{\partial x} \quad \frac{\partial \sigma_{yy}}{\partial y} \quad \frac{\partial \sigma_{yz}}{\partial z} + \bar{Y} = 0 \qquad (2.7)$$

$$\frac{\partial \sigma_{zx}}{\partial x} \quad \frac{\partial \sigma_{zy}}{\partial y} \quad \frac{\partial \sigma_{zz}}{\partial z} + \bar{Z} = 0 \qquad (2.8)$$

where X, Y, Z are the local components of the body forces per unit volume acting on the continuum in the co-ordinate directions. The most common cause of such forces is gravity. Inertia forces are normally neglected in stress analysis problems in solids, but in fluids they can only be neglected if the flows are sufficiently slow to be dominated by pressure and viscous forces.

Strains or strain rates must be compatible with each other. The physical interpretation of compatibility is that no discontinuities such as holes or overlaps of material exist in the continuum: u,v and w are continuous and differentiable functions of position. Hence, from the six strain (rate) definitions given in equations 2.2 to 2.5, the following six relationships can be obtained by eliminating u, v and w by differentiation in various ways.

$$\frac{\partial^2 \varepsilon_{xx}}{\partial y^2} + \frac{\partial^2 \varepsilon_{yy}}{\partial x^2} = \frac{\partial^2 \varepsilon_{xy}}{\partial x \, \partial y} \qquad (2.9)$$

$$\frac{\partial^2 \varepsilon_{yy}}{\partial z^2} + \frac{\partial^2 \varepsilon_{zz}}{\partial y^2} = \frac{\partial^2 \varepsilon_{yz}}{\partial y \partial z} \qquad (2.10)$$

$$\frac{\partial^2 \varepsilon_{zz}}{\partial x^2} + \frac{\partial^2 \varepsilon_{xx}}{\partial z^2} = \frac{\partial^2 \varepsilon_{zx}}{\partial z \partial x} \qquad (2.11)$$

$$2\frac{\partial^2 \varepsilon_{xx}}{\partial y \, \partial z} = \frac{\partial}{\partial x}\left[-\frac{\partial \varepsilon_{yz}}{\partial x} + \frac{\partial \varepsilon_{zx}}{\partial y} + \frac{\partial \varepsilon_{xy}}{\partial z}\right] \qquad (2.12)$$

$$2\frac{\partial^2 \varepsilon_{yy}}{\partial z \, \partial x} = \frac{\partial}{\partial y}\left[\frac{\partial \varepsilon_{yz}}{\partial x} - \frac{\partial \varepsilon_{zx}}{\partial y} + \frac{\partial \varepsilon_{xy}}{\partial z}\right] \qquad (2.13)$$

$$2\frac{\partial^2 \varepsilon_{zz}}{\partial x\,\partial y} = \frac{\partial}{\partial z}\left[\frac{\partial \varepsilon_{yz}}{\partial x} + \frac{\partial \varepsilon_{zx}}{\partial y} - \frac{\partial \varepsilon_{xy}}{\partial z}\right] \qquad (2.14)$$

These compatibility equations ensure that the strains calculated from unknown stresses are compatible.

The relationships between stresses and strains or strain rates are expressed in terms of constitutive equations, which introduce the relevant material properties. For the present study we ignore viscoelastic materials, and assume the material is purely elastic. For an elastic solid, the strains defined by equations 2.2 to 2.5 may be produced both by the application of stress and by raising the temperature. In general the properties of material may vary. If they are independent of position within the body, direction at any particular point, and stress or strain applied, then the material is said to be homogeneous, isotropic and linearly elastic. Then the constitutive equations are:

$$\varepsilon_{xx} = \frac{1}{E}\left[\sigma_{xx} - \nu\,(\sigma_{yy} + \sigma_{zz})\right] + \alpha\Delta T \qquad (2.15)$$

$$\varepsilon_{yy} = \frac{1}{E}\left[\sigma_{yy} - \nu\,(\sigma_{zz} + \sigma_{xx})\right] + \alpha\Delta T \qquad (2.16)$$

$$\varepsilon_{zz} = \frac{1}{E}\left[\sigma_{zz} - \nu\,(\sigma_{xx} + \sigma_{yy})\right] + \alpha\Delta T \qquad (2.17)$$

$$\varepsilon_{xy} = \frac{\sigma_{xy}}{G} = \frac{2(1+\nu)}{E}\,\sigma_{xy} \qquad (2.18)$$

$$\varepsilon_{yz} = \frac{\sigma_{yz}}{G} = \frac{2(1+\nu)}{E}\,\sigma_{yz} \qquad (2.19)$$

$$\varepsilon_{zx} = \frac{\sigma_{zx}}{G} = \frac{2(1+\nu)}{E}\,\sigma_{zx} \qquad (2.20)$$

Where E is Young's modulus, G is the shear modulus, ν is Poisson's ratio, α is the coefficient of thermal expansion and ΔT is the temperature rise. The thermal expansions and contractions must be considered for each of the three axes X, Y, and Z, since the failure mechanisms are different for these different axes.

In two dimensional simulation, plane strain, and plane stress are two important modes of deformation. Figure 2-2, shows a solid body whose cross section is uniform in the z-direction. If its length in z direction is large, the typical section OABC can be regarded as being remote from the ends. If the surface forces applied to the body are in the X-Y plane, the resulting state of stress at such section is two-dimensional, and it is independent of Z with w=0. From the strain definition equations 2.2 to 2.5 $\varepsilon_{zz} = \varepsilon_{yz} = \varepsilon_{zx} = 0$

For the solid plate shown in Figure 2-3, which is lying in the x-y plane; if the applied traction's are in the same plane, the stress on the faces of the plate are zero. If the plate is sufficiently thin then the plane stress approximation $\sigma_{zz} = \sigma_{yz} = \sigma_{xz} = 0$ can be applied throughout the material.

Structural static analysis is used to determine the displacements, stress, strains, and forces that occur in a structure or component as a result of applied loads. Static analysis is appropriate for solving problems in which the time–dependent effects of inertia and damping do not significantly affect the structure's response. This analysis can be used for many applications, including the prediction of stresses in a component resulting from a temperature distribution.

The solution to linear problems involves the solution of sets of linear algebraic equations. Various types of non-linearity are discussed later. Typically geometric non-linearity's can be introduced in a problem involving solid media in which the strains are sufficiently large to significantly affect the shape of the solution domain. There are different approaches to solving this type of problems. One method is called the incremental approach. In which the non-linear analysis is replaced by a series of linear analyses for progressively increasing external loads, after each of which the finite element mesh geometry is recomputed. This method would be tedious if the model simulated is a complicated geometry. Alternatively, the overall equations can be solved by an "iterative" method and the mesh geometry and hence the overall stiffness matrix updated at prescribed intervals during the solution process.

Either geometric or material property effects introduce non-linearity. Examples of material non-linearity include non-Newtonian fluids and non-linearly elastic solids, whose properties are functions of the local state of deformation. If it is determined that the non-linearity's affect the behavior of a structure to the extent that they cannot be ignored, nonlinear analysis is required. In this study only linear solutions were determined.

Material Nonlinearities: A material non-linearity exists when stress is not proportional to strain. There are various types of nonlinear behavior. Plasticity, multilinear elasticity, and hyperelasticity are characterized by a nonlinear stress-strain relationship. Visco-plasticity, creep, and visco-elasticity are behaviors in which strain may depend on other factors such as time, temperature, or stress. In numerical modeling, there are different ways to simulate non-linear behavior of materials. In the ANSYS program a Newton-Raphson method accounts for nonlinear material behavior.

Geometric Nonlinearities: Geometric Nonlinearities occur when the displacements of a structure significantly change its stiffness. In numerical simulations there are different ways to account for these types of geometric Nonlinearities. Large strain, large deflection, stress stiffening, and spin softening. Large strain geometric Nonlinearities account for the large localized deformations that may occur as a structure deforms. There are no assumptions on the magnitude of the strains or rotations that occur in the material. Large strains can be accommodated by adjusting element shapes to reflect the changing geometry.

Large deflections represents a change in global structural stiffness resulting from a change in element spatial orientation as the structure deflects. The strains are assumed to be small, but the rotations are large. In simulation we can account for the large deflection by updating the element orientations as the structure deflects. In ANSYS program large rotation and consistent stiffness capabilities are available for beam and shell elements. Another method is to use follower loads that always act normal to the structure's elements. Element pressures are used to describe such loads. This method is also available in the ANSYS program.

For large strain and large deflections, the stiffness is affected by the displacements. Therefore, an iterative solution is required to solve for changes in stiffness and Newton-Raphson procedure is normally employed for this solution.

Element Nonlinearities: Nonlinear elements are those elements that have their own nonlinear behavior, independent of other elements. This behavior is typically characterized by an abrupt change in stiffness due to a change in status. Status means a contact surface element changing from open to closed. Element Nonlinearities provide various capabilities that are not normally possible with global Nonlinearities. In numerical simulation these Nonlinearities are addressed by the use of different types of nonlinear elements. Normally the element libraries in the software program include various nonlinear elements to address this behavior.

In the absence of significant thermal convection effects, the condition for conservation of energy within a solid or fluid medium may be expressed as:

In Cartesian coordinates:

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right) + Q = \rho C_p \frac{\partial T}{\partial t} \qquad (2.21)$$

In cylindrical coordinates:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(kr\frac{\partial T}{\partial r}\right) + \frac{1}{r^2}\frac{\partial}{\partial \theta}\left(k\frac{\partial T}{\partial \theta}\right) + \frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right) + Q = \rho C_p \frac{\partial T}{\partial t} \qquad (2.22)$$

Where:

T - temperature C_p - heat capacity

K - thermal conductivity ρ - density

Q - heat generation rate per unit volume

x,y,z coordinate directions t – time

Most branches of modern technology involve heat transfer rate as a significant factor at some stage in the design. From the earliest times, scientists and engineers have made use of the fact that heat will flow naturally, from a hot body to a cold body, without mechanical aid. But it is only in recent times with pressure to operate components near

the temperature limits of available materials, that the heat transfer process has tended to become a controlling factor in design.

The thermodynamic definition of 'heat' is energy transfer between communicating systems, arising solely from a temperature difference. Thus heat transfer is strictly a phenomenon occurring only at boundaries of systems, and heat transfer elsewhere in a system is more correctly a redistribution of internal energy within the system. The three modes of heat transfer are conduction, convection, and radiation.

Some of the difficulties associated with modeling thermal process come from the high non-linearity of the problem resulting from temperature dependent material properties such as k(T), ρ(T), C_p(T), boundary conditions, and complex heat generation rate. Specifying boundary conditions accurately is quite difficult due to high non-linear heat transfer mechanism occurring at the surface of the component, irregularities caused by intermetallic fusions at inter-connections etc. A simple but efficient method uses a comprehensive boundary heat transfer parameter, generally being the overall heat transfer coefficient. It incorporates all possible heat transfer mechanisms occurring on the boundaries of the component, such as convective and radiative heat transfer. Mixed boundary condition is normally applied in modeling as follows:

$$h_o (T_{surf} - T_f) + k\frac{\partial T}{\partial n}\Big|_{ref} = 0$$

where:

h_o - overall heat exchange coefficient

T_{surf} - surface temperature

T_f - bulk temperature :

Specifying initial conditions is normally straightforward since most equipment start with a uniform temperature such as room temperature. Generally the initial condition is expressed as:

$T_t = 0 = f(x,y,z)$

or $T_t = 0 = f(r, 0, z)$

Equation Solver The finite element approach to solving continuum mechanics problems involves first dividing the solution domain into small subregions or finite elements. A mathematical model consisting of discrete regions (elements) connected at a finite number of points (nodes) represents the system to be analyzed. The primary unknowns in an analysis are the degrees of freedom (DOF) for each node in the finite element model. The DOF may include displacements, rotations, temperatures, pressures, velocities, etc.; and are defined by the elements attached to the node. Corresponding to the degrees of freedom, stiffness (or conductivity), mass, and damping (or specific heat); matrices are generated as appropriate for each element in the model. These matrices are then assembled to form sets of simultaneous equations that can be processed by the solver.

The degrees of freedom set present in the assembled matrix at any given time is known as the wave front, which expands and contracts as degrees of freedom are introduced to and from the matrix. After the wave front has passed through all the elements and the response of each degree of freedom has been computed, post processing can be used to display integrated results for the entire model.

Different codes have different types of solvers based on the problem being solved. In this study a direct solver from the ANSYS program is used. Direct solvers, such as the frontal solver, calculate exact solutions for a set of linear simultaneous equations. A frontal solver simultaneously assembles and solves an overall stiffness matrix made up of the individual element matrices. This procedure progressively moves through the model, element by element, introducing the equations corresponding to the particular element's degree of freedom. At the same time, degrees of freedom are solved and deleted (using Gaussian elimination) from the matrix as soon as possible.

Element Selection In finite element method element selection is one of the key decisions to be made in solving the problem accurately. Depending on the dimensions, finite elements can be divided into the following three categories and basic element types:

1. One-dimensional: Line elements - Truss, beam and boundary elements.
2. Two- dimensional: Plane elements – Plane stress, plain strain, Axi-symmetric, membrane, plate and shell elements.

3. Three dimensional: Volume elements – Tetrahedral, hexahedral, and brick elements.

Most commercial finite element codes have an element library with many different one-, two-, and three- dimensional elements. The number of different types of elements available, under the above three basic categories depends on the sophistication and cost of the computer code. Many have options that allow further specialization of the element formulation in some manner, effectively increasing the element library. Continuous research is being done in developing new elements worldwide. The complexity of an element increases as the number of degrees of freedom are increased. As the complexity of the elements and the total number of elements is increased the cost and the accuracy is increased and a compromise has to be made between them

Since element libraries vary in different computer codes, the discussion of details of elements used in this dissertation is limited to the above three categories. Details of elements used from the ANSYS library are in chapter 3.

2.3 THERMAL-STRUCTURAL ANALYSIS

Most computer programs use two different approaches to determine the effects of temperature distribution on the structural response of the model. The first method involves performing two analyses in a series. A thermal analysis is first used to solve for the temperature distribution within the model from the given heat transfer boundary conditions. The temperatures from the thermal solution are then used as loads by the preprocessing and solution phases of a subsequent structural analysis of the model. The second method provides a simultaneous thermal-structural solution. This method uses coupled-field elements that have both temperature and displacement degrees of freedom. The user constructs the analysis model using these elements and specifies thermal and structural boundary conditions. In the solution phase, each iteration calculates both the thermal solution and the structural solution based on the temperature and displacement data from the previous iteration. With the simultaneous solution process, it is possible to couple complex heat transfer and structural problems, such as transient thermal and nonlinear dynamics analyses. This method is more effective in the study of interconnects, due to the fact that, large deformation may occur due to the

different rates of expansions of the interconnect materials, which may affect the conductivity matrix. In this study the first method is used in the ANSYS program simulation, and the second method is used in the IDEAS program simulation.

2.4 EFFECT OF MATERIAL PROPERTIES

Many of the materials used in circuit board design, have high CTE, and a high modulus of elasticity. The combined effect of this gives rise to high stress for the following reasons:

$$E = \frac{\sigma}{e} \qquad (2.26)$$

where E = Modulus of elasticity

σ = Stress (lb/in2)

e = Strain (in/in)

A high TCE results in higher expansion, and hence a higher strain. Thus in the above equation if the strain e is replaced by , α, the TCE, then

$$\sigma = E\alpha \qquad (2.27)$$

The above equation shows that a high modulus of elasticity E, and a high thermal coefficient of expansion α, will give rise to high stress in the chipboard and interconnect.

2.5 EFFECT OF WIRE DIAMETER

If a component fails, it is normally accepted to make the component stronger, by making it stiffer. However, in the case of multiple wires, it may not be true for the following reasons:

$$F = K_{wire}\, y \qquad (2.28)$$

Where F = force

K_{wire} = stiffness

Y = displacement

From equation 2.28 , if the displacement is kept constant, the force will be reduced if the stiffness or spring rate is reduced.

Also, $$K_{wire} = \frac{E\, I_{wire}}{L^3} \qquad (2.29)$$

Where E = modulus of elasticity
I_{wire} = moment of inertia of the wire
L = wire length

Where I_{wire} for wire is given by

$$I_{wire} = \frac{\pi D^4}{64} \qquad (2.30)$$

Equation 2.29 shows that decreasing the moment of inertia of the wire will rapidly decrease the wire stiffness. Equation 2.30 shows that the moment of inertial of the wire varies as the fourth power of wire diameter. Hence a decrease in wire diameter by a factor of two, would decrease the stiffness of the wire and the stresses in the wire by a factor of sixteen. Equation 2-29 shows that increasing the length L of the wire by a factor of two will decrease the stiffness of the wire, or the stress in the wire by a factor of eight. The wires are forced to bend back and forth during resonant condition. Hence, wire stiffness plays a major role for a specific dynamic displacement generated by the resonant frequency and acceleration level.

2.6 VIBRATION ANALYSIS

The advent of high speed digital computers, and the simultaneous development of finite element method, enables to-days engineers to conduct numerically detailed vibration analysis of complex systems; displaying thousands of degrees of freedom. The mathematical modeling of vibration problems are discussed in many references, and the following are from Rao [46], Steinberg [54], Timoshenko, Young, Weaver [57], Tse, Morse, Hinkle [59].

Vibration analysis consists of modal analysis, and harmonic analysis. Modal analysis is used to determine the natural frequencies and the mode shape of the component. In addition the results of the modal analysis is used in harmonic analysis. The steady state response of a component to a sinusoidally varying forcing function is determined by Harmonic response analysis.

2.6.1 MODAL ANALYSIS

The following equation of motion describes free (unforced), damped, or undamped vibration:

$$[M]\{\ddot{u}\} + [C]\{\dot{u}\} + [K]\{u\} = 0 \qquad (2.23)$$

For modal analysis the damping term $[C]\{\dot{u}\}$ is ignored and the equation reduces to:

$$([K] - \omega^2 [M])\{\bar{u}\} = 0 \qquad (2.24)$$

where ω^2 (the square of natural frequencies) represents the Eigen values, and $\{\bar{u}\}$ (the mode shapes, which do not change with time) represents the Eigen vectors. There are several techniques available for modal extraction. The technique used in this study is discussed in section 3.6.1.1.

2.6.2 HARMONIC ANALYSIS

The governing equation for harmonic response analysis is a special case of the general equation of motion, in which the forcing function, {F(t)}, is a known function of time varying sinusoidally with a known amplitude, F_0, at a known frequency ω (and phase angle, ϕ):

$$\{F(t)\} = \{F_0 (\cos(\omega t + \phi) + i\sin(\omega t + \phi))\} \qquad (2.25)$$

The displacement can vary sinusoidally at the same frequency, ω, but are not necessarily in phase with the forcing function. There are several methods available to do harmonic response analysis. The method used in this study is discussed in section 3.6.2.

The attachment of components on the board, reinforces or increases the stiffness of the board in the immediate region of the component, according to Pecht [41]. The stiffness and mass effects are functions of component size, thickness, material, and attachment technology. Also, the location where component is attached to the board is important. Components should typically be attached to the edges of the board than at the

center, where there is greater stiffness. In vibration analysis it is not the stresses in the board which are important, but the outer fiber strains, according to Pecht [41]. The strains are a measure of the elongation of the board, and it must be accounted for. The component attached to the board must be able to accommodate this elongation.

There are two types of losses due to internal strains developed during bending deflections of the board: friction losses that are generally due to relative motion between high pressure interfaces such as mounting surfaces, stiffening ribs etc. These energy losses are greatest when the deflections are greatest, and smallest when the deflections are smallest. Since high frequencies have smaller deflections, they will also have less damping. This would mean high frequencies will have higher transmissibility at resonant condition. Most PWB's have fundamental resonant frequencies between 200 and 300 Hz.

2.7 COMBINED VIBRATION AND THERMAL LOAD

The electronic component is normally subjected simultaneously to vibration and thermal cycles. For an accurate account the effects of vibration strain, and thermal strain should be superposed appropriately , according to Pecht[41] . One of the simplest and most widely used superposition scheme is Miner's rule according to Miner [35]. Miner assumes that every structural member has a useful fatigue life and that every stress cycle uses up a part of this life. When enough damage has been accumulated due to stress/strain cycling, the effective life is exhausted and the member fails. Effective superposition is possible once the strain histories from vibrational and thermal loading are quantified. Most electronic devices are subjected to random vibrations as shown schematically in Figure 2-4[41]. The associated stress or strain amplitude in the solder joints can be assumed to have a Gaussian distribution about the rms amplitude near the PWB's natural frequency. For properly designed electronics, vibration strain amplitudes that exceed the 3σ values are considered to cause fatigue according to Markstein[33]. Some feel that 3σ is not conservative enough and use 2.2σ according to Steinberg[54]. Strain amplitudes above the 3σ value occur only 0.135% of the time in the Gaussian distribution, and thus the PWB has to be designed to handle only 0.135% of the total number of vibration cycles.

2.7.1 STRAIN AND SOLDER JOINT FATIGUE CALCULATIONS

The strain developed in the solder joint due to thermal cycling is a key design parameter because it drives the rate of solder joint fatigue, which is the limiting life cycle factor, according to Morris [36]. The Coffin-Manson fatigue relationship discussed in Manson [32], Eckel[13], recommend the following form to give a reasonable representative fit to experimental solder fatigue data in shear.

$$N_f(v, T_{max}) = C\,(\Delta e^2_p)\, v^{1/3} \exp(1.87\text{-}0.0134\, T_{max})$$

where:

N_f = number of fatigue cycle to failure

v = cyclic frequency

T_{max} = maximum excursion temperature

C = proportionality constant, approximately equal to 120

Δ_{ep} = is the plastic strain excursion, and is given by

$$\Delta_{ep} = ([L\,(I_U\,\Delta T_U - I_L\,\Delta T_L)] / 2t) \times 100, \%$$

where L is the largest dimension of the joint

I_U and I_L are the expansion coefficient of the upper and lower materials being soldered together, respectively.

ΔT_U and ΔT_L are the corresponding temperature excursions for the upper and lower surface, respectively, and t is the solder thickness.

From this relationship it can be seen that the fatigue life is increased quadratically, with a decrease in the strain range.

Hence any attempt to decrease the strain in solder joints will increase the reliability of the electronic equipment. The results of the numerical simulations are in chapter 3.

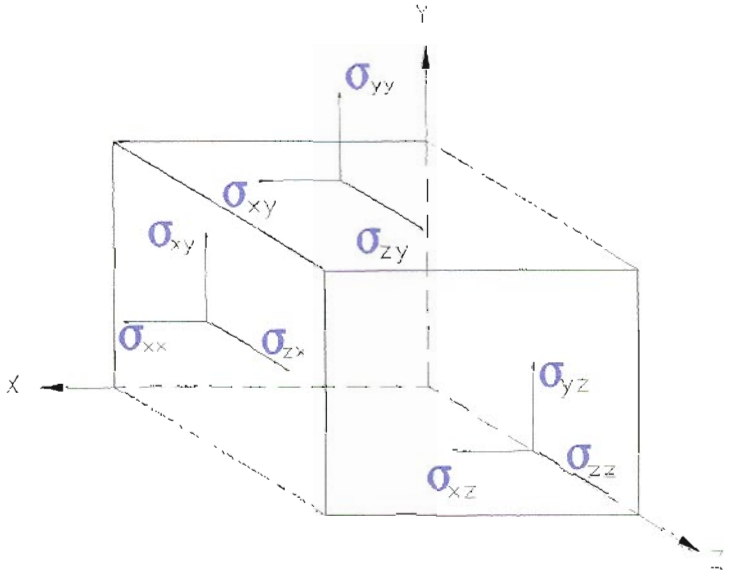


Figure 2-1 Cartesian Stress Components

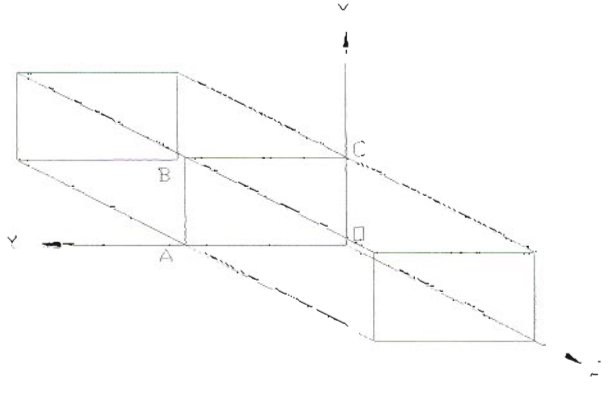


Figure 2-2 Plane Strain Approximation for a Prismatic Solid Body

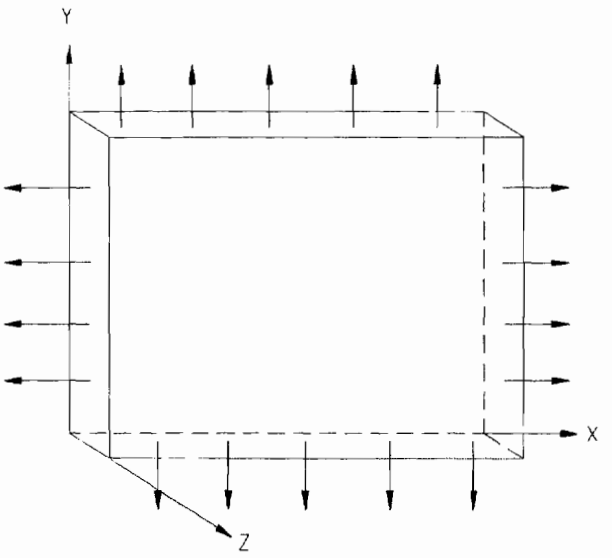


Figure 2-3 Plane Stress Approximation for a Thin Solid Body

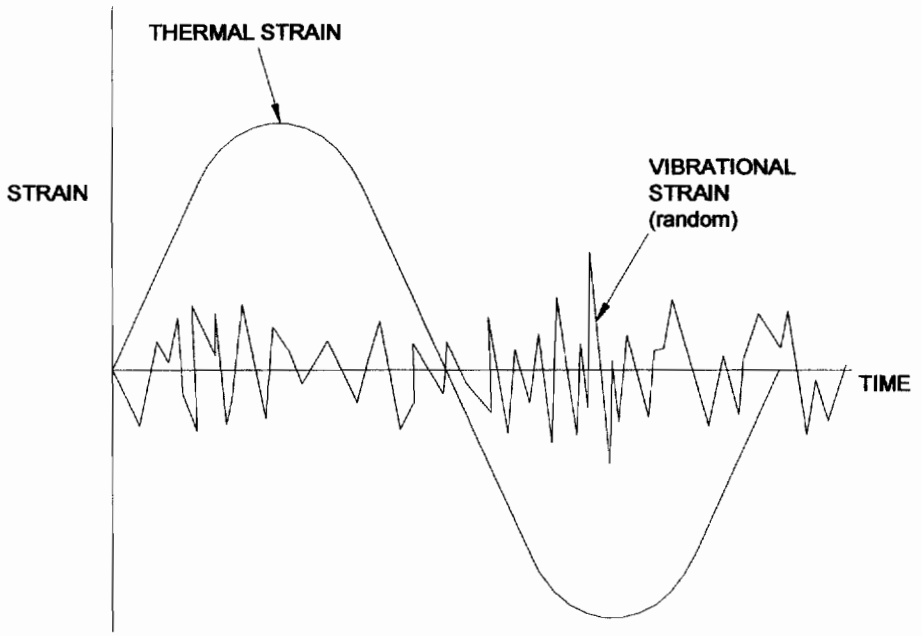


Figure 2-4 Schematic Representation of Vibrational and Thermal Strain (Adapted From Ref. 41)

CHAPTER 3

RESULTS OF NUMERICAL SIMULATION

3.1 NUMERICAL SIMULATION

One of the most important advantages of Finite Element Method simulation for electronic equipment is that one model can often be used for both thermal and structural analysis. This dual ability makes this technique very powerful, since it sharply reduces the amount of time required to analyze and design electronic systems. Not all finite element codes have the dual capability for performing both the thermal and structural analysis for electronic systems. A few codes which have some limited dual functions are NASTRAN, ANSYS, STRUDAL, COSMOS, and STARDYNE. For this analysis ANSYS version 5.6 is used, taking advantage of the dual ability.

Numerical simulations of the chip, board, wires, and solder joints are developed using both two-dimensional and three-dimensional models. The two-dimensional model does not yield the true stress state of the system, but it provides useful information on strains, stress and deformed shapes. The two-dimensional model requires little computing resources, and is developed very quickly. Further the two-dimensional simulation provides insight in to the loading conditions, boundary conditions, and symmetry conditions.

Structural nonlinearities cause the response of a structure or component to vary disproportionately with the applied force. Realistically, all structures are nonlinear in nature but not always to a degree that the nonlinearities have a significant effect on an analysis. Nonlinear FEM simulations sharply improve the accuracy of the stresses in the wires, and solder joints, when accurate plastic properties of the various materials are included in the computer model. But the drawback to nonlinear models is the large increase in the amount of computer resources, and time. The ANSYS program solves both static and transient nonlinear problems. Static analysis in the ANSYS program can also include nonlinearities such as plasticity, creep, large deflection, large strain, and

contact surfaces. A non-linear static analysis is usually performed by applying the load gradually so that an accurate solution can be obtained. In this dissertation only linear static simulation is used for structural analysis.

The drawing of the chip attached to the board by means of wire (Wire Interconnect) are shown in Figure 3-1. The chip attached to the board directly (Solder Interconnect) are shown in Figure 3-2. As explained previously to make the model simple, details such as adhesive layers, heat sinks, thermal vias have been omitted. Details of the wire diameter (.05 mm), the distance between wires (.025 mm), length of wire (.076 mm), and the solder height (.05 mm) are shown in Figure 3-3. The material properties used are in Table 3-1.

3.2 TWO-DIMENSIONAL MODEL

Prior to carrying out the three-dimensional analysis, it is important to do an approximate preliminary analysis to gain some insights into the problem. To reduce the number of elements in the model, and the time required to develop the model, half symmetry of the original domain is made use in the two-dimensional simulation. An ANSYS analysis consists of three phases: preprocessing, solution, and post processing. In the preprocessing phase, data needed to perform a solution is specified. In the preprocessing stage the following are defined, and performed: coordinate system, element types, real constants and material properties, create solid models, mesh model, manipulate nodes and elements, and define coupling and constraint equations.

For the ANSYS analysis consistent units have to be used. The dimensions shown in Figures 3-1 – 3-3 are in millimeters, and the properties used in Table 3-1 is in metric units. Hence the dimensions were entered in meters. In ANSYS program there are three different methods for generating a model: importing, solid modeling, and direct generation. For this simulation direct generation was used.

Thermal Analysis

For the thermal analysis Thermal Solid, PLANE55– 4 nodes, 2D space, DOF: TEMP elements was used for the chip and board. For the wires and solder conduction Bar, LINK33, 2 nodes, 3D space, DOF: TEMP was used. The meshed model for the wire interconnect are shown in Figure 3-4. The meshed model for the solder interconnect, with element PLANE55 used for the solder thickness, are shown in Figure 3-5. The ANSYS program provides four types of meshing: extrusion, mapped, free (or automatic), and adaptive. For this simulation initially free meshing was tried, and it was found to be coarse. Hence, mapped mesh was used. Uniform temperature of 135°C was prescribed to the chip area and a uniform temperature of 22°C was prescribed to the bottom of the board. No boundary condition was prescribed to the symmetry boundary condition, since it was assumed to be adiabatic boundary condition. The results of the thermal analysis for the wire interconnect are shown in Figure 3-6. The results of the thermal analysis for the solder interconnect are shown in Figure 3-7.

The results show that the temperatures of the solder interconnection is on an average 50^0C higher than the wire interconnection.

Structural Analysis

As mentioned previously, in ANSYS the thermal analysis model was used for structural analysis as well. For this change over used a new name for the job name, and in the preprocessor element type, the selected element type was switched. ANSYS selects equivalent element type from thermal to structural analysis. However, for this simulation, the automatic switch over selection of Spar-LINK8 for the wires was not suitable, since this is a truss element and does not have bending stiffness. Hence, for the wires and the solder connecting the wires, Elastic Beam-BEAM3, 2 nodes, 2D space, DOF:UX,UY,ROTZ was used.

For the structural analysis the temperature distribution obtained from the thermal analysis was applied. At the bottom of the plate the boundary condition was stipulated as fixed, no rotation, no displacement. The symmetry boundary condition was no rotation in z-direction, and no displacement in the x-direction. The initial simulation was performed in the plane stress condition. However, when the results was compared with the three-

dimensional solution, it became clear that for the two-dimensional geometry, the plane strain condition applied. The rationale was that the plain stress condition does not allow any stress in the z-direction. The results of the structural analysis for the wire interconnect displacement are shown in Figure 3-8, and the Von Mises stress are shown in Figure 3-9. The stress distribution in the solder joints, and wires only are shown in Figure 3-10. The results for the solder interconnect, displacement, are shown in Figure 3-11, and the Von Mises stress are shown in Figure 3-12.

The results show that the average Von Mises stress in the wire interconnect is 0.1 MPa compared to average Von Mises stress of 37.8 MPa for the solder interconnect.

3.3 THREE-DIMENSIONAL MODEL

A finite element model using three-dimensional solid elements may look the most realistic. However, this type of model also requires more elements, which implies more mathematical equations and therefore requires more computational resources and time. As in the two-dimensional model, symmetry is used, in order to reduce the computational requirements to a minimum. In this simulation quarter symmetry is used. The boundary condition must be examined carefully when symmetry is used.

Except the wires, the three-dimensional model was extruded from the two dimensional model. For extruding, the thermal solid-SOLID70, 8 NODES 3D space, DOF:TEMP was used. This element was used because this was the only element with lower order. In order to do this a simple macro was written, which is a simple Do loop. The wires were copied from two-dimensional to three-dimensional, since the same LINK33 element was used.

Thermal Analysis-Wire Interconnect

The model was refined with further use of different elements. For areas near the wires, SOLID70 was replaced with Tetrahedral Thermal Solid-SOLID87, 10 nodes, 3D space, DOF:TEMP. For the transition between SOLID87 and SOLID70, Thermal Solid-SOLID90, 20 nodes, 3D space, DOF:TEMP was used. As mentioned before the wires, and the solder connections used LINK33 element. The mesh generated in the quarter

symmetry are shown in Figure 3-13. The same mesh, with a slightly enlarged view are shown in Figure 3-14.

The thermal boundary conditions were the same as for the two-dimensional simulation. Except that the whole chip volume was selected and a temperature of 135°C was prescribed, and for the board the bottom area was selected and the temperature of 22°C was prescribed. The two symmetry boundary conditions were as same as before, i.e. adiabatic boundary conditions. The results of the thermal analysis are shown in Figure 3-15.

Structural Analysis-Wire Interconnect

As in the two-dimensional case, the temperature from the thermal solution was used as loads for the structural analysis. As in previous models, the elements were switched from thermal to structural elements. The element switch over was as follows:

SOLID70 to Structural Solid-SOLID45, 8 nodes, 3D space, DOF: UX,UY,UZ

SOLID87 to Tetrhedral Solid-SOLID92, 10 nodes, 3D space, DOF:UX,UY,UZ

SOLID 90 to Structural Solid-SOLID95, 20 nodes, 3D space, DOF:UX,UY,UZ

LINK33 to Elastic Beam-BEAM4, 2 nodes, 3D space, DOF:
UX,UY,UZ,ROTX,ROTY,ROTZ.

. For the wires the DOF were set as follows:

1. No motion in to the symmetry plane, UZ=0, and UX=0
2. For all beam elements, the rotation about their own axis was prevented by fixing rotation about Y direction. This will not allow twisting, but can bend in X, Y directions.
3. The rotation of the beam element in the X and Y direction is tied to the nodes at the ends of the solid element. This holds the beam elements in place.
4. Beam 4 is a 3 noded element, i.e. in addition to the 2 nodes, it has an orientation node. The third node in the beam element is for the purpose of defining the element co-ordinate system. In addition to defining the ends of the beam, the cross section is defined by the 3rd node.

The quarter symmetry simulation for structural analysis, with the prescribed boundary conditions are shown in Figure 3-16. The results of the structural analysis, displacements

are shown in Figure 3-17, and the Von Mises stress are shown in Figure 3-18. The Z-direction stresses are shown in Figure 3-19, and the stresses in the solder joints and the wires are shown in Figure 3-20.

Thermal Analysis-Solder Interconnect

The wires and the solders at the end of the wires were deleted, and the solder area was created. As mentioned in section 3.3.1, the model was created with SOLID70, and SOLID87 with SOLID87 elements used to model the solder thickness. The thickness of the solder was equal to the total length of the wires and the solder thickness at the wire ends (.034 inch). This mesh is shown in Figure 3-21, and an enlarged view is shown in Figure 3-22. The boundary conditions were the same as explained in section 3.3.1 for the wire interconnect. The thermal results are shown in Figure 3-23.

The three dimensional model predicts a similar temperature difference of 50^0C higher in the solder interconnect compared to the wire interconnect

Structural Analysis - Solder Interconnect

The structural analysis was similar to the wire interconnection as explained in section 3.3.2, except that there was no BEAM4 elements. The solder area was modeled with SOLID92 elements. The boundary conditions are shown in Figure 3-24. The results of the structural analysis for the displacement is shown in Figure 3-25, and for the Von mises stress are shown in Figure 3-26. The stress in the Z-directions are shown in Figure 3-27.

The results show the average value for Von Mises stress distribution for the wire interconnect as 0.114 MPa, compared to 36.4 MPa for the solder interconnect.

3.4 DIFFERENT WIRE MATERIALS

Material properties play a critical role in system performance and in manufacturing process effectiveness. Packaging and interconnection structures are composites containing many different materials in close proximity. Thus, interfacial properties and materials compatibility factors are often more important than bulk

properties of the isolated materials. The dependence of the materials properties on the manufacturing process is also important.

Several relevant material properties effect the selection of wire material. Wire materials are selected based on electrical, thermal, structural, ease of manufacture, availability, corrosion resistance, and cost. The common material in use for wire-interconnect in industry today is aluminum. In this study the critical properties which effect thermal analysis are modulus of elasticity, thermal conductivity and CTE. The materials selected for research in this dissertation was based on the difference in the above mentioned properties, and their combined effect.

The three different materials studied are silver (Ag), gold (Au), and Beryllium copper (BeCu). The bulk properties of the materials selected for study are shown in Table 3-2. The results of thermal and structural analysis for the three-dimensional wire interconnect, using silver as the wire material is in sections 3.3.

Gold as Wire Material

The ANSYS program for thermal, and stress analysis were repeated for the three-dimensional wire interconnect simulation with only the wire properties changed.
The results of the thermal analysis are shown in Figure 3-28. The results of the structural analysis , displacement are shown in Figure 3-29, and the Von Mises stress are shown in Figure 3-30. The Z-direction stress are shown in Figure 3-31. The stress in the wire joints are shown in Figure 3-32.

Beryllium Copper as Wire Material

As in the above section the ANSYS program for thermal, and stress analysis were repeated for the three-dimensional wire interconnect simulation with only the wire properties changed. The results of the thermal analysis is shown in Fig. 3-33. The results of the structural analysis , displacement are shown in Figure 3-34, and the Von Mises stress are shown in Figure 3-35. The Z-direction stress are shown in Figure 3-36, and the stress in the solder joints, and the wires are shown in Figure 3-37.

The results show an average Von Mises stress of 0.114 MPa for silver, 0.078 MPa for Gold and 0.310 MPa for Beryllium Copper.

3.5 DIFFERENT WIRE DIAMETERS

Different wire diameters were used to simulate the wire interconnect for two reasons. First to determine the model capabilities to optimize wire size for the interconnect and second, to validate the numerical model. Since beam elements are were used to model the wires, changing the real constants of the beam element changed the wire diameter. Changing real constants essentially meant changing moment of inertia etc., which effects the stiffness. The results of the thermal analysis are shown in Figure 3-38. The results of the structural analysis displacement are shown in Figure 3-39, and the Von Mises stress are shown in Fig. 3-40. The Z-direction stress are shown in Figure 3-41, and the stress in the solder joints, and the wires are shown in Figure 3-42.

The results show a displacement of 1.41 μm for wire diameter 0f 0.05 mm compared to a displacement of 1.63 μm for wire diameter of 0.5 mm. The average Von Mises stress in the wires for the wire 0.05 mm was 0.114 MPa and for the 0.5 mm wire the average Von Mises stress was 0.351 MPa.

3.6 VIBRATION ANALYSIS

Electronic systems that are used in any vibration or shock environments will expose the electronic components to some level of vibration and shock. These levels may be amplified or attenuated, depending upon the characteristics of the dynamic system. When Printed Circuit Boards (PCB) are used in these electronic systems, the resonant frequencies of the PCBs are often excited, which forces the PCBs to bend back and forth. This motion forces the wires on the chip to also bend back and forth. This will lead to stresses and strains in the wire and solder joints. When enough stress cycles have been experienced, the fatigue life will be used up and cracks will develop in solder joints, and the wires, and failure will result.

Electronic components can be mounted in any location and in any orientation on a Printed Circuit Board (PCB). Smaller components, less than about one inch, very seldom cause any vibration problems, unless the component happens to be very tall and heavy, according to Steinberg [54]. Larger components, greater than about one inch, are where vibration problems start. The PCBs are usually of the plug in type which are guided along the edges to permit easy connector engagement. Under these conditions,

the edges of the PCB can be assumed as simply supported. Hence in this simulation the edges of the board was considered simply supported.

Vibration frequency and the acceleration levels vary depending on where the electronic system is being used. Typically in airplanes the frequency varies from about 3 to 1000 Hz, and the acceleration levels range from 1 G to about 5 G. Random vibration over a broad frequency range from 20 to 2000 Hz was found to be an effective screening test for military electronic systems, according to Steinberg[54] . Random vibration will excite all of the resonant frequencies within the frequency band at the same time, which would improve the quality of the screening. Using sinusoidal sweeps would likely excite one resonance at a time. In this simulation it was decided to use a sinusoidal-vibration input with a maximum acceleration input level of 7.0 G peak.

Modal Analysis

Modal analysis is useful for any application in which the natural frequencies of a structure are of interest. The electronic component should be designed to produce natural frequencies that will prevent the component from vibrating at one of its fundamental modes under operating conditions. Modal analysis is used to extract the natural frequencies and mode shape of a component. It is important as a precursor to any dynamic analysis because knowledge of the component's fundamental mode shapes and frequencies can help characterize its dynamic response. The results of this analysis also help determine the number of modes or the integration time step to be used in subsequent dynamic analysis. Additionally, some transient and harmonic solution procedures require the results of a modal analysis. The ANSYS program permits a pre-stressed modal analysis, as well as running a modal analysis following a large deflection analysis.

Two-dimensional - Wire Interconnect

Several numerical methods are available in ANSYS for extracting modes. These include the Block Lanczos, Power Dynamics, and the reduced methods. For this simulation, the Block Lanczos method was selected. The two-dimensional model created for the stress analysis was also used for the modal analysis, with symmetry boundary conditions as before. The board was simply supported at the end opposite to the

symmetry boundary condition. Five modes were extracted for each case. The results for the modal analysis of the wire interconnect are shown in the following figures:

First Mode - Figure 3-43 - frequency 3153 Hz
Second Mode - Figure 3-44 - frequency 6134 Hz
Third Mode - Figure 3-45 - frequency 12972 Hz
Fourth Mode - Figure 3-46 - frequency 20575 Hz
Fifth Mode - Figure 3-47 - frequency 52127 Hz

Two-dimensional – Solder Interconnect

The simulation was performed similar to the wire interconnect as described for the wire interconnect. The results for the modal analysis of the solder interconnect are shown in the following figures:

First Mode - Figure 3-51 - frequency 2917
Second Mode - Figure 3-52 - frequency 19837
Third Mode - Figure 3-53 - frequency 51358
Fourth Mode - Figure 3-54 - frequency 87414
Fifth Mode - Figure 3-55 - frequency 113600

Harmonic Response

Harmonic response analysis is used to determine the steady-state response of a component to a sinusoidally varying forcing function. This analysis type is useful for studying the effects of load conditions that vary harmonically with time. Harmonic analysis is done to make sure that the component can withstand sinusoidal loads at different frequencies. It also detects the resonant response of the system, including the effects of material damping. Three numerical methods are available to do harmonic response analysis in ANSYS program: full, reduced and mode superposition. In this simulation, the full method was used.

Two-dimensional – Wire Interconnect

For this simulation, a sinusoidal acceleration with a maximum value of 7G, and a damping ratio of 0.2 was used. The first modal frequency was determined from the above modal simulation results. The harmonic load was specified (over a range of Frequency 1 to Frequency 2 - to capture the response of the first mode) as a stepped load, meaning the full amplitude of the forcing function was applied at the start of the load step. After applying the harmonic load the solution process was started. To review the results, the time history post processor (POST26) was used. A node on the board was picked (node # 455), where the highest deformation was expected, and the degree of freedom was selected as UY. The values of Y-deflection, frequency, and phase are shown in Table 3-3. The plot of frequency vs amplitude are shown in Figure 3-48. From this plot the frequency was determined as 3016 Hz, at a phase angle of –84.5864, when the highest amplitude is 0.3445 μm. In order to review the displacements and stresses over the entire board, the general post processor (POST1) was used. The standard ANSYS program HRCPLX macro was used to combine the real and imaginary components of the solution. The displacement results are shown in Figure 3-49, and the stresses are shown in Figure 3-50.

The maximum displacement was found to be 1.96 μm and the maximum stress was found to be 14.4 MPa.

Two-dimensional – Solder Interconnect

This simulation was performed similar to the wire interconnect. A node on the board was picked (node # 132), at the same location as in the wire interconnect, where the highest deformation was expected. The degree of freedom was selected as UY. The values of Y-deflection, frequency, and phase are shown in Table 3-4. The plot of frequency vs amplitude is shown in Figure 3-56. From this plot the frequency at which the maximum response to the first mode occurs is determined as 2896 Hz This occurs at a phase angle of –85.9744, with a peak response amplitude of 0.11185 μm. In order to review the displacements and stresses over the entire board, the general post processor (POST1) was used, with the command HRCPLX. The displacement results are shown in Figure 3-57, and the stresses are shown in Figure 3-58

Three-dimensional – Wire Interconnect

The solution of the modal analysis of the model containing the wires required a significant amount of computational resources due to its size. The three available modal extraction methods available in ANSYS program, mentioned in section 3.5 were tried. Out of the three, Block Lanczos was the method used for the two-dimensional model. Power Dynamics (subspace technique) was designed specially for models that contain solid elements. The Reduced Method, is specially designed to handle when insufficient memory/disk space is encountered, however it can require the identification of a large number of master degrees of freedom. In this simulation, in each case, the 2 Gb memory available in the HP workstation was exceeded, hence the run was not successful.

Three-dimensional –Solder Interconnect

The simulation method used was similar to the two-dimensional model, except for the boundary condition of the board. The board was simply supported at the four edges. Figure 3-59 shows the boundary conditions. The problem was solved using Block Lanczos method. The results of the modal analysis for the solder interconnect are shown in the following figures:

First Mode - Figure 3-60 - frequency 5618
Second Mode - Figure 3-61 - frequency 22552
Third Mode - Figure 3-62 - frequency 23630
Fourth Mode - Figure 3-63 - frequency 40806
Fifth Mode - Figure 3-64 - frequency 55616

Harmonic analysis was not performed due to significant amount of computer resources required.

3.7 NUMERICAL MODEL VALIDATION

There are many ways to validate a numerical model. Model validation could be based on published data of other peers if available. Numerical experiments could be compared to results from different numerical methods, different mesh schemes, or different approaches. It is a good idea to compare the results from a full three-dimensional model and a 30^{o} slice out of the symmetrical model. This would help to understand the restraints that must be applied at the boundaries of the sliced model. There can be large changes in the stresses for what might appear to be minor changes in the boundary conditions or the loading conditions at the node points in the model.

In this study a full three-dimensional model of the wire interconnect could not be analyzed due to the limited availability of computing resources. Table 3-5, gives details of the numerical model statistics. Therefore, the number of elements, nodes, and DOF, for the quarter symmetry three-dimensional model, of the wire, and solder interconnect simulated using the ANSYS program. This indicates that full three-dimensional model of the wire interconnect would require large computer resources.

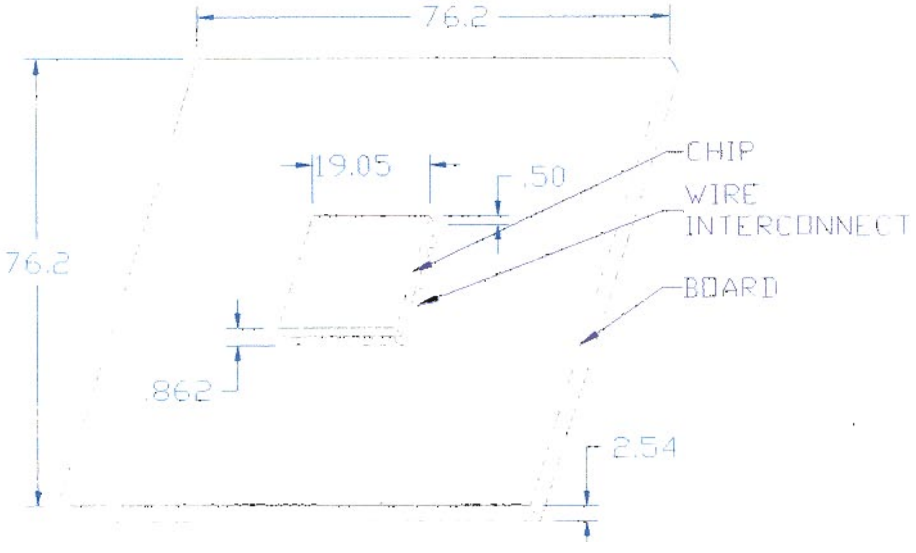
To cross check the results obtained using the ANSYS program, IDEAS[23] program was used. The IDEAS program is a finite element code, with limited capabilities. For this simulation IDEAS program version 6A was used. The IDEAS program, version 8 presently available has more capabilities than the version 6A used in this study.

The ANSYS simulation of the solder interconnect was validated by comparing the results with the published results of other researchers, namely Nakagawa, Sawa, Nakano, Hagiwara.[37]. The peak stress obtained for the solder interconnect of 36.4 MPa in this dissertation is in excellent agreement with the peak stress result of 35.8 MPa obtained by Nakagawa, Sawa, Nakano, Hagiwara [37].

Solder Interconnect

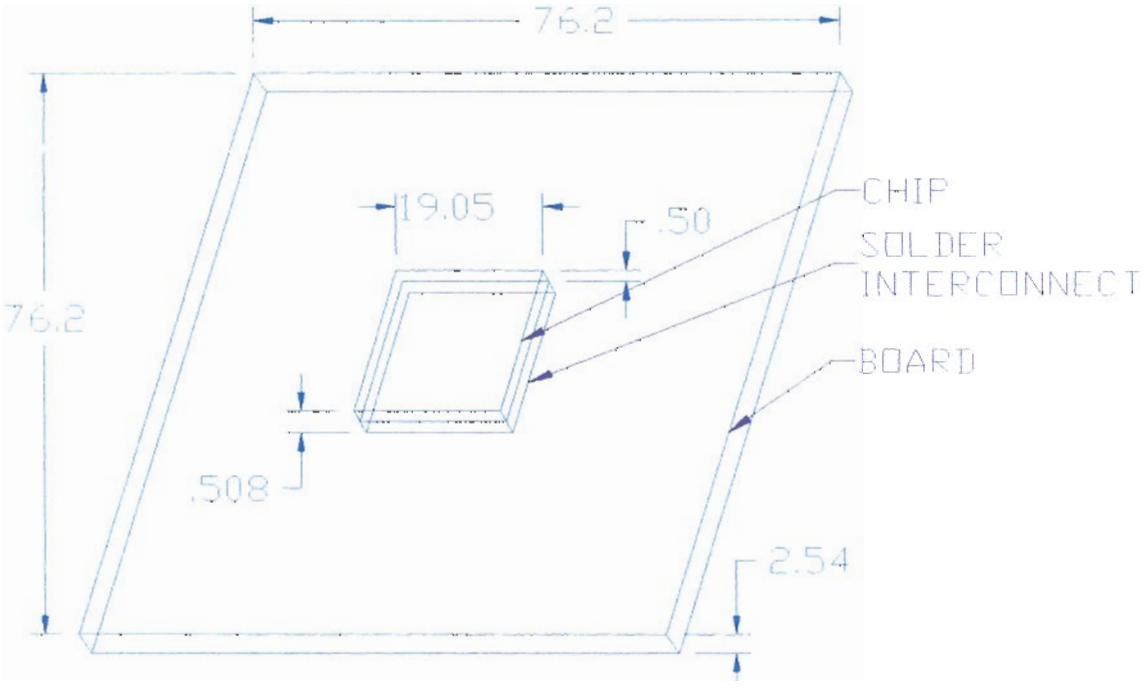
A full three-dimensional model of the solder interconnect was simulated using the IDEAS program. The model was created using brick elements, and the same model used for ANSYS simulation was used. The chip, solder, and board properties were as given in Table 3-1. The meshed model of the solder interconnect is shown in Figure 3-65. The side view of the stress distribution are shown in Figure 3-66, and the isometric view of the stress distribution are shown in Figure 3-67. Just as in ANSYS program, a full three-dimensional model could not be simulated using IDEAS program, due to the lack of significant amount of computer resources.

The results show an average Von Mises stress of 34.5 MPa for the solder interconnect.



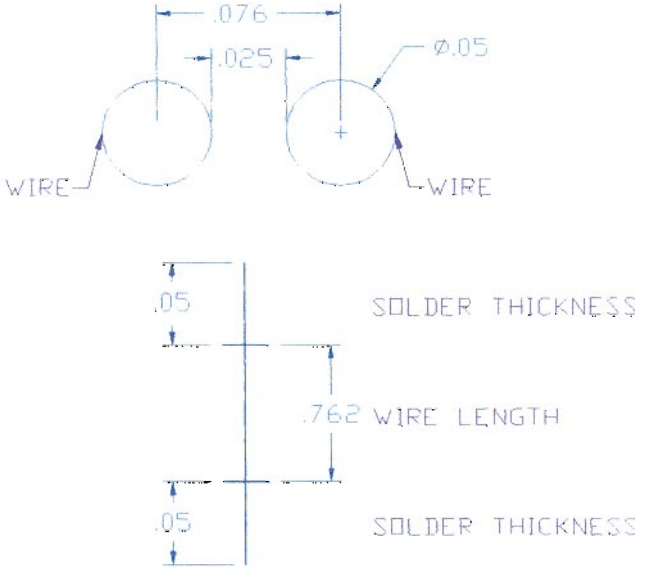
Note: Not to Scale - Dimensions in millimeters - Enlarged View

Figure 3-1 Chip Attached to Board by Wires - Wire Interconnect



Note: Not to Scale - Dimensions in millimeters - Enlarged View

Figure 3-2 Chip Directly Soldered to Board – Solder Interconnect



Wire Length = 0.762 mm Wire Diameter = 0.05 mm

Distance Between Wires = 0.025 mm Solder thickness = 0.05 mm

Note: Not to Scale - Dimensions in millimeters - Enlarged View

Figure 3-3 Details of Wire Interconnect

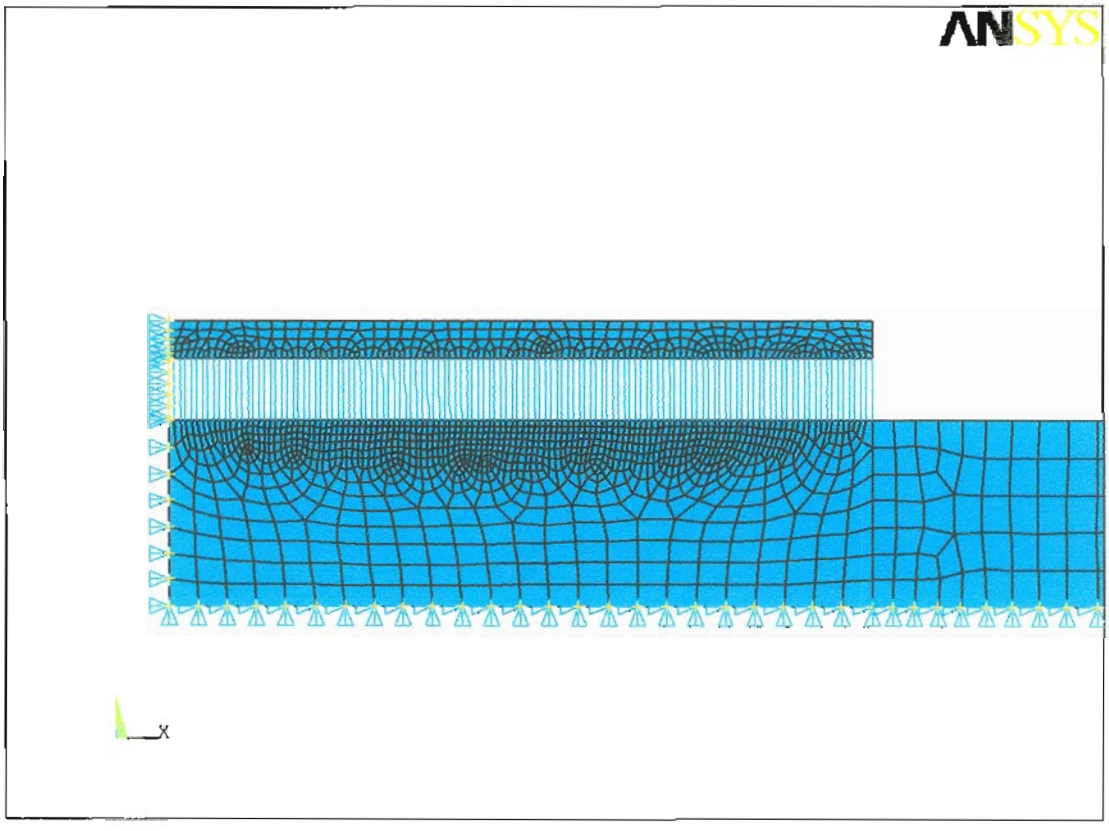


Figure 3-4 Mesh – 2D - Half Symmetry – Wire Interconnect

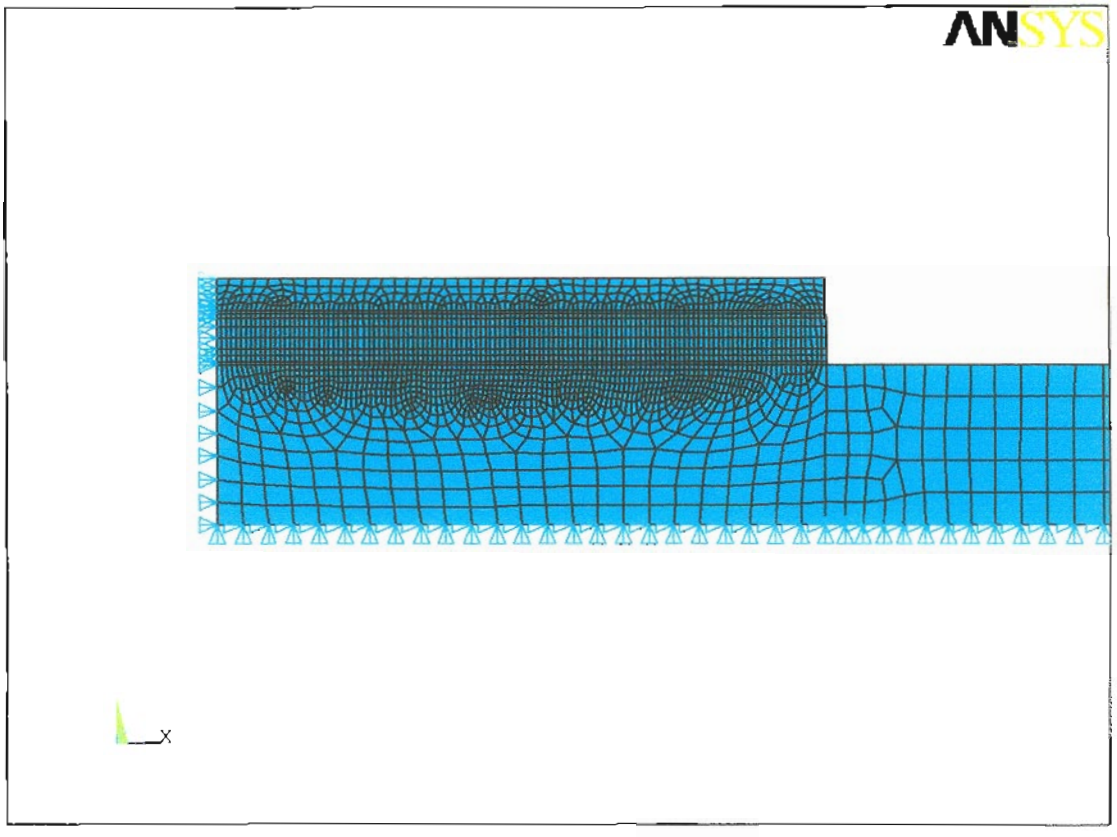


Figure 3-5 Mesh – 2D - Half Symmetry - Solder Interconnect

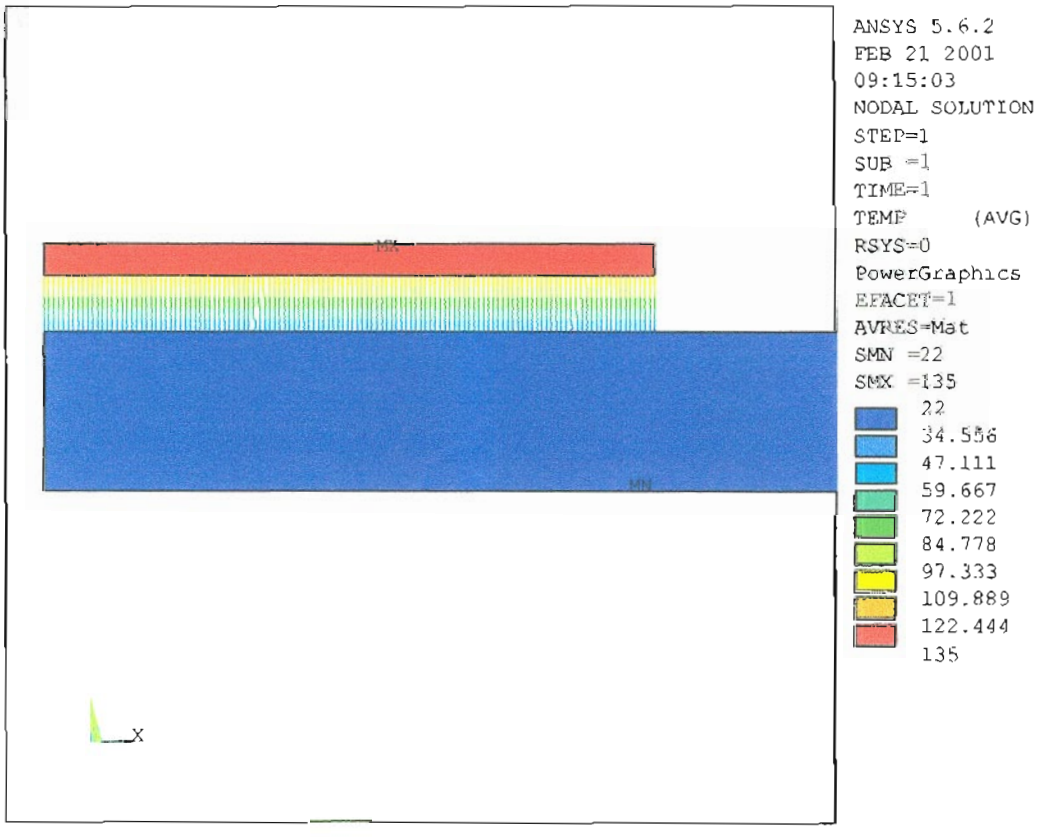


Figure 3-6 Temperature Distribution - 2D – Half Symmetry - Wire Interconnect

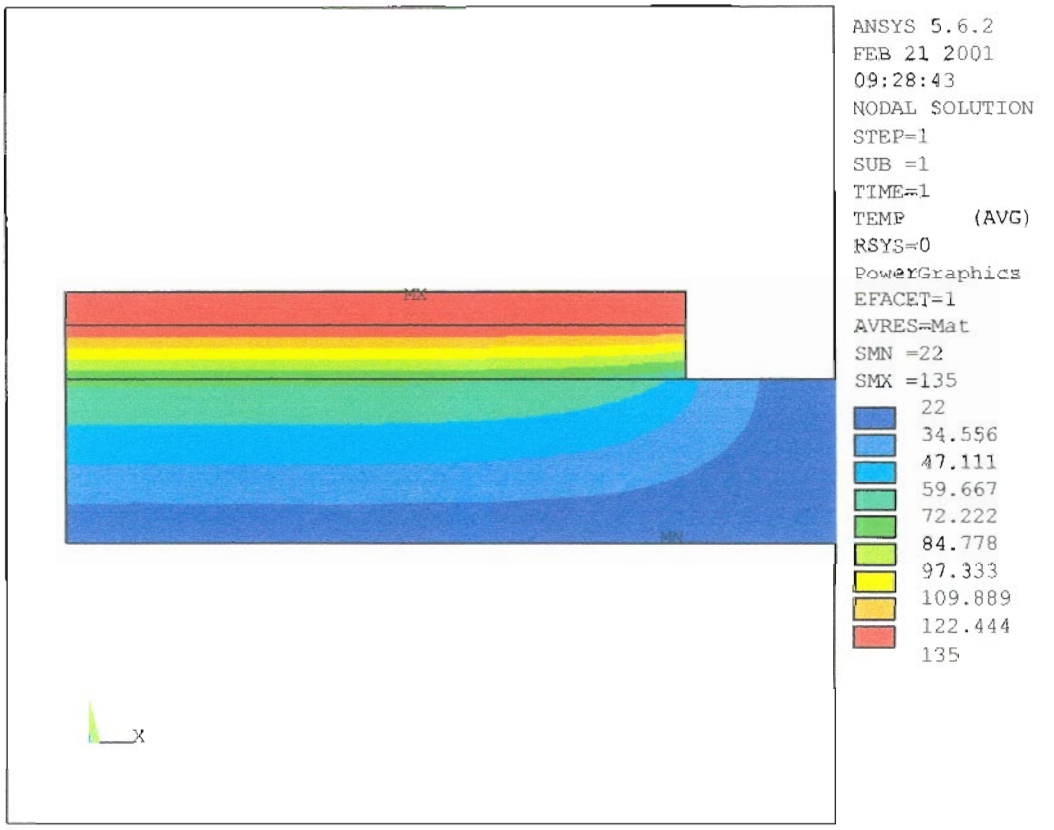


Figure 3-7 Temperature Distribution - 2D – Half Symmetry - Solder Interconnect

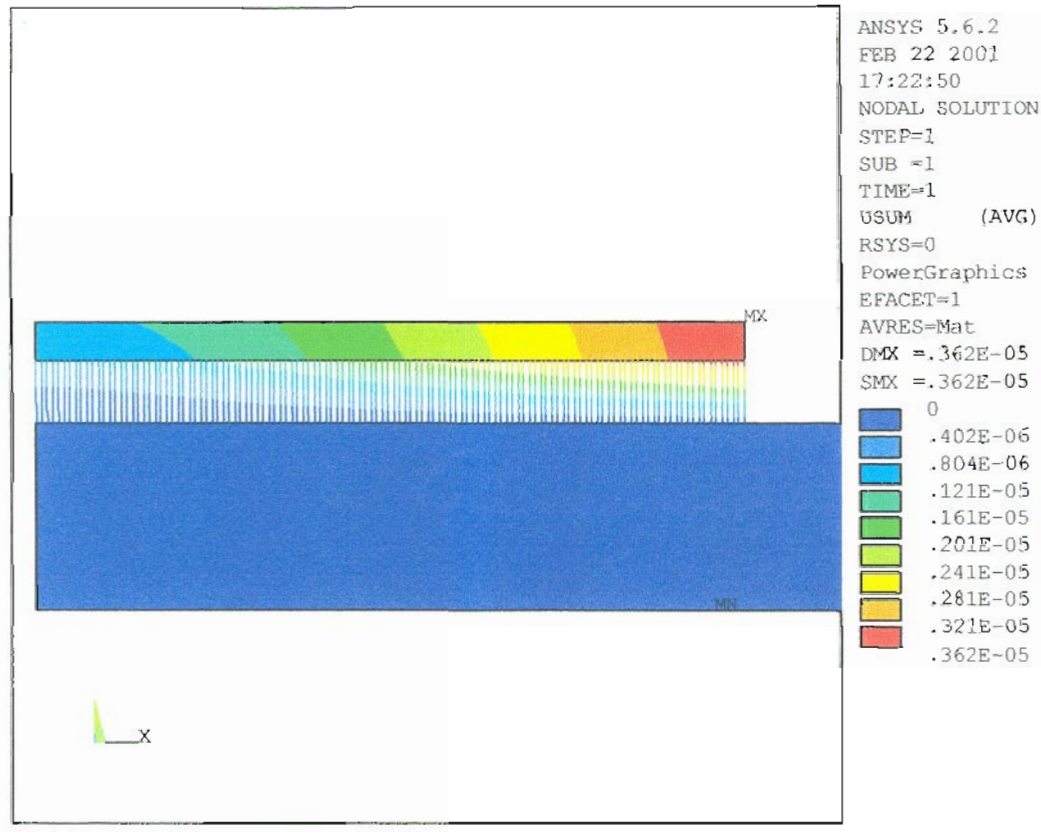


Figure 3-8 Displacements – 2D – Half Symmetry - Wire Interconnect

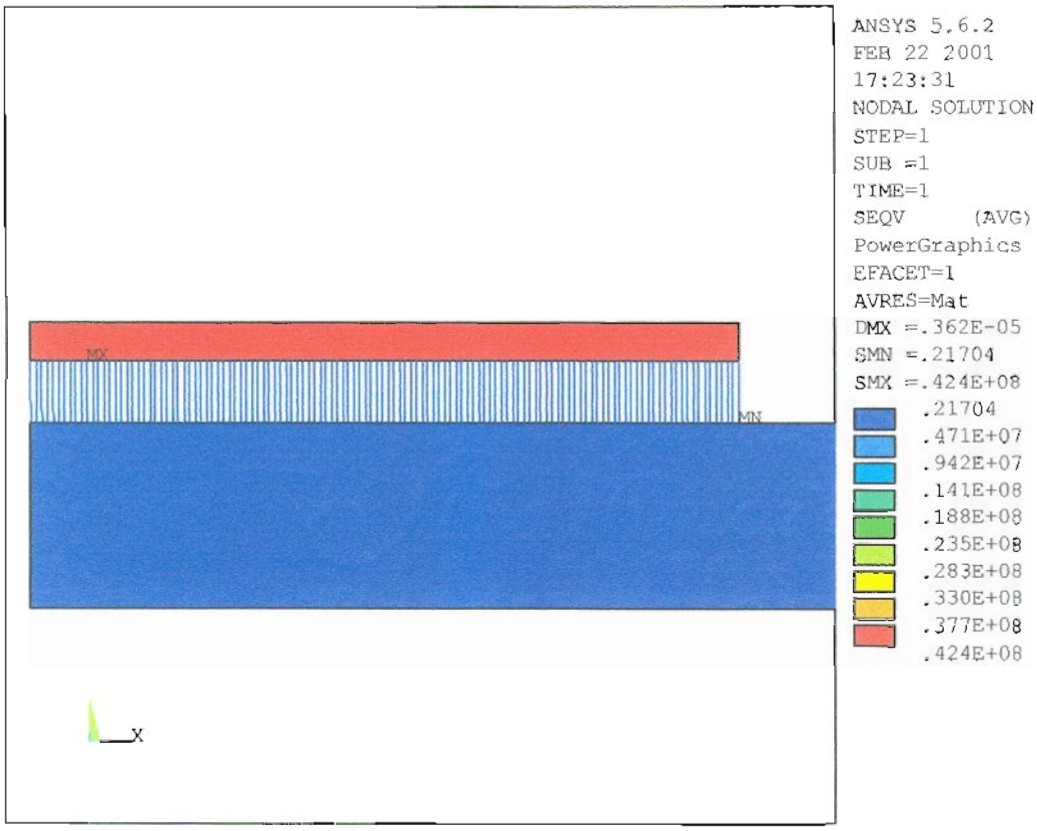


Figure. 3-9 Von Mises Stress - 2D – Half Symmetry - Wire Interconnect

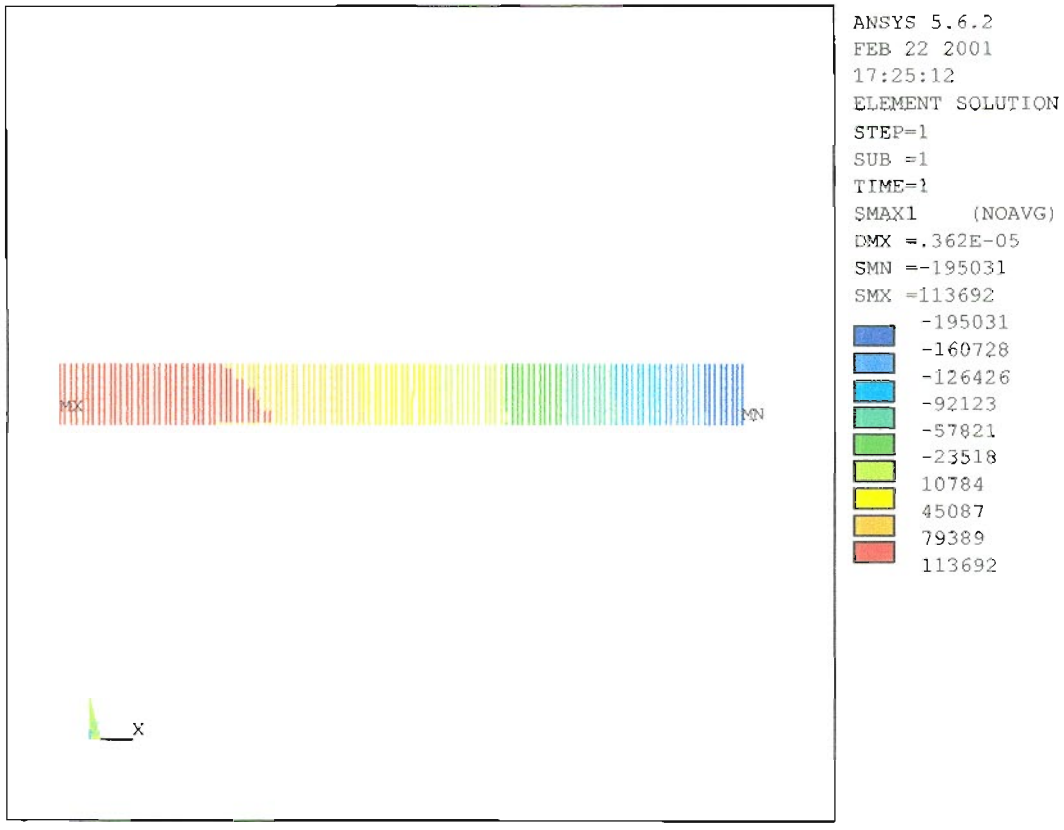


Figure 3-10 Wire Stress – 2D – Half Symmetry - Wire Interconnect

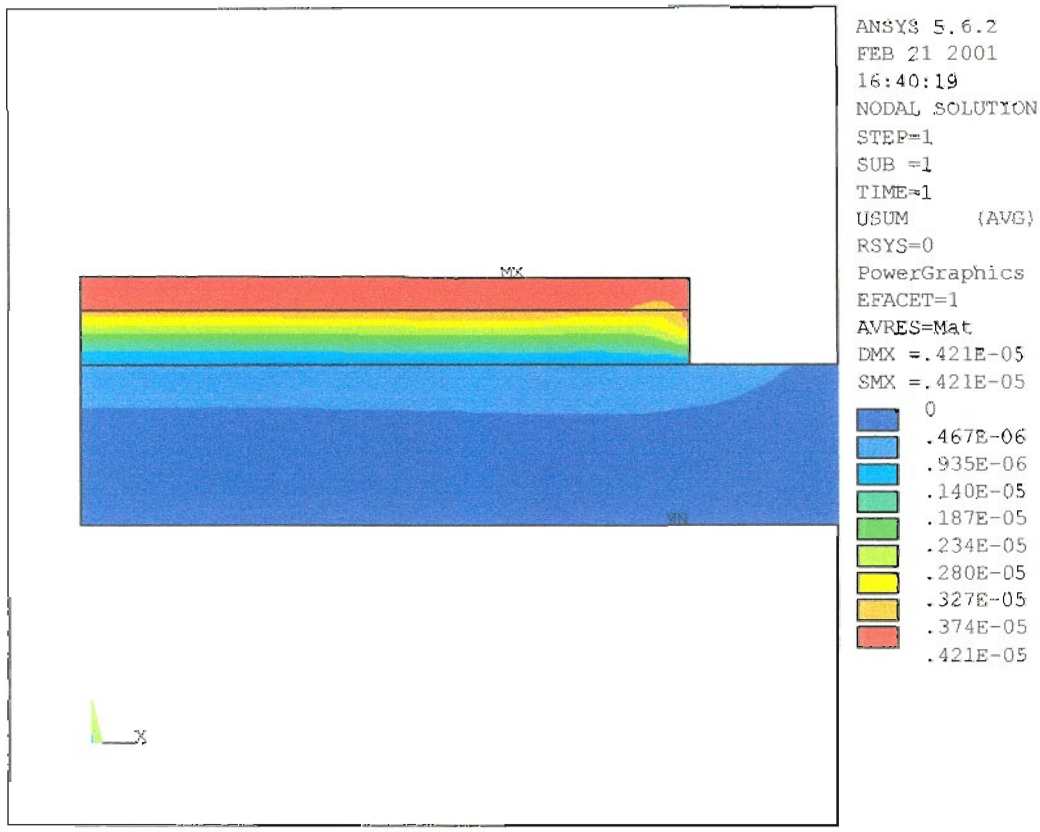


Figure. 3-11 Displacement – 2D – Half Symmetry - Solder Interconnect

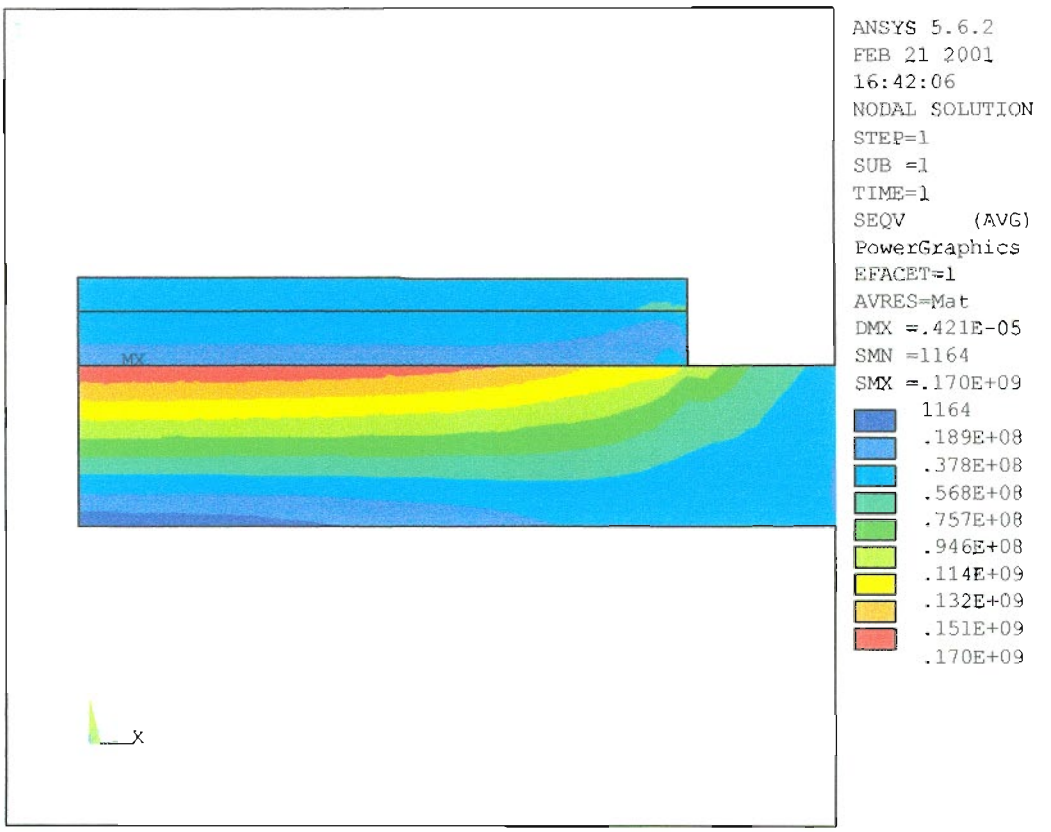


Figure 3-12 Von Mises Stress – 2D –Half Symmetry - Solder Interconnect

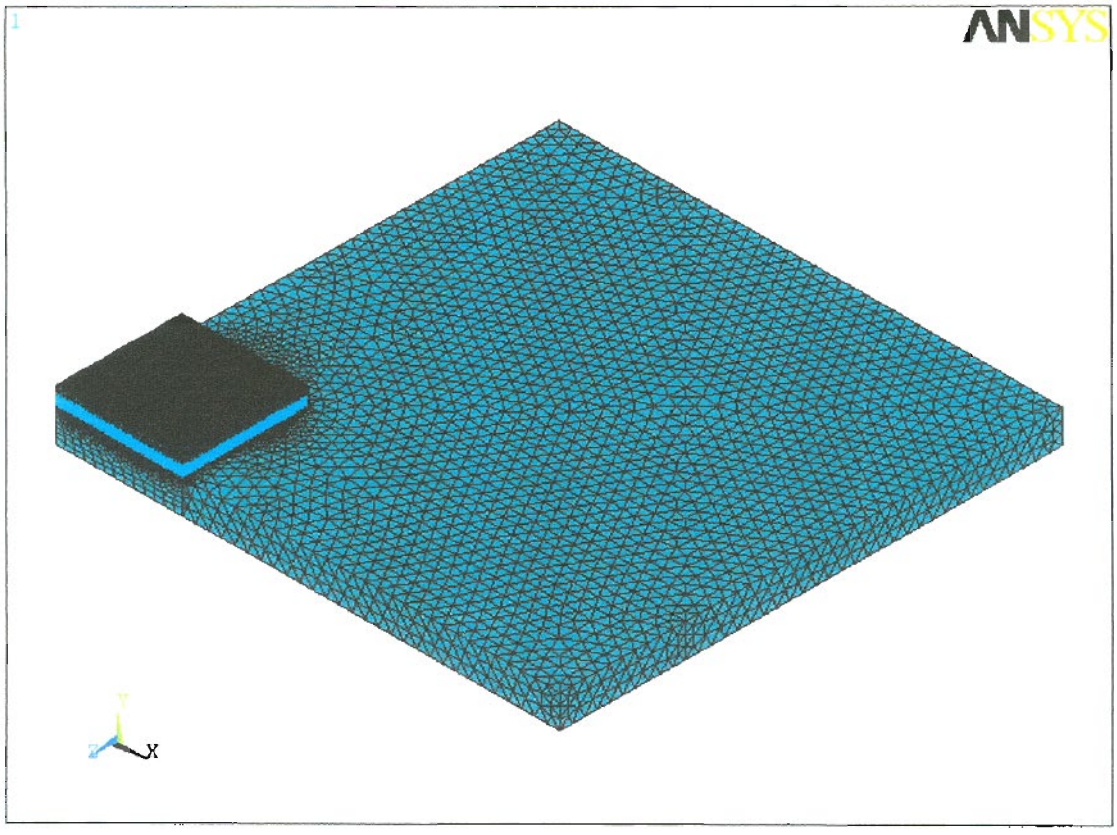


Figure 3-13 Mesh – 3D - Quarter Symmetry – Wire Interconnect

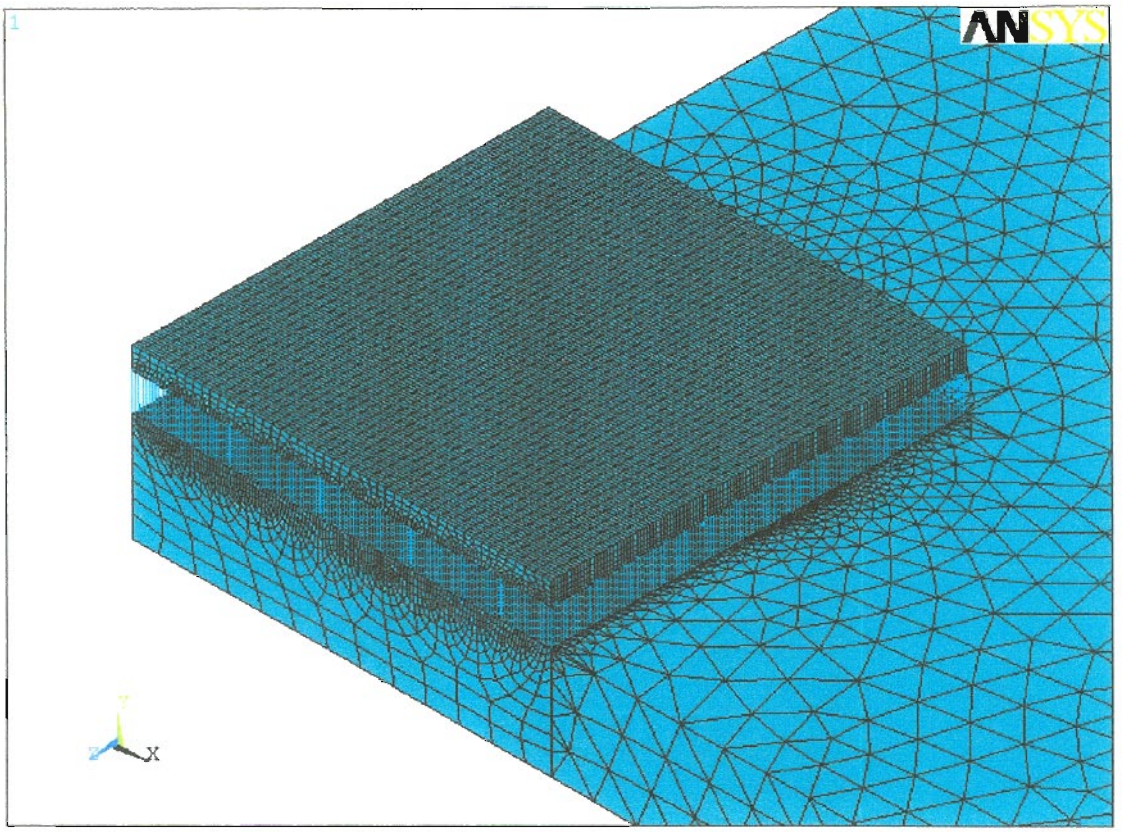


Figure 3-14 Enlarged Mesh – 3D - Quarter Symmetry – Wire Interconnect

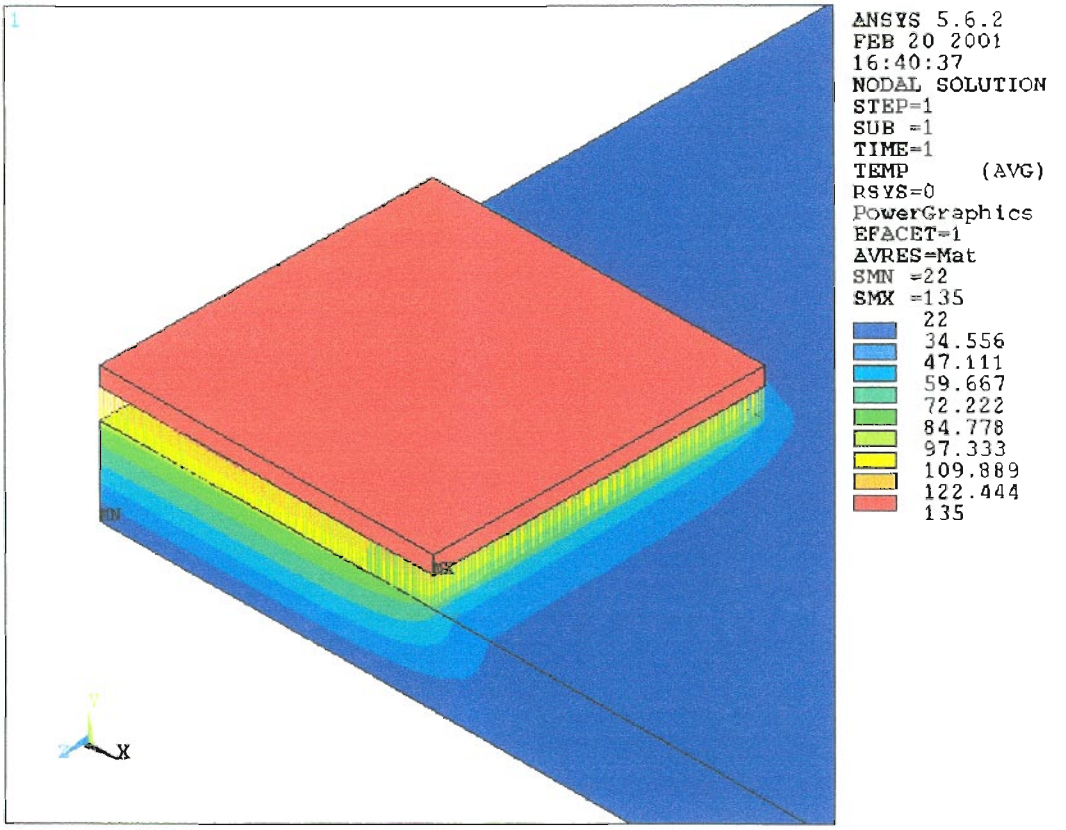


Figure 3-15 Temperature – 3D - Quarter Symmetry – Wire Interconnect
Wire Material – Silver, Wire Diameter = .05 mm

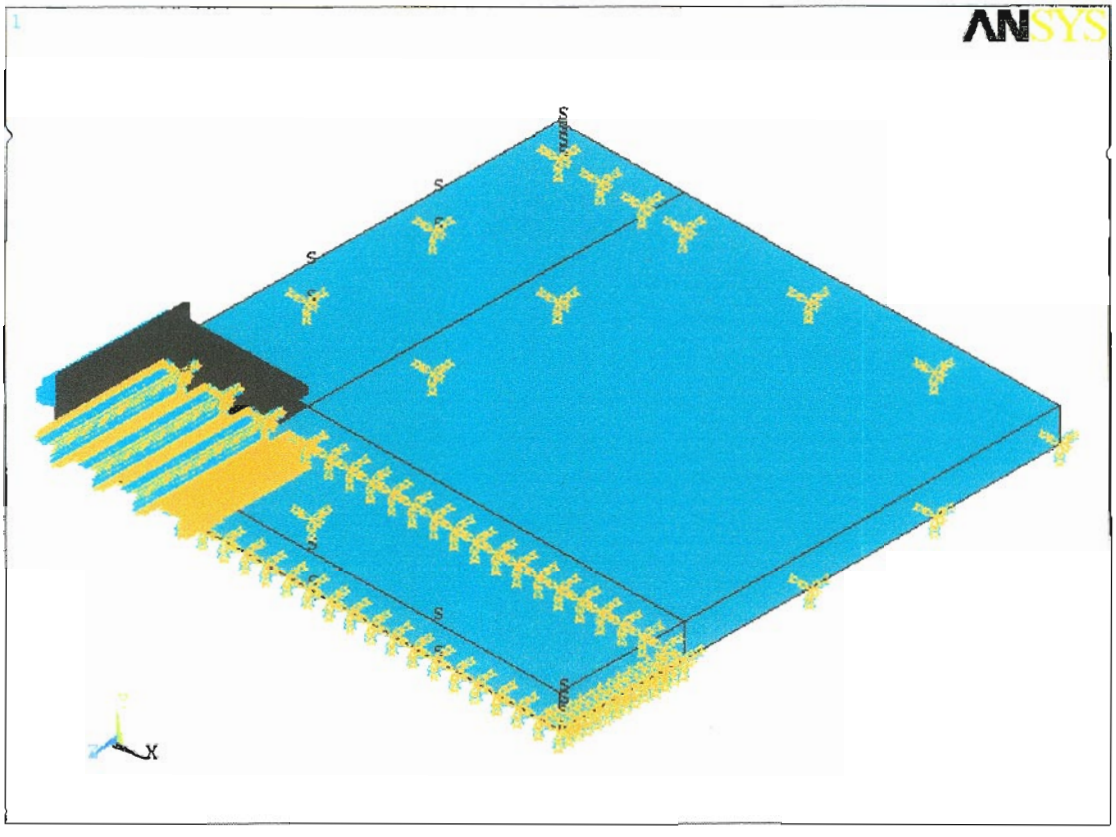


Figure 3-16 Boundary Conditions – 3D - Quarter Symmetry – Wire Interconnect

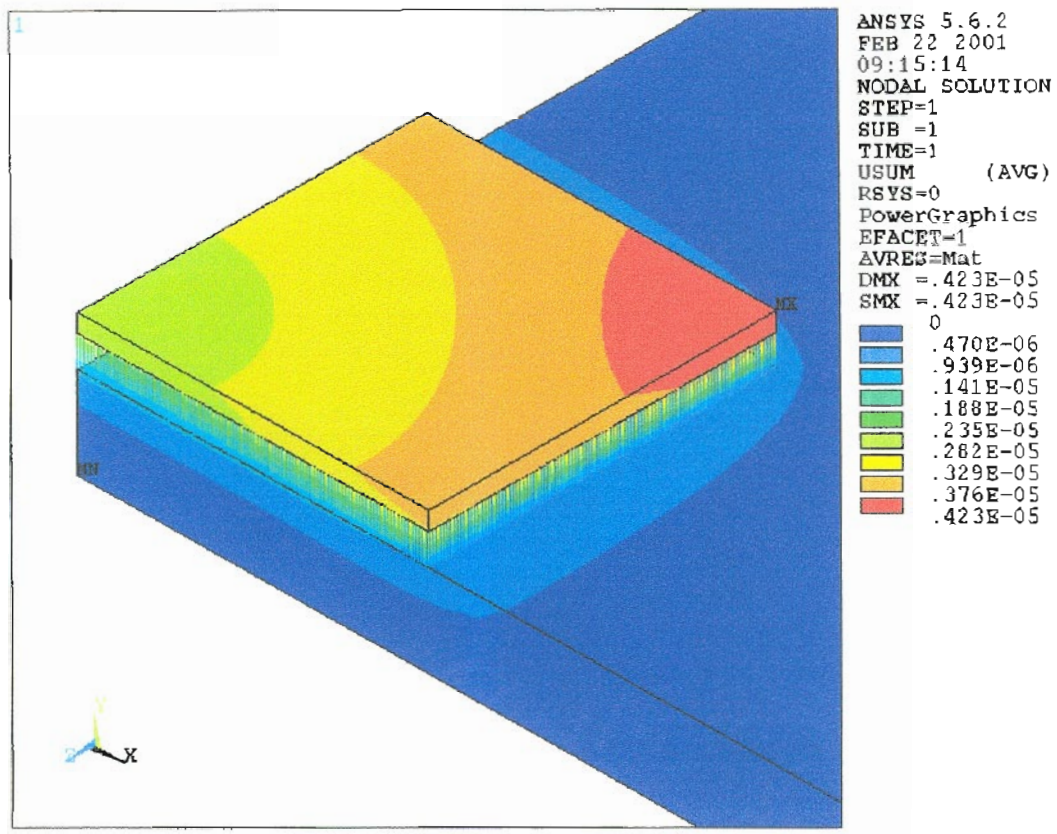


Figure 3-17 Displacement – 3D - Quarter Symmetry – Wire Interconnect
Wire Material – Silver, Wire Diameter = .05 mm

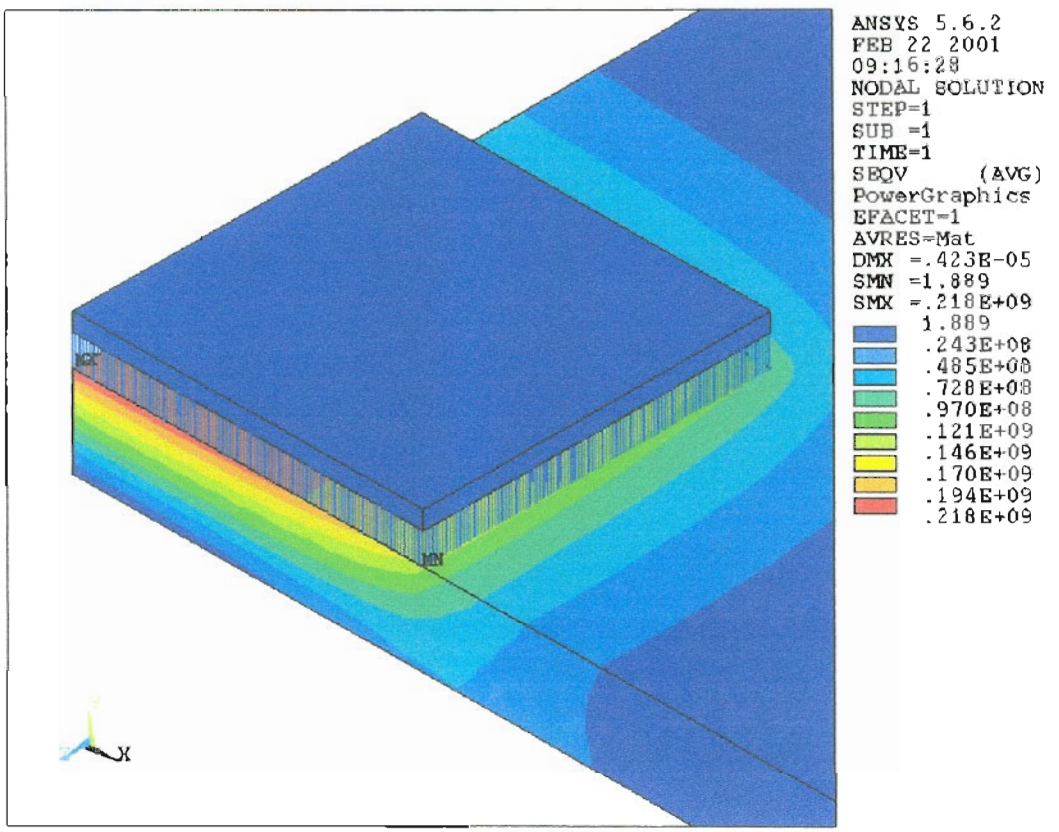


Figure 3-18 Von Mises Stress – 3D - Quarter Symmetry – Wire Interconnect
Wire Material – Silver, Wire Diameter = .05 mm

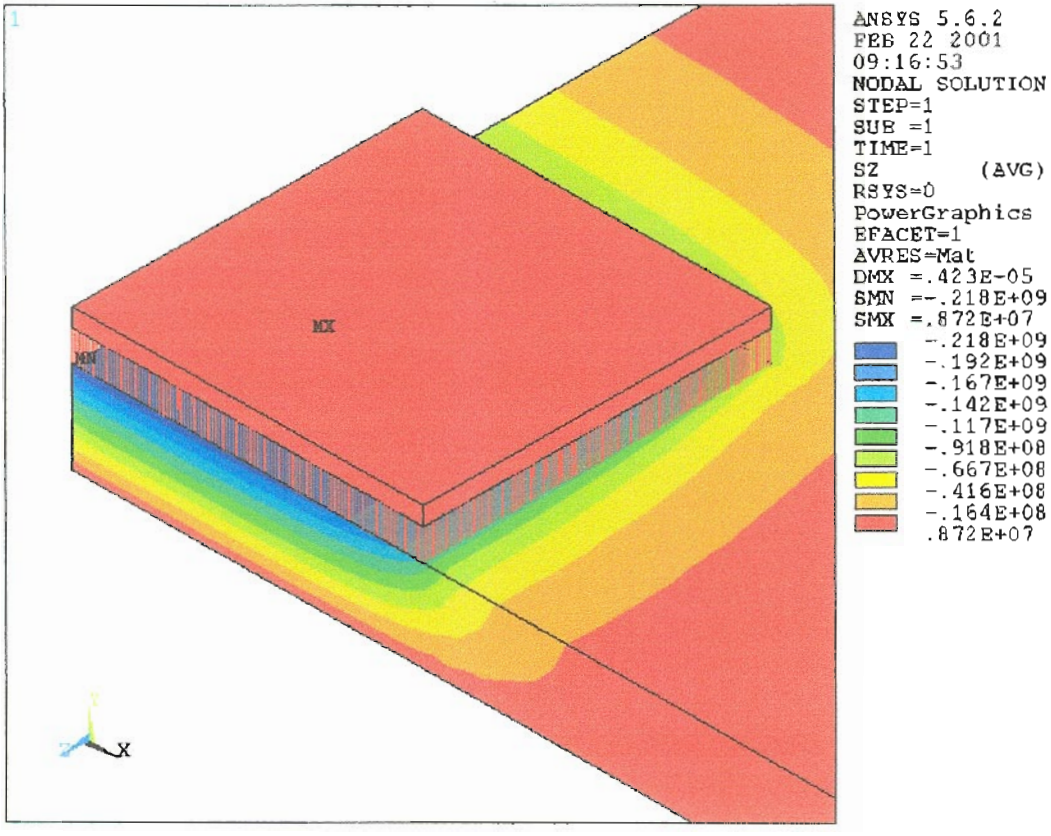


Figure. 3-19 Z – Direction Stress – 3D - Quarter Symmetry – Wire Interconnect Wire Material – Silver, Wire Diameter = .05 mm

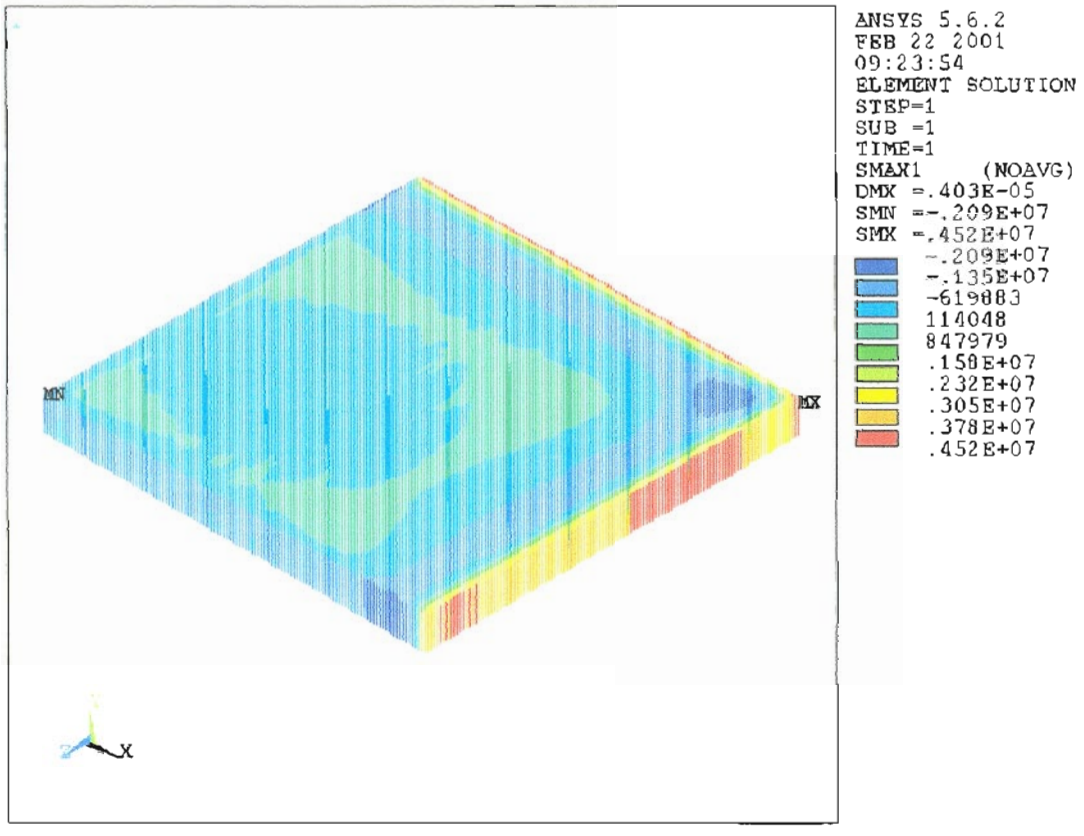


Figure. 3-20 Wire Stress – 3D - Quarter Symmetry – Wire Interconnect

Wire Material – Silver, Wire Diameter = .05 mm

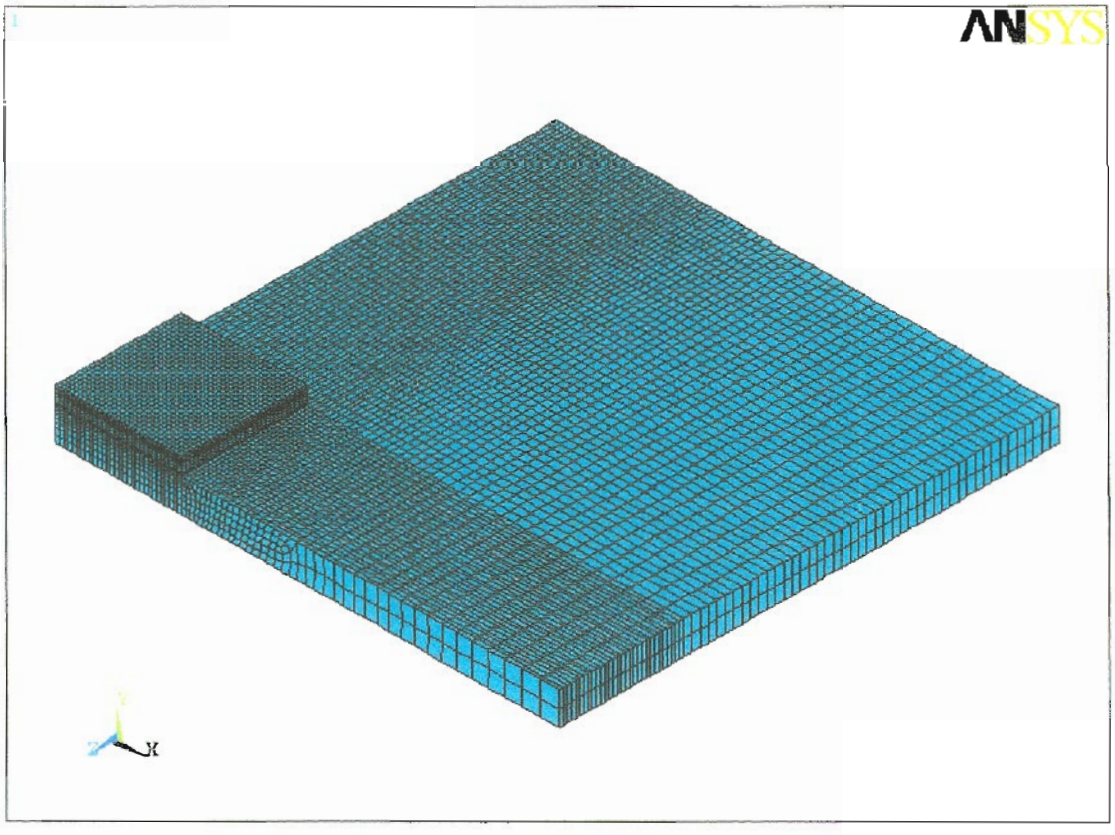


Figure. 3-21 Mesh– 3D - Quarter Symmetry – Wire Interconnect

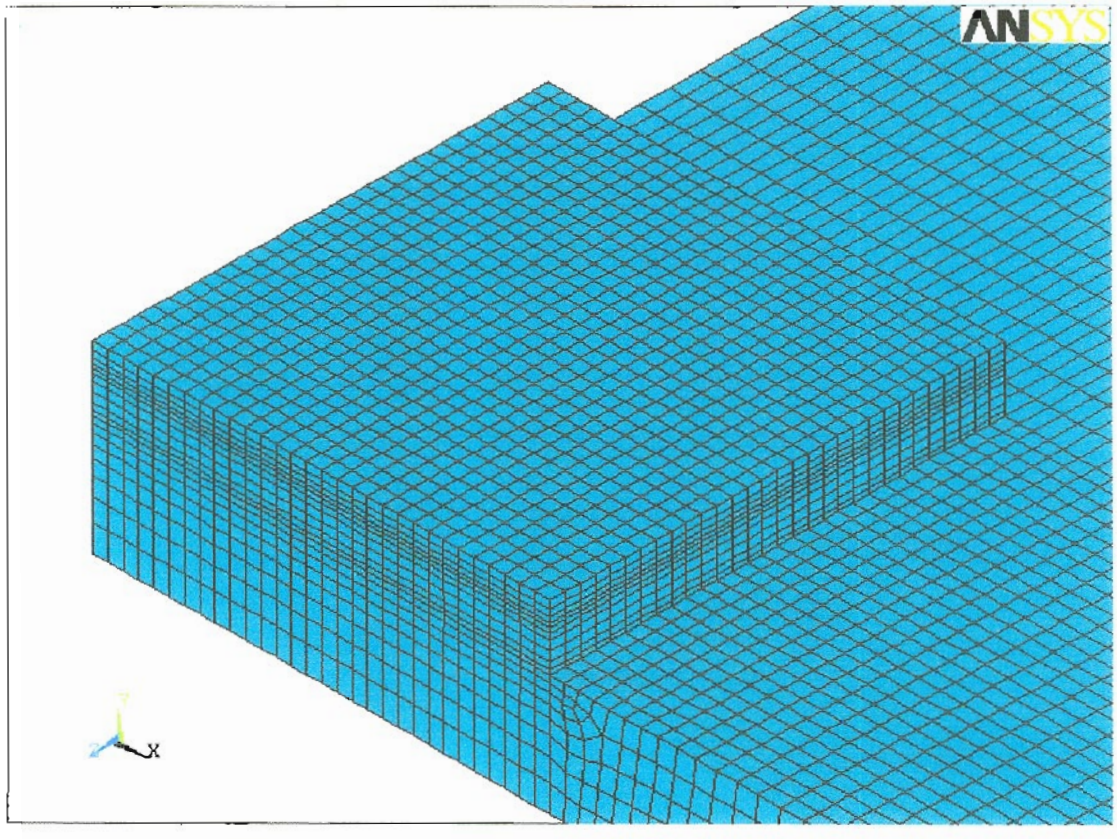


Figure. 3-22 Enlarged Mesh – 3D - Quarter Symmetry – Solder Interconnect

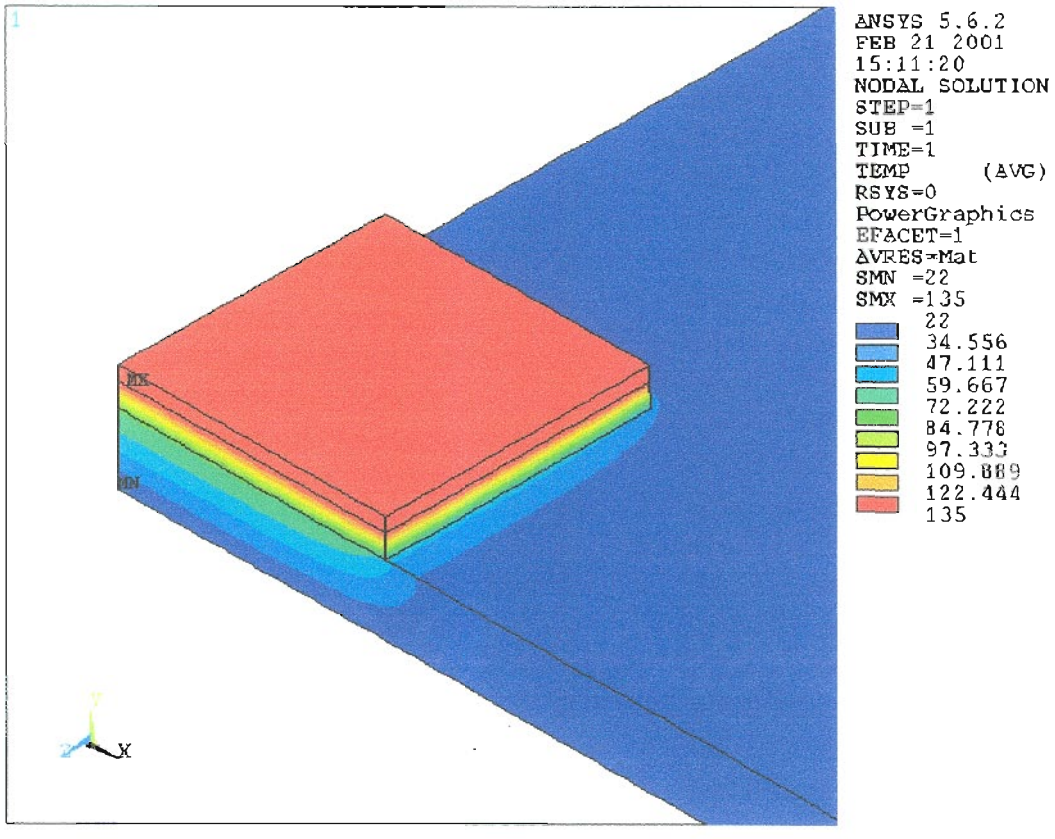


Figure. 3-23 Temperature– 3D - Quarter Symmetry –Solder Interconnect

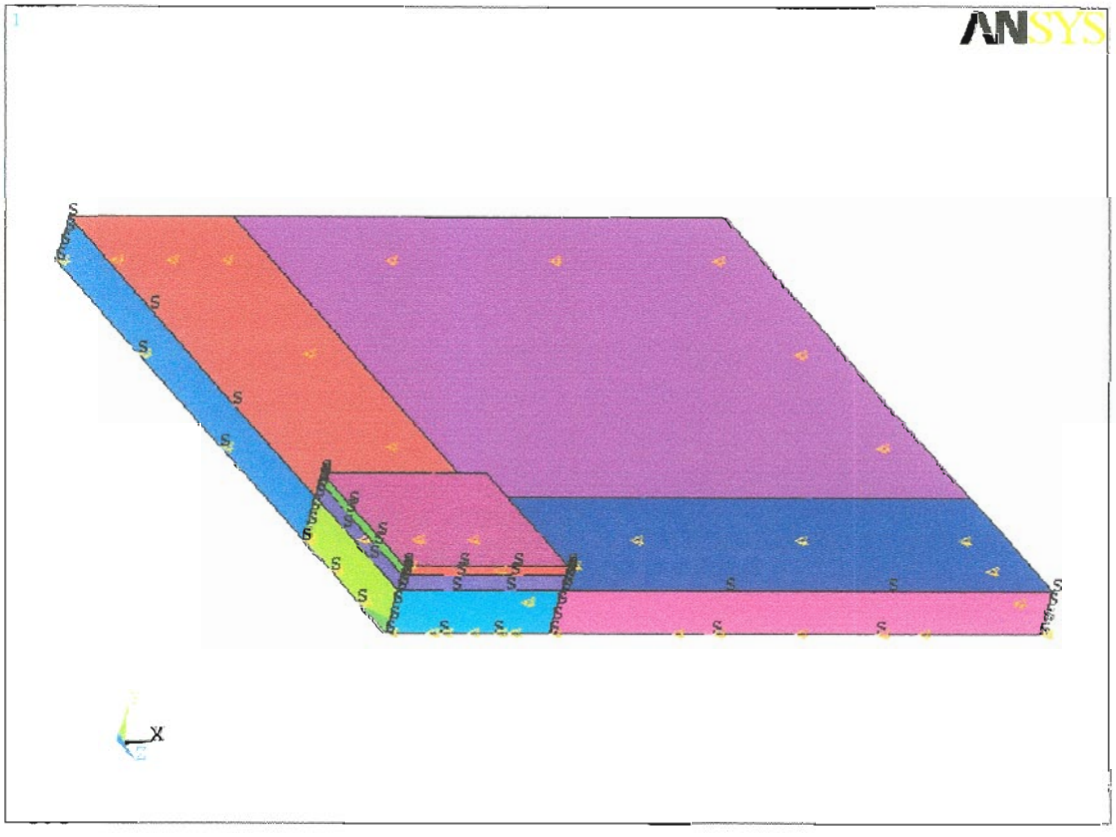


Figure. 3-24 Boundary Conditions – 3D - Quarter Symmetry –Solder Interconnect

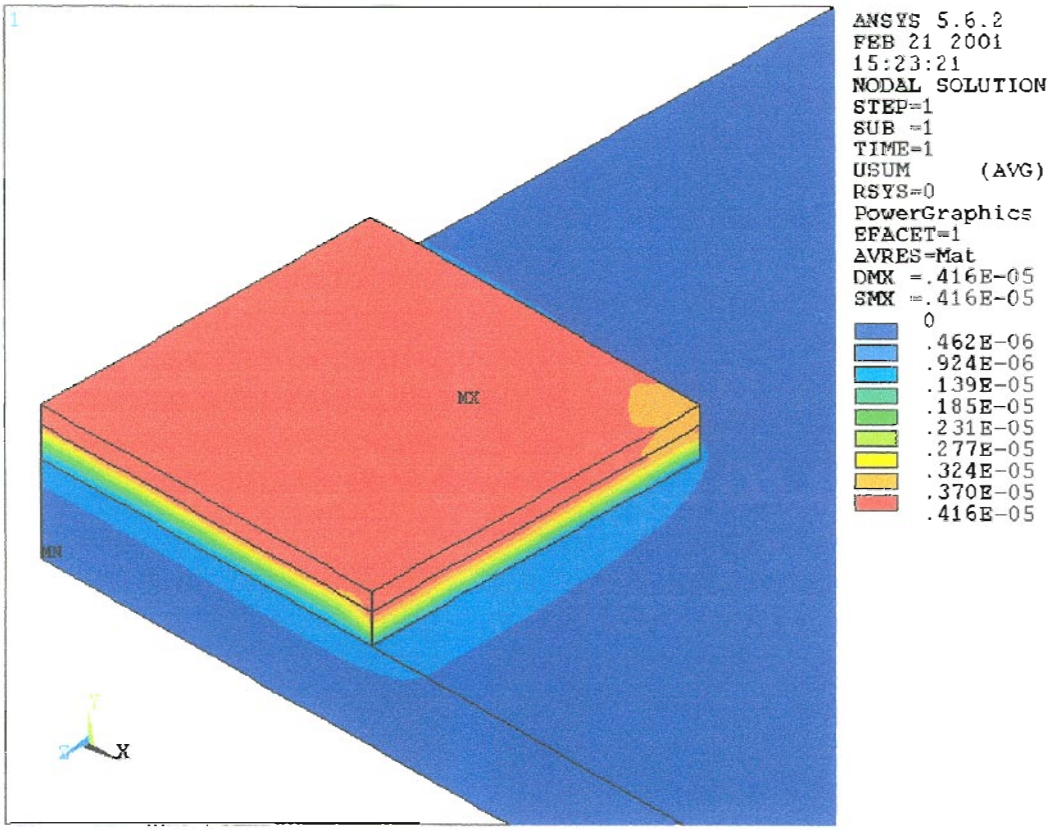


Figure. 3-25 Displacements – 3D - Quarter Symmetry – Solder Interconnect

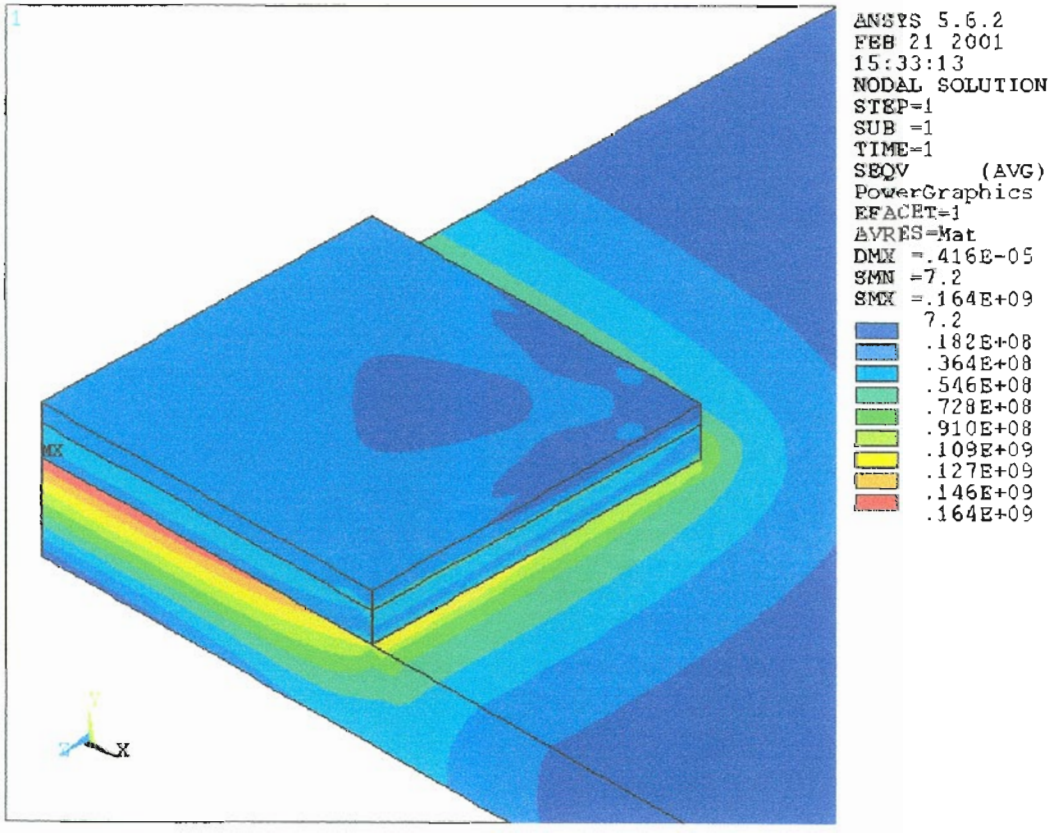


Figure 3-26 Von Mises Stress – 3D - Quarter Symmetry – Solder Interconnect

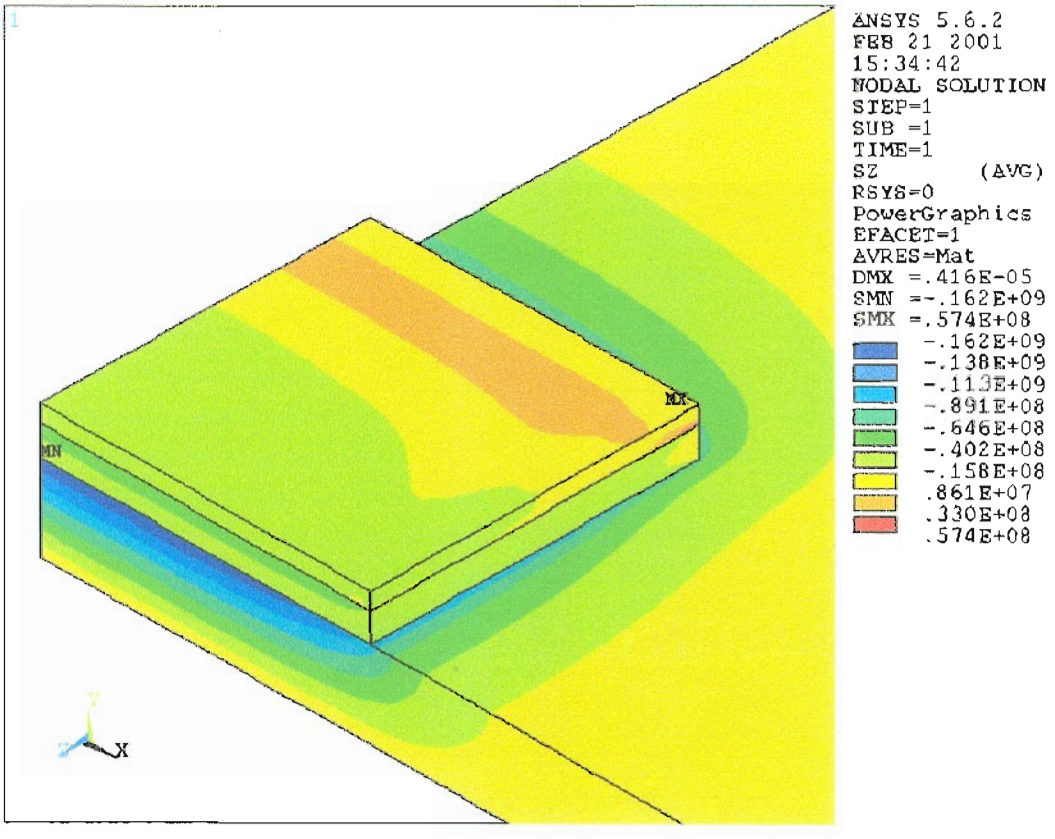


Figure. 3-27 Z-Direction Stress – 3D - Quarter Symmetry – Solder Interconnect

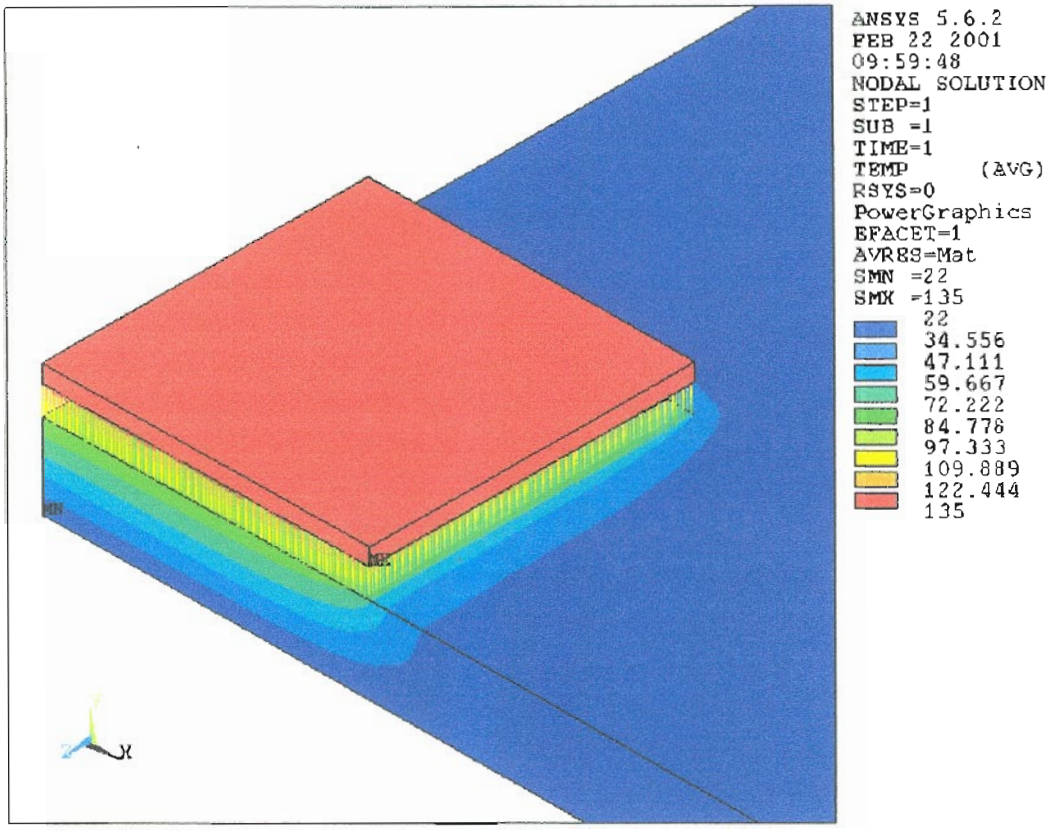


Figure. 3-28 Temperature Distribution – 3D - Quarter Symmetry

Wire Interconnect -Wire Material - Gold

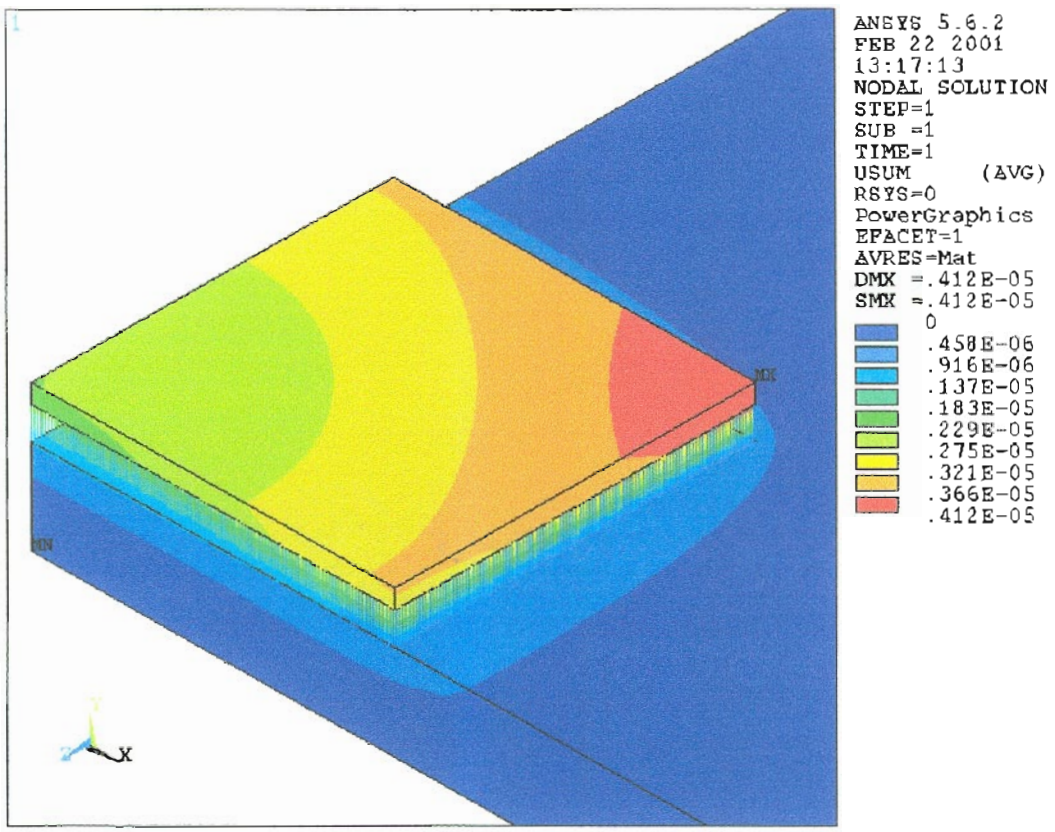


Figure 3-29 Displacement – 3D - Quarter Symmetry

Wire Interconnect - Wire Material - Gold

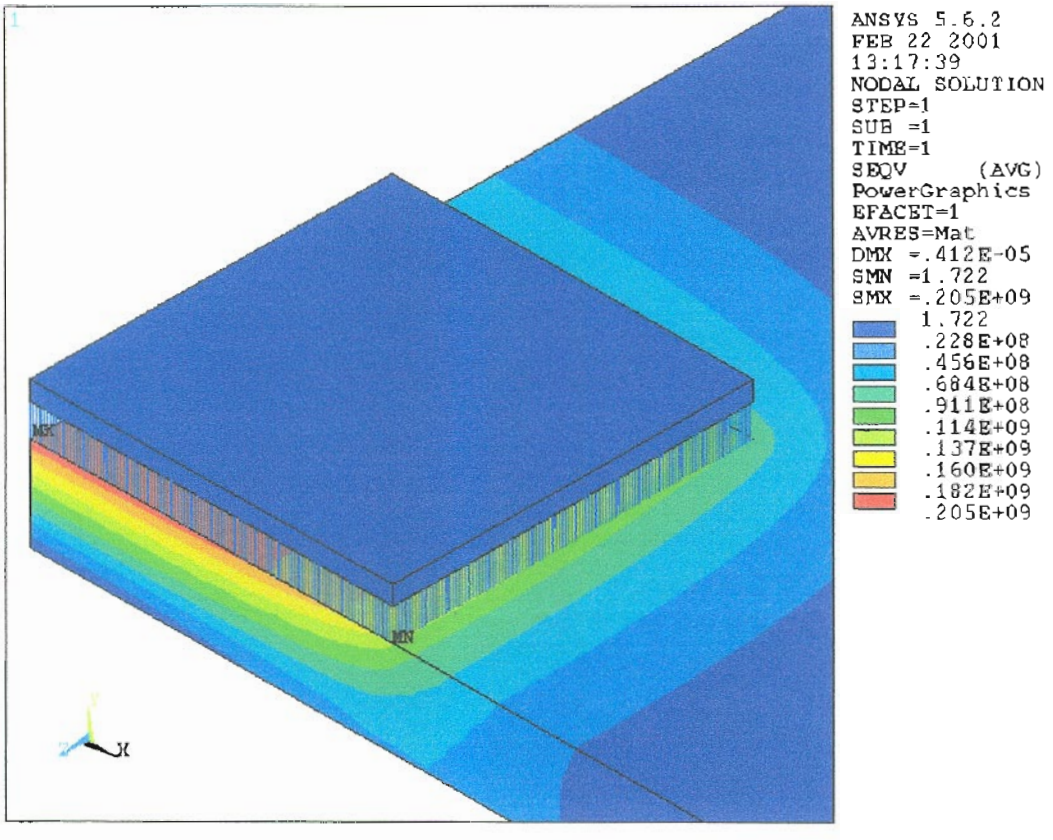


Figure 3-30 Von Mises Stress– 3D - Quarter Symmetry

Wire Interconnect - Wire Material - Gold

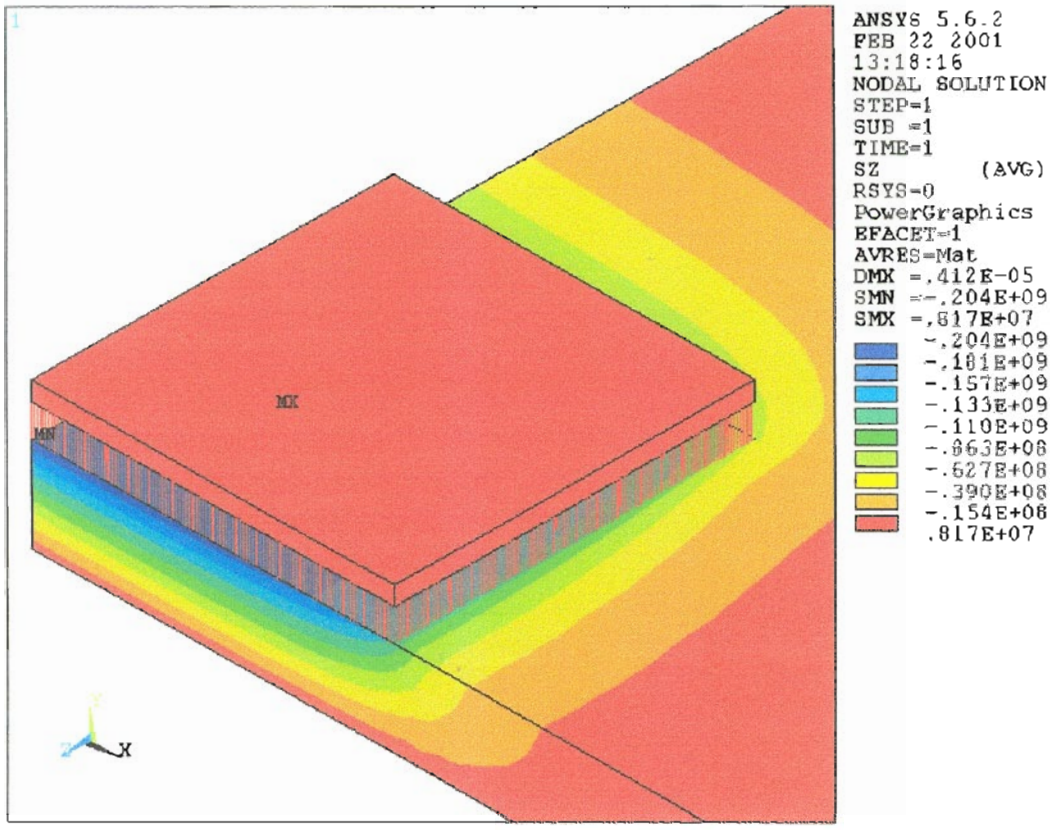


Figure 3-31 Z-Direction Stress– 3D - Quarter Symmetry

Wire Interconnect - Wire Material – Gold

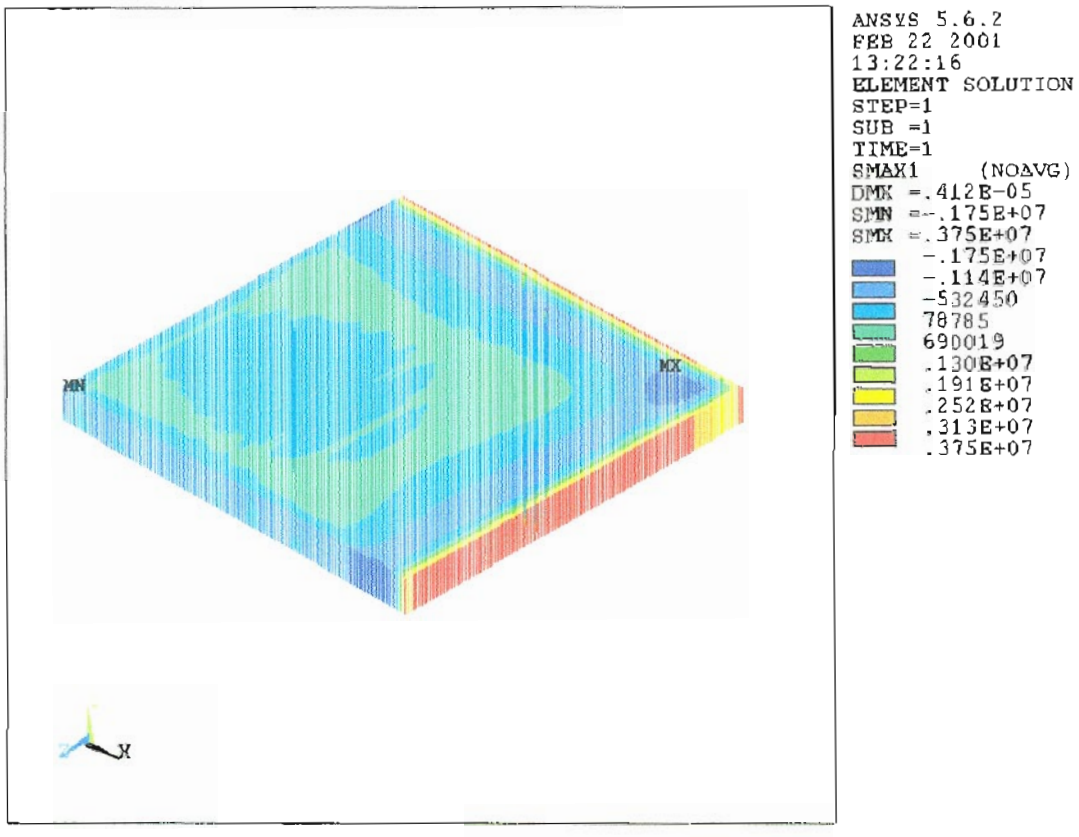


Figure 3-32 Wire Stress– 3D - Quarter Symmetry

Wire Interconnect - Wire Material – Gold

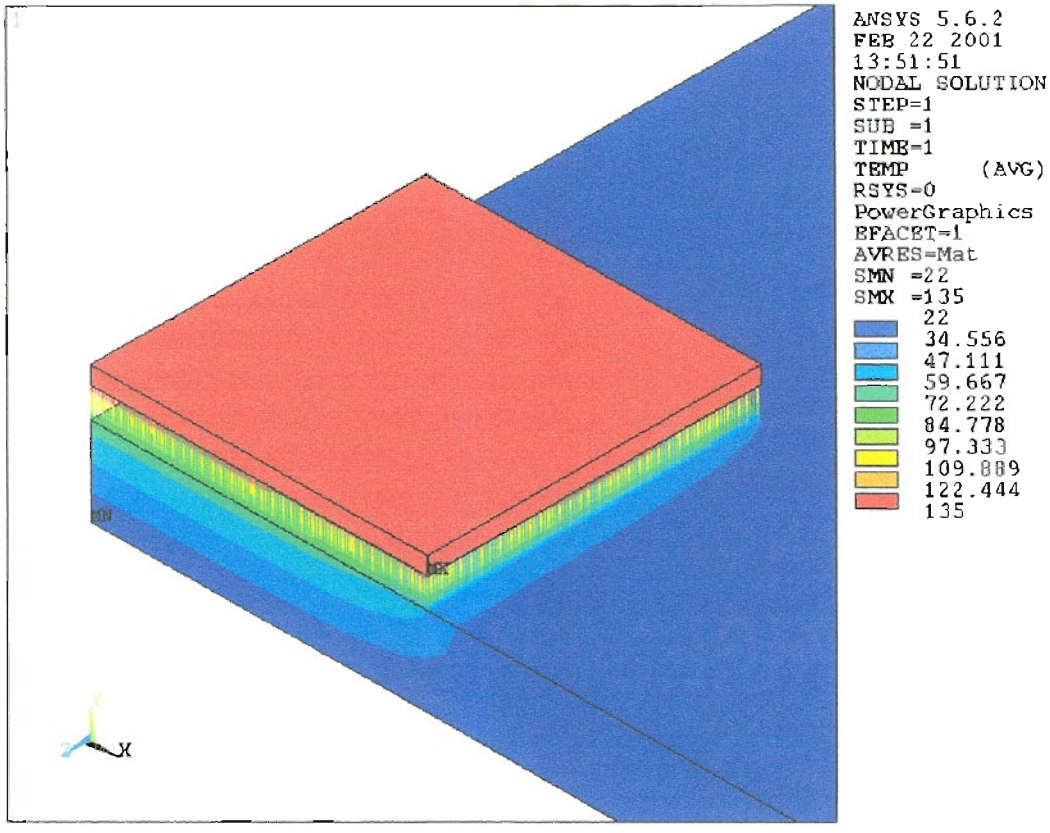


Figure 3-33 Temperature Distribution – 3D - Quarter Symmetry

Wire Interconnect - Wire Material – Beryllium Copper

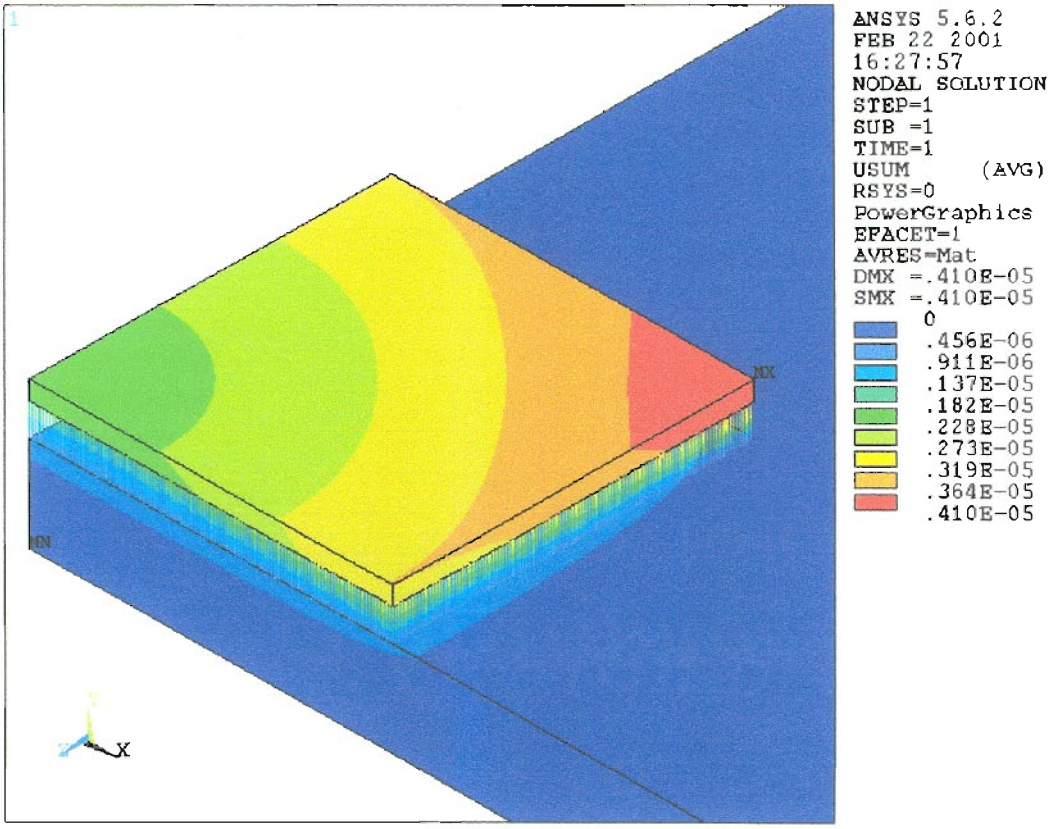


Figure 3-34 Displacement – 3D - Quarter Symmetry

Wire Interconnect - Wire Material – Beryllium Copper

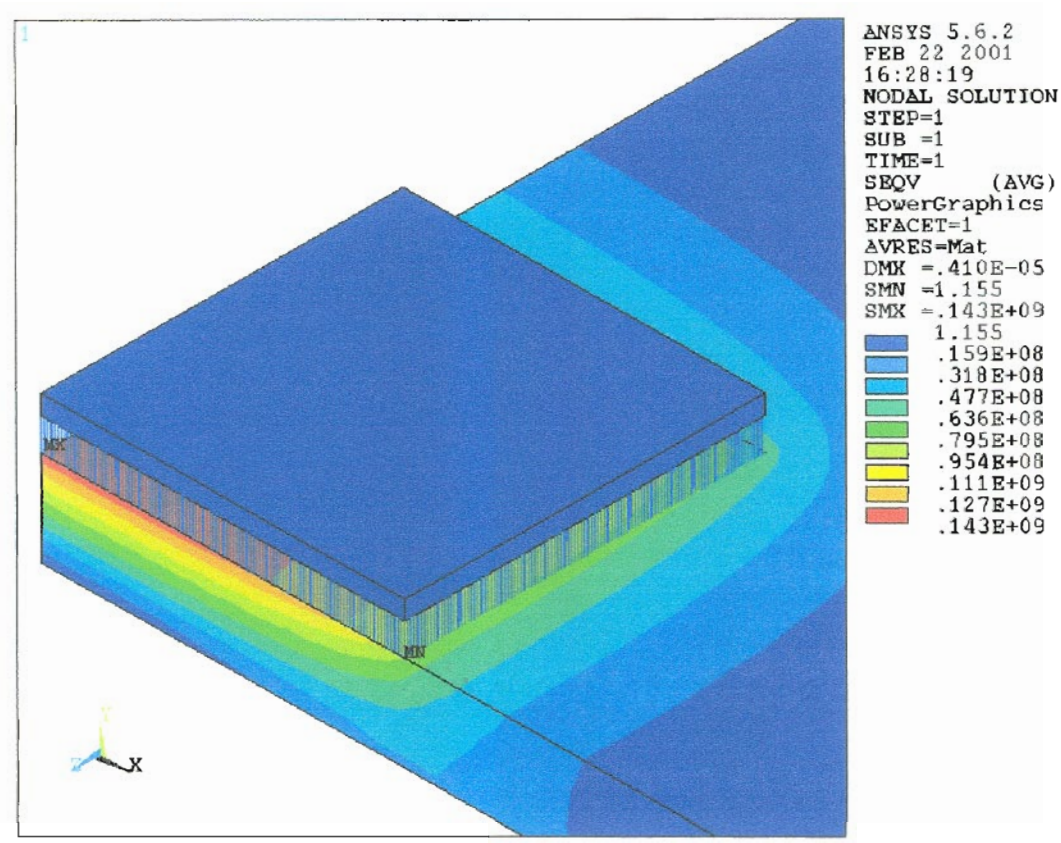


Figure. 3-35 Von Mises Stress– 3D - Quarter Symmetry

Wire Interconnect - Wire Material – Beryllium Copper

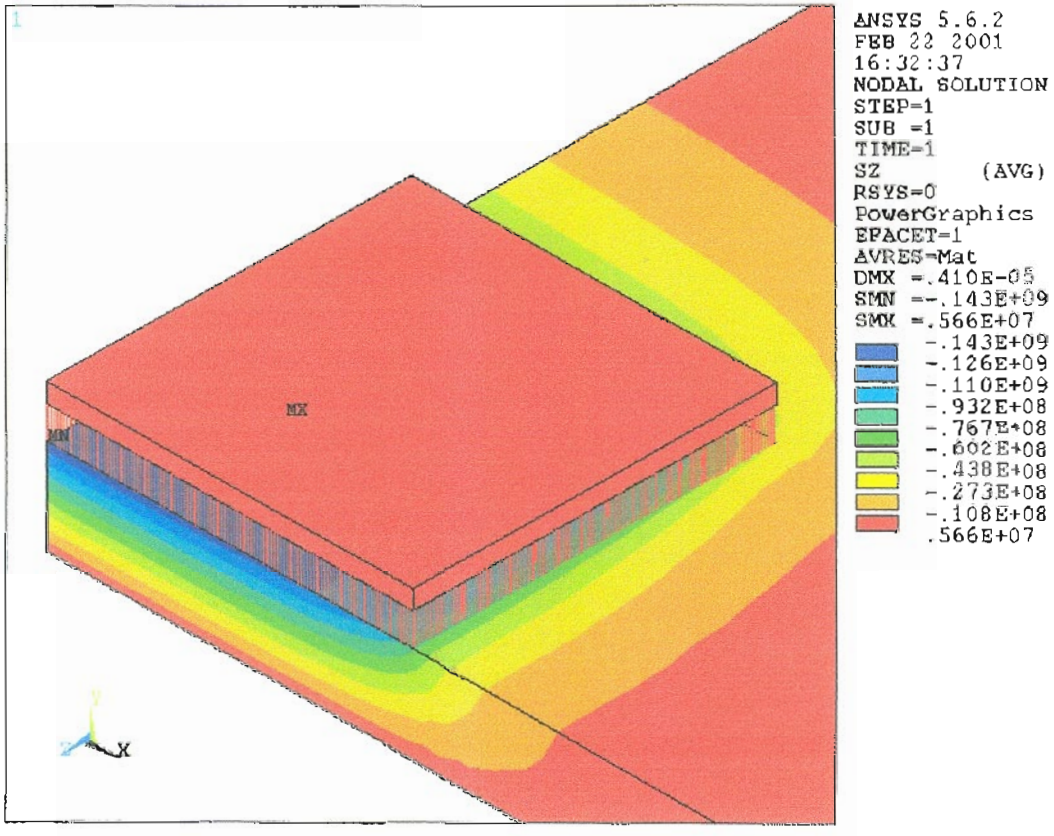


Figure 3-36 Z- Direction Stress– 3D - Quarter Symmetry

Wire Interconnect - Wire Material – Beryllium Copper

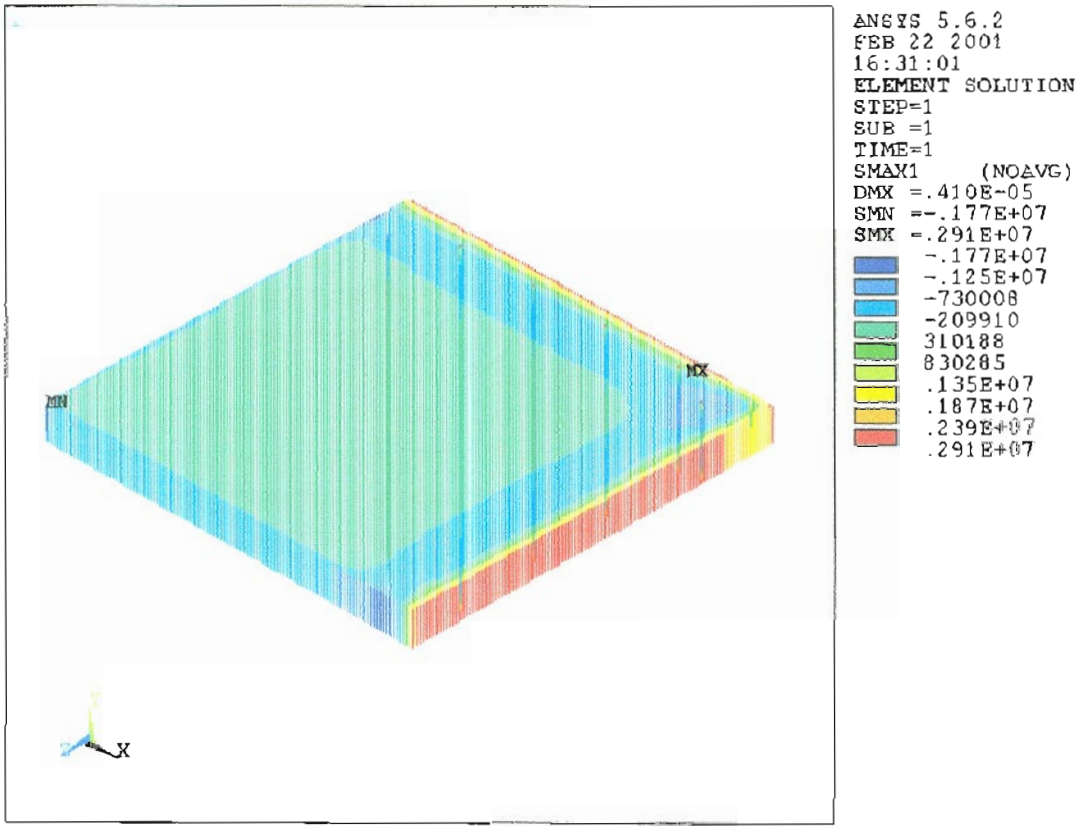


Figure 3-37 Wire Stress– 3D - Quarter Symmetry

Wire Interconnect - Wire Material – Beryllium Copper

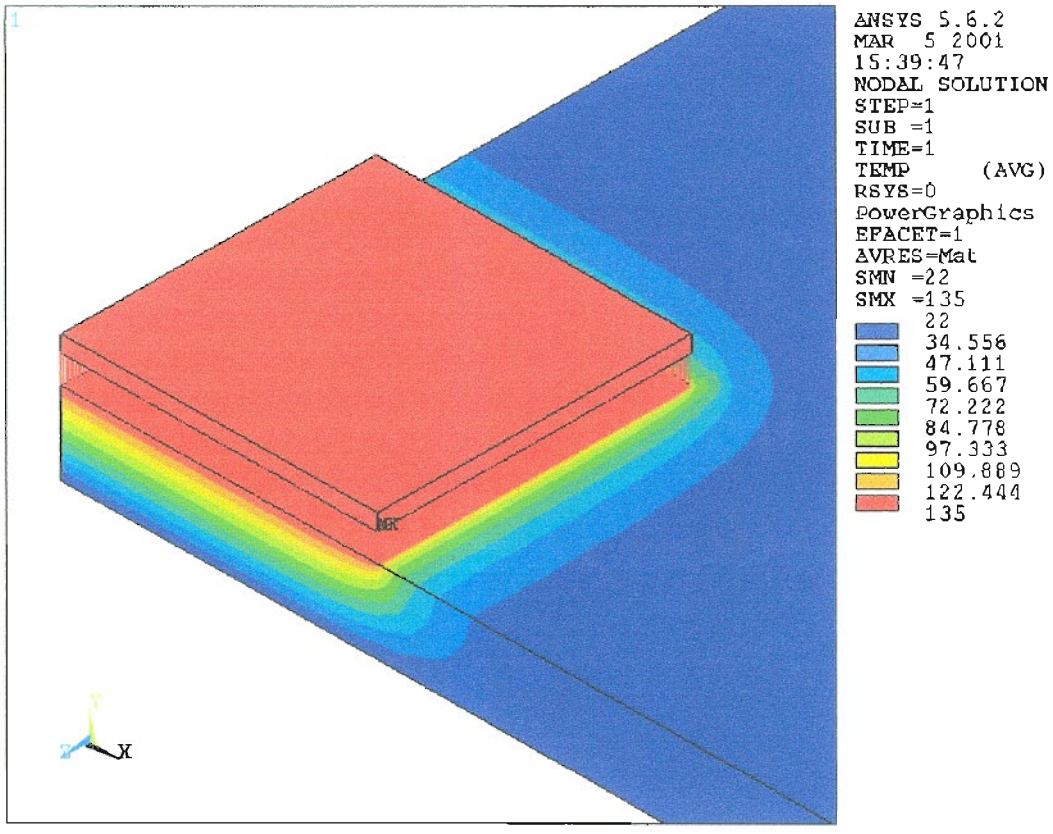


Figure 3-38 Temperature– 3D - Quarter Symmetry - Wire Interconnect

Wire Material – Silver - Wire Diameter = 0.5 mm

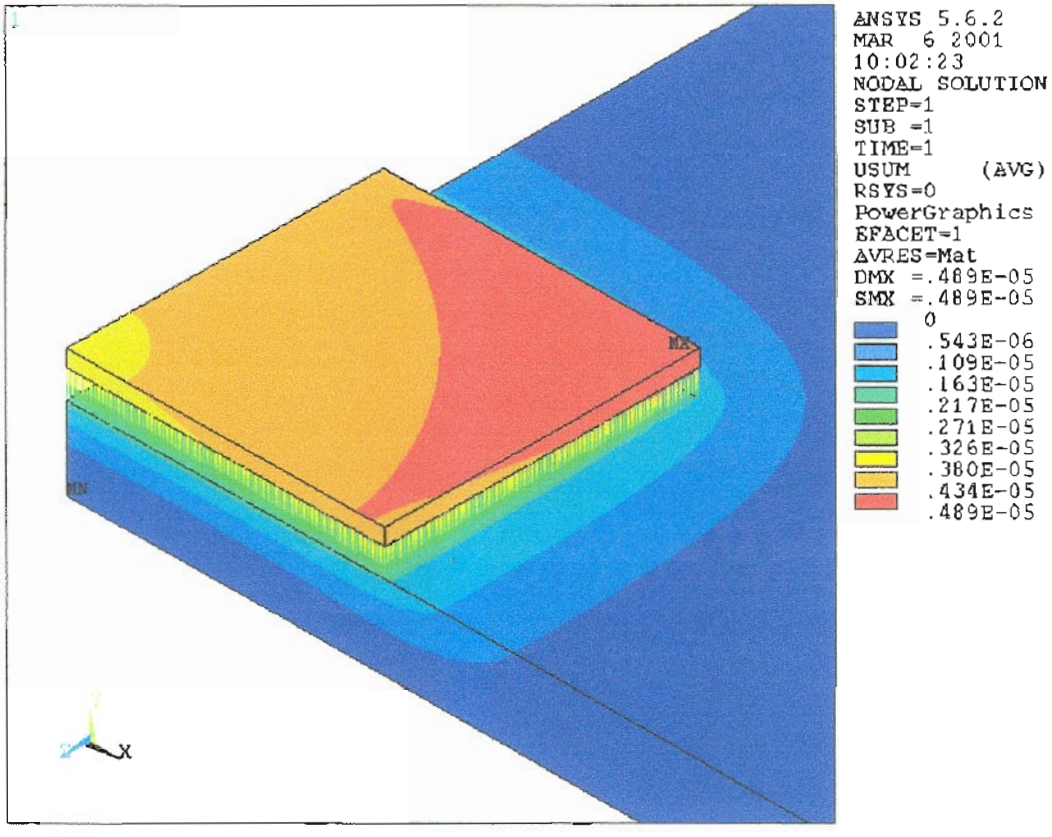


Figure 3-39 Displacement – 3D - Quarter Symmetry – Wire Interconnect
Wire Material – Silver, Wire Diameter = 0.5 mm

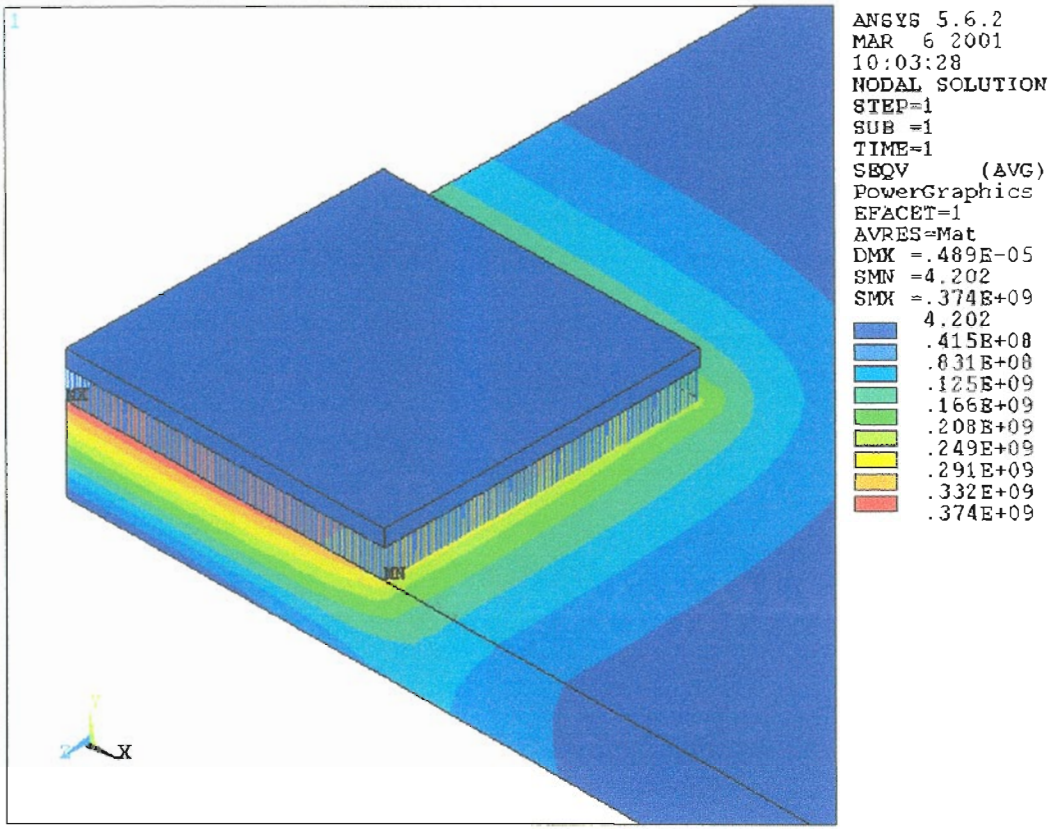


Figure 3-40 Von Mises Stress– 3D - Quarter Symmetry – Wire Interconnect

Wire Material – Silver, Wire Diameter = 0.5 mm

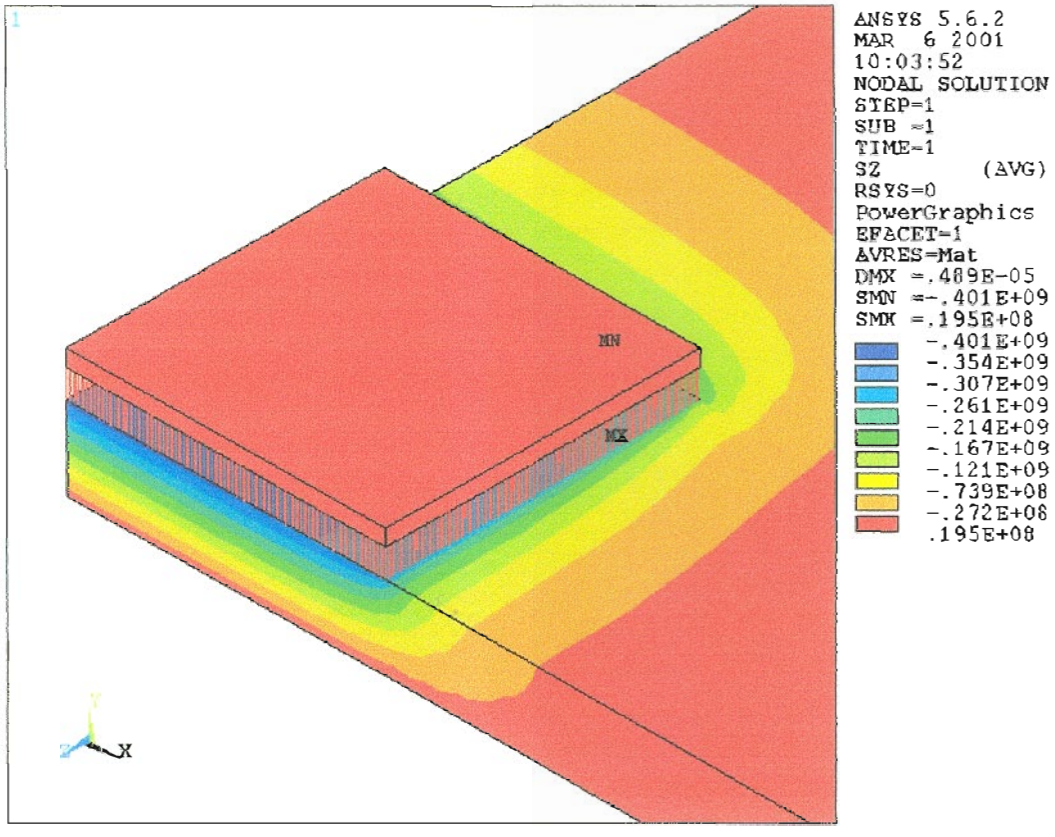


Figure 3-41 Z-Direction Stress – 3D - Quarter Symmetry – Wire Interconnect
Wire Material – Silver, Wire Diameter = 0.5 mm

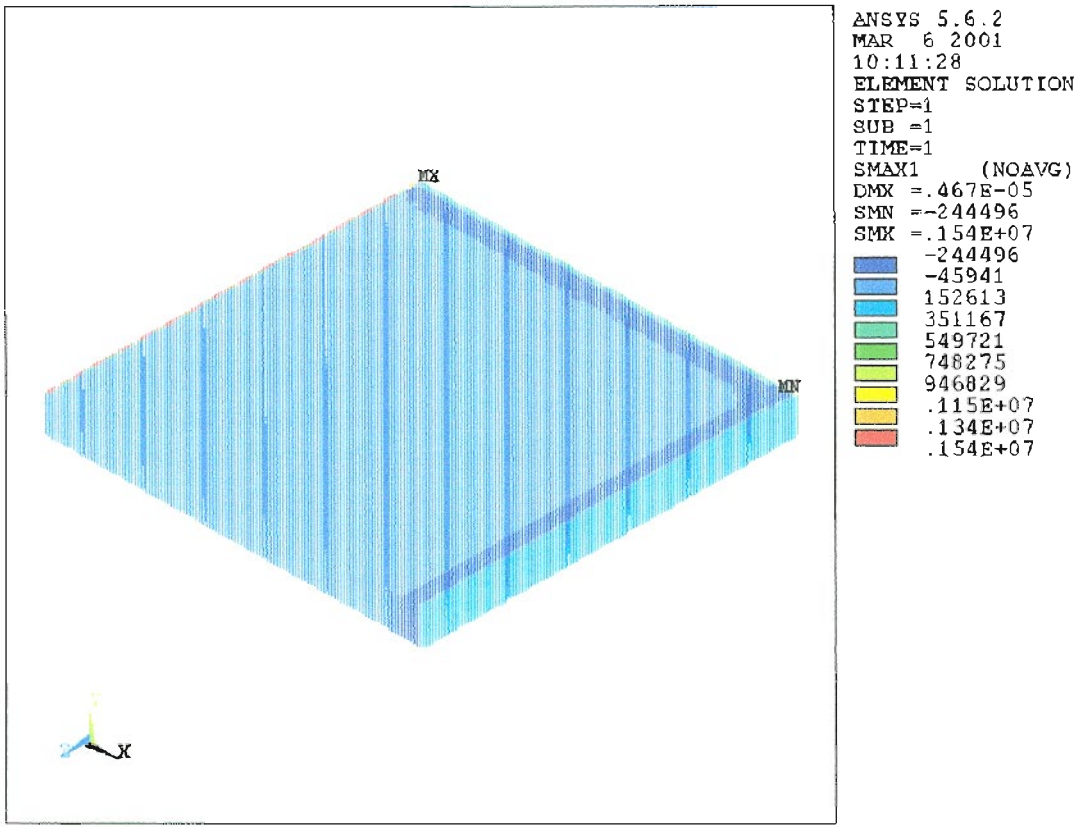


Figure 3-42 Wire Stress – 3D - Quarter Symmetry – Wire Interconnect

Wire Material – Silver, Wire Diameter = 0.5 mm

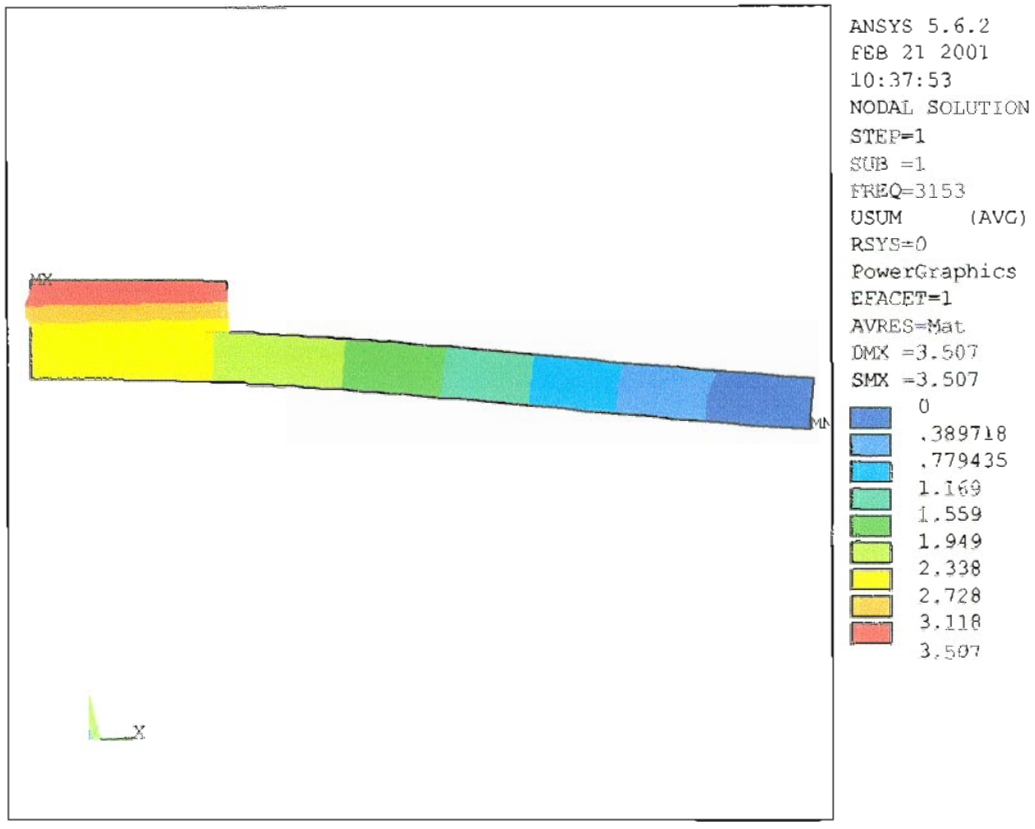


Figure 3-43 Vibrations - First Mode – 2D – Half Symmetry - Wire Interconnect
Wire Material – Silver, Wire Diameter = 0.05 mm

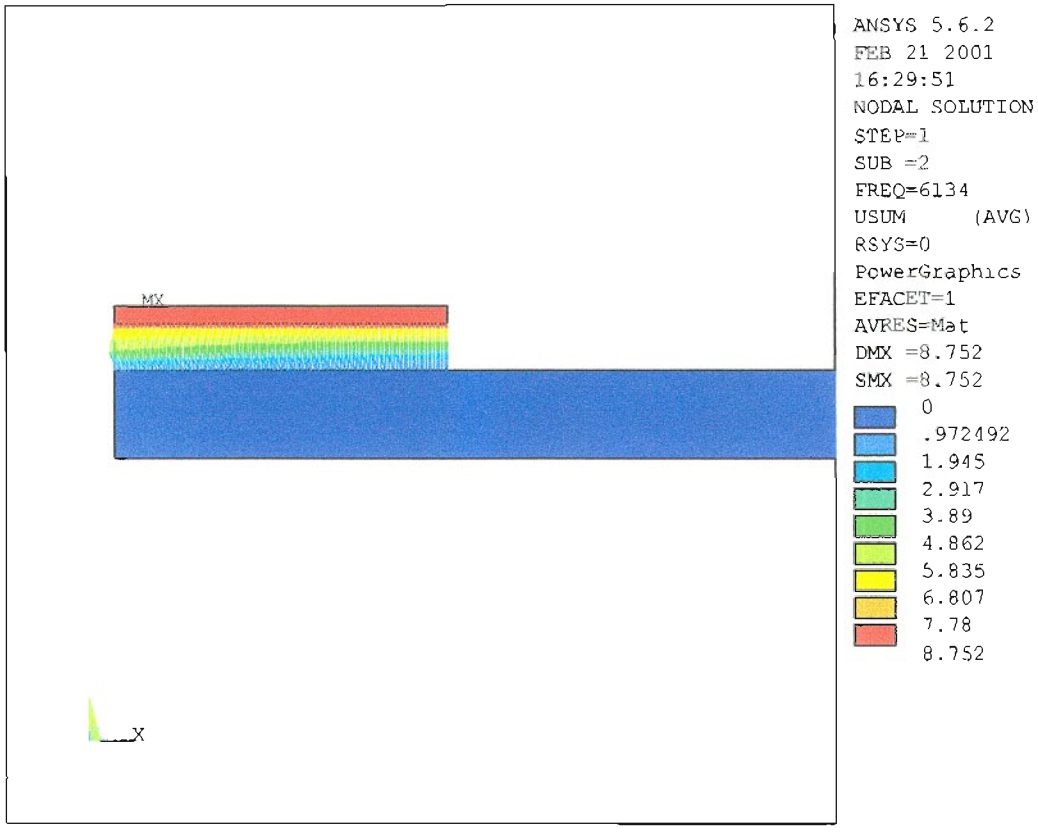


Figure 3-44 Vibrations - Second Mode – 2D – Half Symmetry - Wire Interconnect Wire Material – Silver, Wire Diameter = 0.05 mm

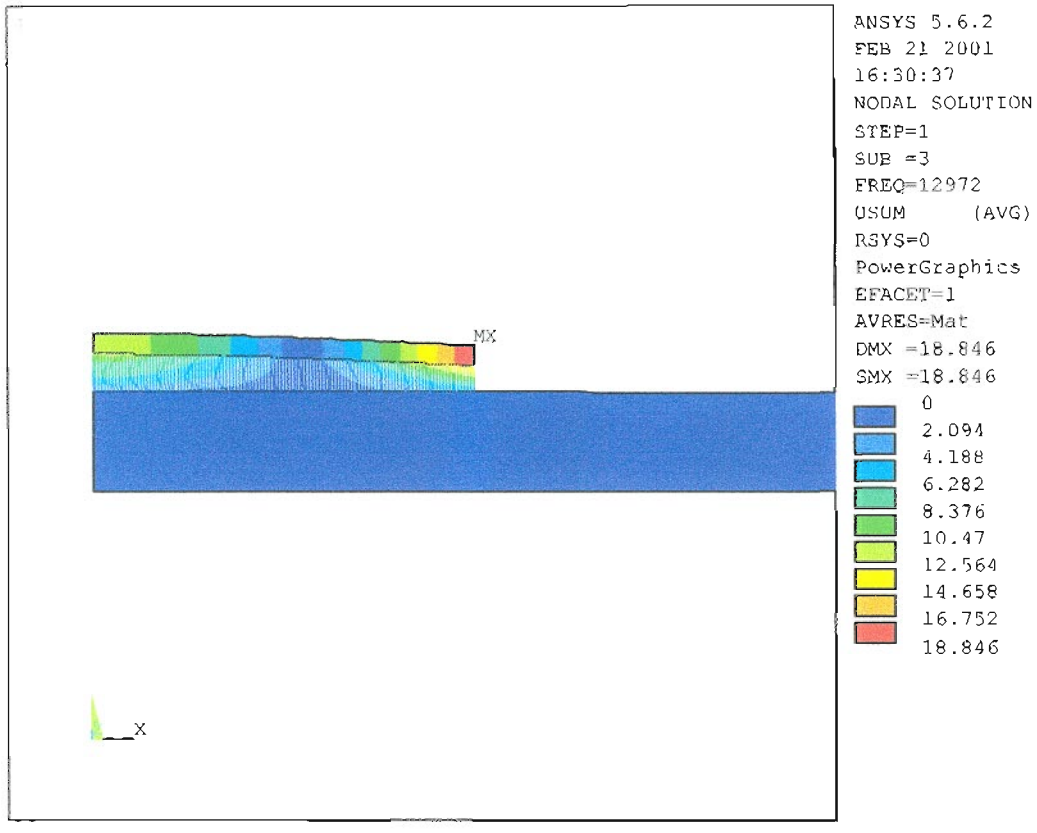


Figure 3-45 Vibrations - Third Mode – 2D – Half Symmetry - Wire Interconnect
Wire Material – Silver, Wire Diameter = 0.05 mm

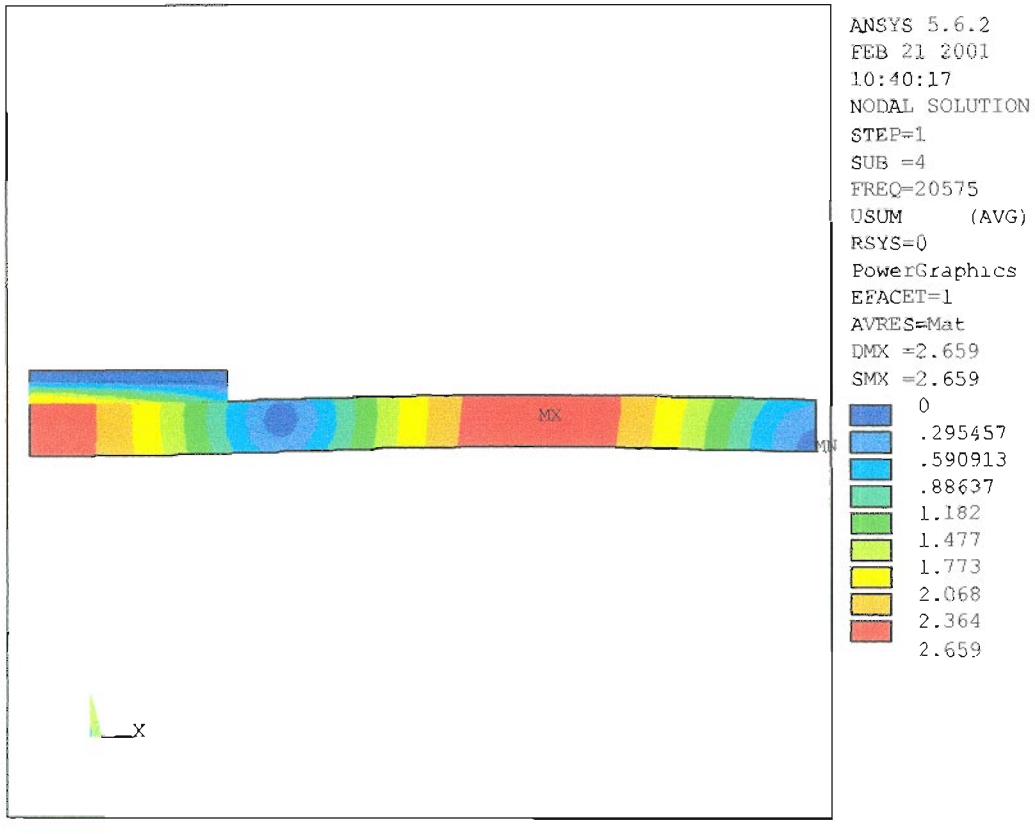


Figure 3-46 Vibrations - Fourth Mode – 2D – Half Symmetry - Wire Interconnect Wire Material – Silver, Wire Diameter = 0.05 mm

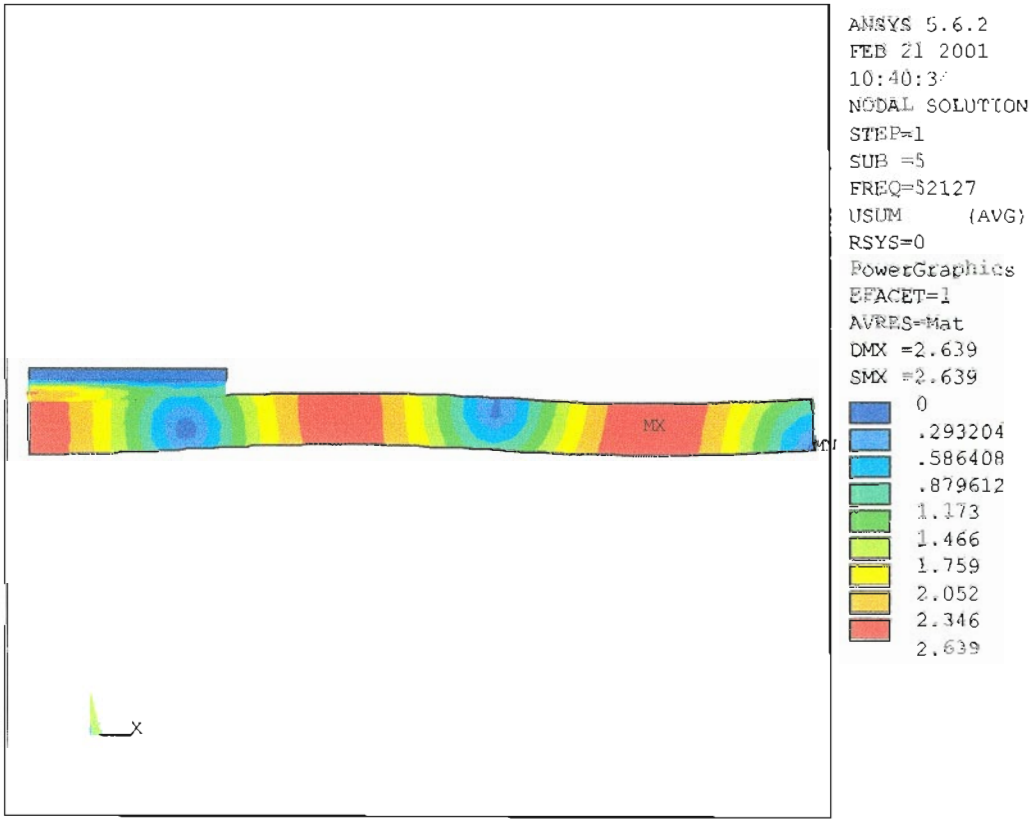


Figure 3-47 Vibrations - Fifth Mode – 2D – Half Symmetry - Wire Interconnect
Wire Material – Silver, Wire Diameter = 0.05 mm

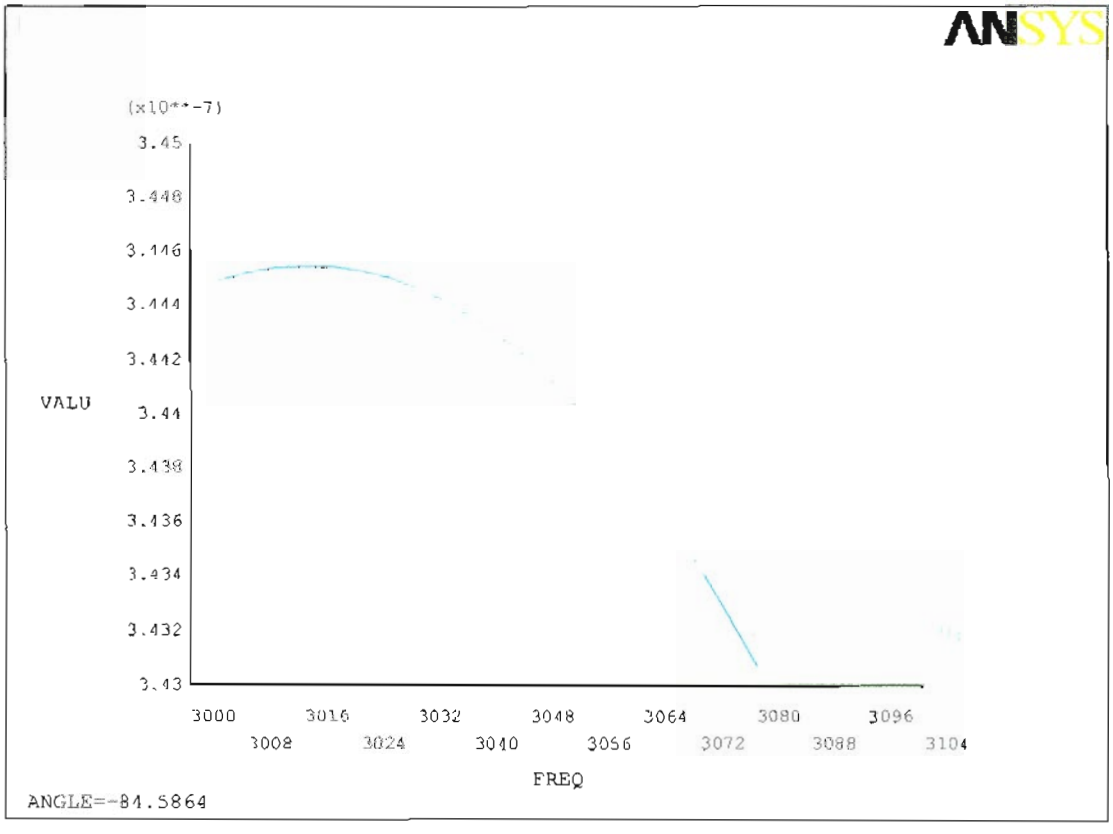


Figure 3-48 Vibrations – Frequency vs Amplitude – 2D – Half Symmetry

Wire Interconnect - Wire Material – Silver, Wire Diameter = 0.05 mm

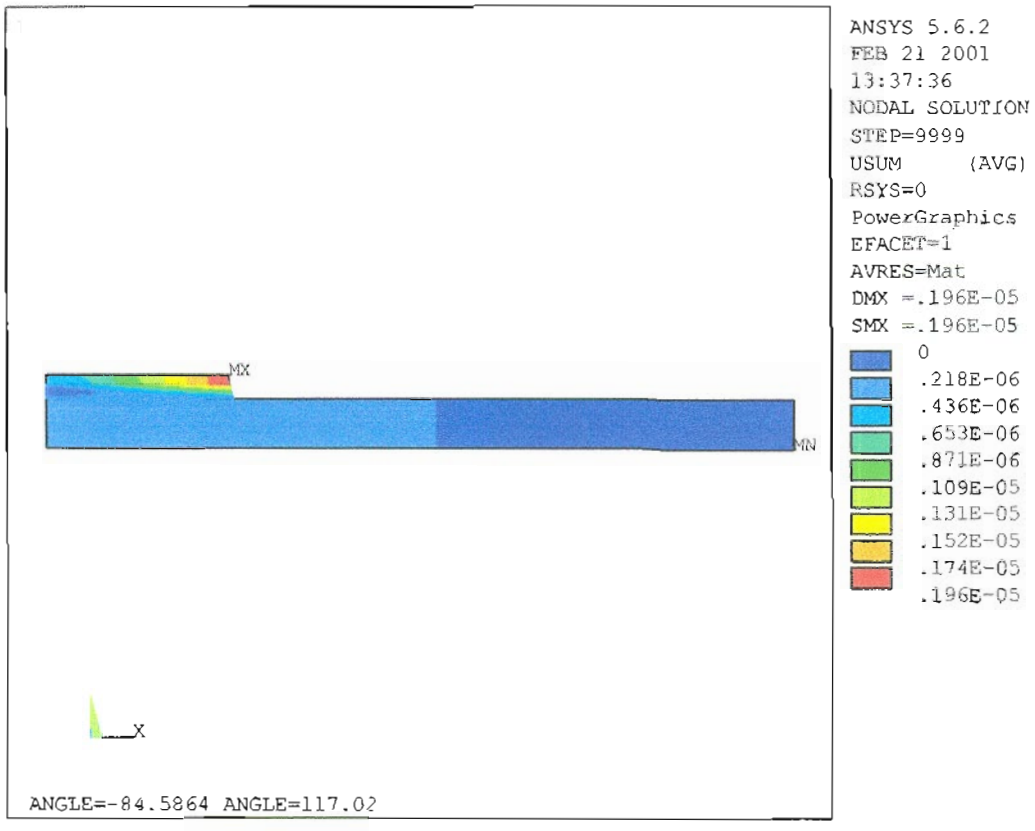


Figure 3-49 Vibrations –Displacement – 2D – Half Symmetry - Wire Interconnect Wire Material – Silver, Wire Diameter = 0.05 mm

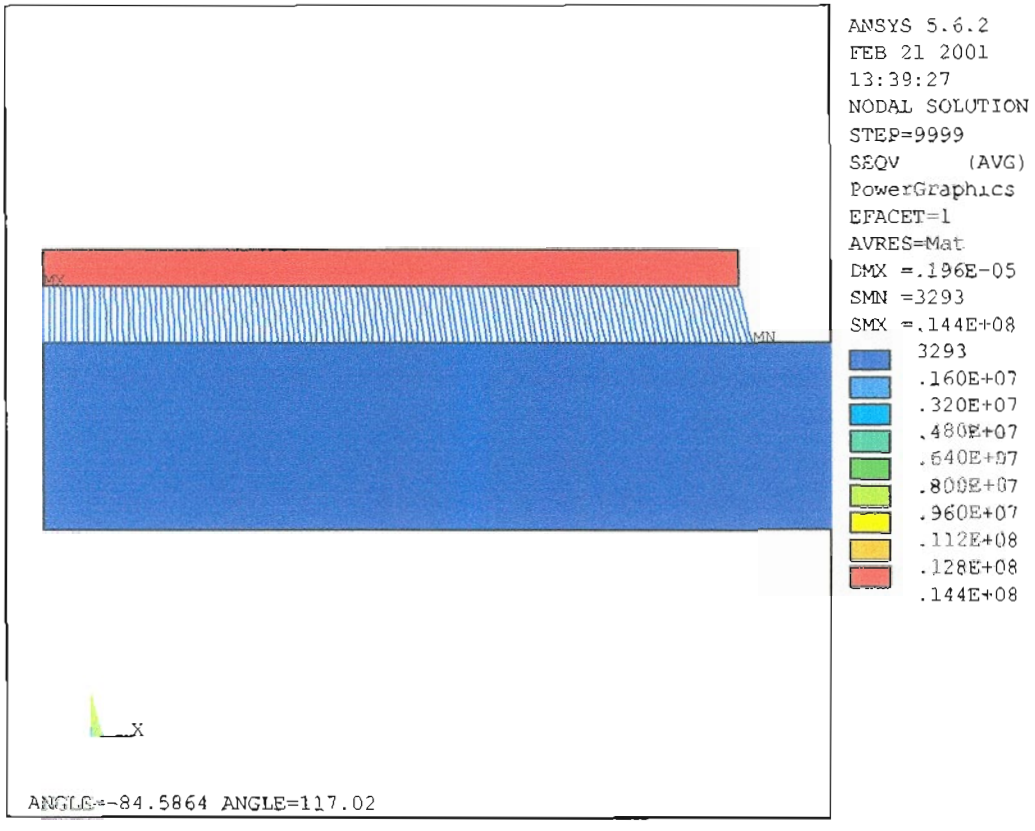


Figure 3-50 Vibrations –Stress – 2D – Half Symmetry - Wire Interconnect
Wire Material – Silver, Wire Diameter = 0.05 mm

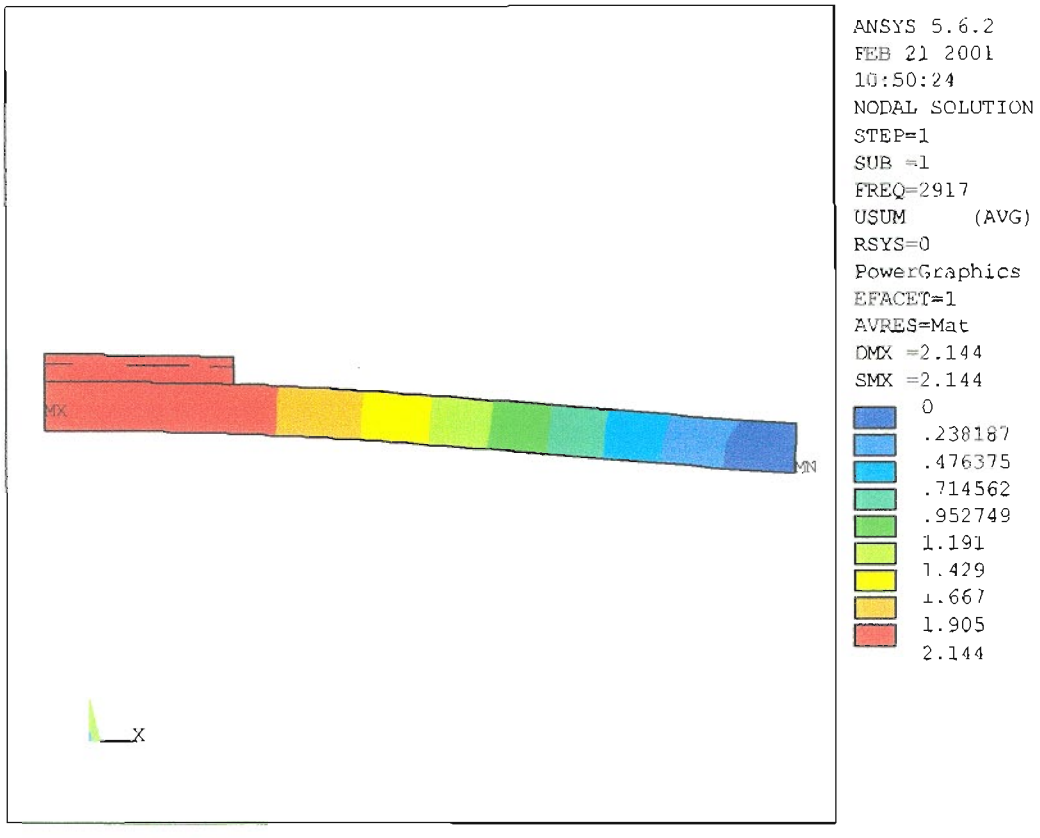


Figure 3-51 Vibrations - First Mode – 2D – Half Symmetry – Solder Interconnect

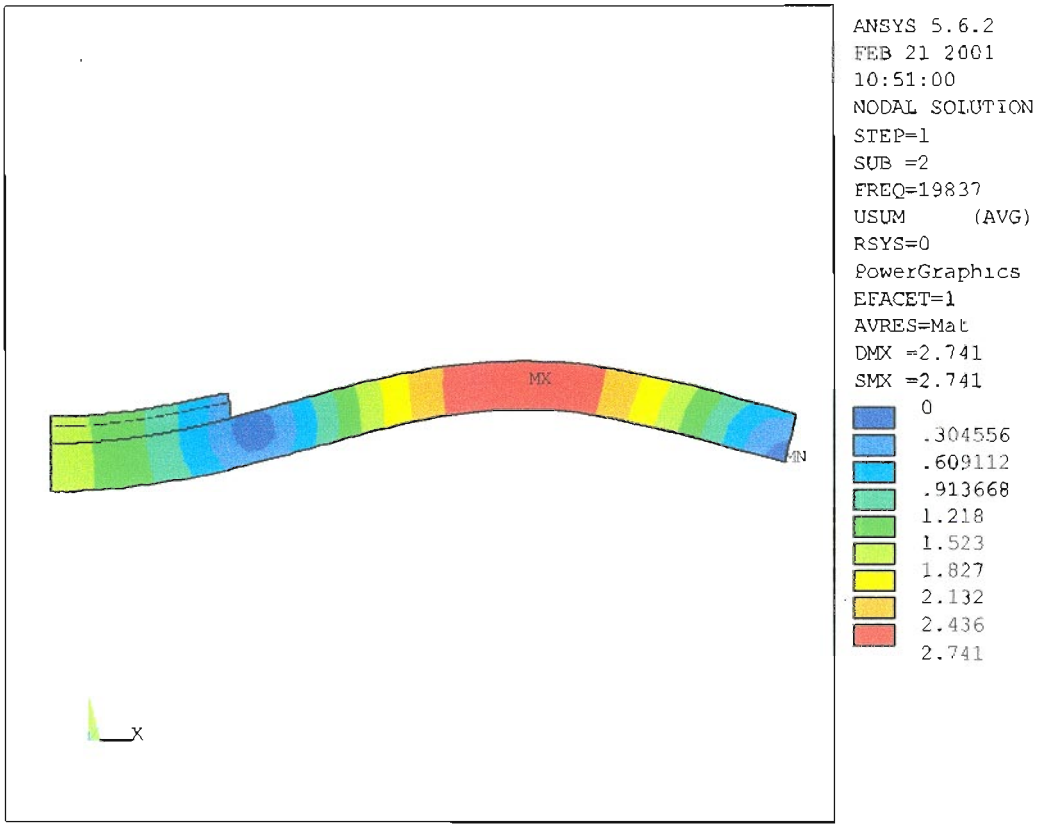


Figure 3-52 Vibrations - Second Mode – 2D – Half Symmetry – Solder Interconnect

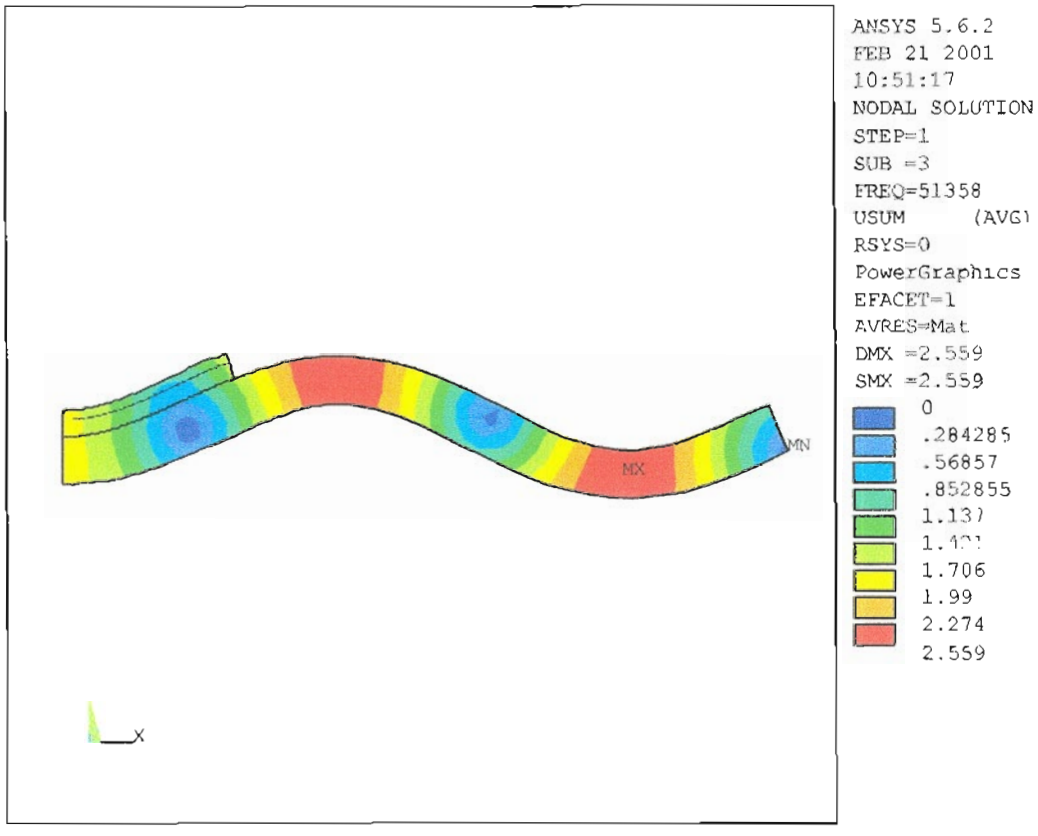


Figure 3-53 Vibrations - Third Mode – 2D – Half Symmetry – Solder Interconnect

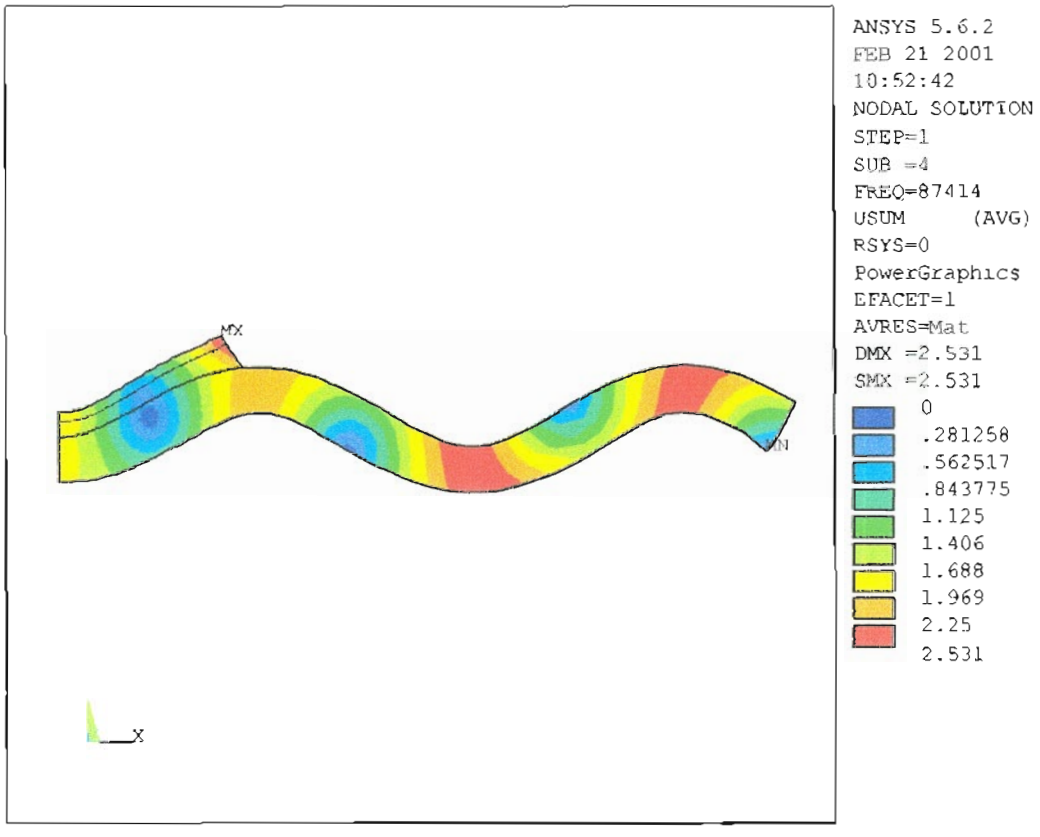


Figure 3-54 Vibrations - Fourth Mode – 2D – Half Symmetry – Solder Interconnect

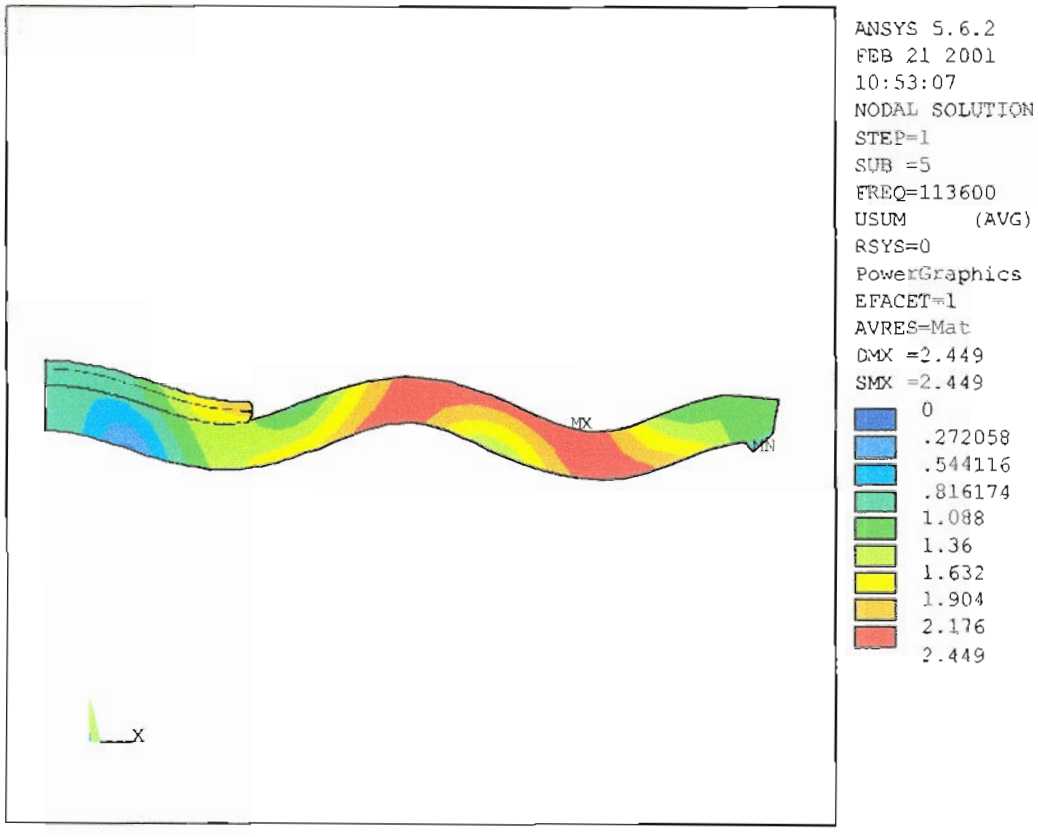


Figure 3-55 Vibrations - Fifth Mode – 2D – Half Symmetry - Solder Interconnect

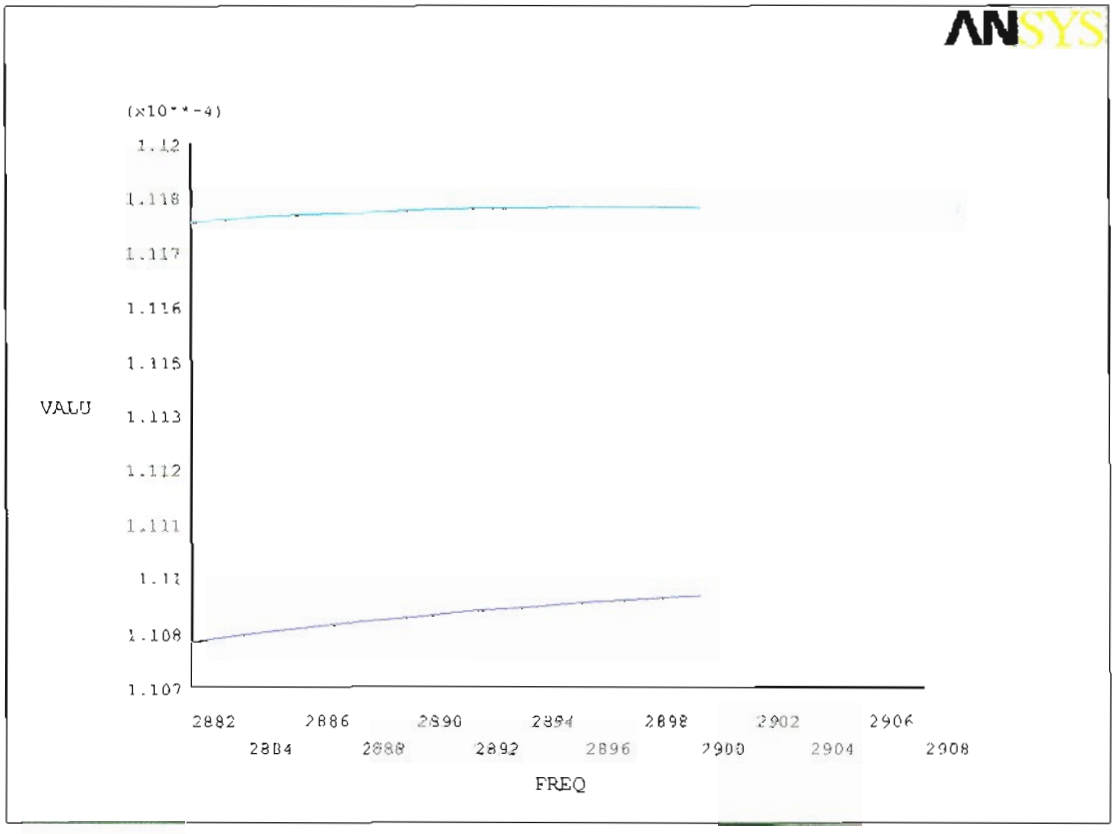


Figure 3-56 Vibrations – Frequency vs Amplitude – 2D – Half Symmetry Solder Interconnect

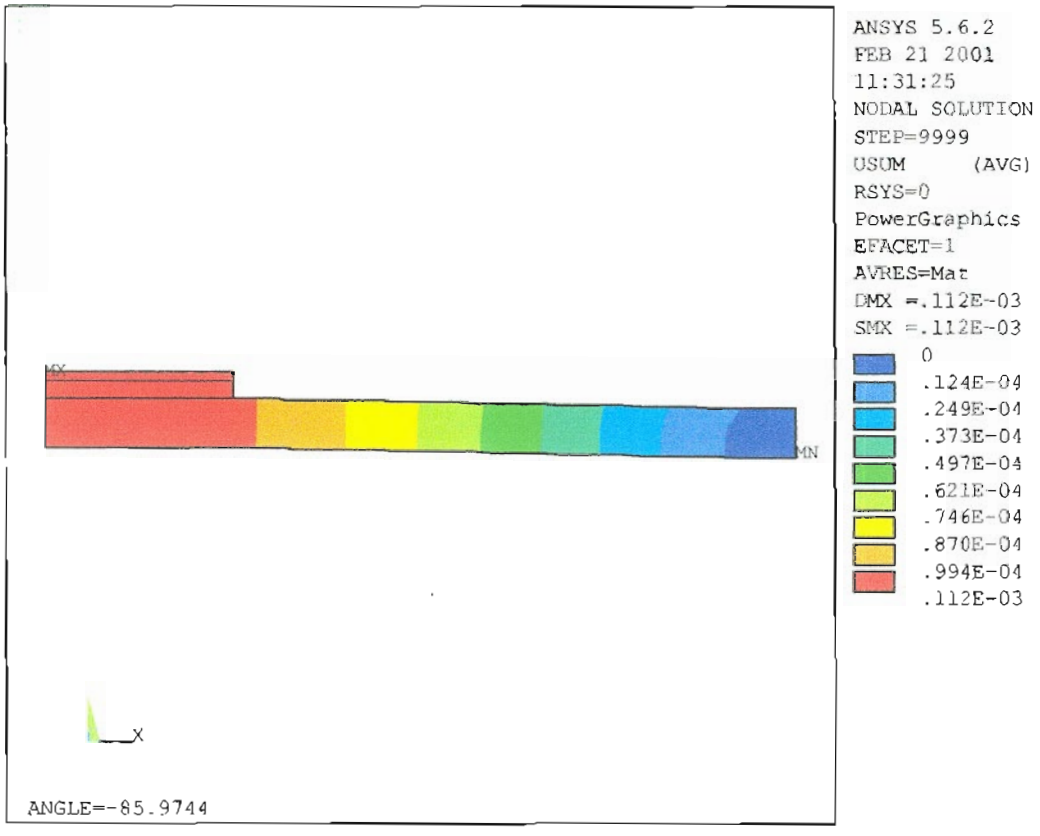


Figure 3-57 Vibrations –Displacement – 2D – Half Symmetry - Solder Interconnect

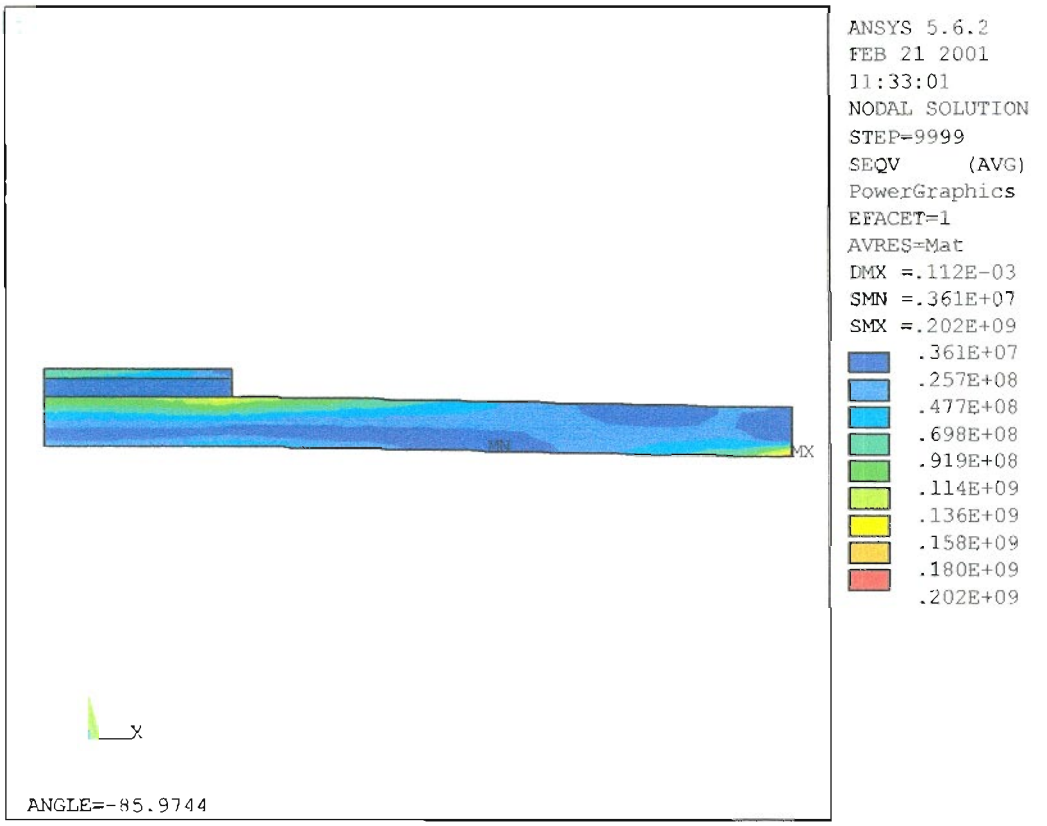


Figure 3-58 Vibrations –Stress – 2D – Half Symmetry - Solder Interconnect

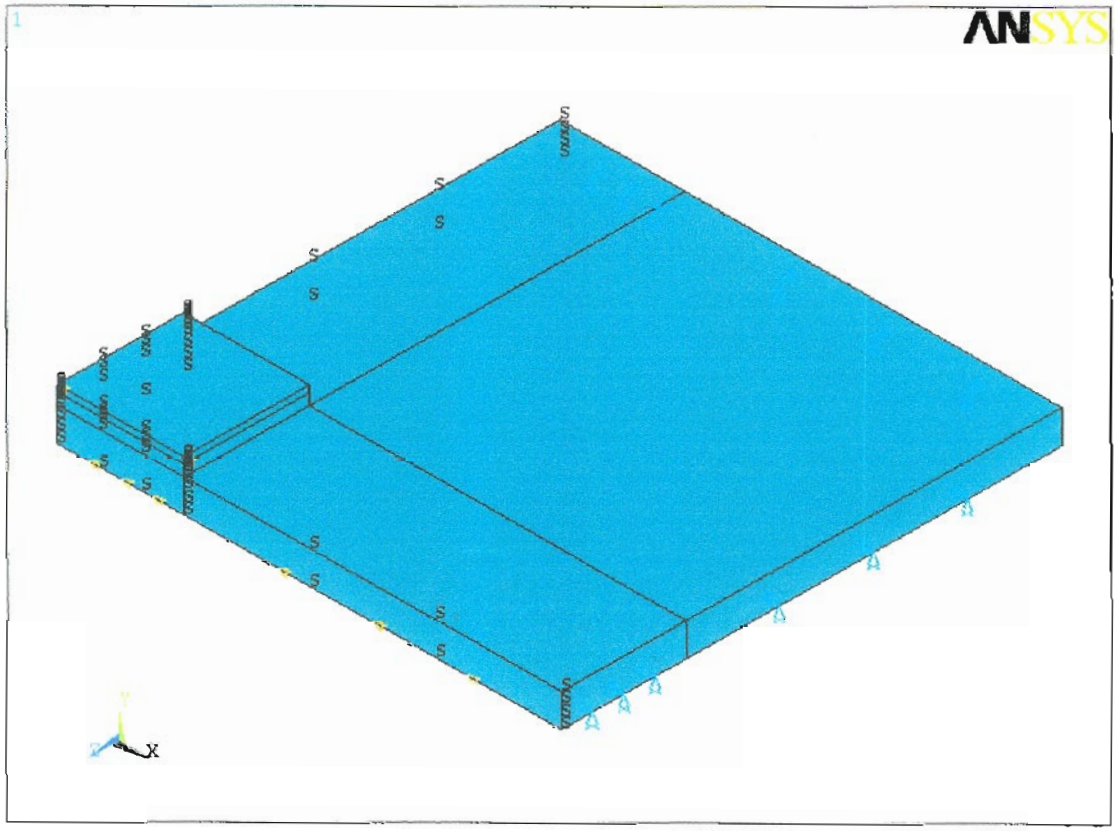


Figure 3-59 Boundary Conditions - 3D – Quarter Symmetry
Solder Interconnect

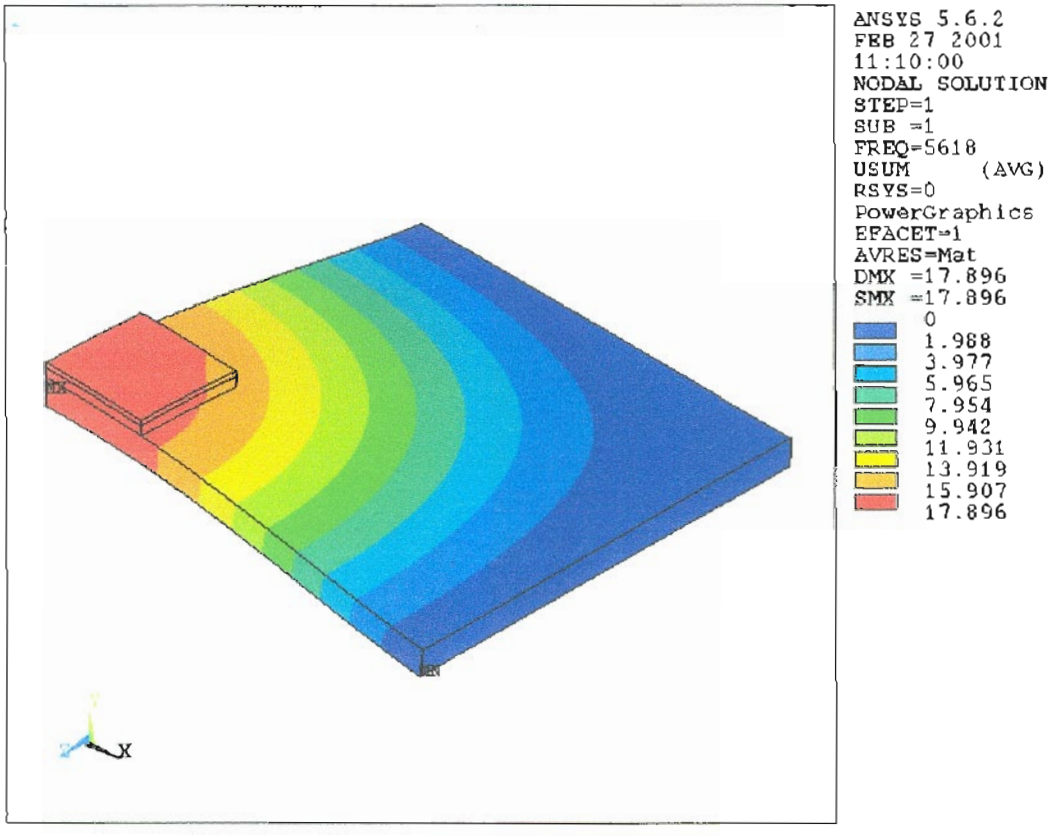


Figure 3-60 Vibrations - First Mode – 3D –Quarter Symmetry Solder Interconnect

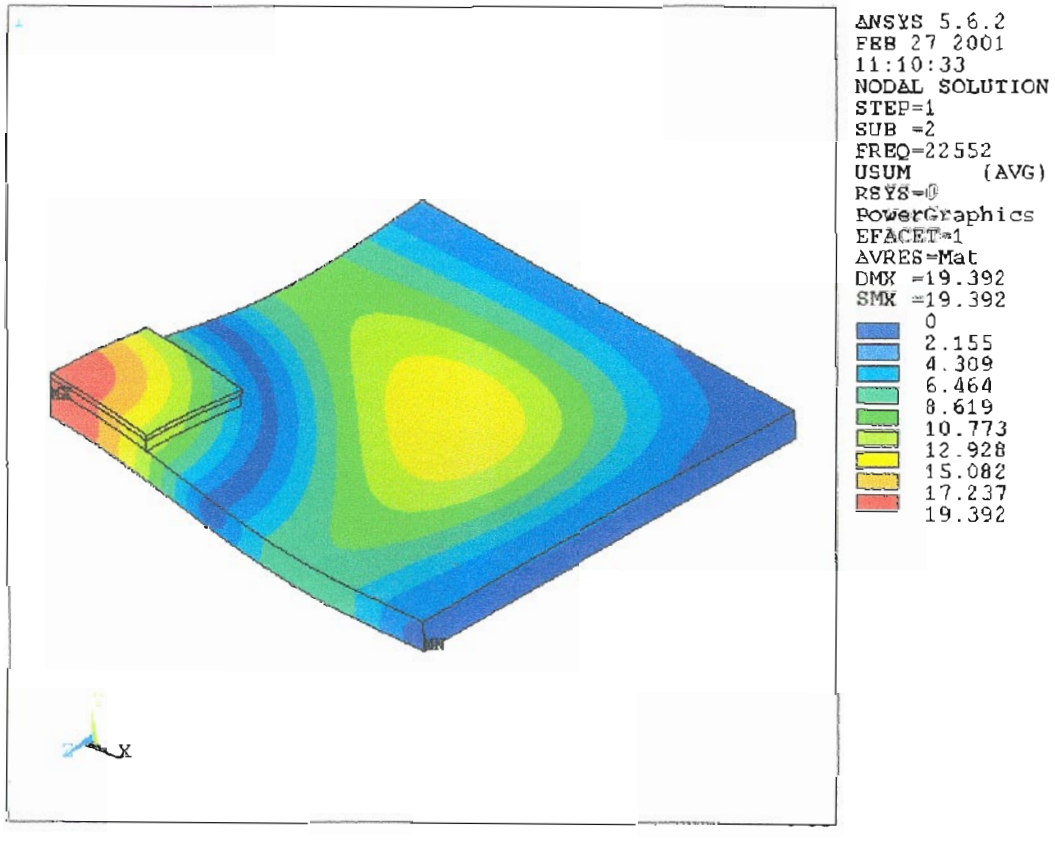


Figure 3-61 Vibrations - Second Mode – 3D –Quarter Symmetry Solder Interconnect

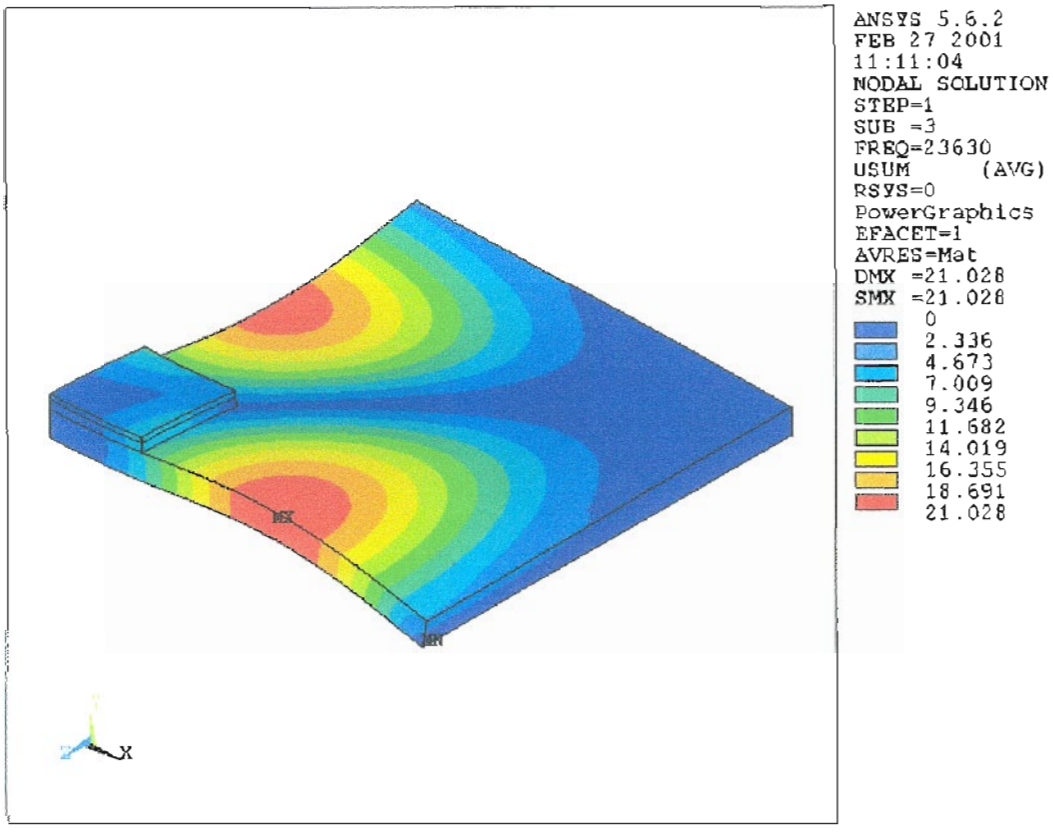


Figure 3-62 Vibrations – Third Mode – 3D –Quarter Symmetry Solder Interconnect

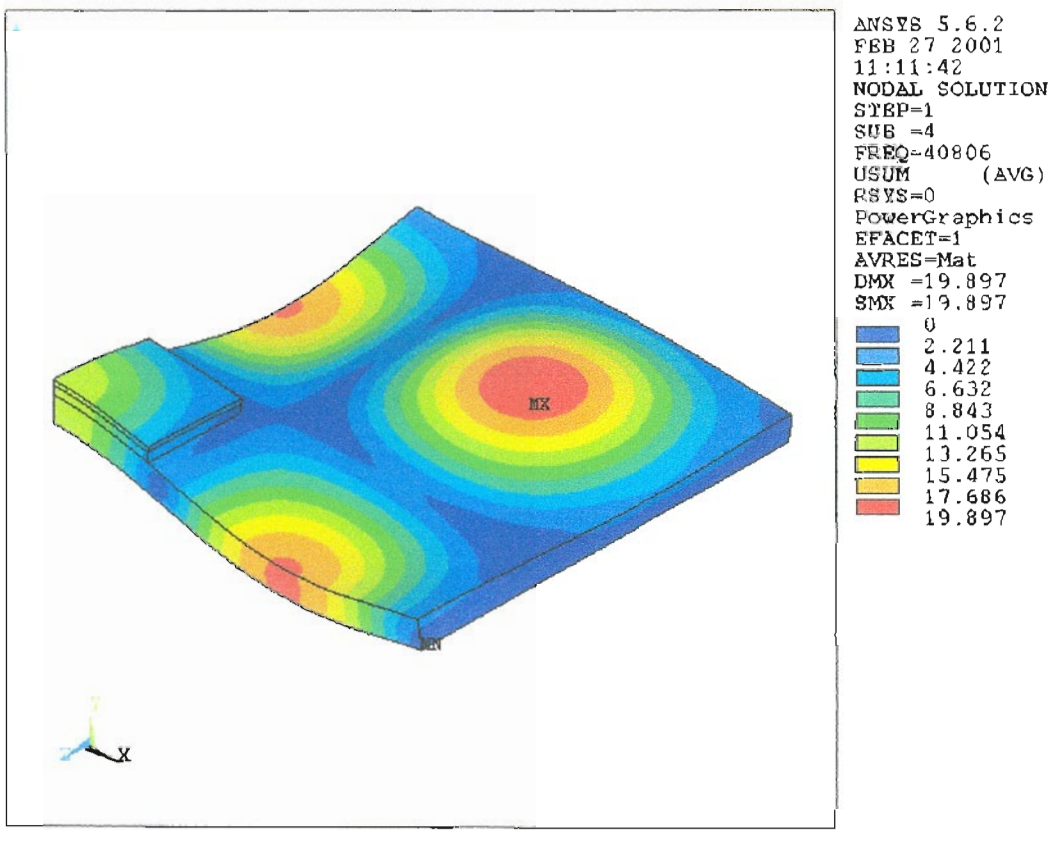


Figure 3-63 Vibrations - Fourth Mode – 3D –Quarter Symmetry Solder Interconnect

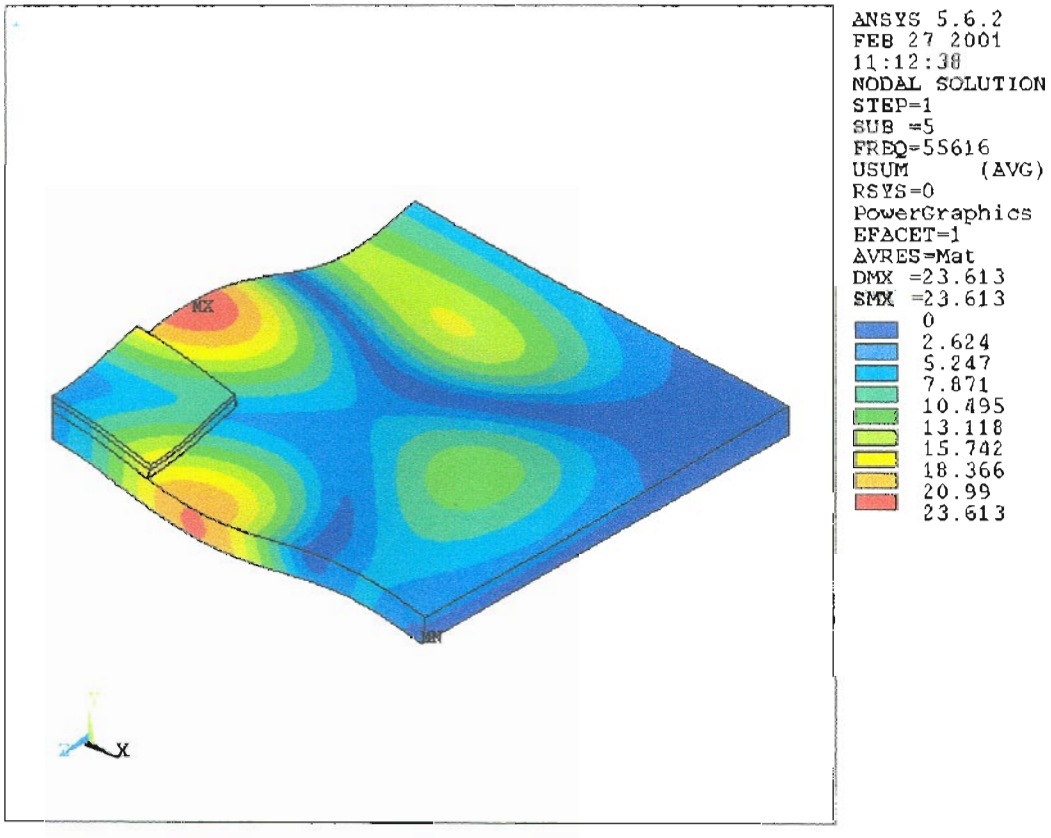


Figure 3-64 Vibrations - Fifth Mode – 3D –Quarter Symmetry - Solder Interconnect

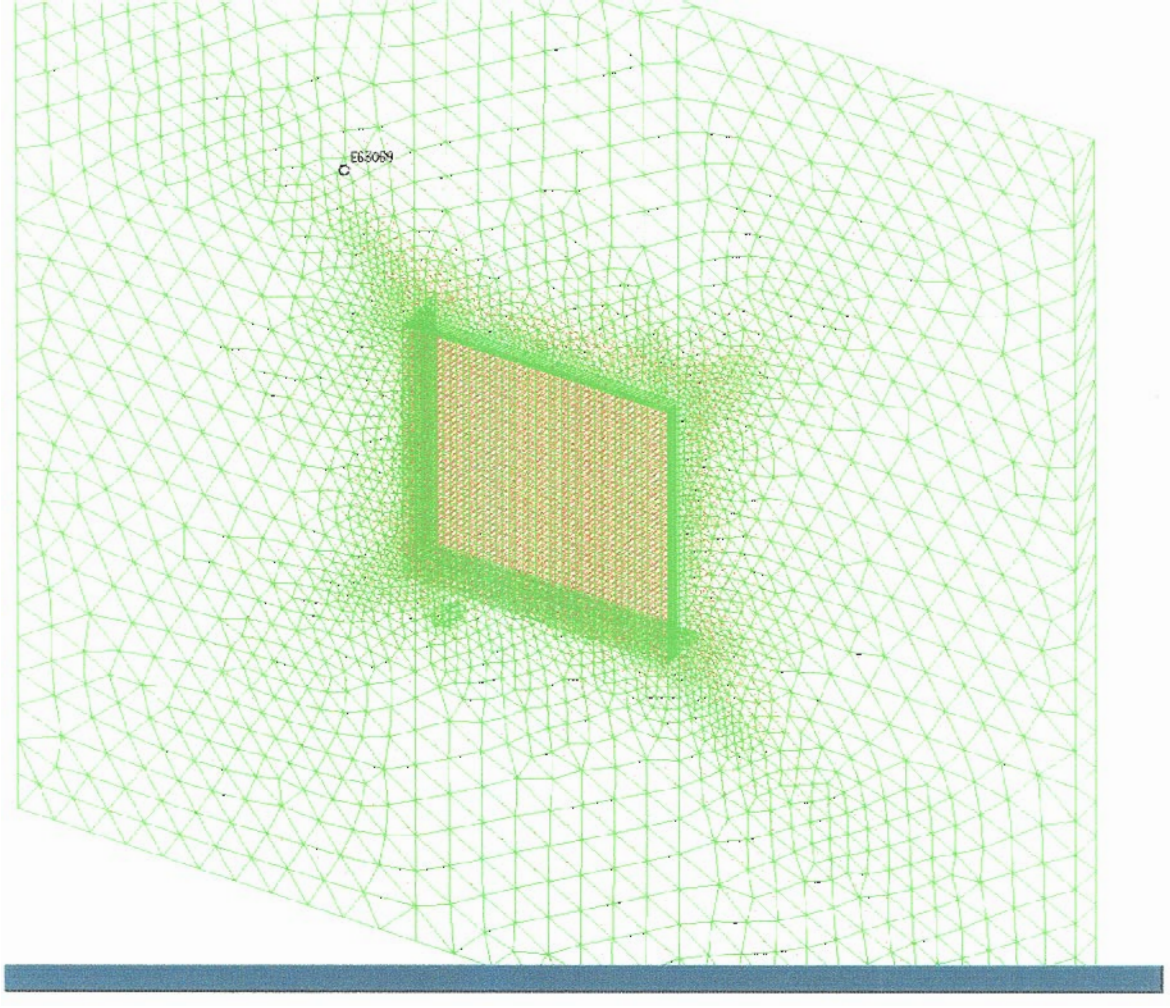


Figure 3-65 Mesh - 3D – IDEAS – Full Model - Solder Interconnect

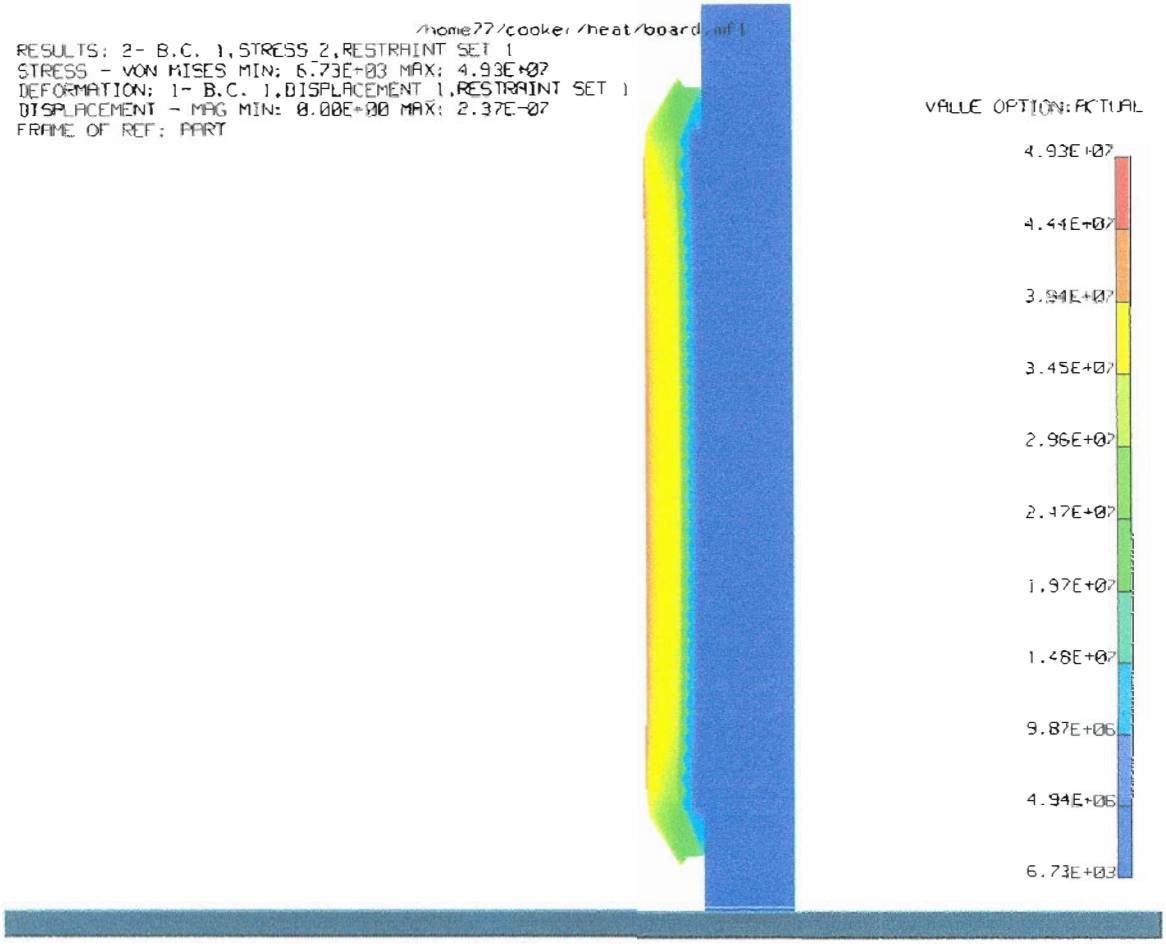


Figure 3-66 Side View Stress Distribution - 3D – IDEAS – Full Model Solder Interconnect

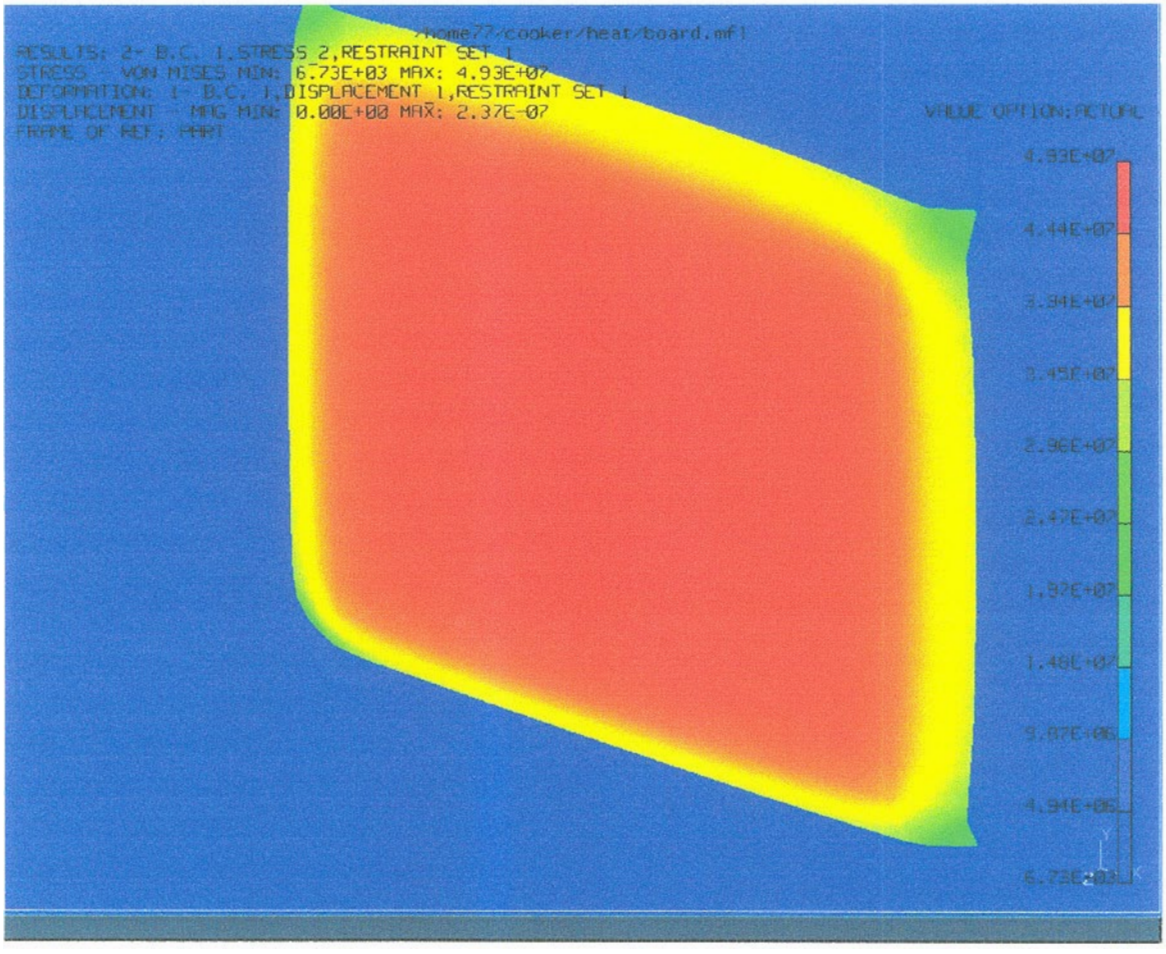


Figure 3-67 Isometric View Stress Distribution - 3D – IDEAS – Full Model Solder Interconnect

Table 3-1 Material Properties

PROPERTIES	UNITS	CHIP Si	SOLDER Sn60	WIRE Ag	BOARD BeO
Modulus of Elasticity	GPa	150	14.9	75.8	345
Density	Kg/m^3	2330	8470	10270	3000
Coeff.. of Thermal Exp.	$1/^oC$	2.5E-06	24.3E-06	18E-06	6.9
Initial Temperature	^oC	22	22	22	22
Poissons Ratio		.28	.29	.29	.3
Thermal Conductivity	W/m-k	148	50.6	419	175

Table 3-2 Different Wire Material Properties

PROPERTIES	UNITS	Silver Ag	Gold Au	Beryllium Copper BeCu
Modulus of Elasticity	GPa	75.8	82.7	110.3
Density	Kg/m^3	10270	19322	8249
Coeff.. of Thermal Exp.	$1/^oC$	18E-06	14.2E-06	17.8E-06
Initial Temperature	^oC	22	22	22
Poissons Ratio		.29	.29	.29
Thermal Conductivity	W/m-k	419	318	117

Table 3-3 Two-dimensional Wire Interconnect – Harmonic Response

TIME	AMPLITUDE UY	PHASE
3004.0	0.344485 μm	117.775
3008.0	0.344515 μm	117.524
3012.0	0.344534 μm	117.272
3016.0	0.344541 μm	117.019
3020.0	0.344538 μm	116.765
3024.0	0.344523 μm	116.511
3028.0	0.344497 μm	116.256
3032.0	0.344459 μm	116.000
3036.0	0.344410μm	115.743
3040.0	0.344349 μm	115.486
3044.0	0.344276 μm	115.228
3048.0	0.344191 μm	114.969
3052.0	0.344094 μm	114.710
3056.0	0.343983 μm	114.450
3060.0	0.343864 μm	114.190
3064.0	0.343730 μm	113.928
3068.0	0.343584 μm	113.667
3072.0	0.343425 μm	113.405
3076.0	0.343254 μm	113.142
3080.0	0.343070 μm	112.879

Table 3-4 Two-dimensional Solder Interconnect – Harmonic Response

TIME	AMPLITUDE UY	PHASE
2882.0	0.111816 mm	-84.6367
2884.0	0.111825 mm	-84.8273
2886.0	0.111832 mm	-85.0180
2888.0	0.111839 mm	-85.2089
2890.0	0.111844 mm	-85.4000
2892.0	0.111847 mm	-85.5913
2894.0	0.111850 mm	-85.7828
2896.0	0.111851 mm	-85.9744
2898.0	0.111851 mm	-86.1663
2900.0	0.111849 mm	-86.3583

Table 3-5 3 D – Quarter Symmetry - Numerical Model Statistics

Model	# of Elements	# of Nodes	DOF
Wire Interconnect	296412	327511	1199253
Solder Interconnect	37875	44646	116132

CHAPTER 4

EXPERIMENTAL APPROACH TO EMPHASIZE PRACTICAL APPLICATIONS

Interconnect technology is multidisciplinary in nature. For successful design in this area one should employ sophisticated knowledge in the areas of materials, mechanical engineering, electrical engineering, manufacturing and computer science. In addition in order to understand the impact of the chip technology on interconnect technology, it is important to understand the interrelationships between physical technology and logical technology.

The processor performance; millions of instructions processed per second (MIPS), is related to physical and logical technologies by the following equation, according to Hannemann, Kraus, Pecht [15]:

$$MIPS = \frac{10^6}{(fmc)\,(ct)} \qquad (4.1)$$

where,

fmc = number of fundamental machine cycles needed to execute the average instruction

ct = fundamental cycle time (the inverse of ct is typically the chip operating frequency).

The logical architecture determines fmc, and the cycle time is determined by the physical implementation technology. Hence either decreasing fmc or ct can improve the MIPS rating. This choice is made depending on cost and complexity of issues.

A good discussion of the relationship of physical, and logical design is given by Hannemann, Kraus, Pecht [15]. There are three fundamental problems to be considered for the physical architecture according to Hannemann, Kraus, Pecht [15]. First the interconnect function must be achieved (wiring problem). Second, the various signals in the systems must reach their destinations with well-understood timing

and with acceptable levels of distortion (signal integrity problem). Third, electrical power must be supplied, and removed to all circuits to allow operation at acceptable temperature levels (power management problem). In addition, size, cost, reliability, and weight provide the other physical technology constraints.

Considering the mechanical-structural functionality, the interconnect should possess the certain characteristics. The CTE should match the CTE of the board and the chip. It should have high thermal conductivity, so that the heat generated in the chip can be removed to the board or heat sink. The modulus of elasticity should be low, so that the stress-strain will be low. The fatigue properties of the wire should be able to withstand vibration and thermal cycling. The modulus of rupture and the fracture toughness need to be considered to prevent substrate cracking. The wire interconnect should be able to be soldered to the chip and the board with conventional solder technology. For the electrical functionality the interconnect should posses the following characteristic according to Hannemann, Kraus, Pecht [15] : Minimum electrical noise, minimum cross talks among conductors, and minimum signal propagation delay required by the circuit logic; Low ohm (DC) interconnect resistance, and low dielectric (AC) power losses. Additionally it should have controlled impedance match to the connected loads. Resistive (ohm) loss leads to heat generation, which increases the thermal load and attenuates magnitude of the signal level. Resistive (ohm) loss is a function of the resistivity of the conductor, interconnect length, diameter, and the current density. Dielectric loss is a function of the dielectric material surrounding a conductor, electrical frequency and power level. The interconnect impedance is a function of line resistance, capacitance, and inductance. The impedance is also affected by the structure of the interconnecting line, and its proximity to a ground plane. This study concentrates on the numerical simulation of thermal-structural aspects of the flexible interconnect. The experimental approach is not to verify the mathematical simulation; but to emphasize the practicality of the flexible interconnect mechanical design.

4.1 MECHANICAL DESIGN

In order to emphasize the practicality of this approach, it was necessary to demonstrate the idea, by making a non-working prototype wire interconnect. The anticipated difficulties was to confine the wires or bundle as a interconnect, prior to it being soldered to the chip and the board. A bundle of wires of diameter 0.05 mm and length 0.762 mm could not be handled manually or mechanically to be confined in to a metal ring. Hence, the mechanical design approach involved in experimenting with different methods of confining the wires together.

The first approach was to use a rolling process as shown in Figure 4-1. In this approach 0.381 mm diameter copper wires were inserted as a bundle in to a larger 19.05 mm copper tube as shown in Figure 4-2. The wires were tightly packed inside the larger tube. The tube diameter was then reduced through a deformation process of cold rolling where the outer tube and the inner wires were reduced in section by compressive deformation between the rolls. Normally cold working gives greater precision and finish, but requires very high pressures and the deformation is limited by work hardening. This attempt was not successful as the material cracked, as large local strains caused the material to tear back on it self.

The second attempt was to make a die as shown in Figure 4-3 (a), with the center hole of 19.05 mm diameter to hold the outer copper tube. The locating pins located the top half of the die to the bottom half. As before the wires were tightly packed inside the larger tube and the larger tube was placed in between the two die halves. With the 19.05 mm tube placed in the center a slight gap is retained between the two die halves. The complete die with the tube bundle in the center is placed in a hydraulic press, as shown in Figure 4-3(b) and pressure is applied to the upper die. Again this process was not successful as the tube cracked due to necking and the tube extruded in to the gap between the two dies. The next attempt was to combine the above two processes in a machine, in a series of steps. The machine selected was used to produce super-conducting wires. There are many different manufacturers of super-conducting materials and they use different process. The process used in this demonstration is called the Modified Jelly Roll (MJR) process.

4.2 MJR PROCESS

The patented MJR process researched by Smathers [50] , McDonald [34] , Lehky [28], Smathers [51],[49] is a process to produce fine composite wires from macroscale materials for Superconductors wires. The Jelly Roll is formed by wrapping alternate layers of copper sheet and expanded niobium mesh around a solid tin core rod, shown in Figure 4-4 (a)[49]. The Jelly Roll formed is inserted in outer copper tube, and the billet is formed ready for drawing, shown in Figure 4-4 (b)[49]. Figure 4-4 (c)[49], shows the billet being drawn to less than 13 mm in diameter. The rods approximately 13 mm in diameter, are cut to shorter lengths and re-bundled in another copper tube, shown in Figure 4-4 (d)[49]. This process is repeated for up to an additional 50 drawing steps to reduce material to wire 2 mm to 0.25 mm in diameter. The original niobium expanded mesh becomes extremely long filaments in the finished wire. A single diamond–shaped segment will be reduced from 6 mm to 1μm in cross section and elongated from 25 mm to 1.5 km, is shown in Figure 4-4 (e)[49].

4.3 DESCRIPTION OF PROTOTYPE

The purpose of the prototype interconnect is to simply demonstrate the feasibility of a bundle of thin wires being held together and inserted between the chip and the board. As demonstrated by the numerical simulation, the stress is reduced by two orders of magnitude by inserting a bundle of fine wires between the chip and the board; instead of direct soldering of the chip to the board. This prototype has not been developed as an interconnect with the ability to transfer electrical signals, or ready to be soldered between the chip and the board.

A sample interconnect was made from the MJR process and is shown in Figure 4-5. The sample has an outside diameter of 28.575 mm, with a 2.381 mm lip at the outer edge. The thickness of the interconnect (wire length) is 1.587 mm. It is feasible to machine the interconnect to 0.793 mm, without the bundle collapsing. The wires were made uniform, without sharp bends or cuts. As demonstrated the techniques and process used to make super-conducting materials can be developed as a viable process to make a flexible interconnect.

Superconductors are materials that undergo a transformation at reduced temperature which gives them the unique electrical properties including the ability to carry electrical currents without any resistance. Without resistance, electrical signals are not dissipated in the form of heat so all manner of electrical and electronic devices and components become far more efficient. There are thousands of superconductors that have been discovered over the decades, and there are many manufactures of super-conducting materials. However, there are no useful room temperature superconductors being discovered. Such a discovery would be very interesting and perhaps super-conducting flexible interconnects would be revolutionary as well.

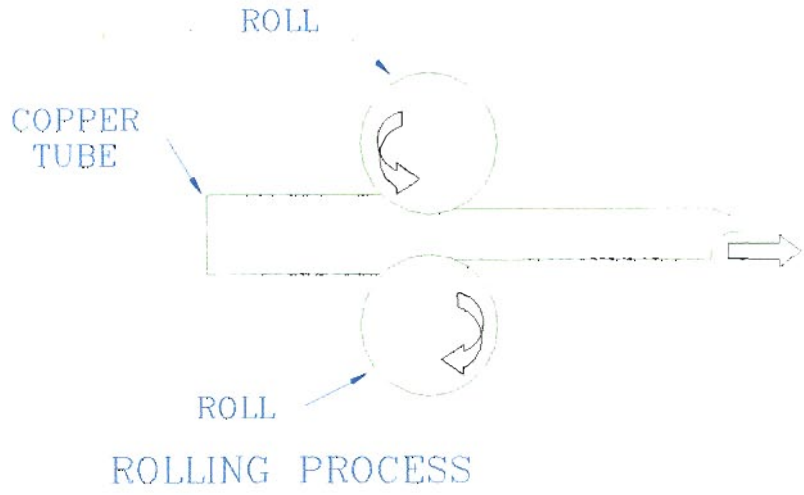


FIG. 4-1 Rolling Process

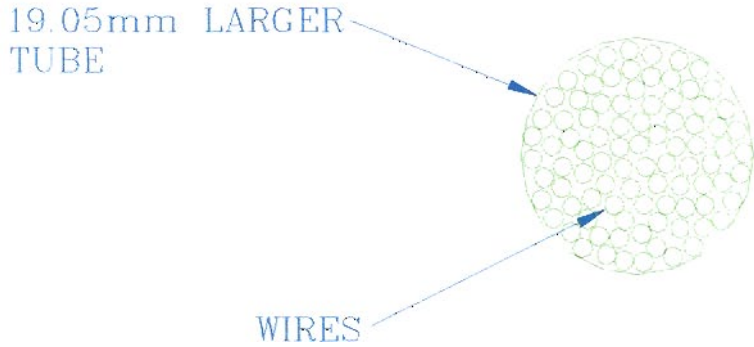


Figure 4-2 Large Copper Tube with Wires

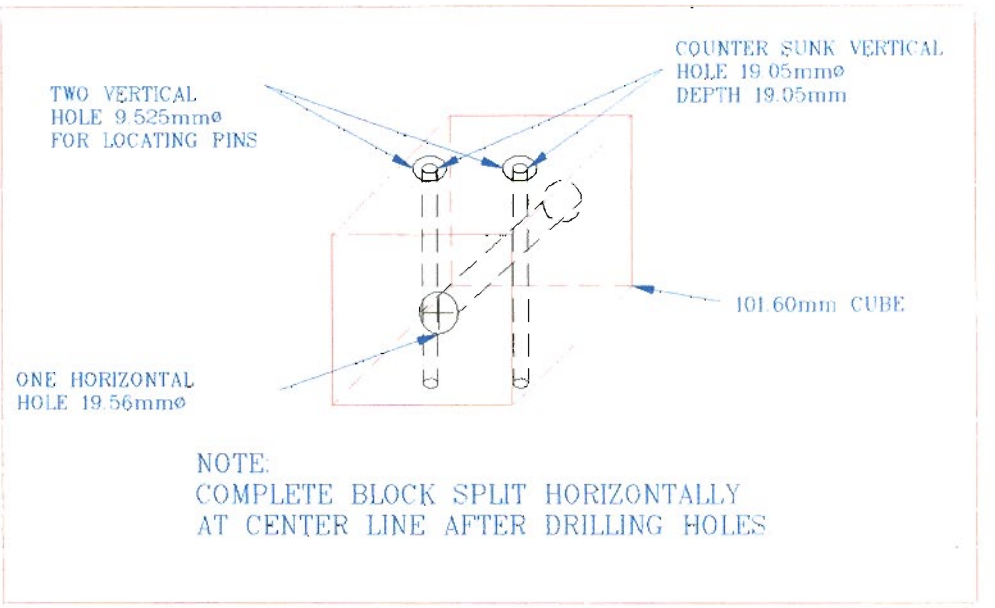


Figure 4-3 (a) Die

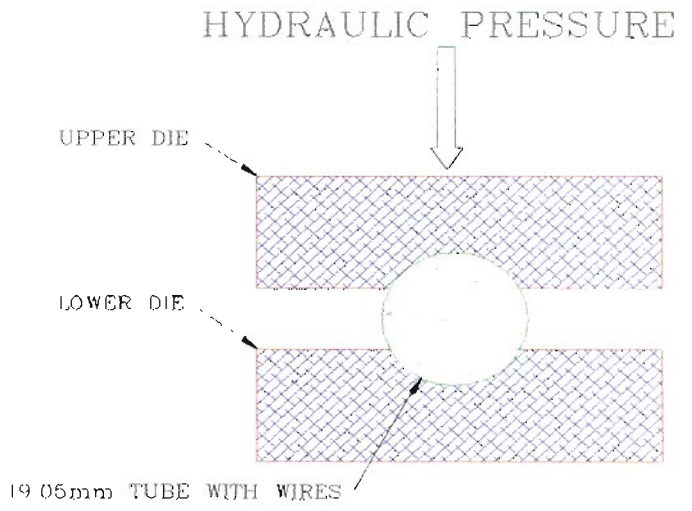
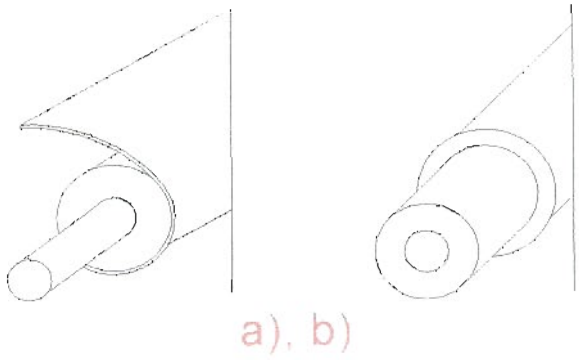
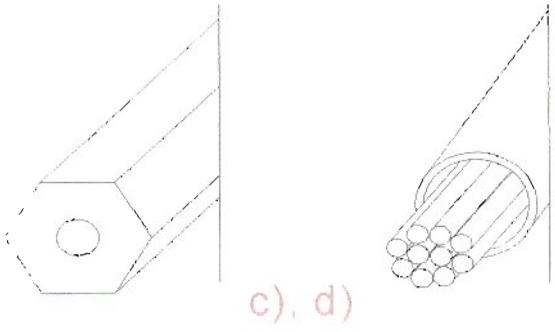


Figure 4-3 (b) Die used in Hydraulic Press





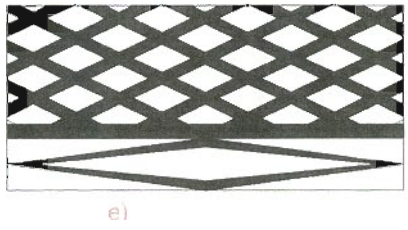


Figure 4-4 (a,b,c,d,e) MJR Process

(Adapted from Reference 49)

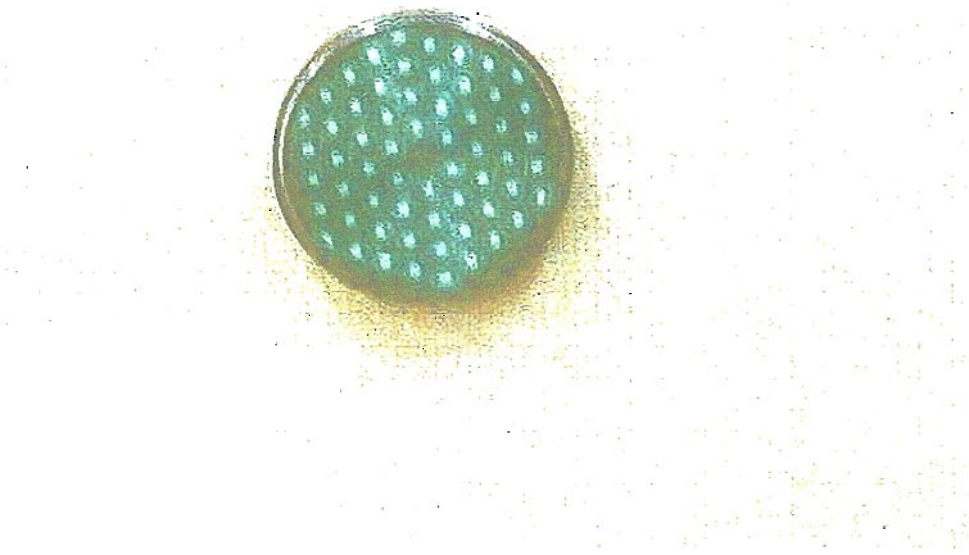


Figure 4-5 Sample Interconnect

CHAPTER 5

DISCUSSIONS OF RESULTS AND FUTURE RESEARCH

As analysts, we tend to forget that engineering is the attempt to idealize a very complex nonlinear world into a linear and simplified set of equations. In order to analyze we make assumptions and simplify the model. In some instances if we do not simplify, we may never be able to solve the problem. In others, we simplify to reduce the total node and element count, reducing computer analysis time. This introduces inaccuracies in functional performance especially in the areas so simplified. Likewise, the material properties are often simplified to a linear isotropic material. Loads and boundary conditions are applied at point locations. Singularities are anomalies that can produce gross errors in stress calculations, especially where very small structural element size requires the use of very fine mesh. When modeling a thickness of the order 0.025 mm, when four layers are used to obtain the stress distribution then each layer will have a thickness of only 0.000625 mm. The FEM model may have over 1000 of these small elements in a matrix. This typically leads to numerical instability in most computer programs. This instability is caused because the numbers are so small it is almost like dividing by zero. This can produce calculated stress values much higher than the true value. When a very fine mesh is used with a concentrated load, the elements in the immediate vicinity of the applied load will show very high stresses that are much higher than the true value, unless a nonlinear model is used. In this simulation, the thermal load was applied as a uniform temperature of 135°C on the chip. Some of these pitfalls were discussed in Chapter 2.

The numerical results from Chapter 3 are tabulated in Tables 5-1, 5-2, 5-3, 5-4.

5.1 THERMAL - STRUCTURAL RESULTS

Comparing the thermal analysis results for the two-dimensional models of the wire interconnect from Figure 3-6, and the solder interconnect from Figure 3-7, the temperatures of the solder joint is on an average 50°C higher than the wires. A similar trend is observed comparing the thermal analysis of the three-dimensional models for the wire interconnect in Figure 3-15, and solder interconnect in Figure 3-23. In this study the simulation was a pure conductive model. Table 3-1 shows that the conductivity of the silver wire is approximately 8 times higher than the solder. Since the board was a heat sink at 22°C, the heat was conducted faster through the wires. If convective heat transfer losses were also simulated, then the wire temperature would be lower, due to the fact that the gap between the wires would enhance a convective heat transfer mode. This would mean a much lower thermal stress in the wires.

The structural analysis results are tabulated in Table 5-1. From the two-dimensional model the average displacement in the wires in Figure 3-8 is approximately 1.2 μm, compared to the displacement in the solder joint in Figure 3-11 which is approximately 2.1μm (average of 2.8 μm and 1.4 μm). A similar effect is observed from the three - dimensional model, and they are as follows: the displacement in the wire interconnect in Figure 3-17 is 1.4 μm, and the displacement in the solder interconnect in Figure 3-25 is 2.3 μm. This difference would be expected, since from Table 3-1, the coefficient of thermal expansion of the wire is 18E-06/ ^{0}C, compared to the solder, from Table 1-3 is 24.3E-06/ ^{0}C. However, based on equation 2-29, from Chapter 2, the effect of the Modulus of Elasticity has to be taken in to account, when accounting for the stress in the wires. In addition the wire stiffness and the solder stiffness has to be considered accounting for the difference in stress, based on equation 2-28.

From the two-dimensional simulation, the Von Mises stress distribution in the wire interconnect is shown in Figure 3-9. This same stress value is shown only for the wires in Figure 3-10, and the average value of the stress in the wires is 0.1 MPa. The average value of Von Mises stress in the solder joint in the solder interconnect is approximated from Figure 3-12 as, 37.8 MPa. Thus, the two-dimensional simulation shows two order of magnitude reductions in stress in the wire interconnect. The corresponding three dimensional simulation of the wire interconnect, for the Von Mises

stress distribution, is shown in Figure 3-18. The average stress in the wires is shown in Figure 3-20, and the value is, 0.114 MPa. The Von Mises stress distribution for the solder interconnect is shown in Figure 3-26, and the average stress in the solder joint is 36.4 MPa. Again, two order of magnitude reduction in stress value in the wire interconnect, compared to the solder interconnect. The three dimensional simulation confirms the values obtained for stresses in the two-dimensional studies.
However, the location where the maximum stress distribution occurs in the two-dimensional simulation is exactly opposite to the location in the three dimensional simulation. In the two-dimensional simulation the maximum stress distribution is in the chip (Figure 3-9), and the minimum stress distribution is in the board. The stress is uniform in the chip, and the board. In the three-dimensional simulation, the chip has uniform minimum stress, and the board has higher stress in the vicinity where the chip is attached. This high stress in the board could be the result of the wires constraining the board from expanding freely, as a result of the fixed boundary condition on the board. The three-dimensional simulation in Figure 3-31 shows the Z-direction stress distribution as compressive. This is the out of plane stress at the symmetry boundary condition. This effect could be observed in the two-dimensional simulation, in Figure 3-10, where the stresses in the wires are shown. However the compressive stress in this case occurs in the free outer edge. These differences are due to the symmetry boundary conditions being enforced. The edge effects are simulated in the three-dimensional model. Thus, though the numerical stress values between the two-dimensional and three-dimensional simulations are close; the two-dimensional simulation does not capture the behavior of the model.

It is also emphasized that coefficient of thermal expansion varies in the three orthogonal directions. In this study only an isotropic value was used for the coefficient of thermal expansion. Both the two-dimensional, and the three-dimensional simulations, confirm, that the stress in the wire interconnect is reduced by two orders of magnitude, compared to the solder interconnect.

5.1.1 DIFFERENR WIRE MATERIAL RESULTS

Results are tabulated in Table 5-2. The wire diameter for the three different materials was the same, 0.05 mm. The thermal analysis results for silver, gold, and beryllium copper are shown in Figure 3-15, Figure.3-28, and Figure 3-33 respectively. The temperature distribution results do not show any marked variations in the wire temperature with material. However, the temperature distribution in the board between beryllium copper and the silver shows a change in temperature profile. From Table 3-2, the thermal conductivity of silver is 419 W/M-K, and beryllium copper is 117 W/M-K. This difference could cause the change in the temperature profile in the board.

Comparing the displacement values in the wires between silver, 1.41 μm in figure 3-17, gold, 1.37 μm in Figure 3-29, and beryllium copper 1.37 μm in Fig. 3-34, the displacements do not show much difference, except for the slightly higher value for silver.

Comparing the stress values in the wires between Silver, 0.114 MPa in Figure 3-20, Gold, 0.078 MPa in Figure 3-32, and Beryllium Copper 0.310 MPa in Figure 3-37, the stress values show considerable difference. These values have to be evaluated comparing their properties as given in Table 3-2; particularly the modulus of elasticity, coefficient of thermal expansion, and thermal conductivity. The modulus of elasticity between silver (75.8 MPa), and gold (82.7 MPa) are much closer than for beryllium copper (110.3 MPa). The thermal conductivity between silver (419 W/M-K), and gold (318 W/M-K), is much higher than for beryllium copper (117 W/M-K). Beryllium copper has much lower thermal conductivity, hence higher values for temperature distribution in the wires. Comparing the coefficient of thermal expansion between silver (18E-06 / °C), and beryllium copper (17.8E-06 / °C), with gold (14.2E-06/°C), gold has a lower coefficient of thermal expansion. Lower coefficient of expansion means lower displacement. Lower value of modulus of elasticity combined with lower value of coefficient of thermal expansion means lower value of stress as discussed in equation 2.27. In addition, higher the value of thermal conductivity for gold, lower the temperature in the wires. Hence, the combined effect of these properties show that the use of gold wires reduces the stress in the wires by an order of magnitude compared to

the use of silver or beryllium copper. However, gold is an expensive material, and the use of gold as a possible candidate for interconnect material is not feasible.

The basic mechanical properties of materials and other relevant properties such as malleability and brittleness need to be considered when selecting wire material. As discussed in chapter 4 to make a bundle composite the wire has to go through a wire drawing process. When the wire thickness reduces to the order of 0.05 mm, it should not be brittle. In addition to other advantages of using wire interconnect, as discussed in section 5.2, the increase in fatigue life due to the reduced stress, is a major design improvement.

5.1.2 DIFFERENT WIRE DIAMETER RESULTS

The effect of changing the wire diameter could have various impacts on the design. These could be reducing or increasing the stress, changing the weight of the component and increasing the ease of manufacture. For this study, only one other wire diameter was considered, 0.5 mm and the material for the wire was silver. Hence the results could be compared with Figure 3-15 through 3-20. The only difference between these two sets of results is the wire diameter being increased from 0.05 mm to 0.5 mm.

In order to reduce the computing cost and the time, the use of changing the wire real constant, and thus the stiffness of the wires, was used. However, it should be emphasized that this approach is not quite correct, and the implications need to be discussed. Changing the stiffness of the wires, without changing the geometry, does not account for the change in the space between the wires. Thus the results from this part of the simulation should be considered for qualitative comparisons only.

The results are tabulated in Table 5-3. Comparing the temperature distribution for wire diameter 0.05 mm (Figure 3-15) with temperature distribution for wire diameter 0.5 mm (Figure 3-38) there is no difference. As explained previously this should be expected, since the geometry was not changed. If the geometry was changed, then it would effect the area of the wire, and thus the bulk thermal conductivity, and hence the temperature distribution. In addition, if heat transfer due to convection mode were simulated, the gap between the wires would effect the cooling of the wires. This would

have a marked change in the stress calculated, due to lower values of temperature distribution.

In Table 5-3, it is seen that the displacement for wire diameter 0.05 mm is 1.41 μm, compared to 1.63 μm for wire diameter 0.5 mm. The average stress in the wires for the wire 0.05 mm was 0.114 MPa and for the 0.5 mm wire the stress is 0.351 MPa. Hence the displacement is slightly higher where as the stress is approximately three times higher. Hence, it could be inferred that increasing the wire diameter by 10 times, increases the stress in the wires by approximately 3 times.

5.2 VIBRATION RESULTS

Vibration induced failures are caused by the relative motion that develops between the chip, the wires and the board. Materials can fracture when they are subjected to repeated stresses that are considerably less than their ultimate static strength. The failure appears to be due to submicroscopic cracks that grow into visible cracks, which then leads to a complete rupture under repeated loading. As discussed in section 2.4.4, the location, orientation of attachment of the component, and the elongation of the board which are important, and not the stresses of the board.

Predicting the fatigue life in thermal cycling and vibration environment is complicated. When the board is excited at its resonant frequency, the resonant frequency of the board must be determined in order to obtain approximate fatigue life relations. In this study the stresses due to vibration environment was simulated (modal and harmonic analysis) for both the two-dimensional models of the wire interconnect and the solder interconnect. In three-dimensional simulation, only modal analysis was performed for the solder interconnect. Subjected to the boundary and loading conditions as given in Section 3.6, results were obtained and tabulated in Table 5-4. For the two-dimensional simulation; the lowest natural frequency for the wire interconnect was 3153 Hz, compared to 2917 Hz for the solder interconnect. This was the value if for entire board with the components attached to it. The increase in natural frequency is due to the increase in stiffness caused by the wires. The corresponding value from the three-dimensional simulation, for the solder interconnect, is 5618 Hz. The natural frequency value from the three-dimensional simulation for the solder interconnect is approximately

twice as that from the two-dimensional simulation. The vibration analysis using the two-dimensional analysis gives insight in to the expected difference in stresses between the wire interconnect and the solder interconnect.

The maximum displacement in the wire interconnect is 1.96 μm, compared to that in the solder interconnect which is 0.112 mm. As discussed in section 2.4.4, higher the natural frequency, the lower the displacement and lower the strain in the chip. Comparing the stresses, the wire interconnect has a maximum stress value of 14.4 MPa compared to the solder interconnect which has a maximum stress value of 202 MPa. Higher the natural frequency, lower the maximum deflection, and lower the stresses. Hence, a vibration load of magnitude 7 G, produces stress in the wire interconnect one order of magnitude lower than that in the solder interconnect. Since the three-dimensional analysis predicts much higher natural frequency, it would be expected that the stress values due to vibration loads in both wire and solder interconnect would be much lower than the values obtained from the two-dimensional simulation.

5.3 MODEL VALIDATION RESULTS

For a complicated geometry, numerical validation using other computer programs, or published data may not be possible. In this study only the solder interconnect results is validated. The peak stress determined for the solder interconnect 36.4 MPa is in excellent agreement with the work of Nakagawa, Sawa, Nakano, Hagiwara [37]. Their peak stress in solder joints assumed to be defect free is $\sigma_1 = 35.8$ MPa. Nakagawa, Sawa, Nakano, Hagiwara [37] numerical results were compared with experimental measurements using two- dimensional photo-elasticity and were found to be in excellent agreement.

The fact that different computer programs have different capabilities and limitations will not simulate the model to the same accuracy. However, as in this study the results could give qualitative numerical values to cross check the model. From the IDEAS program simulation of the full three-dimensional solder interconnect, the stress in the solder joint from Figure 3-66, and Figure 3-67 is 34.5 MPa. The corresponding value of stress in the solder joint obtained from the ANSYS program simulation of the quarter symmetry solder interconnect, is shown in Figure 3-26 and it is 36.4 MPa. The stress values are of the same order of magnitude, though the actual value from the ANSYS

program simulation is only 1.9 MPa higher than that obtained from IDEAS simulation for the solder interconnect. Comparing the two numerical simulations the error of 5.2% was acceptable. It is a standard practice in the electronic industry to require that the analysis to agree within + or – 10% of the qualification test values. Typical example would be the temperature of a component. Though the analysis in this study did not use a qualification test, an error of 5 % is acceptable for the model validation. The IDEAS simulation was for a full three-dimensional model, compared to the ANSYS simulation, which was for a quarter symmetry three-dimensional model. As discussed in Section 5.1, part of the error could be attributed to the out of plane stresses at the symmetry boundary condition used in the ANSYS model.

The three-dimensional wire interconnect model was not validated. However, the validation of the solder interconnect of the ANSYS simulation, could justify the acceptance of the ANSYS simulation of the wire interconnect.

5.4 EXPERIMENTAL APPROACH RESULTS

The experimental approach in this study was to emphasize the practical aspects and the potential of wire bundle interconnects and not the design of an actual functioning interconnect. As mentioned in Chapter 4, the design of a functioning interconnect is multidisciplinary in nature, and it is quite involved. Considering only the manufacture, the MJR process seems to be a promising candidate to be readily adapted for manufacturing wire interconnects.

The experiment confirmed that interconnect wires or fibers can be confined in a bundle, and the manufacturing technology is readily available. It is feasible to adapt the MJR process to produce wires made of gold, aluminum, copper and other materials. The wires can be produced uniformly and consistently. Manufacturing wires without sharp bends or cuts would prevent wire failure. For electrical power and signal transmission, the wires can be insulated. Further, the manufacturing process can be easily adapted for manufacturing insulated interconnection wires.

5.5 CONCLUSION

The chips, mounted on the board must be attached in such a way as to provide electrical connections and power supply connections to each chip. Since each chip may dissipate as much as 200 Watts of power, large thermal stresses can be set up in the connections made to the chip. Thermal stresses are created due to the mismatch in coefficient of thermal expansion (CTE) between the chip, board, solder joint and lead wires. In addition the systems containing these modules is cycled on and off, causing cycled stress, and the module can fail from fatigue.

From the numerical analysis done in this dissertation it is confirmed that replacing the solder interconnect with a wire or flexible interconnect would reduce the thermal stress due to the difference in coefficient of thermal expansion between the chip and the board by two order of magnitude. In addition the wire interconnect could replace the lead wires, transmitting signals, and providing power supply to the chip. There is more research and design related work to be completed in the areas of electrical, mechanical, materials, computer science and manufacturing engineering and few of them related to numerical simulation are mentioned in Section 5.6.

5.6 FUTURE RESEARCH

In this study the thermal model considered only conduction heat transfer process. However, for correct house keeping of energy losses, the convective heat transfer losses has to be accounted for. Hence the future numerical simulations have to account for heat losses due to convection from the gaps between wires in the wire interconnection. This will have the effect of lowering the temperature of the wires, and hence lower the thermal stress in the wires.

The numerical simulation in this study is based on linear isotropic material properties, and on linear static analysis. However, as explained, non-linear material properties, including temperature dependent thermal conductivity, density, heat capacity, and coefficient of thermal expansion has to be accounted for. The coefficient of thermal expansion, and thermal conductivity vary in each of the 3 orthogonal directions. The failure mechanisms are different in these three different directions. Hence, future

numerical simulations should account for the different dimensional changes that occur in the three different coordinate directions.

If the interconnect length is increased, interconnect resistance is increased. Due to the increased resistance the resistive capacitance (RC) time constant is increased, contributing to signal propagation delay. In this study the interconnect wire length was kept constant at 0.762 mm, as shown in Figure 3-3. Future simulation should vary the interconnect length, and study its effect on both mechanical stress, and electrical signal transmission. Also the effect of wire length on manufacture, and its effect on the solder at both ends has to be investigated.

A uniform temperature of 135°C was prescribed to the chip. The board was the heat sink maintained at 22°C. Future simulations should vary these two temperatures, and study for thermal and power cycling effects. The chip could be simulated for heat generation rather than with uniform temperature and this will provide with the maximum temperature with in the chip.

This simulation considered three different material types. Future simulations should consider new materials and aluminum, which is a standard lead wire material in the electronic industry at present. Only two different wire diameters were considered. Future studies should consider different wire diameters, and optimize for length, diameter, and spacing between wires.

The modal and harmonic analysis in this study was limited to two-dimensional simulation. Only the quarter-symmetry three-dimensional model of the solder interconnect modal analysis was done. Future simulations should include both modal and harmonic analysis using the quarter symmetry three-dimensional models for both the wire and solder interconnects.

Table 5-1 Structural Analysis Results

	Two-dimensional		Three-dimensional	
	Wire Interconnect	**Solder Interconnect**	**Wire Interconnect**	**Solder Interconnect**
Average Stress MPa	0.113	37.8	0.114	36.4
Displacement (μm)	1.21	2.1	1.41	2.31

Wire Material – Silver

Wire Diameter – 0.05 mm

Table 5-2 Different Wire Materials Results

	Silver Ag	**Gold Au**	**Beryllium Copper BeCu**
Average Stress (MPa)	0.114	0.078	0.310
Displacement (μm)	0.14	0.13	0.13

Wire Diameter – 0.05 mm

Table 5-3 Different Wire Diameter Results

	0.002 inch	**0.02 inch**
Average Stress (MPa)	.114	.351
Displacement (μm)	1.41	1.63

Wire Material – Silver

Table 5-4 Vibrations Analysis Results

	Two-dimensional		**Three-dimensional**
	Modal Analysis		
Frequency (HZ)	**Wire Interconnect**	**Solder Interconnect**	**Solder Interconnect**
1st Mode	3153	2917	5618
2nd Mode	6134	19837	22552
3rd Mode	12972	51358	23630
4th Mode	20575	87414	40806
5th Mode	52127	113600	55616
	Harmonic Analysis		
Maximum Stress (MPa)	14.4	202	-
Maximum Displacement (μm)	1.96	112	-

Wire Material – Silver

Wire Diameter – 0.05 mm

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