HIGH FREQUENCY CHARACTERIZATION AND MODELING OF ALGAAS/GAAS HBT DARLINGTON FEEDBACK AMPLIFIERS

Ding Li

B.S., Suzhou University, China, 1982

M.S., Shanghai Institute of Laser Technology, China, 1987

MSEE, Oregon Graduate Institute, Portland, Oregon, 1993

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The dissertation "High Frequency Characterization and Modeling of AlGaAs/ GaAs HBT Darlington Feedback Amplifiers" by Ding Li has been examined and approved by the following Examination Committee:

Raj Solanki, Dissertation Adviser
Associate Professor

V. S. Rao Gudimetla
Assistant Professor

Anthony E. Bell
Associate Professor

Dr. Sudarsan Uppili
Tektronix, Inc.

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DEDICATION

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ABSTRACT

HIGH FREQUENCY CHARACTERIZATION AND MODELING OF ALGAAS/GAAS HBT DARLINGTON FEEDBACK AMPLIFIERS

Ding Li

Supervising Professor: Raj Solanki

High frequency (1 GHz - 20 GHz) S-parameter data were collected from a novel circuit configuration of AlGaAs/GaAs HBTs combined as Darlington feedback amplifier for the use of high frequency characterization of such devices, which is believed to be important for understanding of the high current capabilities and improving the integration of multi-stage HBT amplifiers. An analysis using SuperCompact simulation software as a guide led to the formation of a new small-signal two-stage hybrid-π model that precisely simulated the observed S-parameter characteristics. The simulation was accomplished at two different bias conditions. Investigations of these modeled element values have shown some interesting device physics. In particular, (a) the large deviation of second stage collector-base junction capacitance value from the well-known reciprocal square-root C-V relationship at the higher bias implies the influence of some transistor high-injection effects or doping profile modification effect; (b) the unusual reverse-directional change of

the second-stage base resistance (increase instead of decrease in the presence of larger emitter area and more fingers) is attributed to the localized heating and current crowding effects, which may result in Kirk effect at relatively low collector current. Moreover, the commonly observed increase of the resistive element values at the higher bias indicated the thermal effect on sheet resistance.

The same kind of device but packaged this time was used for high-speed switching analysis, which has been currently less investigated for HBTs. This analysis was based on the TDR (time domain reflectometer) measurements and previous model. A new analysis technique is proposed here specially for small-signal (low-level) switching performance analysis, and characterized by separating the input from output loop, which significantly simplifies the circuit complexity. The hybrid-π model is found to be a good model in completing this task. Several different approaches achieved led to quite consistent results which also match the experimental data and Spice simulation results well. In this investigation, the parasitic load capacitance C_L is found to be the most sensitive element to affect the speed. The transconductance g_m (or the current gain β) and the voltage gain are the main intrinsic parameters contributing to the delay performance. For HBTs, the collector-base junction capacitance appears to be the dominant factor limiting the intrinsic switching speed, specially in the case that a large output-input voltage ratio is expected.

CHAPTER I

INTRODUCTION

After a long term of research and development since its becoming a reality with the advent of molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) technologies in the mid-70's, heterojunction bipolar transistor (HBT) — a concept as old as the transistor itself[1-3] — has more and more proved itself as one of the most promising semiconductor devices with its prominent performance in many aspects over its homojunction competitors.

The unique feature of a HBT is its wide-gap emitter. By creating a band-gap difference on the different sides of base-emitter junction, a series of significant changes have occurred and a number of advantages can thereby be achieved.

First of all, electron injection efficiency is significantly raised in a heterostructure bipolar transistor while the back injection is effectively impeded due to the gap variations, which enables one to achieve an extremely high current gain. From another point of view, it can be taken as a trade-off to achieve a very high base doping without degrading the gain too much. Once a very highly doped base is available, a very thin base can be made without increasing the base layer sheet resistance. As is well-known, a thin base layer will cause a lower base transit time, which is considered as a main interior speed limit. Meanwhile, a high base doping allows one to have a relatively thick base-emitter depletion layer with most part of it located inside the lightly doped emitter region, hence a low junction

capacitance. Since the base resistance is reduced, the whole emitter area can conduct current easily such that its capability to handle large current is largely raised. Other desired features such as low base-collector junction capacitance, a desired level of collector breakdown voltage, low surface recombination and bulk generation effects, can also be achieved by optimizing the device parameters in the fabrication of HBTs.

Among the different material combinations for a heterostructure emitter-base formation, the AlGaAs/GaAs system appears to be the most promising since its prominent ability in achieving a good lattice match between $Al_xGa_{1-x}As$ and GaAs without introducing severe interface state effects as well as providing a desired semi-insulating substrate. More important, a relatively high electron mobility in GaAs contributes to a very low base transit time in a n-p-n transistor.

As a bipolar transistor, HBT retains most of the behaviors of a BJT. But for cost consideration, HBT finds its special applications in microwave and millimeter-wave frequency range with its particularly high f_{max} and f_t features.

As a III-V device, GaAs HBTs offer many important advantages over GaAs MESFETs and HEMTs. Some of those advantages, for example, are[4]: (a) The vertical structure of a HBT allows that the thin base layer can be easily realized by epitaxial growth with relaxed lithographic dimensions in achieving microwave and millimeter-wave frequency capabilities; (b) The HBT's higher transconductance g_m (10-100 times greater, depending on the output current) permits small input voltage swings and facilitates low (common-collector) output impedance for fast charging of load capacitances in ICs; (c) The lower (common-emitter) output conductance g_o of the HBT resulted from the highly doped base yields high device linearity and dc voltage gain, important in analog applications. Other advantages include stable turn-on voltage, low $1/f$ noise and trapping effects, higher current capability per effective transistor area, and greater radiation hardness.

With all these important features, HBT is finding its widespread applications in many circuits. HBT is a generic candidate in microwave circuits, and can be used in amplifier, oscillator, and mixer. Another promising application of HBT is in high speed digital circuits where high performance emitter-coupled logic (ECL) and integrated-injection logic (I^2L) can be implemented by HBTs to achieve LSI-VLSI capabilities[5]. For an amplifier, the highest performance of a GaAs HBT is in power amplifier circuits because of its high current and voltage capabilities[6-8]. Wideband amplifier is another example making HBTs attractive since its high intrinsic gain, high speed, and freedom from trapping effects. Broadband amplifier performance from dc to 20 GHz has been realized by a very simple, monolithic, Darlington-coupled feedback amplifier design using two-quad $3 \times 10\mu m^2$ emitter HBTs and no I/O matching[9]. These amplifiers demonstrate significantly improved bandwidth over advanced Si bipolar[10], and reduced size and power over conventional MESFET approaches that use passive matching networks. For this reason, AlGaAs/GaAs HBT Darlington feedback amplifier has been chosen here as the device under investigation. Some other motivations for this are further elucidated later on.

Driven by the practical needs, a lot of papers have been published on HBT device characterization. Most of them, however, focused on carrier transport mechanism studies and dc analysis to achieve Ebers-Moll (EM) or Gummel-Poon (GP) alike models[11-18] rather than high frequency/speed characterization though the latter is very important for device designs. Although not the only way in use[19-22], equivalent circuit method combined with computer-aided simulation is a most effective approach for microwave device modeling, in which the device is modeled by an equivalent network, and by the aid of some kind of simulation software, a match between measured data and modeled results can be finally achieved, and a set of circuit parameters can thus be obtained to characterize the device. This approach is most appropriate for characterizing a specific device, and the device parameters obtained in this way are often quite useful in improving the device design.

In this dissertation, the AlGaAs/GaAs HBT feedback amplifier is first time characterized in GHz frequency range, and simulated by a lumped small-signal two-stage hybrid-π equivalent circuit model achieved by using SuperCompact software. The simulation results bring about an excellent agreement with the measured two-port high frequency parameters (S-parameters). Subsequent switching analysis of the same kind of device is implemented based on high speed pulse response measurements, and also is first time reported in this area. Choosing Darlington configuration device as a study object is based on such an idea that since Darlington pair is not only a very popularly used device but also a simplest unit circuit with two stage amplifiers cascaded, it may be a good candidate for multistage HBT studies, which is commonly considered very important for the integration of HBTs. While Darlington device is not an ideal switching device, it is still helpful for one's better understanding of the switching mechanism of HBTs since the device can be considered as a composite transistor.

This dissertation is organized as follows: In Chapter II, the general ideas of a HBT are reviewed. Chapter III introduces some conventionally used device models, such as T-model, hybrid-π model, high frequency small-signal model, and charge-control model. Parasitics limiting the high frequency performance of HBTs are also discussed in this chapter.

In Chapter IV the state-of-art high frequency measurement techniques are introduced. S-parameter concepts and basic microwave circuit theories are reviewed too.

Chapter V is the main part of this dissertation, where the AlGaAs/GaAs HBT Darlington-pair feedback amplifier is under high frequency characterization. The S-parameter measurements were implemented using HP 8510 network analyzer combined with Cascade Microtech microprobe systems, and the device was successfully simulated using SuperCompact simulator. The subsequent investigations of the obtained model parameters have given a clear picture how the device performanced.

Chapter VI copes with another topic of this project, which is primarily a time domain problem. The same kind of device but packaged at this time was characterized at high speed using Tektronix digital sampling oscilloscope at its time-domain reflectometry (TDR) mode. Based on the previously obtained model and parameters, a transient analysis of the device under measurement environment was accomplished by implementing a new analysis method. The extrinsic and intrinsic speed limitations are discussed and a very good consistence among the model, Spice simulation and the experimental results reveals the switching mechanism of the HBT device in detail, which is believed to be instructive in switching circuit design.

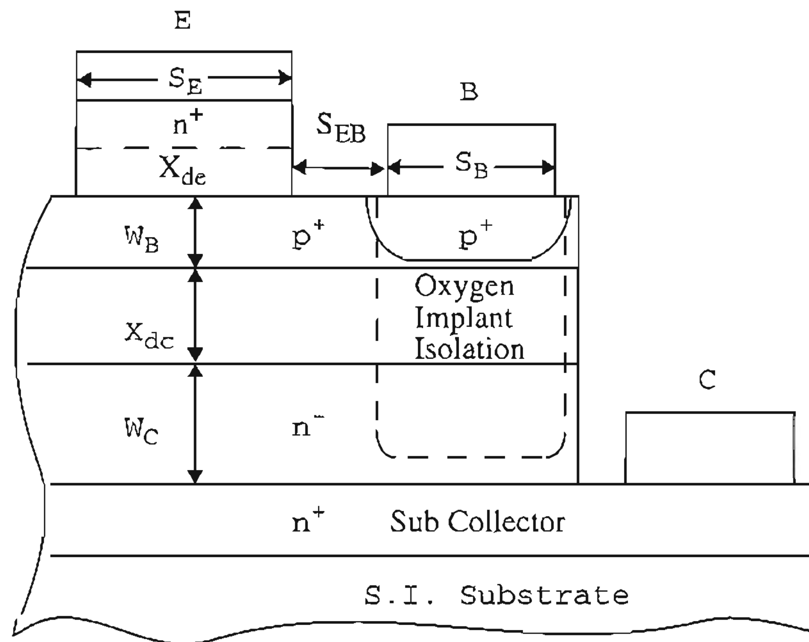
CHAPTER II

HETEROJUNCTION BIPOLAR TRANSISTOR

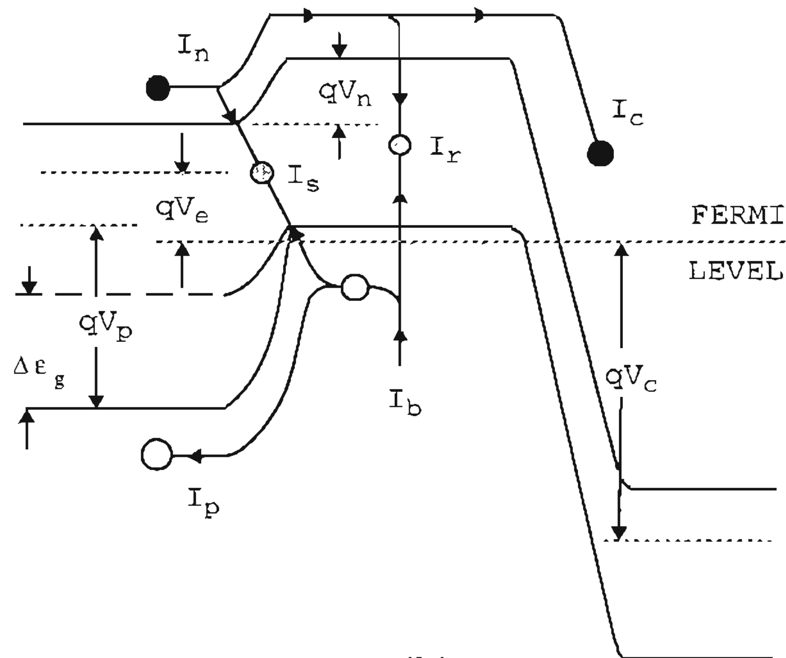
2.1.0 What is a HBT?

A typical HBT consists of a minimum of five epitaxial layers. The cross-sectional schematic diagram is shown in Figure 2.1(a). The emitter layer is comprised of an "emitter-cap" layer and a wide band-gap emitter layer underneath. The cap layer is used to make low-resistivity ohmic contacts to the emitter. This layer often consists of high-conductivity GaAs with a thin layer of AlGaAs, the composition of which is gradually changed to match that of the cap and wide band-gap emitter layers. The wide band-gap emitter layer is $Al_xGa_{1-x}As$ with x-value of about 0.3. The doping and thickness of this layer are chosen to minimize the emitter resistance and emitter-base capcitance while maximizing reverse breakdown voltage.

The base layer of HBTs is usually very heavily doped to minimize the base resistance and hence improve the device power gain. Typically, a base layer of $0.1\mu m$ and a doping concentration of $1 \times 10^{19}\text{cm}^{-3}$ are used for device designed for X-band (8-12 GHz) operation. Higher frequency operation requires somewhat thinner layers with doping concentrations up to $1 \times 10^{20}\text{cm}^{-3}$. The carrier transit time through the base can be improved by either reducing the thickness of the base layer or compositionally grading the base layer.



(a)



(b)

FIGURE 2.1 (a) Schematic cross-section view of a N-p-n HBT structure; (b) Band diagram with a wide-gap emitter.

The design of the collector layer critically influences the power potential of devices. The main consideration for this layer is the collector transit time delay and breakdown voltage requirements. A thicker layer will improve the breakdown voltage of the base-collector junction, but introduces a proportionally longer transit time delay. In most power devices, carriers move through the collector at their scatter-limited velocities because very large electrical fields are sustained in this layer. Larger velocities can be realized by so-called *ballistic collector transistor* (BCT) technology, in which the doping profile of the collector is modified to lower the electric field over a large portion of the collector such that electrons entering the collector layer can be maintained in the higher mobility lower valley during most of the collector-layer transit time. One way to achieve this modification is to use p^- collectors with a p^+ pulse-doped layer near the subcollector[23]. We did not examine this kind of structures.

Since the devices fabricated on semi-insulating (SI) substrates take best advantage of the GaAs technology and provide greater design flexibility in both device and circuit designs, most HBT-based ICs are now fabricated by using SI substrates.

To begin, let's first take a look at the energy band diagram of an N-p-n HBT biased in its forward active mode, as shown in Figure 2.1(b). The big N here denotes wider band-gap zone. This diagram is featured by a wide-gap emitter, and the smoothly changed band edges at the emitter-base interface are assuming that the emitter junction has been graded sufficiently to obliterate any band edge discontinuity in that region.

As shown in Figure 2.1(b), there are several current paths in the transistor. They are basically two injection-related dc currents and two recombination currents if we neglect the capacitive currents that accompany any voltage changes, the surface recombination current, and the hole-electron generation currents in the collector depletion layer or the collector body. The two injection-related currents are:

(a) Electron current I_n injected from the emitter into the base;

(b) Hole current I_p injected from the base into the emitter;

and the two recombination currents are:

(c) Recombination current I_s due to electron-hole recombination within the forward biased emitter-base space charge region.

(d) I_r, a small part of I_n, is lost in base due to bulk recombination.

The three terminal currents can be written out in terms of these current components:

Emitter current $I_e = I_n + I_p + I_s$

Collector current $I_c = I_n - I_r$

Base current $I_b = I_p + I_r + I_s$

The current gain for a bipolar transistor can therefore be expressed as:

$$\beta = \frac{I_c}{I_b} = \frac{I_n - I_r}{I_p + I_r + I_s} < \frac{I_n}{I_p} \equiv \beta_{max} \tag{2.1}$$

where β_{max} is the highest possible value of β in the case of neglecting recombination currents. Through the discussion of β_{max} one can see how a heterojunction transistor works.

To estimate β_{max}, a prototype diffusion model is used here as in ref.[24], in which emitter and base are assumed uniformly doped to levels N_e and P_b, and the height of the potential energy barriers for electrons and holes at the emitter-base interface are denoted with qV_n and qV_p, as shown in Figure 2.1(b). One may then write the electron and hole injection current densities as follows:

$$J_n = N_e v_{nb} exp(-qV_n/kT) \tag{2.2}$$

$$J_p = P_b v_{pe} exp(-qV_p/kT) \tag{2.3}$$

where v_{nb} and v_{pe} are the mean drift velocities of electrons at the emitter-end of the base, and of holes at the base-end of the emitter, respectively.

In writing (2.2) and (2.3), it has been implicitly assumed that both the emitter and base as nondegenerate. Therefore simple Boltzman factors apply. This assumption might not be true for the base layer in a HBT. It may need small corrections in that case but, for simplicity, we neglect them here.

We are only interested in the ratio of the two currents. In the case of a wide-gap emitter, the gap difference between emitter and base is given by:

$$\Delta E_g = q(V_p - V_n) \tag{2.4}$$

We thus obtain:

$$\beta_{max} = \frac{I_n}{I_p} = \frac{N_e}{P_b}\frac{v_{nb}}{v_{pe}} exp(\Delta E_g/kT) \tag{2.5}$$

For a good transistor, normally $\beta_{max} \geq 100$. Since the ratio v_{nb}/v_{pe} is fixed at a range from 5 to 50, to achieve $\beta_{max} \geq 100$, there are two options available that either to make $N_e \gg P_b$ or ΔE_g is at least a few kTs.

In a homojunction device, high current gain is attained typically by constructing a very high doping density emitter such that $N_e \gg P_b$, but this limits the ultimate thickness of the base due to eventual punch-through effects. Thicker base entails longer base transit time, and lower base doping causes higher base resistance. These two factors severely inhibit the switching speed. Even worse, highly doped emitter (typically beginning at a doping level $N_d \sim 10^{17}$ cm^{-3}) brings about an emitter-gap shrinkage, which produces a negative effect on raising current gain, according to (2.5), reducing the ratio I_n/I_p by a factor $e^{-3} \sim 1/20$ at doping level $N_d \sim 10^{19}$ cm^{-3}. As a result, it is as if the emitter were

doped only to 5×10^{17} cm^{-3} without gap shrinkage[25].

In heterostructure transistors, however, these drawbacks are completely eliminated because it makes possible now to take advantages of the exponential term presented in (2.5), which is much more sensitive in affecting current gain than the doping ratio. By selecting an appropriate material, an energy gap difference that is many times kT can be readily obtained such that very high injection efficiency can be achieved almost regardless of the doping issue. This major change enables us to turn around the hole injection current I_p to an immaterial position compared to the two recombination currents: I_s and I_r. Furthermore, notice that $I_r \ll I_n$, and $I_s \ll I_r$ are basically true in a properly designed heterostructure transistor, we have now:

$$\beta = \frac{I_n}{I_r} \tag{2.6}$$

The bulk recombination current density can be written as

$$J_r = \frac{qn_e(0)\, W_B}{2\tau_n} \tag{2.7}$$

if a short base is assumed. Here $n_e(0)$ is the injected electron concentration at the emitter end of the base, W_B is the base width, and τ_n is the average electron lifetime in the base. Upon the substitution of (2.2) and (2.7) in (2.6), we obtain

$$\beta \approx \frac{v_{nb}\tau_n}{2W_B} \tag{2.8}$$

In the above expression, lifetime τ_n is the only factor that refers β to the base doping through its doping level dependence.

Although the electron lifetime may be very short in the case of heavy base doping, high β is still achievable with a sufficiently thin base region. As an example, assume $W_B \approx 1000A$, and $v_{nb} \approx 10^7 cm \cdot s^{-1}$, which are reachable under a very strong electron

field, due to the effect of high electron concentration gradient. In this case, even for a lifetime as short as $10^{-9}s$, this would lead to $\beta \approx 10^3$, a value beyond the capability of a conventional silicon bipolar transistor.

Although high β-values may be preferred in photo-transistors, however, in general they are not the most favored issues for other applications. Therefore, the principal benefit of heterostructures lies by no means in high current gain ability rather than the trade-offs in achieving very high base doping. In fact, almost all the advantages that a wide-gap emitter HBT can offer somehow benefit from the high base doping, as can be seen clearer in the following sections.

2.2.0 Figures of Merit

2.2.1 Microwave Transistors

As mentioned earlier, HBT has its successful application as a microwave transistor. Ladd and Faucht [3] have given a detail analysis of microwave transistor behavior by using the maximum oscillation frequency f_{max} as the figure of merit, which can be approximately written in the form:

$$f_{max} = \sqrt{\frac{f_t}{8\pi r_b C_c}} \tag{2.9}$$

where r_b is the effective base resistance, C_c is the effective collector-base capacitance, and f_t is the frequency at which the common emitter current gain becomes unity, which can be expressed further as

$$f_t = [2\pi\tau_{ec}(1+\nu)]^{-1} \tag{2.10}$$

where ν is the excess phase factor associated with the graded base doping. The delay time

τ_{ec} can be written as:

$$\tau_{ec} = \tau_b + \tau_e + \tau_{dc} + \tau_c \tag{2.11}$$

where

τ_b = base transit time,

$\tau_e = r_e C_{je}$ time constant for charging emitter capacitance,

τ_{dc} = the effective collector-base depletion layer transit time,

and

τ_c = the RC time constant for charging the collector capacitance.

f_{max} is the most appropriate figure of merit for broad-band applications, which is defined as the frequency at which the unilateral power gain of the transistor becomes unity. Therefore it is also called the unity power gain. The unilateral power gain is the maximum available power gain of the transistor when the reverse gain is zero, and is independent of the terminal configuration.

In the expression (2.10), the most sensitive factors affecting f_{max} are the total emitter-to-collector delay time and the base-resistance-collector-capacitance time constant $r_b C_c$. We'll discuss them one after one by following the ref.[3], [24] and [26].

Base Transit Time

The base transit time τ_b is defined as Q_B/I_C according to the charge control concept. For a uniform base doping, and considering a background constant electron concentration (for n-p-n transistor) existing in the neutral base caused by the velocity saturated carrier concentration extended from the collector depletion region (x_{dc}) to the

base region, the base transit time can be written as:

$$\tau_b = \frac{W_B^2}{2D_n} + \frac{W_B}{v_{sat}} \tag{2.12}$$

where W_B is the base width, D_n is the diffusion constant of minority carriers in the base, and v_{sat} is the saturation velocity in the base-collector depletion region.

In the case of HBTs, base doping is increased to a very high level in order to keep a lower base resistance. Meanwhile, a sufficient thin base is achieved for a shorter base transit time, both of them benefiting a larger f_{max}. Since D_n decreases as the base doping increases, however, it turns out that τ_b will increase as r_b is lowered by raising the doping density of base if W_B is kept constant. In fact, r_b is much more important than τ_b in determining f_{max} because in general τ_b is only about 10 to 15 percent of τ_{ec}. This leads to a consideration that there exists an optimum value of base doping level P_b at a particular value of W_B for an optimum f_{max}. Since increasing P_b causes only a slight increase in τ_{ec}, the optimum base doping level of a heterojunction transistor will be virtually limited by solid solubility consideration without introducing secondary effects.The value of τ_b thus obtained will be larger than the shortest τ_b which could be obtained by arbitrarily reducing W_B and increasing D_n to the device limit.

Collector Time Constant

The time constant τ_c is given by

$$\tau_c = r_c C_i \tag{2.13}$$

where r_c is the ohmic resistance of the epi-substrate, and C_i is the inner collector transition region capacitance. In calculating r_c and C_i, the area is that of the emitter stripes, i.e., the active area of the device. C_i is different from C_c in that the latter is comprised of the

parasitic capacitance of the collector junction associated with the remaining device area.

The collector depletion region transit time is given by

$$\tau_{dc} = \frac{x_{dc}}{2v_{sat}} \tag{2.14}$$

where x_{dc} is the width of collector depletion region and v_{sat} is the saturation velocity in the collector. The factor 2 accounts for the effect of the drift limited flow of carriers across the depletion region[3, 26, 27].

Emitter Time Constant

The emitter time delay τ_e is defined by

$$\tau_e = r_e C_{je} \tag{2.15}$$

where the differential emitter resistance r_e is kT/qI_e, C_{je} is the emitter-base junction capacitance, and the series resistance of the emitter bulk is neglected. An intuitive inference which can be drawn from the above equation is that this time constant may be largely reduced by operating the transistor under a higher current density condition.

The calculation of C_{je} may use the formula for an abrupt junction with one side heavily doped. Since the emitter doping is now dropped far below the base doping, the emitter capacitance of the transistor then depends principally on the emitter doping, roughly as:

$$C_e \propto N_e^{1/2} \tag{2.16}$$

Evidently the lower emitter doping, the larger reduction in emitter capacitance can be obtained. This reduction will improve the speed, but it is not the key step because this time delay is only one of several delays. The true significance of the reduction of the

capacitance per unit area lies in two different facts. First, it permits an increase in capacitive emitter area in the inverted transistor design, which has important applications in integrated-injection logic (I^2L), without increase in total emitter capacitance. Second, in the case of HBTs, for small-signal microwave amplifications, a reduction in emitter capacitance will improve the noise figure significantly.

$r_b C_c$ Time Constant

Inspection of the f_{max} expression (2.9) shows that this time constant has a large effect. The most important single change made possible by a wide-gap emitter is a major reduction in base resistance due to a drastic increase in base doping, but this is only a part of the base resistance underneath the emitter area. The external base resistance (between the emitter edge and the base contact) had been a problem for a long time, due to the thin outer base caused by the emitter island design that popularly used in current HBT technology. In today's HBT technology, the total base resistance reduction has been made possible by the development of various self-aligned processing technologies[28-30], which largely shortens the lateral separation between the base and the emitter metallization. Further improvements in this aspect are expected as the HBT technology matures.

The parasitic capacitance between the extrinsic base metallization region and the underlying collector was another drawback of the planar technology for HBTs. As the vertical dimension of the device is reduced to achieve shorter transit time, the collector-to-base feedback capacitance increases rapidly, and this limits the power gain of the device. Use of buried oxygen implantation between outer base and collector[31] significantly reduces the feedback capacitance (see Figure 2.1(a)), and the figure of merit f_{max} improves accordingly.

Calculation of the $r_b C_c$ product is relatively straightforward if the base contact

resistance does not have to be taken into account. For uniform current density over the emitter stripe area, the r_b formula is given by

$$r_b = \frac{\rho_s S_{EB}}{12 l_E} \tag{2.17}$$

where ρ_s is the sheet resistance of the p^+ base layer under the emitter, S_{EB} is the gap region between the emitter and the base metallization, and l_E is the emitter stripe length. The collector capacitance is simply

$$C_c = \frac{\varepsilon A_e}{x_{dc}} \tag{2.18}$$

when the wafer parasitics are neglected.

As considering the effect of distributed outer base resistance and base-collector capacitance between the emitter and base metallization, the calculation of $r_b C_c$ is somewhat involved. We'll leave this in Chapter III for further discussions.

2.2.2 Digital Switching Transistors

While f_{max} is an appropriate figure of merit of speed limitation for small-signal microwave applications, it is not directly usable to define switching speed limitations of a digital device. The switching speed of a circuit is related to the active device parameters, mode of operation, values of the passive elements, and dependent on the circuit itself. No standard measure for switching time had been agreed upon until the conception of delay figure was defined by K. G. Ashar[32] in his effort to find a simple method of estimating delay in a switching network, which is still most popularly used as the figure of merit of a switching transistor. According to Ashar, the delay D of a linear network is the average time by which the response of the delta function input is delayed, which can be finally

expressed in the form

$$D = \left[\frac{-\frac{d}{ds}F(s)}{F(s)} \right] \Bigg|_{s=0} \tag{2.19}$$

where $F(s)$ is the transfer function of the network. For a switching circuit with a few time constants, the time average D appropriately gives switching delay plus 50 percent of the rise time, which is basically equivalent to the conception of a propagation delay time used in today's industry. The success of Ashar's method lies in its capability to characterize the switching speed of a relatively complicated network in a simple way without the necessity of solving the complete network equations, and of course, in the price of sacrificing some accuracy due to approximations. Based on Ashar's analysis of a two-transistor circuit, Dumke modified the results to be suitable for the case of HBTs. Dumke's modification simply consists of the assumption that the load resistance must be large enough to develop a potential change equal to the required emitter swing ΔV on the next stage[24]. Therefore we have $R_L = \Delta V/I = R_E$, where I is the current that is switched to. Making the appropriate substitutions in Ashar's expression yields the estimation of the switching time of a HBT as[33]

$$\tau_s = \frac{5}{2} r_b C_c + \frac{r_b}{R_L} \tau_b + (3C_c + C_L) R_L \tag{2.20}$$

where r_b is the base resistance, C_c is the collector capacitance, τ_b the base transit time, R_L and C_L are load resistance and capacitance of the circuit, respectively. The importance of the Ashar-Dumke result is that it indicates the relative significance of the most important transistor parameters. For example, from the above equation one can see r_b is even more effective in a digital switching transistor than in a microwave transistor, since two of the three terms in (2.20) depend linearly on r_b rather than with the square root as does f_{max}.

2.3.0 Graded and Abrupt Emitter Junctions

In Figure 2.1(b), we have seen that the band edges at emitter-base interface vary smoothly and monotonically based on the assumption that the emitter-base junction is completely graded. It will not be the case, however, if no appropriate measure has been taken. Instead, the current epitaxial technology tends to produce abrupt junction at emitter-base interface in which band edge discontinuities are present due to the different affinities in emitter and base regions. In the case of a wide-gap emitter, this leads to the "spike-and-notch" energy band structure shown in Figure 2.2. The potential spike projects above the conductance band in the neutral base region, forming a potential barrier of net height ΔE_B. This barrier is often considered as an undesirable feature that leads to the accompanying increase of the order ΔE_q in required emitter-base forward bias voltage to yield a given current density. The more severe drawback, on the other hand, is that the ratio J_n/J_p is drastically reduced due to the presence of the potential barrier ΔE_B, from the value in (2.5), by a factor of $exp(-\Delta E_B/kT)$. Instead of (2.5), we now have[24, 34]

$$q(V_p - V_n) = \Delta E_g - \Delta E_B \approx \Delta E_V \tag{2.21}$$

The last equality is appropriately equal if one assume the notch depth is small compared to kT, in which case $\Delta E_B = \Delta E_C$. Here ΔE_C and ΔE_V represent the conduction and valence band discontinuities. This assumption is true because the notch is quite shallow due to the low emitter-to-base doping ratio expected in HBTs. Therefore, we obtain

$$\frac{I_n}{I_p} = \beta_{max} = \frac{N_e}{P_b}\frac{v_{nb}}{v_{pe}} exp(\Delta E_V/kT) \tag{2.22}$$

If the valence band discontinuity is sufficiently large, a major improvement remains. Unfortunately, in the AlGaAs/GaAs system which is of current interest, the valence band discontinuity is quite small, $\Delta E_V = 0.15\Delta E_g$ [35], and the reduction of the spike by grading is thus essential.

One compensation for the disadvantages of the spike is its ballistic effect, which acts as if the electrons are injected into the base from a "ballistic launching ramp". This will result in a highly efficient and very high speed transport through the base because the polar optical photon-scattering, the dominant scattering process in III-V compounds, would not be able to stop it effectively.

As for the notch, it is a highly undesirable effect because a notch will collect injected electrons and therefore enhance recombination loses. Hence it would be desirable to eliminate it altogether.

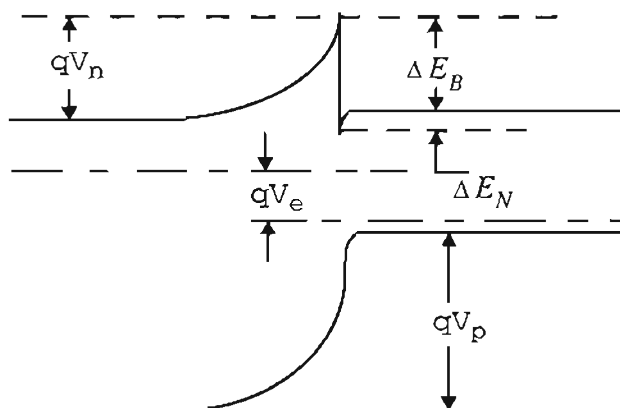


FIGURE 2.2 Band structure of an abrupt wide-gap emitter, showing the spike barrier and the accompanying electron trapping notch.

2.4.0 Carrier Transport in HBT Structure

For a graded emitter-base junction HBT, the carrier transport mechanism is essentially similar to a BJT. In the case of N-p-n structure, electrons are injected across the

emitter-base junction from emitter area to base region if the junction is forward-biased. The injected electrons will travel through the p^+ base region by drift and diffusion process, and then sweep rapidly through the base-collector space charge region and into the n-type collector region. Since the latter process is very fast under the action of a high electric field across the reverse-biased base-collector junction, electrons are stored in the base region in the transport process due to their finite effective velocity.

There are mainly three kinds of recombination process, which are space charge region (SCR) recombination, neutral base recombination, and surface recombination. B. R. Rynum and I. M. Abdel-Motaleb[15] have taken the effect of interface recombination into consideration, which used to be neglected by most of the published models. Also in the same paper, they claimed that surface recombination has a more significant contribution than SCR recombination, specially for smaller emitter structure, and this effect is thus called the "emitter-size" effect. The interface recombination current in the vicinity of the graded composition region was found to dominate other components. This explanation supports the claim that the rapid decrease of current gain occurs at the lower collector current end.

Although a detailed drift-and-diffusion theory of the minority-carrier transport in HBTs has been presented by A. Marty et al.[11] in 1979, it essentially applies only to the graded HBT case. A number of papers[13-17] have pointed out that the correct mechanism of transport across an abrupt heterointerface is thermionic emission. Based on this assumption, a new boundary condition for pn heterojunctions was obtained by balancing the thermionic emission flux of carriers by the diffusion flux at the edge of the SCR[13], and the models of Ebers-Moll and Gummel-Poon types were developed subsequently[14-15] in an effort to improve the theory applicable to either the case of abrupt HBTs, or to the limit, the case of graded ones.

In conclusion, HBT is featured with a wide-gap emitter, which provides one with the freedom of raising the base doping level to achieve a low spreading base resistance and a thin base layer thickness simultaneously. Comparing with its homojunction competitors, HBT finds its most widespread applications in microwave and millimeter-wave frequency range. Also, it has obvious advantages over GaAs FETs and HEMTs in many aspects. As a good figure of merit, maximum oscillation frequency f_{max} is used to characterize the microwave behavior of HBTs while propagation time delay concept was defined for the digital switching transistors. For AlGaAs/GaAs system HBTs, it was found that a graded emitter junction is essential for the reduction of the spike caused by the conduction band edge discontinuities.

CHAPTER III

DEVICE MODEL

3.1.0 Low-Frequency T-Model and Hybrid- π Model

The most useful equivalent network models for small-signal bipolar transistor amplifier are T-model and hybrid-π model. One may tend to use one of them in certain cases for convenience but essentially they are equivalent. The small-signal T-model, which was initially developed for modeling common-base configuration network, can be obtained from the large-signal Ebers-Moll (EM) model, as explained by Bar-Lev[36]. In the active region, and at low frequencies the large-signal EM model will degenerate to the form of Fig. 3.1(a), where the small internal capacitances and base spreading resistance $r_{b'b}$ are neglected.

In the case of small signals, the low frequency common-base (CB) model further changes into the form of Fig. 3.1(b), in which the forward-biased emitter-base diode D_E is replaced by its differential resistance r_e, which can be represented by:

$$\frac{1}{r_e} = \left.\frac{dI_E}{dV_{EB}}\right|_{V_{CB}} = \frac{1}{\alpha}\frac{dI_C}{dV_{EB}} = \frac{qI_C}{\alpha kT} = \frac{qI_E}{kT} \tag{3.1}$$

The $\alpha_F I_E$ current source can be replaced by its small-signal equivalent αi_e, where i_e is the a.c. component of I_E and α is defined as:

$$\alpha = \left.\frac{dI_C}{dI_E}\right|_{V_{CB}} \tag{3.2}$$

The resistance r_c represents the slope of the $I_C - V_{CB}$ characteristics and is defined by

$$\frac{1}{r_c} \equiv \left.\frac{dI_C}{dV_{CB}}\right|_{I_E} \tag{3.3}$$

It can be seen here that r_c contains the effects of base-width modulation. An additional effect due to the V_{CB} change is that there must be a change in V_{EB} if I_E keeps constant. But this is exactly the definition of h_{12b}:

$$h_{12b} = \left.\frac{v_1}{v_2}\right|_{i_1 = 0} = \left.\frac{dV_{EB}}{dV_{CB}}\right|_{I_E} \tag{3.4}$$

where h_{12b} represents the reverse voltage transfer ratio in CB connection. To add h_{12b} to the model of Fig. 3.1(b), it is necessary to include a controlled voltage source $h_{12b}\Delta V_{CB} = h_{12b}v_2$ in the input circuit.

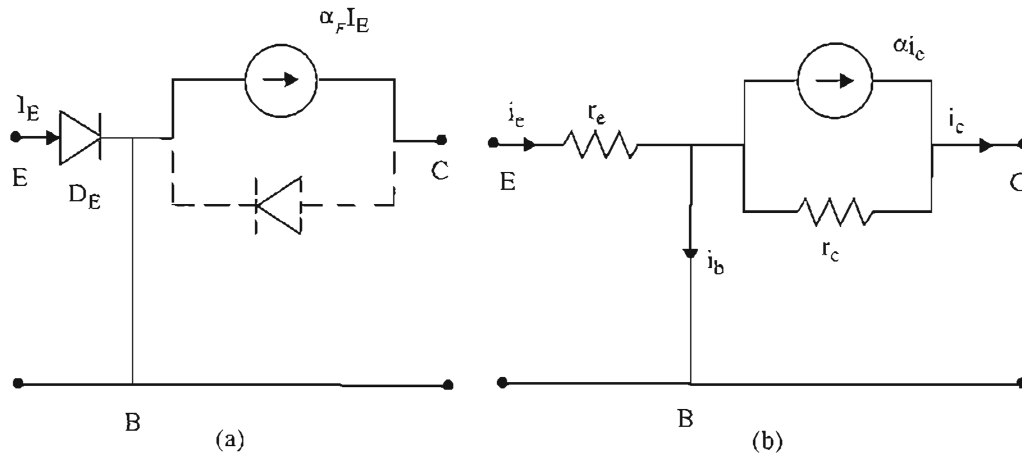


FIGURE 3.1 (a) Active mode large-signal EM model; (b) Small-signal representation of (a)

A complete T-model equivalent circuit for CB configuration is drawn in Fig. 3.2, which is adaptable to a wide range of frequencies. In Fig. 3.2, C_d is diffusion capacitance, appearing only in the emitter junction, which is forward biased, while the depletion-layer capacitance C_c appears in the collector. C_{je} is also kind of depletion capacitance, but is only a week function of I_E here. In a transistor with uniformly doped base, C_{je} is much smaller than C_d while in a transistor with a drift field in the base, C_d may reduce to the order of C_{je} or lower.

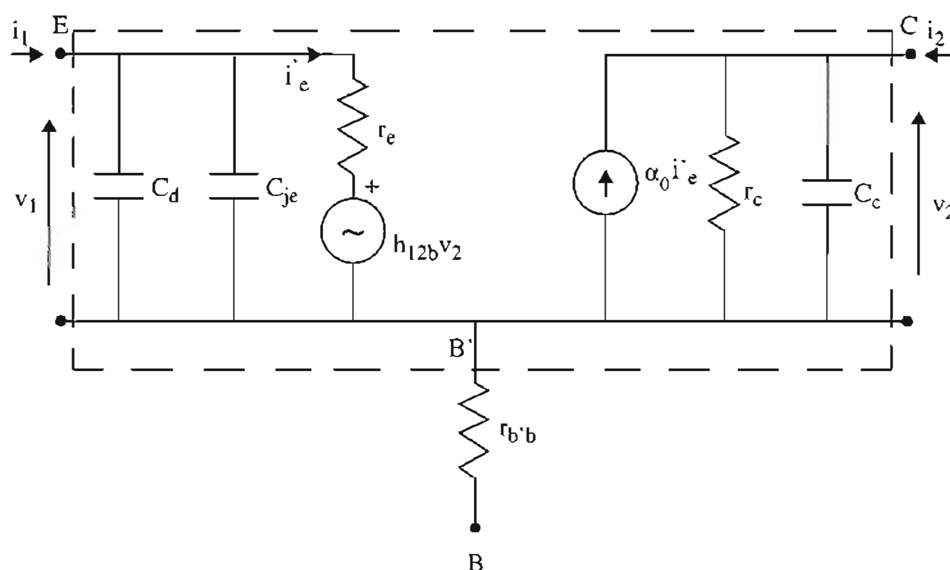


FIGURE 3.2 The complete CB model

The y parameters of the two-port network enclosed by the dashed box in Fig.3.2 can be written easily by using their definitions:

$$y_{11b} = \left.\frac{i_1}{v_1}\right|_{v_2} = \frac{1}{r_e} + j\omega\left(C_{je} + C_d\right) \tag{3.5}$$

$$y_{12b} = \left.\frac{i_1}{v_2}\right|_{v_1 = 0} = -\frac{h_{12b}}{r_e} \tag{3.6}$$

$$y_{21b} = \left.\frac{i_2}{v_1}\right|_{v_2 = 0} = -\frac{\alpha_0}{r_e} \tag{3.7}$$

$$y_{22b} = \left.\frac{i_2}{v_2}\right|_{v_1 = 0} = \frac{1}{r_c} + \frac{\alpha_0 h_{12b}}{r_e} + j\omega C_c \tag{3.8}$$

It should be noticed that the current source αi_e in Fig. 3.1(b) is replaced by $\alpha_0 i_e'$ in Fig. 3.2, which means the current source is controlled only by the part of i_e that flows through r_e. If we continue using the total emitter current i_e (which is more convenient), we can define an effective α as follows:

$$\alpha_0 i_e' = \frac{\alpha_0 i_e}{1 + j\omega r_e (C_{je} + C_d)} \equiv \alpha i_e \tag{3.9}$$

we can also define an ω_a as:

$$\omega_a \equiv \frac{1}{r_e (C_{je} + C_d)} \tag{3.10}$$

where ω_a is called the *half-power frequency* because the power amplification is reduced to half the low-frequency value when $\omega = \omega_a$. The effective α is then given by

$$\alpha \equiv \frac{\alpha_0}{1 + j\omega / \omega_a} \tag{3.11}$$

This model represents the bipolar transistor very well so long as the base transition time τ_b is much shorter than the period T of the amplified signal. At higher frequencies an appreciable phase shift $\omega\tau_b$ may appear between the electron current at its point of injection into the base, and at the point where it leaves the base. The ratio of the electron currents at those two points is the base transport factor b which now becomes a complex function of the frequency. This function has an infinite number of poles along the negative real axis. The first and most significant one is at $\omega = \omega_a$. The expression (3.11) is there-

fore just a single-pole approximation to the correct form of α. The neglected, far poles have little effect on the magnitude of α but add a significant phase shift to it. A better approximation, therefore, for the effective α includes an additional phase shift factor:

$$\alpha = \frac{\alpha_0 exp\,(-jm\omega / \omega_a)}{1 + j\omega / \omega_a} \tag{3.12}$$

where $m \approx 0.2$ for a uniform base junction transistor, but is much larger and may be as high as 1 for the transistor with high impurity gradients in their bases. Further discussion about common-base current gain α is left to the section 3.3, where the high frequency model case is discussed.

The models of Fig. 3.1(b) or Fig. 3.2 can be used for any transistor configuration. They can represent a common-emitter (CE) connection just by drawn sidewise. But using them this way is inconvenient since the internal source should be controlled by the input, which is i_b now rather than i_e.

A more convenient model for CE configuration, which is known as the hybrid-π model of the bipolar transistor, can be derived from the previous CB T-model, by simply transforming the y_b to y_e parameters of the CE connection as follows:

$$y_{11e} = \Sigma y_b = \frac{(1-\alpha_0)\,(1-h_{12b})}{r_e} + \frac{1}{r_c} + j\omega\,(C_{je} + C_c + C_d) \tag{3.13}$$

$$y_{12e} = -y_{12b} - y_{22b} = \frac{1-\alpha_0}{r_e} h_{12b} - \frac{1}{r_c} - j\omega C_c \tag{3.14}$$

$$y_{21e} = -y_{21b} - y_{22b} = \frac{\alpha_0\,(1-h_{12b})}{r_e} - \frac{1}{r_c} - j\omega C_c \tag{3.15}$$

$$y_{22e} = y_{22b} = \frac{1}{r_c} + \frac{\alpha_0 h_{12b}}{r_e} + j\omega C_c \tag{3.16}$$

Fig. 3.3 shows the complete hybrid-π model, in which the values of the various components can be represented as follows

$$r_\pi = \frac{r_e}{1-\alpha_0} \tag{3.17}$$

$$C_\pi = C_{je} + C_d \tag{3.18}$$

$$r_\mu = r_c \tag{3.19}$$

$$C_\mu = C_c \tag{3.20}$$

$$g_m v_{be'} = \frac{\alpha_0}{r_e} \tag{3.21}$$

$$g_0 = \frac{h_{12b}}{r_e} \tag{3.22}$$

It can be easily verified that these values satisfy a general two-port network representation described by its y parameters[36].

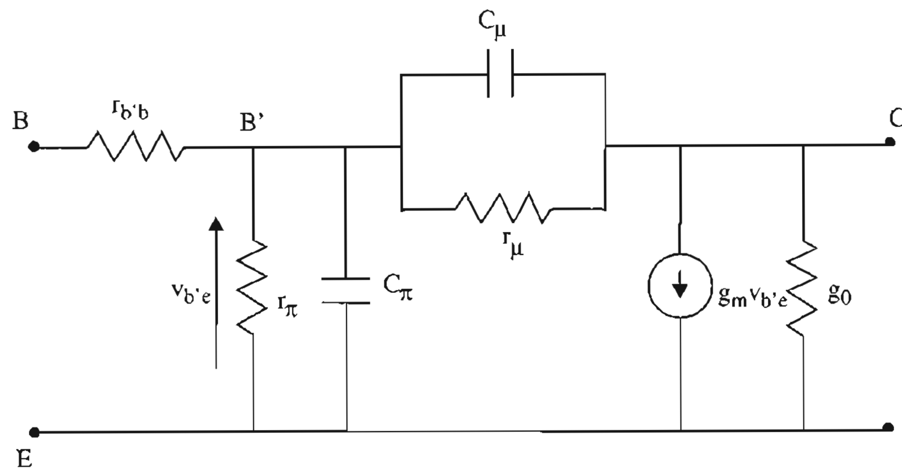


FIGURE 3.3 The hybrid-π model

The big advantages of CE model is that all its constituents are simple resistors or capacitors whose frequency behaviors are known. It can represent the transistor in a wide

range of frequencies. The very high frequency case will be discussed further later.

On the other hand, the low-frequency small-signal hybrid-π model can also be obtained directly from EM model[37]. The elements are given by

$$r_\pi = \frac{\beta_F}{g_{mF}} \tag{3.23}$$

$$r_\mu = \frac{\beta_R}{g_{mR}} \tag{3.24}$$

$$C_\pi = g_{mF}\tau_F + C_{je}(V_{B'E'}) \tag{3.25}$$

$$C_\mu = g_{mR}\tau_R + C_{jc}(V_{B'C'}) \tag{3.26}$$

where β_F and β_R are the large-signal forward and reverse current gains of a CE transistor, respectively, g_{mF} is the forward transconductance, and g_{mR} is the reverse transconductance. τ_F is the total forward transit time, and τ_R is for the reverse case. C_{je} and C_{jc} denote two junction capacitors for the base-emitter junction and the base-collector junction, respectively. In the normal region of operation, g_{mR} is essentially zero, so that resistance r_μ can be regarded as infinite and capacitance $C_\mu \approx C_{jc}(V_{B'C'})$.

3.2.0 Charge-Control Model

The charge-control concept is a simple and useful one that relates the base stored charge to the terminal currents. The concept was introduced by Sparks and Beaufoy[38, 39] in the analysis of the relationship between the currents flowing through the neutral base and the excess minority carrier charge stored in this region. It was found that the ratio Q_B/I_C is a fundamental parameter of a transistor, and since it has a dimension of time constant, it was defined as the neutral base region carrier transit time τ_b.

$$\tau_b = \frac{Q_B}{I_C} = \frac{W_B^2}{2D_n} \tag{3.27}$$

where W_B is the effective base width, and D_n is the electron diffusion constant in the base. In the case of considering the effect of finite saturated velocity v_{sat} caused by the high-field in the base-collector space charge region, which is usually true for HBTs, the base transit time can be corrected as

$$\tau_b = \frac{W_B^2}{2D_n} + \frac{W_B}{v_{sat}} \tag{3.28}$$

The recombination base current can be obtained by defining another time constant τ_n, such that

$$I_B = \frac{Q_B}{\tau_n} \tag{3.29}$$

where τ_n represents the average electron lifetime in the base due to the effect of base recombination. Since $\beta_F = I_C / I_B$, we have

$$\beta_F = \frac{\tau_n}{\tau_b} \tag{3.30}$$

(3.30) tells us that to obtain a high value of β_F, a transistor must be designed to achieve a large ratio of minority carrier lifetime to base transit time.

Charge control model is a more fundamental description of the transistor than it being represented as a current control source. Assume an "ideal" transistor without minority carrier recombination either in the base or the emitter and in which the extrinsic base resistance is zero. One could "turn on" this transistor by discharging a capacitor, then an amount of lossless Q_B could inject into the base region and a steady emitter-collector current would then flow until the base charge was removed. Such an ideal transistor would draw no base current, and base current control of the collector current would not be possible. It is only as a result of "imperfections" in the transistor that current control becomes a

practical possibility. Therefore (3.29) indicates that it becomes necessary to supply a steady current to the base region in order to maintain the level of Q_B.

In a transient case, I_B not only provides the recombination current and the back injection current but also reflects the change rate of the minority carriers Q_B stored in the neutral base region, which evidently is different from its normal value of (3.29). The behavior can be expressed as follows

$$i_B(t) = \frac{Q_B(t)}{\tau_n} + \frac{dQ_B}{dt} \tag{3.31}$$

A corresponding expression for the collector current is

$$i_C(t) = \frac{Q_B(t)}{\tau_b} \tag{3.32}$$

From (3.31) and (3.32), the rise time t_r, required for the collector current in a simple CE amplifier, starting from zero to reach, say 90 per cent of its final value I_C, can be estimated as follows[40]

$$t_r = \tau_n In \frac{\beta_F I_B - 0.1 I_C}{\beta_F I_B - 0.9 I_C} \approx 2.2\tau_n \tag{3.33}$$

By combining (3.31) and (3.32), we have

$$\begin{aligned} i_E &= i_C(t) + i_B(t) \\ &= \frac{Q_B(t)}{\tau_b} + \frac{Q_B(t)}{\tau_n} + \frac{dQ_B}{dt} \end{aligned} \tag{3.34}$$

Fig. 3.4 (a) shows the equivalent circuit that represents the simple charge-control model. Note Q_B is a nonlinear function of V_{BE}, and the excess minority carrier base charge is represented as stored on a nonlinear capacitor.

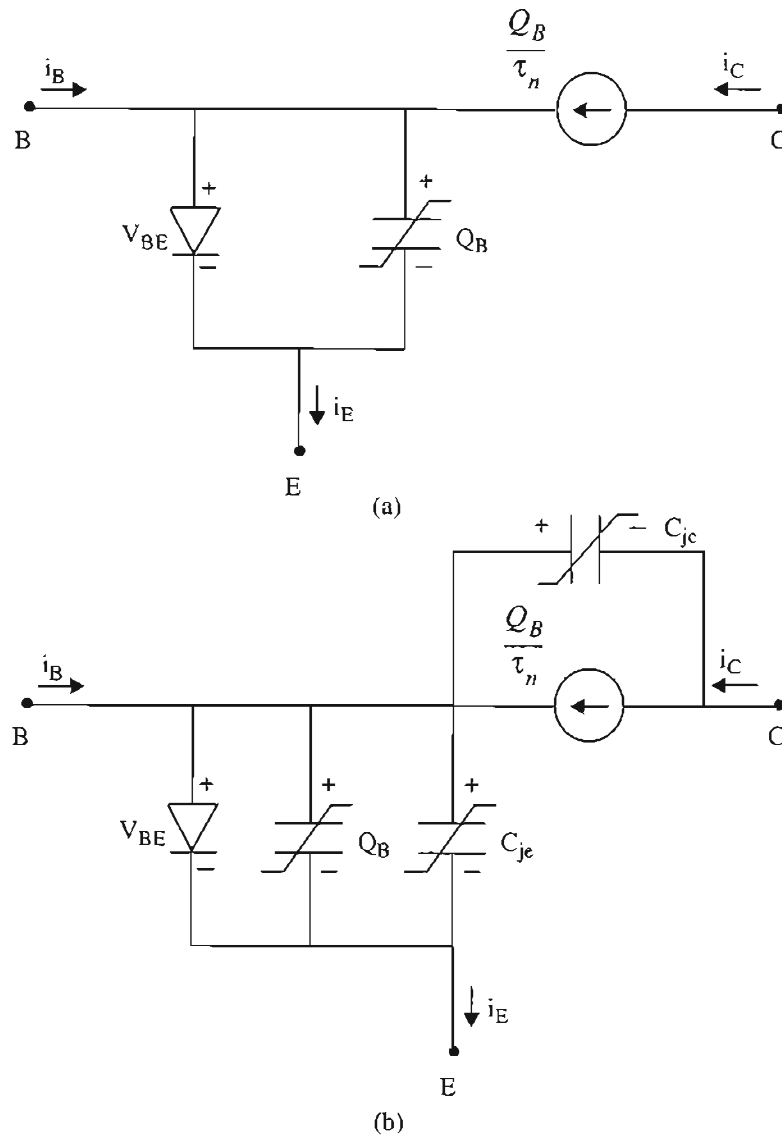


FIGURE 3.4 (a) Simple charge-control model; (b) Charge-control model in forward active mode

Taking account of the junction capacitance charging effects and ignoring the injection from the collector, the charge-control equations in forward active mode can be expressed as follows:

$$i_E = -\frac{dQ_B}{dt} - \frac{Q_B}{\tau_e} - -\overline{C_{je}}\frac{dV_{BE}}{dt} \qquad (3.35)$$

$$i_C = \frac{Q_B}{\tau_b} - \overline{C_{jc}}\frac{dV_{BC}}{dt} \qquad (3.36)$$

$$i_B = \frac{Q_B}{\tau_n} + \frac{dQ_B}{dt} + \overline{C_{je}}\frac{dV_{BE}}{dt} + \overline{C_{jc}}\frac{dV_{BC}}{dt} \qquad (3.37)$$

where V_{BE} and V_{BC} represent the emitter -base and base-collector time-dependent voltages, τ_n is the effective base recombination time, τ_b is the base carrier transit time and

$$\tau_e = \left(\frac{1}{\tau_n} + \frac{1}{\tau_b}\right)^{-1} \qquad (3.38)$$

Because the junction capacitances are voltage dependant, their averages (indicated by $\overline{C_{je}}$ and $\overline{C_{jc}}$) are used. The Eqns. (3.35) — (3.37) are modeled in Fig. 3.4 (b)

So far we have discussed several different models. Ebers-Moll model and charge-control model are valid for all ranges of bias. The latter is specially useful for transient analysis of transistors. T-model and hybrid-π model are small-signal models for use only in the region of active bias. Since these models have regions of overlapping validity, a series of relationships between their parameters can be expressed. For example, the EM parameters α_F is related to the charge-control parameter τ_b and τ_n by

$$\alpha_F = \frac{\tau_n}{\tau_n + \tau_b} \qquad (3.39)$$

A similar relationship can also be found between reverse-active-mode parameters.

3.3.0 High-Frequency Transistor model

To consider the high-frequency behavior of HBTs, one has to deal with the base region continuity equation[41]. Assuming that a small-signal sinusoidal voltage excitation v_{eb} is applied between the emitter and base, we have

$$V(t) = V_{EB} + v_{eb} exp(j\omega t) \tag{3.40}$$

For n-p-n transistor, the continuity equation is written as follows:

$$\frac{\partial n}{\partial t} = -\frac{n - n_0}{\tau_n} + D_n \frac{\partial^2 n}{\partial x^2} \tag{3.41}$$

In this equation, the built-in electric field in the base region has been neglected. To solve (3.41), we substitute for $n(x)$

$$n(x) = n_{dc}(x) + n_{ac} exp(j\omega t) \tag{3.42}$$

in which $n_{dc}(x)$ satisfies the dc diffusion equation

$$D_n \frac{\partial^2 n_{dc}}{\partial x^2} - \frac{n_{dc} - n_0}{\tau_n} = 0 \tag{3.43}$$

Substituting (3.42) into (3.41), and collecting the ac terms yields

$$\frac{\partial^2 n_{ac}}{\partial x^2} = \frac{n_{ac}}{(L_n')^2} \tag{3.44}$$

where

$$L_n' = \frac{L_n}{(1 + j\omega\tau_n)^{1/2}} \tag{3.45}$$

and

$$L_n = \sqrt{D_n \tau_n} \tag{3.46}$$

Considering the saturated velocity effect, the appropriate small-signal boundary

conditions can be written as

$$n_{ac}\big|_{x=0} = n_{dc}(0)\frac{qv_{eb}}{kT} \tag{3.47}$$

$$n_{ac}\big|_{x=W_B} = n_c\frac{qv_{eb}}{kT} \tag{3.48}$$

where $n_{dc}(0) = n_{po}exp(qV_{EB}/kT)$, n_{p0} is the base electron density at emitter side in the equilibrium, and

$$n_c = \frac{J_c}{qv_{sat}} \tag{3.49}$$

n_c is the velocity saturated carrier concentration in the collector depletion region. n_{ac} can be obtained by solving (3.44).

$$\begin{aligned} n_{ac}(x) = \frac{qv_{eb}}{kT}\{&\left[n_{dc}(0) - \frac{n_{dc}(0)e^{W_B/L_n'} - n_c}{2\sinh(W_B/L_n')}\right]e^{x/L_n'} \\ &+ \frac{n_{dc}(0)e^{W_B/L_n'} - n_c}{2\sinh(W_B/L_n')}e^{-x/L_n'}\} \end{aligned} \tag{3.50}$$

The emitter and the collector small-signal currents can be expressed in the following manner:

$$\begin{aligned} i_e &= qD_nA_e\frac{d}{dx}n_{ac}(x)\Big|_{x=0} \\ &= -\frac{qD_nA_e}{L_n'}\left(\frac{qv_{eb}}{kT}\right)\frac{n_{dc}(0)\cosh(W_B/L_n') - n_c}{\sinh(W_B/L_n')} \end{aligned} \tag{3.51}$$

$$\begin{aligned} i_c &= -qD_nA_e\frac{d}{dx}n_{ac}(x)\big|_{x=W_B} \\ &= \frac{qD_nA_e}{kT}\left(\frac{qv_{eb}}{kT}\right)\frac{n_{dc}(0) - n_c\cosh(W_B/L_n')}{\sinh(W_B/L_n')} \end{aligned} \tag{3.52}$$

Starting with these results, one can calculate the high-frequency common-base current gain α, the high-frequency transconductance g_m, and the high-frequency common-emitter admittances y_{11e} and y_{21e}. It is a straightforward but cumbersome task. For simplicity, M. B. Das solved this problem in two steps[19, 26, 42-44]. First, he obtained the base region minority carrier concentration and the two-port admittance parameters of the intrinsic HBT under the assumption of infinity carrier velocity through the collector depletion layer. Then the effects of the excess base region stored charge, and that in the collector-base depletion region are reconsidered, and added to obtain the overall forward transfer admittance y^i_{21e} of intrinsic device as follows

$$y^i_{21e} = g_m \frac{e^{-j\omega(k_0\tau_{b0}/s_0)}}{1 + (j\omega\tau_{b0}/s_0)} e^{-j\omega\tau_{bs}} \frac{\sin(\omega\tau_{cs}/2)}{\omega\tau_{cs}/2} e^{-j\omega(\tau_{cs}/2)} \tag{3.53}$$

where $k_0 \approx 0.61$, $s_0 \approx 4.79$, $\tau_{b0} = \frac{W_B^2}{2D_n}$, $\tau_{bs} = \frac{W_B}{v_{sat}}$, $\tau_{cs} = \frac{x_{dc}}{v_{sat}}$, and x_{dc} is the thickness of the base-collector depletion region.

The common-emitter input admittance y^i_{11e} can be expressed in terms of the common-emitter transadmittance y^i_{21e} and the common-base input admittance in this way

$$y^i_{11e} \approx y_{11b} - y^i_{21e} \tag{3.54}$$

By using a series expansion of y^i_{21e}, and neglecting the second and higher order terms in ω, finally we have

$$y^i_{11e} \approx g_m \frac{(1-\alpha_0)}{a_0} + j\omega g_m \tau^i_{ec} \tag{3.55}$$

where $\tau^i_{ec} = \tau_{b0} + \tau_{bs} + (\tau_{cs}/2)$.

(3.55) can be used to construct a high-frequency equivalent circuit model for the intrinsic HBT, which is shown in Fig. 3.5 (a).

3.4.0 The Complete Equivalent Network Model

At high frequencies, the impacts of the parasitic resistances and capacitances on the characteristics of HBTs can not be neglected. A complete equivalent circuit model of HBTs must include the parasitic RC network so as to be able to characterize the transistor more accurately. Among them, two of the most important ones are base resistance and collector capacitance. As mentioned in the previous chapter, the base-resistance-collector-capacitance time constant can affect the frequency response significantly. On the other hand, the potential drop on the base resistance will modify the internal emitter-base bias. This modulation, though very small, will cause a large difference due to the exponential diode relationship between I_c and V_{BE}.

To model the parasitic RC network in HBTs, a lumped equivalent circuit model shown in Fig. 3.5 (b) can be used if it is satisfied with the condition that the sizes of the emitter and base stripe widths and lengths are much less than the signal wavelength in the device, as is the case assumed here. Following Das' analysis[19], the base resistance is comprised of three components, namely, the spreading base resistance under the emitter, the resistance between the emitter and base metal stripe, and the transfer resistance under the ohmic contact. The overall base resistance can thus be written as

$$r_{bb'} = r_{b'} + r_{b1} + r_{b2} \tag{3.56}$$

where

$$r_{b'} = \frac{\rho_{b'} S_E}{12 W_B L_E}$$

$$r_{b1} = \frac{\rho_{bs} S_{EB}}{2 L_E}$$

$$r_{b2} = \frac{\rho_{bs'} L_T \coth\left(S_B / L_T\right)}{2 L_E} \tag{3.57}$$

where $\rho_{b'}$ is the intrinsic base region resistivity, ρ_{bs} is the sheet resistance of the extrinsic

base layer between the emitter and base contacts, and $\rho_{bs'}$ is the same under the ohmic contact. The transfer length L_T is obtained from

$$L_T^2 = (\rho_c / \rho_{bs'}) \quad (3.58)$$

where ρ_c is the ohmic contact resistivity.

The loss element r_{bo} of Fig. 3.5 (b) represents the base contact resistance, and is given as

$$r_{bo} = \frac{r_c(base)}{2L_E S_B} + \frac{\rho_{bs'}(\Delta t)^2}{2L_E S_B} \quad (3.59)$$

where r_c (base) is the base contact resistivity and Δt is the thickness of the implanted layer (see Fig. 2.1 (a)). The dimensional parameters S_E and L_E are the emitter stripe width and length, respectively. S_B is the base metallization stripe width, and S_{EB} refers to the gap between the emitter and the base metallization.

Note that the base resistance can not be calculated in a straightforward way for ohmic drop because of the *current crowding* effect, which means that the density of injected-electron current has its highest value along the emitter periphery while a minimum at the center of the emitter[45]. This phenomenon is caused by the fact that the potential dropped on the *base spreading resistance* along the lateral base region decreases the emitter-base bias along the same path. Therefore the base current decreases continuously as one moves toward the center line of the emitter. This *current crowding* toward the periphery of the emitter increases with bias and causes localized heating and high-injection effects at relatively low current level because of the uneven current density across the active region. In HBTs, the high base doping minimizes the *current crowding* effect but it can not be avoided completely. Therefore, in order to reduce base resistance and enhance the high-current capability, power transistors are made with interdigitated pattern for base and emitter contacts, which gives rise of a high perimeter-to-area ratio.

As with the base resistance, the collector capacitance is also dissected into several component parts. The elements $C_{b'c}$ and C_{cx} represent capacitances directly under the emitter stripe and that under the base-emitter gap, respectively. These can be represented by the T-networks as shown in Fig. 3.5 (b). The capacitance between the base metallization and the collector is represented by C_{cxo}. The applicable analytical expressions for the component capacitance values are

$$C_{b'c} = \frac{L_E S_E \varepsilon}{x_{dc}} \tag{3.60}$$

$$C_{cx} = \frac{2 L_E S_{EB} \varepsilon}{x_{dc}} \tag{3.61}$$

$$C_{cxo} = \frac{2 \varepsilon L_E S_B}{x_{dco}} \tag{3.62}$$

where x_{dc} and x_{dco} represent the depletion width of the collector-base junction directly under the emitter stripe S_E, and directly under the base-emitter space S_{EB}, respectively.

In view of the distributed nature of the base-collector RC network, an effective base-collector RC time constant can be defined in the following way (considering that the various collector capacitance charging current flow toward the external base)

$$r_{bb'} C_c = C_{b'c} \left(\frac{1}{2} r_{b'} + r_{b1} + r_{b2} \right) + C_{cx} \left(\frac{1}{2} r_{b1} + r_{b2} \right) \tag{3.63}$$

At this point, we will be able to construct the complete equivalent network model based on the various intrinsic and extrinsic device and small-signal circuit characteristics as discussed above. In the network shown in Fig. 3.5 (c), the distributed base-collector capacitance is simplified by splitting it into two parts, one is an inner effective capacitance C_c and the other an outer effective capacitance C_{bc} keeping the total base resistance as a single lumped element. The effective capacitance C_c can be readily obtained from (3.63), and C_{bc} follows from

$$C_{bc} = (C_{b'c} + C_{cx} + C_{cxo}) - C_c \tag{3.64}$$

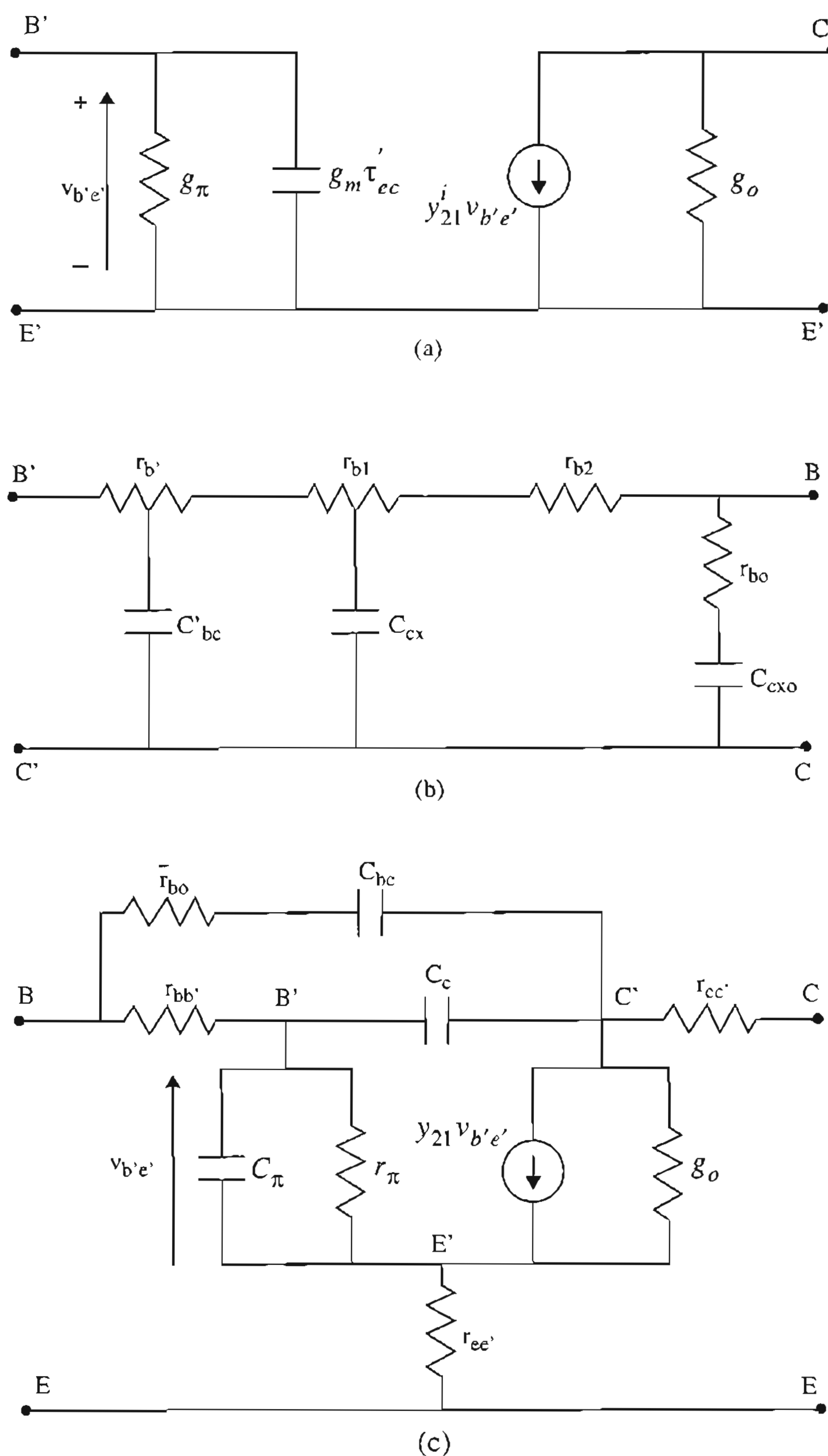


FIGURE 3.5 (a) High-frequency CE HBT internal equivalent network model; (b) Parasitic network model; (c) The complete high-frequency HBT equivalent network model.

Following the discussion given in the previous and current sections, the small-signal T equivalent circuit for HBTs can also be obtained, including the output conductance and the parasitic series resistance, and the split collector capacitance, as shown in Fig.3.6. The components of this circuit have the same definitions as the corresponding components in the hybrid-π equivalent circuit. With the components so designated, the y-parameters for the hybrid-π and the T equivalent circuits are exactly the same[46].

The equivalent circuit shown in Fig. 3.6 is the same as reported elsewhere[20, 46, 47], but some of the components have different values, as we now discuss.

The differences stem both from the level of approximation used for α, and from the manner in which α is represented in the equivalent network.

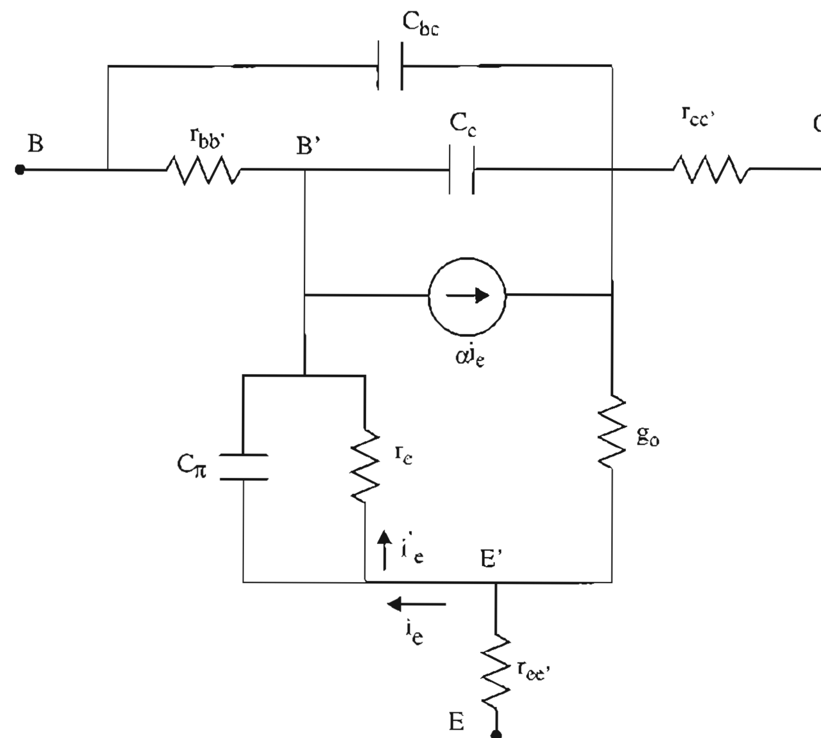


FIGURE 3.6 T equivalent circuit

One difference worth discussing here is that the current source of the equivalent circuit in Fig. 3.6 was represented by $\alpha_0' i_e'$ in ref. [46], and by $\alpha i_e'$ in ref. [20] and [47], as opposed to αi_e used here. The relationship between α_0' and α is

$$\alpha = \frac{\alpha_0'}{1 + j\omega / \omega_\beta} \tag{3.65}$$

where α_0' is a replacement for α_0, the dc common-base current gain of the intrinsic transistor as follows

$$\alpha_0' = \alpha_0 \left(\frac{\sin \omega \tau_c}{\omega \tau_c} \right) exp\,(-j\omega\phi) \tag{3.66}$$

where ω is the angular frequency of operation, τ_c is the collector-base depletion region transit time, as shown in (2.14) and (3.53), and $\phi = m\tau_b / 1.2 + \tau_c$, where τ_b is the base transit time, and m is an empirical factor of magnitude 0.22[20, 48], as compared with the theoretically resultant term shown in (3.53). α differs from α_0' in that it concludes the single-pole (RC-type) representation of the magnitude and phase shift associated with the base transport factor. The reason for that a_0' is used in ref. [46] rather than α is regarded as that the RC phenomenon is naturally represented in the equivalent circuit by the resistance r_e and the effective contribution of the actual base-emitter diffusion capacitance C_d to C_π[36].

As indicated in (3.9), use of $\alpha i_e'$ effectively accounts twice for the term $(1 + j\omega / \omega_\beta)$. The only way to reconcile having a in the current source, r_e and C_d in the emitter circuit is to control the current source by the terminal emitter current i_e, as shown in Fig. 3.6.

In a summary of this chapter, several kinds of transistor models were reviewed. Low frequency, small-signal hybrid-π model can be derived from low frequency T-model, and also, can be extracted from large-signal EM model directly. Hybrid-π model, though equivalent to T-model, proves to be more convenient in the case of common-emitter configuration since it enables the current source to be controlled by the input. The derivation of high frequency prototype transistor equivalent circuit model has to be started from the current continuity equation and diffusion equation. In conjunction with the parasitic network model, a complete high frequency bipolar transistor model can be finally derived on a strict theoretical basis.

CHAPTER IV

HIGH FREQUENCY MEASUREMENTS

4.1.0 General

GaAs-based HBTs have their best advantages in microwave and millimeter wave applications. The high frequency characterization of these devices requires high frequency measurement techniques, which are different from the conventional methods of measuring at dc, and low frequency conditions. At low frequencies, the Z, Y, H, or ABCD parameters can be used in the description of two-port networks. These parameters can be determined by applying short- and open-circuit tests, which are essential for making these measurements. Moving to higher frequencies, some problems arise:

1. Equipment is not readily available to measure total voltage and total current at the ports of network.

2. Short and open circuits are difficult to achieve over a broad band of frequencies.

3. Active devices, such as transistors and tunnel diodes, often will not be short or open circuit stable.

A set of parameters that is very useful in the microwave range are the scattering parameters (S-parameters). These parameters are defined in terms of traveling waves and completely characterize the behavior of two-port networks at microwave frequencies. Since S-parameters are determined with resistive terminations, the difficulties involved in obtaining the broadband open and short circuit conditions required for H, Y and Z-param-

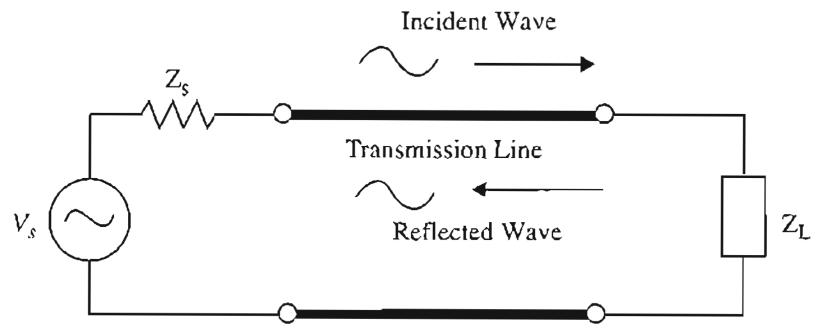
eters are obviated, and the parasitic oscillations in active devices are minimized. Since only incident and reflected voltages need to be measured, automatic network analyzers (ANAs) are currently available for S-parameter measurements. The S-parameters are simple to use in analysis, and can be used not only in the characterization of two-port networks, but also in the characterization of n-port networks. In next section, we'll review the S-parameter concept and introduce some typical transistor parameters that are useful in high frequency characterizations[49, 50], and can be obtained from S-parameters.

The advent of high frequency device era occurred at the same time as the minimum device sizes decreased to $1 \times 1\,\mu m$, and smaller. In the case of small-size devices, the bond pad admittances can overwhelm the intrinsic device S-parameters, leading to significant errors if not corrected for. In order to obtain accurate information to develop accurate models, the current state-of-the-art for measuring devices is to use coplanar probes in conjunction with a network analyzer and a calibration substrate. These probes are designed to provide transmission lines right up to the bond pads of the device under test (DUT), and are currently the most accurate way of guiding high frequency waves onto and off a die, package, or printed circuit board (PCB). In section 4.3, we'll introduce the state-of-the-art high frequency measurement techniques, including the typical equipment setup used for these measurements, the calibration techniques of the measurement system, and the pad parasitics correction procedures[51, 52, 53].

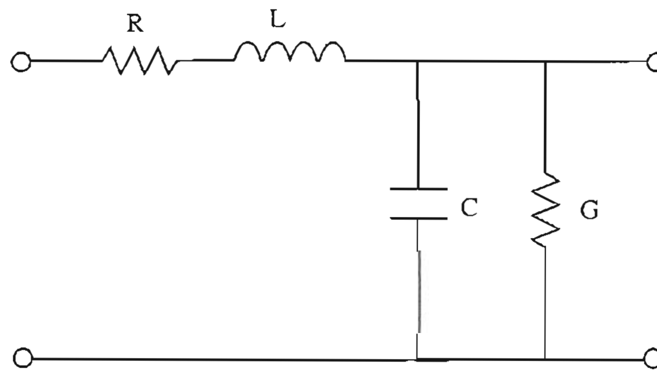
4.2.0 S-parameters and their measurements

Transmission Line Theory

Initially, the properties of traveling wave will be examined. High frequency systems have a source of power. A portion of this power is delivered to a load by means of transmission lines as illustrated in Fig. 4.1 (a).



(a)



(b)

FIGURE 4.1 (a) Power in wave form delivered to a load through transmission lines; (b) Equivalent circuit of uniform transmission line.

Voltage, current, and power can be considered to be in the form of waves traveling in both directions along this transmission line. A portion of the waves incident on the load will be reflected. It then becomes incident on the source, and in turn re-reflects from the source (if $Z_s \neq Z_0$), resulting in a standing wave on the line.

If this transmission line is uniform in cross section, it can be thought of as having an equivalent series impedance and equivalent shunt admittance per unit length, as shown in Fig. 4.1 (b).

A lossless line would simply have a series inductance and a shunt capacitance. The characteristic impedance of the lossless line, Z_0, is defined as $Z_0 = \sqrt{L/C}$. At microwave frequencies, most transmission lines have a 50-ohm characteristic impedance.

The value of the total voltage at a given point along the length of the transmission line is the sum of the incident and reflected waves at that point

$$V(x) = V^{+}(x) + V^{-}(x) \tag{4.1}$$

and the value of the current

$$I(x) = \frac{V^{+}(x)}{Z_0} - \frac{V^{-}(x)}{Z_0} \tag{4.2}$$

Also, the reflection coefficient between the incident and reflected wave can be written as

$$\Gamma(x) = \frac{V^{-}(x)}{V^{+}(x)} \tag{4.3}$$

where $\Gamma_0 = \Gamma(0) = V^{-}(0)/V^{+}(0) = (Z_L - Z_0)/(Z_L + Z_0)$ is the load reflection coefficient.

S-Parameters

If we embed the two-port device into a transmission line, and terminate the transmission line in its characteristic impedance, we can think of the stimulus signal as a traveling wave incident on the device, and the response signal as a wave reflecting from the

device or being transmitted through the device as shown in Fig. 4.2. A new set of equations can then be established to relate these incident and "scattered" waves as

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \tag{4.4}$$

$$V_2^- = S_{21}V_1^+ + S_{22}V^+ \tag{4.5}$$

where V_1^- and V_2^- are the voltages reflected from the first and second ports, V_1^+ and V_2^+ are the voltages incident upon the first and second ports. By dividing through by $\sqrt{Z_0}$ these equations can be altered to a more recognizable form

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{4.6}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{4.7}$$

where $b_i = \frac{V_i^-}{\sqrt{Z_0}}$ and $a_i = \frac{V_i^+}{\sqrt{Z_0}}$. Now $|b_1|^2$ = power reflected from the first port, and $|a_1|^2$ = power incident on the first port. There are similar definitions for $|b_2|^2$ and $|a_2|^2$.

The parameters S_{11}, S_{12}, S_{21}, and S_{22}, which represent reflection and transmission coefficients, are called the *scattering parameters* of the two-port network or *S-parameters*. From (4.6) and (4.7), they are defined as follows

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2 = 0} \quad \text{(input reflection coefficient with the output matched)}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2 = 0} \quad \text{(forward transmission coefficient with the input matched)}$$

which is also the gain or attenuation of the network.

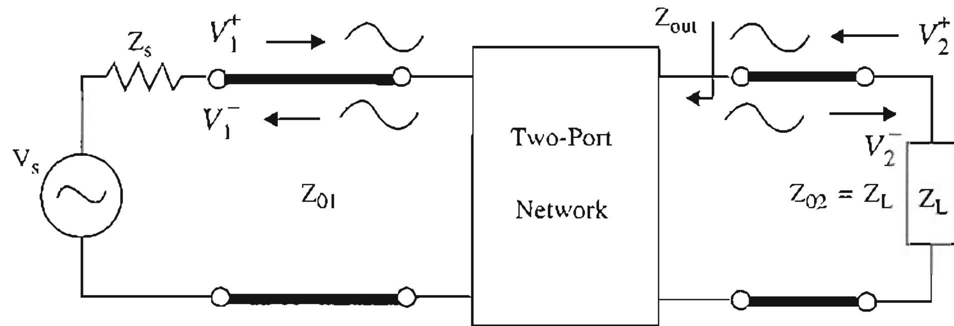


FIGURE 4.2 Two-port network for S-parameter derivation.

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1 = 0} \quad \text{(reverse transmission coefficient with the input matched)}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1 = 0} \quad \text{(output reflection coefficient with the input matched)}$$

S_{11} here is simply reflection coefficient Γ at the input port. This is very similar to how a TDR (time domain reflectometry) functions, where a voltage step is incident on a network and a portion of the incident voltage wave is reflected depending on the network. The TDR reflection coefficient ρ is then

$$\rho = \frac{V_2}{V_1} \tag{4.8}$$

where V_1 is the incident voltage wave, and V_2 is the reflected voltage wave. Measurements of S-parameters and TDR response are fundamentally similar. S_{11} is normally expressed as a reflection magnitude and angle at a particular frequency. A TDR-derived ρ

is expressed as magnitude at a particular point in time or distance, assuming a specific propagation velocity. The biggest practical difference is that S-parameters can be used to develop a quantitative model, whereas TDR data generally provides qualitative data.

The advantage of using S-parameters is obvious from their definitions. They are measured using a matched termination (i.e., making $a_1 = 0$ or $a_2 = 0$). Terminating the output port with an impedance equal to the characteristic impedance of the transmission line produces $a_2 = 0$, because a traveling wave incident on the load will be totally absorbed and no energy will be returned to the output port.

Note that the network output impedance Z_{out} does not have to be matched to Z_{02}. In fact, with $Z_L = Z_{02}$ the condition $a_2 = 0$ is satisfied. Similar considerations apply to measurements at the input port. Also, the characteristic impedances of the transmission lines are usually identical (i.e., $Z_{01} = Z_{02}$).

The Smith Chart

Another basic tool used extensively in conjunction with S-parameters is the *Smith Chart.* Back in the 30s, Phillip Smith, a Bell Lab engineer, devised a graphical method for solving the often-repeated expressions appearing in microwave theory. Solving the equations including expressions like the one for reflection coefficient, $\Gamma = (Z-1)/(Z+1)$, is a tedious task since all the values in this equation are complex numbers, which could be reduced by using Smith's graphical technique. *Smith Chart* was a natural name for this technique.

This chart is essentially a mapping between two planes — the impedance or Z plane and the reflection coefficient or Γ plane. Impedances with positive real parts map inside the unit radius circle on the *Smith Chart.* Impedances with negative real parts map

outside this unit radius circle. Impedances having positive real parts and inductive reactance map into the upper half of the *Smith Chart.* Those with capacitive reactance map into the lower half.

Typical Transistor Parameters

There are three parameters often used by transistor circuit designers. They are:

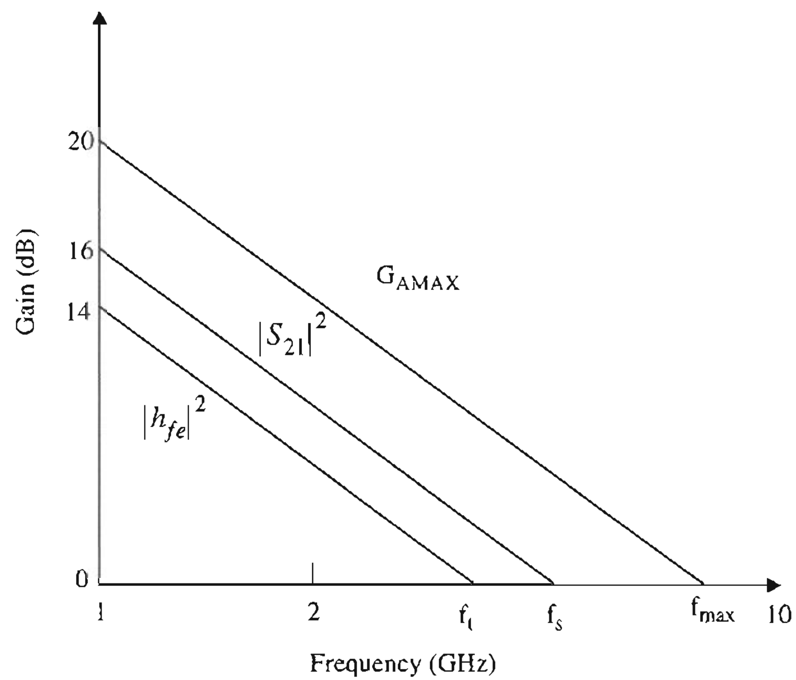


FIGURE 4.3 Schematic plot of several important transistor parameters vs. frequency

1. f_t or the frequency at which the short circuit current gain in equal to one.

2. f_s or the frequency where $|S_{21}| = 1$ or the power gain of the device, $|S_{21}|^2$, expressed in dB is zero.

3. f_{max} or the frequency where the maximum available power gain, G_{amax}, of the device is equal to one. f_{max} is also referred to as the maximum frequency of oscillation.

To determine f_s of a transistor connected in a common-emitter configuration, we drive the base with a 50-ohm voltage source and terminate the collector in the 50-ohm characteristic impedance. This results in a gain versus frequency plot, as shown in Fig.4.3, that decays at about 6 dB per octave at higher frequencies.

Due to the problems involved in obtaining true short circuits at high frequencies, the short circuit current gain $|h_{fe}|$ cannot be measured directly, but can be derived from measured S-parameter data. The shape of this gain versus frequency is similar to that of $|S_{21}|^2$ and, for example, f_t is slightly less than f_s.

f_{max} is determined after conjugately matching the voltage source to the transistor input, and the transistor output to the characteristic impedance of the line. The resultant gain is the maximum available power gain as a function of frequency. It is higher than $|S_{21}|^2$ because of impedance matching at the input and output. With proper impedance matching techniques, the transistor is usable above f_s in actual circuit design.

Transducer Power Gain

In the design of amplifiers, one is most interested in the *transducer power gain*. We will briefly examine it here.

Transducer power gain is defined as the power delivered to the load divided by the power available from the source. If the network is assumed to be unilateral, say, S_{12} is equal to zero, this will refer to the *unilateral transducer power gain*

$$G_{Tu} = \frac{(1-|\Gamma_s|^2)}{|1-S_{11}\Gamma_s|^2} \cdot |S_{21}|^2 \cdot \frac{(1-|\Gamma_L|^2)}{|1-S_{22}\Gamma_L|^2} \tag{4.9}$$

where Γ_s is the source reflection coefficient, and Γ_L is the load reflection coefficient.

Maximum unilateral transducer gain can be accomplished by choosing impedance matching networks such that $\Gamma_s = S_{11}^*$ and $\Gamma_L = S_{22}^*$. Then

$$G_{Tumax} = \frac{1}{1-|S_{11}|^2} \cdot |S_{21}|^2 \cdot \frac{1}{1-|S_{22}|^2} \tag{4.10}$$

or as shown in Fig. 4.4

$$G_{Tumax} = G_{smax} \cdot |S_{21}|^2 \cdot G_{Lmax} \tag{4.11}$$

(4.12)

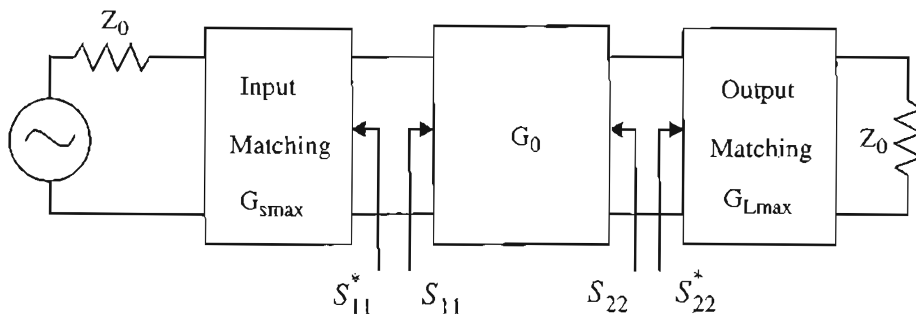


FIGURE 4.4 Network designed for maximum unilateral transducer gain

4.3.0 High-Frequency Measurement Techniques

High-Frequency Measurements Setup

A complete and accurate testing of fabricated devices provides the feedback that is essential for modeling, design and processing iterations. A complete test routine includes in-process testing, on-wafer measurements, chip measurements, package measurements, and the printed circuit board (PCB) level measurements, related to different fabrication stages. From another standpoint, the measurements can also be classified as interconnect measurements, device measurements and IC measurements. For the purpose of device modeling, we are here focusing on the high frequency device measurements mainly in on-wafer or chip form. Fig. 4.5 shows the on-wafer noise and S-parameter measurement setup. The system is comprised of four parts: (a) a vector network analyzer, (b) noise source, a radiometer for noise power detection and electronic tuners, (c) wafer probes and an automatic probe station, and (d) a control computer, microwave switches, bias supply, and software. Specifically, the system can be used to measure the S-parameters, noise parameters, constant noise circles, gain parameters, and gain circles of HBTs. In this system, the S-parameters and noise parameters are measured by coupling the network analyzer to noise measurement equipment. The DUT is first tuned for gain with the switches on tuner. Then, the switches are moved to the measurement loops, and the S-parameters and noise figure are measured. The classic noise-parameter measurement system uses a manual or automated tuner on each end of the DUT[54]. The tuners are used to simulate the input and output matching networks of a low-noise amplifier stage, so the noise figure and gain can be measured directly. The optimum source and load impedances can be found by locking the tuner at its optimum setting and measuring the tuner impedance with a network analyzer.

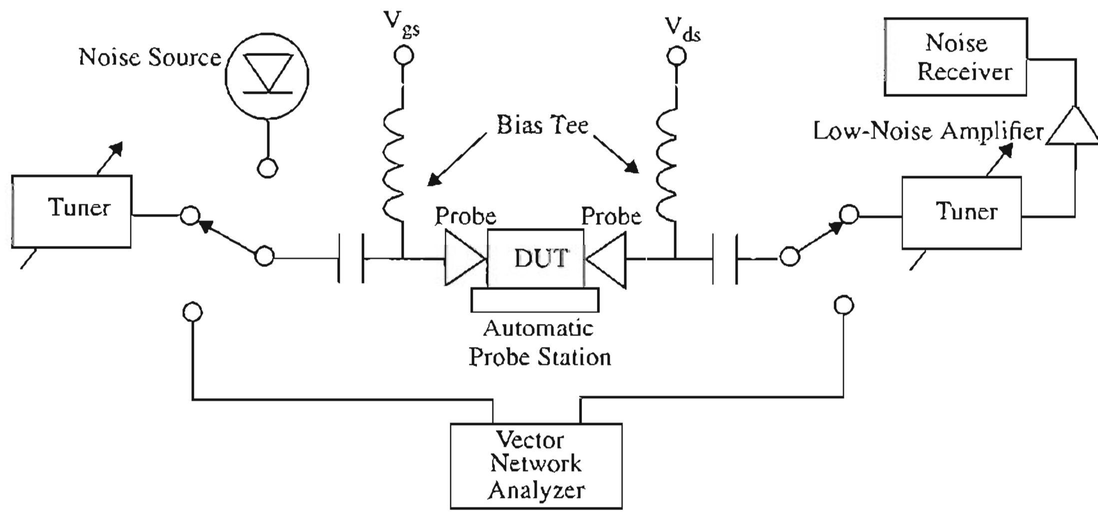


FIGURE 4.5 Combined S-parameter and noise parameter measurement setup.

Since conventionally used needle probes do not work in high frequency measurements, coplanar waveguide wafer probes have to be used. These coplanar probes are designed to provide transmission lines all the way to the probe tips, and match fields from the DUT through the coaxial connector all the way to the scope, TDR, or network analyzer. There are all kinds of probes available depending on needs in different layout and required frequency range, currently through 65 GHz.

For chip measurements, test fixture and test carrier with suitable matching circuits have to be developed first. During the measurement, a fixed matching circuit is not expected to provide perfect matching (due to insufficient knowledge of device S-parameters and noise parameters). An empirical approach to fine-tuning the performance of the matched device is typically employed so that the true potential of the device can be determined.

Calibration of the system

To calibrate the system, the vector network analyzer is first calibrated at the DUT connection planes. By using planar calibration standards, for example, like the Impedance Standard Substrate (ISS) made by Cascade Microtech, the probe and cable responses can be calibrated out. This substrate contains various precision elements, including 0.3% trimmed resistors, transmission lines, shorts, and throughs necessary to calibrate the measurement system up to the probe tips. Conventional calibration sequence is to perform open (probes in air), shorts, 50Ω load, and thru calibrations to the probe tips. Recently, Cascade Microtech and Hewlett-Packard jointly developed the state-of-the-art *line-reflection-match (LRM)* ISS, which provides one with faster, more accurate on-wafer measurement calibrations for high frequency applications, by combining the strengths of *thru-reflect-line (TRL)* and traditional *short-open-load-thru (SOLT)* calibration techniques[55]. The particular calibration substrate material, which is typically fabricated on sapphire or alumina for low loss and smooth surface, is irrelevant as long as the calibration standards are well understood and accurately described to the ANA correction algorithm. The characteristics of the standards are defined to the network analyzer, usually with a magnetic tape, so the operator does not have to manually enter them.

While the ISS calibration sets the measurement reference plane at the probe tips, the S-parameters measured will still include the bond pad parasitics. If the desire is to characterize the intrinsic device embedded in an integrated circuit without bond pads, then the measurement must be corrected for the bond pad parasitics. If the desire is to measure a discrete device (with bond pads) which will be used as a discrete device, then the effect of the bond pads should be included in the data and not be corrected for.

Pad Parasitics Correction Techniques

In the case of bond pad parasitics correction needed, an adequate correction measure should be taken. When measuring small, high impedance devices, the bond pad parasitics which affect the measurement accuracy are the parallel RC parasitics associated with the semi-conductive substrate being in close proximity to the pads as shown in Fig. 4.6. The pad parasitics is specially severe for silicon substrate because of the higher conductivity in silicon substrate than GaAs. Assuming pad sizes of $100 \times 100 \mu m$, the parasitic values are the same order of magnitude as typical devices, resulting in significant errors[53].

One recommended technique currently used for correcting pad parasitics is called YPADS methods, which depends on the fact that the primary RC parasitics are in parallel with the pad structure as shown in Fig. 4.6. Therefore, if one converts S-parameters to Y-parameters, and subtracts the measurements of an open set of pads from the measurements of a DUT plus the pads, these parasitics are removed from the measurement.This currently is considered as the most accurate method[56, 57].

The measurement sequence then becomes:

1. Calibrate the entire measurement system to the probe tips.

2. Measure S-parameters of the dummy device (an open set of pads)

    a. Convert S-parameters to Y-parameters, store data.

3. Measure DUT S-parameters.

    a. Convert S-parameters to Y-parameters.

    b. Subtract dummy Y-parameters from DUT Y-parameters.

c. Convert back to S-parameters as desired, store data.

4. Repeat step 2 for each DUT surrounding the dummy.

Additionally, to ensure the measurement accuracy, the system needs to be frequently calibrated using the hot-cold method (which means to connect the external calibrated hot or cold noise source to the DUT and test for all test frequencies). A cross-checking with other systems is also needed.

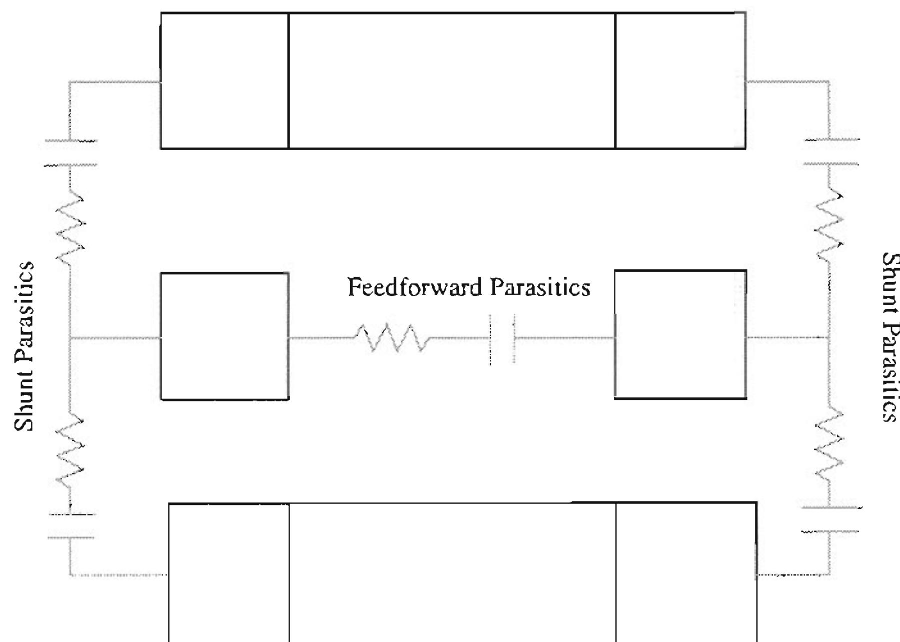


FIGURE 4.6 Pad parasitics affecting measurement accuracy of small devices.

In this chapter, high frequency measurement concepts and techniques were introduced. First, transmission line theories were briefly overviewed, which were followed by the introduction to S-parameters that proved to be a set of effective two-port parameters in overcoming the conventional difficulties in high frequency network analysis routines. The state-of-the-art high frequency measurement techniques are described here and mainly include the equipment setup, calibration method of the system, and the pad parasitics correction techniques.

CHAPTER V

HIGH FREQUENCY MODELING OF ALGAAS/GAAS HBT DARLINGTON FEEDBACK AMPLIFIER

5.1.0 Introduction

Wideband amplification is one of the main purpose of HBTs, which can be best realized by a Darlington feedback amplifier. Despite the abundance of available HBT equivalent circuit models (either large signal or small signal)[58-62], few of them have focused on two-stage devices, such as Darlington-pair configurations. Furthermore, it is more typical to model HBTs with emitter-current controlled T-model rather than hybrid-π model as shown in Ref. [58]-[60]. M. B. Das[19] has theoretically derived a hybrid-π HBT equivalent circuit model for high-frequency purpose, as introduced in Chapter III, but little effort has been made to identify its predicted parameters with actual device structures.

In this chapter, high frequency characterization and modeling of AlGaAs/GaAs HBT Darlington feedback amplifier are for the first time reported. This part of work is done based on the high-frequency measurements of a HBT Darlington configuration feedback amplifier fabricated on epitaxially-grown GaAs/AlGaAs layers. The Darlington configuration device has been chosen in an attempt to investigate the high current capabilities in a cascaded amplifier. Two sets of S-parameters measured under two different bias conditions applied to the device were obtained in chip form using HP 8510 Network Analyzer in conjunction with Cascade Microtech probe system. The high-frequency modeling and simulation are achieved by first creating an equivalent circuit model, and then fitting the

modeled results to the measured data with the aid of SuperCompact, a kind of microwave software. A two-stage small-signal hybrid-π equivalent circuit model is derived for the use of simulation of the actual HBT device, and two sets of element parameters for two different biases have been generated, both of which have excellent agreement with the measured data. T-model is considered as an equality with hybrid-π model, and popularly used in HBT modeling. Here for the case of two-stage simulation, however, it does not work as well as the latter, for some unknown reasons.

DC measurements were also implemented for the purpose of extraction of dc parameters. Some interesting phenomena observed during the characterization practice are discussed to further explore the device physics.

The switching analysis of the device is discussed in the next chapter.

5.2.0 Device Description and S-Parameter Measurements

The AlGaAs/GaAs epilayers were grown by MOCVD techniques, which provided a structure with the process data listed in Table 5.1. The vertical structure of the epilayers is similar to the one shown in Fig. 2.1(a), and designed to meet typical HBT specifications, such as high-doped thin base and low-doped thick collector, and the specific requirements for broadband microwave amplifier applications.

The device under investigation is a Darlington-coupled feedback amplifier consisting of 2 HBTs. The corresponding circuit diagram is illustrated in Fig. 5.1(a). As shown in the figure, Darlington configuration is a composite two-transistor device in which the collectors are tied together and the emitter of the first transistor drives the base of the second one. A series resistor is used as a biasing element to control the emitter current of Q_1. This composite transistor can, in principle, be used in place of a single transistor in common-

emitter (CE), common-base (CB), and common-collector (CC) configurations in achieving a much higher current gain (approximately a product of two current gains at each stage), and enhancing driving ability. When used as an emitter follower, the device is identical to the CC-CC connection. When used as a common-emitter amplifier, as shown in Fig. 5.1(a), the device is very similar to the CC-CE connection, except that the collector of Q_1 is connected to the output instead of to the power supply, which results in the reduction of the effective output resistance of the device because of the feedback through r_{o1} of Q_1, and causes an increase of input capacitance because of the parallel distribution of the base-collector capacitances of Q_1 and Q_2. With these specialities, the CC-CE connection is normally preferable in integrated small-signal amplifiers[63]. The term Darlington is often used to both the CC-CE and CC-CC connections.

A compound feedback, which is comprised of current-series and voltage-shunt feedback, is commonly used in broadband amplifiers as it is here. Usually, R_1 is added for dc biasing and has a large value. By proper adjustment of R_f and R_2 in combination with reactive elements, a flatband amplifier can be realized by sacrificing some gain[64]. When higher gain is required more stages can be cascaded in the final amplifier.

The photographic monolithic layout of the device is shown in Fig. 5.1(b). As seen in this picture, this device has a common-emitter configuration with the emitter pad connected to the ground. The first stage consists of one subcell which has two emitter fingers, three base fingers and two collector contacts. The base and emitter fingers are designed in an interdigital structure to increase emitter periphery. By contrast, the second stage has three subcells, each of them having the same topology as the first stage. This arrangement allows a higher output power capability in the second stage. The stripe width and length of emitter fingers are $1.4\mu m$ and $3.0\mu m$ for the first stage, $1.4\mu m$ and $8.5\mu m$ for second stage. The passive components (such as R_f, R_1 and R_2) are formed by thin film techniques.

The S-parameters were measured in a chip form over frequency range 1 GHz-20 GHz using HP 8510B network analyzer and Cascade Microtech microprobe system Summit 10600. The equipment setup is shown in Fig. 5.2. Power to the device under test (DUT) is provided through bias-Tee built in the network analyzer. A 3 m long 50Ω coax line connects the network analyzer with the heavy-duty probe station through SMA connectors. 26 GHz, $150\mu m$ pitch, nickel head-contact wafer probes were used in the measurements and calibrated up to the probe tips using LRM ISS techniques. The device was mounted on a glass slide using double-stick tape. R_b is a $10k\Omega$ resistor connected in series in the backside loop of the network analyzer as a current limit element.

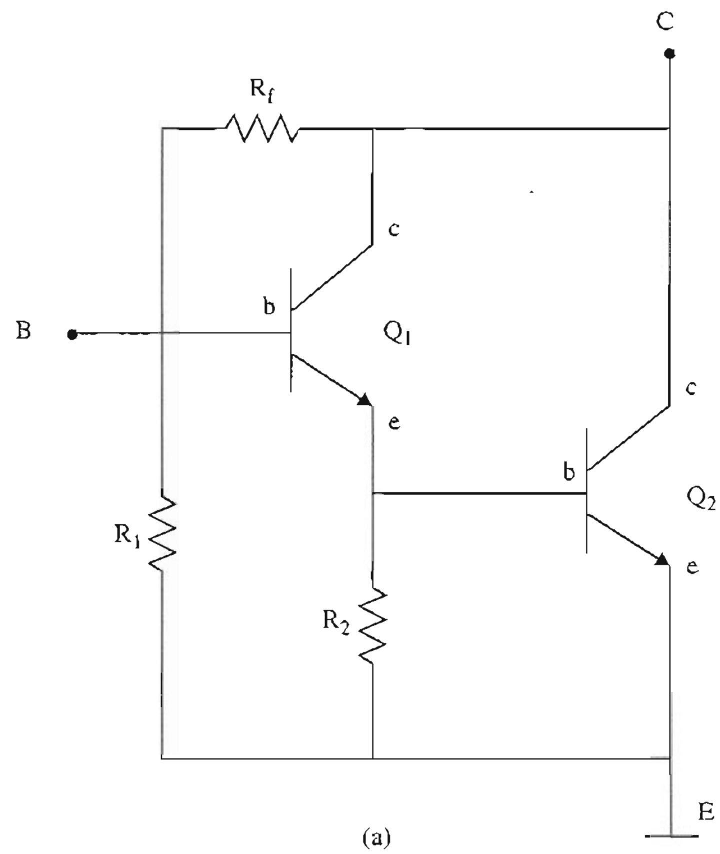
Device was driven by a $-5dBm$ driver and testing started from a relative low V_{CC}. No gain was observed until $V_{CC} \geq 3.5$ volts, which was to be expected for the two-stage transistor configuration.

The device was tested at two different bias conditions. (1) $V_{CC} = 3.5V$, $I_{CC} = 13mA$; (2) $V_{CC} = 3.7V$, $I_{CC} = 23.5mA$. Two sets of *Smith Chart* representations of S-parameters are shown in Fig. 5.3, and 5.4, respectively, from 1 GHz through 20 GHz. The data of S-parameters and h_{12} vs. frequency in the same frequency range were collected on a floppy disk for simulation. A Bode plot is plotted in Fig. 5.5, from which f_t can be found to be about 37 GHz, and $f_{-3dB} = 5$ GHz. The total transit time of the device τ_{ec}, defined as $1/2\pi f_t$, is determined to be $4.3ps$.

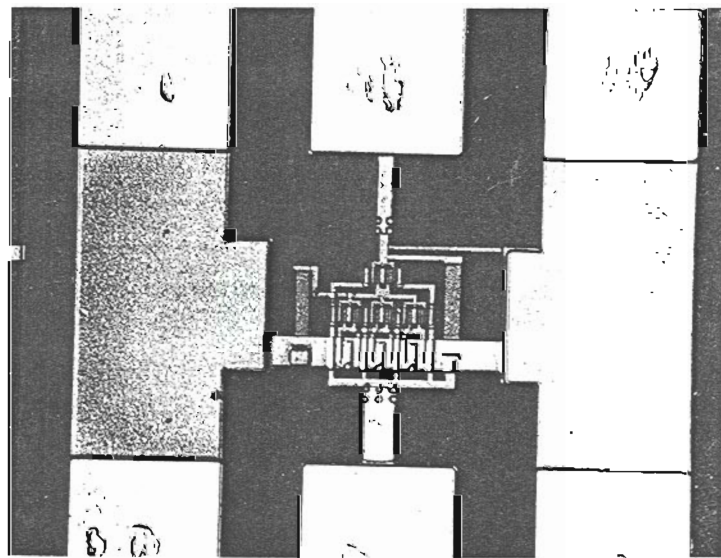
The same device was measured a second time with a 50 GHz probe, and the curves of $|S_{21}|^2$ vs. frequency up to 50 GHz, expressed in dB, are drawn at three different biases of $V_{CC} = 3.2V$, $3.5V$, and $3.8V$ as shown in Fig. 5.6. From this plot it can be found that the optimum bias condition is $V_{cc} = 3.5V$ with the f_s (the frequency where $|S_{21}| = 1$ or the power gain of the device, $|S_{21}|^2$, expressed in dB is zero) as large as 30 GHz.

TABLE 5.1. Epilayer process data

Layer	Material	Thickness (Å)	Doping (cm^{-3})
Emitter Cap	GaAs	2100	4×10^{18}
	$Al_xGa_{1-x}As$ $(0\rightarrow0.25)$	200	$5\times10^{17}-4\times10^{18}$
Emitter	$Al_xGa_{1-x}As$ $(x=0.25)$	800	$1\times10^{17}-4\times10^{17}$
	$Al_xGa_{1-x}As$ $(0.25\rightarrow0)$	200	1×10^{17}
Spacer	GaAs	—	—
Base	GaAs	1000	7×10^{19}
Collector	GaAs	8000	2×10^{16}
Subcollector	GaAS	7000	3×10^{18}
Substrate	GaAs	—	SI



(a)



(b)

FIGURE 5.1 (a) Circuit diagram of Darlington feedback amplifier; (b) Photographic monolithic layout of the device under investigation.

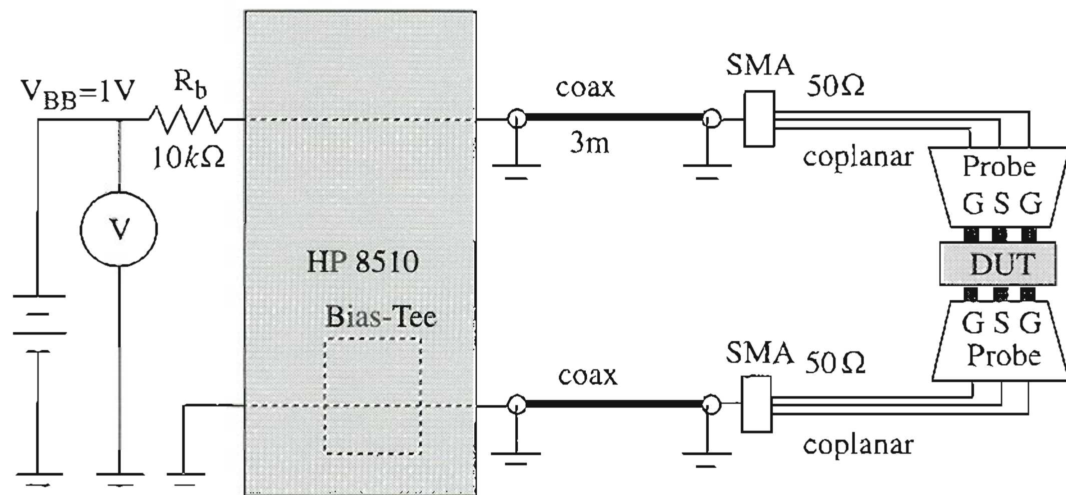


FIGURE 5.2 S-parameter measurement set-up

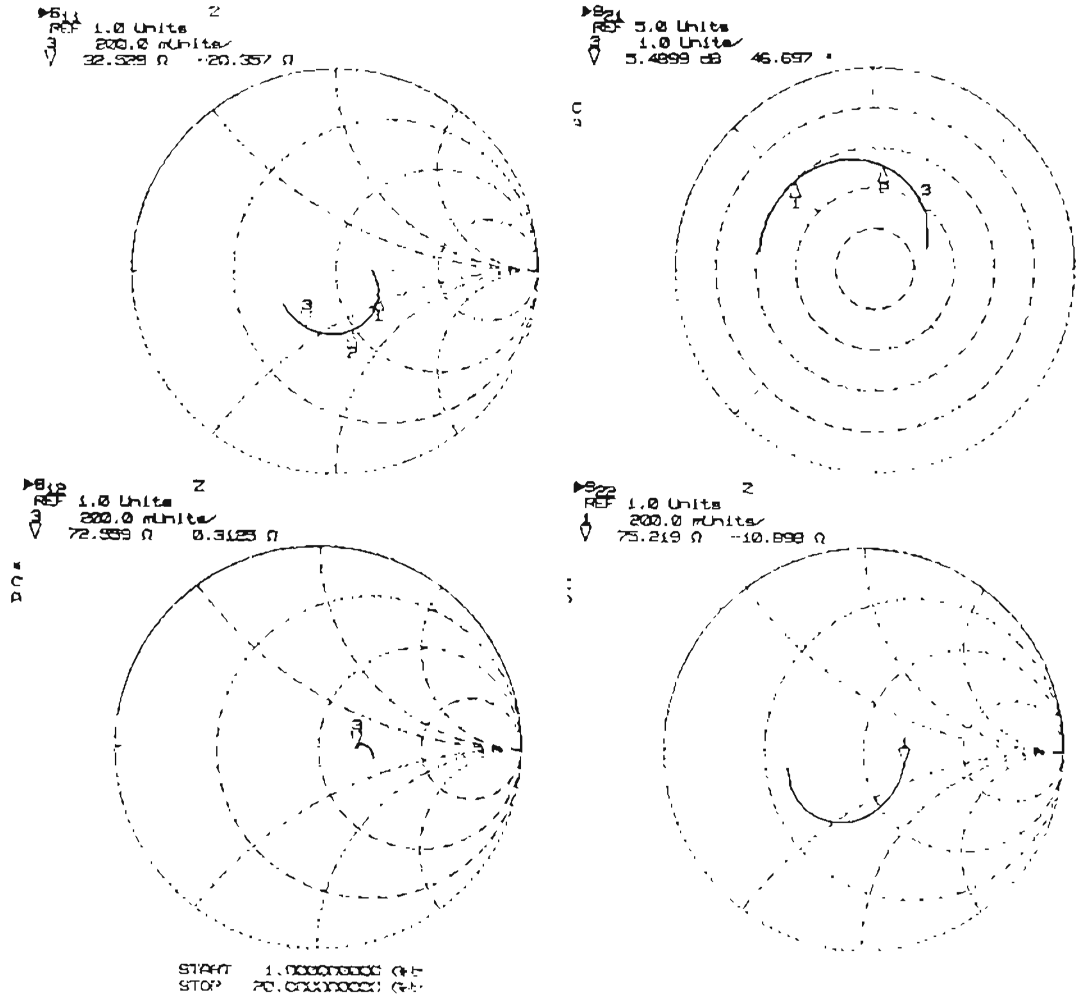


FIGURE 5.3 Smith Charts of measured S-parameters at bias condition V_{CC}=3.5V, I_{CC}=13mA

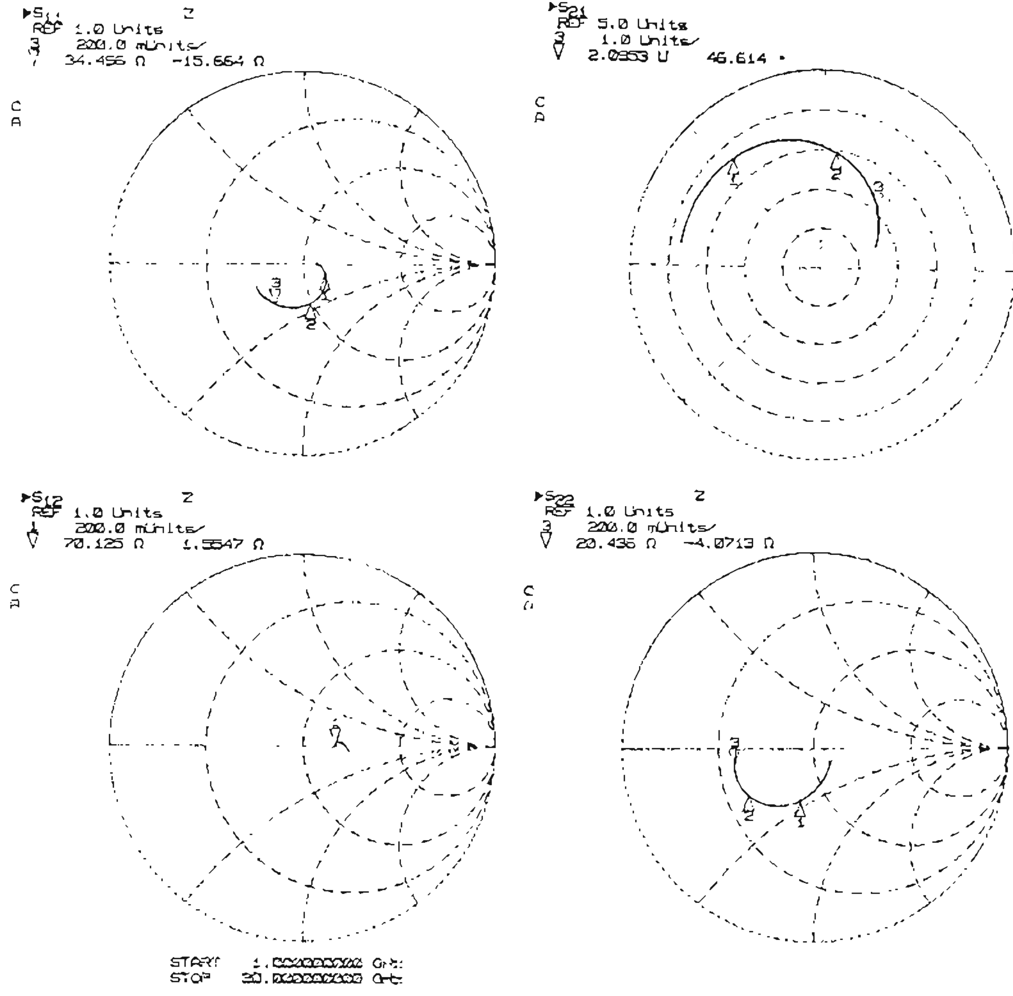


FIGURE 5.4 Smith Charts of measured S-parameters at bias condition V_{CC}=3.7V, I_{CC}=23.5mA

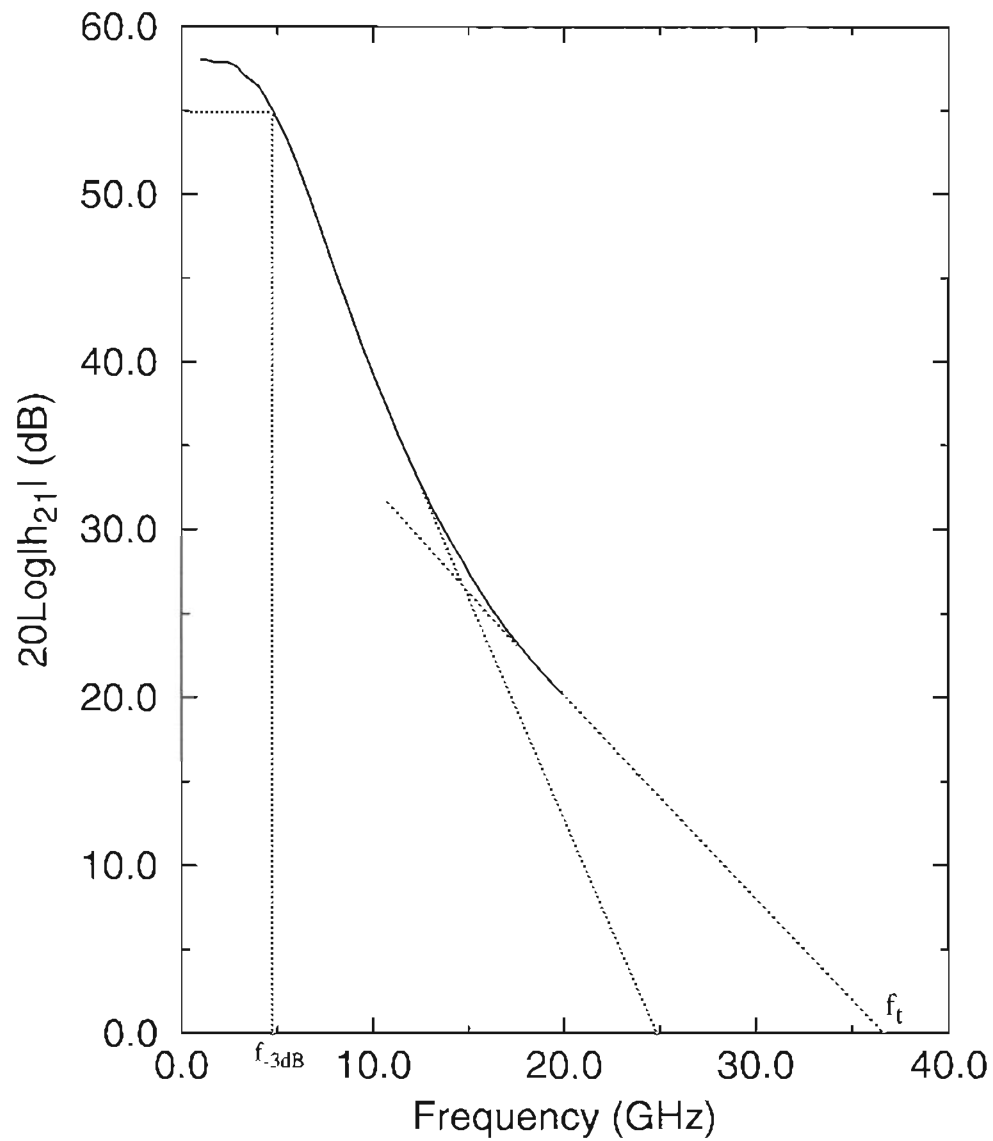


FIGURE 5.5 Bode plot of the device at bias condition V_{CC}=3.7V, I_{CC}=23.5mA.

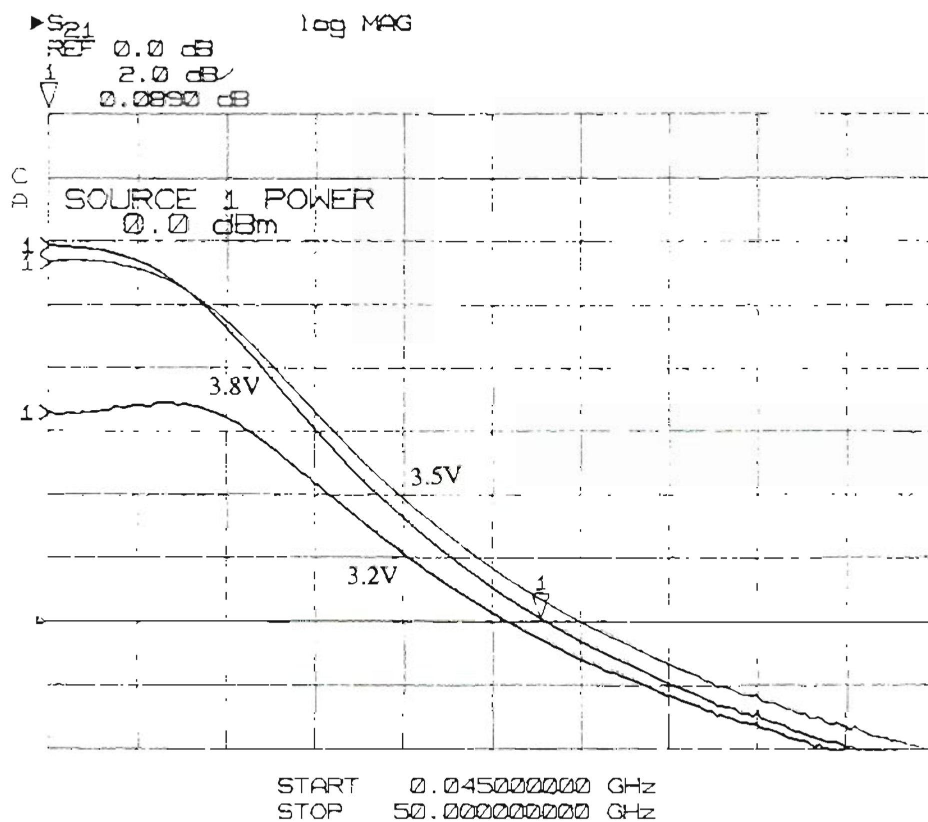


FIGURE 5.6 Power gains vs. frequency up to 50 GHz under different biases with V_{CC}=3.2V, 3.5V, and 3.8V, respectively

5.3.0 DC Measurements and Parameters Extraction

DC characteristics of the device were investigated with a HP 4145B parameter analyzer. Gummel plot of the HBT Darlington composite transistor is shown in Fig. 5.7. In this plot I_B and I_C vs. V_{BE} are plotted in semi-logarithmic form. Note that I_B varies flatly with V_{BE} because a certain amount of current flowing through the bias resistor R_1 all the time under the applied forward bias V_{BE}, therefore when referring to the real base current $I_{B'}$, I_{R_1} has to be subtracted from the total I_B. I_C distinguishes itself by its multi-step configuration. The first step region at the lower end side of V_{BE} is obviously the turn-off region of the device. In this region I_C represents the reverse leakage current which is now at several μA level, a value much larger than that a good device should be, therefore perhaps caused by the instrument error. The second region, in the middle, indicates that the first transistor is conducting, which results in a significant increase in I_C up to mA level. The third step region accounts for the case when the second stage of the device conducts, where the collector current has an additional increase. The total common-emitter forward dc current gain β_F and turn-on voltage of the device can be extracted from the Gummel plot. The turn-on voltage can be readily found to be about $1.2V$ by finding the V_{BE} value at the crosspoint of the first and second regions of I_C curve. β_F of this composite transistor can be obtained by using $I_{B'}$ data mentioned above. The relationship of β_F vs. V_{BE} is shown in Fig. 5.8, in which the dotted curves illustrate the fact that the composite current gain β can be represented by the products of the two gains at each stage.

Additional dc analysis includes the diode I-V curve measurements of the device, through which the values of R_f, R_1, R_2, and R_3 can be extracted by taking measurements of the slopes of these I-V curves in different diode-connection modes. They were found to be 275Ω, 1270Ω, 320Ω, and 16Ω, respectively, for the device under test (DUT).

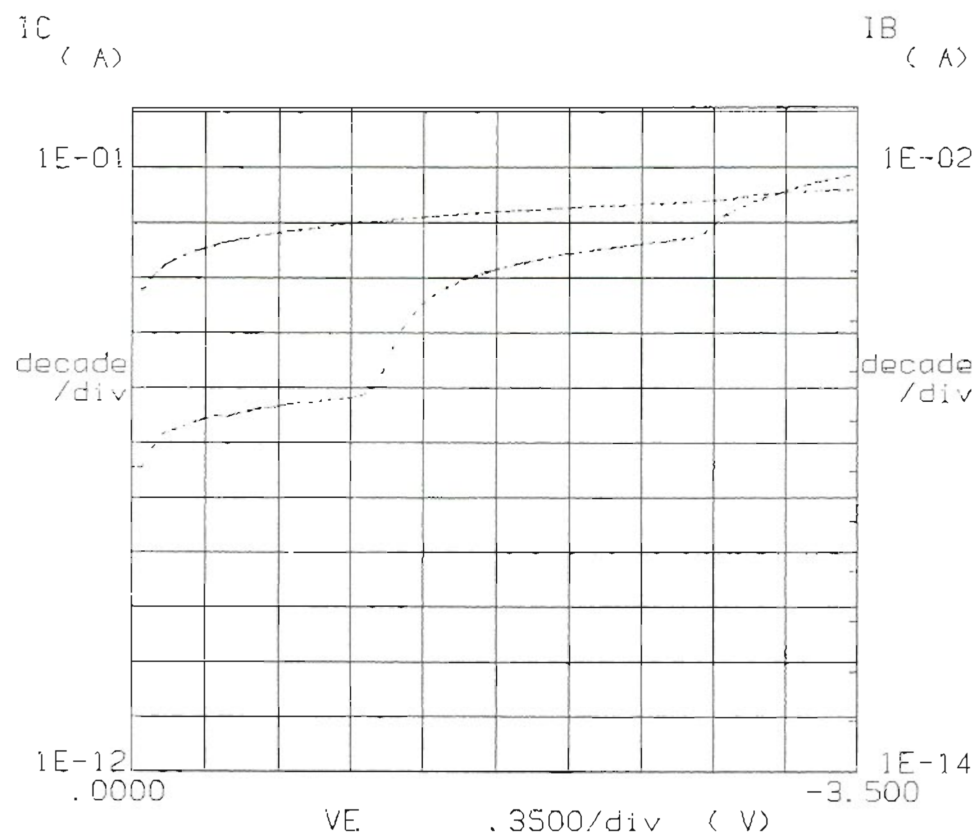


FIGURE 5.7 Gummel Plot of AlGaAs/GaAs HBT Darlington composite transistor

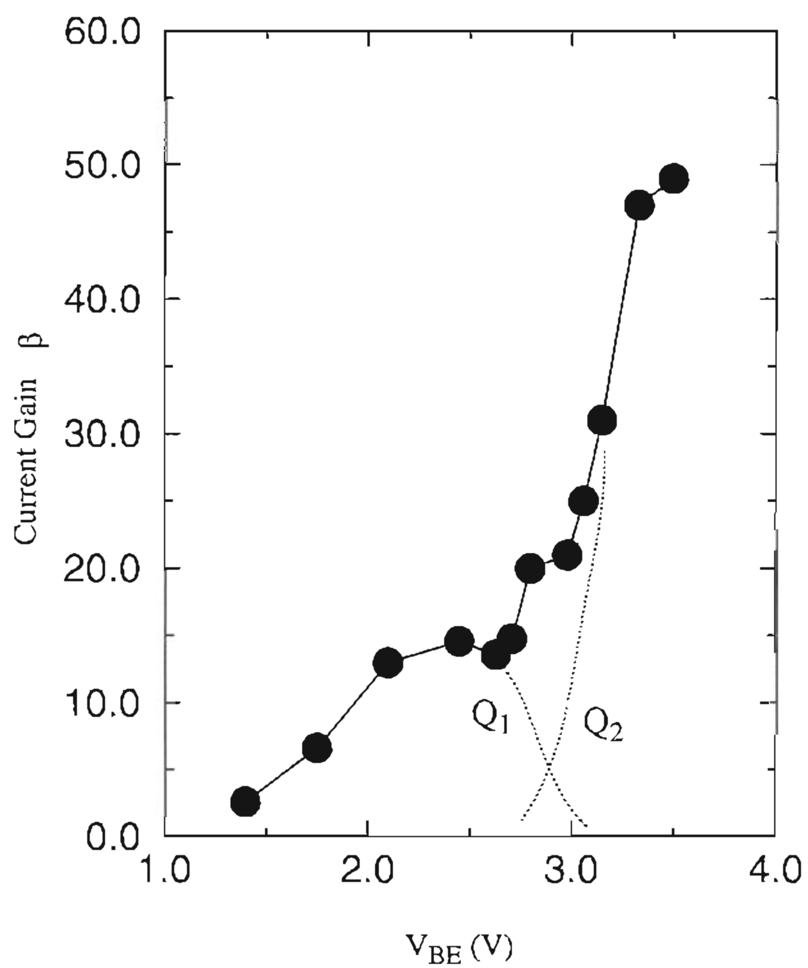


FIGURE 5.8 Common-emitter current gain β vs. base-emitter voltage V_{BE}

5.4.0 Device Modeling and Simulation

SuperCompact was used to simulate the collected S-parameter data and extracted dc parameters. SuperCompact is a software designed for microwave circuit design, synthesis, and simulation, and operates in frequency domain. By taking the measured two-port parameter data as a target, one is allowed to create lumped or a distributed equivalent circuits to model the real devices. Two kinds of optimization algorithm, random and gradient, are available for the optimization of circuit element values to fit experimental data. By adopting an appropriate equivalent circuit model, carefully adjusting the initial parameter values, and alternatively utilizing the optimizors, a good match between the modeled and measured data can be finally achieved.

The SuperCompact program has all kinds of built-in circuit models available for varieties of two-port networks. For example, BIP is a model name designated to bipolar transistor model which is actually a complex of an intrinsic T-model plus a number of periphery elements to account for parasitics, bonding pad capacitance, and lead conduct inductance. VGC is another built-in model name used for voltage-control current generator which can be used as a center part when creating a hybrid-π model.

The whole modeling process conducted here can be summarized in three steps. First step is a process for choosing proper model configuration. It was found after sufficient trials that hybrid-π model is a better choice than T-model because the former has achieved, in this preliminary modeling stage, a smaller error function value, which is defined as a weighted error of the standard objective functions for all the model parameters at all frequencies. Then every effort was made to improve the single-stage hybrid-π model. After a failure to achieve a satisfactory result with such a simple model, which can only reach an error function value of 0.11, a two-stage model based on the former single-stage prototype circuit model was developed. An obvious improvement was immediately observed, and significant progress was made after taking the following steps:

(a) The input and output matching network consisting of a series inductance and a shunt capacitance were added to the ports of the two-port model network to simulate the bonding pad parasitics and lead inductance.

(b) Inductive elements were inserted in the series at the collector terminals to improve the broadbanding characteristics. Specially, it was found that the inductor inserted in the first-stage loop had played a very important role in S_{21} curve simulation, and its value finally fixed at about 0.5 nH, a value one order of magnitude larger than the second stage equivalent.

(c) The base-collector capacitances were split-up in an attempt to better represent the distributed base-collector RC network.

An excellent fit was eventually achieved with a statistically-based error function value of only 0.0083 for the case of $V_{CC} = 3.5V$ bias condition. A similar result was obtained later for $V_{CC} = 3.7V$ with an error function value of 0.0092. Fig. 5.9 and Fig. 5.10 show the *Smith Charts* drawn by the SuperCompact program with both the modeled and measured S-parameter curves on them for comparisons. Fig. 5.11 plots the circuit diagram of the small-signal two-stage lumped hybrid-π equivalent circuit model used in this device simulation process, and the corresponding element values obtained at different voltage supplies are listed in Table 5.2.

Although the single-stage model does not work well, a comparison between the single- and two-stage model parameter values is still informative. It can be seen that the output resistance r_o in the single-stage model is approximately equivalent to the values of r_{o1} and r_{o2}, the output resistances in the two-stage model, shunted together. On the other hand, r_π of the single-stage model approximates to be the sum of $r_{\pi 1}$ and $r_{\pi 2}$ in the two-stage model while with g_m remaining almost the same as g_{m1} (see Appendix A for one-stage model data).

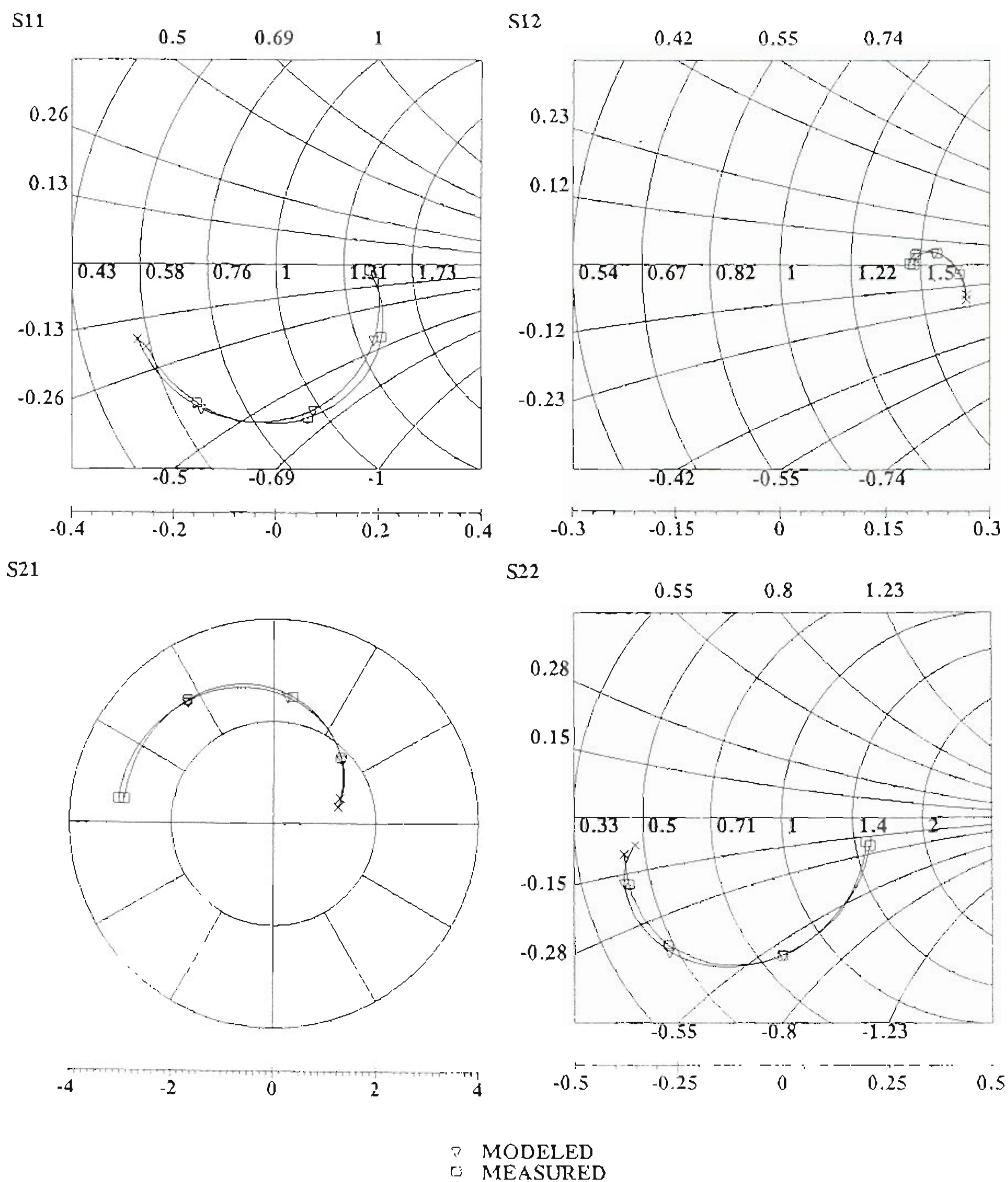


FIGURE 5.9 Comparison of modeled S-parameters with measured data obtained at V_{CC}=3.5V, I_{CC}=13mA. □ — 1GHz; × — 20GHz.

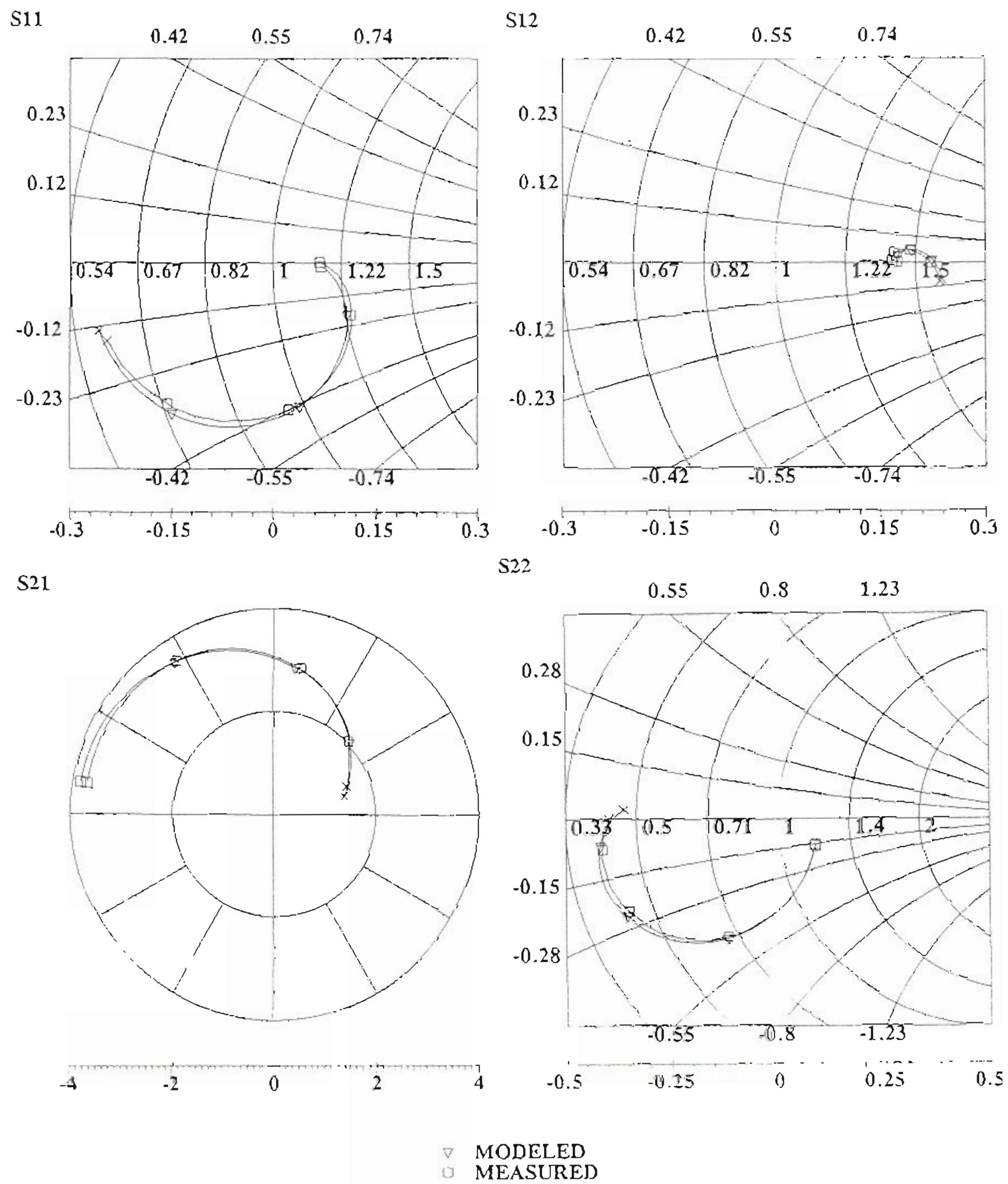


FIGURE 5.10 Comparison of modeled S-parameters with measured data obtained at V_{CC}=3.7V, I_{CC}=23.5mA. □ — 1 GHz; × — 20 GHz.

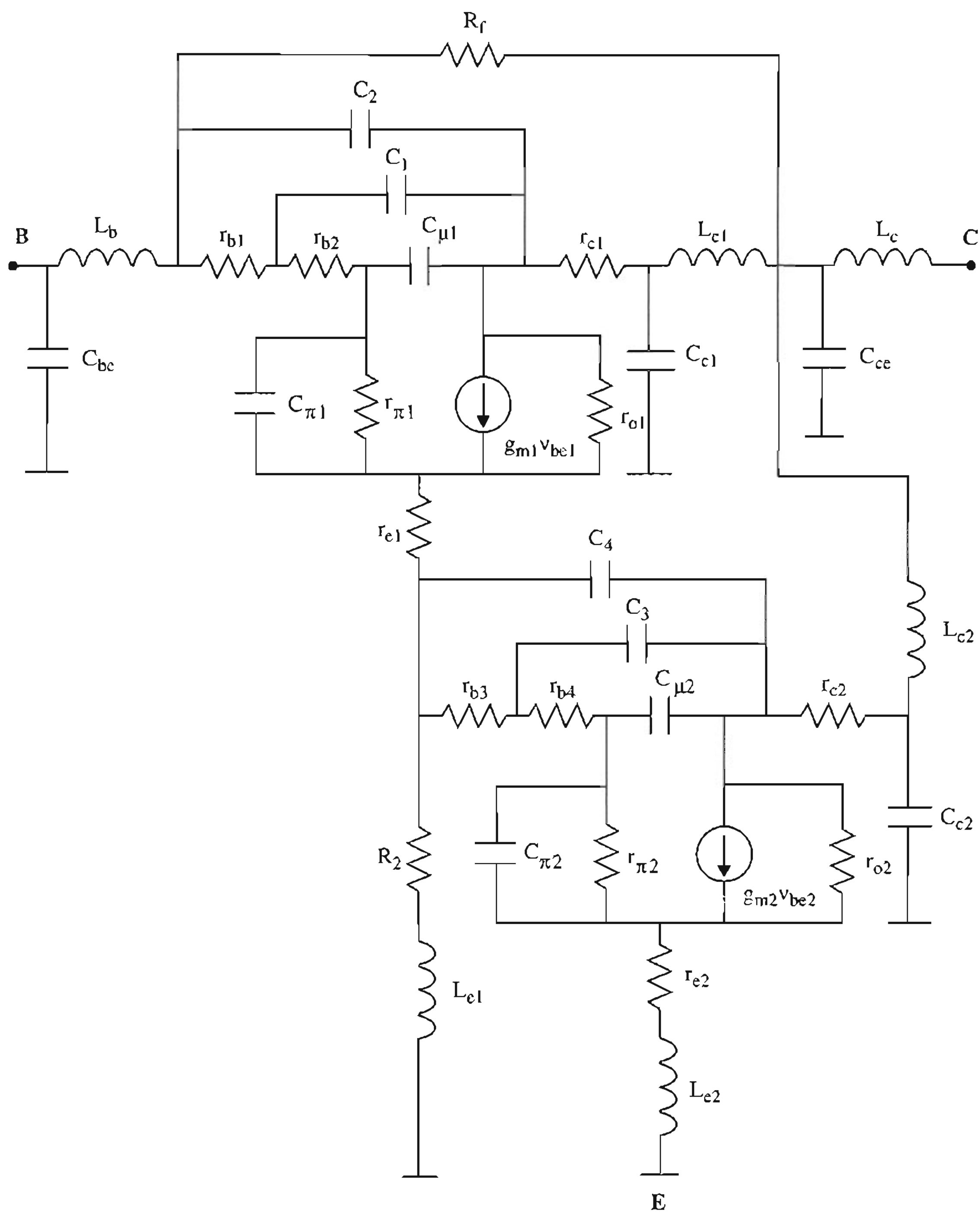


FIGURE 5.11 Diagram of hybrid-π small-signal high-frequency two-stage equivalent circuit model of HBT Darlington-pair feedback amplifier

TABLE 5.2. Modeled two-stage equivalent circuit element values

Element	V_{CC}=3.5V	V_{CC}=3.7V	Element	V_{CC}=3.5V	V_{CC}=3.7V
r_{b1}	14.28Ω	12.81Ω	r_{b3}	57.49Ω	66.82Ω
r_{b2}	6.18Ω	5.38Ω	r_{b4}	14.83Ω	16.25Ω
$r_{\pi 1}$	$9.59 \times 10^5\Omega$	$4.23 \times 10^3\Omega$	$r_{\pi 2}$	$7.32 \times 10^5\Omega$	$7.19 \times 10^5\Omega$
r_{o1}	$1.51 \times 10^6\Omega$	$1.44 \times 10^6\Omega$	r_{o2}	$1.82 \times 10^6\Omega$	$1.85 \times 10^6\Omega$
r_{e1}	48.57Ω	59.53Ω	r_{e2}	12.82Ω	13.83Ω
r_{c1}	1.30Ω	1.68Ω	r_{c2}	2.83Ω	4.14Ω
$C_{\pi 1}$	$65.14FF$	$69.62FF$	$C_{\pi 2}$	$0.17PF$	$0.17PF$
$C_{\mu 1}$	$34.34FF$	$32.21FF$	$C_{\mu 2}$	$40.95FF$	$27.54FF$
C_1	$9.63FF$	$13.21FF$	C_3	$42.32FF$	$30.68FF$
C_2	$4.49FF$	$2.61FF$	C_4	$15.03FF$	$10.76FF$
g_{m1}	$0.06468S$	$0.09075S$	g_{m2}	$0.05682S$	$0.0862S$
R_f	262.91Ω	268.06Ω	R_2	398.86Ω	—
C_{be}	$33.4FF$	$33.7FF$	C_{ce}	$3.62FF$	$17.9FF$
C_{c1}	$3.40FF$	$17.9FF$	C_{c2}	$35.22FF$	$18.4FF$
L_b	$0.085NH$	$0.036NH$	L_c	$0.012NH$	$0.014NH$
L_{e1}	$0.036NH$	—	L_{e2}	$0.041NH$	$0.059NH$
L_{c1}	$0.536NH$	$0.502NH$	L_{c2}	$0.035NH$	$0.021NH$

5.5.0 Discussions

Base-Collector Capacitances

In this model, the distributed base-collector parasitics are simulated by split-up RC networks. The equivalent base-collector capacitance can be approximately expressed as $C_{c_1} = C_{\mu 1} + C_1 + C_2$ for the first stage, and $C_{c_2} = C_{\mu 2} + C_3 + C_4$ for second stage. In the case of forward-active operation mode, base-collector junction is under a reverse bias, therefore the base-collector capacitance is mainly determined by the fixed space charges stored in the base-collector depletion region, which is usually modeled by a depletion capacitor. Depletion capacitance is a nonlinear function of the voltage across the junction, and can be expressed as

$$C_{jc}(V_{B'C'}) = \frac{C_{jco}}{\left(1 - \frac{V_{B'C'}}{\phi_c}\right)^{m_c}} \tag{5.1}$$

for a npn transistor, where $V_{B'C'}$ is the voltage across the internal base-collector junction, C_{jco} is the value of the base-collector junction capacitance at $V_{B'C'} = 0$, ϕ_c is the base-collector barrier potential, and m_c is the base-collector capacitance gradient factor. For a step junction, $m_c = 0.5$, for a linear junction, $m_c = 0.33$. Most of practical junctions lie in between. Assuming a step junction formed here, the base-collector C-V plot should simply follow the well-known reciprocal square-root relationship, which expects a monotonously decreasing curve with a faster drop-down rate at low reverse bias, a slower decrease rate at high reverse bias, and a flat asymptote at the infinity.

Now look at the element values listed in Table 5.1 for C_{c_1} and C_{c_2}. It can be found that $C_{c_1} \approx 48.46fF$ at $V_{cc} = 3.5V$, and $48.03fF$ at $V_{cc} = 3.7V$, almost no change. By contrast, $C_{c_2} \approx 98fF$ at $V_{cc} = 3.5V$ drops down to about $69fF$ at $V_{cc} = 3.7V$, almost 1/3 lower than the lower bias case. For Darlington device, as is known, the first-stage base-

collector voltage drop is lower than the second one, the magnitude difference depending on the resistance ratio of the voltage-divider in the bias loop. In our case, V_{BC1} is about $-0.7V$, and V_{BC2} is about $-2.3V$. As the supply voltage V_{CC} increases, the reverse voltages across the base-collector junctions increase accordingly, but much smaller at the first stage than the second stage. For example, as V_{CC} changes from $3.5V$ to $3.7V$, only about$-0.04V$ added to the first-stage base-collector junction comparing with an increment of $-0.2V$ at the second stage. According to this, we can expect only a small fraction of change in the junction capacitance values. In fact, a quick estimation can be readily done by inserting appropriate data into Eqn. (5.1), which shows that the first-stage base-collector junction capacitance will drop down by 0.01 as V_{CC} increases from $3.5V$ to $3.7V$ if ϕ_c is set up at $1.1V$. This is quite consistent with the modeled results, in which a difference of 0.9% is observed for C_{c_1} at different biases. The disparate thing, however, has happened to the second stage, where a significant drop on C_{c_2} (about 30%) at higher bias has shown a large deviation from the theoretical estimation value which expects only a 3% difference for these two different biases.

As far as the current knowledge, the base-collector junction capacitance under high reverse bias is commonly expected to reach a minimum constant value. This phenomenon was discussed and explained by P. C. Grossman's two-region depletion capacitance model[61] as an effect occurred as the collector edge of the base-collector depletion region reaches the collector contact layer at a sufficient high reverse junction voltage. Nevertheless, it is worth pointing out that the previous studies on this topic, either experimentally or theoretically, were purely focused on the performance of a single pn junction, no transistor behavior ever involved or considered. In the case of a real transistor device operation, as a matter of fact, some transistor effects may affect the junction characteristics, e.g. the junction capacitance under certain conditions. Although the observation obtained here is expected further investigations for more direct evidences, a qualitative discussion based on these modeled data may give rise to some tutorial indications because

simulation results often show us a rather practical circumstance.

For a pn junction with an arbitrarily doped interface region, junction capacitance can be generally expressed in a form of

$$C_{jc} = \frac{\varepsilon A}{x_d} \tag{5.2}$$

where ε is the permittivity of the semiconductor material, A is the junction area, and x_d is the depletion layer width. In an one-side heavily doped junction case, x_d is mainly located in the lightly doped side of the depletion region, e.g. in the collector side for a HBT base-collector junction. As a reverse bias is applied to the junction, the depletion region will become wider. The junction capacitance thus becomes smaller. For a single-side junction, the widening effect mainly occurs in the lightly-doped side. In the case of HBTs, base-collector capacitance will keep going down with the increased supply voltage until the collector region is depleted all the way to the point where the depletion region extends to the heavily doped collector contact layer. At that point the junction capacitance will stop decreasing and keep almost constant afterwards. This can be seen clearly by writing (5.2) into another form:

$$C_{jc} = \frac{\varepsilon A}{x_p + x_n + (x_{nc} - x_n)} \tag{5.3}$$

where x_p is the depletion region width in the base layer, x_n is the depletion region width in the collector layer, and equals x_c, the collector layer width for the time being. $x_{nc} - x_n$ is the part of the collector depletion region invaded into the contact layer. For simplicity, assume a uniform doping profile realized in the base, collector, and collector contact region, respectively, and the depletion region already extends to the contact layer under certain level bias, the charge density distribution in the whole depletion region can be schematically shown (see Appendix B) under depletion approximation, and expressed as:

$$\rho(x) = \begin{cases} -qN_A & -x_p \le x < 0 \\ qN_D & 0 \le x < x_n \\ qN_D^+ & x_n \le x \le x_{nc} \end{cases} \tag{5.4}$$

where N_A, N_D, and N_D^+ are the doping density in the base, collector, collector contact layer, respectively. Using the neutral charge condition, and solving Poisson's equation, $x_{nc} - x_c$ can be found out as (see Appendix B for detail)

$$x_{nc} - x_n = \frac{2\varepsilon\phi_n}{qN_D^+ x_n} \tag{5.5}$$

In this equation, ϕ_n is the potential at the outside edge of the collector depletion region. This result is essentially equivalent to that claimed by Grossman's model. In fact, $x_{nc} - x_n$ is a very small constant compared to x_n, and can be ignored in normal case. In high current case for an actual device, however, x_n could change drastically if some high-injection effect, e.g. Kirk effect, is involved. As Kirk effect occurs, the base layer will push out, and in the meanwhile, the junction will move rapidly towards collector contact layer. In this case, x_n will decrease in a manner much faster than $x_p + x_n$, which causes a rapid increase in $x_{nc} - x_n$, and eventually results in a fast decrease in junction capacitance.

Simple calculation shows that, however, the voltage here across the base-collector junction is not high enough for completely depleting the collector layer. This implies that Kirk effect may occur sometime before x_n has been widened to reach the contact layer. Another question is if Kirk effect can happen in such a relative low bias voltage. The answer is that it may be made possible if there exists severe current crowding and localized heating effects. We'll see it below.

Another point of view for this C-V relationship deviation is the doping profile modification effect. In hyperabrupt doping profile case at the base-emitter junction, for example, the gradient factor m_c can be equal to 2, which may cause a C-V curve as shown

in Fig. 5.12. It was reported that a GaAs hyperabrupt varactor exhibited a capacitance C vs. voltage V characteristics with $m_c = 2$ between 4 and 8 V.[65]

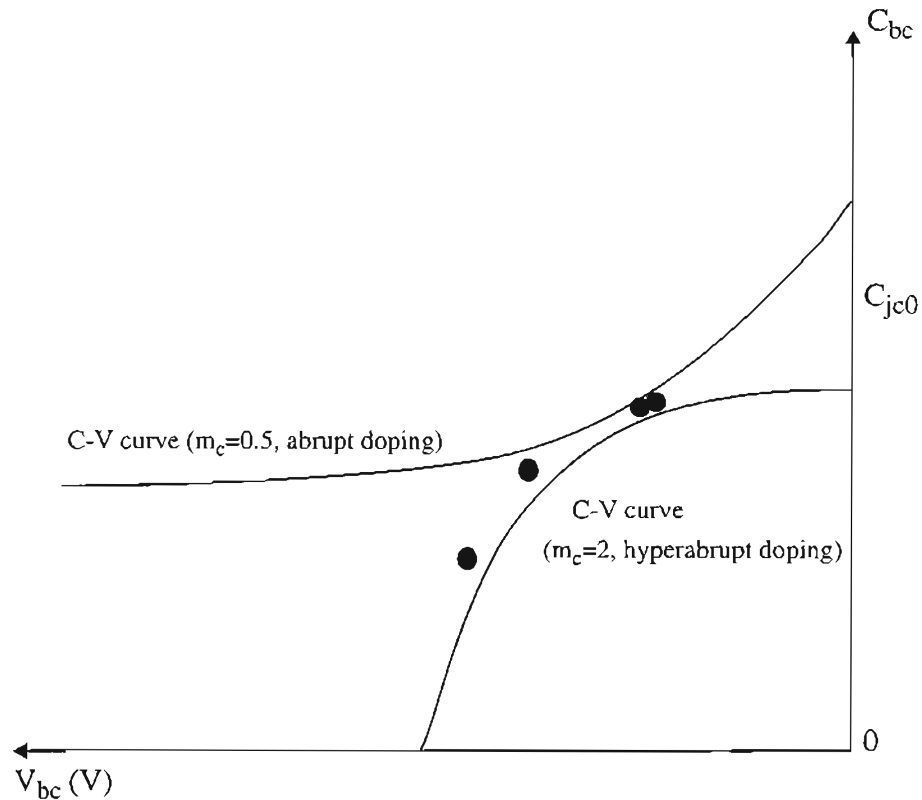


FIGURE 5.12 Schematic plot of second-stage base-collector capacitance deviation from the typical C-V relationship. • model parameter data

Thermal Effect on Base Resistance

As mentioned earlier, the layout of this device has a multi-subcell design at the second stage where the emitter stripe length has been designed longer as well ($8.3\mu m$ at the second stage vs. $3.0\mu m$ at the first stage) for the purpose of high current enhancement capability by increasing the active area and emitter periphery. Theoretically, the increase of subcells will not alter a device's small signal performance if appropriate precautions are taken to minimize the size of parasitics, because as more subcells are connected in paral-

lel, all resistive element values are reduced in proportion to the number of subcells, whereas all the capacitive element values increase by the same factor. The RC product (i.e. charging time) therefore remains constant

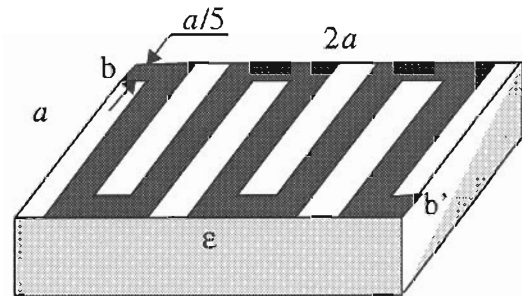


FIGURE 5.13 Exaggerated schematic of degraded external base path, which causes a fairly reduced capacitance but a much increased resistance

The data listed in Table 5.2, however, doesn't follow the theoretical prediction. For example, the base-collector capacitance of the second stage at $V_{CC} = 3.5V$ is only twice as large as the value for the first stage at same bias. And even if take the higher junction voltage factor into account, the ratio of these two capacitances will not surpass 3, a value still much smaller than the capacitance area ratio between these two stages, which is about 9. Perhaps, the reduction of C_{c_2} than the expectation value may be partly attributed to the Kirk effect as discussed above. The significant increase instead of decease of the second stage base resistance, however, makes one even more confused. A possible explanation is that in the second stage there may exist a severe current crowding effect which causes a drastic reduction of active area. The localized heating effect may also have occurred and be responsible for the degradation of the external base path. Specially, external base path degradation may change the external base resistance to a much more severe extent than for

the distributed base-collector capacitance. The schematic graph shown in Fig. 5.13 may give one a clearer idea on this point of view. In this exaggerated graph, the external base area is degraded into a square-wave form path as shown in the figure, which reduces the effective area by a factor of about 1/2, hence the distributed capacitance value reduced by 1/2 correspondingly. But the same fact causes a reduction of the cross-section of the base path by a factor of 5 as well as a 2.5-fold longer path length, which results in a total increase of the external base resistance by a factor of 12.5.

In a contrast to the case of second-stage base-collector capacitance, it is found that almost all the real resistive element values have increased under higher voltage supply by a factor ranging from 1.1 to 1.5, with the only exception of first-stage base resistance $r_{bb'1} = r_{b1} + r_{b2}$. This phenomenon is regarded here as a result from thermal effect. Thermal effect is commonly considered as an important factor affecting HBT performance since semi-insulating GaAs substrate has a poorer thermal conductivity than Si. As is well-known, the electrical conductivity of semiconductor material has a very sensitive dependance upon temperature basically following the relationship

$$\sigma = qN\mu(T) \tag{5.6}$$

where q is electron charge, N is carrier density (electrons for n-type, holes for p-type), and $\mu(T)$ is the carrier mobility, which is a function of temperature, and empirically found in proportion to $T^{-2.3}$ for GaAs material in an intermediate temperature range[66]. The thermal effect on the device here can be estimated by using thermal resistance concept. A reported experimental result shows the local thermal resistance R_{TH} of a 3×10 micron emitter $GaAl_xAs_{1-x}$ HBT on a GaAs substrate is about $1100°C/W$ at $25°C$ and $1200°C/W$ at $50°C$[61]. In this case, with a V_{CC} of $3.5V$ and a I_C of $5mA$ (assume an equal amount of current flowing through each collector), a temperature rise of $19.3°C$ in the second stage above the substrate temperature will occur. As V_{CC} increases to $3.7V$ along with a I_C of about $10mA$ in each collector, a temperature rise larger than $60°C$

above the room temperature seems reasonable. A calculation from (5.6) shows a typical increase in a factor of 1.35, a value right in between our observed range. This large thermal effect has severe consequence on device operation. Given that V_{BE} changes about $-1.4 mV/°C$, the second-stage V_{BE} of the device here will decrease by approximately $0.1 V$, which will largely reduce the second stage collector current. This may explain why a fairly close transconductance value has been obtained in the model, which is considered as unusual for a Darlington configuration device.

5.6.0 Summary

- A small-signal two-stage hybrid-π equivalent circuit model was developed for simulating the high-frequency performance of the AlGaAs/GaAs HBT Darlington feedback amplifier with the aid of SuperCompact software. Excellent agreement with the measured S-parameter data was achieved simultaneously at two different bias conditions.

- Hybrid-π model proved to be more effective than T-model in this case. It has shown that a two-stage equivalent network is a necessity for simulation of a Darlington configuration device. The inductive element connected in series with the first-stage collector terminal is considered as a key element for S_{21} characteristics improvements.

- The severe deviation of the base-collector capacitance values from the typical C-V relationship at high reverse bias shown in the model parameter table implies that high-injection effects, which are often seen in BJTs, possibly exist in cascaded HBTs as well. Parameter variations at different bias also indicate an observable thermal effect on terminal resistances mainly at second stage, where a significant temperature increase is expected due to a larger power dissipation.

CHAPTER VI

SMALL-SIGNAL SWITCHING ANALYSIS OF ALGAAS/GAAS HBT DEVICE

6.1.0 GaAs HBT as A Digital Device

The high-speed related features, such as high f_t and f_{max}, and lower substrate capacitance, make GaAs-based HBTs ideal for digital applications. Frequency dividers are of fundamental importance in frequency synthesizers and clock drivers for digital circuits. The HBT's high-speed capabilities make it ideal for frequency dividers of fixed and variable modulus. Recent report has shown that HBT-based ECL (emitter-coupled logic) frequency dividers have operated up to 36 GHz[67]. Programmable 4/5 dividers operating up to 6 GHz was also reported a few years ago. Phase-locked loop (PLL) frequency synthesizers are critical to communications. The GaAs HBT permits high-edge-rate detection and fast switching to achieve high linearity and low phase noise phase detector which is required in fractional-n PLL synthesizers to minimize the output spurs. Future fiber optic transmitter and receiver circuits operating in the range above 10 Gb/s are potential applications of these functions.

Although Darlington amplifier is not a typical digital device and generally has a slower speed than a single transistor because of its larger base-collector capacitance, it is used here for switching analysis simply because we had already calculated its simulation parameters. On the other hand, it can be certainly considered as a composite heterojunction transistor, and its switching performance evaluation will without doubt reflect HBT's

switching characteristics to some extent.

Since K. Ashar proposed the propagation delay concept as a switching figure, it has led to an effective method of estimating delay time in switching circuits and been commonly considered as a solution for transistor switching analysis. Indeed, this method is applicable to a general class of switching problems. However, in the case of complex circuits, it is rather difficult to find out the transfer function of the network, which is a pre-requisite for the use of Ashar's model. Some other approaches, such as those proposed by Y. Ikawa[68] and M. Kurata[69], either conducted a large-signal transient analysis of semiconductor device based directly on small-signal frequency response data, e.g., S-parameters, or developed a numerical model by directly solving one-dimensional basic device equations under transient condition, without considering an equivalent circuit. These methods, although creative, didn't relate the model to physical parameters, therefore are lack of instructive information for improving device design.

Despite the rapid development of HBT digital devices, their switching characteristics have been less investigated. In this chapter, a new technique is proposed for small-signal (low-level) switching analysis of aforementioned HBT Darlington device in a real experimental environment. High speed measurements using digitizing sampling oscilloscope operated in TDR (time-domain reflectometry) mode were implemented for high-speed characterization and simulation of the device. The basic idea of the present technique is to separate the whole network into input loop and output loop, which will reduce the circuit complexity significantly. Hybrid-π model is adequate to be used for this purpose. The first step of the analysis procedures is to find out the instantaneously changed base current during the switching by analyzing the transient behavior of the input loop. Then four different approaches were employed to solve for the delay time or the output voltage waveforms. They are, charge-conservation method, nodal analysis method, charge-control method, and Spice simulation method. Among them, the charge-control

method is also applicable to large-signal (high-level) switching case. These analytical and computer-aided simulation methods turned out quite consistent results, which also fit the measured data. Through these analyses the designer-concerned extrinsic and intrinsic speed limitations at different circumstances can be seen clearly.

Section 6.2 describes the TDR measurement results. Section 6.3 derives the voltage transfer characteristics of the device, which is indispensable information for the transient analysis of an unknown device. The subsequent sections are focused on the switching analyses and results discussions.

6.2.0 High-Speed Switching Performance Testing

High-Speed pulse response measurements were implemented using Tek 11801 digitizing sampling oscilloscope operated in TDR mode, which is a time domain test method. Schematic measurement set-up is shown in Fig. 6.1. The device under test (DUT) is still the HBT Darlington pair, but packaged at this time. Ground lead was soldered on to a copper ground plane. The input and output leads were soldered to short matched coax lines. The outer conductor of the coax line was made also of copper, and soldered on to the ground plane. The other ends of these coax lines were soldered to SMA connectors, through which the device was connected to the tester. The whole assembly was used as a fixture.

Since the device is self-biased, only one bias-Tee was needed at the collector terminal. A 50Ω "DC Block" (bandwidth =100 MHz — 18 GHz) was required by the measurement system, and inserted on the input side of the DUT, which is actually realized by a $1500pF$ capacitor. The bandwidth of Bias-Tee[a] is also at the same range. $14dB$ attenuation pads were introduced to improve 50Ω matching (helps to prevent ringing).

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a. The bias-Tee was made by Hewlett Packard Company. The value of the inductive element in the equivalent circuit shown in Fig. 6.1 is not available from the maker.

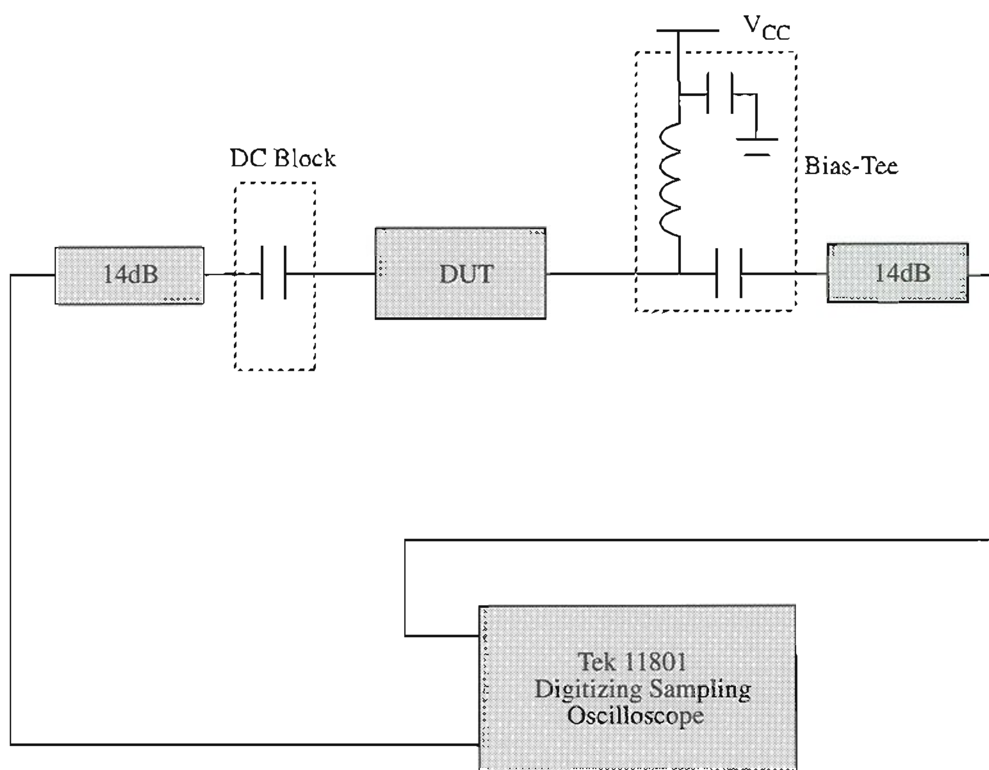


FIGURE 6.1 TDR measurements set-up

The input signal was a series of square-wave pulses, with a period of $1\mu s$, and an amplitude of $0.25V$. The signal generated by the digitizing sampling oscilloscope has a rise (or fall) time of $20ps$ when used in TDR mode, and leaves another edge uncontrolled. A voltage value of $2.7V$ at base terminal was observed from the oscilloscope dc test when the voltage supply was $3.5V$. The system was calibrated to subtract the delay time introduced by the long coaxial lines, but still retained about a $300ps$ delay on input and output coax lead lines.

The test results are shown in Fig. 6.2 and Fig. 6.3. Fig. 6.2 shows that the fall time t_f of the output responding to a "turn-on" input signal is $867ps$, and the propagation delay time is $804ps$. Fig. 6.3 shows that the rise time t_r of the output in response to a "turn-off" input signal is $746ps$, and the propagation delay is $703ps$. For the inverter circuit, the rise (fall) time is customarily defined as the time that it takes the collector current rising (falling) from 10 (90) to 90 (10)% point of the current waveform, and the turn-on propagation delay time is defined as

$$t_{PHL} = t_d + \frac{t_f}{2} \tag{6.1}$$

where t_d is the delay time before the device turns on. The turn-off propagation delay time is defined as

$$t_{PLH} = t_s + \frac{t_r}{2} \tag{6.2}$$

where t_s is saturation delay time.

Some other data sheets collected in the measurements are shown in Appendix D. Fig. D.1 shows the sinusoidal signal response of the device. The frequency of input signal is about 790 MHz and the measured rise time and fall time are $338ps$ and $365ps$, respectively. Fig. D.2 shows the return and insert losses of the packaged device measured at the frequency range 0.5 GHz - 15.5 GHz at different biases for the two ports, respectively.

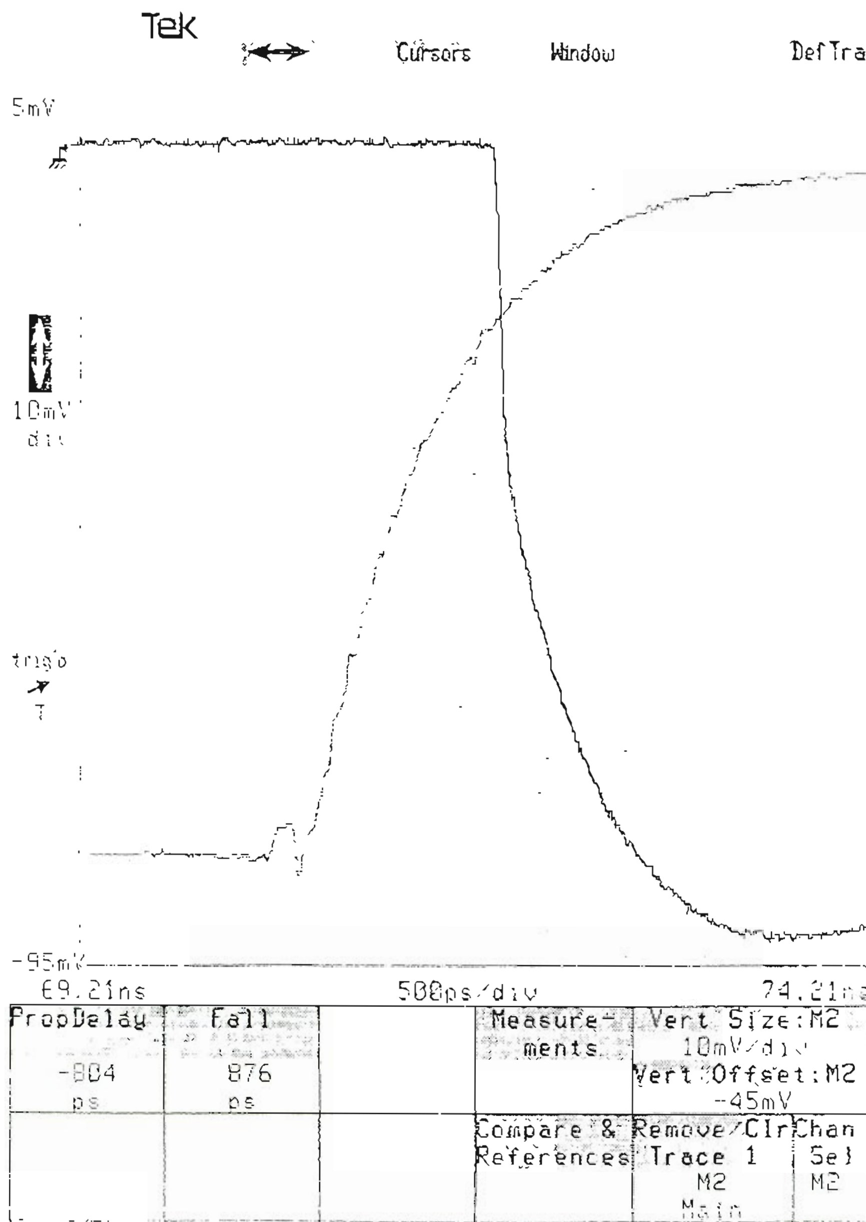


FIGURE 6.2 High speed step signal response of HBT Darlington device for "turn-on" case

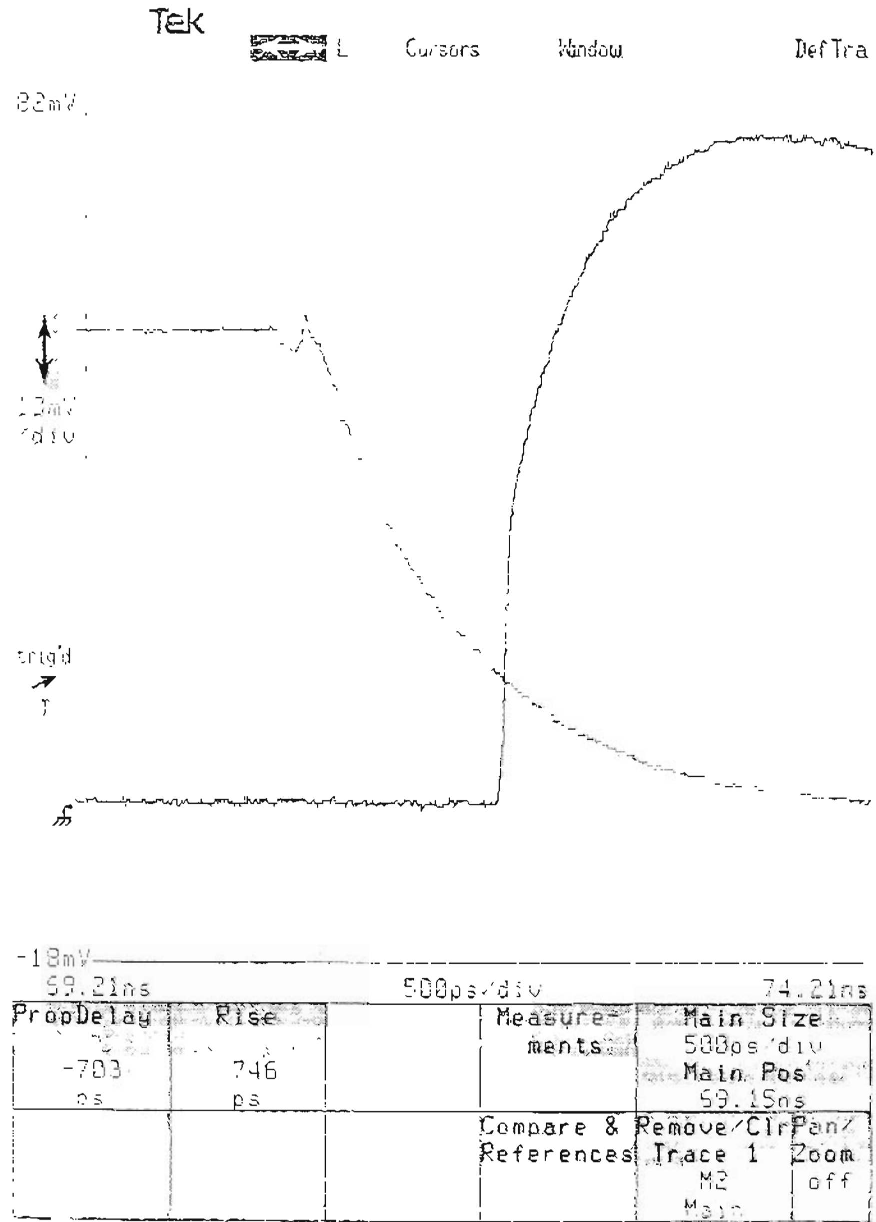


FIGURE 6.3 High speed step signal response of HBT Darlington device for "turn-off" case

6.3.0 Voltage Transfer Characteristics of the Device

Voltage Transfer Characteristics (VTC) is one of the principal properties of interest for any digital circuit, which relates the output voltage to the input voltage under static (or steady-state or low-frequency) conditions. Through VTC curve many important parameters, such as noise margin, logic swing can be determined.The purposes to discuss VTC here are: (a) to see if this device can serve the function of switching, and if yes, (b) where is the proper switching operating point.

Looking at the circuit shown in Fig. 6.4, the device inside the dashed block is so-called HBT Darlington feedback amplifier. Based on the known model parameters, assume $R_f = 260\Omega$, $R_1 = 1300\Omega$, $R_2 = 400\Omega$, $R_3 = 13\Omega$. Two external resistive elements are added to the input and output. They are $R_g = 50\Omega$ representing the source resistance, and $R_C = 1k\Omega$ as the load resistance. V_{CC} is assumed to be $5V$, providing a similar bias condition as the practical test case.

Nodal analysis is implemented to determine the VTC under certain conditions. Detailed derivation procedures are referred to Appendix C. The calculated VTC curve is drawn in Fig. 6.5(a), in which this curve is comprised of four regions, representing different operating states of the device. Region I starts from $V_i = 0$ through the first breakpoint (BP1). Obviously this region accounts for the turn-off state of the device. In this region, the output is pulled down by the input through the feedback loop. Region II indicates that the first stage of the device is turned-on but the second-stage is still off. In this region, despite the significant increase of I_{C1}, the output voltage still keeps going up but with a reduced rate. This is because the current in the feedback loop is decreasing quickly due to the reduction of V_{bc}. At BP2 the second stage starts conducting. At this point since I_f keeps going down, the second-stage collector current I_{C2}, combined with I_{C1}, begins dominating I_C, the total collector current. Therefore, the output voltage drops off rapidly with the drastically increased I_C until BP3, where the first-transistor was saturated, which

means that V_{ce1} can be considered as a constant. On the other hand, since V_{be2} drops down with V_o, Q_2 is basically off. In the equivalent circuit shown in Fig. C.1 of Appendix C, Q_1 is considered as an equivalent voltage source V_{eq} in series with a resistor R_{eq}, where V_{eq} is assumed as the sum of $V_{ce1}(sat)$ and the voltage drop on R_2, and R_{eq} mainly accounts for the emitter and collector resistances. Then the output will linearly increase with the input again at a gentle rate.

From Fig. 6.5(a), it can be clearly seen that region III is suitable for switching operations, with the logic swing of about $1V$, and the transition width $0.5V$, but it brings about a negative high noise margin (NM_H) since the high turn-on voltage requirement for two stage device, which is unapplicable for practical logic circuits. In our switching measurements, the self-biased base dc voltage is located right in the middle of region III, where both transistors are operating in forward-active region. Therefore no cut-off or saturate delay time is accounted for here.

The device operating states for each stage and at each region are listed in Table 6.1. In the VTC analysis, the saturation current I_s of HBTs is assumed to be $10^{-23}A$, $V_{be}(on) = 1.15V$, and $V_{be}(sat) = 1.35V$ for both stages.

The Spice simulation result is shown in Fig. 6.5(b) as a comparison, where the transistor model parameters are referred to the previously obtained HBT Darlington-pair model, listed in Table 5.2. Other parameters and operation conditions are totally same as these used in hand-calculations.

TABLE 6.1. Device Operating States for each stage and region on VTC curve

Region	I	II	III	IV
Operating State	Both Off	Q_1 On Q_2 Off	Q_1 On Q_2 On	Q_1 Saturated Q_2 Off

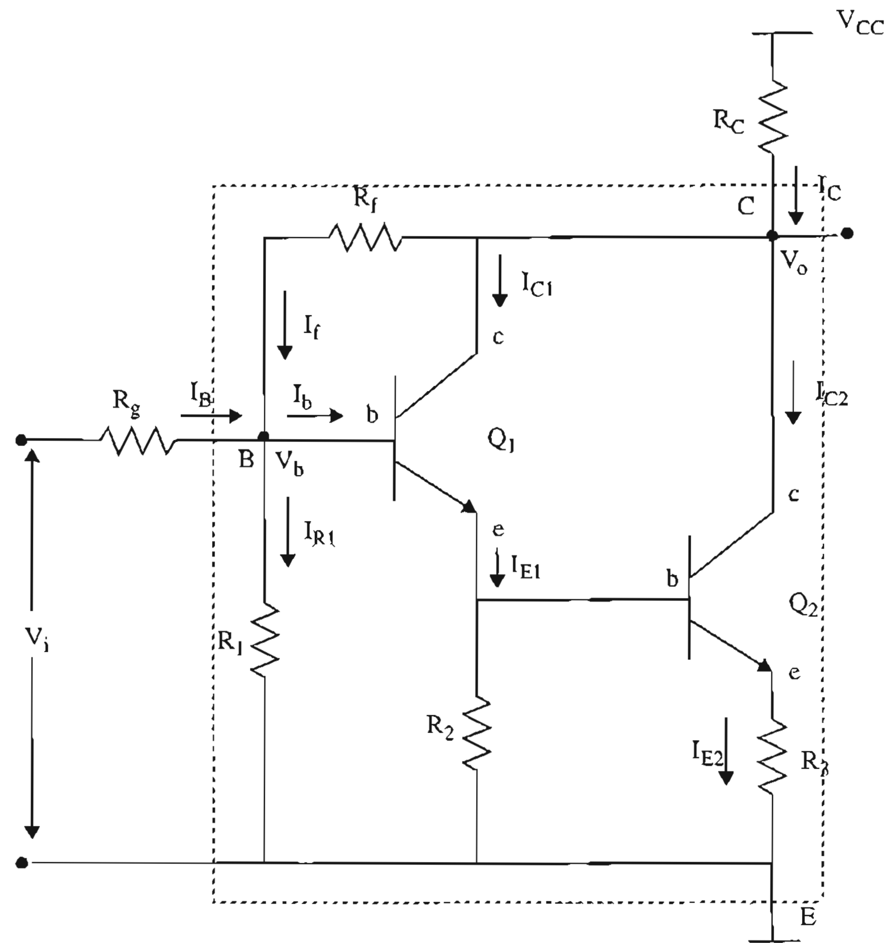
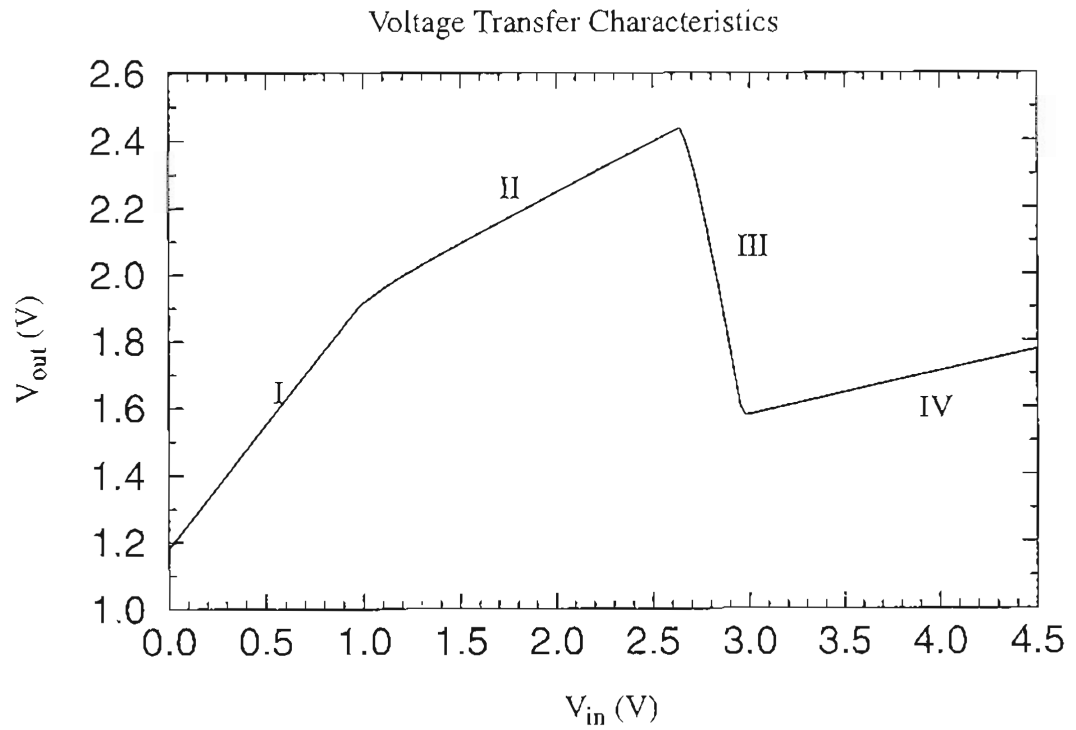
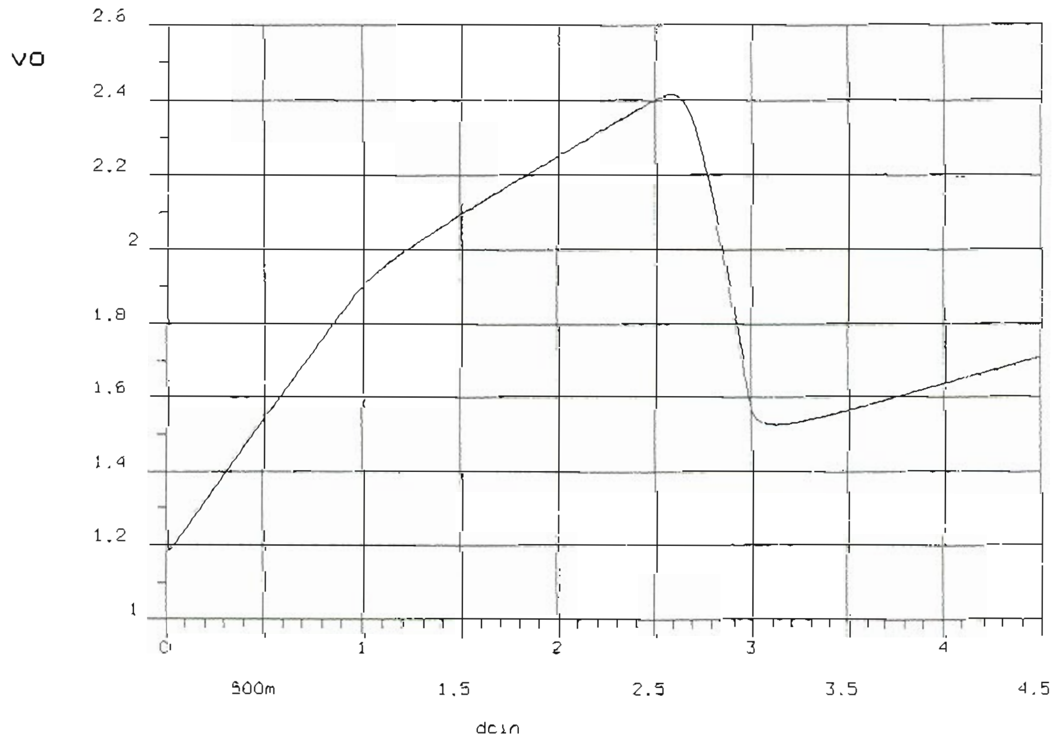


FIGURE 6.4 Network for voltage transfer characteristics analysis



(a)



(b)

FIGURE 6.5 Voltage transfer characteristics analysis and simulation results. (a) Hand-calculation result; (b) Spice simulation result.

6.4.0 Switching Analysis

6.4.1 Simplified Small-Signal Switching Circuit Model

Charge-control model is an effective method in transient analysis. It is difficult here, however, to find some required parameters for charge-control method, such as the change of excess minority carrier charge ΔQ_B and average base current $\overline{I_B}$ of each stage, due to the complexity of the device configuration. A simple method for switching analysis presented here is under the small-signal assumption and quasi-linear approximation. This assumption allows the application of hybrid-π model and the separation of the whole network into input and output loops such that the circuit complexity is reduced.

For the two-stage circuit shown in Fig. 5.1(a) the equivalent circuit is simplified into a one-stage small-signal transistor model plus the feedback loop as shown in Fig. 6.6, where the subscript "eq" denotes the equivalent element that can be lumped or derived from the complex network model.

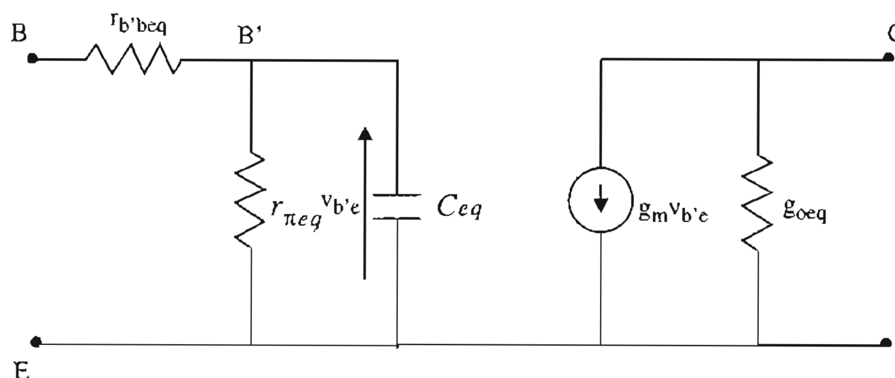


FIGURE 6.6 Simplified HBT equivalent circuit model

With this simplification the entire network under investigation can be drawn as Fig. 6.7, where the input dc block and the output bias-Tee are also included.

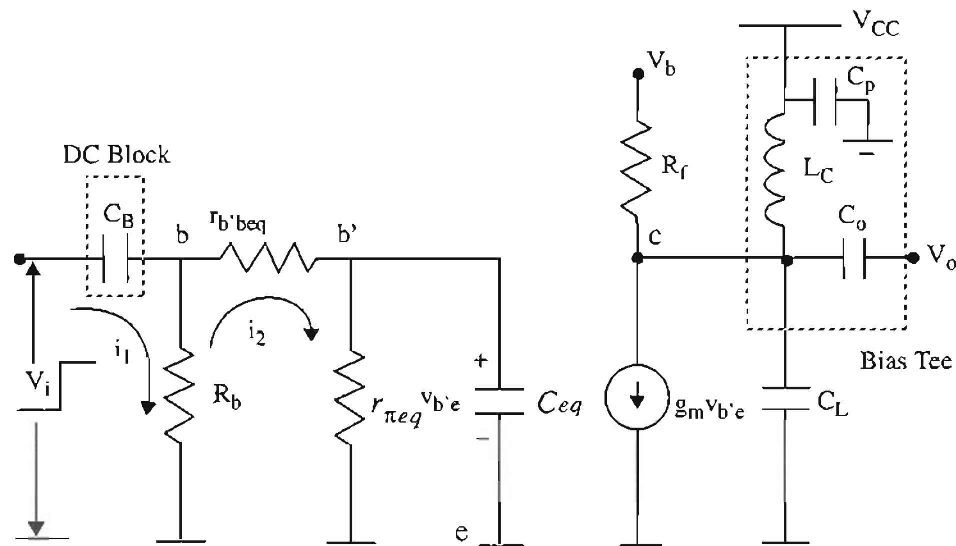


FIGURE 6.7 Measurement equivalent network

6.4.2 Charge Conservation Method

(a) *Without Considering Base Resistance.* Now first look at the input part in Fig. 6.7 without considering the base resistance $r_{bb'eq}$. C_B is the input dc block capacitance, which isolates the DUT from the measurement systems. C_{eq} is the total equivalent capacitance seen from the base terminal. The base-collector capacitance C_{bc} usually needed in high frequency model is not drawn here since it can be lumped into C_{eq} and C_L, respectively. R_b is the bias resistance, which can be expressed as

$$R_b = R_1 \| R_f \tag{6.3}$$

where the impact of the output on the input impedance through the feedback loop is not considered since the switching is a very short instant. The equivalent differential resistance $r_{\pi eq}$ is often negligible in high frequency case. The input signal is a step voltage and can be expressed as $V_i(t) = \Delta V_b U(t)$. The circuit equations can be written as follows by following Kirchoff voltage law (KVL):

$$\left(R_b + \frac{1}{sC_B}\right) i_1 - R_b i_2 = \frac{\Delta V_b}{s} \tag{6.4}$$

$$-R_b i_1 + \left(R_b + \frac{1}{sC_{eq}}\right) i_2 = 0 \tag{6.5}$$

where i_1 and i_2 are the incremental currents in input loop1 and loop2, respectively, caused by the switching as shown in Fig. 6.7. From (6.5), we have:

$$i_1 = \left(1 + \frac{1}{sR_b C_{eq}}\right) i_2 \tag{6.6}$$

Substituting (6.6) into (6.4), and solve for i_1 and i_2

$$i_1 = \frac{\Delta V_b C_B C_{eq}}{C_B + C_{eq}} + \frac{\Delta V_b C_B^2}{R_b (C_B + C_{eq})^2} \frac{1}{s + \frac{1}{R_b (C_B + C_{eq})}} \tag{6.7}$$

$$i_2 = \frac{\Delta V_b C_B C_{eq}}{C_B + C_{eq}} - \frac{\Delta V_b C_B C_{eq}}{R_b (C_B + C_{eq})^2} \frac{1}{s + \frac{1}{R_b (C_B + C_{eq})}} \tag{6.8}$$

Take *Inverse Laplace Transformations* of (6.7) and (6.8), and we get the currents expressed in time domain.

$$i_1(t) = \frac{\Delta V_b C_B C_{eq}}{C_B + C_{eq}} \delta(t) + \frac{\Delta V_b C_B^2}{R_b (C_B + C_{eq})^2} e^{-\frac{t}{R_b (C_B + C_{eq})}} \tag{6.9}$$

$$i_2(t) = \frac{\Delta V_b C_B C_{eq}}{C_B + C_{eq}} \delta(t) - \frac{\Delta V_b C_B C_{eq}}{R_b (C_B + C_{eq})^2} e^{-\frac{t}{R_b (C_B + C_{eq})}} \tag{6.10}$$

What we are concern about here is $i_2(t)$. The first term of $i_2(t)$ in (6.10) indicates the fact that an instantaneous current pulse in a δ-function form was injected into the base at $t = 0$, responding to the triggered input signal. The second term is much smaller in amplitude and is a slowly changed term since $C_B \gg C_{eq}$, representing the slowly discharging process of the dc block capacitance. We needn't consider this term here.

Now the intrinsic basic-emitter ac voltage $v_{b'e}$ can be expressed as:

$$\begin{aligned} v_{b'e} &= \frac{1}{C_{eq}} \int_0^t i_2(t)\, dt = \frac{1}{C_{eq}} \int_0^t \frac{\Delta V_b C_B C_{eq}}{C_B + C_{eq}} \delta(t)\, dt \\ &= \frac{\Delta V_b C_B}{(C_B + C_{eq})} \approx \Delta V_b \end{aligned} \tag{6.11}$$

This is an expected result because $r_{b'b}$ and $r_{\pi eq}$ are not considered here. The collector ac current i_c is a constant in this short instant until the capacitance starts discharging.

$$i_c = g_m v_{b'e} \approx g_m \Delta V_b \tag{6.12}$$

The total charge transferred into the collector in the instant t_d is:

$$\Delta Q_{i_c} = i_c \cdot t_d = g_m \Delta V_b t_d \tag{6.13}$$

where t_d means delay time. Applying the charge conservation law to the output node, we have

$$\Delta Q_{i_c} + \Delta Q_L + \Delta Q_{R_f} + \Delta Q_{C_L} = 0 \tag{6.14}$$

where

$$\Delta Q_{C_L} = C_L \Delta V_o \tag{6.15}$$

$$\Delta Q_{R_f} = \frac{\Delta V_o - \Delta V_b}{2R_f} t_d \tag{6.16}$$

As for ΔQ_L, we have several ways to simulate the time dependence of the self-inductive electrodynamic potential in the inductor L_C during the switching. First one is called *linear approximation*, which is the simplest model but leads to an acceptable result.

In *linear approximation*, the self-inductive electrodynamic potential versus time is assumed linearly changed:

$$\Delta V(t) = \frac{\Delta V_o t}{t_d} \tag{6.17}$$

Therefore,

$$-L_C \frac{di_L}{dt} = \frac{\Delta V_o t}{t_d} \tag{6.18}$$

where ΔV_o is the total output voltage change during the delay time t_d.

$$i_L = -\int \frac{\Delta V_o}{L_C t_d} t dt = -\frac{\Delta V_o}{2L_C t_d} t^2 + C \tag{6.19}$$

From the initial condition $i|_{t=0} = 0$, we have $C = 0$, hence

$$i_L(t) = -\frac{\Delta V_o}{2L_C t_d} t^2 \tag{6.20}$$

$$\Delta Q_L = \int_0^{t_d} i_L(t) dt = -\int_0^{t_d} \frac{\Delta V_o}{2L_C t_d} t^2 dt = -\frac{\Delta V_o}{6L_C} t_d^2 \tag{6.21}$$

Inserting (6.13), (6.15), (6.16), and (6.21) into (6.14), the complete equation with respect to delay time t_d is

$$-\frac{\Delta V_o}{6L_C}t_d^2 + \left(g_m \Delta V_b + \frac{\Delta V_o - \Delta V_b}{2R_f}\right)t_d + C_L \Delta V_o = 0 \quad (6.22)$$

It can be further solved as follows

$$t_d = -\frac{3L_C}{A_v}\left[-g_m - \frac{A_v - 1}{2R_f} + \sqrt{\left(g_m + \frac{A_v - 1}{2R_f}\right)^2 + \frac{2A_v^2 C_L}{3L_C}}\right] \quad (6.23)$$

where $A_v = \Delta V_o / \Delta V_b$ is the voltage gain of the network. It is interesting to look at this formula at two limit conditions. First, when the second term under the square root is much greater than the first term, the delay time can be approximately expressed as

$$t_{dl} \approx \sqrt{6L_C C_L} \approx 2.5\tau_{LC} \quad (6.24)$$

where t_{dl} denotes the long delay limit and $t_{LC} \equiv \sqrt{L_C C_L}$. (6.23) provides a simple way to estimate the delay when the load parasitics limit the speed. Secondly, considering the case when the second term is much smaller than the first term, the delay time is given by

$$t_{ds} \approx \frac{A_v C_L}{g_m + \frac{A_v - 1}{2R_f}} \quad (6.25)$$

where t_{ds} denotes the short delay limit. Note that in this expression, the delay time is independant of L_C, which means that L_C is no more as sensitive to the delay as is C_L at this point. It must also be pointed out that the results obtained so far are all based on the assumption of ignoring the base resistance impact. As the delay represented by (6.25) further decreases with C_L, the intrinsic time constant τ_{in} has to be taken into account as it can be seen later. The feedback resistance always plays as a speed-degrading element but at the former limit condition, its impact can be ignored.

The second way to simulate ΔQ_L is called *exponential approximation*, in which

$$\Delta V(t) = \Delta V_o\left(1 - e^{-\frac{t}{t_d/n}}\right) \tag{6.26}$$

where n is a correction factor that can be adjusted to make this equation best matching the actual curve. Under this approximation and going through the same procedures as (6.18)-(6.21), we have

$$\Delta Q_L = -\frac{\Delta V_o}{L_C}t_d^2\left[\frac{1}{2} - \frac{1}{n} + \frac{1}{n^2}(1 - e^{-n})\right] \tag{6.27}$$

In the present case, it is sufficiently accurate to let n be 4, then

$$\Delta Q_L \approx -\frac{5\Delta V_o}{16L_C}t_d^2 \tag{6.28}$$

Replacing the first term of (6.22) with (6.28) and implementing the same limit condition analyses, one can get a series of parallel results as follows

$$t_d = -\frac{8L_C}{5A_v}\left[-g_m - \frac{A_v - 1}{2R_f} + \sqrt{\left(g_m + \frac{A_v - 1}{2R_f}\right)^2 + \frac{5A_v^2C_L}{4L_C}}\right] \tag{6.29}$$

$$t_{dl} \approx 1.79\sqrt{L_CC_L} \tag{6.30}$$

$$t_{ds} \approx \frac{A_vC_L}{g_m + \frac{A_v - 1}{2R_f}} \tag{6.31}$$

Another approximation approach is referred to *sinusoidal approximation*, in which

$$\Delta V(t) = \Delta V_o \sin\frac{\pi t}{2t_d} \tag{6.32}$$

In this case, we have

$$\Delta Q_L = -\frac{2}{\pi}\left(1 - \frac{2}{\pi}\right)\frac{\Delta V_o}{L_C}t_d^2 \approx -\frac{0.23\Delta V_o}{L_C}t_d^2 \tag{6.33}$$

$$t_d = -\frac{2.18L_C}{A_v}\left[-g_m - \frac{A_v - 1}{2R_f} + \sqrt{\left(g_m + \frac{A_v - 1}{2R_f}\right)^2 + \frac{A_v^2 C_L}{1.09L_C}}\right] \quad (6.34)$$

$$t_{dl} \approx 2.15\sqrt{L_C C_L} \quad (6.35)$$

$$t_{ds} \approx \frac{A_v C_L}{g_m + \frac{A_v - 1}{2R_f}} \quad (6.36)$$

Note that same t_{ds} expression was resulted from these three approximation methods. It can also be seen later that the second method has resulted in a best agreement with the nodal analysis results.

We assume here $L = 100 - 400nH$, which is equivalent to a $300 - 1200\Omega$ resistor at the frequency of 500 MHz, the highest harmonic frequency component corresponding to the rise time observed in the measurements. C_L is chosen between 1 and $6ps$, which includes all the parasitics existing in the output signal line. g_m is referred to the single-stage modeled value listed in Appendix A, where it equals about $0.063S$. Here it is assumed to be $0.03S$ since the model in Appendix A is an emitter degradation-type common emitter configuration (see section 6.5 for detail). In the "turn-on" case, $\Delta V_b = 50mV$ after $14dB$ attenuation. $\Delta V_o = -0.45V$ accounts for the device output. In the case of "turn-off", $\Delta V_b = -50mV$, and $\Delta V_o = 0.40V$ were observed from the measurements. Using *exponential approximation* and inserting these parameters into (6.29), a set of time delay values are readily obtained as listed in Table 6.2:

TABLE 6.2. Calculated fall and rise time at certain LC time constant with charge conservation method

	$L_C = 400nH$ $C_L = 1.5pF$	$L_C = 300nH$ $C_L = 2pF$	$L_C = 200nH$ $C_L = 3pF$	$L_C = 100nH$ $C_L = 6pF$
$t_{df}(ns)$	0.815	0.924	1.05	1.21
$t_{dr}(ns)$	0.702	0.819	0.968	1.15

where t_{df} and t_{dr} are defined as fall time delay and rise time delay, respectively. It should be noted that the fall and rise times defined here are different from the customary definition where they represent the time taken between the 10 - 90% points of the output waveforms. From this set of results, one can see a good agreement achieved with the experimental data when $L_C = 300nH$, and $C_L = 2pF$.

(b) *Considering Base Resistance*. Now consider the influence of base resistance $r_{bb'}$. Solve the circuit equation (6.4) combined with

$$-R_b i_1 + (R_b + r_{bb'} + \frac{1}{sC_{eq}})\, i_2 = 0 \tag{6.37}$$

It turns out

$$i_2 \approx \frac{\Delta V_b}{r_{bb'}} e^{-\frac{t}{r_{bb'}C_{eq}}} \tag{6.38}$$

under the approximation of $C_{eq} \ll C_B$ and $r_{bb'} \sim R_b$. In this case,

$$v_{b'e} = \Delta V_b \left(1 - e^{-\frac{t}{\tau_{in}}}\right) \tag{6.39}$$

where the intrinsic time constant τ_{in} is defined as $r_{bb'}C_{eq}$, hence

$$i_c(t) = g_m v_{b'e} = g_m \Delta V_b \left(1 - e^{-\frac{t}{\tau_{in}}}\right) \tag{6.40}$$

$$\overline{i_c} = \frac{1}{t_d}\int i_c dt = g_m \Delta V_b \left[1 + \frac{\tau_{in}}{t_d}\left(e^{-\frac{t_d}{\tau_{in}}} - 1\right)\right] \tag{6.41}$$

$$\Delta Q_{i_c} = \overline{i_c} \cdot t_d = g_m \Delta V_b \left[t_d + \tau_{in}\left(e^{-\frac{t_d}{\tau_{in}}} - 1\right)\right] \tag{6.42}$$

If we assume $t_d \gg \tau_{in}$, which is true in our case, again obtained is the same result: as before

$$\Delta Q_{i_c} = g_m \Delta V_b t_d \tag{6.43}$$

which means that the influence of base resistance is negligible here. In most of practical situations, in fact, the delay caused by intrinsic parasitics is much smaller compared to that by extrinsic elements.

6.4.3 Nodal Analysis Method

A further nodal analysis at the output node derives out the output waveforms in the time sequence. Fig. 6.8 shows the ac output equivalent circuit, where

$$i_c(t) = g_m \Delta V_b \left(1 - e^{-\frac{t}{\tau_{in}}}\right) \tag{6.44}$$

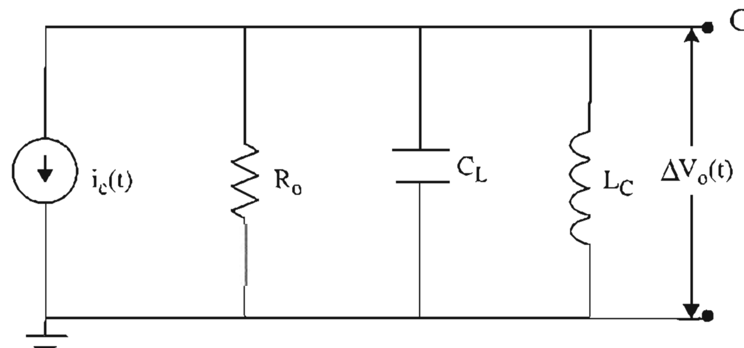


FIGURE 6.8 Equivalent circuit of ac output loop

In frequency domain,

$$\begin{aligned} i_c(s) &= g_m \Delta V_b \left(\frac{1}{s} - \frac{1}{s + \frac{1}{\tau_{in}}} \right) \\ &= g_m \Delta V_b \frac{1}{\tau_{in} s \left(s + \frac{1}{\tau_{in}}\right)} \end{aligned} \quad (6.45)$$

Therefore,

$$\begin{aligned} \Delta V_o &= -\frac{i_c}{\frac{1}{R_o} + sC_L + \frac{1}{sL_C}} \\ &= -\frac{g_m \Delta V_b}{\tau s \left(s + \frac{1}{\tau_{in}}\right)\left(\frac{1}{R_o} + sC_L + \frac{1}{sL_C}\right)} \\ &= -\frac{g_m \Delta V_b}{\tau_{in} C_L} \frac{1}{\left(s + \frac{1}{\tau_{in}}\right)\left(s^2 + \frac{s}{\tau_{RC}} + \frac{1}{\tau_{LC}^2}\right)} \end{aligned} \quad (6.46)$$

where $\tau_{RC} \equiv R_o C_L$, $\tau_{LC} \equiv \sqrt{L_C C_L}$. (6.46) can be dissected into

$$\begin{aligned} \Delta V_o(s) = -\frac{g_m \Delta V_b}{\tau_{in} C_L} \Bigg\{ & \frac{1}{\frac{1}{\tau_{in}^2} + \frac{1}{\tau_{RC}\tau} + \frac{1}{\tau_{LC}^2}} \cdot \frac{1}{s + \frac{1}{\tau_{in}}} \\ & + \frac{1}{\frac{\sqrt{\delta}}{\tau_{RC}}\left[\frac{1}{\tau_{in}} - \frac{1}{2\tau_{RC}}(1 - \sqrt{\delta})\right]} \cdot \frac{1}{s + \frac{1}{2\tau_{RC}}(1 - \sqrt{\delta})} \\ & - \frac{1}{\frac{\sqrt{\delta}}{\tau_{RC}}\left[\frac{1}{\tau_{in}} - \frac{1}{2\tau_{RC}}(1 + \sqrt{\delta})\right]} \cdot \frac{1}{s + \frac{1}{2\tau_{RC}}(1 + \sqrt{\delta})} \Bigg\} \end{aligned} \quad (6.47)$$

where $\delta = 1 - 4\tau_{RC}^2/\tau_{LC}^2 = 1 - 4R_o^2 C_L/L_C$.

Perform *Inverse Laplace Transformation* of (6.33)

$$\Delta V_o(t) = -\frac{g_m \Delta V_b}{\tau_{in} C_L}\left\{\frac{1}{\frac{1}{\tau_{in}^2} - \frac{1}{\tau_{RC}\tau_{in}} + \frac{1}{\tau_{LC}^2}} e^{-\frac{t}{\tau_{in}}} + \frac{1}{\frac{\sqrt{\delta}}{\tau_{RC}}\left[\frac{1}{\tau_{in}} - \frac{1}{2\tau_{RC}}(1-\sqrt{\delta})\right]} e^{-\frac{(1-\sqrt{\delta})}{2\tau_{RC}}t} - \frac{1}{\frac{\sqrt{\delta}}{\tau_{RC}}\left[\frac{1}{\tau_{in}} - \frac{1}{2\tau_{RC}}(1+\sqrt{\delta})\right]} e^{-\frac{(1+\sqrt{\delta})}{2\tau_{RC}}t}\right\} \quad (6.48)$$

Consider the case $\tau_{in} \ll \tau_{RC}, \tau_{LC}$, which is true here.

$$\Delta V_o(t) \approx -\frac{g_m \Delta V_b}{\tau_{in} C_L}\left[\tau_{in}^2 e^{-\frac{t}{\tau_{in}}} + \frac{\tau_{in}\tau_{RC}}{\sqrt{\delta}} e^{-\frac{(1-\sqrt{\delta})}{2\tau_{RC}}t} - \frac{\tau_{in}\tau_{RC}}{\sqrt{\delta}} e^{-\frac{(1+\sqrt{\delta})}{2\tau_{RC}}t}\right] \quad (6.49)$$

As $\delta < 0$, we have

$$\begin{aligned}\Delta V_o(t) &= -\frac{g_m \Delta V_b}{\tau_{in} C_L}\left[\tau_{in}^2 e^{-\frac{t}{\tau_{in}}} + \frac{\tau_{in}\tau_{RC}}{i\sqrt{|\delta|}} e^{-\frac{t}{2\tau_{RC}}}\left(e^{\frac{i\sqrt{|\delta|}}{2\tau_{RC}}t} - e^{-\frac{i\sqrt{|\delta|}}{2\tau_{RC}}t}\right)\right] \\ &= -\frac{2 g_m \Delta V_b \tau_{RC}}{\sqrt{|\delta|}\, C_L}\left(\frac{\sqrt{|\delta|}\,\tau_{in}}{2\tau_{RC}} e^{-\frac{t}{\tau_{in}}} + e^{-\frac{t}{2\tau_{RC}}} \sin\frac{\sqrt{|\delta|}}{2\tau_{RC}} t\right)\end{aligned} \quad (6.50)$$

As $t \sim \tau_{in} \ll \tau_{RC}$, $\Delta V_o(t)$ will approximately follow

$$\Delta V_o(t) \approx -\frac{g_m \Delta V_b}{C_L}\left(\tau_{in} + \frac{t^2}{2\tau_{in}}\right) \quad (6.51)$$

Since $\tau_{in} \ll \tau_{RC}$, the first term in the parenthesis of last equation in (6.50) can be neglected as $t \gg \tau_{in}$ such that

$$\Delta V_o(t) = -\frac{2g_m \Delta V_b \tau_{RC}}{\sqrt{|\delta|}C_L} e^{-\frac{t}{2\tau_{RC}}} \sin\frac{\sqrt{|\delta|}}{2\tau_{RC}} t \qquad t \gg \tau_{in} \tag{6.52}$$

As $\tau_{in} \ll t \ll \tau_{RC}$, $\Delta V_o(t)$ is basically linear:

$$\Delta V_o(t) \approx -\frac{g_m \Delta V_b}{C_L} t \tag{6.53}$$

Both (6.51) and (6.53)show an independence of L_C.

In the long delay limit case, which means C_L relatively large, we have $4R_o^2 C_L / L_C \gg 1$ such that $\sqrt{|\delta|} \approx 2R_o\sqrt{C_L/L_C}$, hence

$$\Delta V_o(t) \approx -g_m \Delta V_b \sqrt{\frac{L_C}{C_L}} e^{-\frac{t}{2\tau_{RC}}} \sin\frac{t}{\tau_{LC}} \tag{6.54}$$

From (6.54), t_{dl} can be estimated as $\frac{\pi}{2}\tau_{LC} \approx 1.57\sqrt{L_C C_L}$. It can be seen that this result is fairly close to that in (6.30), which was obtained by *exponential approximation* in the charge conservation method.

As $\delta \geq 0$, (6.49) becomes

$$\Delta V_o(t) \approx -\frac{2g_m \Delta V_b \tau_{RC}}{\sqrt{\delta}C_L} \left(\frac{\sqrt{\delta}\tau_{in}}{2\tau_{RC}} e^{-\frac{t}{\tau_{in}}} + e^{-\frac{t}{2\tau_{RC}}} \sinh\frac{\sqrt{\delta}}{2\tau_{RC}} t \right) \tag{6.55}$$

Fig. 6.9 plots the output waveforms calculated from (6.50) and (6.55) for "turn-off" case, where $g_m = 0.03S$, $\Delta V_b = 50mV$, $R_o \approx (R_f + R_s) = 310\Omega$, where $R_s = 50\Omega$ is the source resistance. The values for L_C and C_L are changed by keeping the time constant $\tau_{LC} = \sqrt{L_C C_L}$ invariant. It can be seen from Fig. 6.9 that in this case, a smaller C_L will improve the speed and increase the gain considerably.

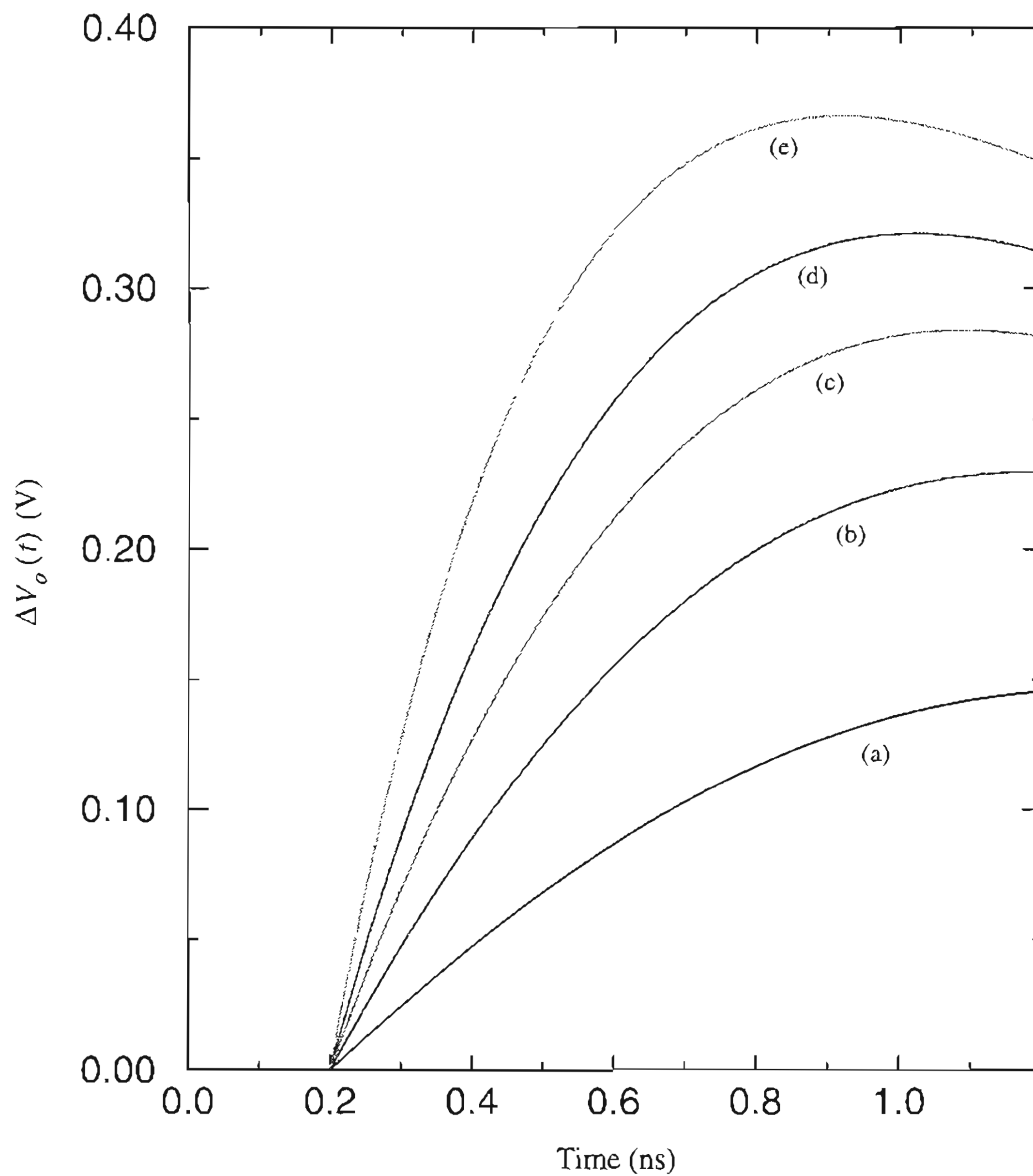


FIGURE 6.9 Calculated switching waveforms for "turn-off" case. (a) L_C=100nH, C_L=6pF; (b) L_C=200nH, C_L=3pF; (c) L_C=300nH, C_L=2pF; (d) L_C=400nH, C_L=1.5pF; (e) L_C=600nH, C_L=1.0pF.

6.4.4 Charge-Control Method

In the case of large signal, R_b can be replaced by a Thévenin equivalent resistor $R_{b'}$, which is approximately equal to R_b in this case, connected in series in the base loop. The average current $\overline{i_b}$ can be found simply as

$$\overline{i_b} = \frac{\Delta V_b}{2\,(R_{b'} + r_{bb'})} \tag{6.56}$$

Then the transient collector current can be found by solving the charge-control equation (see Fig. 3.4a)

$$\overline{i_b} = \frac{\Delta Q_B}{\tau_n} + \frac{d}{dt}(\Delta Q_B) \tag{6.57}$$

where τ_n is the minority lifetime in the base, and ΔQ_B is the excess minority carrier charge change during the switching, which turns out

$$i_c = \beta \overline{i_b}\left(1 - e^{-\frac{t}{\tau_n}}\right) \tag{6.58}$$

This leads to an expression of ΔQ_{i_c} similar to (6.13)

$$\Delta Q_{i_c} = \beta \overline{i_b} t_d \tag{6.59}$$

as $t_d \gg \tau_n$. Taking it into (6.14) and solving for t_d, we get a similar expression to (6.29)

$$t_d = -\frac{8L_C}{5A_v}\left[-\frac{\beta \overline{i_b}}{\Delta V_b} - \frac{A_v - 1}{2R_f} + \sqrt{\left(\frac{\beta \overline{i_b}}{\Delta V_b} + \frac{A_v - 1}{2R_f}\right)^2 + \frac{5A_v^2 C_L}{4L_C}}\right] \tag{6.60}$$

Assume $\beta = 20$ (see Fig. 5.8) and keep other parameters same as before, the fall time t_{df} and rise time t_{dr} at different L_C and C_L combinations can be listed as follows

TABLE 6.3. Calculated fall and rise time at certain LC time constant with charge-control method

	$L_C = 400nH$ $C_L = 1.5pF$	$L_C = 300nH$ $C_L = 2pF$	$L_C = 200nH$ $C_L = 3pF$	$L_C = 100nH$ $C_L = 6pF$
$t_{df}(ns)$	0.610	0.730	0.890	1.10
$t_{dr}(ns)$	0.522	0.639	0.806	1.05

As (6.59) is used in small signal case, it is basically equivalent to (6.29) because g_m can be approximately expressed as $\frac{\beta \bar{i_b}}{\Delta V_b}$ since i_b is a variant during switching. The difference between the results of (6.29) and (6.59) may come from several reasons, such as the measurement error of β and simulation error of g_m. In fact, the assumption $t_d \gg \tau_n$ is not always true, specially in the case of high base doping, which tends to reduce the value of ΔQ_{i_c} and increase the delay. It's worth pointing out that although the data of g_m and β used here came from different sources, one from the simulation model based on the high-frequency measurements, another from the direct dc measurements, they turned out quite consistent results.

6.5.0 Spice Simulation Results

TekSpice transient analysis results (taking the "turn-on" case as an example) obtained by using the single transistor equivalent circuit model are plotted in Fig. 6.10, where the circuit connection and element values are the same as that used in hand-analysis calculation. The transistor model parameters are listed as follows, basically following those listed in Table A.1.

TABLE 6.4. Single stage model transistor parameters

$\beta_F = 50$	$i_s = 10^{-23}A$	$t_F = 4.30ps$	$r_b = 50\Omega$	$r_c = 1.0\Omega$	$r_e = 16\Omega$
$C_{ie} = 0.118p$	$\phi_e = 1.2V$	$m_e = 0.33$	$C_{jc} = 70f$	$\phi_c = 1.2V$	$m_c = 0.50$

Note that $\beta = 50$ used here is the intrinsic current gain of the transistor. Compared to the measured current gain of the Darlington-pair shown in Fig. 5.8, the intrinsic current gain is larger than the measured value since the single-stage transistor model is an emitter degradation-type common-emitter configuration circuit, in which the total network gain is greatly degraded by the emitter feedback resistor. According to the relationship between the degraded transconductance g_m' and the intrinsic conductance g_m

$$g_m' = \frac{g_m}{1 + g_m R_E} \tag{6.61}$$

and the relationship $\beta \propto g_m$, the intrinsic transistor current gain should be enlarged by the same factor as that the total transconductance was degraded. In (6.61), R_E is the emitter resistor.

In Fig. 6.10, three groups of curves are plotted, corresponding to the C_L values of $2pF$, $4pF$ and $6pF$, respectively. Each of them comprises three curves, too, which are obtained by changing L_C from $100nH$ to $300nH$ at each fixed C_L value. One can see that in short time delay case, it is basically C_L that determines the speed and output amplitude. Only at certain delay level, the influence of L_C starts to show up. In this family of curves, it can be seen that the bottom two curves represent the present device behavior best.

Fig. 6.11 is the Spice transient analysis results (still the "turn-on" case) obtained by applying the two-stage equivalent circuit model. The transistor configuration is the Dar-

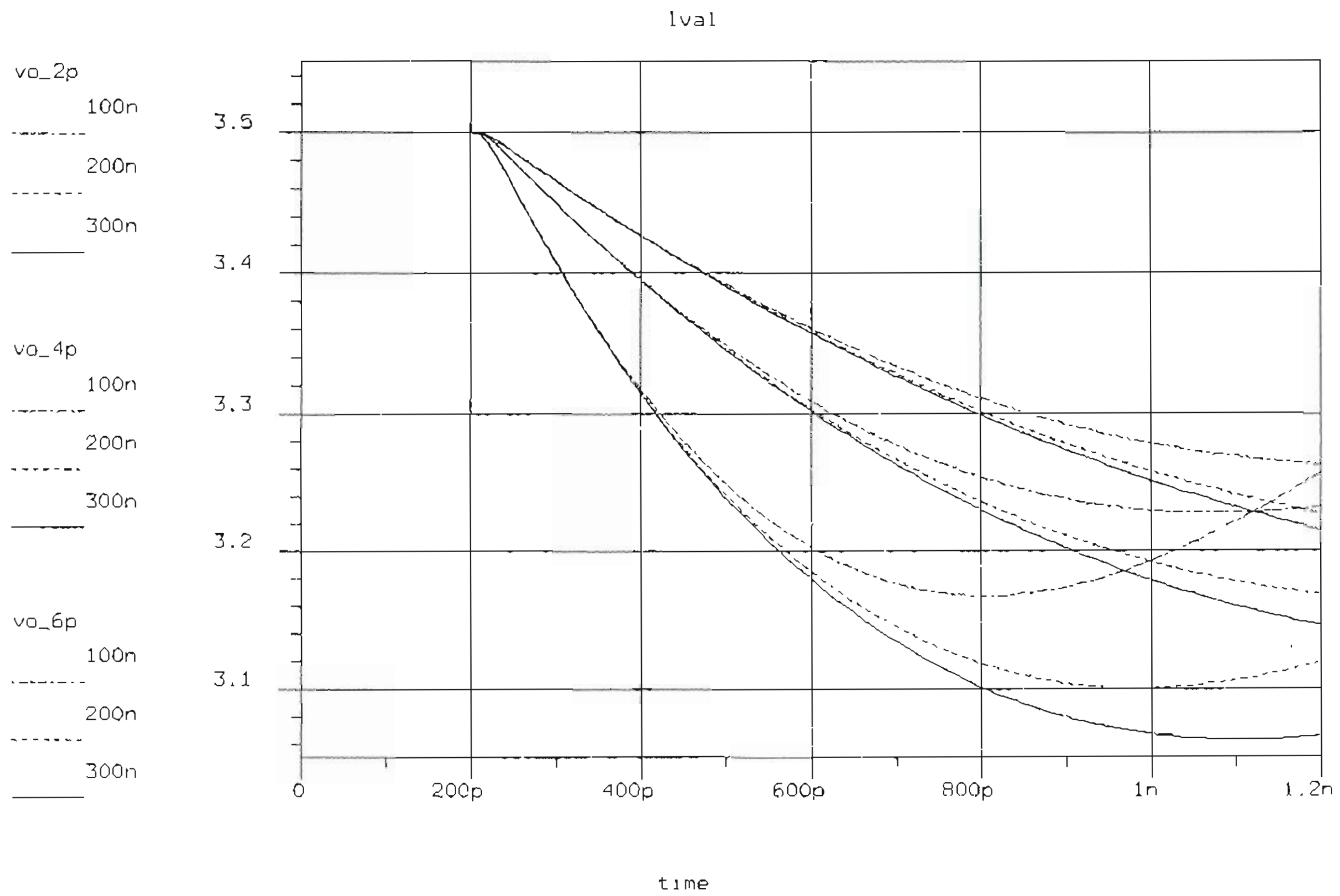


FIGURE 6.10 Spice transient simulation results by using the single-stage model for "turn-on" case

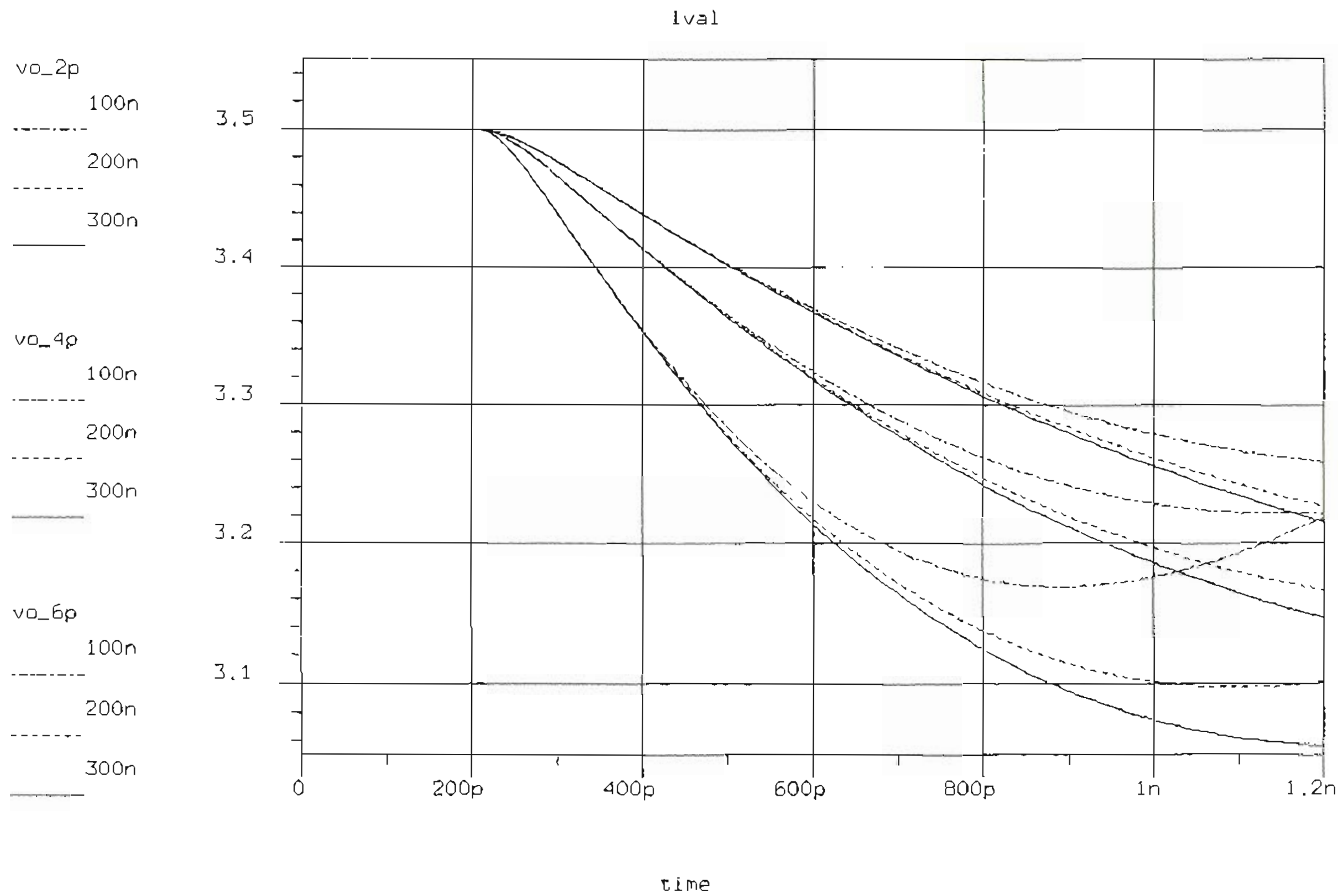


FIGURE 6.11 Spice transient simulation results by using the two-stage model for "turn-on" case

lington feedback amplifier as shown in Fig. 5.1a, and the external circuit connection and element values are same as before. The transistor model parameters are based on those listed in Table 5.2, and listed now as follows:

TABLE 6.5. Two stage model transistor parameters

Q_1:	$\beta_F = 450$	$i_s = 10^{-23}A$	$t_F = 2.30ps$	$r_b = 20\Omega$	$r_c = 1.3\Omega$	$r_e = 50\Omega$
	$C_{je} = 65f$	$\phi_e = 1.2V$	$m_e = 0.33$	$C_{jc} = 50f$	$\phi_c = 1.2V$	$m_c = 0.50$
Q_2:	$\beta_F = 150$	$i_s = 10^{-23}A$	$t_F = 4.30ps$	$r_b = 70\Omega$	$r_c = 2.80\Omega$	$r_e = 13\Omega$
	$C_{je} = 0.117p$	$\phi_e = 1.2V$	$m_e = 0.33$	$C_{jc} = 0.10p$	$\phi_c = 1.2V$	$m_c = 0.50$

In this two-stage model, the explanation for $\beta_{F1} = 450$ and $\beta_{F2} = 150$ follows the same reason as mentioned above. In the first stage, the total R_E is equal to $r_{e1} + R_2 = 450\Omega$. In Fig. 6.11, the similar curves family is produced by using the same sweeping values of L_C and C_L. Comparing Fig. 6.10 and Fig. 6.11 with Fig. 6.9, one can see they are quite consistent in describing the switching behavior of the device presently under investigation.

6.6.0 Discussions

In most practical circumstances it is the load elements limiting the switching speed of the device. Among them load capacitance C_L plays a key role. As seen in present case, combined with the inductance L_C, the time constant τ_{LC} is formed in determining the rise or fall delay rate. With a certain value of τ_{LC}, smaller C_L will improve the speed and achieve higher output voltage. Therefore, minimizing the load capacitance is an important issue in switching circuit design.

It should be noted that besides those extrinsic elements, the only intrinsic parameter involved in (6.29) is the transconductance g_m of the composite transistor. The voltage

gain A_v, which relates to the transfer characteristics of the device, depends on the device configuration, and partly reflects the intrinsic properties, is another important parameter affecting the switching performance. In large signal case, common-emitter dc current gain β takes place of g_m. According to (6.29) and (6.59), a switching device with higher g_m or β suggests a faster speed, which can become another useful criterion of design.

Now consider the case that the external parasitics are minimized to a very low degree such that all the extrinsic time constants are less than the intrinsic time constants, e.g. τ_{in} as defined in (6.39). In this case, the delay time t_d is mainly limited by τ_{in}. A customary way for rise time estimation tells us that it takes about $2.2\tau_{in}$ in a typical inverter circuit for the collector current rising from 10 to 90% point of the current waveform, whatever τ_{in} accounts for. We can get this conclusion for this specific case in another way by expanding the term $exp\,(-t_d/\tau_{in})$ in (6.42) into *Tailor series* up to third term, hence

$$\Delta Q_{ic} \approx g_m \Delta V_b \left(\frac{t_d^2}{2\tau_{in}} - \frac{t_d^3}{6\tau_{in}^2} \right) \tag{6.62}$$

Inserting it in (6.14), it turns out

$$-\frac{g_m \Delta V_b}{6\tau_{in}^2} t_d^3 - \left(\frac{\Delta V_o}{6L_C} - \frac{g_m \Delta V_b}{2\tau_{in}} \right) t_d^2 + \frac{\Delta V_o - \Delta V_b}{2R_f} t_d + C_L \Delta V_o = 0 \tag{6.63}$$

Assuming C_L very small and the feedback loop open, which mean $C_L \to 0$ and $R_f \to \infty$, the last two terms can be neglected, we simply have

$$-\frac{g_m \Delta V_b}{3\tau_{in}^2} t_d = \frac{\Delta V_o}{3L_C} - \frac{g_m \Delta V_b}{\tau_{in}} \tag{6.64}$$

Solve for t_d,

$$t_d = 3\tau_{in} - \frac{A_v \tau_{in}^2}{g_m L_C} \tag{6.65}$$

As $\frac{3g_m L_C}{A_v} \gg \tau_{in}$,

$$t_d \approx 3\tau_{in} \tag{6.66}$$

which is fairly close to $2.2\tau_{in}$ if we use the customary definition for the delay time.

In present case, τ_{in} is defined as $r_{b'b}C_{eq}$, where $r_{b'b}$ is the spread base resistance, and C_{eq} is the equivalent capacitance seen from the base port. In general, C_{eq} can be expressed as $C_\pi + \left|1 - \frac{\Delta V_o}{\Delta V_{b'}}\right| C_c$. C_π is dominated by the diffusion capacitance C_{de}, which characterizes the influence of mobile carriers on currents flowing through the transistor in forward active mode, and can be expressed as $\tau_{ec} g_m$ in small signal condition, where τ_{ec} is forward transit time; C_c is the distributed base-collector junction capacitance, now lumped into base-emitter loop, and $\Delta V_{b'}$ is the intrinsic base-emitter voltage change. It is not difficult to find by a careful comparison that the intrinsic time constant τ_{in} defined here is basically corresponding to the intrinsic part of the propagation delay time D defined in Ashar's paper[19] for voltage drive switching circuit case, which is expressed as

$$R_b [C_d + C_{te} + (1 + R_L/R_e) C_c] \tag{6.67}$$

where R_b is the base resistance, R_e is emitter diode resistance, C_d is diffusion capacitance, C_{te} and C_c are emitter-to-base and collector-to-base transition (junction) capacitances, respectively. As claimed by Ashar, it is $R_b C_d$ (denoted by $r_{b'b}C_\pi$ in our case) rather than $T_e = R_e C_d$ (denoted by τ_{ec} here) that plays a major role in voltage switching since C_c is usually much smaller than C_d there. It is not exactly the case here, however, since typical GaAs-based HBT technology tends to present a comparable base-collector junction capacitance which may dominate the capacitance factor of time constant τ_{in} after lumped into C_{eq}, specially in the case with a large voltage gain. One can see this point by

examining the value of τ_{in} using the data obtained from the previous model. It can be found from Table A.1 in Appendix A that the Darlington composite transistor represented by the single-stage model has $r_{b'b} = 49.3\Omega$, $C_\pi = 0.118pF$ and $C_c = 71.5fF$. Assuming $\Delta V_{b'} \approx \Delta V_b$, C_{eq} can be calculated as

$$C_{eq} = 0.118 + 10 \times 0.0715 = 0.83pF \tag{6.68}$$

Therefore,

$$\tau_{in} = r_{b'b} C_{eq} = 40.9ps \tag{6.69}$$

The shortest delay time determined by the device itself is thus

$$t_d \approx 3\tau_{in} = 123ps \tag{6.70}$$

or with customary definition is about $2.2\tau_{in} = 90ps$.

If only the first stage is under operation, from Table 5.2, we have $r_{b'b1} = 20.4\Omega$, $C_{\pi 1} = 65.1fF$ and $C_{c1} = 48.5fF$, therefore

$$\tau_{in} = 11.2ps \tag{6.71}$$

From this example it can be seen that the base-collector capacitance is actually dominant term in forming the total capacitance factor, and also that the switching speed was degraded a lot by the poor base resistance and base-emitter capacitance characteristics of the second stage.

Modern HBT technology tends to pursue very thin base layer to achieve very short base transit time τ_b under the prerequisite of keeping a relatively low base resistance by making a high base doping, which is the major trade-off of HBT technology. It now seems more important to achieve a low base resistance rather than a thin base layer. Too high base doping, however, will degrade β or g_m of the device. Therefore, a compromise of several factors should be taken into account in switching device design.

6.7.0 Summary

- A small-signal switching analysis of packaged Darlington configuration device was implemented based on the previous model. This new switching analysis technique separates the input loop from the output loop for the purpose of simplifying the charge transfer calculation. The hybrid-π model was for the first time used for switching analysis, and is a good model in realizing the desired simplification. Several different methods were employed for solving the same problem, and turned out quite consistent results which also have good agreements with the experimental data obtained by the TDR measurements and the Spice simulation results.

- The waveform analysis shows that the load capacitance impacts the speed significantly. Small load capacitance is always preferred because it not only improves the speed but also raises the output voltage under certain value of LC time constant.

- In the small-signal switching delay time formula, transconductance g_m is found as the only intrinsic parameter. Voltage gain A_v is a partly intrinsic parameter in the formula. The higher g_m and A_v, the faster speed. Large-signal formula, where β takes place of g_m, can also be used as a small-signal switching formula.

- Assuming that the extrinsic elements can be ignored, the intrinsic time constant τ_{in} becomes the main limitation of the delay time. For GaAs-based HBT devices, it is base-collector capacitance that dominates the capacitance factor in τ_{in}. In present case the shortest delay time is estimated as $3\tau_{in} = 123ps$, equivalent to the customarily defined delay time $2.2\tau_{in} = 90ps$. This value is much larger than that obtained by only considering a one-stage device since the poor base resistance and base-emitter capacitance characteristics of the second stage severely degraded the speed response.

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APPENDIX A

The single-stage hybrid-π equivalent circuit model of HBT Darlington feedback amplifier is shown in Fig. A.1, and the corresponding element values are listed in Table A.1.

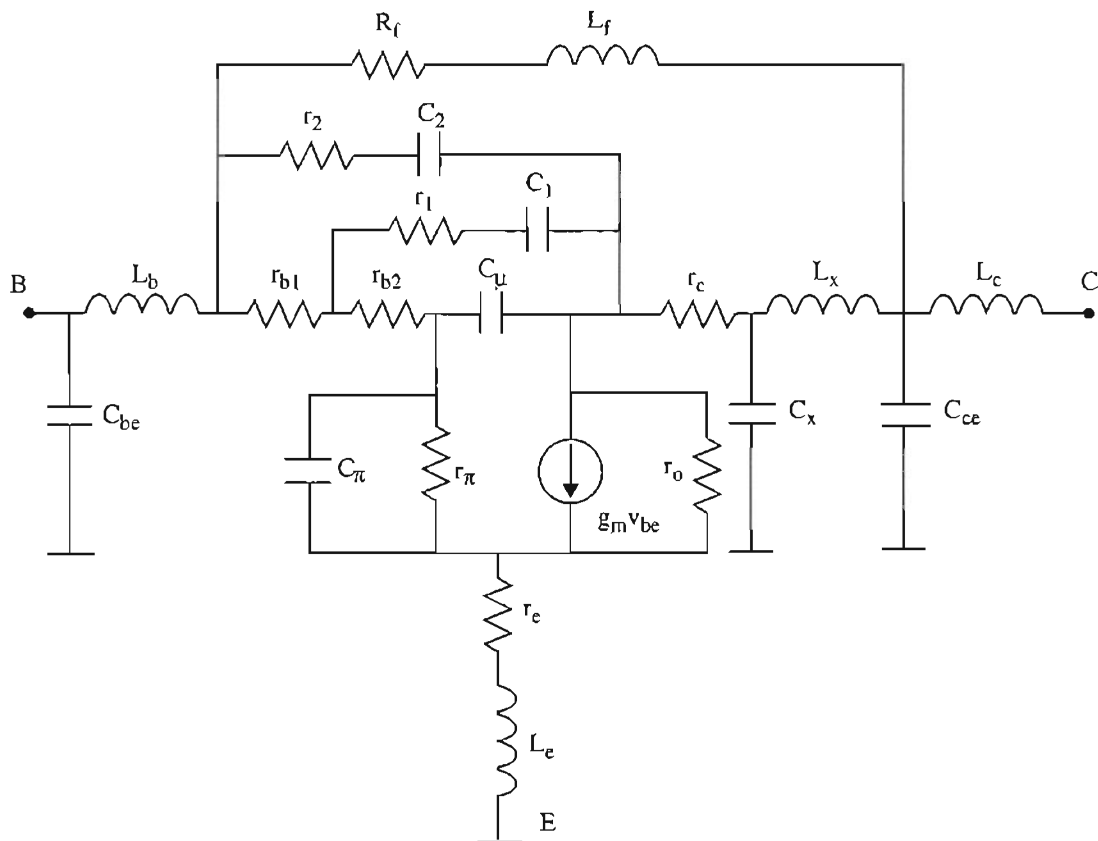

FIGURE A.1 Diagram of single-stage hybrid-π equivalent circuit model for HBT Darlington feedback amplifier

TABLE A.1 Single-stage model element values of HBT Darlington feedback amplifier (obtained from SuperCompact simulation based on the S-parameters measured at V_{CC}=3.5V. Error function = 0.11)

Element	Values	Element	Values
r_{b1}	7.69Ω	C_{μ}	4.02FF
r_{b2}	41.64Ω	C_1	6.26FF
r_{π}	1.69×10^6Ω	C_2	61.17FF
r_o	5.92×10^5Ω	C_{be}	4.35FF
r_e	19.93Ω	C_{ce}	0.143PF
r_c	0.72Ω	C_x	74.5FF
r_1	0.64Ω	L_b	0.069NH
r_2	0.18Ω	L_c	0.021NH
g_m	0.06325S	L_e	0.036NH
R_f	281.53Ω	L_x	0.283NH
C_{π}	0.118PF	L_f	0.083NH

APPENDIX B

Assume a uniform doping density formed in the base, collector, and collector contact layer, respectively, and the collector edge of the depletion region has reached the collector contact layer under sufficient high reverse bias. The depletion charge density ρ, electrical field E, and potential V in these regions can be schematically plotted in Fig. B.1(a), (b), and (c), and expressed as

$$\rho(x) = \begin{cases} -qN_A & -x_p \le x < 0 \\ qN_D & 0 \le x < x_n \\ qN_D^+ & x_n \le x \le x_{nc} \end{cases} \tag{B.1}$$

$$E(x) = \begin{cases} -\dfrac{qN_A}{\varepsilon}(x + x_p) & -x_p \le x < 0 \\ \dfrac{qN_D}{\varepsilon}(x - x_n) - \dfrac{qN_D^+}{\varepsilon}(x_{nc} - x_n) & 0 \le x < x_n \\ \dfrac{qN_D^+}{\varepsilon}(x - x_{nc}) & x_n \le x \le x_{nc} \end{cases} \tag{B.2}$$

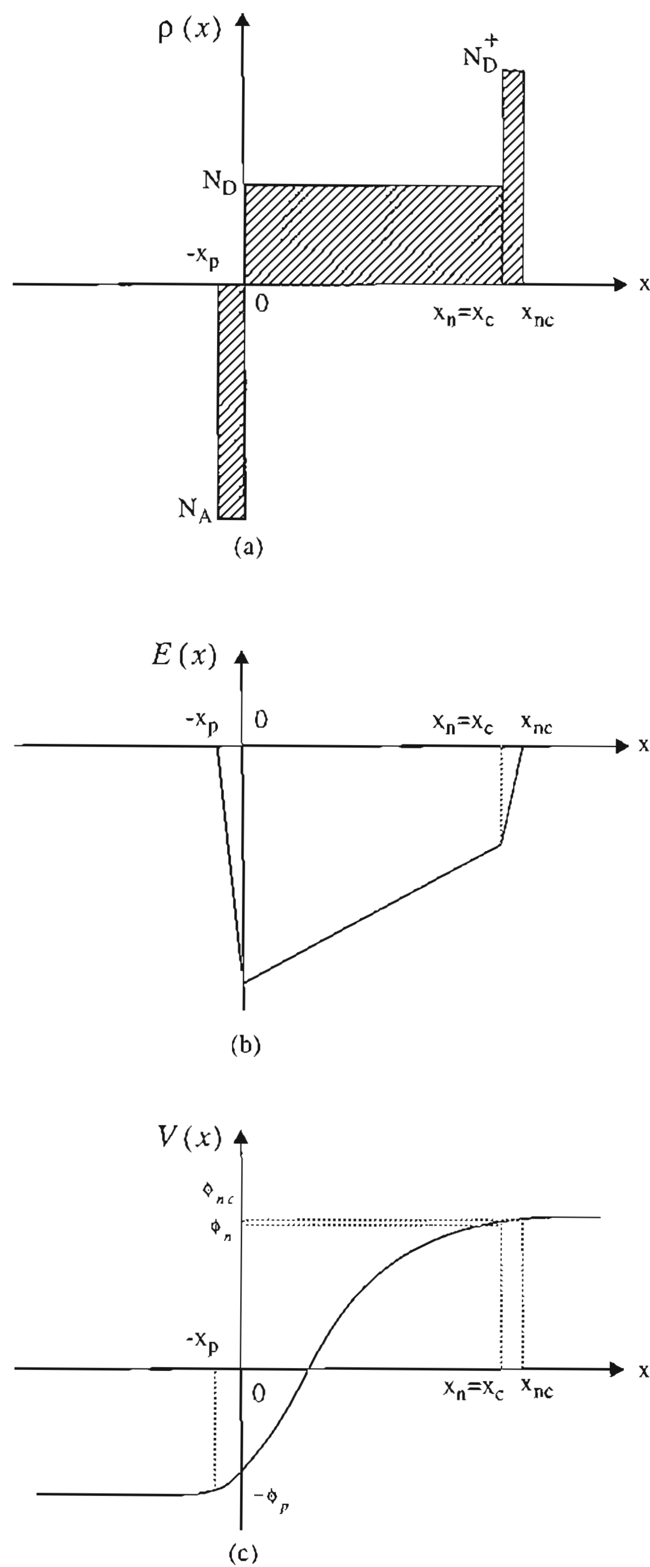

FIGURE B.1 (a) Depletion charge density, (b) electrical field, and (c) potential in depletion regions.

$$V(x) = \begin{cases} \phi_p & x < -x_p \\ \frac{qN_A}{2\varepsilon}(x+x_p)^2 + \phi_p & -x_p \le x < 0 \\ \phi_n - \frac{qN_D}{2\varepsilon}(x-x_n)^2 - \frac{qN_D^+}{\varepsilon}(x_{nc}-x_n)(x_n - x) & 0 \le x < x_n \\ \phi_{nc} - \frac{qN_D^+}{2\varepsilon}(x-x_{nc})^2 & x_n \le x \le x_{nc} \\ \phi_{nc} & x \ge x_{nc} \end{cases} \tag{B.3}$$

Charge neutral requirement gives

$$qN_A x_p = qN_D x_n + qN_D^+ (x_{nc} - x_n) \tag{B.4}$$

$V(x)$ should meet the continuity condition at $x = 0$ and $x = x_n$

$$\frac{qN_A}{2\varepsilon}x_p^2 + \phi_p = \phi_n - \frac{qN_D}{2\varepsilon}x_n^2 - \frac{qN_D^+}{\varepsilon}(x_{nc} - x_n)x_n \tag{B.5}$$

$$\phi_n = \phi_{nc} - \frac{qN_D^+}{2\varepsilon}(x_n - x_{nc})^2 \tag{B.6}$$

From Eqn. (B.4), we have

$$x_{nc} - x_n = \frac{N_A x_p - N_D x_n}{N_D^+} \tag{B.7}$$

Substituting Eqn. (B.7) in (B.5), and after rearrangement, we get a quadratic equation with respect to x_p

$$x_p^2 + 2x_p x_n - \frac{N_D}{N_A}x_n^2 - \frac{2\varepsilon}{qN_A}\phi_i = 0 \tag{B.8}$$

where $\phi_i = \phi_n - \phi_p$. Solve for x_p

$$x_p = \left(\frac{N_D}{N_A} + \frac{2\varepsilon\phi_i}{qN_A x_n^2}\right)x_n \tag{B.9}$$

Take the result of (B.9) back to (B.7), finally we have:

$$x_{nc} - x_n = \frac{2\varepsilon\phi_i}{qN_D^+ x_n} \tag{B.10}$$

APPENDIX C

Voltage Transfer Characteristics Analysis

Applying Kirchoff current law (KCL) to node V_b of the circuit shown in Fig. 6.4 and ignoring the base current I_b, we have equation

$$\frac{V_i - V_b}{R_g} + \frac{V_o - V_b}{R_f} = \frac{V_b}{R_1} \tag{C.3}$$

<u>*CASE A.*</u> Assume both Q_1 an Q_2 being off, $I_{C_1} = I_{C_2} = 0$ at node V_o, then

$$\frac{V_{CC} - V_o}{R_C} = \frac{V_o - V_b}{R_f} \tag{C.4}$$

Therefore,

$$V_b = -\frac{V_{CC}}{R_C/R_f} + \left(1 + \frac{R_f}{R_C}\right)V_o \tag{C.5}$$

Substitution of (C.3) into (C.1), solve for V_o

$$V_o = \frac{1}{1 + \frac{R_f}{R_C} - \frac{1}{1 + \frac{R_f}{R_1} + \frac{R_f}{R_g}}}\left(\frac{V_i}{1 + \frac{R_g}{R_1} + \frac{R_g}{R_f}} + \frac{V_{CC}}{R_C/R_f}\right) \tag{C.6}$$

As $\frac{R_f}{R_C} - \frac{1}{1 + \frac{R_f}{R_1} + \frac{R_f}{R_g}} \ll 1$, which is true in current case,

$$V_o \approx \frac{V_i}{1 + \frac{R_g}{R_1} + \frac{R_g}{R_f}} + \frac{V_{CC}}{R_C/R_f} \tag{C.7}$$

CASE B. Q_1 starts to conduct — the first breakpoint (BP1), where still with $I_{C_1} = I_{C_2} = 0$ but $V_{b1} = V_{be}(\text{on})$. From (C.2),

$$V_{o1} = \frac{V_{be}(\text{on})}{1 + \frac{R_f}{R_C}} + \frac{V_{CC}}{1 + \frac{R_C}{R_f}} \tag{C.8}$$

Equate (C.5) and (C.6) and solve for V_{i1}

$$V_{i1} = \frac{1 + \frac{R_g}{R_1} + \frac{R_g}{R_f}}{1 + \frac{R_f}{R_C}} \left[V_{be}(\text{on}) - \frac{V_{CC}}{(R_C/R_f)^2} \right] \tag{C.9}$$

CASE C. Q_1 conducts but Q_2 is still off. At node V_o,

$$\frac{V_{CC} - V_o}{R_C} - \frac{V_o - V_b}{R_f} = I_{C_1} \approx I_{E_1} = \frac{V_b - V_{be1}}{R_2} \tag{C.10}$$

$$V_o = \frac{V_{CC}}{1 + \frac{R_C}{R_f}} + \frac{V_b(1 - R_f/R_2)}{1 + \frac{R_f}{R_C}} + \frac{(R_f/R_2)V_{be1}}{1 + \frac{R_f}{R_C}} \tag{C.11}$$

Since

$$V_b = V_{be1} + I_{C_1}R_2 = V_{be1} + I_s e^{\frac{V_{be1}}{V_T}} \cdot R_2 \tag{C.12}$$

where $V_T = kT/q$. Rewrite V_o as

$$V_o = \frac{V_{CC}}{1+\dfrac{R_C}{R_f}} + \frac{V_{be1}}{1+\dfrac{R_f}{R_C}} + \frac{I_s e^{V_{be1}/V_T} \cdot (1 - R_f/R_2)}{1+\dfrac{R_f}{R_C}} \tag{C.13}$$

From (C.1), also we have

$$V_o = \left(1 + \frac{R_f}{R_1} + \frac{R_f}{R_g}\right)V_b - \frac{V_i}{R_g/R_f} \tag{C.14}$$

Substitute V_b with (C.11)

$$V_o = \left(1 + \frac{R_f}{R_1} + \frac{R_f}{R_g}\right)\left(V_{be1} + I_s R_2 e^{\frac{V_{be1}}{V_T}}\right) - \frac{V_i}{R_g/R_f} \tag{C.15}$$

Equate (C.12) and (C.14) and solve for V_i

$$\begin{aligned} V_i = \frac{R_g}{R_f}\Bigg[&\left(1 + \frac{R_f}{R_1} + \frac{R_f}{R_g} - \frac{1}{1+R_f/R_C}\right)V_{be1} \\ &+ \left(1 + \frac{R_f}{R_1} + \frac{R_f}{R_g} - \frac{1-R_f/R_2}{1+R_f/R_C}\right)I_s R_2 e^{\frac{V_{be1}}{V_T}} - \frac{V_{CC}}{1+R_C/R_f}\Bigg] \end{aligned} \tag{C.16}$$

The transfer function V_o vs. V_i is now expressed as a set of parametric functions

$$\begin{aligned} V_{oII} &= V_{oII}\,(V_{be1}) \\ V_{iII} &= V_{iII}\,(V_{be1}) \end{aligned} \tag{C.17}$$

where the subscript II means region II.

<u>CASE D.</u> Q_2 starts to conduct — the second breakpoint (BP2), but still with $I_{C_2} = 0$. We have

$$\frac{V_{CC} - V_{o2}}{R_C} = \frac{V_{o2} - V_{b2}}{R_f} + I_{C1} \tag{C.18}$$

$$V_{b2} = V_{be1} + V_{be}(\text{on}) \tag{C.19}$$

and

$$I_{C_1} = \frac{V_{be}(\text{on})}{R_2} \tag{C.20}$$

Insert (C.18) and (C.19) into (C.17) and take some rearrangement

$$V_{o2} = \frac{V_{CC}}{1+\frac{R_C}{R_f}} + \frac{V_{be}(\text{on})}{1+\frac{R_f}{R_C}} + \frac{V_{be1} - (R_f/R_2)\,V_{be}(\text{on})}{1+\frac{R_f}{R_C}} \tag{C.21}$$

Compare (C.20) with (C.6) and note $R_f/R_2 < 1$, one can see:

$$V_{o2} > V_{o1} \tag{C.22}$$

From (C.17), (C.18) and (C.19)

$$V_{b2} = \left(1+\frac{R_f}{R_C}\right)V_{o2} - \frac{V_{CC}}{R_C/R_f} + \frac{V_{be}(\text{on})}{R_2/R_f} \tag{C.23}$$

Substitute (C.22) into (C.13) and rearrange it

$$\left(1+\frac{R_f}{R_C} - \frac{1}{1+\frac{R_f}{R_1}+\frac{R_f}{R_g}}\right)V_{o2} = \frac{V_{CC}}{R_C/R_f} + \frac{V_{i2}}{1+\frac{R_g}{R_1}+\frac{R_g}{R_f}} - \frac{V_{be}(\text{on})}{R_2/R_f} \tag{C.24}$$

Again, assume $R_f/R_C - 1/(1+R_f/R_1+R_f/R_g) \ll 1$

$$V_{o2} \approx \frac{V_{i2}}{1+\frac{R_g}{R_1}+\frac{R_g}{R_f}} + \frac{V_{CC}}{R_C/R_f} - \frac{V_{be}(\text{on})}{R_2/R_f} \tag{C.25}$$

Equate (C.24) and (C.20) and solve for V_{i2}

$$V_{i2} = \frac{1+\frac{R_g}{R_1}+\frac{R_g}{R_f}}{1+\frac{R_f}{R_C}}\left[V_{be}(\text{on}) - \frac{V_{CC}}{(R_C/R_f)^2} + \frac{R_f}{R_2}\left(V_{be1} + \frac{R_f}{R_C}V_{be}(\text{on})\right)\right] \tag{C.26}$$

The curve slope of region II can be expressed as follows:

$$\frac{\Delta V_{oII}}{\Delta V_{iII}} = \frac{V_{o2} - V_{o1}}{V_{i2} - V_{i1}} = \frac{1}{\frac{R_f}{R_2}\left(1 + \frac{R_g}{R_1} + \frac{R_g}{R_f}\right)\frac{V_{be1} + (R_f/R_C)\,V_{be}(\mathrm{on})}{V_{be1} - (R_f/R_2)\,V_{be}(\mathrm{on})}} \tag{C.27}$$

In our case,

$$\frac{R_f}{R_2} \cdot \frac{V_{be1} + (R_f\,/R_C)\,V_{be}(\mathrm{on})}{V_{be1} - (R_f\,/R_2)\,V_{be}(\mathrm{on})} > 1 \tag{C.28}$$

Therefore

$$\frac{\Delta V_{oII}}{\Delta V_{iII}} < \frac{1}{1 + \frac{R_g}{R_1} + \frac{R_g}{R_f}} = \text{SLOPE OF REGION I} \tag{C.29}$$

CASE E. Both Q_1 and Q_2 conduct. At node V_o, the current equation is:

$$\frac{V_{CC} - V_o}{R_C} + \frac{V_b - V_o}{R_f} = I_{C_1} + I_{C_2} \tag{C.30}$$

with

$$I_{C_1} = \frac{V_b - V_{be1}}{R_2} \tag{C.31}$$

$$I_{C_2} = \frac{V_b - V_{be1} - V_{be2}}{R_3} \tag{C.32}$$

Rearrange (C.29) into

$$\left(\frac{1}{R_C} + \frac{1}{R_f}\right) V_o = \frac{V_{CC}}{R_C} + \frac{V_{be1}}{R_f} + \left(\frac{1}{R_f} - \frac{1}{R_2}\right) V_{be2} - \left(1 - \frac{R_3}{R_f} + \frac{R_3}{R_2}\right) I_{C_2} \tag{C.33}$$

Assume $\frac{R_3}{R_f}, \frac{R_3}{R_2} \ll 1$ and note $I_{C_2} = I_s e^{V_{be2}/V_T}$

$$V_o \approx \frac{V_{CC}}{1+\frac{R_C}{R_f}} + \frac{V_{be1}}{1+\frac{R_f}{R_C}} + \frac{(1-R_f/R_2)\,V_{be2}}{1+\frac{R_f}{R_C}} - \frac{R_f}{1+\frac{R_f}{R_C}} I_s e^{V_{be2}/V_T} \tag{C.34}$$

In this region V_o will drop off drastically due to the conduction of Q_2.

Since $V_b = V_{be1} + V_{be2} + I_{C_2} R_3$ at here, repeat the procedure done before and get

$$\begin{aligned} V_i = \frac{R_g}{R_f} \Bigg\{ & -\frac{V_{CC}}{1+\frac{R_C}{R_f}} + \left(1 + \frac{R_f}{R_1} + \frac{R_f}{R_g} - \frac{1}{1+\frac{R_f}{R_C}}\right) V_{be1} \\ & + \left(1 + \frac{R_f}{R_1} + \frac{R_f}{R_g} - \frac{1-R_f/R_2}{1+R_f/R_C}\right) V_{be2} \\ & + \left[R_3 \left(1 + \frac{R_f}{R_1} + \frac{R_f}{R_g}\right) + \frac{R_f}{1+\frac{R_f}{R_C}} \right] I_s e^{V_{be2}/V_T} \Bigg\} \end{aligned} \tag{C.35}$$

Similar to *Case E*, we can get the transfer function in this region in the form of follows:

$$\begin{aligned} V_{oIII} &= V_{oIII}(V_{be2}) \\ V_{iIII} &= V_{iIII}(V_{be2}) \end{aligned} \tag{C.36}$$

as shown in (C.33) and (C.34) with V_{be1} approximately taken as a constant here.

CASE F.The point where V_o stops dropping — the third breakpoint (BP3). At this point $V_{be1} = V_{be}$(satuation) and V_{ce1} can be considered as a constant. On the other hand, V_{be2} drops down as V_o does and so is I_{C_2}, which now is much less than I_{C_1} again.

CASE G. After BP3, V_o will increase again since I_{C_1} dominates the collector current once more. The equivalent circuit at this moment can be drawn as shown in Fig. C1.

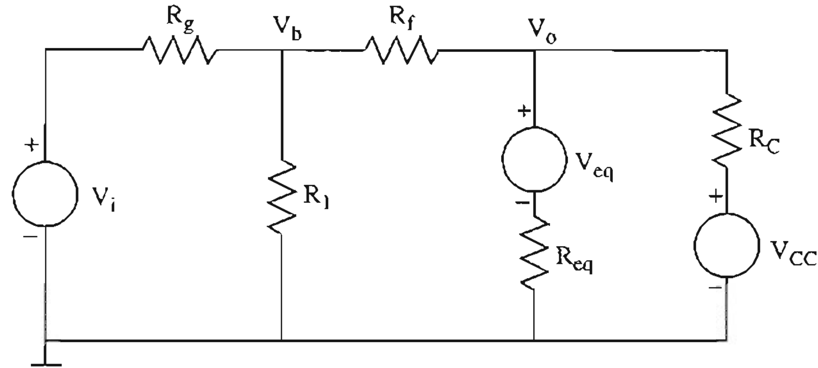

FIGURE C.1 Equivalent circuit in CASE F

In the equivalent circuit, Q_1 is considered as an equivalent voltage source V_{eq} in series with a resistor R_{eq}, where V_{eq} is assumed as the sum of $V_{ce1}(\text{sat})$ and the voltage drop on R_2, and R_{eq} is mainly account for the emitter and collector resistance. At node V_o, the current equation can be written as follows:

$$\frac{V_b - V_o}{R_f} = \frac{V_o - V_{eq}}{R_{eq}} + \frac{V_o - V_{CC}}{R_C} \tag{C.37}$$

which turns out

$$V_b = \left(1 + \frac{R_f}{R_C} + \frac{R_f}{R_{eq}}\right)V_o - \frac{R_f}{R_{eq}}V_{eq} - \frac{R_f}{R_C}V_{CC} \tag{C.38}$$

Take (C.37) into (C.13) and solve for V_o, finally we have

$$V_o = \frac{1}{\left(1+\frac{R_g}{R_f}+\frac{R_g}{R_1}\right)\left(1+\frac{R_f}{R_C}+\frac{R_f}{R_{eq}}\right)-\frac{R_g}{R_f}} \cdot \left[V_i+\left(1+\frac{R_g}{R_f}+\frac{R_g}{R_1}\right)\left(\frac{R_f}{R_{eq}}V_{eq}+\frac{R_f}{R_C}V_{CC}\right)\right] \quad \text{(C.39)}$$

This is the transfer function in region IV, the last region of the VTC curve. From the above equation, one can see that the output increases linearly with the input simply due to the pushed-up effect by the input.

With these transfer functions in different regions determined, now it is ready for plotting out the curve of V_{out} vs. V_{in}, which is shown in Fig. 6.5(a). The data used for the VTC calculations are listed as follows:

$R_f = 260\Omega$	$R_1 = 1300\Omega$	$R_2 = 400\Omega$	$R_3 = 13\Omega$
$R_{eq} = 50\Omega$	$R_g = 50\Omega$	$R_C = 1000\Omega$	$I_s = 10^{-23}A$
$V_{CC} = 5V$	$V_{eq} = 1.2V$	$V_{be}(\text{on}) = 1.15V$	$V_{be}(\text{sat}) \geq 1.35V$

APPENDIX D

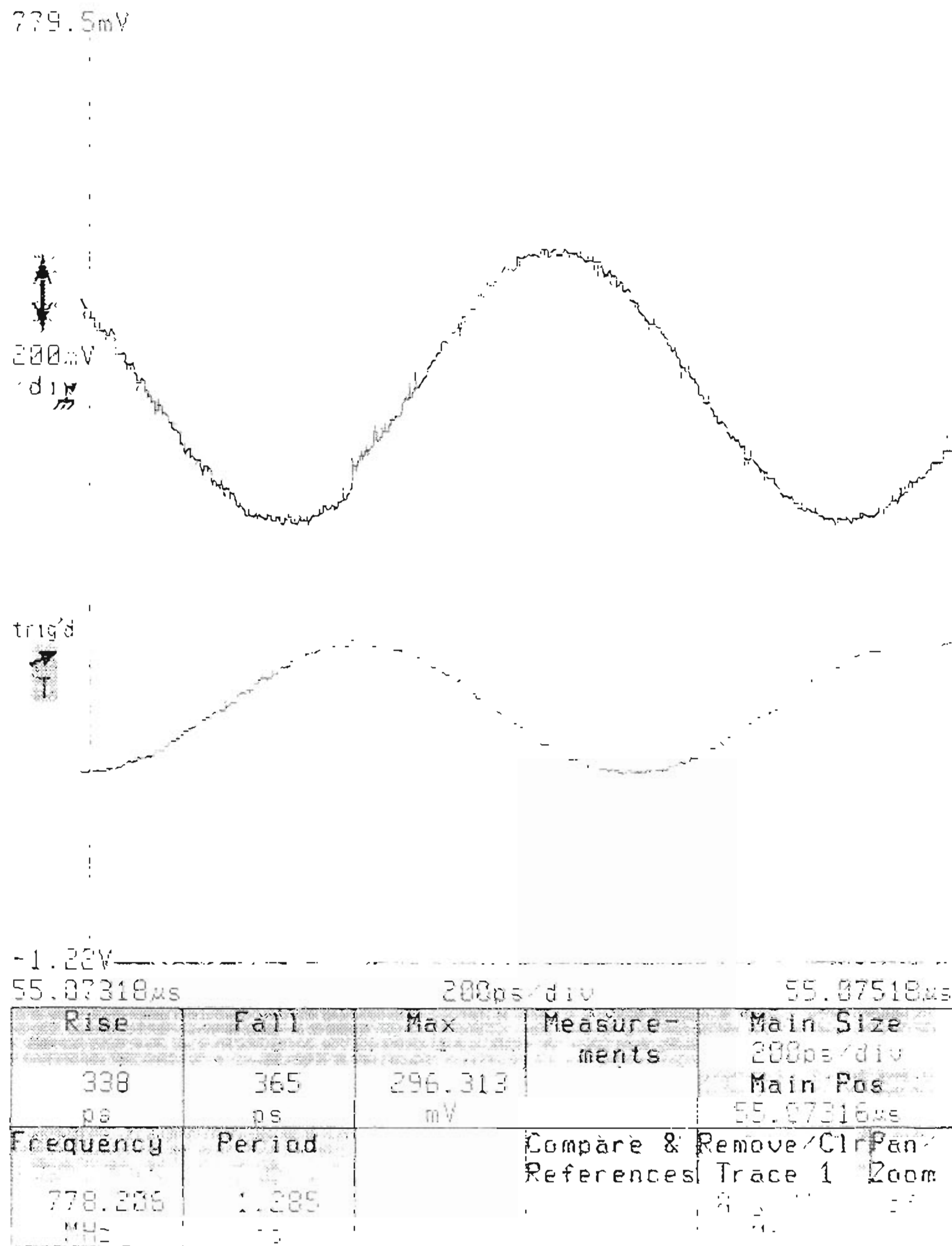

FIGURE D.1 High-speed sinusoidal signal response of the packaged AlGaAs/GaAs HBT Darlington feedback amplifier

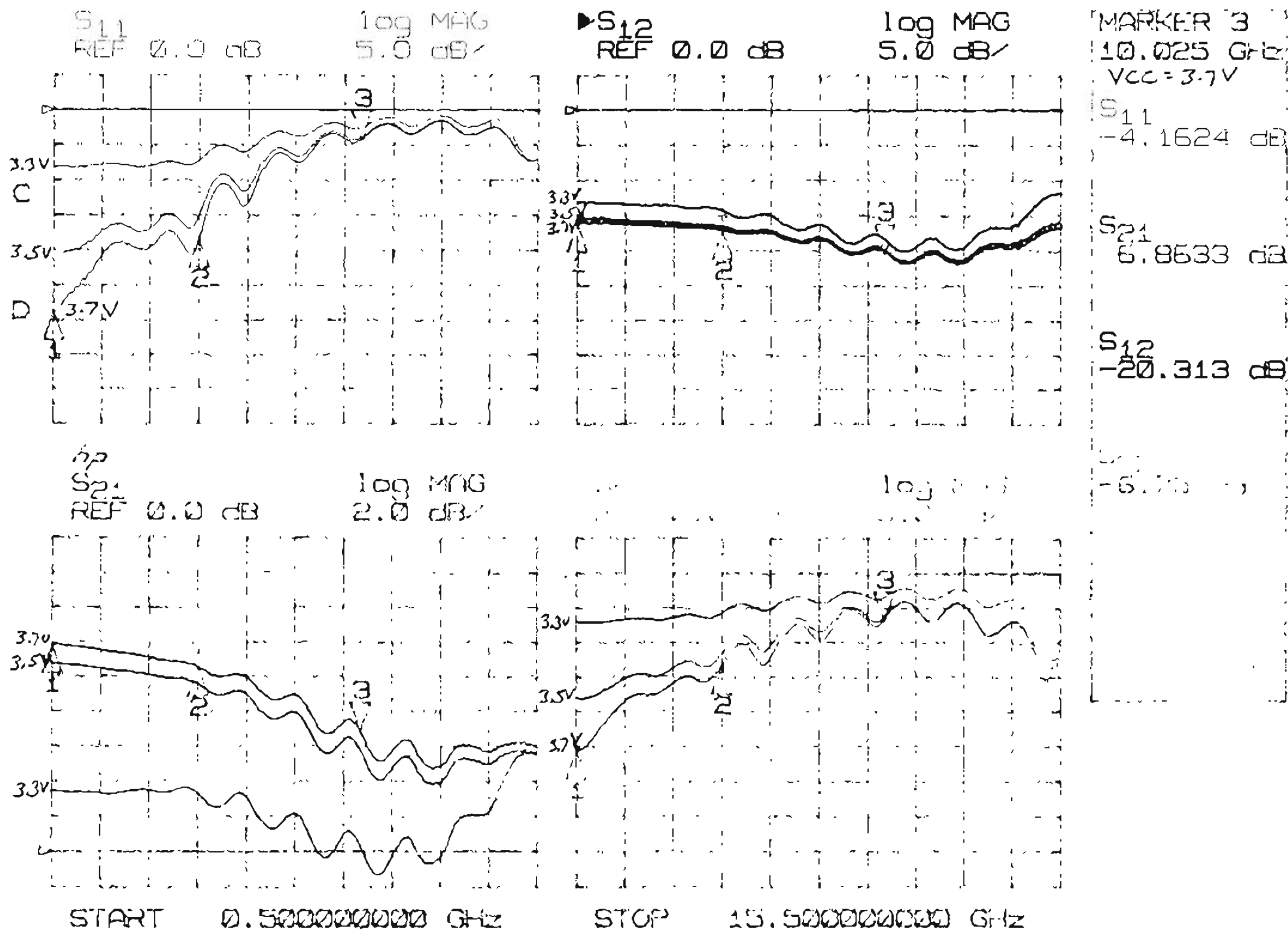

FIGURE D.2 Return losses and insert losses of the packaged AlGaAs/GaAs HBT Darlington feedback amplifier measured at the frequency range 0.5 GHz - 15.5 GHz and at different biases

VITA

The author was born on Nov. 11, 1955 in Shuyang, Jiangsu Province, China. He earned a B.S. degree in Physics from Suzhou University in 1982, and was assigned a position in local education administration engaged in the research on teaching methodology. Two years later, he entered Shanghai Institute of Laser Technology for Master program studies and worked on laser-induced chemical vapor deposition (LCVD) technology. In 1987, he earned a M.S. degree in Optics from SILT, and then accepted an electrical engineer position in Shanghai Medical Laser Instruments Factory, where he spent three years to develop a new model of laser-Doppler flowmeter (LDF) to monitor the average blood perfusion in tissue by using laser-Doppler techniques. This machine was appraised by Shanghai Division of the State Science & Technology Commission of China in January, 1991, and awarded a silver medal by the National Bureau of Medicine of China in 1992. In September, 1990, he came to Oregon Graduate Institute and started his Ph.D program studies in semiconductor materials and devices area.