SENSOR–ARRAY CHIP HYBRID FOR SIMULTANEOUS MULTIPLE ANALYTE DETECTION

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Abstract

SENSOR–ARRAY CHIP HYBRID FOR SIMULTANEOUS MULTIPLE ANALYTE DETECTION

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Advancements in the micro sensor and integrated chip technologies have led to the integration of sensors and the quantifying electronics in a single package. Various lab-on-chip (LOC) techniques have been developed and are usually geared towards the bio-tech industry, dealing frequently with analysis of target molecules in liquid medium. Similar integrated technology has also evolved for the detection of gaseous analytes and is commonly known as electronic nose or e-nose. It would be of great advantage if multiple targets in both liquid and gaseous mediums could be identified and quantified by a single device. This would also serve as a common platform for the development of new detection strategies.

In this dissertation, I have developed a sensor-array chip hybrid for rapid parallel detection of multiple organic or inorganic target molecules in either gas or liquid mediums. The developed system is based on measuring minute changes in capacitances for detection. The sensors in the designed sensor-array chip hybrid are capacitive sensors, micro fabricated on top of a pre-designed CMOS chip with circuitry to measure small changes in capacitance. The capacitor sensors were built using the well advanced technique of focused ion beam

(FIB) micromachining and microforming. In this thesis I also present multiple circuit techniques that can detect femto farad changes in sensor capacitance. I have validated these circuits by simulation and post fabrication electrical testing. I have also evaluated the applications of this system in multidisciplinary research including:

1) Detection and measurement of organophosphate neurotoxins
2) Air quality monitoring - detection of low concentrations of carbon monoxide gas
3) Aid in the study of early detection of stroke

1. Introduction

Multidisciplinary research in life science and engineering for the past thirty years has led to the development of a multitude of sensors with various material compositions to detect trace amounts of diverse target molecules. In recent years, biotechnology and medical fields have seen great advances in the development of novel biosensor technologies that open new horizons for identifying and quantifying biomolecules and diagnosing diseases.

A biosensor is a device that consists of a biological detection element or bioreceptor (e.g. an antibody, an enzyme, a protein, a nucleic acid, whole cells, tissues or whole organisms) and a signal transducer. When the analyte interacts with the bioreceptor, the resulting complex produces a change which is converted into a measurable effect (e.g. an electrical signal) by the transducer [1].

The most common types of biosensors are based on:

1) Antibody/antigen interactions
2) Nucleic acid interactions
3) Enzymatic interactions
4) Cellular interactions (e.g. microorganisms, proteins)
5) Interactions using synthetic bioreceptors

The most prevalent signal transduction methods include:

1) Optical measurements (e.g. luminescence, absorption, etc.)
2) Electrochemical (e.g. potentiometric, amperometric, etc.)
3) Mass-sensitive measurements (e.g. surface acoustic wave, micro-cantilever, etc.)

There is an increasing need to perform biological testing for on site environmental, medical, forensics, and biohazard detection [2-5]. On site detection of low concentrations of environmental toxins, without extensive lab processing has become imperative.

Steps involved in a typical biological test procedure are shown in Figure 1.1. Conventional biological assay techniques are labor intensive, and the protocols implemented and followed during analysis often require days or weeks to perform at a cost of hundreds of dollars per test. Problems remain in detecting and quantifying low levels of biological compounds reliably, conveniently, safely and quickly.

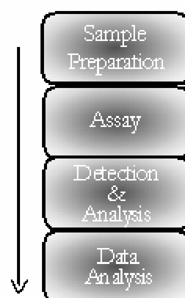


Figure 1.1: Typical biological testing procedure.

Consequently this necessitates the development of a device capable of integrating multiple analytical and detection procedures on a single platform to enable robust, low-cost point-of-care analysis. There have been recent efforts to develop such lab-on-chip (LOC) solutions in which sampling, analysis and reporting of a wide range of target compounds are integrated and automated, Figure 1.2. These lab-on-chips devices bring the analysis platform to integrated chip (IC) technology which paves the way for reduction in system size. In addition to reducing system size, cost, and power consumption, such lab-on-chips can increase system throughput, thus reducing testing time and labor.

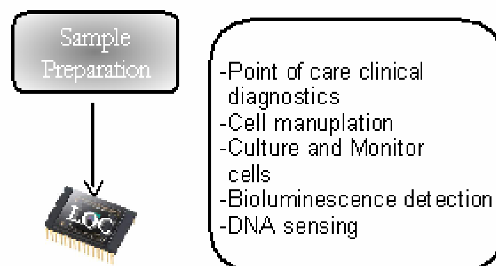


Figure 1.2: Lab-on-Chip.

Typical applications for chips that were developed based on lab-on-chip technology include:

1) LOC for individual cell manipulation and detection using dielectrophoretic actuators and optical sensors that allow biologists to displace individual cells to specific locations on the chip using software [6-7]. This enables them to orient and place cells in complex interaction schemes without damaging the viability of the cells.
2) LOC for localization of bio-particles on CMOS chip [8].
3) LOC for DNA sensing which detects the presence/absence of specific DNA sequence [9].
4) Disposable biochip with passive micro-fluidics for applications in clinical diagnostics and point-of-care testing [10].

LOC techniques are usually geared towards the bio-tech industry dealing frequently with analysis of target molecules in liquid medium. Similar integrated technology has also evolved for the detection of gaseous analytes and is commonly known as electronic nose or e-nose, refer Figure 1.3.

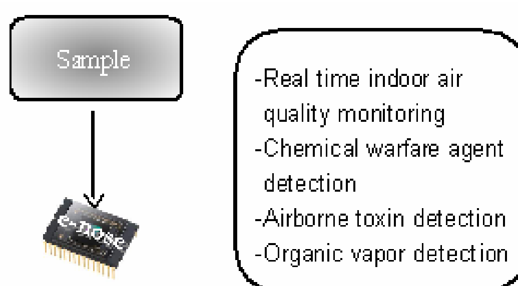


Figure 1.3: e-nose.

Typical chips derived from e-nose technology offer:

- Low-cost real time indoor air quality monitoring applications for the detection and quantification of low concentrations of gases like CO, N2, etc. [11]
- Chemical warfare agent and toxic industrial chemical detection [12]

- Detection of low level concentrations of organic vapors (methanol, ethanol, isopropyl alcohol, etc.) [13]

To design a platform that can be used by multidisciplinary researchers, the sensing element or the transducer should be able to translate the output from various detection techniques implemented (potentiometric, amperometric, luminescence, absorption, nucleic acid interactions, antibody/antigen interactions, enzymatic interactions, cellular interactions, etc.) into a form that can be electrically measured. All elements and compounds have a specific dielectric constant or relative permittivity. When a target molecule interacts with the sensing element the relative permittivity of the reaction mixture is likely to be different than that of the reactants. This can be generalized for almost all detection schemes. For example, a conventional amperometric system relies on the generation of current (electrons) for detection. If the same transducer material that generates current in the presence of the target molecule is incorporated as the dielectric layer in a capacitor, the generation of current would normally reflect as a reduction in capacitance. This change in capacitance can be measured. Likewise any reaction or interaction used by other detection techniques will most likely result in a capacitance change caused by changes in relative permittivity. Measuring the change in relative permittivity is a direct measure of the reaction rate and hence the target molecule concentration. The dielectric constant of the sensing elements and that of the elements present in the sensing environment also cause a change in the dielectric constant which has to be analyzed and quantified to establish selectivity. Hence capacitive sensors through which changes in relative permittivity can be measured are most suited for developing a multidisciplinary test platform. Change in dielectric constant between the active elements of a capacitor sensor causes a change in absolute capacitance which can be measured electrically.

The most prevalent applications for capacitor sensors are in pressure sensing and in accelerometers. Conventional capacitance based pressure sensors derived from discrete solid state sensor technologies are being integrated on silicon along with the detection circuits in a single package [14]. In these applications, a thin silicon membrane is employed as a diaphragm layer over a solid substrate with a small air gap between the two layers. Variations

in pressure would cause compression or relaxation of the diaphragm layer causing a change in the air gap between the layers. This change in air gap reports as capacitance change which is measured using integrated circuits fabricated on the same substrate. These sensor structures are generally large and produce changes in pico-farad scale. Fabrication of these sensors commonly involve wet etch techniques and extra lithography mask development stages beside the steps involved in the fabrication of the detection circuitry. Similar sensors have been developed for implantable pressure sensing applications using bio-compatible materials [15]. The development of lab-on-chip devices for biochemical analysis has seen a tremendous growth over the past decade. Capacitance sensor based lab-on-chips are being explored to develop sensor hybrids for monitoring live biological cells and also for point of care clinical diagnostics. Somashekar Prakash et al. [16] have developed a capacitor sensor based lab-on-chip for monitoring biological cells. They exploit the fringing capacitance of an exposed top metal sensor structure to track biological cell adhesion and assessing cell viability. A similar system which exploits fringing capacitance of a large top metal sensor structure has been recently demonstrated by Ebrahim Ghafar-Zadeh et al. [17] for blood based biochemical and cellular analysis. They describe the development of a micro-fluidic channel on top of the sensor structure and also demonstrate excellent circuit sensitivity to sub femto farad changes. Complex micro-fluidic systems have been developed for delivering the analyte liquids to the sensor structures [5].

Many of these developed hybrid systems rely on the fringing capacitance of sensor structures fabricated using the top metal layer of an integrated chip. For target specific sensing applications these structures have to be coated or treated with a biomarker or target selective layer. This layer has to be thin; else the fringing field above the sensor structures would reduce, thereby degrading sensitivity. To offset this problem, the sizes of these structures need to be increased. The system designed in this thesis uses parallel plate capacitor sensors fabricated on the top surface of an integrated chip. The gap between the capacitor plates are coated with the target selective layer. Since the system relies on direct field between the plates along with the fringing fields, higher sensitivities can be achieved in relatively smaller footprint. Most of the previously developed capacitance based LOCs are geared towards analysis of liquid mediums alone. It would be of great advantage if multiple

targets in either liquid or gaseous mediums could be identified and quantified by a single device. This would also serve as a common platform for the development of new detection strategies.

This dissertation focuses on

1. Developing sensor-array chip hybrids for the rapid parallel detection of multiple organic and inorganic target molecules in gas and liquid environments, unlike typical LOCs' that cater to analysis of only liquid test mediums.
2. Designing the hybrid with minimal post fabrication steps.
3. Creating an array of highly sensitive microelectronic sensor platform.
4. Designing and developing a set of circuits that translate the output of the sensors into measurable electrical readings.
5. Providing a platform for researchers in a variety of disciplines to develop micron scale arrays of sensors to monitor diverse analytes.
6. Developing and testing target specific application on a chip.

The sensors in the designed sensor-array chip hybrid are capacitive sensors micro fabricated on top of a pre-designed CMOS chip with circuitry to measure small changes in capacitance. The sensors in the chip hybrid when exposed to environmental stimuli containing the target molecule would respond as a change in capacitance. This change in capacitance will be measured by the underlying circuits that were designed and fabricated to be sensitive to sub-femto farad changes. The sensitivity of the system depends on the detection circuit that measures the change in capacitance. Multiple circuit designs with a range of sensitivities have been designed and fabricated for measuring sub-femto farad changes in capacitance using conventional CMOS 1.5μm process. Each fabricated chip has been designed to contain 16-24 sensor sites which can be used to simultaneously detect multiple analytes.

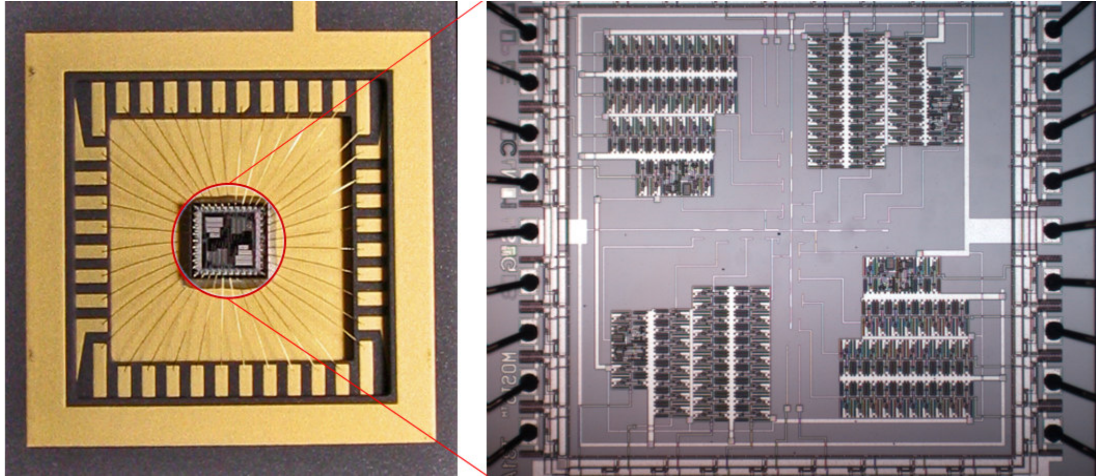


Figure 1.4: Optical image of packaged chip showing active die area.

The capacitor sensors are built using the well advanced technique of focused ion beam (FIB) micromachining and microforming. The FIB workstations have been commonly used in the micro-electronics industry for micro-fabrication, post fabrication editing and debugging. It is a tool capable of milling/machining in the micron and sub-micron scale and can also be used for depositing various types of metals (Platinum, Tungsten, etc.) and oxides for electrical insulation. Using the FIB workstation for fabricating the sensors shortens the development period and allows for rapid prototyping of sensor geometries for any given application. Fabrication of sensors using conventional lithography or MEMS techniques are time consuming and expensive.

Conventional MOS fabrication technique involves designing a lithography mask for each individual layer incorporated in the integrated chip. Any small changes made to the sensor structure require the production of a new lithography mask and re-fabrication of the whole chip which is very expensive and time exhaustive. Also, the conventional CMOS fabrication process does not allow for change in the thicknesses of the embedded layers. The layer thicknesses are defined by the foundry and fabrication technology. Most of the conventional CMOS processes have the outermost metal layer as their thickest layer for carrying higher currents and are generally less than 1 micron. This does not allow much flexibility for sensor geometry.

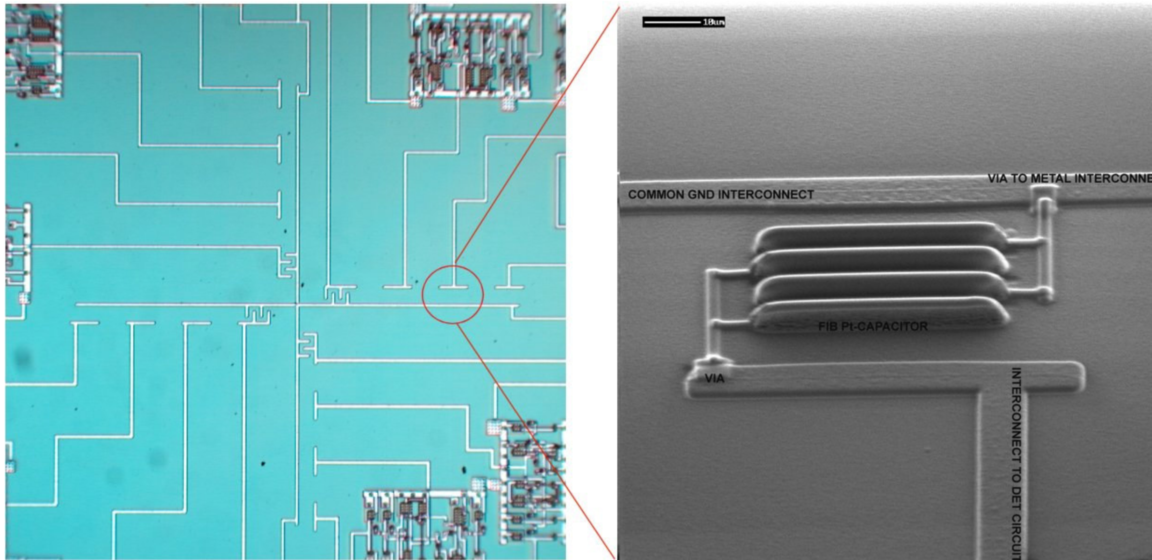


Figure 1.5: Optical and SEM image (marker is 10µm) showing sensor site on SiN passivated chip and FIB fabricated Pt plate interdigitated capacitor sensor.

Micron sized capacitive sensors are fabricated on the silicon nitride passivation of a completed chip using the FIB's ability to deposit Pt metal. See figure 1.4 for an optical image of an entire fabricated chip with multiple detection/conversion circuits and interconnects running to the center of the chip for wiring to an array of sensors. Figure 1.5 shows a typical FIB deposited platinum interdigitated parallel plate capacitor sensor wired to the detection circuit.

The left side of Figure 1.5 shows an optical image of the buried detection or conversion circuitry below the passivation (small rectangular structures at corners) with buried insulated metal interconnects from each circuit terminating at the center of the layout. This end along with a common ground interconnect constitute the active ends to which the sensors are attached. The FIB is used to mill Vias through the micron thick passivation layer at the sensor sites to expose the underlying metal (Al) interconnects. The electrical connection between the capacitor sensors and the buried interconnects is established by filling the Vias with platinum and extending platinum traces from the sensors to the filled Vias. See second half of Figure 1.5

The FIB fabricated platinum sensors are treated with a target selective layer (thin film of a metal, oxide, polymer, antibody/antigen, etc.) developed by other researchers.

1.1. Applications researched and tested using the sensor-array chip hybrid

1.1.1. Detection and measurement of organophosphate neurotoxins

Organophosphate (OP) insecticides and OP nerve gases such as Sarin are neurotoxic compounds. Because of the potential for use of OP chemicals by terrorist organizations, a high priority of various federal agencies is the development of methods for monitoring exposure to these compounds in humans and for detecting small amounts of Ops in the environment. Additionally, increasing concern regarding the use of OP insecticides in the U.S. has led to recent re-evaluation of their registered uses by the EPA. A major issue that complicates the risk assessment of Ops to humans is the lack of information regarding exposure to low levels of Ops. Standard immunoblot tests and electrophoresis based tests were developed by a collabo-rative research group led by Dr. Pamela Lein at CROET (Center for Research on Occupational and Environmental Toxicology) at Oregon Health & Sciences University (OHSU) for the detection of organophosphorus compounds. Reactants used in those methods were tested on the sensor-array chip hybrid with an objective to expedite the detection process by eliminating the generally time consuming electrophoretic methods.

1.1.2. Air quality monitoring – detection of low concentrations of carbon monoxide gas

Air quality monitoring is of utmost importance and exposure to air contaminants like carbon monoxide poses a likely hazard to human well being. Carbon monoxide (CO) is the gas produced during incomplete combustion processes from sources like car engines and exhaust systems and is toxic even at low concentrations. Exposure to CO gas at concentrations of 50ppm in normal atmosphere over a period of 8 hours is considered to be the maximum tolerable level. Various sensors have been developed to detect carbon monoxide and most of them operate at temperatures ranging from 150 to 400 ^{o}C. This means that a heating element must be included along with the sensor which effectively increases the overall power consumption of the device. A tin oxide based room temperature

carbon monoxide sensing system has been developed and implemented on the sensor-array chip hybrid.

1.1.3. Biochemistry of stroke - understanding mechanisms of damage and the development of protective therapies

Stroke is the third leading cause of death and a major cause of long-term disability in the United States. Unfortunately, most clinical trials of acute stroke therapy have proven unsuccessful, and currently there are very limited therapeutic choices in the clinical management of stroke patients and virtually no therapies to reduce brain damage and disability beyond thrombolytic therapy to restore blood brain perfusion. CART, *cocaine- and amphetamine-regulated transcript*, was identified as a neuroprotective gene using DNA microarrays to determine genes differentially regulated by estrogen in brain under ischemic conditions [19]. Monitoring CART would play an important role in early detection of stroke. Anti-CART peptide antibody has been used in standard Western blot to quantify CART neuropeptide [20]. Reactants used in those methods were tested on the sensor-array chip hybrid to detect CART and have an instantaneous electrical output.

Once a given application has been developed it can supplement other developed detection techniques and can be mass produced. Using the FIB to micro-form the sensors can be replaced by additional conventional lithography steps along with the CMOS process to make it more economically viable. More advanced integrated chip technology (smaller gate size) can be used to increase area density, improve on sensitivity and reduce power consumption. Further circuits could be added to digitize the output of the detection circuits and format it to be read by software. The chips application can further be extended to in-vivo tests by encasing the chip with appropriate bio-compatible packaging. Thus, the sensor-array chip hybrid would perform as a universal test bed for a variety of researchers in rapid parallel detection of multiple organic and inorganic molecules.

2. Sensor Operating Principle

The transducers used in the sensor-array chip hybrid are micron scale platinum capacitors. They are fabricated on the surface of silicon nitride passivation of an integrated chip, using the FIB. A capacitor is a passive electronic component that stores energy in the form of an electrostatic field. In its simplest form, a capacitor consists of two conducting plates separated by an insulating material called the dielectric. The capacitance is directly proportional to the dielectric constant of the material between the plates, surface area of one plate, and is inversely proportional to the separation between the plates. Consider the simple parallel plate capacitor, shown in Figure 2.1

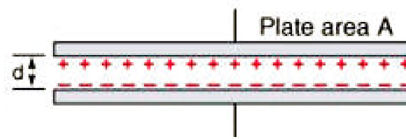


Figure 2.1: Parallel plate capacitor.

Capacitance is given by $$C = \frac{\varepsilon_o \varepsilon_r A}{d} \text{ (Farads)}$$

Eq-2.1: Sensor capacitance

ε_o = Permittivity of free space = 8.854 × 10-12 F/m, ε_r = Relative permittivity or dielectric constant (k) of material between the plates, A= Plate area, d = Distance between the plates.

The increase or decrease in relative permittivity (ε_r) of the material between the plates causes a direct change in the absolute capacitance. Measure of this change in capacitance from baseline value constitutes the basic operating principle of this detection technique.

The platinum capacitors deposited by the FIB are the active devices on which a target selective layer or membrane is deposited. This layer could be a thin film of a metal, oxide, polymer, antibody, etc., depending on the intended target and application.

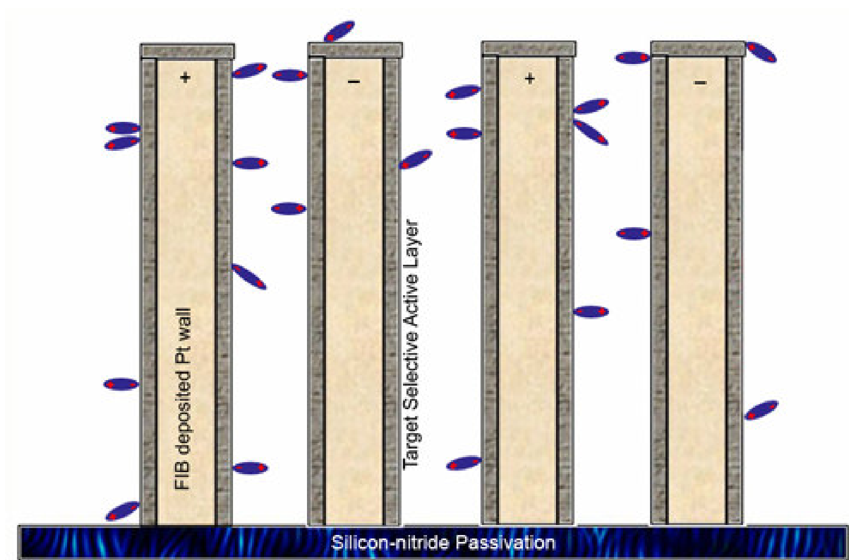


Figure 2.2: Illustration of FIB deposited parallel plate capacitor on Silicon nitride passivation with target selective active thin film or deposit.

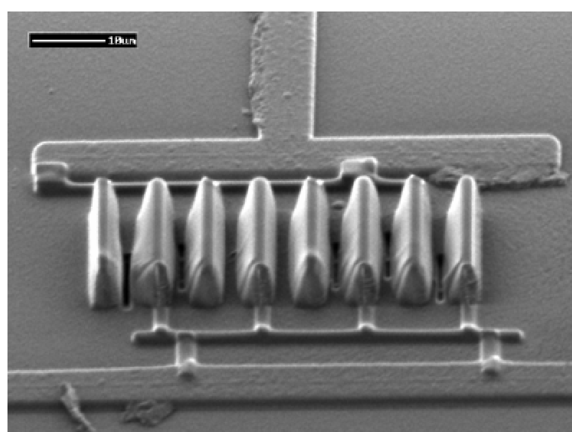


Figure 2.3: SEM micrograph of typical platinum interdigitated capacitor sensor ready to be coated with a target selective layer. (Scale is 10μm)

A target molecule, airborne or in liquid, enters the gap between the plates and reacts with the activated surfaces (Figure 2.2). The target molecules collide with the activated

surfaces and if the translational energy is just right, it is driven close enough to the activated surface to form a bond with the atoms of the surface, without sufficient recoil energy to break the bond and thereby is chemisorbed or physisorbed. The magnitude of the change in capacitance depends on the relative permittivity ε_r of the molecule reacting with the activated thin film and the total area covered by this reaction product. As this reaction progresses, depending on the arrival rate and the probability of bonding or the sticking coefficient of the target molecules, the capacitance of the sensor changes which gives a measure of the concentration of the target molecules in the ambient.
Capacitance of the sensor can also be represented by actual permittivity of the material.

$$C = \frac{\varepsilon_o \varepsilon_r A}{d} = \frac{\varepsilon A}{d} \quad \text{(Farads)}$$

Eq-2.2: Sensor capacitance

Where ε is the actual permittivity of the material which is the product of relative permittivity (ε_r) and permittivity of vacuum or free space (ε_o).

$$\varepsilon = \varepsilon_o \varepsilon_r = (1 + \chi_e)\varepsilon_o$$

Eq-2.3: Permittivity [21]

$$\chi_e = \varepsilon_r - 1$$

Eq-2.4: Electrical susceptibility [21]

χ_e is the electrical susceptibility of the material. Electrical susceptibility of a dielectric material is a measure of how easily it polarizes in response to exposure to an electric field. Polarization density or simply polarization is the vector field that expresses the density of permanent or induced electric dipole moment in a dielectric material. The polarization vector P is defined as the dipole moment per unit volume. The SI unit of measure is coulombs per square meter.

$$P = (\varepsilon_r - 1)\varepsilon_o E$$

Eq-2.5: Polarization [22]

E is the applied electric field. From Eq-2.4 and 2.5 polarization can also be represented in terms of electrical susceptibility.

$$P = \chi_e \varepsilon_o E$$

Eq-2.5: Polarization in terms of electrical susceptibility [22]

The dipole moment per unit volume of the dielectric material can be represented as an additive action of N elementary dipole moments $\overline{p}$ [21]. The average dipole moment $\overline{p}$ of the atoms and molecules may be assumed to be proportional to the local electric field strength E' that acts on the particle.

$$P = N\alpha E'$$

Eq-2.6: Polarization [21]

α is a proportionality factor called *polarizability* which measures the electrical pliability of the molecule, that is, the average induced dipole moment per unit field strength. Upon application of an external electric field to a material, the electrons surrounding the nuclei of the matter are displaced slightly with respect to the nuclei and gives rise to induced dipole moments. This is referred to as **electronic polarization** α_e of materials. When atoms of different types form a molecule, the electrons are generally not shared symmetrically; instead electron clouds will be displaced eccentrically towards the stronger binding atom thereby creating a separation of the $+^{ve}$ and $-^{ve}$ charge centers of the molecule or atom. When such molecules are subjected to an electric field the net charges due to existing polarity will tend to change the equilibrium positions of the atoms themselves. A second type of induced dipole moment is created by this displacement of charged atoms with respect to each other. This represents the **atomic polarization** α_a of the dielectric. The asymmetric charge distribution between unlike partners of a molecule gives rise to permanent dipole moments and these moments experience a torque when an electric field is applied. This tends to orient them in the direction of the field giving rise to **orientation or dipole polarization** α_d. There is a fourth form of polarization at the interfaces where the electric fields are not well defined and is called **space-charge or interfacial polarization** α_s [21]. When the dielectrics

are subjected to alternating fields, which will be the case in most of the techniques used for measuring capacitance, a phase shift may occur between the driving field and the resulting polarization. This makes polarization α complex and dependent on frequency of the applied field.

The average induced dipole moment per molecule P_{av} is the sum of all the contributing polarization mechanisms in terms of the local electric field acting on the individual molecules.

$$P_{av} = \alpha_e E' + \alpha_i E' + \alpha_d E'$$

Eq-2.7: Average dipole moment [22]

Interfacial polarization cannot be directly added to P_{av} like other polarization mechanisms because it occurs at the interfaces and cannot be put into an average polarization per molecule in bulk [22]. The dielectric constant under ionic and electronic polarizations is given by the famous Clausius-Mosotti equation,

$$\frac{\varepsilon_r - 1}{\varepsilon_r + 2} = \frac{1}{3\varepsilon_o}[N_e \alpha_e + N_i \alpha_i]$$

Eq-2.8: Clausius-Mosotti equation [22], [23]

Where N_e is the number of ions or atoms exhibiting electronic polarization and N_i is the number of ion pairs per unit volume. In the case of materials with orientation polarization, we cannot use local field approximation. That is, the Clausius-Mosotti equation does not work with dipolar dielec-trics and the calculation of the local field is complicated. The response of normal materials to external fields generally depends on the frequency of the field. This frequency dependence reflects the fact that a material's polarization does not respond instantaneously to an applied field. For this reason permittivity is often treated as a complex function of the frequency of the applied field ω. However, in the narrow frequency ranges that are often studied in practice, the permittivity can be approximated as frequency independent or by model functions.

Modeling relative permittivity for homogenous materials by itself is a fairly complex process involving intense computation of electric fields. The platinum sensors after FIB

depo-sition will likely have an active target specific layer which would be subjected to the ambient medium containing the target molecules. Each of the components of the sensor and all the individual elements involved in the reaction at the sensor will polarize differently and will contribute to the overall change in the measured dielectric constant. It is not possible to easily develop a unifying model that fits all these parameters to predict or estimate the expected change in relative permittivity. It would be more practical to measure the individual response of the reactants on the chip and then determine a baseline for the reaction.

2.1. Detection principle of organophosphate neurotoxins

The detection mechanism exploits the published observation of our research collaborator, Dr. Pamela Lein at CROET (Center for Research on Occupational and Environmental Toxicology) at OHSU. The groups' research indicates that extremely low concentrations (fM to pM range) of organophosphate (OP) pesticides can cause a significant increase in primary neuronal cell cultures of intracellular levels of the phosphorylated form of a protein known as Ca2+/cAMP Response Element Binding Protein (CREB) [24]. Thus OP-induced pCREB represents one of the most sensitive biomarkers of OP exposure identified thus far.

CREB functions as a transcription factor, regulating transcription of genes responsive to increased calcium and cAMP. Binding of CREB to DNA is controlled by enzymatic phosphor-rylation and dephosphorylation of CREB at serine-133 [25]. The biological consequences of increased pCREB in OP treated neurons are not known. Increased pCREB may underlie the neurotoxicity of these compounds by altering the complex regulation of CREB transcriptional activity that is critical for neurodevelopment and cognitive function. Alternatively, since CREB phosphorylation is critical in the survival of neurons [26], OP-induced increases in pCREB may be neuroprotective and part of a generalized response to cellular stress. Whether the OP-induced phosphorylation of CREB is deleterious or protective to neurons, this biochemical change may be a sensitive biomarker of OPs.

2.1.1. Preliminary investigation performed at CROET-OHSU

Very low levels of OP pesticides and OP nerve agents increase levels of pCREB in primary neuronal cell cultures. An acute exposure of primary cultures of cortical neurons derived from prenatal rat brain to the prototype OP pesticide, chlorpyrifos (CPF) or its oxon metabolite, chlorpyrifos-oxon (CPFO) causes levels of phosphorylated CREB (pCREB) to increase by as much as 400% relative to cultures treated with vehicle control. Robust increases in pCREB were observed using CPF concentrations as low as 30 fM in the absence of any changes in total CREB or the cytoskeletal protein α-tubulin [24].

Schuh et al. [24] have performed representative immunoblots of lysates from primary cortical neurons (cultured for 72 hours) that were exposed to CPF or CPFO for 1 hour. They immunoblotted proteins separated by SDS PAGE with antibodies that specifically recognize CREB phosphorylated at Ser133, α-tubulin, or both phosphorylated and non-phosphorylated CREB (total CREB). Densitometric analyses of blots expressed as a percentage of the control value on each gel were performed. Data collected by them indicate that exposure to CPF or CPFO increased pCREB as much as 400% over control levels. Mean optical densities from additional studies of cortical cultures exposed to lower doses of CPF (0-10 nM) or CPFO (0-10 pM) indicate that the concentration that elicits half-maximal response (EC_{50}) is approximately 0.06 nM for CPF and < 30 fM for CPFO [24]. CPF and CPFO similarly upregulated pCREB levels in primary hippocampal cultures, and other OP pesticides, including paraoxon, malathion, and diisopropylfluorophosphate (DFP) also increase levels of pCREB in neurons with approximate EC_{50} values of 30 fM, 1pM and 2 pM respectively [24]. These observations suggest that increased phosphorylation of CREB can be utilized as a biomarker of OP exposure.

2.1.2. CREBtide as a biosensor substrate for detecting agents that phosphorylate CREB

CREBtide is a synthetic peptide that contains the consensus sequence for the Ser-133 phosphorylation site of CREB. It is widely used in biochemical studies of enzymatic pathways that phosphorylate CREB. Because of these characteristics, it is better suited for

use in a biosensor than CREB. Preliminary data from studies conducted at CROET-OHSU indicate that CREBtide is robustly phosphorylated in the presence of the enzyme protein kinase A (PKA) and the phosphate donor ATP (Figure 2.4). Inclusion of CPF in the reaction mixture did not alter phosphorylation of CREBtide in the presence of PKA (Figure 2.4), consistent with the hypothesis that OPs increase levels of pCREB via direct phosphorylation of CREB. Interestingly, in the absence of PKA, the addition of CPF decreased the amount of radioactive phosphate incorporated into CREBtide, suggesting that CPF is competing with ^{32}P-ATP in phosphorylating CREBtide (Figure 2.4). The response is concentration-dependent and significantly different from vehicle control at the highest concentration tested. The fact that the metabolic pathways required for generation of the more potent oxon metabolite CPFO are not present in the reaction mixture may explain why the pesticide did not cause a more robust inhibition of radiolabeling of CREBtide.

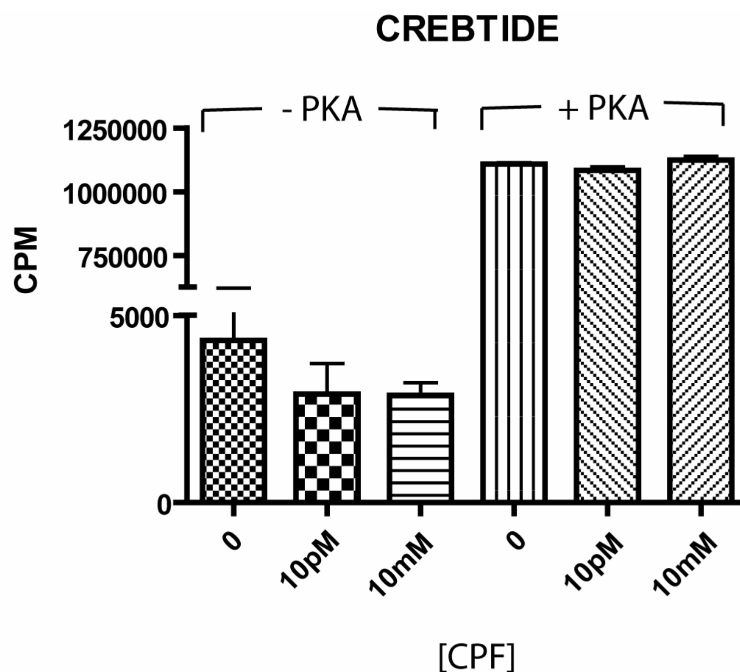


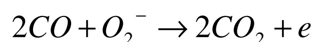
Figure 2.4: Effects of CPF on phosphorylation of CREBtide. CPF was added to the reaction mixture at 10pM or 10mM, CPF in reaction mixture in the presence of ^{32}P-ATP in the absence or presence of protein kinase A (PKA). Phosphorylation was determined as the incorporation of ^{32}P label into CREBtide. Data presented as the mean ± SEM (N = 4 per condition). [CROET-OHSU]

The concept behind the on chip electrical detection technique is that the phosphorylated CREBtide will polarize differently than un-phosphorylated CREBtide. If this change in polarization or permittivity is significant and within the measurable range of the on chip CMOS detection circuit then this would be a direct measure of the phosphorylated CREBtide which in turn is a function of OP concentration. The individual components of the reaction mixture need to be analyzed separately to understand their dielectric constant contributions and a baseline reading needs to be established for un-phosphorylated CREBtide to be able to discriminate the change caused by phosphorylation. The development goal of this work is to amplify the detectability of the reaction by immobilizing the CREBtide on the surfaces of the capacitor sensors. This would localize the reaction at the sensor sites and increase the change in dielectric constant between the plates.

2.2. Carbon Monoxide gas sensor detection principle

A wide variety of solid state sensors are available for the detection of carbon monoxide (CO). Solid state gas sensors are usually operated at 150 to 400 ºC to decrease absorption time and to increase sensitivity. Typical sensor design would include a heating element below the active sensing device connected to a heater control. In one design example, Lilin Li et al. [27] demonstrates a simple resistive platinum film CO sensor without a selective layer sensitive to 50 to 1000ppm CO operating at 80 to 150 ºC. She also observes oscillatory and non-oscillatory changes in resistance of the thin film Platinum resistor. Both the amplitude and period were observed to increase with the increase in CO concentration. A wide variety of materials have been researched that are sensitive to CO gas of which tin oxide based CO sensors have been extensively developed as it is cheap, reliable and convenient for domestic applications [28]. Rajnish Sharma et al. [29] demonstrate the preparation, electrical and surface characterization of Cu doped tin dioxide thin-films for highly selective CO sensor operating at 270 to 320 ºC. He also observes that the sensitivity and the response time improve with increasing operating temperature of the sensor. Another tin oxide based CO sensor with low power consumption has been reported by Kyoung Ran Han et al. [30] who shows CO detection capabilities of tin oxide at low

temperatures and also reports output amplitude oscillations and relates it to the surface temperature of the sensor. It is interesting to note that similar output oscillatory behavior was demonstrated by the simple platinum film carbon monoxide sensor without any selective layer reported by Lilin Li et al. [27]. All of the referenced tin oxide based CO sensors measure the conductance of the sensor as the sensory output. When CO gas is introduced, the conductance of the sensor increases due to the CO molecules being adsorbed to the sensor surface and then reacting with the negative oxygen ions to produce electrons [31].



$$2CO + O_2^- \rightarrow 2CO_2 + e$$

Eq-2.9: Tin oxide CO sensor reaction [31]

All of these properties of tin oxide render it an excellent material for the detection of very low levels of carbon monoxide. Nano particles of tin oxide in suspension have been used to develop a novel low power, low temperature CO gas sensor, which was reported to be stable and sensitive to as low as 10ppm concentration of CO [32]. In this method, a suspension of tin oxide colloid is dropped onto sensing electrodes along with buried heater electrodes, which then heat-treat the tin oxide to temperatures close to 500 ºC.

When the CO molecules react with the tin oxide surface and produce electrons [31], the conductivity of the bulk material increases. This can also be visualized in terms of capacitance or relative permittivity. As the material becomes more conductive, its relative permittivity decreases and becomes less of a capacitor. So this increase in conductivity of the tin oxide sensor material, when subjected to carbon monoxide would manifest as reduction in capacitance, if a capacitor is built with tin oxide as the dielectric material between the capacitor plates. The FIB would be used to deposit parallel plate capacitors on the surface of the proposed chip, and tin oxide dispersed between the plates using thermal evaporation techniques, e-beam evaporation or simple dispersion of tin oxide suspension (Figure 2.5). In the presence of CO gas, the baseline capacitance of the sensor should decrease in relation to the concentration of the gas, which would be detected and converted to an electrical signal by the detection circuit.

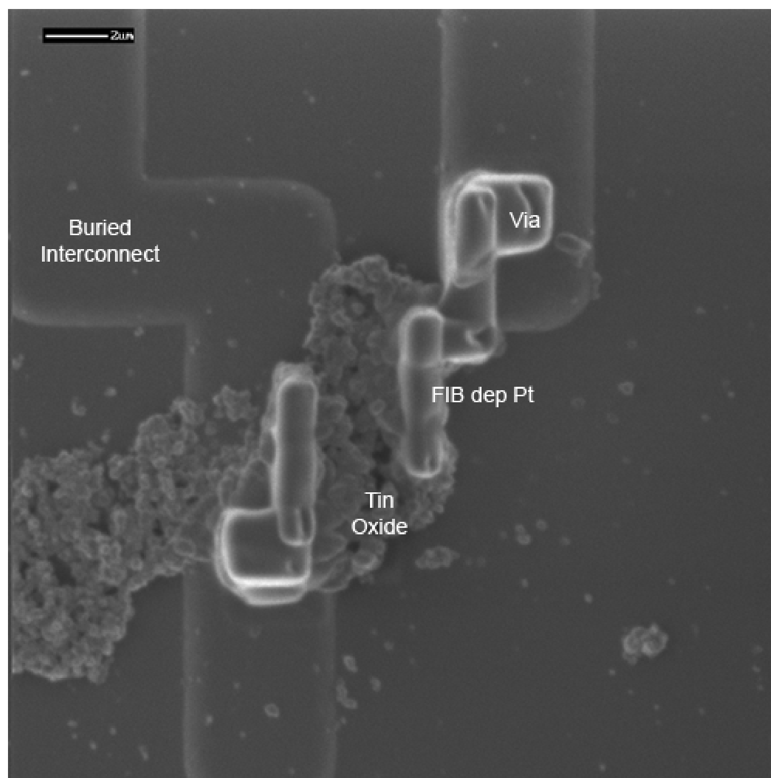


Figure 2.5: Example tin oxide CO sensor on a chip with FIB deposited platinum electrodes.

2.3. Neuroprotective gene detection - Research on the reduction of neuronal damage during stroke

CART [19], or *cocaine- and amphetamine-regulated transcript*, was identified as a neuroprotective gene using DNA microarrays to determine genes differentially regulated by estrogen in brain under ischemic conditions. Preliminary work done by Nabil Alkayed et al. (Anesthesiology and Peri-Operative Medicine - OHSU) determined that female animals sustain smaller brain injuries after experimental stroke compared to age-matched males [33], and that female protection is abolished by the removal of endogenous female hormones[34] and restored by estrogen replacement [35]. They analyzed mRNA expression in sub-dissected cerebral cortex after middle cerebral artery (MCA) occlusion (MCAO) and compared levels of expression between estradiol-treated and untreated ovariectomized

female rats. They also identified a transcript, *cocaine and amphetamine-regulated transcript* (CART) that is highly regulated by estradiol in the cerebral cortex after MCAO. CART mRNA encodes a secretory neuropeptide with diverse biological actions and multiple sites of expression in the brain [19]. They subsequently confirmed their initial microarray observation that CART is upregulated by estradiol after MCAO using standard techniques of Northern and Western blotting and demonstrated for the first time that CART peptide is protective against neuronal cell death in culture and more recently against ischemic brain damage after MCAO in mice. CART functions in the brain continue to be investigated and remain largely unknown. Monitoring CART would play an important role in early detection of stroke. Anti-CART peptide antibody has been used in standard Western blot to quantify CART neuropeptide [20].

The on chip detection principle would be similar to that of the Organophosphate detection. The detection principle would be based on antigen antibody bonding. When the Anti-CART peptide antibody bonds with the CART it would likely polarize differently with a different dipole moment than the individual components themselves. Individual components, in this case CART peptide and Anti-CART peptide antibody need to be tested for their characteristic relative permittivity to establish a baseline before the reaction product can be quantified.

3. FIB Sensor Fabrication

The FIB workstation has been prevalently used in the micro-electronics industry for micro-fabrication, post fabrication editing and debugging. The use of the FIB workstation for fabricating the sensors shortens the development period and allows for rapid prototyping of sensor geometries. The FIB workstation uses accelerated gallium ions to mill or deposit materials (in the presence of precursor gasses) on the micron and sub-micron scales. It serves as a rapid mask-less and resistless design modification and test tool. It has the ability to cut metal interconnects, drill vias, deposit oxide and deposit metal interconnects without lithography. The nano, submicron and micron scale machining and micro forming capability of the FIB will also allow extremely high density sensor arrays. The FIB workstation used is FEI FIB 610 and is setup to deposit Platinum metal. Pt sensors can be fabricated in a variety of designs on the same chip and then individually tested for performance when wired to one of the detection circuits below the passivation layer. Figure 3.1 shows the FEI FIB 610 workstation.

Figure 3.1: Digital photograph of FEI FIB 610 workstation.

3.1. Fabrication Process

Initially, before the fabrication of platinum sensors, test cross sections are made on the prefabricated die to determine the layer thickness. This is done by defining a mill area that includes the top metal at the sensor sites. FIB produced cross sections of two of the fabricated chips is shown in Figure 3.2.

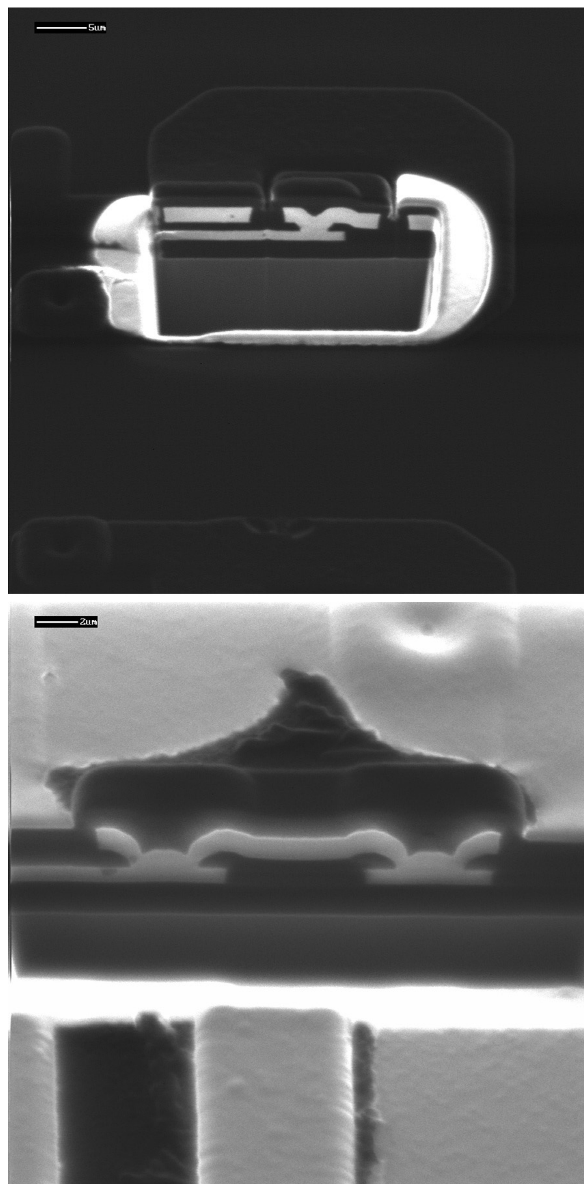


Figure 3.2: Secondary electron images of FIB cross sectional areas at 45 degrees tilt.

The thickness of the passivation layer and the metal layers vary slightly between fabrication runs. The oxy-nitride passivation layer thickness was found to be between 0.6μm to 0.8μm. Figure 3.3 shows a typical FIB fabricated parallel plate gang capacitor sensor.

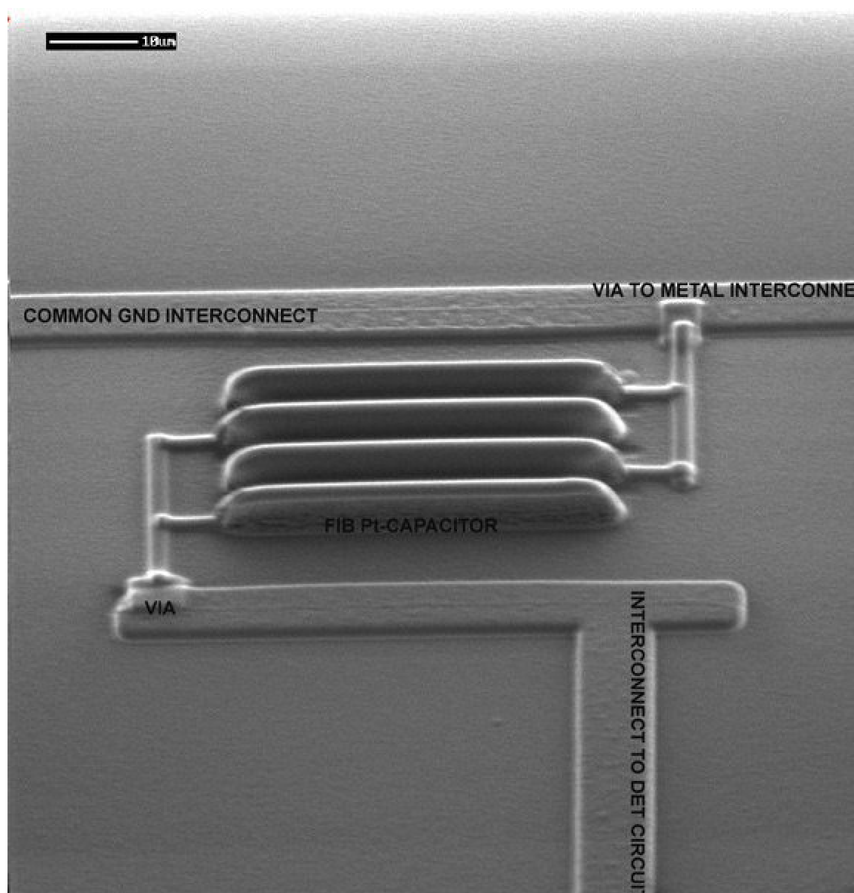


Figure 3.3: Secondary electron image of FIB fabricated parallel plate gang capacitor sensor.

The capacitor plates are made by depositing platinum with the desired length, width and thickness. Platinum was typically deposited using 1100ºA spot size (Ga beam size) at 25KV accelerating voltage. Next Vias are made by milling 2μm×2μm holes on the desired interconnect to expose the buried metal and then platinum is deposited into the milled void to establish connection to the buried metal. End point detection (EPD) signal was used while milling the Vias. When the gallium ion beam is incident on a sample, a small current in the pico-amp scale is induced and flows through the sample stage. This current is dependent

on the material being milled and is higher for metals as opposed to insulating layers. This current is detected and plotted on a graph as the milling progresses and is called the EPD graph. Also the secondary electron production for metal is higher than that of insulating layers and registers as a bright region once the milling depth reaches the underlying metal. Both the EPD and the secondary electron image were used in determining the end point of milling while making the Vias. Once the buried metal is exposed, platinum is deposited to fill the milled hole and establish electrical connection to the buried metal. Platinum traces are deposited from these vias to the previously deposited capacitor plates to complete the electrical connection between the detection circuits and the platinum sensors. Examples of FIB micro fabricated sensor structures are shown in Figures 3.4 and 3.5.

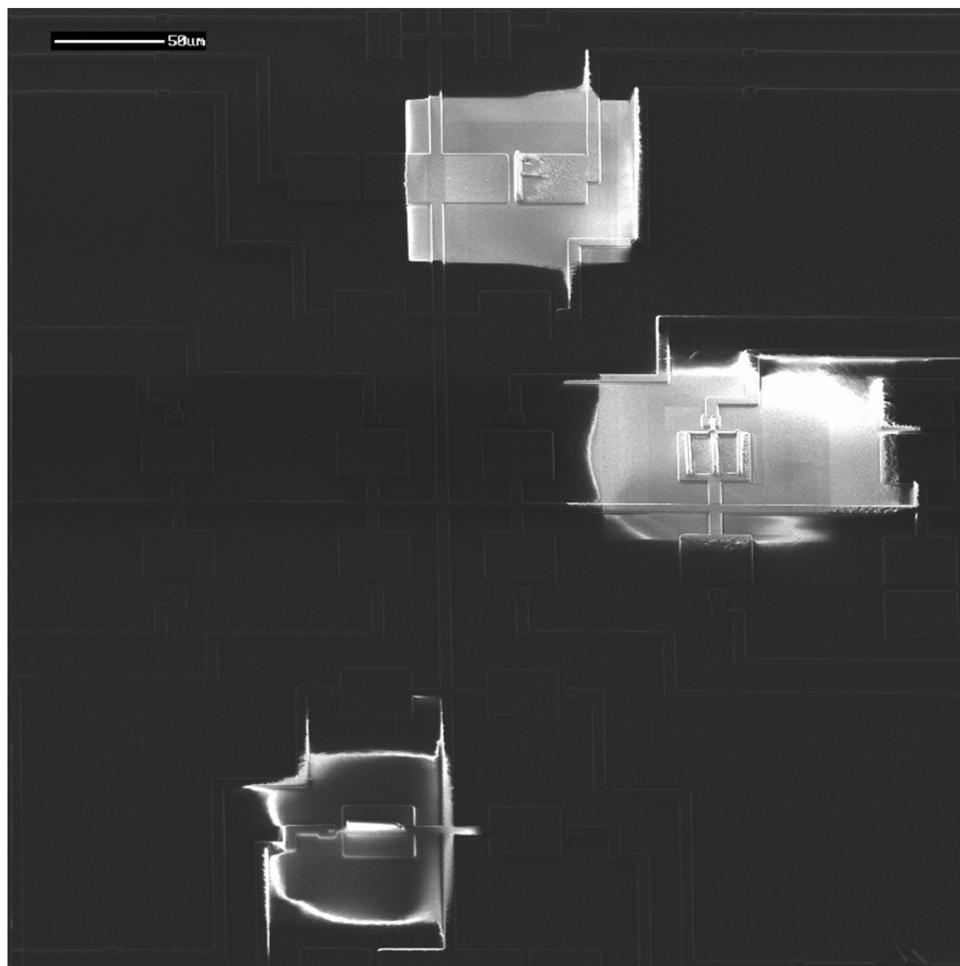


Figure 3.4: Secondary electron image of multiple FIB fabricated sensor structures on the same chip.

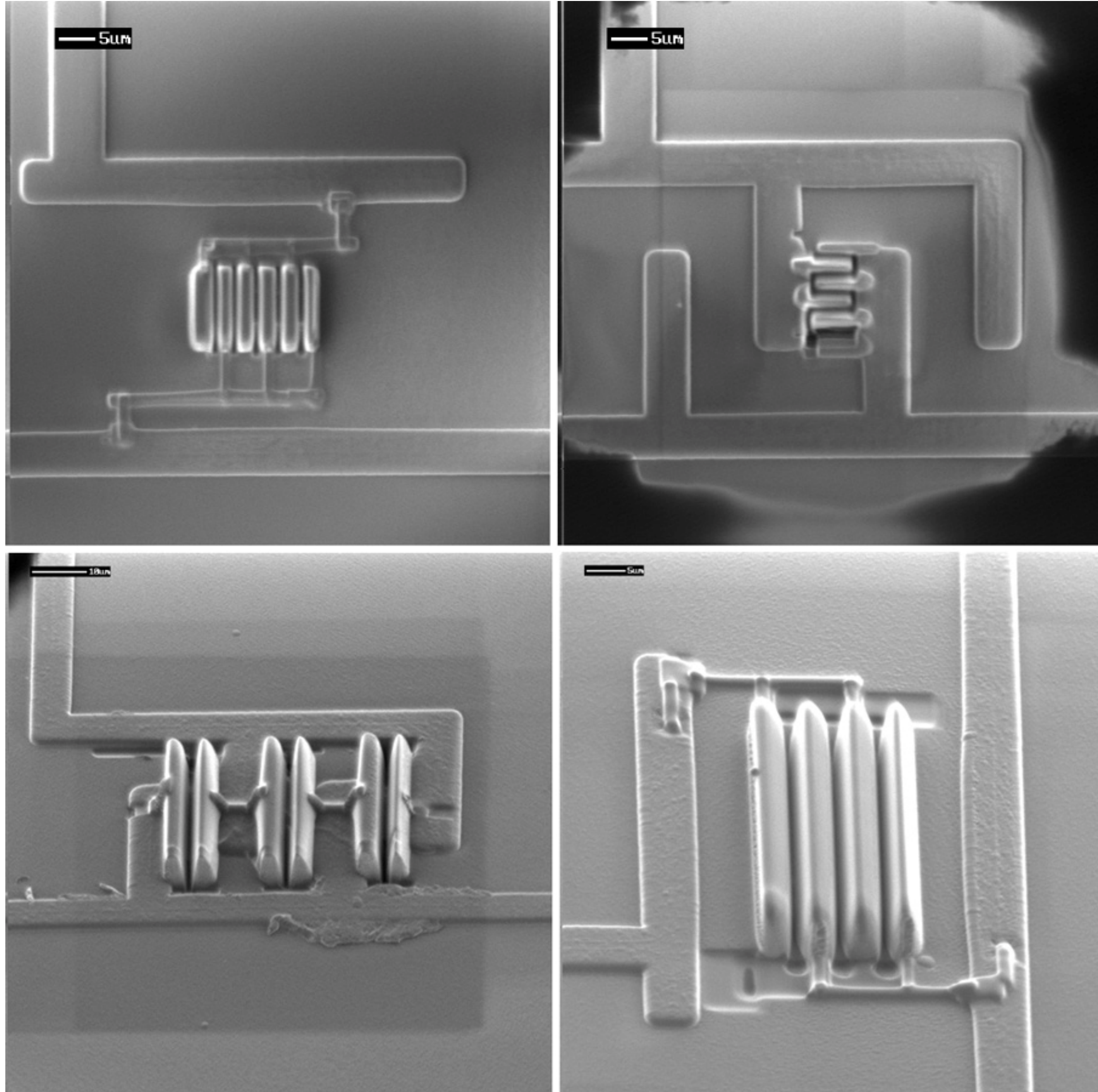


Figure 3.5: Secondary electron images of various FIB fabricated sensor structures.

3.2. Sensor size

The size of the capacitor sensors is dependent on the capability of the detection circuit to measure small changes in capacitance. As the sensor size gets smaller, the complexity of the detection circuit increases. It can be visualized that a larger sensor structure in general would increase sensitivity. However, increasing the sensor size would also increase the FIB fabrication time. For example, to fabricate a gang capacitance sensor

structure that has an air capacitance of 100ff, with a gap of 2μm between adjacent plates and a height of 3μm per plate would require fifty, 153μm long plates as per Eq-3.1

$$C = (n-1)\frac{\varepsilon_o \varepsilon_r A}{d} \text{ (Farads)}$$

Eq-3.1: Sensor capacitance

n = number of plates, ε_o = permittivity of free space (8.854 × 10-12 F/m), ε_r = dielectric constant (k) of material between the plates (Air = 1), A= plate area, d = distance between the plates.

This would result in a sensor structure that is 150μm×153μm and would require more than 5 hours to fabricate, which is not practical. Also, increasing the sensor size would decrease the array density per chip. So, smaller sensor structures with baseline air capacitances typically less than 5ff were implemented, whose fabrication periods were less than 20 minutes per sensor. The capacitor plates in the sensor structures shown in Figures 3.3 and 3.4 were 10μm to 20μm long and 1μm to 4μm tall. The average time to deposit one such sensor structure using the FIB was 15 minutes, which enables the fabrication of a whole array within reasonable time.

In a capacitor based sensing system, sensitivity is defined by the gain of the detection circuit. Higher gain systems generally are limited by the range of input capacitances that can be measured without saturation. For example, consider a detection circuit that has a gain of 20mV per femto farad with a relatively large sensor structure with air capacitance of 20ff. If this sensor is exposed to an analyte in a liquid medium with dielectric constant of 80, the absolute value of the sensor becomes 1600ff. This means the output of the detection circuit should be 32 V for 20mV/ff gain, which is not practically possible because of power supply limitations defined by the integrated technology in use. Typical power supply for a 1.5μm CMOS process is 5 V and that for a 0.35 μm process is 3.3 V. As the fabrication technology gets smaller the maximum supply voltage than can be used generally reduces in compliance with the break down voltages of the devices. So smaller sensor structures with air

capacitances ranging from 1ff to 5ff was designed for use with liquid test mediums. Larger sensor structures can be used to improve sensitivity while analyzing gaseous targets.

Sensitivity of the system for any particular target molecule can be improved by treating multiple sensor structures with the same target selective material. This would increase the probability of the event of target molecule and selective material interaction. Fabricating the sensors with the FIB provides the flexibility of modifying or increasing the sensor sizes at the sacrifice of fabrication time, as the application demands.

4. Circuit Design

To take advantage of the change in capacitance to measure or detect concentration variations of target molecules requires a detecting circuit sensitive to very small changes in capacitance. The size of the sensors is interdependent on the capability of the detecting mechanism to sense small changes. As the sensor gets smaller, the complexity of the detecting mechanism increases. The standalone air capacitance of the sensors fabricated using the FIB workstation is very small and are in the range of 0.5ff to 5ff. If conventional probes and instrumentation were to be used for measuring these sensors, the parasitic capacitances associated with the probes, interconnects and wires used between the detecting equipment and the sensor would overwhelm the capacitance of the sensor in use. Even with the best probes and interconnects the incurred parasitic capacitances are generally greater than 1pf and would require bulky and expensive instrumentation to offset this parasitic influence. For sensitivity and good dynamic range, the sensors must be in the pico-farad scale and produce changes in the range of pico farads for conventional instruments to measure with ease. To fabricate sensors with baseline air capacitances greater than 1pf would generally require a large area, and this would greatly reduce the area density if an array of sensors were to be constructed on an integrated chip. Hence, it is mandatory to have the sensing circuit at close proximity to the sensors with minimal parasitic capacitance influence. A viable approach would be to build the sensing circuit on chip along with the sensors.

The detection circuit should be designed to be sensitive to sub-femto farad changes and also have a range of sensitivities to allow for measuring large swings in capacitances. It should also have a small footprint and have low power consumption because each sensor in the array has to be connected to its individual detection circuit, and thereby deciding the number of sensor-detector circuit pair that can be incorporated on chip. The designed circuit

must also have good immunity to noise and should be able to compensate for ambient thermal and field variations.

Four generations of circuits with sites to accept sensors have been designed and fabricated. All chips were fabricated using AMI 1.5 micron CMOS process with the help of MOSIS educational program. MOSIS is a low-cost prototyping and small-volume production service for VLSI circuit development. AMI 1.5µm process is a 2-metal, 2-poly CMOS process. Even though the 1.5µm process is an older process it is well suited for prototyping applications because of its low cost. All fabricated dies were packaged in DIP-40 ceramic package and were not hermetically sealed. The wire bonded 'Si' die was accessible from top, refer Figure 4.1. Circuit design, simulation and mask layout design was performed using Mentor Graphic's ASIC (Application Specific Integrated Circuit) design kit (ADK).

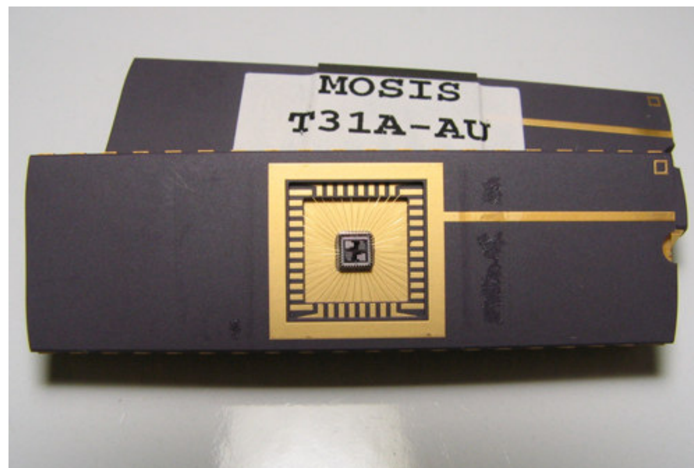


Figure 4.1: Fabricated chip with top access to die.

4.1. First Generation circuit design

The detection circuitry for the first generation is a capacitance to frequency converter [36]. The output frequency of the detection circuit is inversely proportional to the absolute capacitance connected i.e. the capacitance of the sensor along with the parasitic capacitance of the metal interconnect that connects the sensor to the detection circuit. The circuit consists of a Schmitt trigger which toggles a current source charging and discharging

the sensor cap in a closed loop making a self sustained oscillator (Figure 4.2). Output of the circuit is a square wave whose time period depends on the value of sensor capacitance.

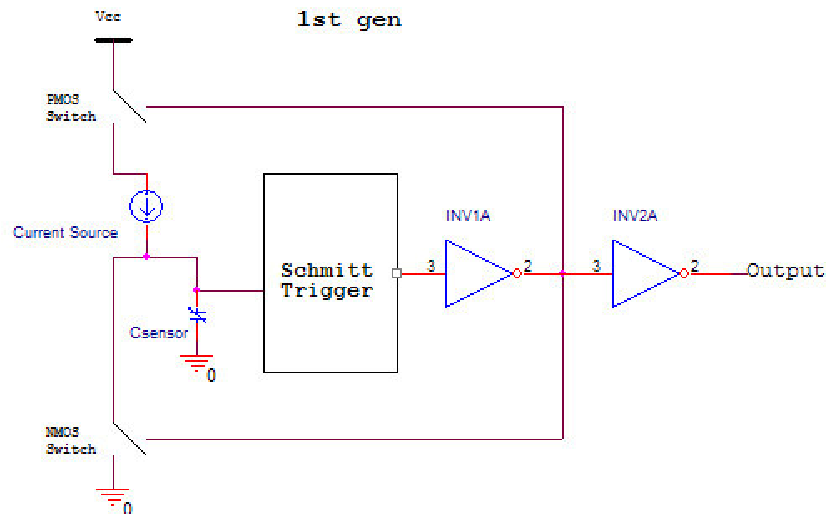


Figure 4.2: Capacitance to frequency converter.

Initially let's assume that the PMOS switch is on and the NMOS switch is off. The fixed current source begins to charge the sensor capacitor. Once the voltage across the sensor capacitor reaches the upper threshold voltage (V_{SH}) of the Schmitt trigger, the output of the Schmitt trigger goes low. This turns off the PMOS switch and turns on the NMOS switch causing the sensor capacitor to discharge. Once the voltage across the sensor capacitor reaches the lower threshold voltage (V_{SL}) of the Schmitt trigger, the output of the Schmitt trigger toggles to high. The process of charging the capacitor repeats, thereby sustaining self oscillation whose frequency depends on the value of the sensor capacitor. The larger the sensor capacitance, the longer it takes to charge and discharge. Hence, the output of this detection circuit is a square wave pulse whose frequency is inversely proportional to the capacitance of the sensor and its associated parasitics.

The schematic for the CMOS circuit, designed using Mentor Graphics ASIC design kit, is shown in Figure 4.3. The circuit was designed in the module or unit-cell approach, where the design was split into smaller functional units and separate mask layouts for each individual block was created. The layout height of the unit cells were kept constant so they line up when grouped to form the complete layout. This method allows for easy future

modifications of the circuit, making changes only to the necessary blocks and its associated layout and not having to redo the lithography mask for the entire design.

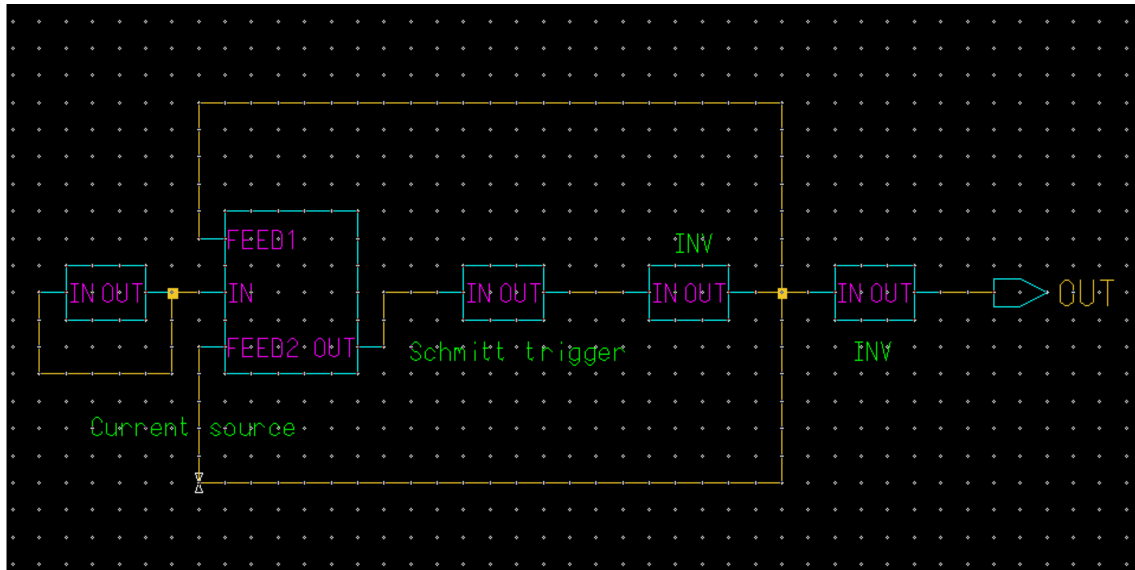


Figure 4.3: Block schematic of 1st generation unit detection circuit.

The constant current source consists of a minimum sized inverter coupled with a current mirror which can be switched by the Schmitt trigger. The inverter with the input and output connected together acts like a voltage divider network and current flowing through this segment can be calculated using drain current equation for a transistor in saturation. For the AMI 1.5µm process with minimum sized transistors, the current through P1 and N1 was calculated to be 170µA. This current will be mirrored across by transistors P2 and N2. The mirrored current can be scaled up or down by the sizing of N2 and P2, as required. The lower the current, the longer it takes to charge and discharge the sensor capacitor to the set thresholds of the Schmitt trigger. Since the sensor capacitance is really small, it would charge and discharge very rapidly. To keep the operating frequency low, small charging currents are desired. Switching transistors P3 and N3 charge and discharge the sensor capacitor depending on the output state of the Schmitt trigger circuit. In order to make sure that the circuit starts in a desirable state and sustain oscillation, transistors N4 and N5 act like high resistance paths that would slowly charge or discharge the sensor capacitor forcing the Schmitt trigger to toggle its output.

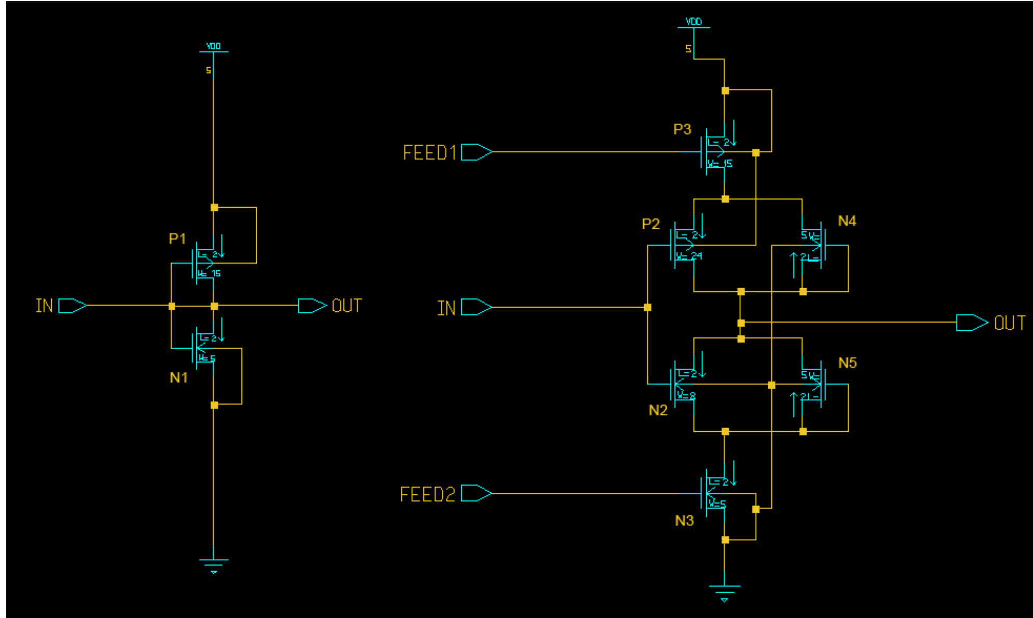


Figure 4.4: Circuit schematic of (charging) constant current source for 1st generation detection circuit.

The basic schematic of a Schmitt trigger is shown in Figure 4.5. The higher switching point V_{SH} for the Schmitt trigger is determined by the sizing of transistors N1 and N3 and the lower switching point V_{SL} by P2 and P3 and is governed by the following transconduction relation [37].

$$\frac{\beta_{N1}}{\beta_{N3}} = \left[\frac{VDD - V_{SH}}{V_{SH} - V_{THn}}\right]^2 = \frac{KP_n \frac{W_{N1}}{L_{N1}}}{KP_n \frac{W_{N3}}{L_{N3}}} = \frac{W_{N1}L_{N3}}{W_{N3}L_{N1}}$$

$$\frac{\beta_{P2}}{\beta_{P3}} = \left[\frac{V_{SL}}{VDD - V_{SL} - V_{THp}}\right]^2 = \frac{KP_p \frac{W_{P2}}{L_{P2}}}{KP_p \frac{W_{P3}}{L_{P3}}} = \frac{W_{P2}L_{P3}}{W_{P3}L_{P2}}$$

Eq-4.1: Schmitt trigger transconduction and switching point relation [37].

Schmitt trigger with transistor sizes designed for V_{SL} = 1V, V_{SH} = 4V is shown in Figure 4.5 and its corresponding transfer function is shown in Figure 4.6. To keep operating frequency lower, wider range between the switching points is desired.

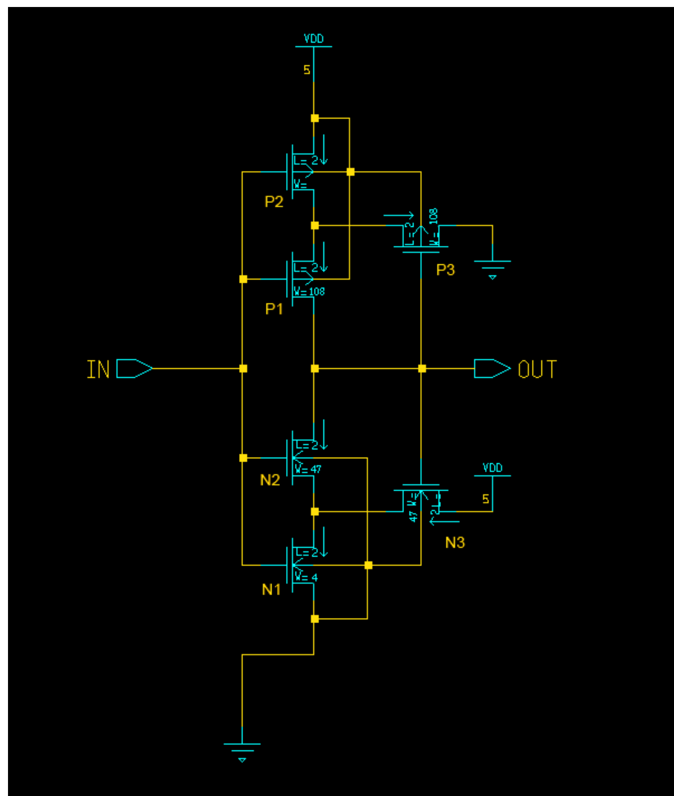


Figure 4.5: Circuit schematic of typical Schmitt trigger for 1st generation detection circuit.

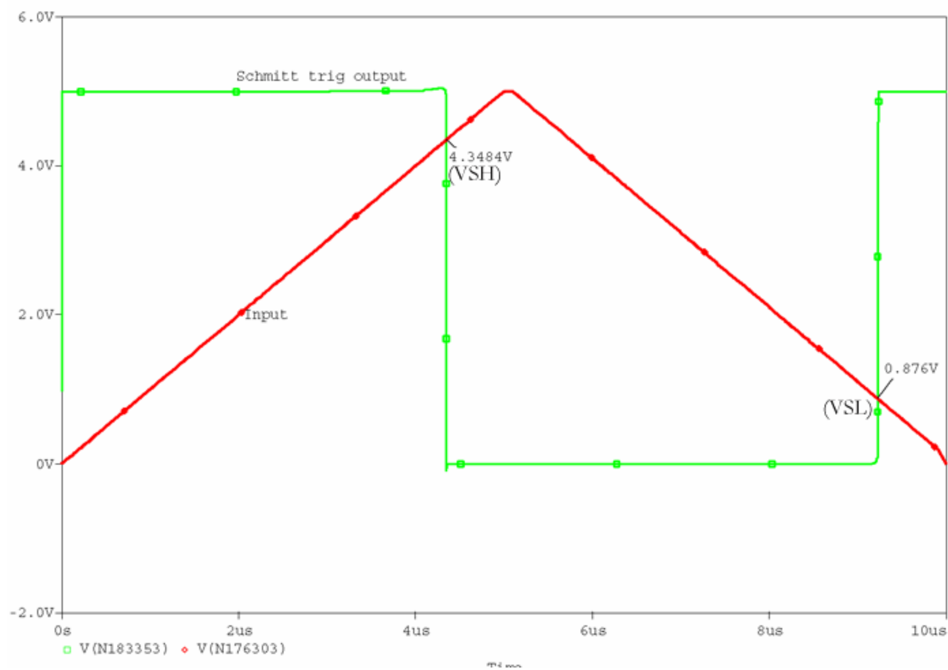


Figure 4.6: Transfer function of typical Schmitt trigger for 1st generation detection circuit.

A complete circuit schematic with all the components is shown in Figure 4.7. Typical frequency response of the detection circuit with change in sensor capacitance is shown in Figure 4.8. The two curves on the graph in Figure 4.8 correspond to two different charging currents (85μA and 40μA) set by the current source. The charging current was altered by changing the ratio of the transistors P2 and N2 in Figure 4.4. The larger of the two currents (85μA) charges and discharges the simulated sensor capacitor more rapidly. Hence the voltage across the sensor capacitor reaches the set points of the Schmitt trigger more rapidly, resulting in a higher operating frequency than the 40μA charging current. Further, the response behavior of the circuit can be modified by altering the set points of the Schmitt trigger. Larger ranges between V_{SH} and V_{SL} are desired for low frequency oscillations and were generally designed with 4V (V_{SH}) and 1V (V_{SL}) respectively. The total current drawn by a typical 1st generation detection circuit connected to a 100ff sensor capacitance was determined to be 630μA. With 5V power supply, the total power consumption of each individual unit in operation would be 3.15mW.

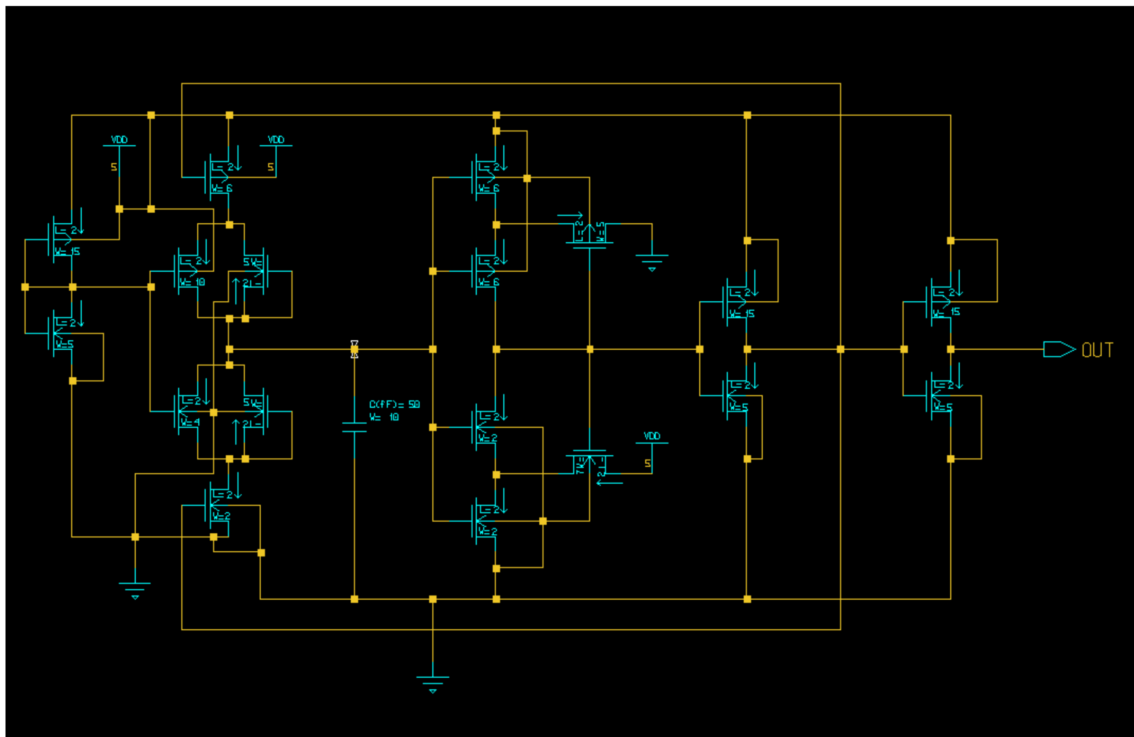


Figure 4.7: Complete circuit schematic of 1st generation detection circuit.

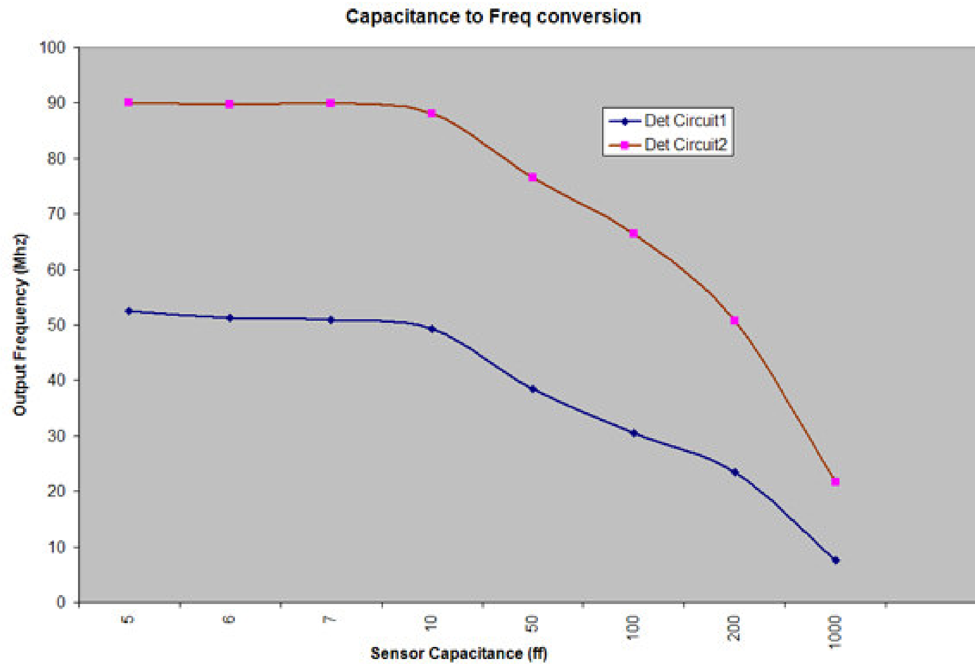


Figure 4.8: Output frequency vs. sensor capacitance plots. Det circuit 1 has a charging current of 40μA. Det circuit 2 has charging current of 85μA.

4.2. First Generation Mask layout design

Unit cell layout for individual components and that of the whole die was designed using Mentor Graphic's IC station. The total die area available for fabrication using AMI 1.5μm process through MOSIS educational program is 2.2mm × 2.2mm. All cells were designed using MOSIS SCMOS design rules and eventually scaled with a λ (scaling factor) of 0.8 microns. Using scalable CMOS rules allows for the layouts to be scaled to many of the smaller and advanced fabrication processes available without having to redo the whole layout. Figure 4.9 shows the layout of a complete detection circuit having a 40μA current source which was designed using the modular unit cells shown in Figure 4.10. Care was taken in designing the layout to minimize the parasitic capacitance of the metal interconnects that connect the sensor metal to the current source and the Schmitt trigger. Figures 4.11 and 4.12 show the layouts of a detection circuit with 85μA current source, the area of which is slightly larger than that of the 40μA circuit because of the larger sized transistors.

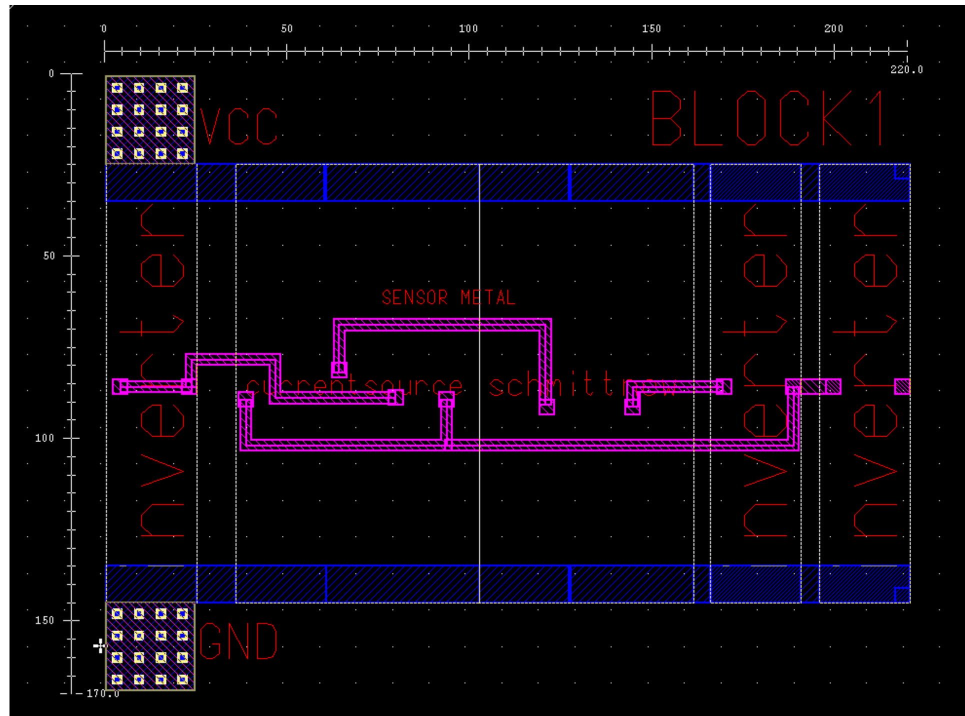


Figure 4.9: Mask layout of detection circuit (1st gen) with 40μA charging current. Area of layout = 220λ× 170λ or 176μm×136μm.

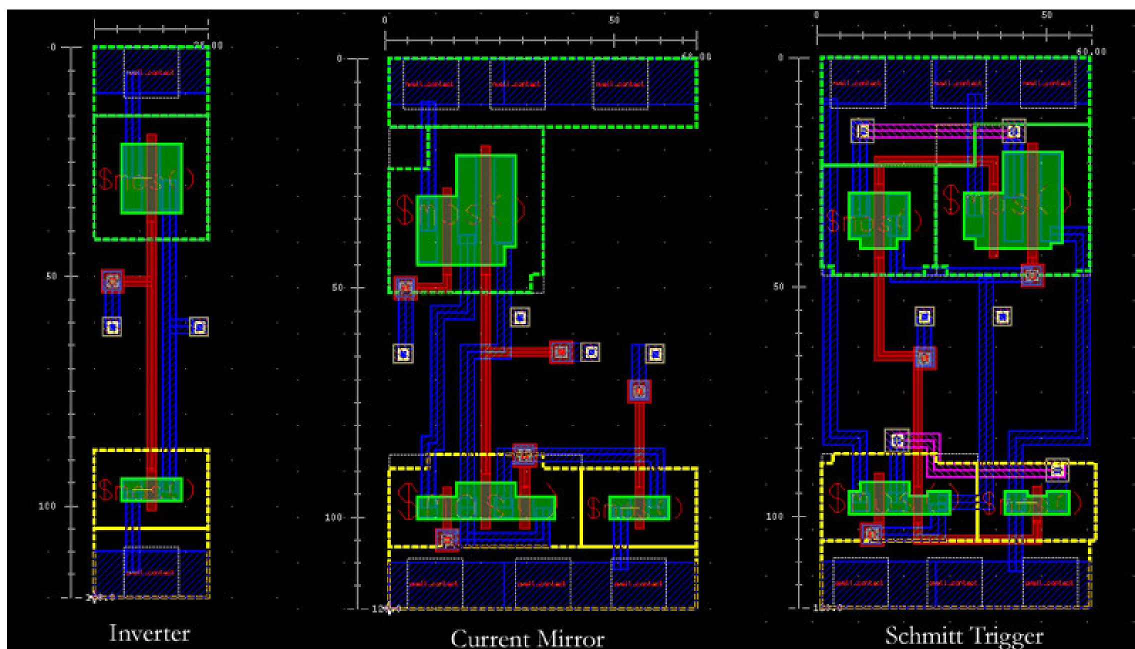


Figure 4.10: Mask layout of individual components for detection circuit (1st gen) with 40μA charging current.

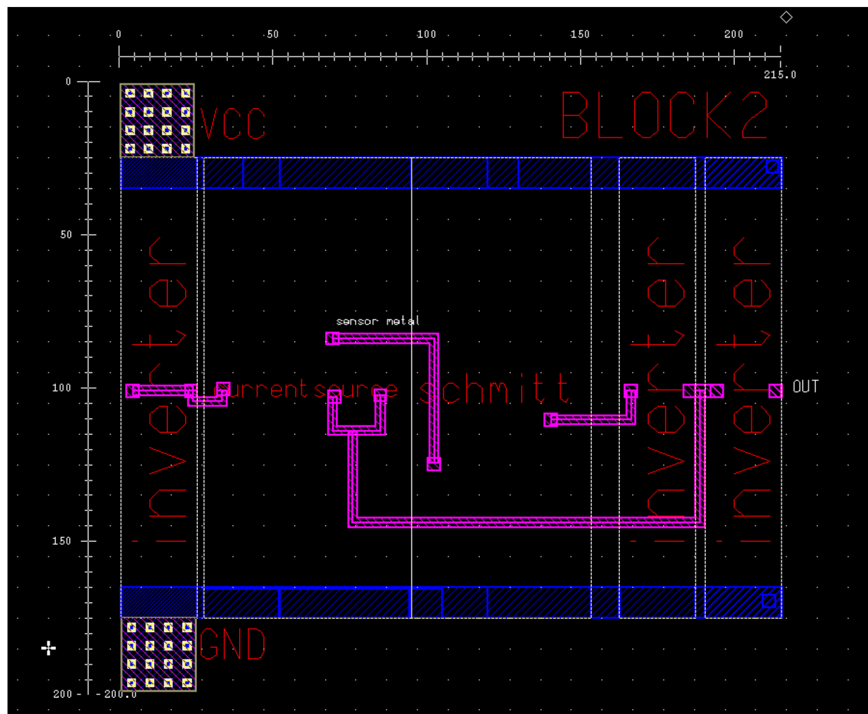


Figure 4.11: Mask layout of detection circuit (1st gen) with 85μA charging current. Area of layout = 215λ ×200λ or 172μm×160μm.

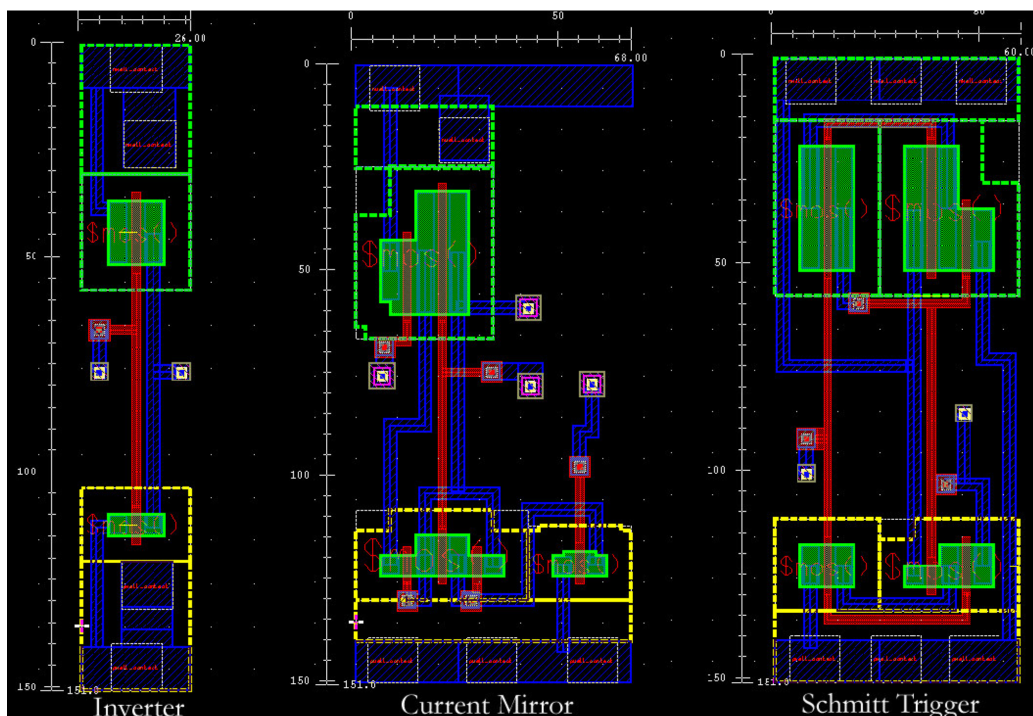


Figure 4.12: Mask layout of individual components for detection circuit (1st gen) with 85μA charging current.

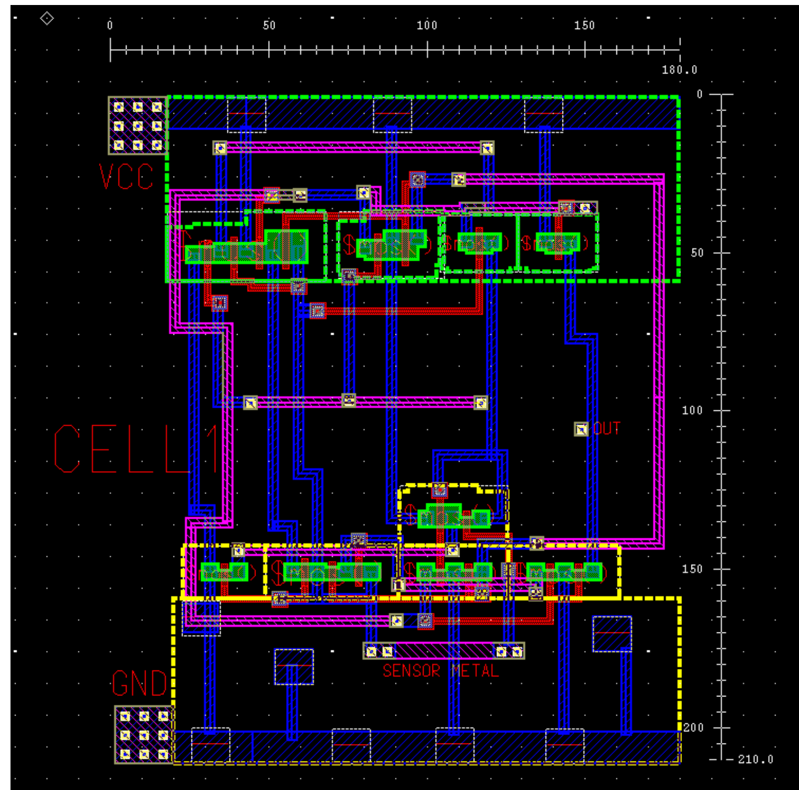


Figure 4.13: Mask layout of detection circuit – non modular (1st gen) with 170µA charging current. Area of layout = 180λ×210λ or 144µm×168µm.

Figure 4.13, above, is the layout of a detection circuit that was designed as a single unit without any modules. This was done to take advantage of any area reduction that can be achieved by the non modular approach. Even though a more compact layout could be achieved by tighter metal routing than the layout shown in Figure 4.13, the routing interconnects were deliberately designed in this fashion so that there is plenty of space between neighboring interconnects to minimize the effect of fringing capacitance and cross talk.

Figure 4.14 shows the complete layout of the 2.2mm × 2.2mm die using 40 pin pad-frame. The detection circuits were incorporated in four quadrants, with each quadrant having four detection circuits with different response behavior. The detection circuits were designed to be off centered, with top metal (M2) traces running from each of the detection circuit's sensor connect site to the center of the die where they terminate close to a common ground plane metal interconnect. The sensors, fabricated using the FIB workstation, will be

connected between these two metal planes. A common power and ground pad powers all the detection circuits in the die.

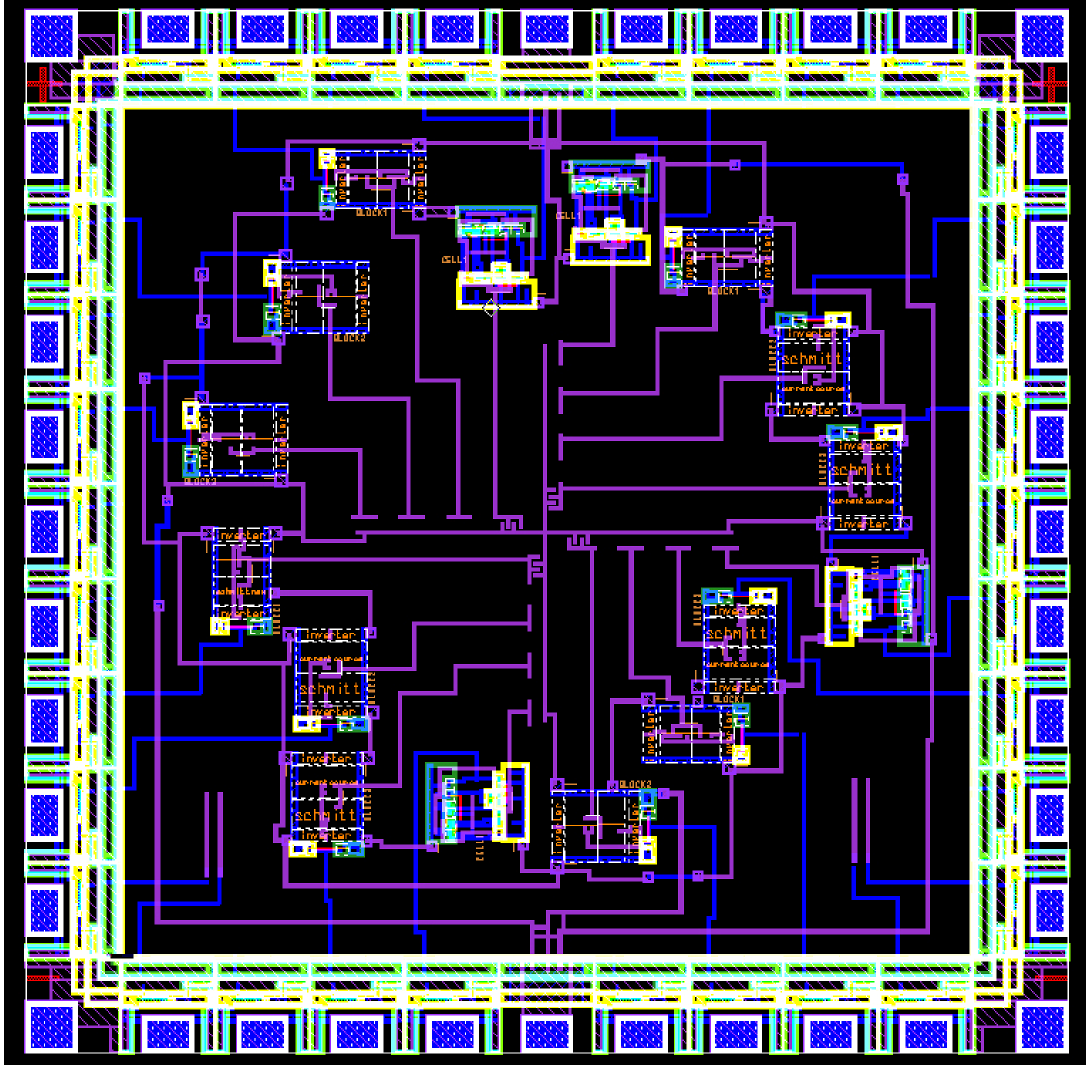


Figure 4.14: Mask layout of complete 1st generation 2.2mm×2.2mm chip with 16 sensor sites and dedicated detection circuits.

Redundant metal traces leading to output pads were also designed to allow for post fabrication debugging (see lower corners of layout in Figure 4.14). The FIB workstation could be used to establish connection between these metal lines and any portion of the circuit on the die. The fabricated silicon dies were wire-bonded and packaged in ceramic 40-lead dual-inline packages (DIP40) with topside cavity. Ten packaged prototype chips were fabricated to test the first generation circuit design.

4.3. Second Generation circuit design

The detection circuitry for the second generation of chips is also a capacitance to frequency converter. The operating principle of the detection circuit is based on the closed loop oscillations of a typical ring oscillator. The circuit consists of a simple ring oscillator with an odd number of minimum sized inverters connected in a closed loop with the sensor capacitance connected to any one of the stages of the ring oscillator, as shown in Figure 4.15. The output frequency of the detection circuit is inversely proportional to the absolute capacitance connected, i.e., the capacitance of the sensor, plus the parasitic capacitance of the metal interconnect connecting the sensors and the circuit.

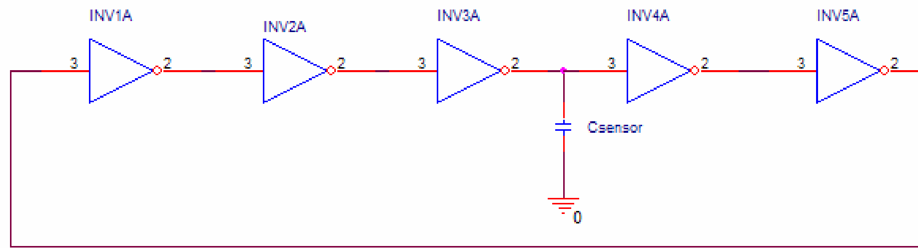


Figure 4.15: Typical Ring oscillator detection circuit for 2nd generation of chips.

The odd number of inverters forms a closed loop with positive feedback. The oscillation frequency of the ring oscillator is given by

$$f_{osc} = \frac{1}{n \cdot (t_{PHL} + t_{PLH})}$$

Eq-4.2: Frequency of a typical ring oscillator [37].

Where n is the odd number of identical inverters in the loop. t_{PHL} and t_{PLH} are the propagation delays of an inverter when the output transitions from high to low and low to high respectively. When an extra load capacitor (sensor capacitor) is added to the inverter chain, the propagation delay will increase depending on the size of the added capacitance. The propagation delays of a typical inverter is given by

$$t_{PHL} = R_n \cdot (C_{outn} + C_{load})$$

$$t_{PLH} = R_p \cdot (C_{outp} + C_{load})$$

Eq-4.2: Propagation delays of inverters in ring oscillator [37].

R_n and R_p are the switching resistances between the source and drain of the NMOS and PMOS transistors. C_{out} is the output capacitance which is equal to the oxide capacitance C_{ox}. C_{load} is the sum of the input capacitance of the next stage and the sensor capacitance. The propagation delays change in concurrence to the sensor capacitance variations and the resulting output frequency also changes following Eq-4.2.

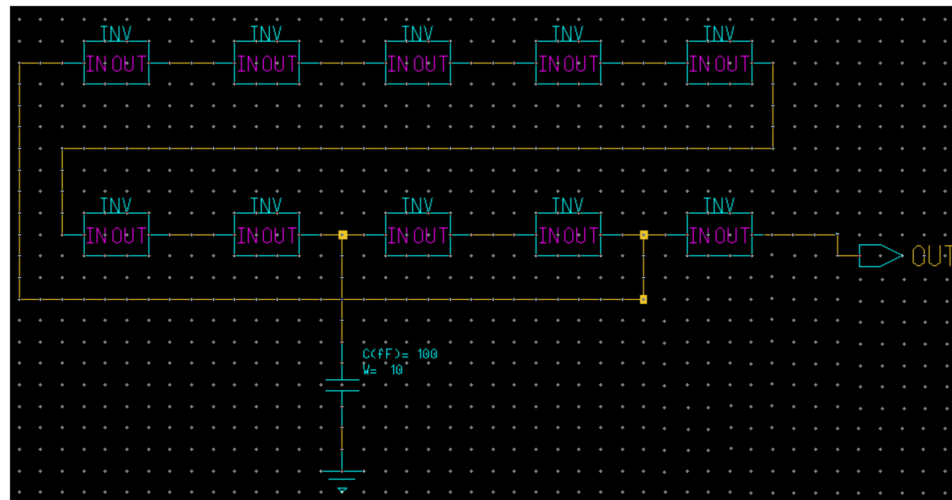


Figure 4.16: Circuit schematic of a 9-stage ring oscillator detection circuit for 2nd generation of chips.

A typical 9-stage ring oscillator with the sensor capacitor connected to the input of the 8th inverter in the loop is shown in Figure 4.16. The sensor capacitor can be connected to any of the inverter stages of the ring oscillator. Figure 4.17 shows the simulated responses of the ring oscillator detection circuits when the sensor capacitance was varied from 1 to 100ff. The detection circuit shows a change in output frequency of about 3MHz for every 10ff change in capacitance. This frequency shift can be easily measured by an external frequency counter. Similar response behavior is exhibited for a wider range of input capacitance variations as depicted in Figure 4.18. More stages could be included in the ring oscillator to reduce the oscillation frequency, but the sensitivity is better at higher operating frequencies. This behavior is also shown in Figure 4.18. Also increasing the ring oscillator stages would

increase the overall layout area of each detection circuit and this would minimize the array density.

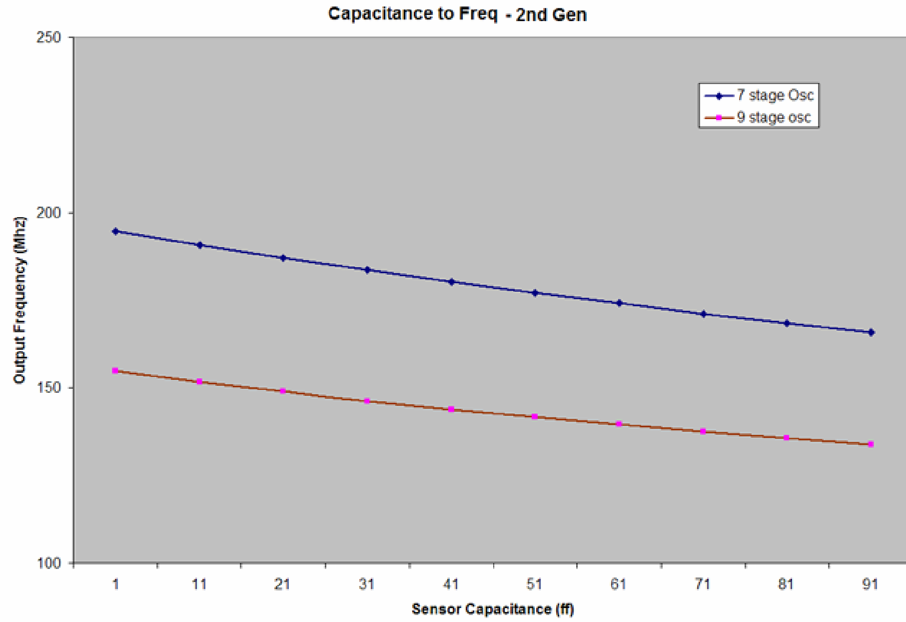


Figure 4.17: Output frequency vs. sensor capacitance plots of a typical 7-stage and 9-stage ring oscillator detection circuit.

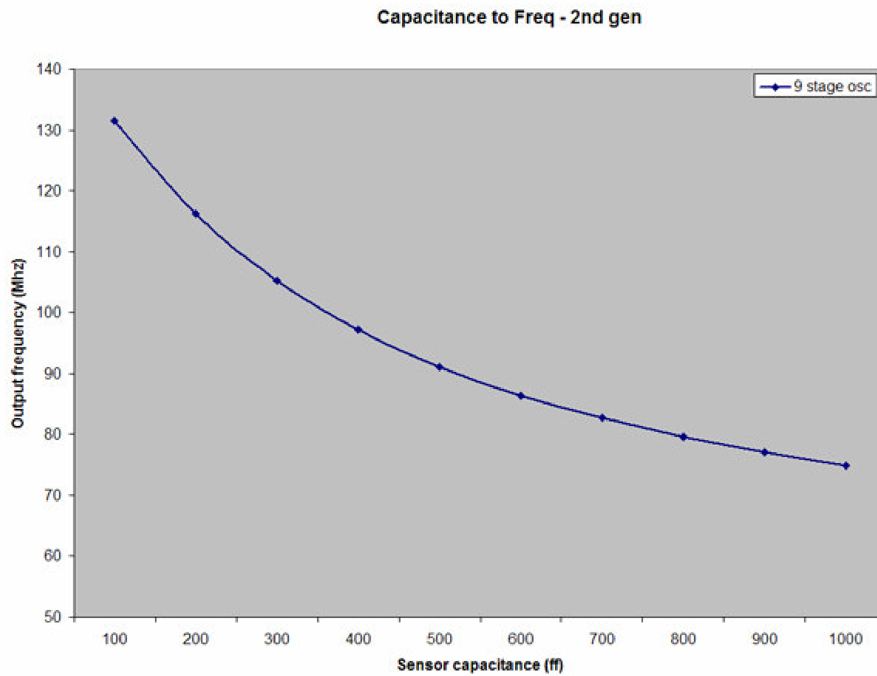


Figure 4.18: Output frequency vs. sensor capacitance plot (large sensor capacitance variations) of a typical 9-stage ring oscillator detection circuit.

4.4. Second Generation Mask layout design

Similar to the previous generation of chips, this design was also implemented using the AMI 1.5μm process through MOSIS educational program with die size 2.2mm×2.2mm. All cells were designed using MOSIS SCMOS design rules and eventually scaled with a λ (scaling factor) of 0.8 microns. Figure 4.19 shows the layout of a 7-stage and 9-stage ring oscillator. The sensor capacitor was connected to one of the inverter inputs in the ring oscillator.

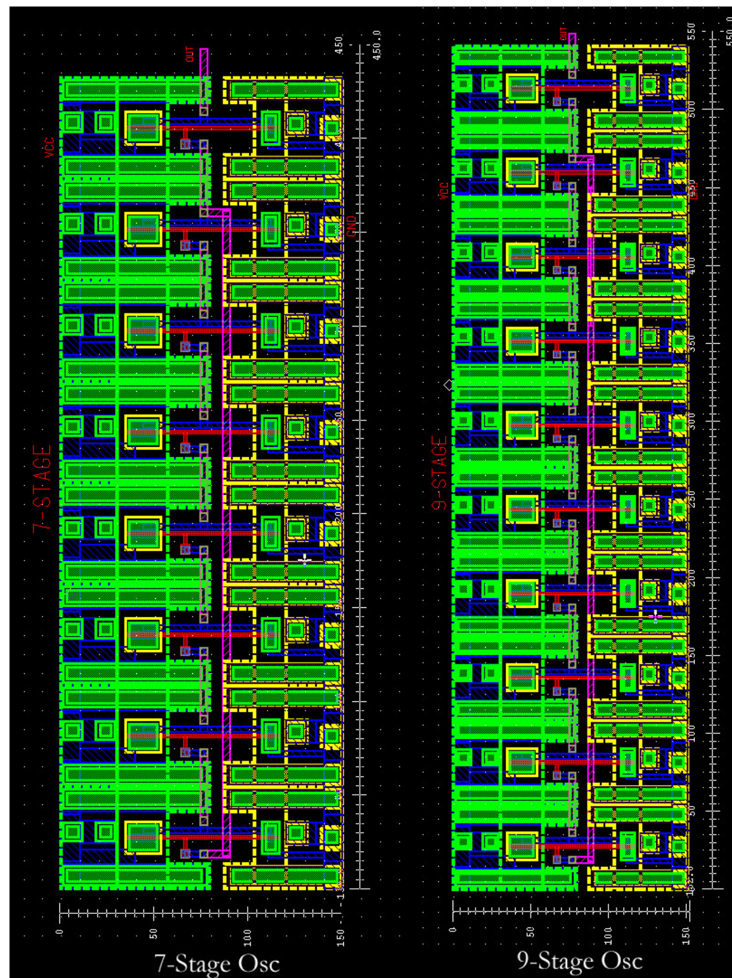


Figure 4.19: Mask layout of a 7-stage and 9 stage Ring oscillator detection circuits for 2nd generation chips. Area of 7-stage detection circuit is 150λ×450λ or 120μm×360μm. Area of 9-stage detection circuit is 150λ×550λ or 120μm×440μm.

Figure 4.20 shows the complete layout of the 2.2mm×2.2mm die using a 40-pin pad-frame. The detection circuits were incorporated into four quadrants similar to the 1st generation design. Each quadrant has two 9-stage and one 7-stage detection circuit, along with one first generation detection unit. The detection circuits were placed off-center with metal-2 traces running from each of the detection circuit's sensor connect sites to the center of the die where it terminates close to a common ground plane metal interconnect, similar to the previous design. This design also has four redundant metal lines from the output pins to enable post fabrication debugging. A common power and ground pad powers all the detection circuits in the die. Twenty packaged (DIP40) and five unpackaged dies were fabricated to test the second generation circuit design.

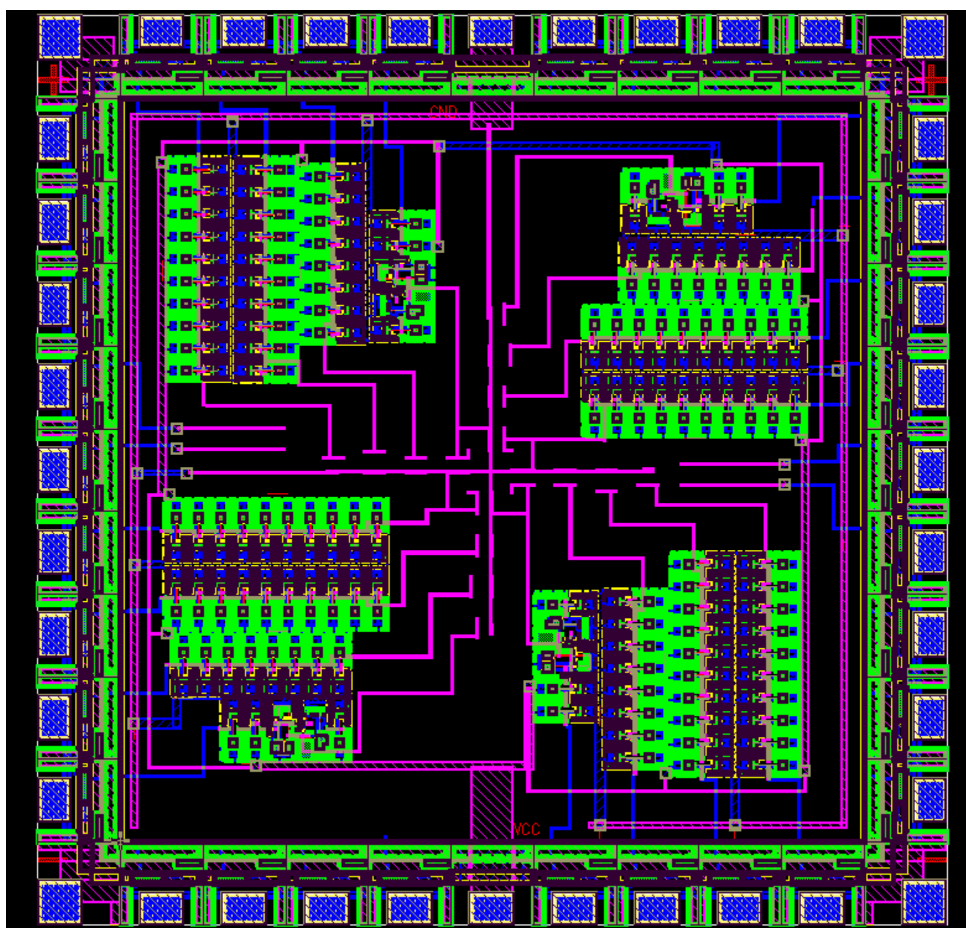


Figure 4.20: Mask layout of complete 2nd generation 2.2mm × 2.2mm chip with 16 sensor sites and dedicated detection circuits.

4.5. Third Generation circuit design

The third generation design converts the change in sensor capacitance to a change in output amplitude. It is simpler to measure changes in amplitude than to measure changes in frequency (1st and 2nd generation of designs) using an external instrument. This circuit design converts the change in absolute capacitance to a change in output voltage amplitude of an AC signal. Temperature variations and noise immunity were not addressed in the previously designed chips. The functional schematic of the circuit is shown in Figure 4.21.

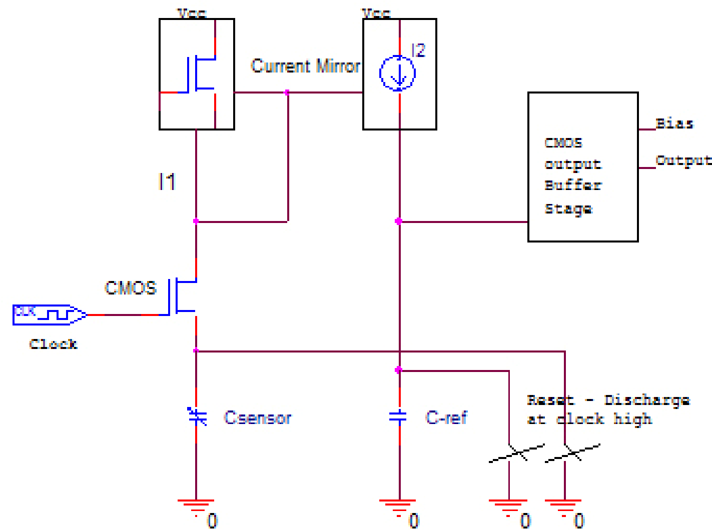


Figure 4.21: Block schematic of 3rd generation detection circuit.

The scheme used for this detection circuit had been developed for measuring low capacitance for micro-capacitance tomography applications [38] and for measuring on-chip interconnect capacitance measurements [39]. This circuit requires an external clock trigger (typically 1 MHz). The working principle of this circuit is simple and can be easily explained. During the positive cycle of the clock, all capacitors are discharged, including the sensor capacitor and its associated parasitic capacitances. During the negative cycle of the clock, a small current I1 charges the sensor capacitor. The voltage across the sensor capacitor is dependent on the charging current I1 and the value of the sensor capacitor. The same

current I1 is mirrored to a larger reference capacitor. The voltage across the reference capacitor is proportional to the sensor capacitance and its associated parasitic or stray capacitances. The resultant voltage is amplified and buffered by the output stage. The clock can be incorporated in the design but was left external for flexibility.

Figure 4.22: CMOS circuit schematic of 3rd generation detection circuit.

The above figure shows the circuit schematic of the detection circuit. Ignoring the impedances of the switching transistors N1, N2 and P1, the charging current I1, flowing through transistor P2 (P2 in saturation and ignoring channel length modulation), is given by

$$I_1 = \frac{\mu_0 C_{ox} W}{2L} (|V_{GS}| - |V_T|)^2$$

Eq-4.3: Current through transistor P1 [38].

Where μ_0 is the mobility of the charge carriers in the channel, C_{ox} is the gate capacitance per unit area and W/L are the dimensions of the gate P2. The current I_1 is the current that charges the sensor capacitance to voltage V_s and is given by

$$V_s = \int_0^t I_1 DT$$

Eq-4.4: Voltage across sensor capacitor [38].

Substituting for I1 from Eq-4.3 yields

$$V_s = \frac{\left[\frac{\mu_0 C_{ox} W_2}{L_2}\right](V_{DD} - |V_T|)^2 t}{2C_{sen} + \left[\frac{\mu_0 C_{ox} W_2}{L_2}\right](V_{DD} - |V_T|)^2 t}$$

Eq-4.5: Voltage across sensor capacitor [38].

Transistors P2 and P3 form a current mirror and PMOS transistor P3 would be operating in saturation mode. Therefore Eq-4.5 can be applied in Eq-4.3 to solve for V_{out} and the output value settles to value given by the equation [38]

$$V_{out} = \frac{L_2 W_3}{W_2 L_3} \frac{(V_{DD} - |V_T|)}{C_{ref}} C_{sen}$$

Eq-4.6: Output voltage across reference capacitor [38].

This resultant output voltage V_{out} is buffered by the output stage and sent to the output pad-frame. Further, immunity to stray capacitance influence and immunity to noises common to the whole chip can be achieved by amplifying the difference signal between a well matched detection circuit pair with no active sensor connected to one of the detection circuits. This can be achieved by connecting the output of two channels of the chip to an external differential amplifier. The output of the amplifier would be an absolute measure of the sensor capacitance, provided the circuit pairs are well matched [38]. The differential amplifiers can also be implemented on chip, but were left external to keep the design simple. The surface of the chips may be exposed to harsh liquid mediums while testing and have a good probability of surface insulation failure. If one channel were to fail, another channel can be used in its place if the differential amplifier is left external. Having a detection circuit pair with both the detection circuit channels connected to sensors would provide thermal

noise immunity in addition to stray capacitance immunity, but only one sensor can be exposed to the target molecule that needs to be measured. If both the sensors are exposed, their responses will be common and will be cancelled by the differential amplifier.

The gain of the detection circuit is set by the value of the reference capacitor used, as per Eq-4.6. Care must be taken in choosing the value of the reference capacitor, as the current mirror (transistors P2 and P3 in Figure 4.22) would fail to operate in the expected fashion if the voltage across the reference capacitor (V_{out}) reaches V_{DD} - $2V_T$ [38]. The gain of the circuit increases as the value of the reference capacitor approaches the value of the sensor capacitor. When the sensor capacitor is subjected to the test medium, its value would increase based on the dielectric property of the analyte. For example, if the analyte under test is in a water based solution, the capacitance of the sensor may increase by 78% from its initial value as the dielectric constant of water is approximately 78 at room temperature. If the initial baseline air capacitance of the sensor is around 1ff, with exposure to the test solution, its value would increase to 78ff. To have flexibility in the detectable range with good sensitivity, a variety of reference capacitors were chosen. Three sets of detection circuits with reference capacitors of 250ff, 350ff and 450ff were designed. The gain plots of these detection circuits are shown in Figures 4.23 to 4.25. It can be seen from the plots that the gain of the detection circuit decreases with increase in reference capacitor, but at the same time it allows for an increased range of sensor capacitor values (dynamic range). The power consumption plots of these three variations of the detection circuit are shown in Figures 4.26 to 4.28. Most of the power is utilized by the buffer stage which drives the capacitive output load of the DIP40 pin and the input impedance of the measuring device. For simulation purposes this load was set at 10pf.

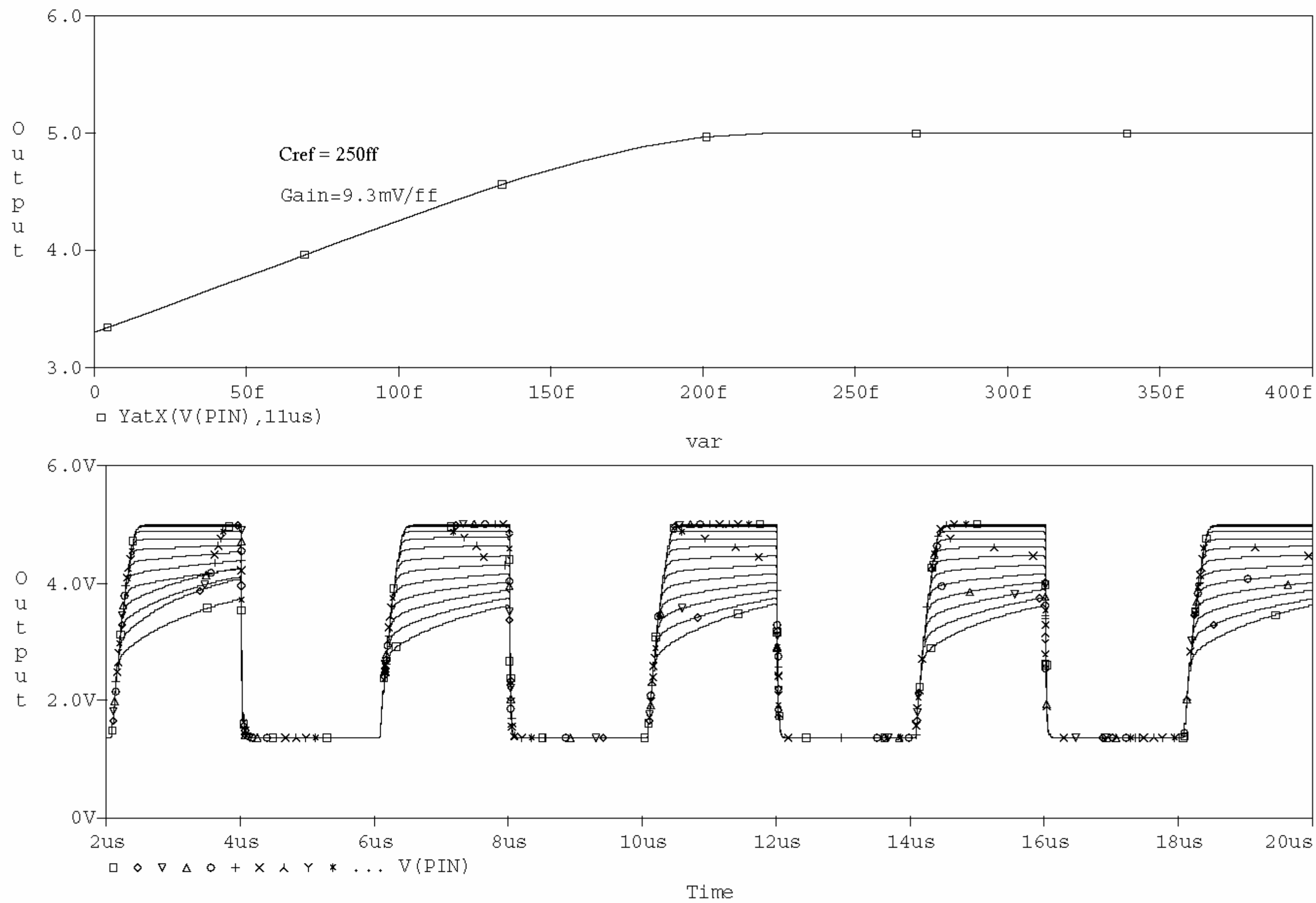


Figure 4.23: Simulated gain plot of the detection circuit with 250ff reference capacitor. The sensor capacitor was swept from 1ff to 400ff. Bottom plot shows voltage output of the circuit and the top plot shows the circuit gain evaluated as an output voltage goal function against variations in sensor capacitance.

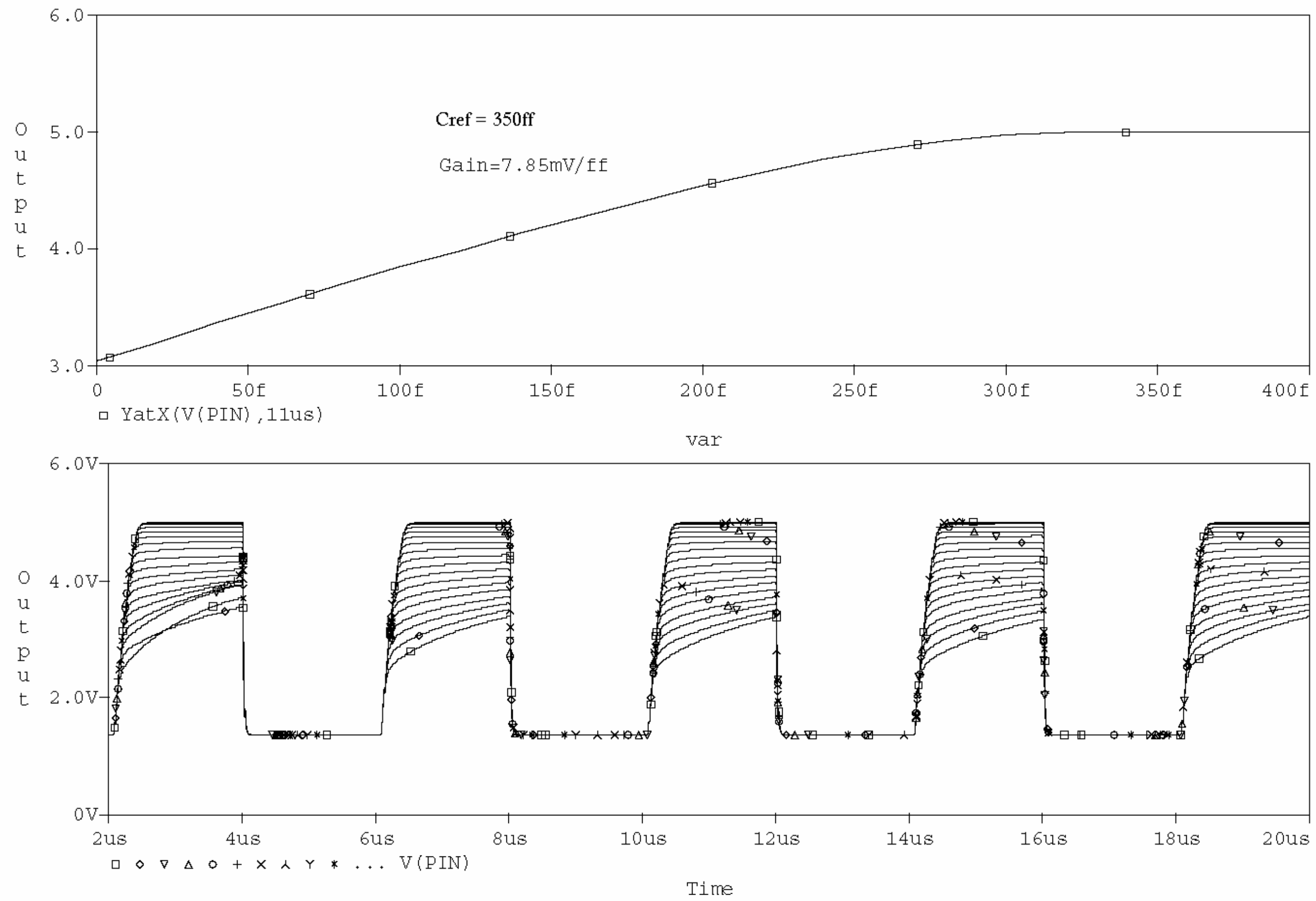


Figure 4.24: Simulated gain plot of the detection circuit with 350ff reference capacitor. The sensor capacitor was swept from 1ff to 400ff. Bottom plot shows voltage output of the circuit and the top plot shows the circuit gain evaluated as an output voltage goal function against variations in sensor capacitance

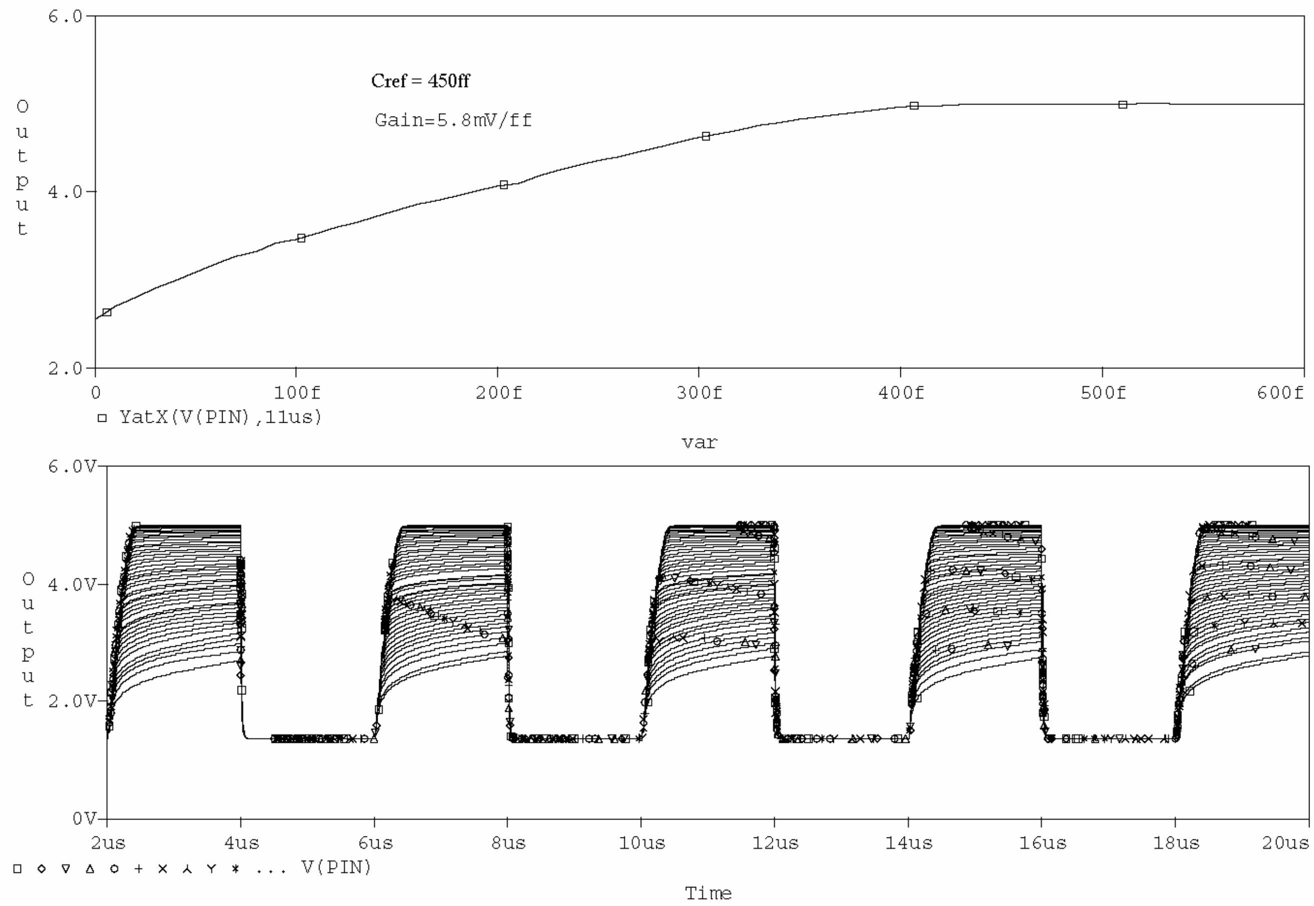


Figure 4.25: Simulated gain plot of the detection circuit with 450ff reference capacitor. The sensor capacitor was swept from 1ff to 600ff. Bottom plot shows voltage output of the circuit and the top plot shows the circuit gain evaluated as an output voltage goal function against variations in sensor capacitance.

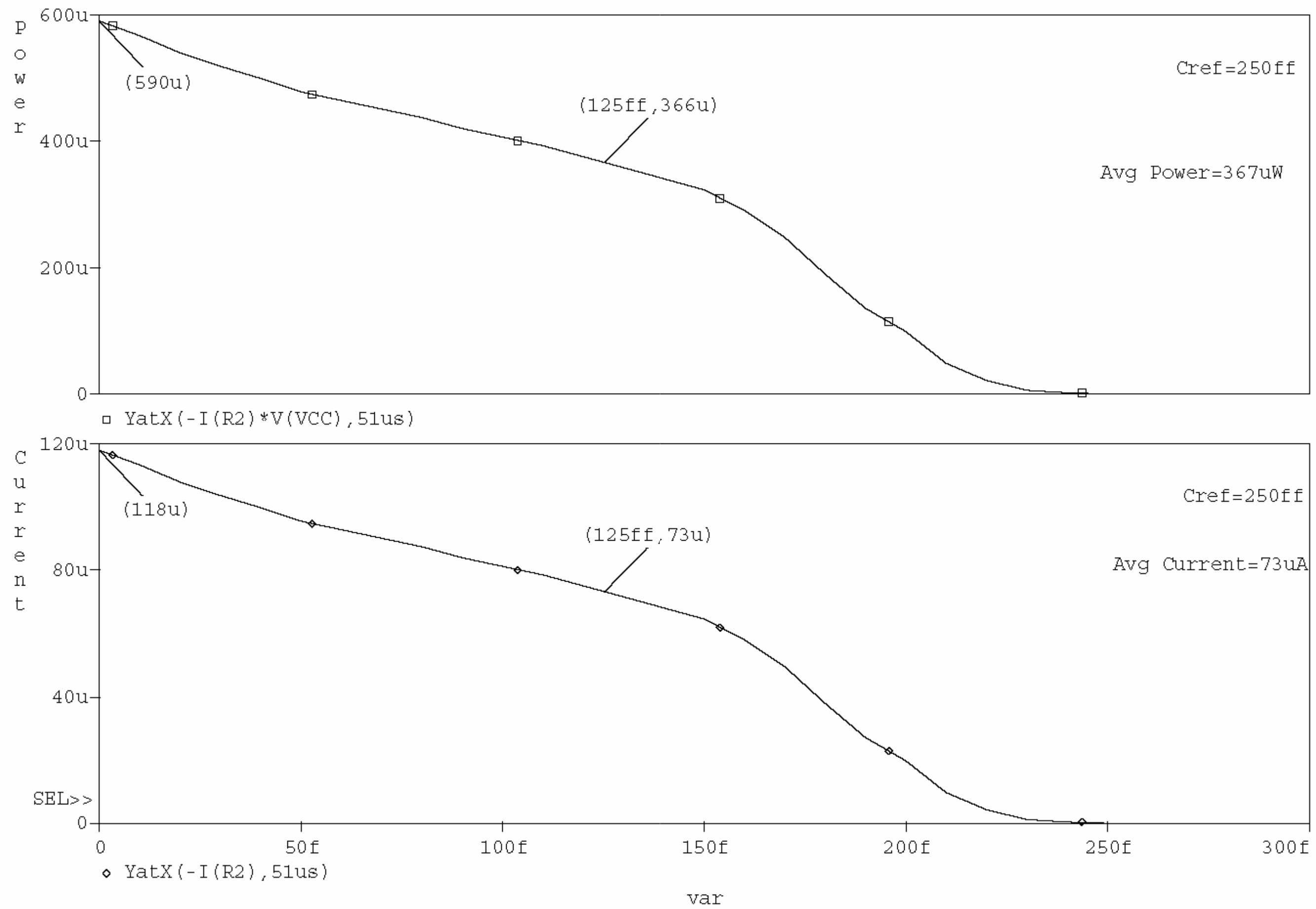


Figure 4.26: Simulated average current and power plots of the detection circuit with reference capacitor as 250ff. The sensor capacitor was swept from 1ff to 300ff. Bottom plot shows the current drawn and the top plot shows the power drawn by the detection circuit while driving an output load of 10pf.

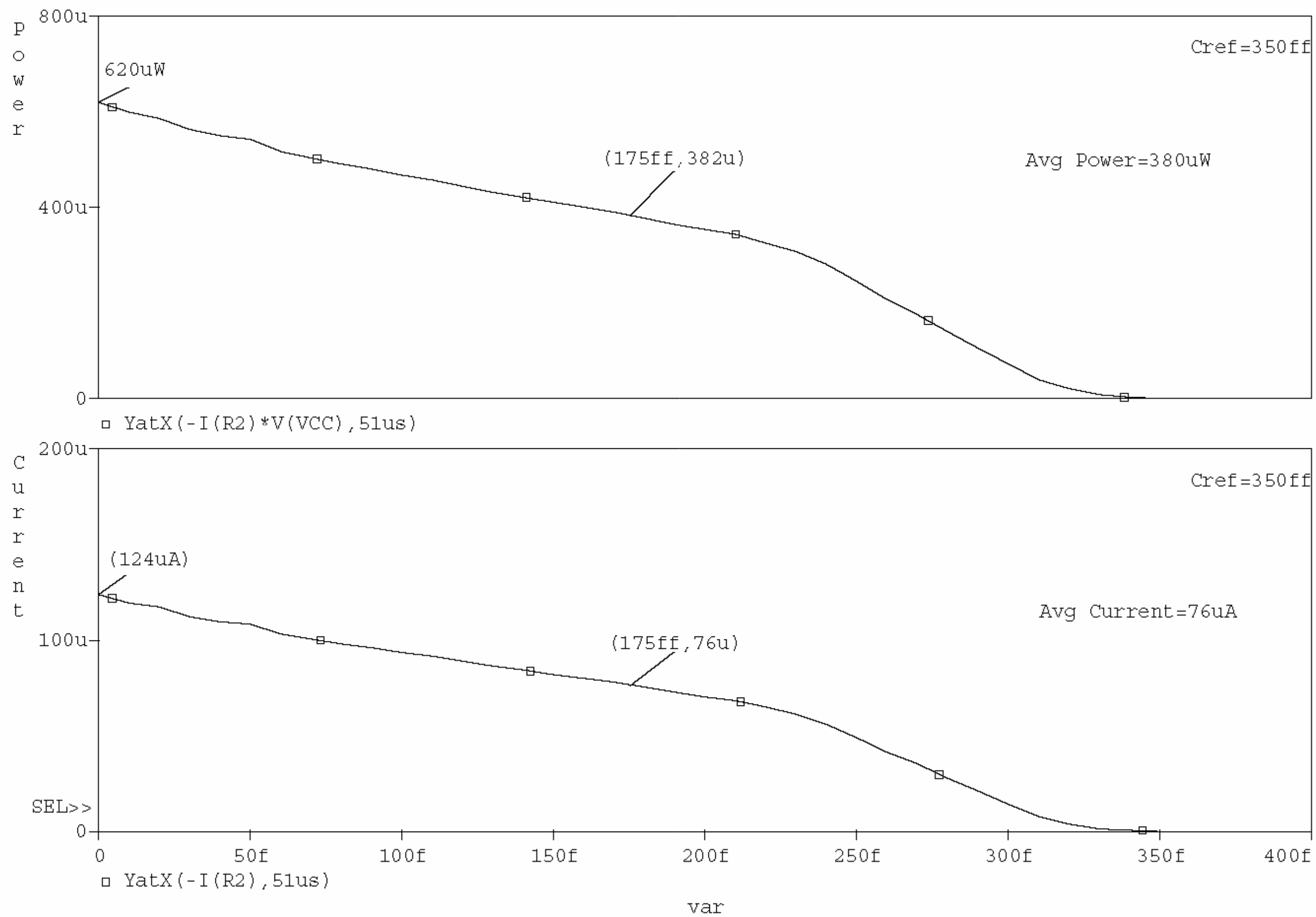


Figure 4.27: Simulated average current and power plots of the detection circuit with reference capacitor as 350ff. The sensor capacitor was swept from 1ff to 400ff. Bottom plot shows the current drawn and the top plot shows the power drawn by the detection circuit while driving an output load of 10pf.

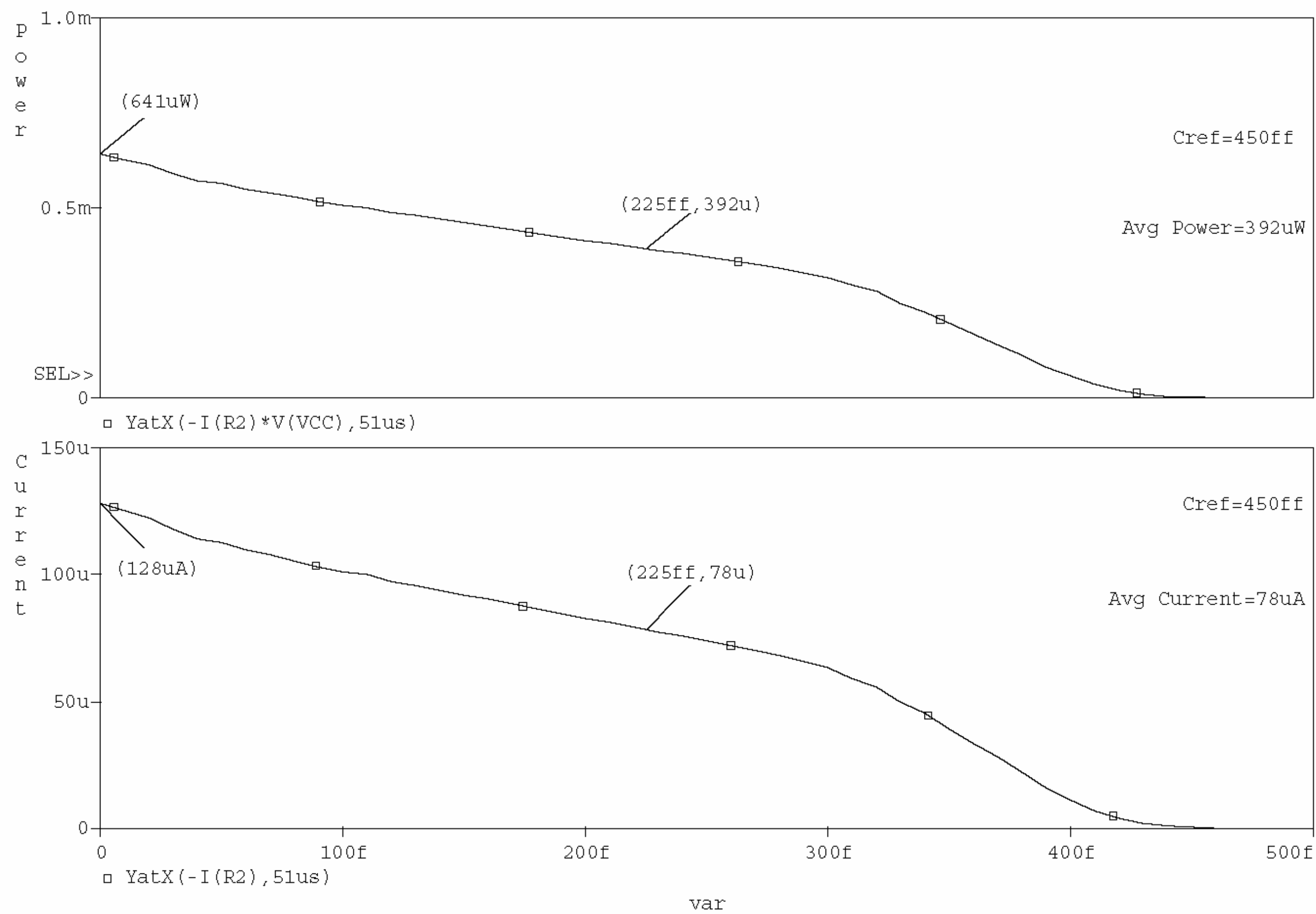


Figure 4.28: Simulated average current and power plots of the detection circuit with reference capacitor as 450ff. The sensor capacitor was swept from 1ff to 500ff. Bottom plot shows the current drawn and the top plot shows the power drawn by the detection circuit while driving an output load of 10pf.

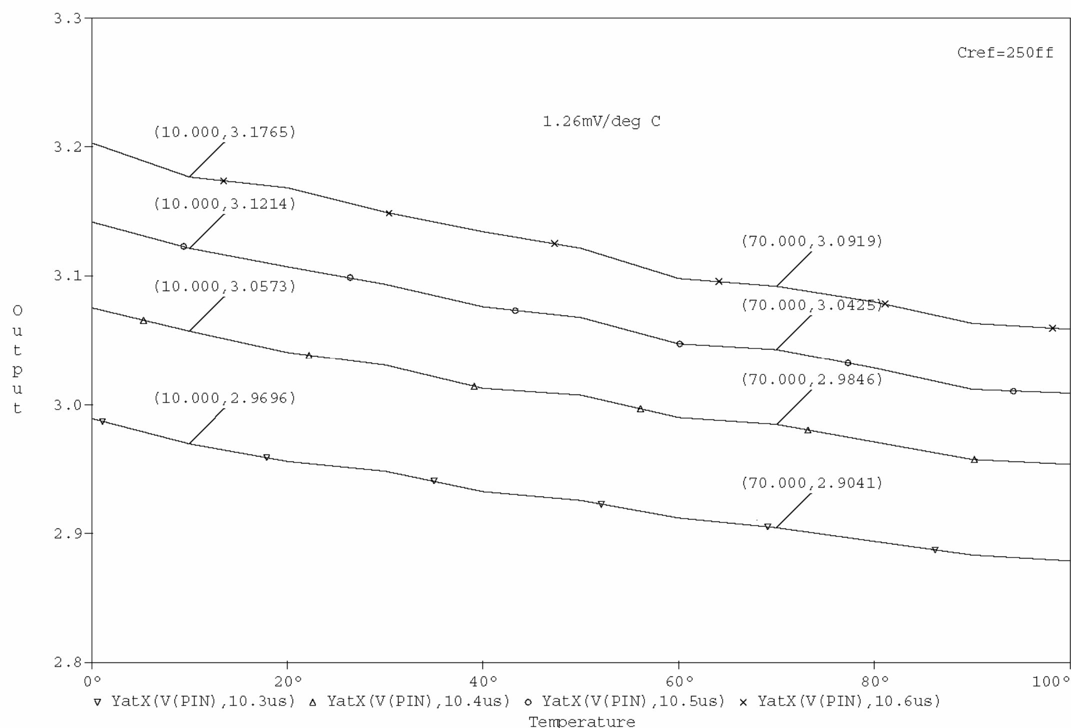


Figure 4.29: Simulated temperature response plot of the detection circuit. The simulation temperature was swept from 0 to 100 ºC, C_{ref} = 250ff, C_s = 5ff, circuit load = 10pf. The plot shows the output response to temperature at various simulation times.

The response of the detection circuit to temperature variations was simulated, as shown in Figure 4.29. Temperature simulations were done with the sensor capacitance kept constant at 5ff and the entire detection circuit driving an external load of 10pf. The output voltage at various simulation times were plotted against temperature. The detection circuit with reference capacitance as 250ff shows an output change of 1.26mV for every ºC change in temperature. Analogous simulations were done for reference capacitors 350ff and 450ff. The detection circuit with 350ff showed a response of 1.54mV, and the one with 450ff showed a response of 1.84mV/ºC change in temperature. These output variations of the detection circuit caused by temperature changes can be minimized by having a well matched detection circuit pair and the difference signal between them measured as output. This scheme is shown in Figure 4.30. Simulations showed that measuring the difference signal between two detection circuits as the output signal is more tolerant to temperature variations.

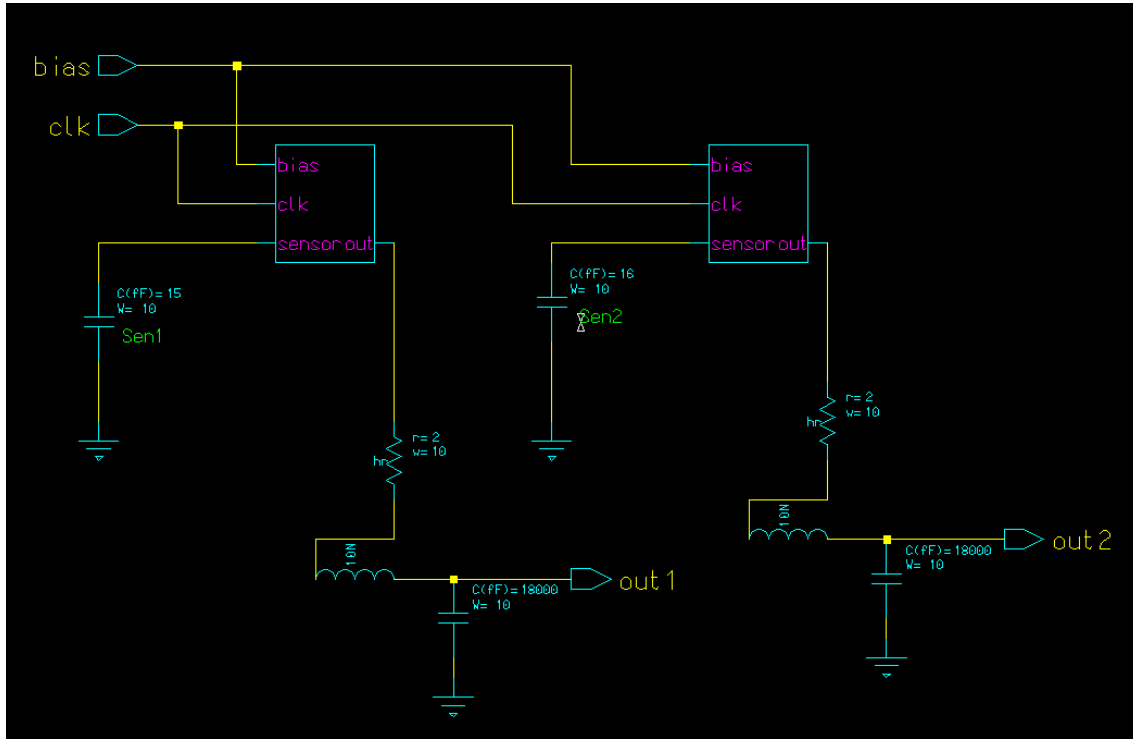


Figure 4.30: Simulation circuit schematic of detection circuit pair for improving stray capacitance and local noise immunity. The simulation also includes the parasitic components of the output bond-wire and DIP40 pins.

4.6. Third Generation Mask layout design

This design was also implemented using AMI 1.5μm process through MOSIS educational program, with a die size of 2.2mm×2.2mm. All cells were designed using MOSIS SCMOS design rules and eventually scaled with a λ (scaling factor) of 0.8 microns. The mask layouts for the three variations of the detection circuit are shown in Figures 4.31 to 4.33. The reference capacitances were designed as poly2 over poly1. On chip capacitors are generally made with the poly layers [37]. Capacitors can also be made using the metal layers, but they are generally area consuming. A MOSFET (metal–oxide–semiconductor field-effect transistor) with the drain and source shorted and operating in strong inversion region, can also behave as a capacitor, but has voltage dependencies. The poly areas for the capacitances were calculated based on AMI process parameters that were measured from previous fabrications. The poly capacitances were generally designed a little smaller (5%) than the

desired value because the gate capacitances of the buffer stage, output capacitances of the current source and switching transistors add to this value. The unit cell layout for the detection circuit was done in a modular fashion, so that for the next variation of the detection circuit only the size of the capacitor's poly layers had to be modified, with no changes in the routing.

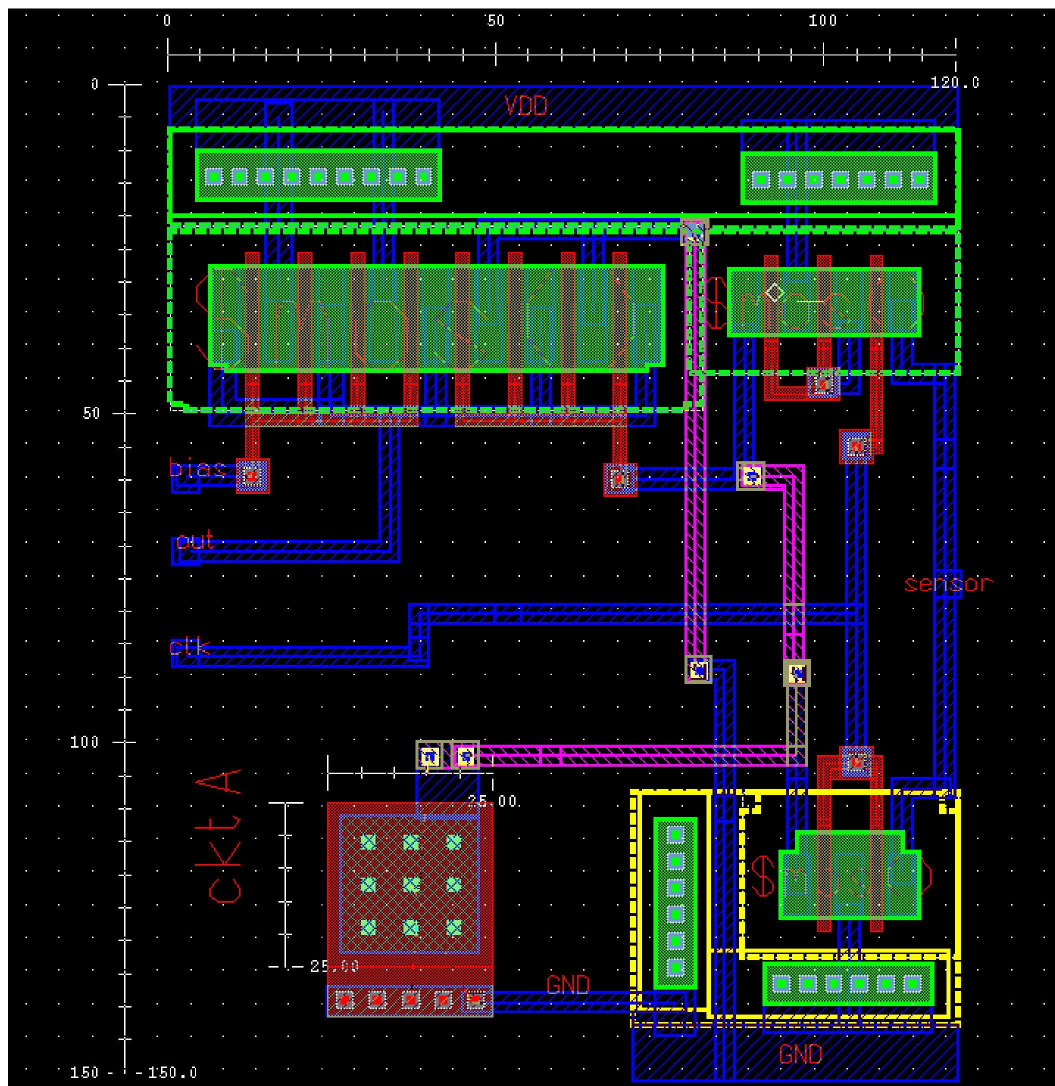


Figure 4.31: Mask layout of detection circuit (3rd gen) with 250ff reference capacitance. Area of the layout = 120λ ×150λ or 96μm×120μm.

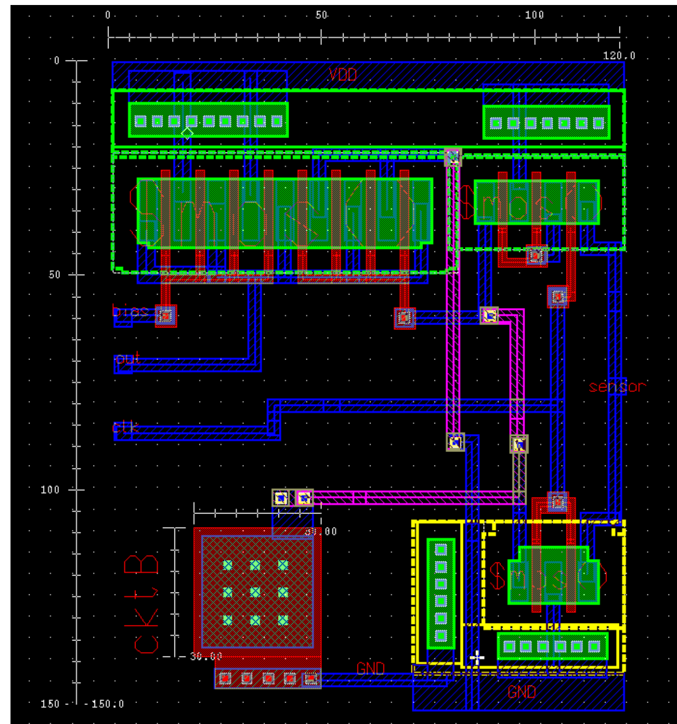


Figure 4.32: Mask layout of detection circuit (3rd gen) with 350ff reference capacitance. Area of the layout = 120λ ×150λ or 96μm×120μm.

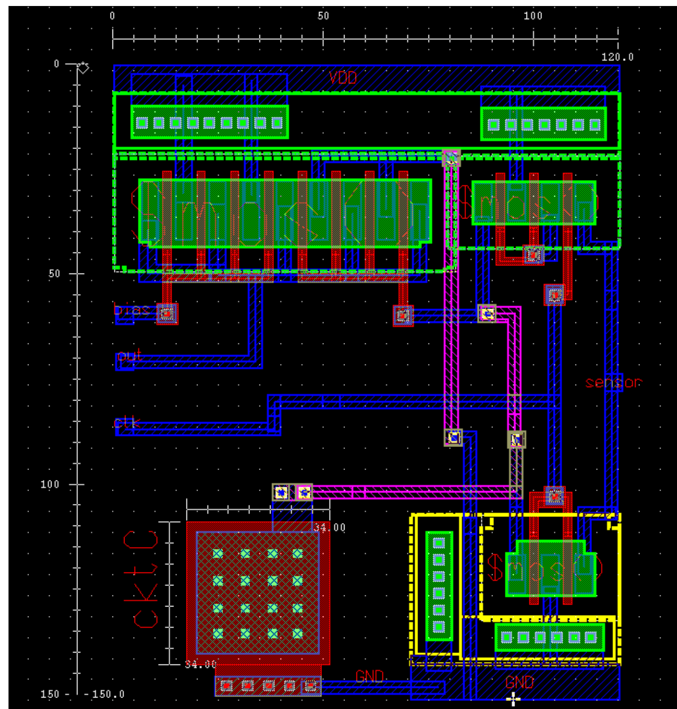


Figure 4.33: Mask layout of detection circuit (3rd gen) with 450ff reference capacitance. Area of the layout = 120λ ×150λ or 96μm×120μm.

Figure 4.34 shows the complete layout of the 2.2mm×2.2mm die using 40 pin pad-frame. The detection circuits were incorporated into four quadrants similar to previous generations. Each quadrant has seven detection circuits with the same reference capacitor size. There are seven circuits with 250ff (quadrant1), seven circuits with 350ff (quadrant2), fourteen circuits with 450ff (quadrants 3 and 4). Each quadrant has its own V_{DD} pad and clock input so that they can be switched independently of the other quadrants. A common bias pin supplies the bias to all the detection circuits in the chip. The detection circuits were placed along the edges of the die to protect them from test solutions, and the sensor sites were located at the center. Metal traces run from each detection circuit to the center of the die where it terminates close to a common ground plane metal interconnect similar to previous designs to form the sensor connect sites. Twenty-five packaged (DIP40) and five unpackaged dies were fabricated to test the third generation circuit design.

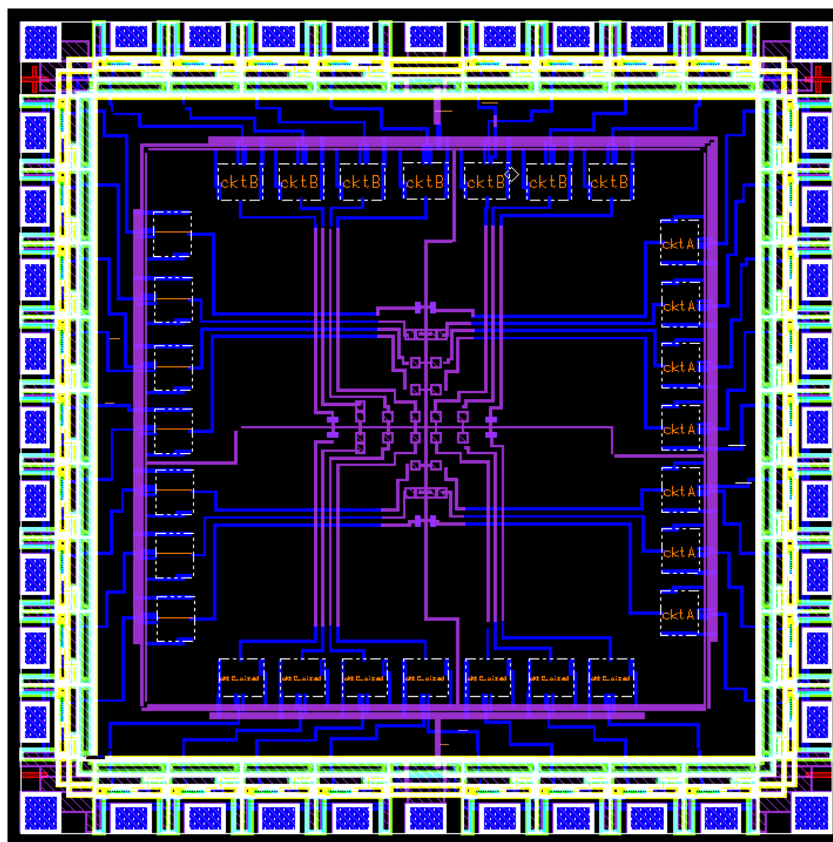


Figure 4.34: Mask layout of complete 3rd generation 2.2mm × 2.2mm chip with 28 sensor sites and dedicated detection circuits.

In this design, the sensor sites have been designed in a way that the buried ground interconnects can be used as one plate of the capacitor, and the other plate of the capacitor would be the platinum wall deposited using the FIB workstation. The square structures in Figure 4.35 are made of metal-2 layer with 15μm on a side and are connected to the common ground. These square structures serve as the buried, unexposed plate of the sensor. Platinum structures (walls) can be deposited on top of the nitride passivation above these square plates. These platinum walls are then wired to the interconnect that connects to the detection circuit. Constructing the sensors by this method provides electrical isolation between the two plates of the sensor capacitor, which is beneficial while dealing with conductive test solutions.

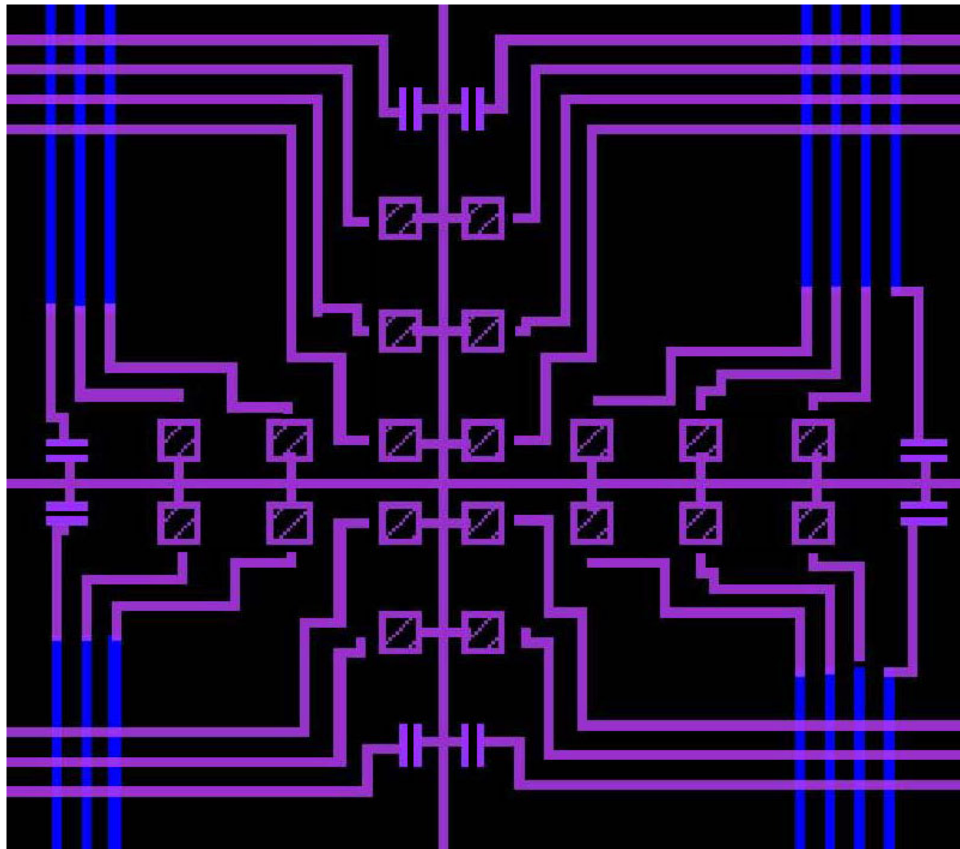


Figure 4.35: Mask layout of the sensor fabrication sites at the center of the die.

4.7. Fourth Generation circuit design

The circuit principle for this generation of chips is the same as that of 3rd generation. In the previous generation, the detection circuits were placed at the edges of the die and long interconnects ran to the center of the die where the sensors were fabricated. This added length of interconnects not only add to the capacitance of the sensors, but also increases the sensitivity to dielectric changes above the passivation. When the die is subjected to the liquid test medium under evaluation, along with the sensors, the parasitic fringing capacitance of these interconnects would also add to the change in capacitance seen by the detection circuit. Sometimes this change in capacitance would be large enough to be comparable to the reference capacitance and the detection circuit would be saturated. Since the detection circuit is already at its input maximum, it would not be able to detect further dielectric changes in the test solution. Hence, it would be better to have the detection circuit as close as possible to the sensors in order to minimize the effect caused by the fringing capacitance of the interconnects. This generation of chips has been designed to have the detection circuit in close proximity to the sensor sites. This would also enable better matching between two identical detection circuits if the difference signal between them is to be used for noise immunity as described earlier.

The range of input capacitance detection is also different from the previous generation of chips. The reference capacitors for this generation of chips were designed to be 250ff, 500ff and 750ff. The detection circuit with 750ff reference capacitor would allow for the detection of a larger range of input capacitance variations but at the expense of sensitivity. Since any parasitic fringing capacitance seen at the input of the detection circuit is responsive to dielectric changes, the interconnects at the sensor sites were modified to have some standing fringing capacitance and would be able to act as sensors even without any FIB micro fabrication. However, the fringing capacitance of these interconnects are generally very small and would be responsive only to large changes in dielectrics above them. The previous generation of chips was designed to drive a capacitive load of 10pf. This is not enough if the chips were to be directly connected to a measuring instrument without any external amplifier. Hence, this generation of design has a larger output buffer stage and

would be able to drive capacitive loads of up to 100pf. The general circuit schematic with larger output buffer transistors is shown in Figure 4.36.

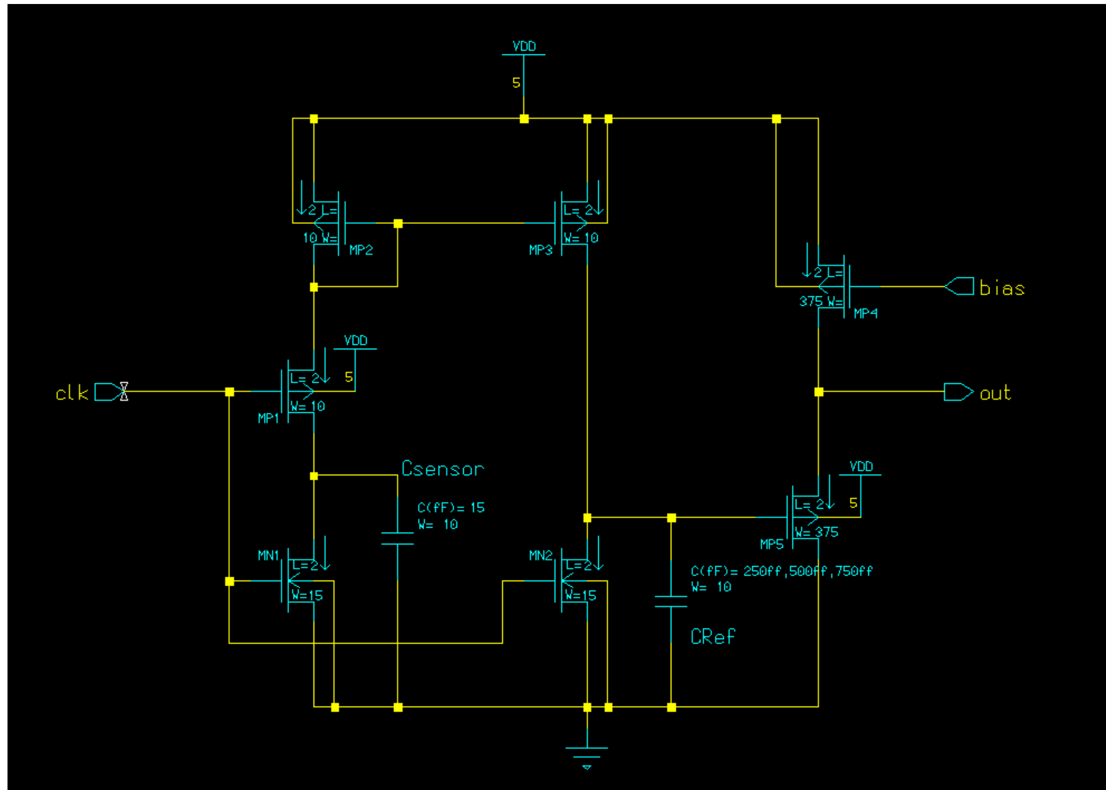


Figure 4.36: CMOS circuit schematic of 3rd generation detection circuit.

The simulated gain plots for the detection circuits with the three variations in the reference capacitances are shown from Figure 4.37 to 4.39. The detection circuit with 250ff as reference capacitor is common between this generation and the previous generation design. But the gain plot for this generation (Figure 4.37) shows that the sensitivity is 7.1mV/ff, whereas the same reference capacitor from the previous generation had a sensitivity of 9.3mV/ff. This drop in sensitivity can be explained by the addition of larger output buffer transistors. The input gate capacitance of the buffer stage adds to the reference capacitor making it effectively more than 250ff and thereby reducing the output response per femto farad change in capacitance. The reference capacitor's value can be reduced in accordance to the size of the buffer transistor, but since absolute input capacitance is not measured quantitatively, the current setup will work without any further

modifications. Average power consumption of these detection circuits is higher than the previous generation design because of the increased buffer size. The power consumption plots of the three variations of the detection circuit are shown in Figures 4.40 to 4.42.

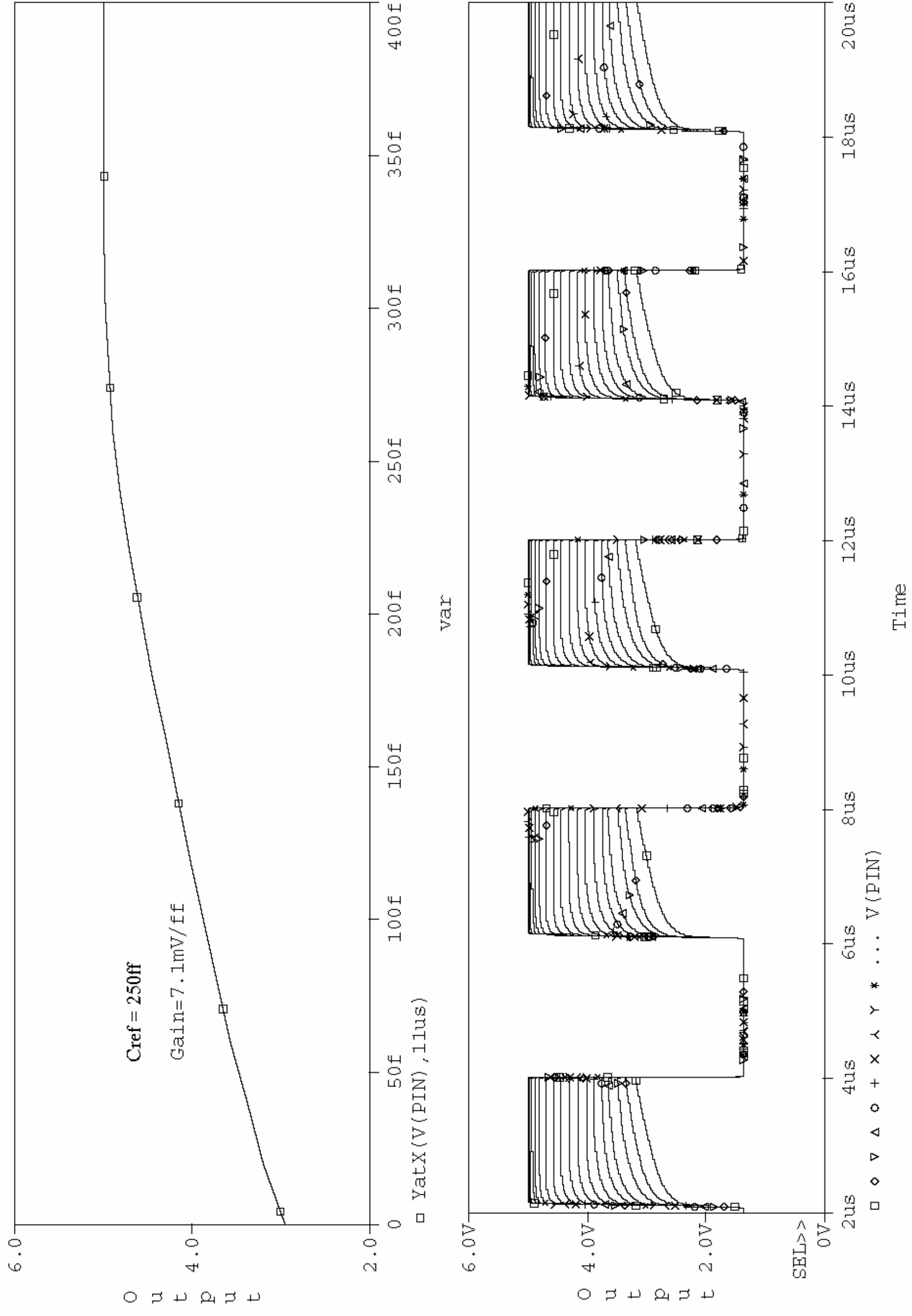


Figure 4.37: Simulated gain plot of the detection circuit with 250ff reference capacitor. The sensor capacitor was swept from 1ff to 400ff. Bottom plot shows voltage output of the circuit and the top plot shows the circuit gain evaluated as an output voltage goal function against variations in sensor capacitance.

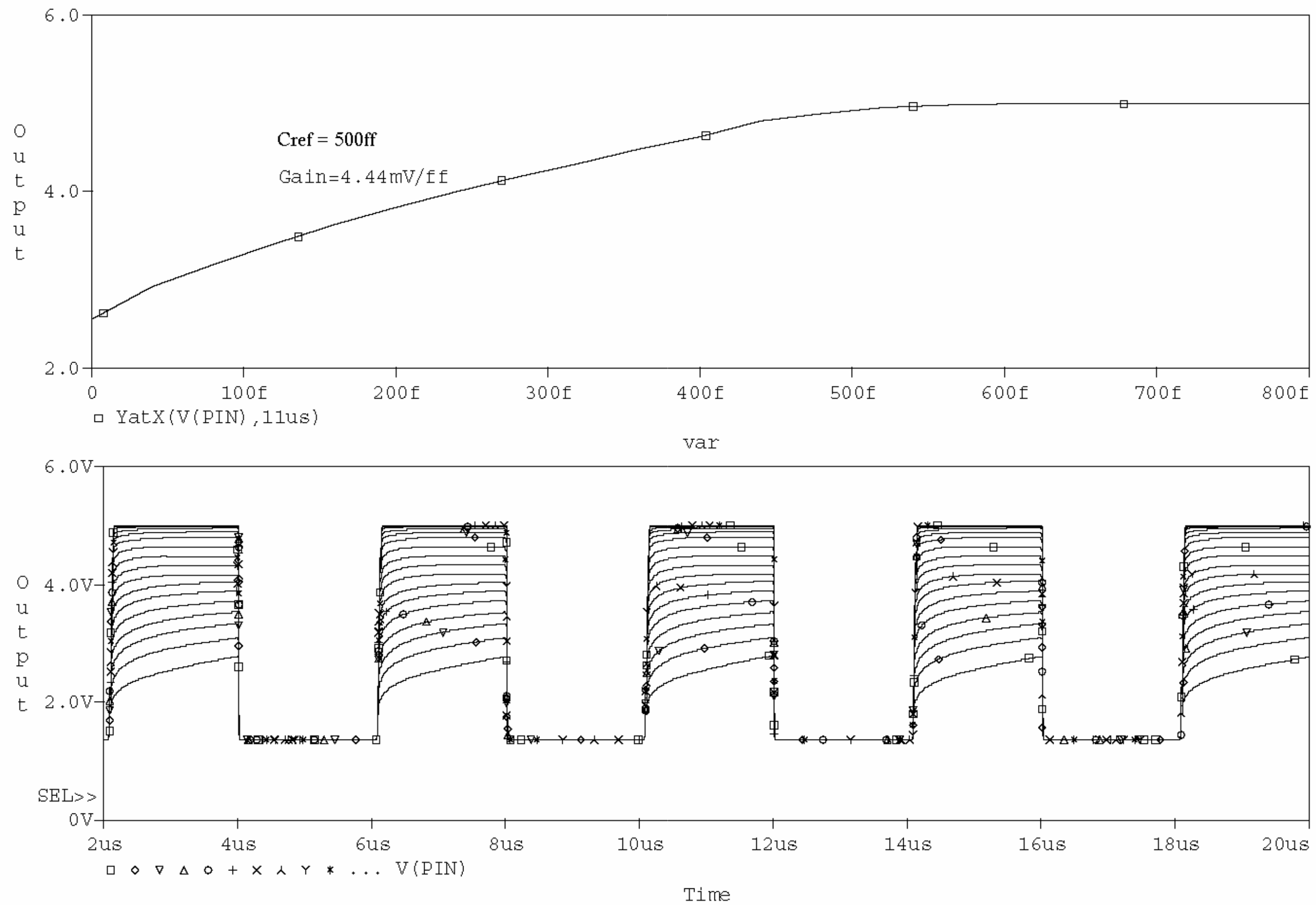


Figure 4.38: Simulated gain plot of the detection circuit with 500ff reference capacitor. The sensor capacitor was swept from 1ff to 800ff. Bottom plot shows voltage output of the circuit and the top plot shows the circuit gain evaluated as an output voltage goal function against variations in sensor capacitance.

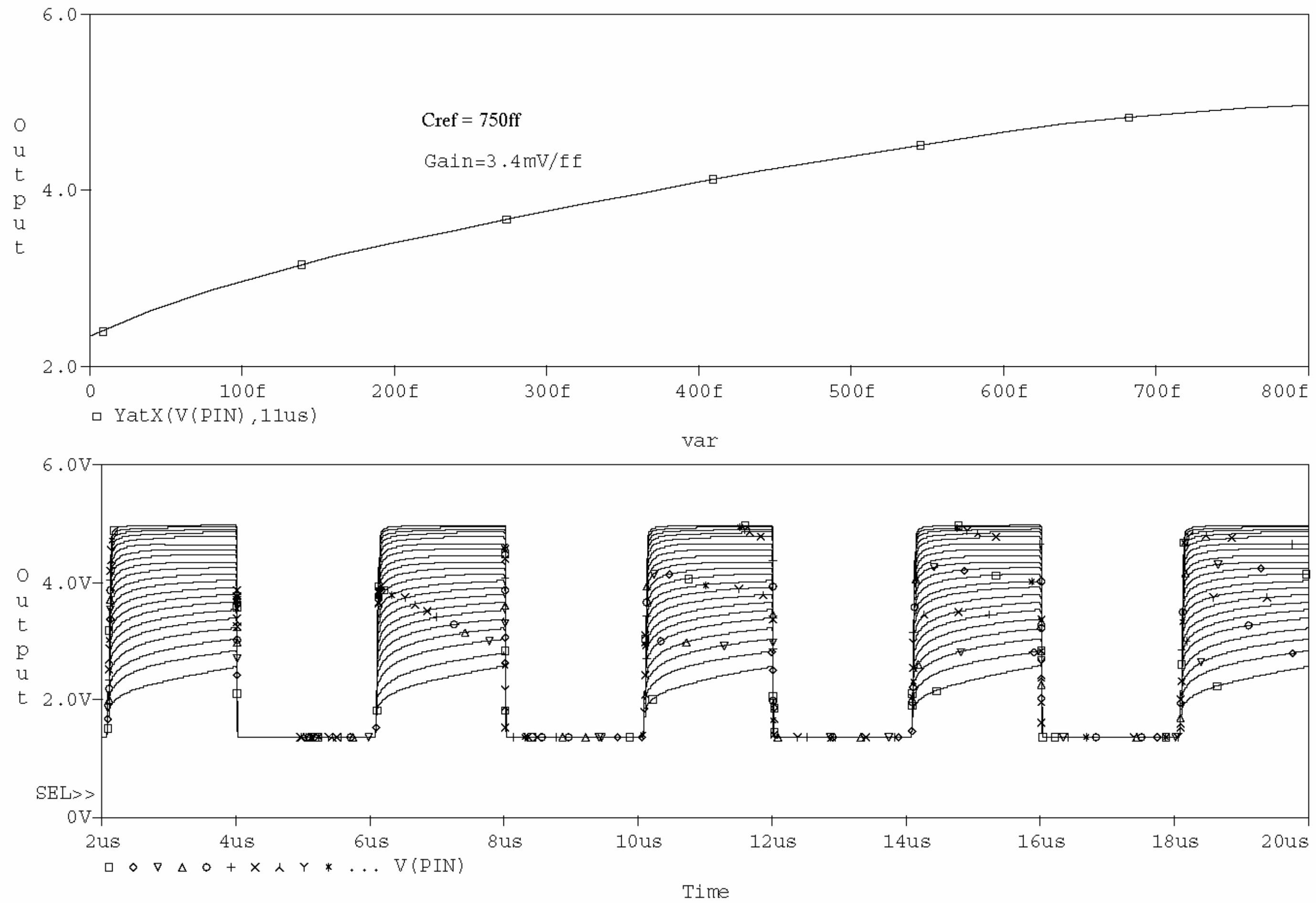


Figure 4.39: Simulated gain plot of the detection circuit with 750ff reference capacitor. The sensor capacitor was swept from 1ff to 800ff. Bottom plot shows voltage output of the circuit and the top plot shows the circuit gain evaluated as an output voltage goal function against variations in sensor capacitance.

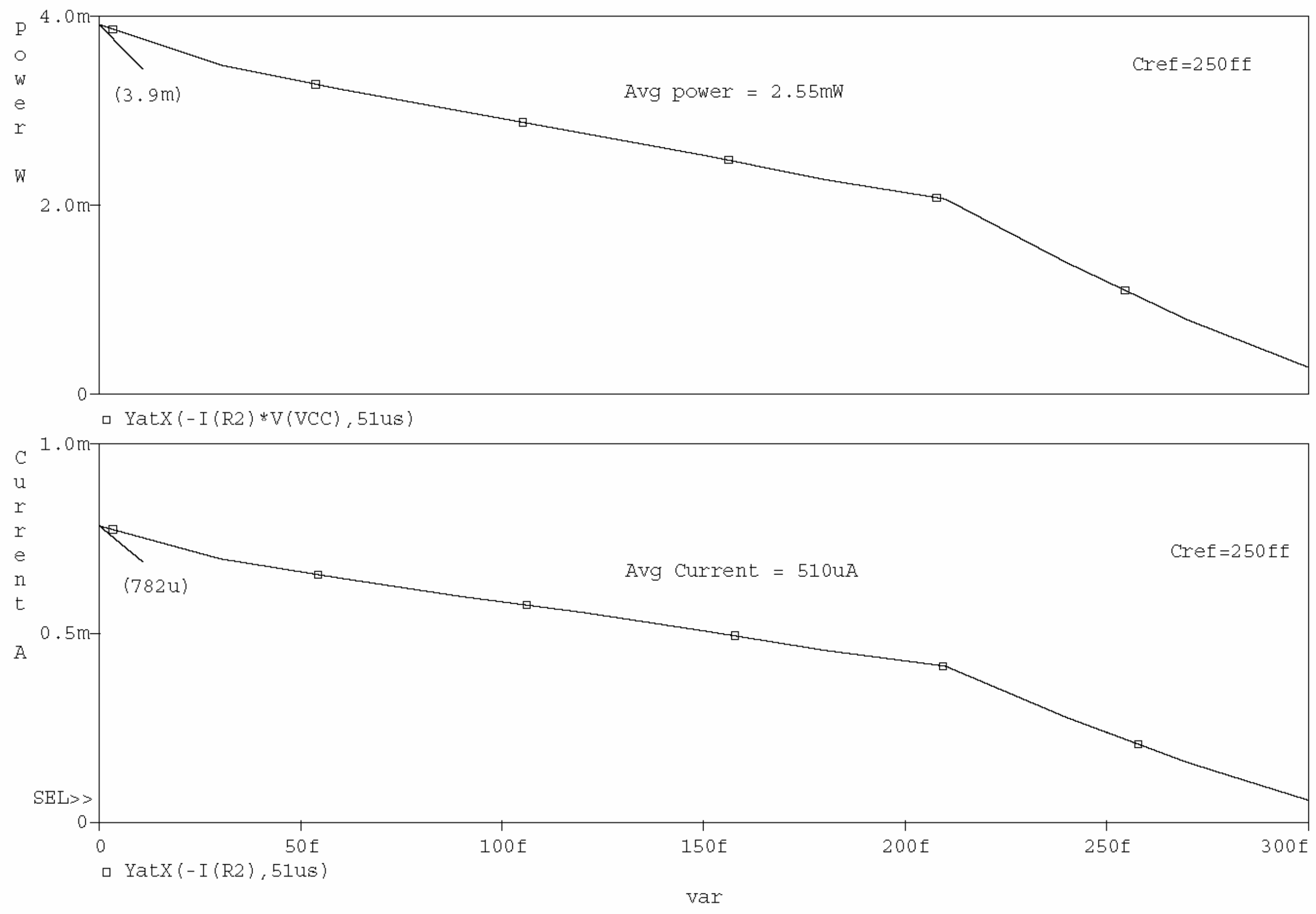


Figure 4.40: Simulated average current and power plots of the detection circuit with reference capacitor as 250ff. The sensor capacitor was swept from 1ff to 300ff. Bottom plot shows the current drawn and the top plot shows the power drawn by the detection circuit while driving an output load of 10pf.

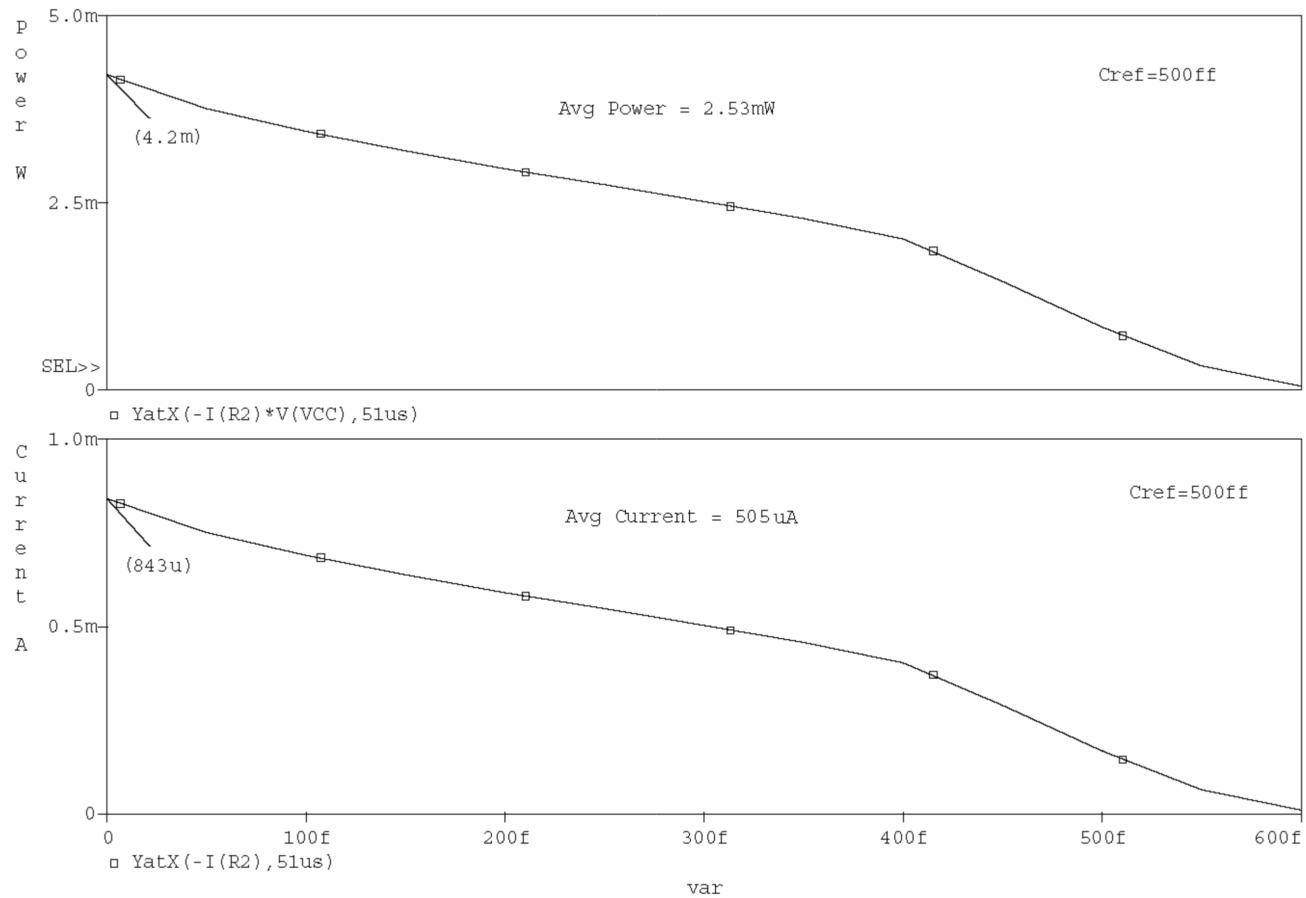


Figure 4.41: Simulated average current and power plots of the detection circuit with reference capacitor as 500ff. The sensor capacitor was swept from 1ff to 600ff. Bottom plot shows the current drawn and the top plot shows the power drawn by the detection circuit while driving an output load of 10pf.

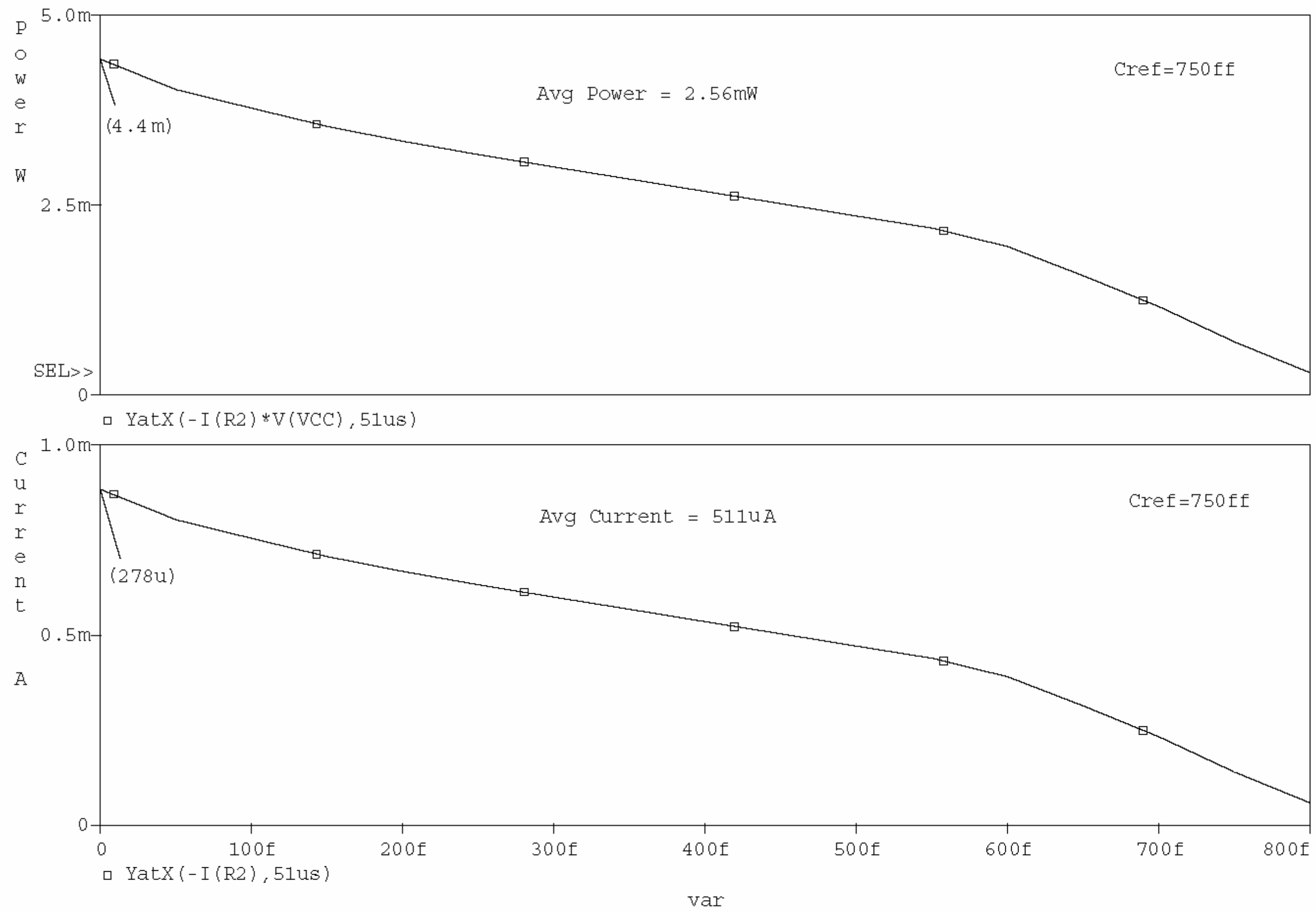


Figure 4.42: Simulated average current and power plots of the detection circuit with reference capacitor as 750ff. The sensor capacitor was swept from 1ff to 800ff. Bottom plot shows the current drawn and the top plot shows the power drawn by the detection circuit while driving an output load of 10pf.

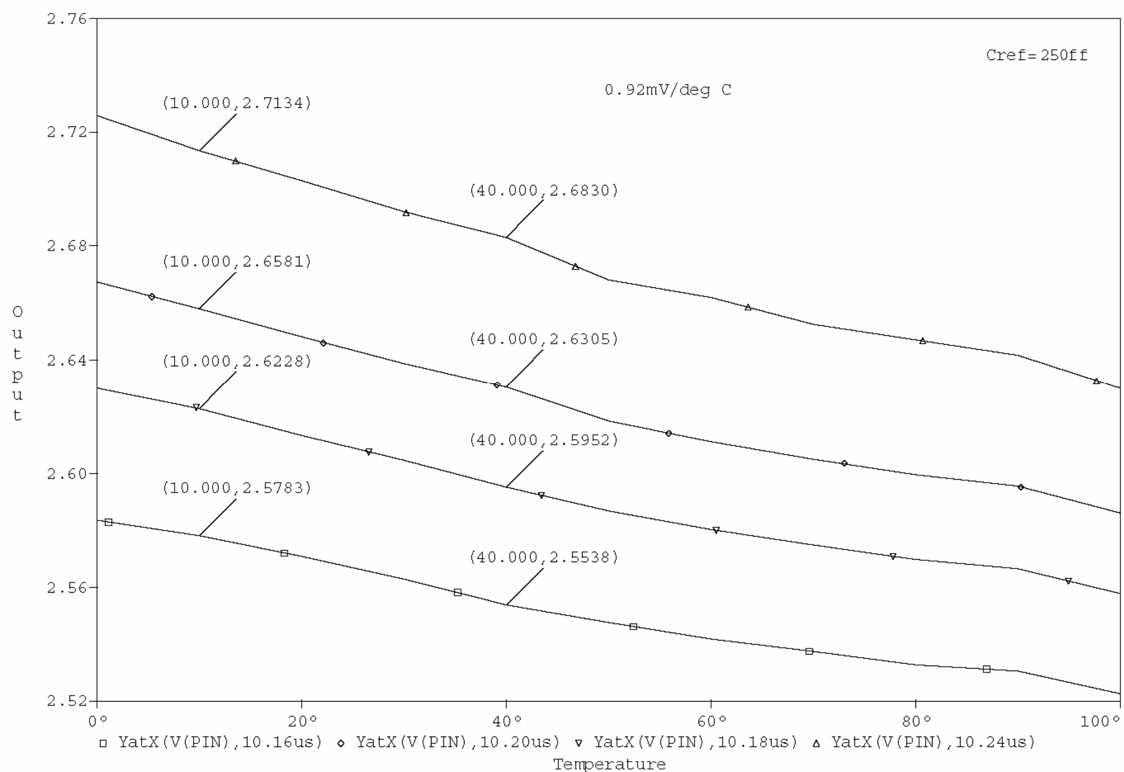


Figure 4.43: Simulated temperature response plot of the detection circuit. The simulation temperature was swept from 0 to 100 ºC, C_{ref} = 250ff, C_s = 5ff, circuit load = 10pf. The plot shows the output response to temperature at various simulation times.

The response of the detection circuit to temperature variations was simulated as shown in Figure 4.43. Temperature simulations were performed with the sensor capacitance kept constant at 5ff and the entire detection circuit driving an external load of 10pf. The output voltage at various simulation times was plotted against temperature. The detection circuit with reference capacitance of 250ff shows an output change of 0.92mV for every ºC change in temperature. Analogous simulations were performed for reference capacitors 500ff and 750ff. The detection circuit with 500ff showed a response of 1.97mV per ºC and the one with 750ff showed a response of 2.58mV per ºC changes in temperature. These local output variations of the detection circuit with temperature changes can be minimized by having a well matched detection circuit pair as suggested earlier.

4.8. Fourth Generation Mask layout design

The mask layout design was carried out in a similar fashion as the previous fabrications for AMI 1.5µm process. The main variations from the previous designs are the proximity of the sensor sites to the circuit, different sizes for reference capacitors and also increased buffer transistor sizes. The layouts of the three variations in detection circuits are shown in Figures 4.44 to 4.46. Instead of having a simple two-wire metal termination at the sensor sites, the two wires that would connect to the FIB deposited sensors were defined to form a range of geometries which would have fringing capacitance because of their proximity to each other. These metal geometries connected to the detection circuit by themselves can act like sensors picking up changes induced to their fringing fields. The sensitivity would only improve when platinum FIB micro structures are deposited and wired to these structures. Examples of these designed top metal (metal2) structures and their dimensions are shown in Figure 4.47. The central smaller square in these structures are generally connected to the detection circuit.

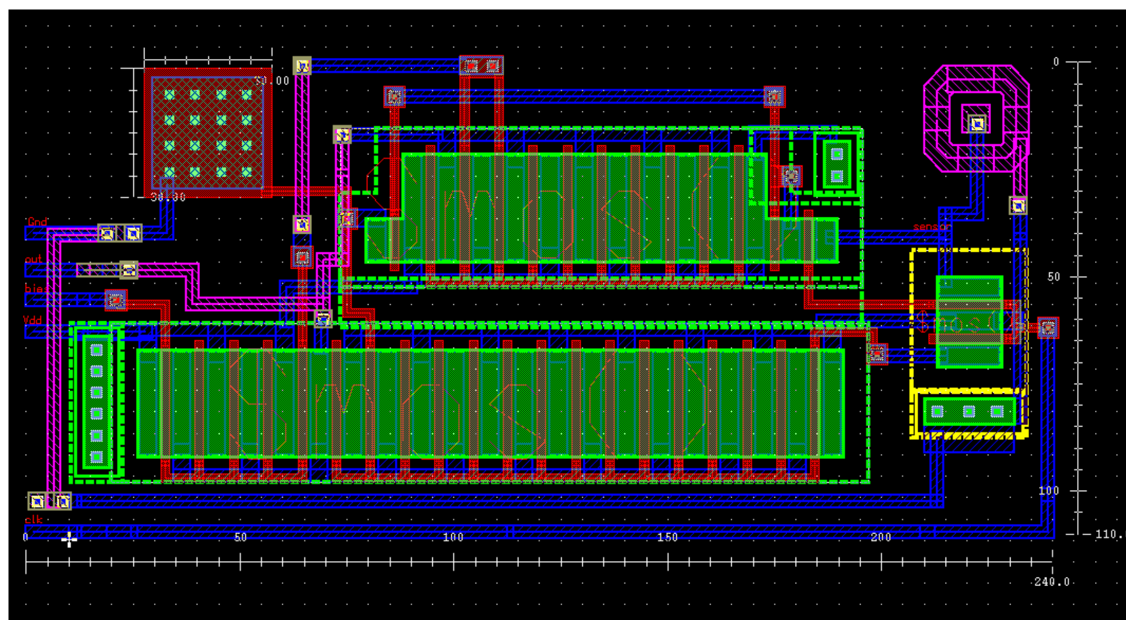
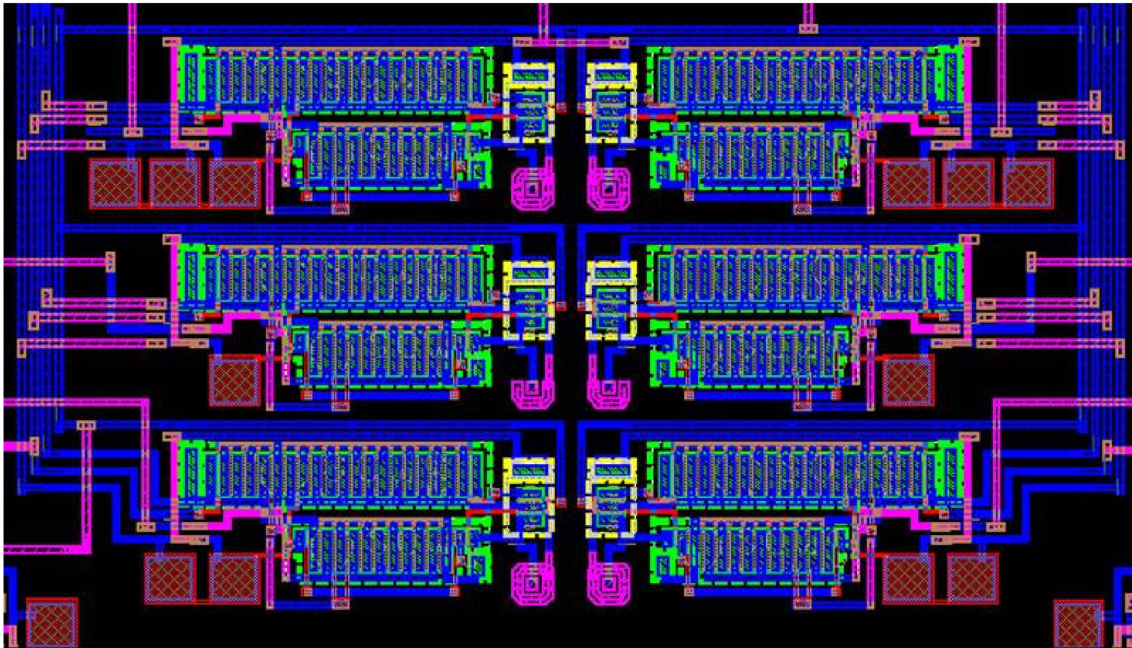


Figure 4.44: Mask layout of detection circuit (4th gen) with 250ff reference capacitance. Area of the layout = 240λ ×110λ or 192µm×88µm.

Figure 4.45: Mask layout of detection circuit (4th gen) with 500ff reference capacitance. Area of the layout = 250λ ×110λ or 200μm×88μm.

Figure 4.46: Mask layout of detection circuit (4th gen) with 750ff reference capacitance. Area of the layout = 285λ ×110λ or 224μm×88μm.

Figure 4.47: Mask layout of typical sensor sites in 4th generation chips.



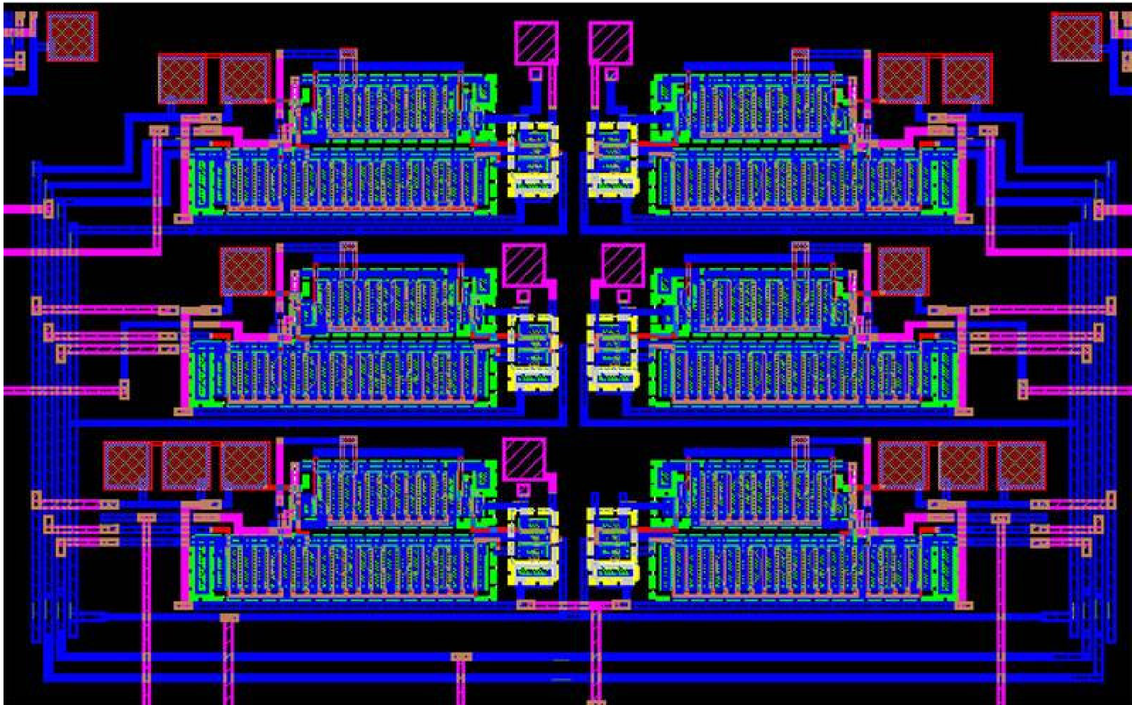


Figure 4.48: Mask layout of quadrant 1 and 3 with three detection circuit pairs with sensor sites.

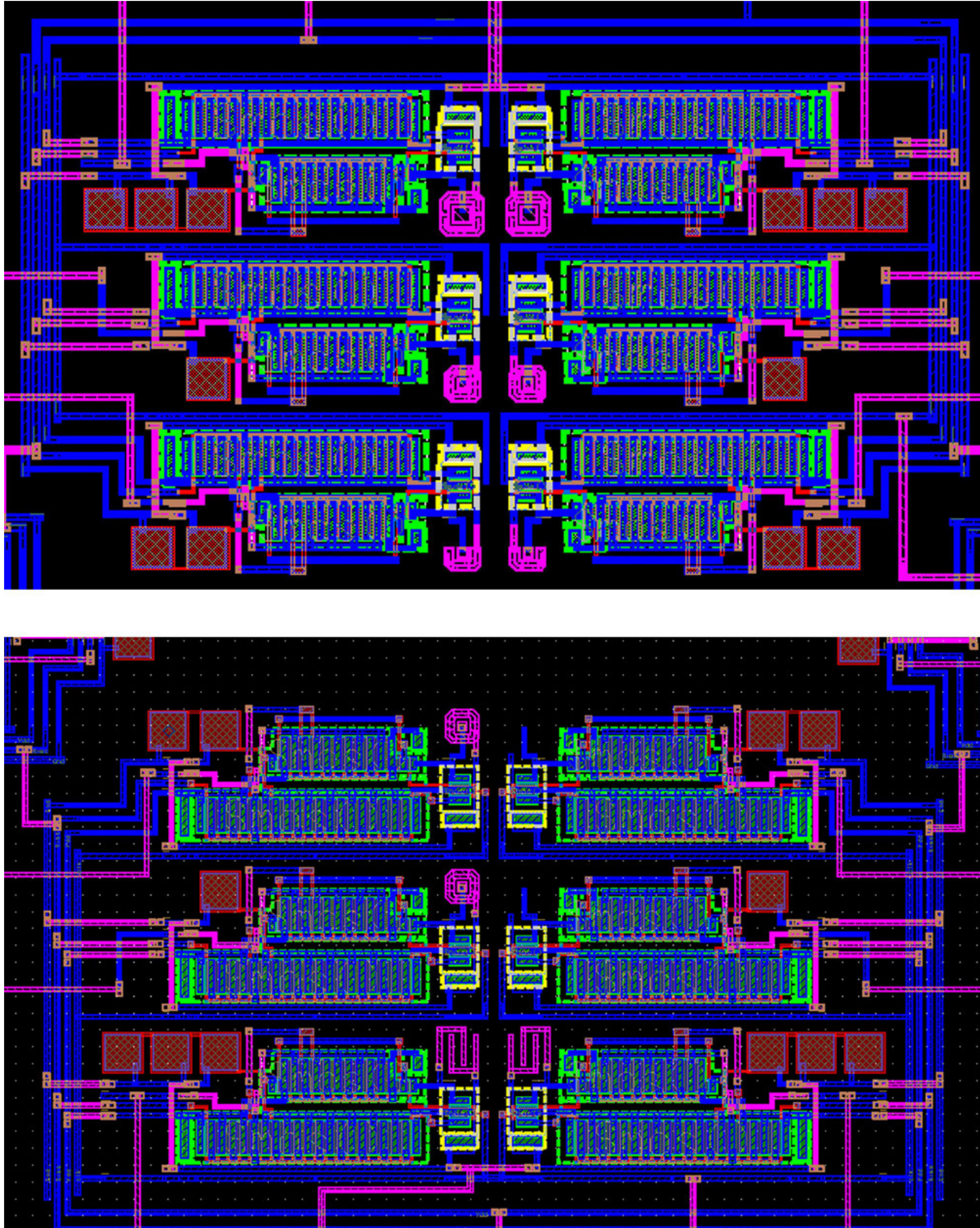


Figure 4.49: Mask layout of quadrant 2 and 4 with three detection circuit pairs with sensor sites.

Detection circuits with the same sized reference capacitors have been arranged as opposing pairs and three such pairs were grouped together to form a quadrant. Thus formed quadrants are shown in Figures 4.48 and 4.49. Some of the sensor sites have been left bare

with no top metal structures. When the output of the detection circuit with no metal2 structures is compared to the output of the opposing circuit with the structures, the difference signal should help qualify the fringing capacitance of these metal2 structures, provided the circuits are well matched. Figure 4.50 shows the complete layout of the 2.2mm×2.2mm die using 40-pin pad-frame. There are a total of 24 individual detection circuits defined as 12 detection circuit pairs in four quadrants. Each quadrant has its own V_{DD}, ground pad and clock input so that they can be switched independent of the other quadrants. A common bias pin supplies the bias to all the detection circuits in the chip. Twenty-five packaged (DIP40) and five unpackaged dies were fabricated to test the fourth generation circuit design.

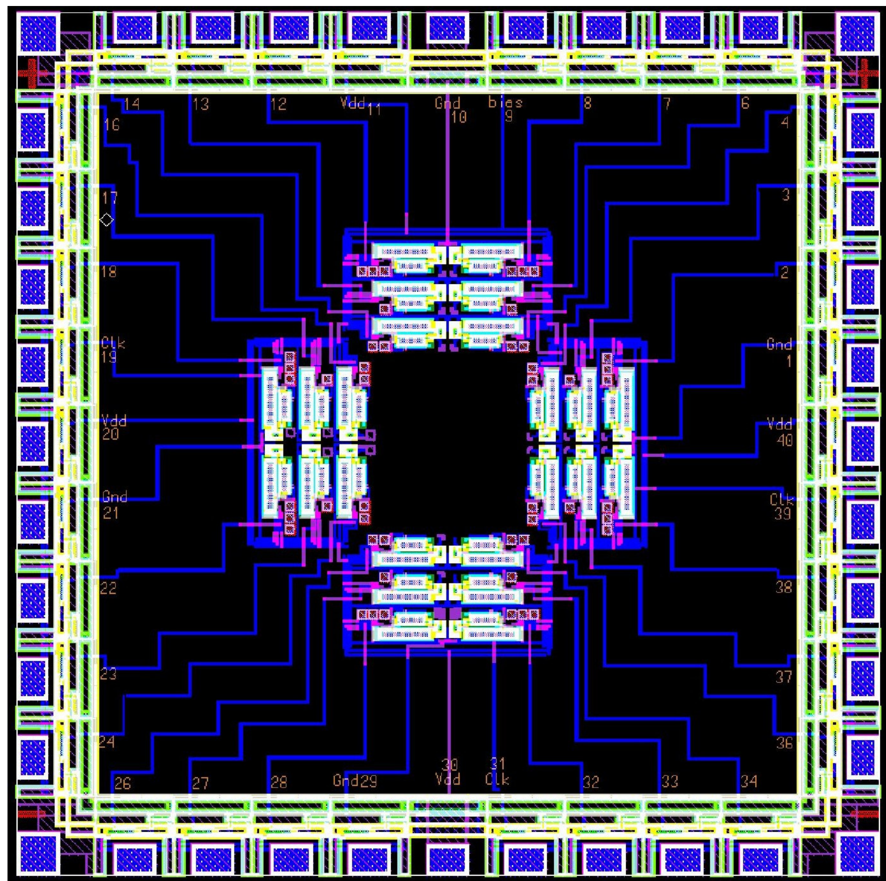


Figure 4.50: Mask layout of complete 4th generation chip with 24 sensor sites and dedicated detection circuits.

Two types of detection circuit techniques that are sensitive to sub femto farad changes in sensor capacitance were designed. One of the designed detection circuits converts the change in sensor capacitance to changes in frequency of a square wave output. This detection circuit scheme has wider input dynamic range and can be used in applications were the capacitance swing is large but at the sacrifice of gain. The second detection circuit technique converts the changes in sensor capacitance to amplitude variations. This detection circuit method has a maximum limit for the sensor capacitance value. Two generations of chips, third and fourth were designed using this technique. So a range of detection circuits with limits varying from 250ff to 750ff were developed to preserve input dynamic range. The detection circuits in the fourth generation of chips were designed in pairs to enable measure the difference signal between them to gain noise immunity.

5. Post Fabrication Testing

5.1. First Generation Design

An optical micrograph of a fabricated first generation chip is shown in Figure 5.1. The top surface of the fabricated chip has an insulation layer of silicon dioxide and silicon nitride for electrical isolation and for physical protection of the underlying layers from the environment. These insulation layers are optically transparent and hence the underlying circuit structures can be clearly identified. Figure 5.2 shows the center of the die where the FIB deposited sensors would be fabricated with interconnects leading to corresponding individual detection circuits.

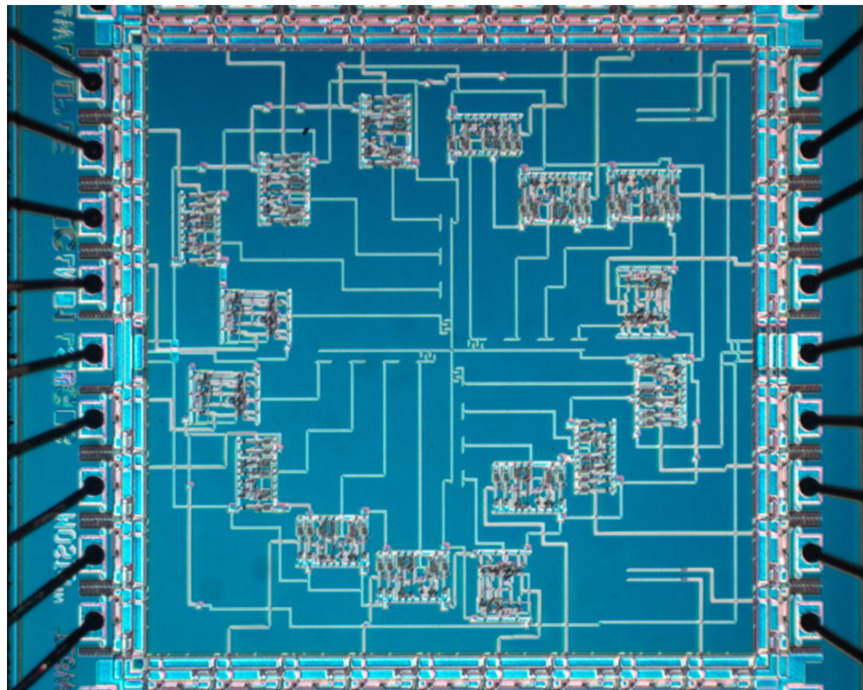


Figure 5.1: Optical micrograph of 1st generation chip.

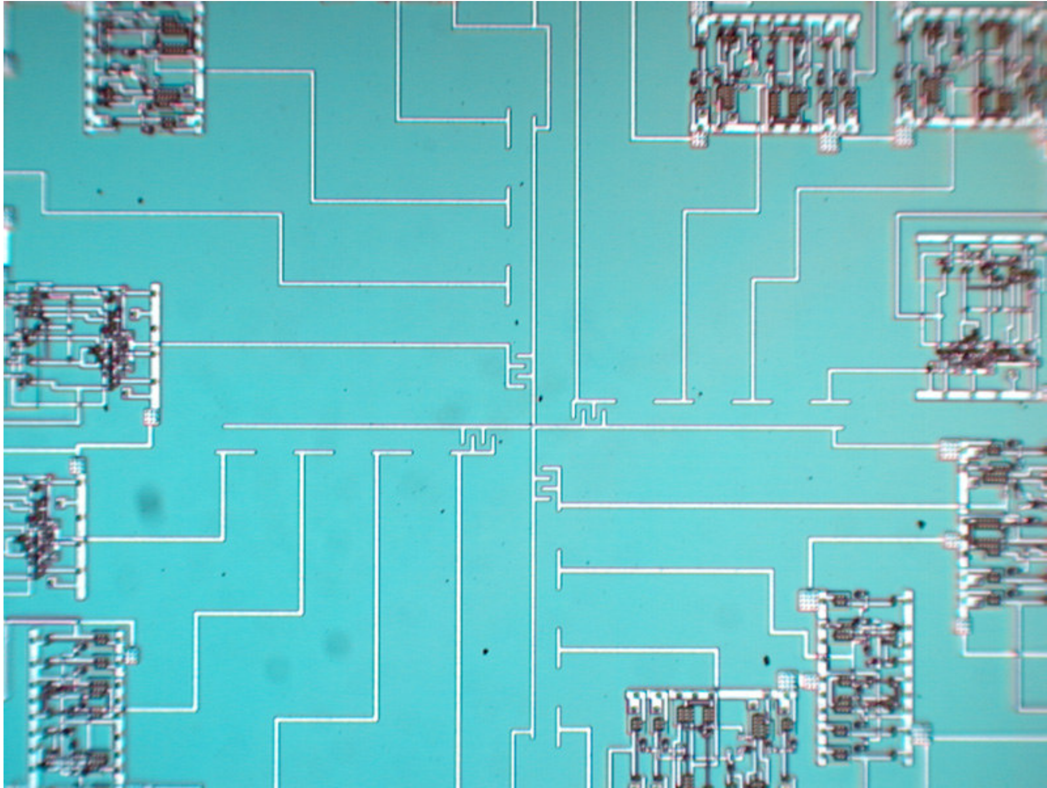


Figure 5.2: Optical micrograph of center of 1st generation chip showing sensor connect sites.

The chips were tested for functionality without the fabrication of the sensors initially. The parasitic capacitance presented by the metal interconnects that connects the sensor sites to the detection circuit should be sufficient to set the circuit into oscillation. Since the chips do not require any complex inputs, biases etc., they were tested on a general circuit breadboard with 5V (V_{DD}) supply provided by a DC power supply (Agilent E3645A) and outputs were monitored on a digital storage oscilloscope (Hitachi VC-6155). It was observed that none of the detection circuits showed a square waveform output as expected from the design. Instead, all of the 16 detection circuit channels showed a constant DC voltage varying between 2.3V to 2.7V. The detection circuits were not functioning as desired. All of the ten chips fabricated in this generation exhibited the same output response behavior. With the assumption that the circuit was not initializing in the proper state, a FIB deposited parallel plate capacitor was fabricated and wired to one of the detection circuits (40μA charging current) to see if this sets the circuit to oscillation. The deposited platinum plate

capacitor consists of eight platinum walls with each plate 15µm in length and 3µm tall as shown in Figure 5.3. The distance between the plates was 1µm. Alternating plates were connected to either the ground plane or to the interconnect from the detection circuit to form a gang capacitor. The estimated air capacitance for this sensor is 2.8 femto farads which was calculated using Eq-5.1

$$\text{Cap} = (n-1)\frac{\varepsilon_r \varepsilon_o A}{d}$$

Eq-5.1: Gang capacitance equation.

Where n is the number of plates (8), ε_r is the relative permittivity of the material between the plates, ε_o is the permittivity of space (8.854 × 10-12 F/m), A is the area of each individual plate (45µm^2), and d is the distance between the plates (1µm). In this case, the material between the plates is air whose relative permittivity is 1.00054.

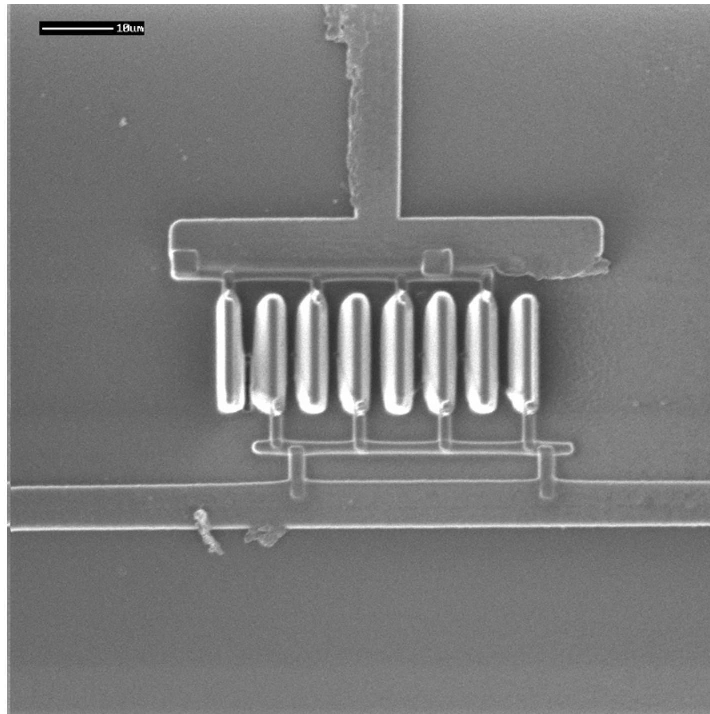


Figure 5.3: Scanning electron microscope (SEM) micrograph of FIB platinum sensor.

Post FIB sensor fabrication testing of the detection circuit exhibited similar behavior as before with a constant DC output of 2.4V. This implied that the problem area was most likely in the design of the circuit itself.

The micro editing capabilities of the FIB could be used to analyze individual components or sections of the circuit and can help isolate the problem areas. The FIB work-station was used to isolate an inverter in one of the detection circuit to check if at least one portion of the chip was functioning as designed. This was done by milling and isolating the input and output interconnects of the inverter which was connected to the rest of the detection circuit. The isolated input and output nodes were then connected to the metal traces that were specifically designed for post fabrication debugging as explained in Chapter 4. Vias were milled at the connection sites and they were filled with platinum deposited by the FIB. Electrical connection between the inverter and debug traces were achieved by depositing platinum traces (0.5µm thick) from these vias to the interconnects that lead to output pins. Figure 5.4 shows the metal traces that lead to the output pads, X marks the areas where vias were milled and the (red) lines depict the platinum traces that were deposited.

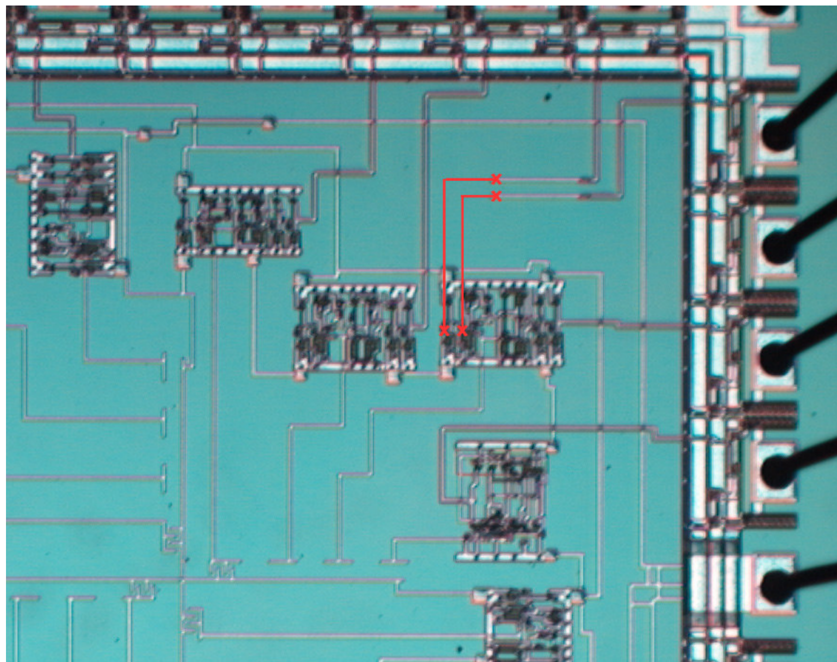


Figure 5.4: Optical micrograph showing FIB circuit editing scheme.

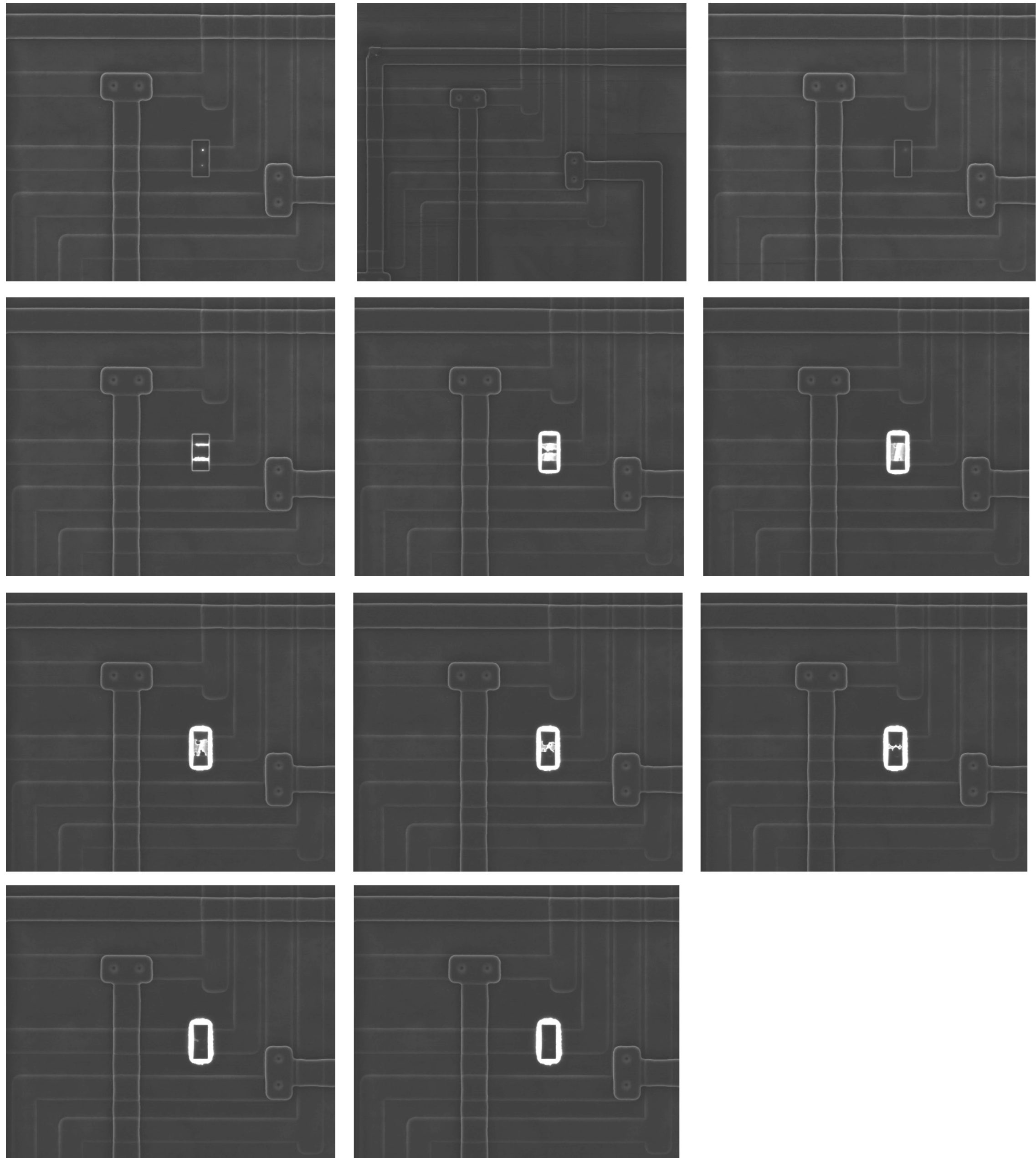


Figure 5.5: Secondary electron images from the FIB workstation showing inverter isolation.

The above figure shows snapshots of the FIB workstation in the process of micro-machining and disconnecting a buried metal interconnect which is connected to the inverter. The bright region along the perimeter of the defined mill area (2.5μm×6μm) in Figure 5.5 is caused by the re-deposition of the sputtered metal as the FIB mills through the metal

interconnect. Vias are made by milling 2μm×2μm holes on the desired interconnect to expose the buried metal and then platinum is deposited into the milled voids to establish connection to the buried metal. The vias were generally made 10μm away from the isolation cuts to avoid any unwanted high resistance paths that may be created by the re-deposited material.

The input of the inverter was connected to a signal generator and output was monitored for varying input frequency (5V square wave input, 50% duty cycle). It was observed that the inverter response deviated from normal at frequencies greater than 1 MHz and at frequencies greater than 5 MHz the output reduced to a constant DC voltage of 2.4V similar to the output observed from the complete detection circuit. Hence, the output pad of the circuit can drive the load of the connected oscilloscope only at frequencies less than 1 MHz. A half meter RG-6 coaxial cable was used between the chip and the digital oscilloscope whose load is estimated to be 67pf [40]. This length was reduced to quarter meter to reduce the load capacitance seen by the chip. The reduced length of the coaxial wire improved the frequency response of the inverter confirming that the output driver was not capable of driving the presented loads efficiently at frequencies greater than 1MHz. The pad-frame used during design and layout of this generation of chips was from a library provided by MOSIS which was not designed for high frequency operations. This was a design oversight and also no specific output drivers were incorporated in the design which would have prevented this behavior.

However, the circuit parameters of the modules used in the design of the detection circuit are dependent on the supply voltage V_{DD}. Therefore, scaling down the power supply would reduce the charging current supplied by the current source and also scale the set points of the Schmitt trigger which is directly related to the supply voltage as defined by Eq-4.1 in chapter 4. With the reduced current from the current source, the sensor capacitor would charge and discharge at a slower rate and hence the frequency of operation of the whole detection circuit would be reduced. When the supply voltage was reduced to 1.15V, the maximum frequency of operation was determined to be 50 KHz which is well below the maximum driving limits (1 MHz) of the output stage. The simulated frequency output response of a typical detection circuit with reduced supply voltage of 1.15V is shown in

Figure 5.6. This reduced power supply allows for the detection circuits in the 1st generation chips to operate in a desired mode but only at the sacrifice of sensitivity (0.53 KHz per femto farad change).

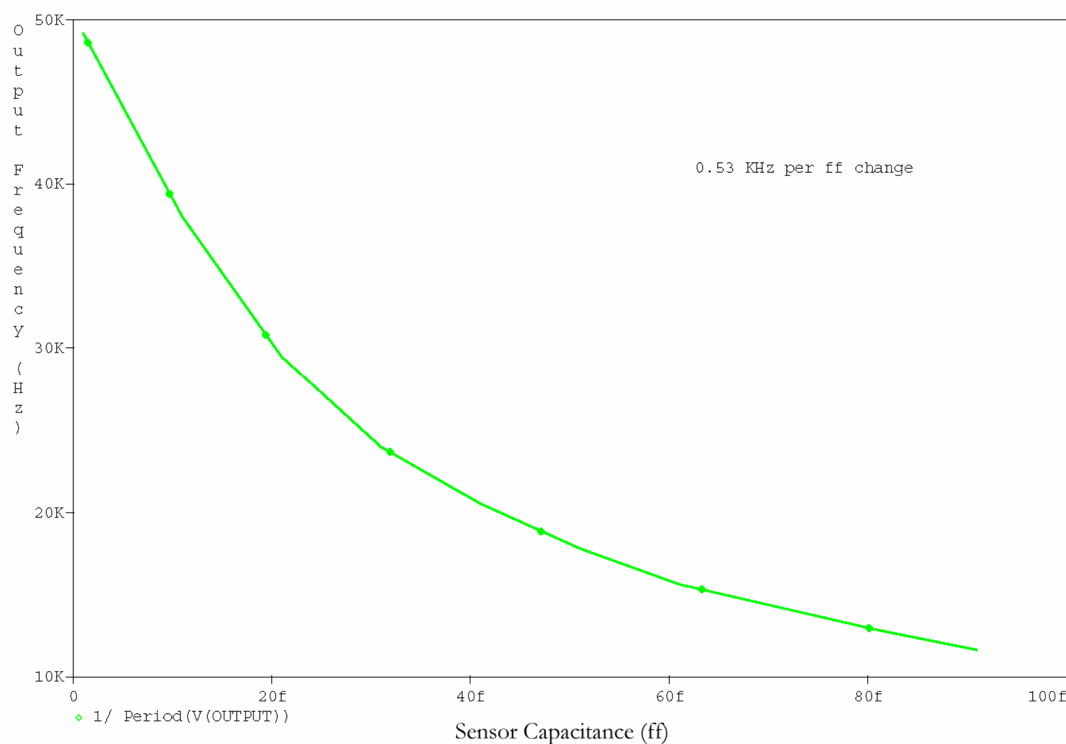


Figure 5.6: Output frequency vs. sensor capacitance plot with reduced supply voltage 1.15V.

The supply voltage was reduced to 1.15V and the outputs of the detection circuits were found to be a pulse stream output signal as designed. The frequency, or the time period of the pulse stream (square wave) output without any FIB platinum sensors, is dependent only on the parasitic interconnect capacitance. The measured outputs from various detection circuits are in agreement with this and are shown in Figure 5.7. Detection circuits 1, 2 and 3 have the same circuit topology with identical current sources, but the measured output time periods were not identical. These are marked in Figure 5.7. Circuit 1 has the shortest time period and corresponds to the shortest interconnect length from the detection circuit to the sensor site. Circuit 3 has a longer interconnect, thereby higher parasitic capacitance which is reflected in the output as a longer time period. Similar behavior was exhibited by the second set of detection circuits 4 to 7 as shown in Figure 5.7. This shows that the detection circuits

are sensitive to small changes in capacitances and function as designed with a lowered power supply of 1.15V.

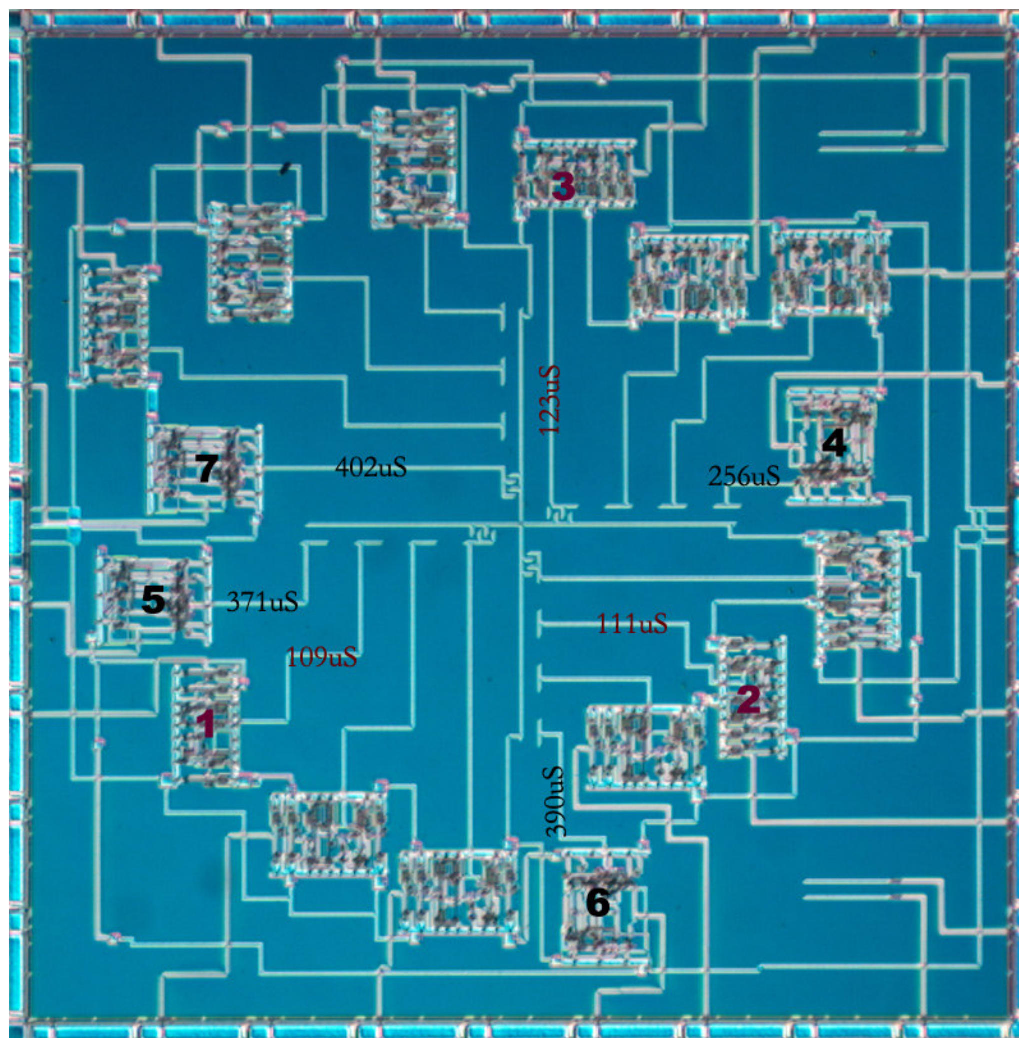
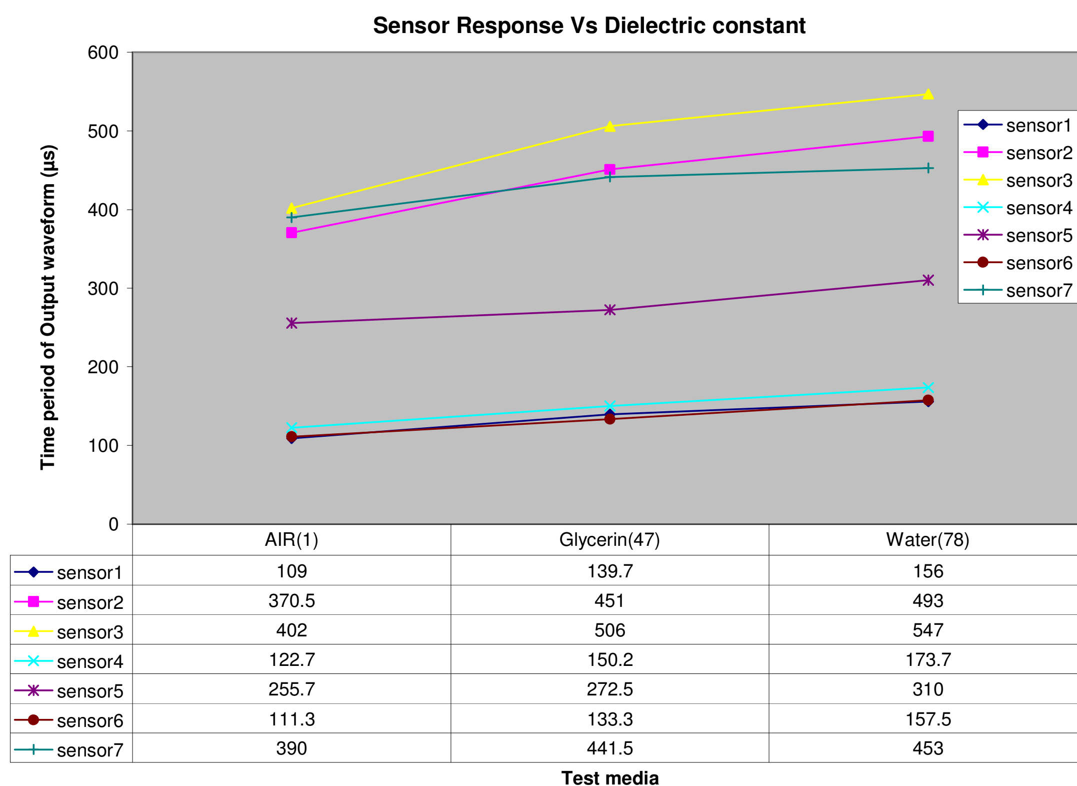


Figure 5.7: Optical micrograph showing output time period of multiple detection circuits for interconnect capacitance without any FIB deposited sensors.

The sensitivity of the chip to external dielectric changes can be determined by subjecting the sensor areas to test mediums with varying dielectric properties. We used glycerin and water with known dielectric constants of 47 and 78 respectively to determine the chip's response to these test solutions and whether their output were in relation to the dielectric constants of the test mediums. The tests were done with no platinum sensors, relying only on the parasitic fringing capacitances of the interconnects to sense the changes

in dielectric constant. This was done by delivering 0.5μl of the test solution using a micro pipette to the center of the chip where the sensor sites are located. After each test, the test solution was wicked using the micro pipette and the die surface was cleaned by delivering and wicking away de-ionized water multiple times till the surface appeared clean under an optical microscope. The output response of the circuit was observed and noted using a storage oscilloscope. The response plots are shown in Figure 5.8



	AIR(1)	Glycerin(47)	Water(78)
sensor1	109	139.7	156
sensor2	370.5	451	493
sensor3	402	506	547
sensor4	122.7	150.2	173.7
sensor5	255.7	272.5	310
sensor6	111.3	133.3	157.5
sensor7	390	441.5	453

Figure 5.8: Output response vs. dielectric constant change with 1.15V V_{DD} supply.

The above plots show the output response of multiple detection circuits and each reading is an average of three measurements. The plots clearly show that the output time period increases with increases in the dielectric constant. This shows that the detection circuits can identify changes in the dielectric constant, confirming the principle of this detection technique.

The FIB workstation was used to fabricate a platinum sensor similar to the one shown in Figure 5.3. The output of the detection circuit, which is connected to the

fabricated sensor, was tested with a lower supply voltage of 1.15V. It was noted that the output was at a constant 0V with no square wave output implying that the fabricated platinum sensor could have a resistive path between the plates. To verify this, a simple two plate platinum capacitor (length = 25μm, height = 2μm, distance between plates = 12μm) was fabricated using the FIB and connected to the interconnects designed for debugging. The resistance between these two plates was measured using a digital multi-meter and was noted to be 3.94KΩ. This is a low resistance path and the deposited parallel plates act more like a resistor than a capacitor. This low resistance path is created by the scattered platinum that is deposited on either side of the sensor walls during fabrication of the sensor plates. The taller the sensor plates, the larger the scattered and re-deposited platinum area. This re-deposited thin platinum layer acts like a low resistance path between the sensor plates, which is not desirable. This thin platinum layer between the plates can be milled away using the FIB. Figure 5.9 shows the parallel plates of the fabricated sensor structure with a thin re-deposited platinum layer between the plates removed by FIB milling. The remnant of the thin platinum film can be seen closer to the left plate. The FIB milling was continued until the entire layer was removed.

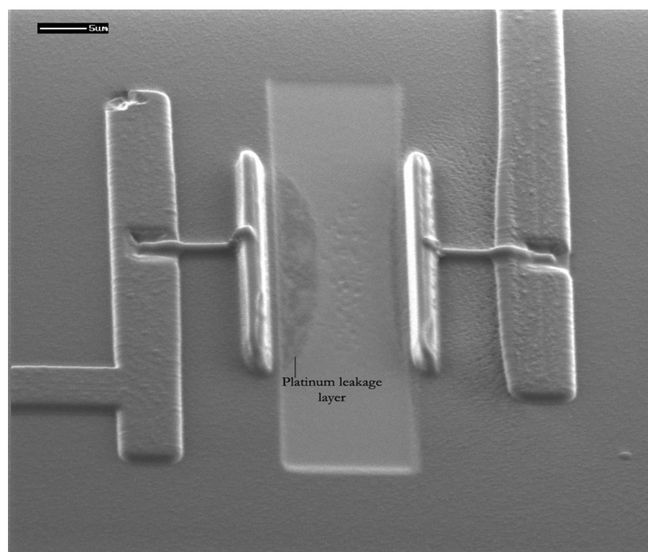


Figure 5.9: Test sensor structure showing platinum leakage path and FIB milling area.

The resistance between the plates was measured after FIB clean-up and was noted to be 4.1MΩ. Hence the FIB cleanup step is essential for proper functioning of the sensors. Multiple sensor structures were fabricated and tested for functionality after the FIB cleanup

process. One such fabricated sensor is shown in Figure 5.10 and its response to different mediums in comparison to a detection circuit with no platinum sensor is shown in Figure 5.11.

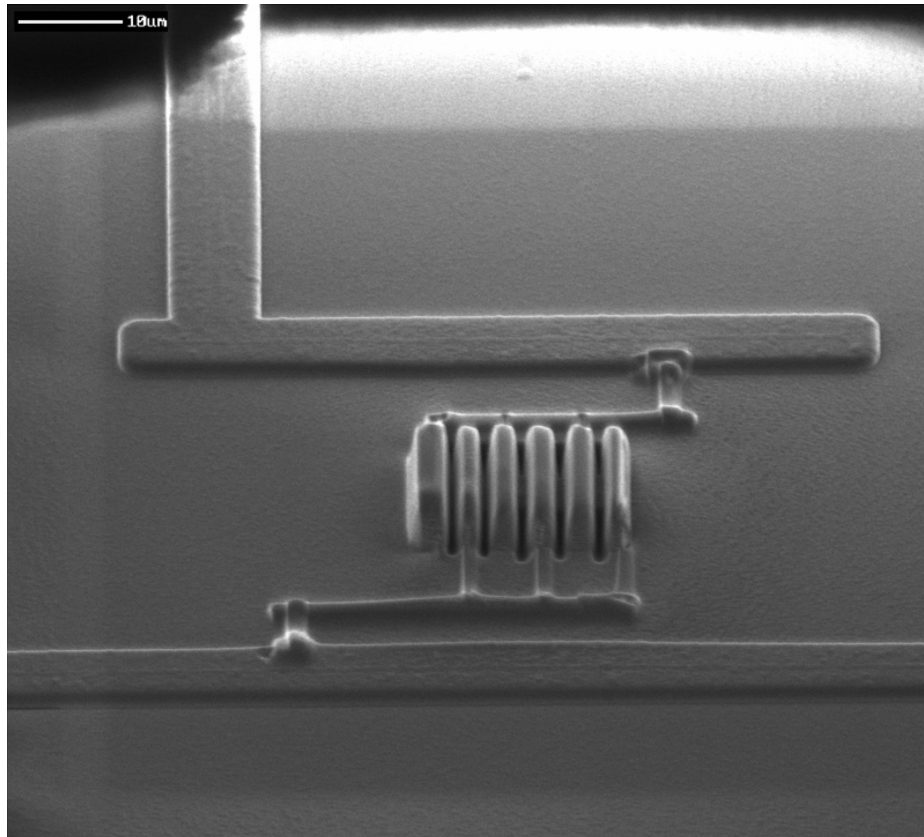
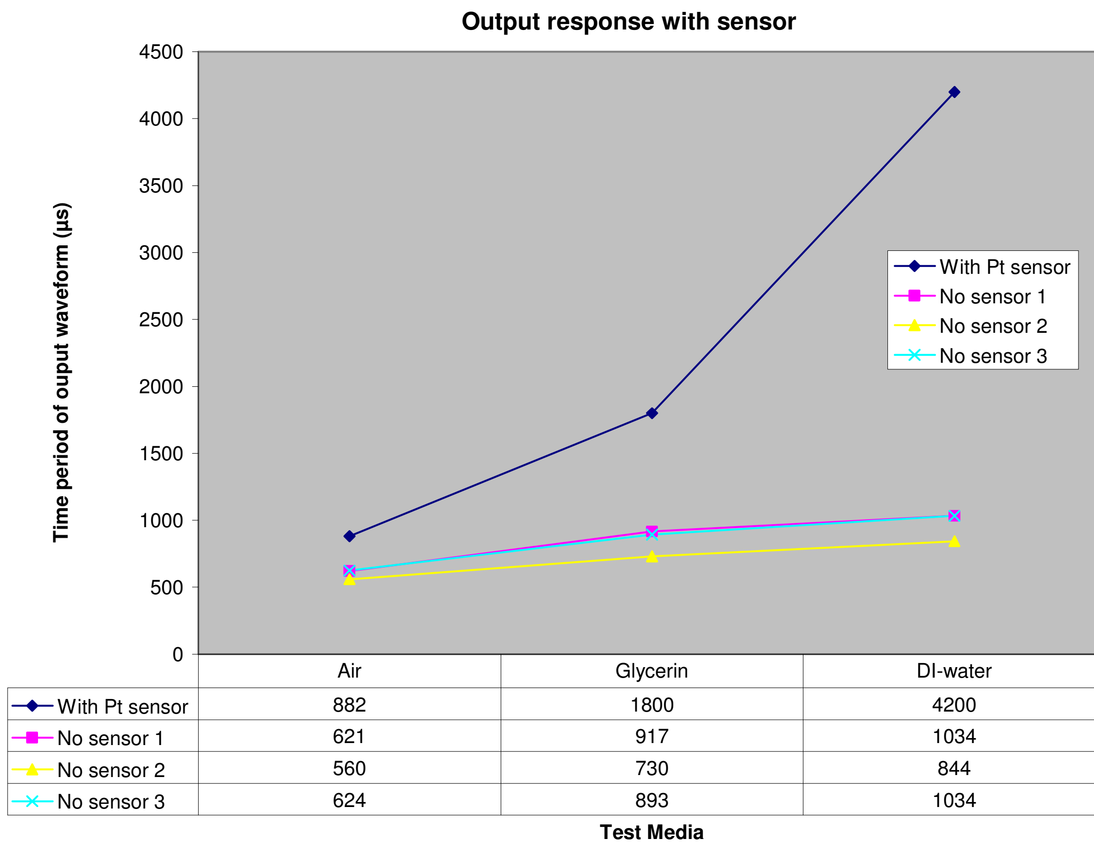


Figure 5.10: Scanning electron microscope (SEM) micrograph of FIB platinum sensor after cleanup between sensor plates.

It can be seen from Figure 5.11 that the response of the detection circuit is more pronounced with the FIB deposited sensor. Different sensor structures have been fabricated and tested with the same dielectric test mediums. All of the fabricated sensors show an improved response in comparison to just the fringing capacitance of the interconnects. Figure 5.12 shows multiple sensor structures fabricated on the same chip.



	Air	Glycerin	DI-water
With Pt sensor	882	1800	4200
No sensor 1	621	917	1034
No sensor 2	560	730	844
No sensor 3	624	893	1034

Figure 5.11: Output response vs. dielectric constant with FIB fabricated sensor.

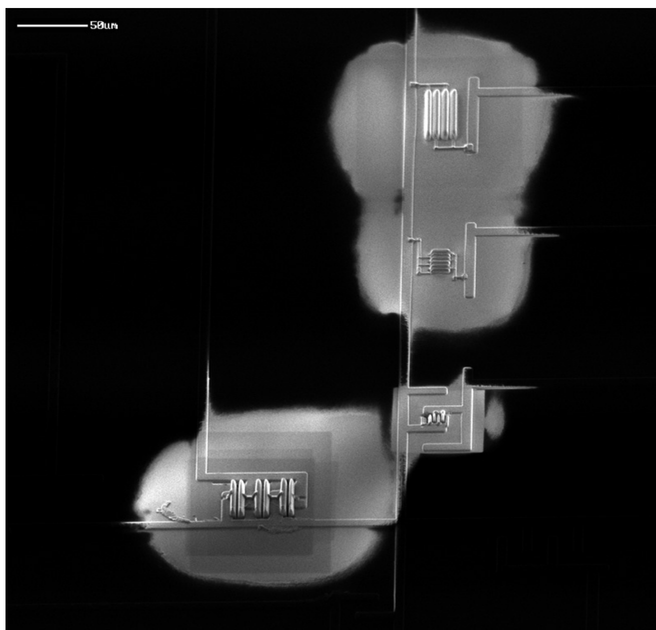


Figure 5.12: SEM micrograph of multiple FIB sensor structure on same chip.

The first generation design of chips shows that the detection circuits are sensitive to changes in dielectric constant. They can be used as a test platform for developing detection techniques to identify target molecules after the sensor sites are treated with the target selective materials. However, this design does not address variations in ambient temperature and noise. These noise factors can be estimated and subtracted from the actual reading by measuring the output of a redundant detection circuit with the sensor site not treated with the selective layer. Any common variation signal between the redundant circuit and the actual measuring circuit can be subtracted as noise.

The detection circuit's behavior and output signal is dependant on having a stable power supply thereby having poor power supply rejection ratio (PSRR). Future circuits should be designed with this in mind and have a charging current source that is less sensitive to variation in power supply. Post processing of the output to measure only the difference signals between a pair of detection circuits to minimize common noise on chip would require converting the output signals to simple analog signals. Since the output information is in the time domain, to build post processing circuits on chip would generally require complex area consuming circuits. Post processing would be easier if the output information is in the form of amplitude variations and was the basis for designing the third and fourth generation of chips.

5.2. Second Generation Design

This generation of chips was designed before the issue of improper output buffer size in the first generation was identified. The same issue plagues this generation of chips as well. However, the detection circuits in this generation of chips consist of simple ring oscillators, and lowering the power supply would make no changes to the circuit behavior. The oscillating frequency of the detection circuits cannot be lowered to a range that the designed output buffers can drive. All outputs of the detection circuits were found to be at a constant DC voltage and were not viable for detection application.

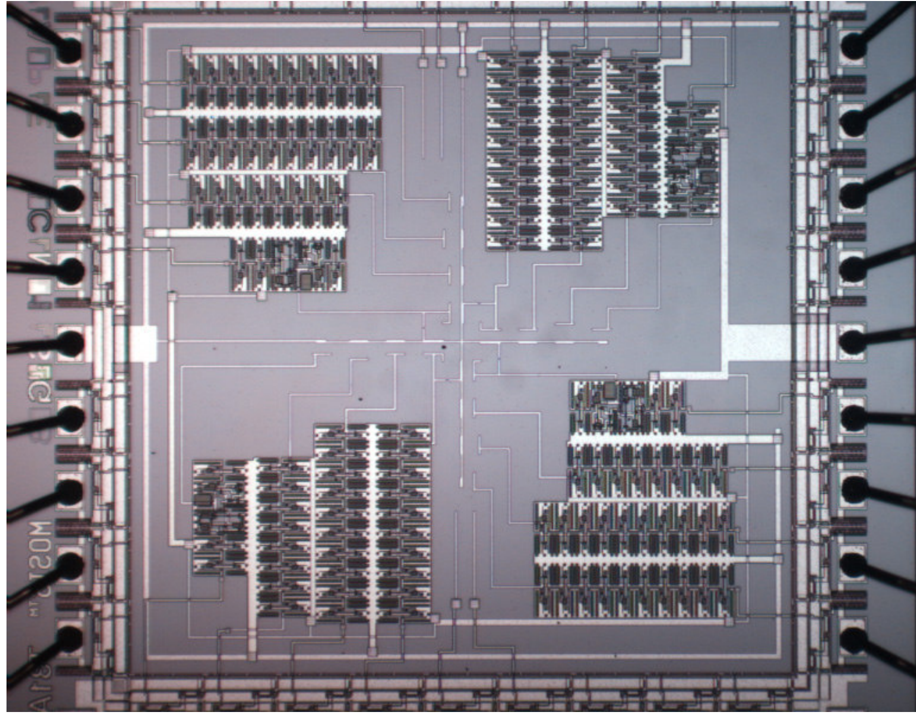


Figure 5.13: Optical micrograph of 2nd generation chip.

5.3. Third Generation Design

An optical micrograph of a fabricated third generation chip is shown in Figure 5.14. The detection circuits are located at the edges of the die and the sensor connect sites are at the center. This generation of chips requires an external bias supply and also a clock input. The chips were initially tested for functionality using a general purpose circuit breadboard. The bias voltage and supply voltage were provided by a DC power supply and the input clock from a signal generator. Initially, the supply Voltage V_{DD} was set at 5V, the bias voltage at 2.5V and the input clock frequency at 100 KHz to check the functionality of the chip. It was observed that all the detection circuits were functional and the outputs were square waves with a DC shift as designed. The DC shift is caused by the design of the output buffers using PMOS transistors to keep the circuit simple with less transistor count.

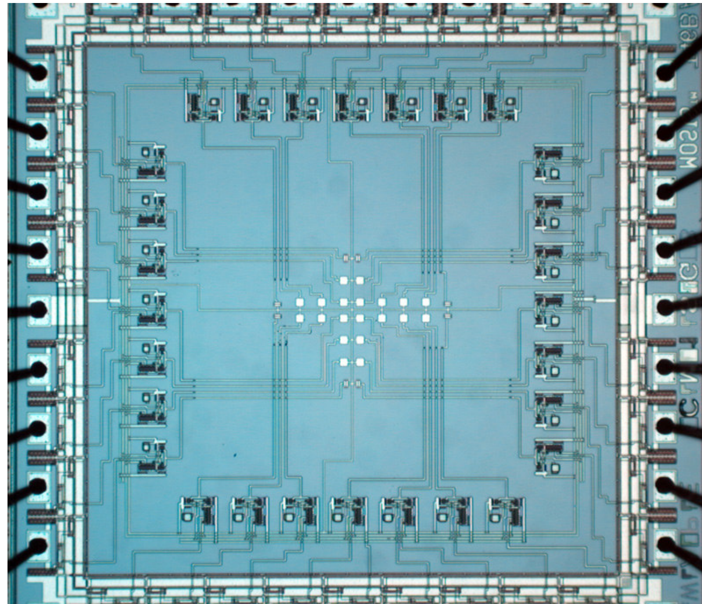


Figure 5.14: Optical micrograph of 3rd generation chip.

A typical output response of the detection circuit, as observed in a digital oscilloscope is shown in Figure 5.15.

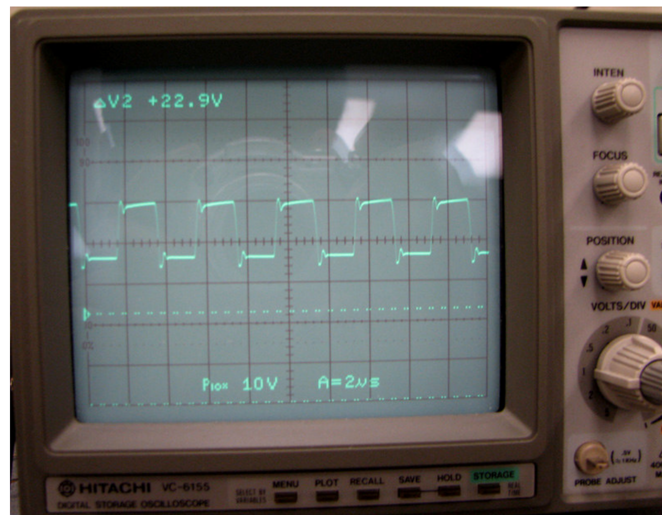


Figure 5.15: Output response of a typical detection circuit.

The amplitude of the pulse signal was designed to be directly proportional to the absolute capacitance at the sensor site (sensor + interconnect capacitance). As the incurred capacitance increases, the amplitude of the square wave would increase. This amplitude can

be measured directly by a digital multi-meter set to measure alternating current (AC) which would bypass the DC shift. The AC output amplitude of the detection circuits without FIB fabricated sensors were noted using a multi-meter. The output values of one of the chips were plotted on the layout as shown in Figure 5.16. It can be seen that the output amplitude is higher for circuits with longer interconnects running between the detection circuits and the sensor sites. This shows that the detection circuits are functioning as designed and are able to detect small changes in capacitance; in this case the capacitance of the connecting interconnects.

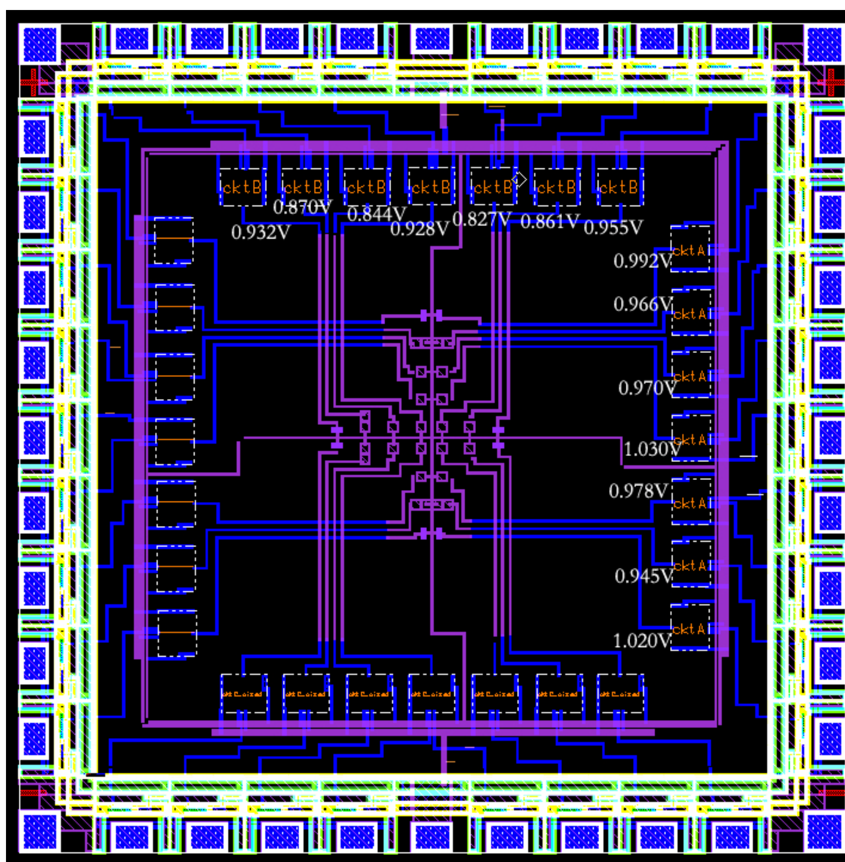


Figure 5.16: Mask layout showing output AC amplitude of multiple detection circuits for interconnect capacitance without any FIB deposited sensors.

The FIB workstation was used to deposit multiple sensor structures and the circuit was tested for functionality after the FIB cleanup process to remove any re-deposited platinum. One such fabricated sensor is shown in Figure 5.17. One of the plates of the

sensor capacitor is the buried ground metal2 (square structure in figure) and the other plate was made by depositing nine walls of platinum to form a cross link structure. Each platinum wall was made 2μm tall. These platinum structures were then connected to the interconnect that runs to the detection circuit by milling a via. The sensor was made this way so that there is electrical isolation between the two plates of the capacitor. Including multiple platinum walls on top of the buried plate increases the fringing capacitance of the sensor and can be more sensitive and responsive when exposed to dielectric changes.

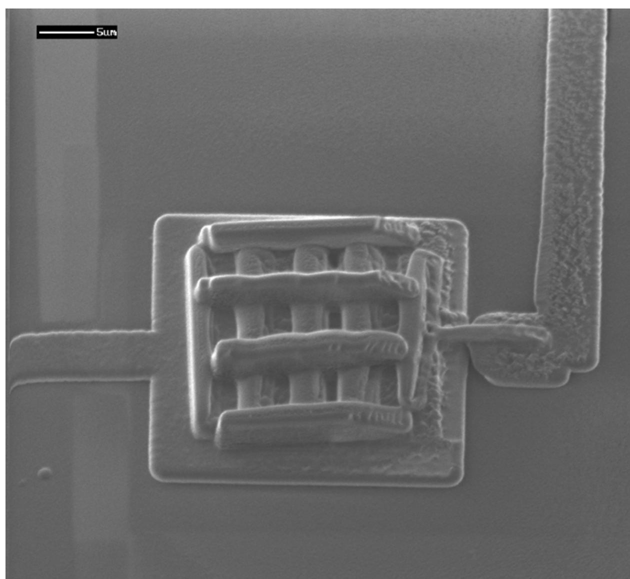


Figure 5.17: Secondary electron micrograph of FIB platinum sensor with buried 2nd plane.

The output AC amplitude of this sensor - detection circuit pair was 0.892V before the fabrication of the sensor, and was measured to be 1.059V after FIB sensor fabrication. Hence, the output change caused by the addition of the FIB platinum sensor structure is 167mV. The detection circuit to which this sensor was connected had the 350ff reference capacitor with a simulated gain of 7.85mV per femto farad change. This implies that the inclusion of the FIB platinum sensor increased the capacitance seen by the detection circuit by 21.3 ff. Measurements were performed on multiple sensor structures fabricated using the FIB, and similar responses were observed. This further confirms that the detection circuit can see femto farad changes in capacitance with ease. To determine the sensitivity of the chip to external dielectric changes, glycerin and water with known dielectric constants of 47

and 78, respectively, were delivered to the center of the die. These tests were performed with no platinum sensors, relying only on the parasitic fringing capacitances of the interconnects to sense the changes in dielectric constants similar to the tests conducted on the first generation of chips. The response of the detection circuits for glycerin was as expected, with the longer interconnects showing higher output amplitudes. But when the chip was tested with water, all the detection circuits showed a similar high response with the tops of the square waves clipped. This implies that the detection circuits' outputs were at maximum, caused by an input capacitance value equal or greater than the value of the reference capacitors used. The fringing capacitance of the long interconnects that run between the detection circuits (edges of die) and sensor sites (center of die) caused a capacitance change greater than the values of the reference capacitors used. The simulated plot of a detection circuit, shown in Figure 5.18 shows the regions of operation for glycerin and water along the gain slope.

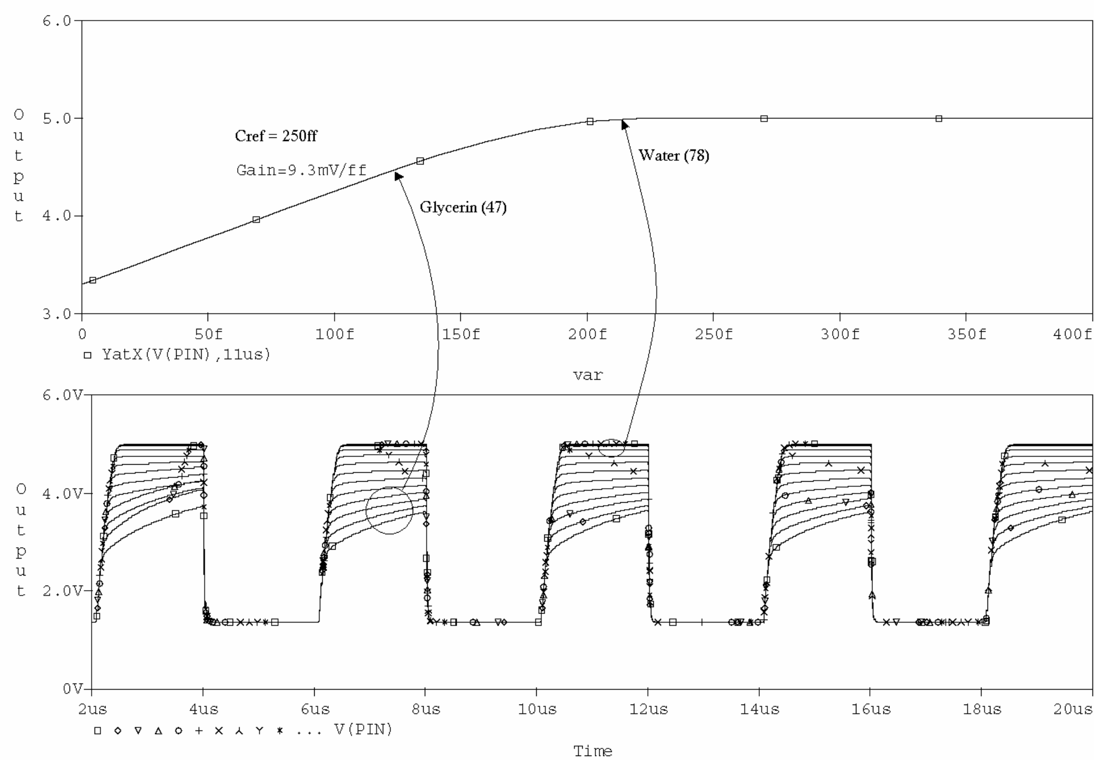


Figure 5.18: Gain plot of detection circuit with 250ff reference capacitor showing regions of operation for glycerin and water test mediums.

Since the detection circuit is already at its input maximum, it was not able to detect further dielectric changes in the test solution. To make this chip usable for detecting changes in aqueous medium, the lengths of the sensor interconnects must be reduced. This is not possible without re-fabricating an entirely new chip with a modified layout. Rather, it would be possible to functionalize this chip by limiting the area of the sensor interconnects exposed to the test solutions. A simple method was tried, where a thermal set nano-crystalline quartz epoxy composite (Gatan G1) was used to cover half of the lengths of the sensor interconnects and the center of the die was left exposed with no epoxy. The epoxy was painted onto the chip under a stereo microscope using a thin strand of copper wire extracted from a regular 22g stranded electrical wire. Care was taken not to cover the entire die, giving enough room for the epoxy to flow and expand while curing. The epoxy was cured in an oven at 70 ºC for 10mins. Figure 5.19 shows this scheme on the layout of the chip.

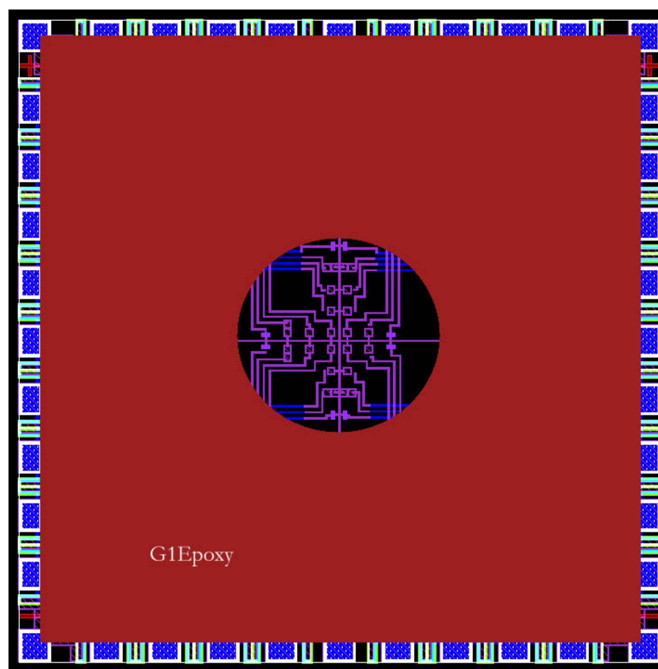


Figure 5.19: Layout of die showing areas covered by G1 epoxy.

The chip with the epoxy was tested with 0.5µl water dispensed onto the exposed regions of the chip. The output square waveforms were not clipped and exhibited amplitude

variations between the different detection circuits. Even within this small exposed area, output signal amplitudes were in agreement with the lengths of interconnects exposed. Longer interconnects showed higher amplitudes than shorter interconnects. This response proves that the exposed sensor interconnect lengths need to be shortened to prevent the detection circuits from saturating. Covering of the die surface with epoxy to expose specific areas of the chip is difficult to repeat. A more reproducible approach would be to build a reservoir on the center of the chip. Glass capillary tubes with 650μm internal diameter were sliced in 1.2mm lengths using a slow speed diamond isomet saw. The sliced cylinders were attached to the die using G1 epoxy and cured. Manual placement of the glass tube was difficult; hence a wire-bonding machine with a micro manipulator stage was modified for this purpose. The wire bonding tip was replaced with a wood adapter to hold the glass tubes while orienting the chip. G1 epoxy was applied to the bottom of the sliced glass cylinder, then centered over the die and carefully set onto the chip. The chip with the central reservoir was cured in an oven at 70 ºC for the epoxy to set. A chip with the attached glass reservoir is shown in figure 5.20.

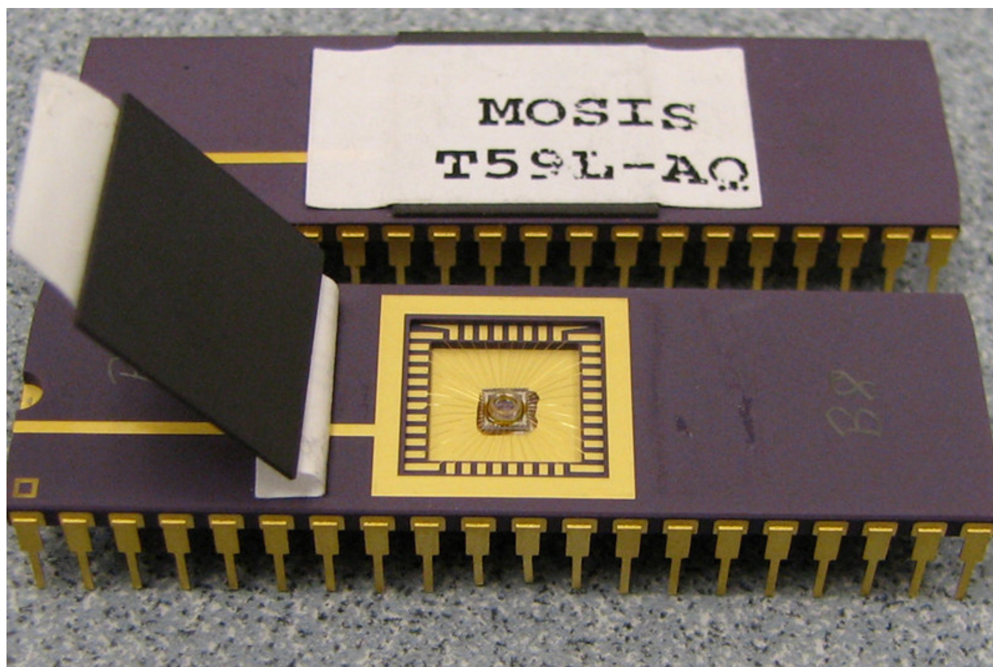


Figure 5.20: Chip with central glass reservoir.

Since the fringing capacitance of the sensor interconnects are high enough and are acting like sensors picking up dielectric changes above them, the addition of FIB micro fabricated sensors would only increase the response which would drive the detection circuits to saturation. Hence, for this generation of chips FIB deposited sensors are not necessary for liquid test mediums. The chips with the glass reservoirs were further tested with different easily available liquids whose dielectric constants were known. The response of one of the detection circuits with 350ff reference capacitor to various test solutions is shown in Figure 5.21.

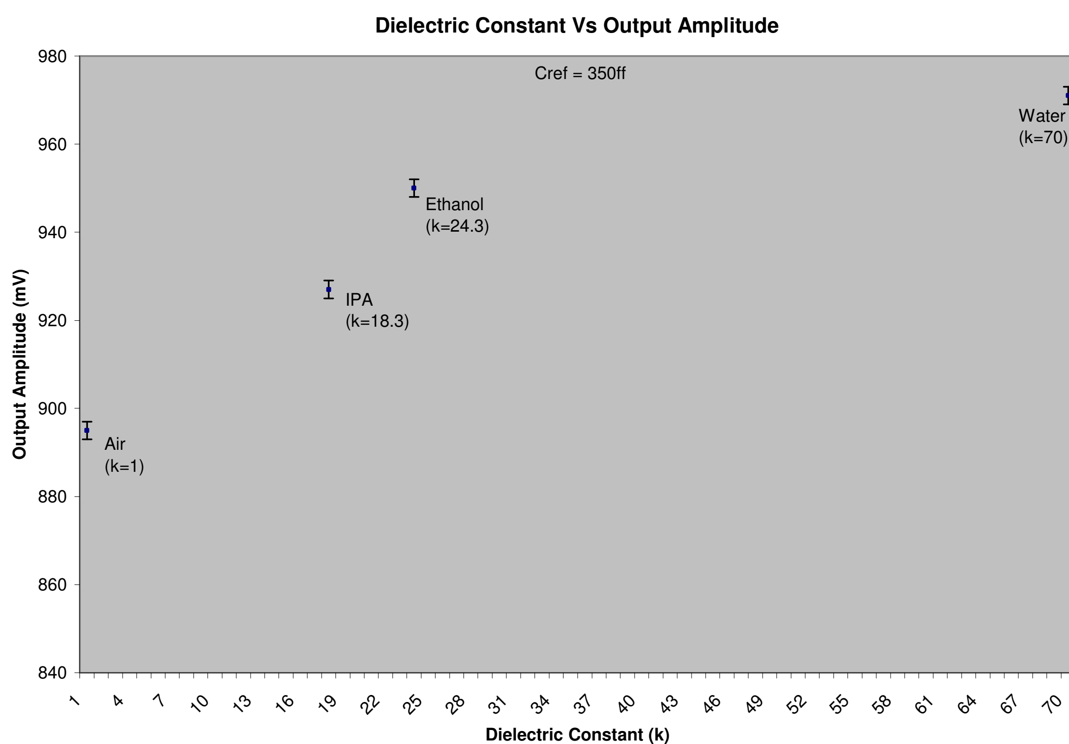


Figure 5.21: Output response of a detection circuit with glass reservoir for varying dielectric constants.

The chips with the glass tubes were also tested for varying concentrations of easily available proteins, bovine serum albumin (BSA) and gamma globulin. The test solutions were weight-volume percentage of these proteins in de-ionized water. The test solutions were delivered using a micro pipette to fill the glass tube reservoir. The chip's lid was closed

during measurements to prevent any errors due to evaporation of the test solutions. The output responses of multiple detection circuits with 350ff reference capacitance are shown in Figures 5.22 and 5.23. The difference in output amplitude from air baseline is plotted instead of absolute values for clarity.

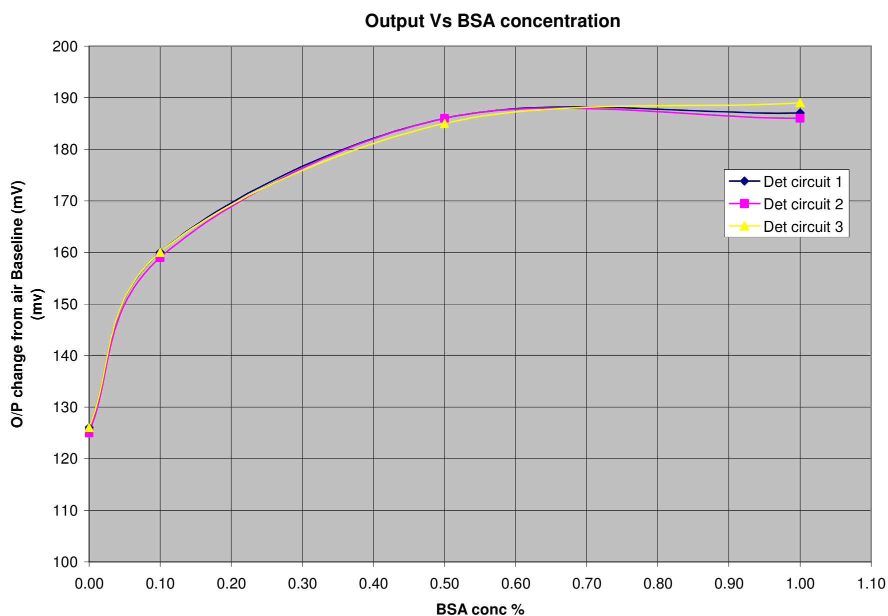


Figure 5.22: Output response Vs bovine serum albumin (BSA) concentrations.

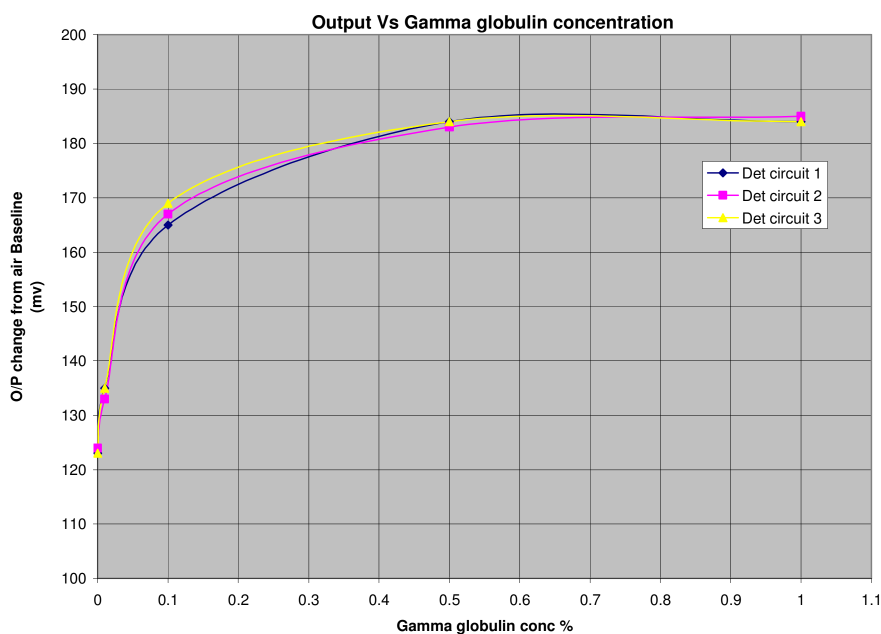


Figure 5.23: Output response Vs gamma globulin concentrations.

From the response plots for BSA and gamma globulin, the minimum detectable level for these proteins were deduced to be 0.1%. The supply clock was left external because of the fact that different materials polarize differently at different frequencies and it may be necessary to vary the frequency to optimize for a particular detection scheme. The protein concentrations were also tested at multiple clock frequencies of 250 KHz to 1.5 MHz in steps of 250 KHz. The response plots were similar in nature with no significant increase in sensitivity.

This generation of chips with the modification made by adding the glass tube shows good response to dielectric changes in liquid medium. The complete surface of chip can be treated with a target specific activation layer and the glass tube reservoir can be added as a secondary step. This would make all the detection circuits in the chip sensitive to a single target. Having this setup with all the detection circuits sensitive to one target would improve sensitivity because the chance of the intended target molecule interacting with at least one of the sensor sites (in this case, sensor interconnect) is higher than having only one sensor site treated.

Since the output information for this generation of detection circuits is in the form of amplitude swings, it would be easy to use an external op-amp in differential mode to measure the difference signal between a detection circuit pair to minimize noise as explained in chapter 4.

5.4. Fourth Generation Design

An optical micrograph of a fabricated fourth generation chip is shown in Figure 5.24. Unlike previous generations of chips, the fourth generation detection circuits were designed to be in close proximity to the sensor sites. The four quadrants with the detection circuit pairs are shown in Figures 5.25 and 5.26. Having the sensors close to the detection circuit minimizes the effect of the sensor interconnects acting like sensors as seen in previous designs. The circuit design of the detection circuits is the same as previous generation and would also require an external bias supply and a clock input.

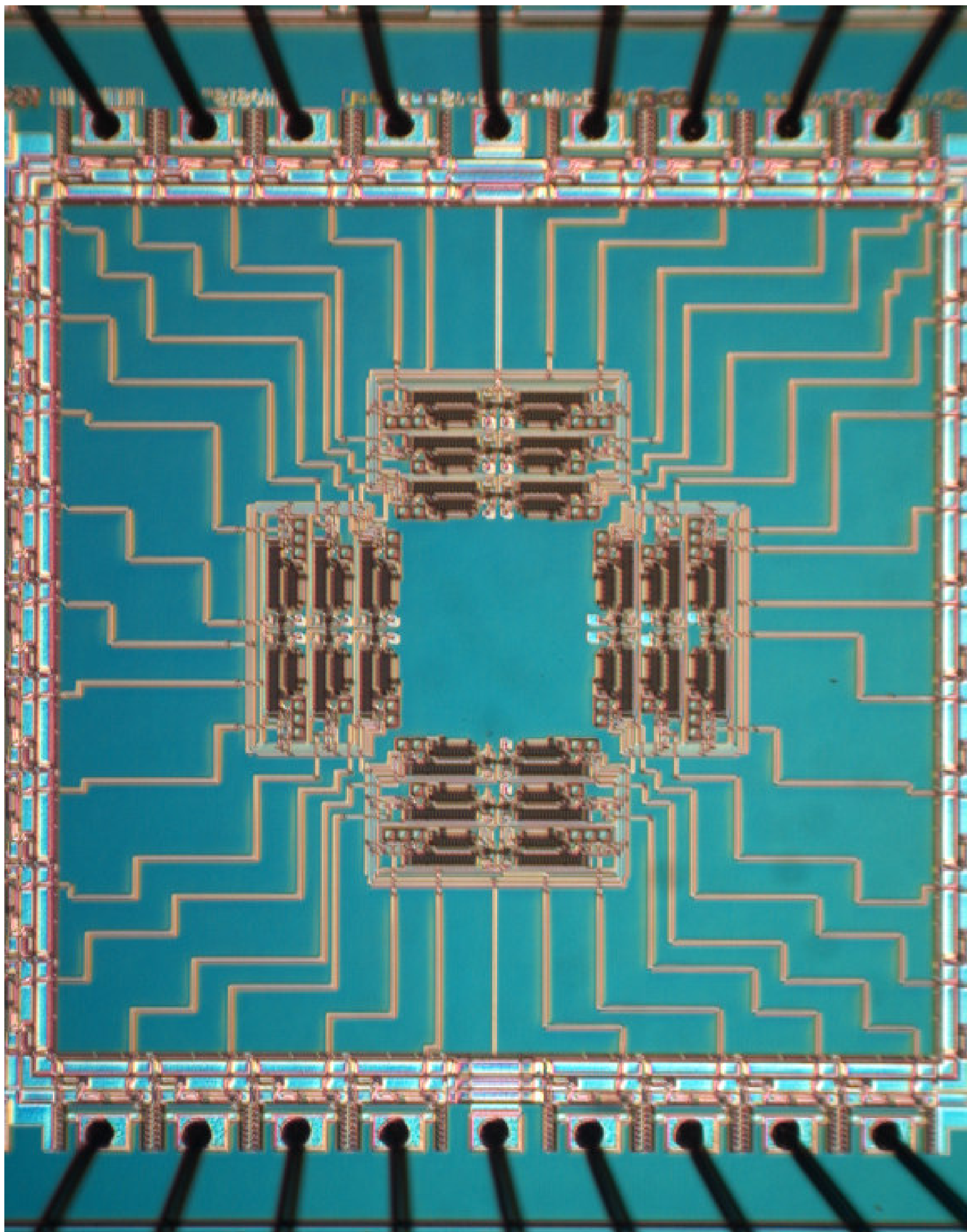


Figure 5.24: Optical micrograph of 4th generation chip.

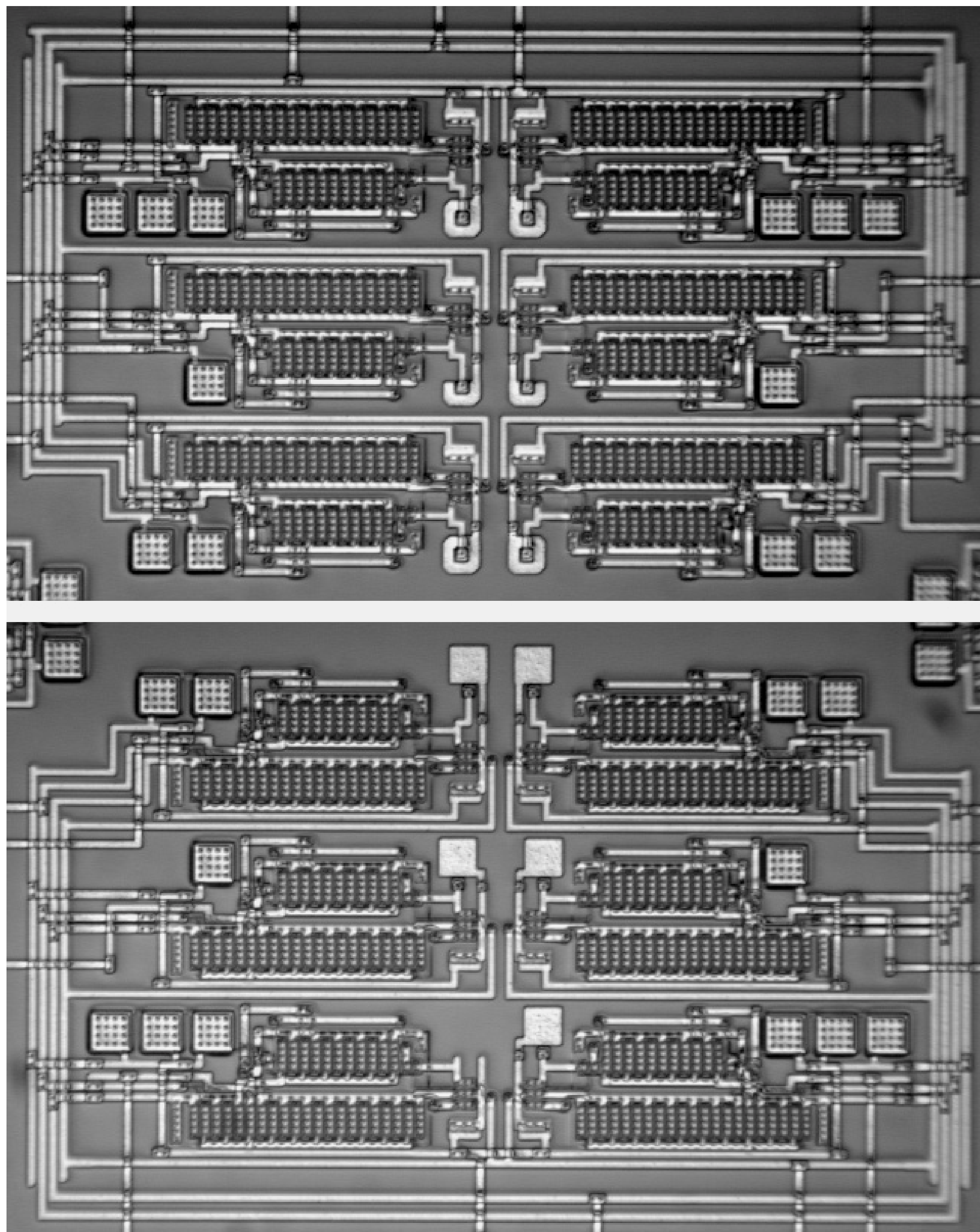


Figure 5.25: Optical micrograph of quadrant 1 and 3 with three detection circuit pairs with sensor sites.

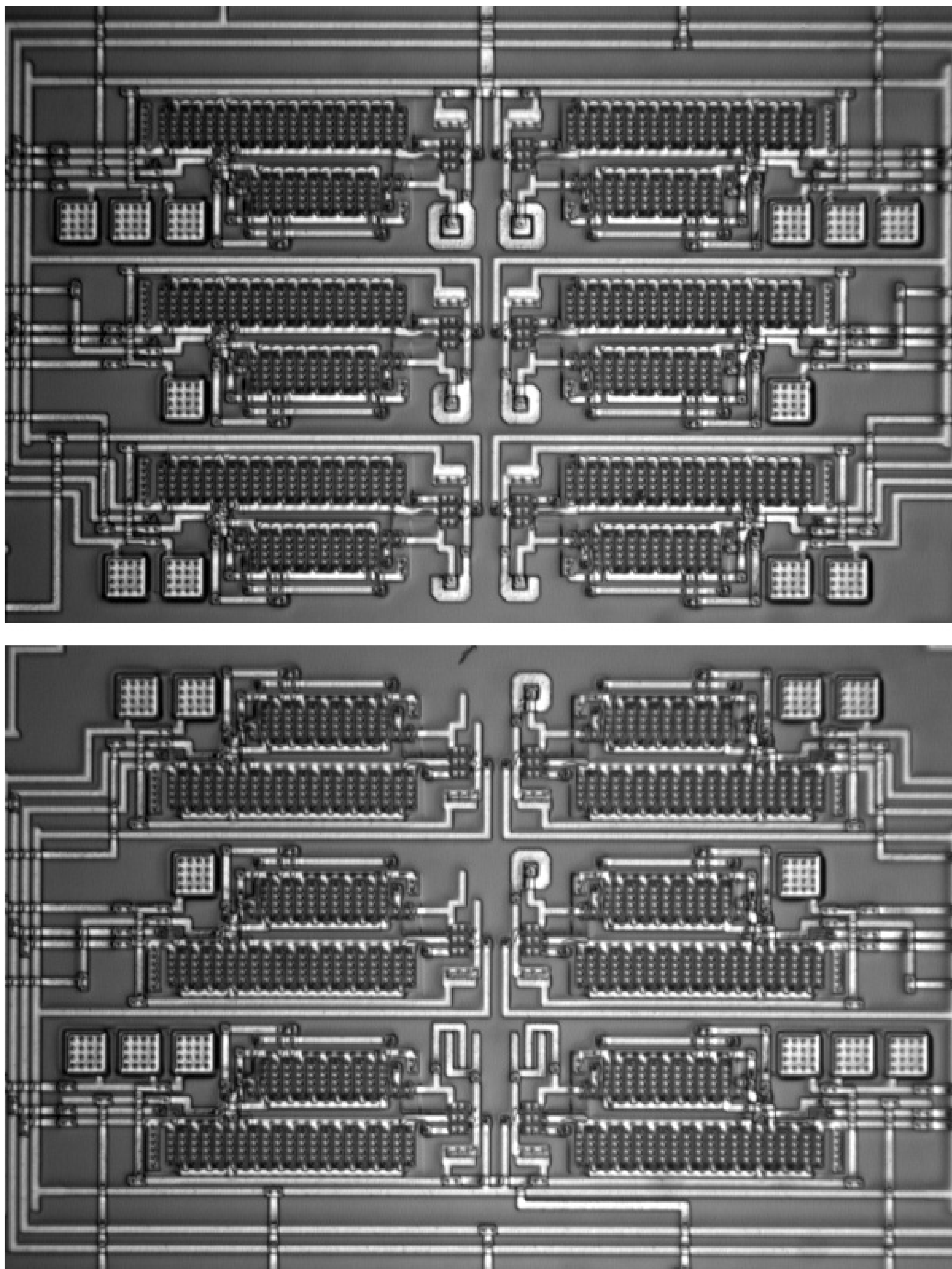


Figure 5.26: Optical micrograph of quadrant 2 and 4 with three detection circuit pairs with sensor sites.

Rather than using the same breadboard and DC power supply used in previous tests, a test circuit board was made with a prototyping board. The test circuit board had a 40 pin dip socket adapter for the test IC's, along with pin adapter socket strips on either side of the IC socket to enable easy selection of any particular output pin. In order to keep the supply voltage to the test chips constant, a commercial 5V power regulator μA78M05 was used with input as 9V from a DC power supply. A DPST switch with 4 positions was used to switch 5V V_{DD} and Gnd to the four detection circuit quadrants in the test chips. A resistor set precision oscillator LTC1799 (1 KHz to 3 MHz) was used to provide the clock inputs to the 4 quadrants. The oscillator's frequency can be set by a single external resistance and calculated from the IC specification sheet to be 39KΩ for an oscillation frequency of 250 KHz. The clock signal was also controlled using a SPST switch to supply input clock to the four quadrants. The oscillator was powered by the 5V power regulator.

Since the outputs of the detection circuits are measured using a multi-meter and also monitored on an oscilloscope concurrently, the loads on the output drivers of the detection circuits are high. A low power, high performance, Rail-to-Rail op-amp LM6152 was configured as a non-inverting amplifier with a gain of 2 which was used as a buffer between the detection circuits and the measuring instruments. This op-amp can be reconfigured to operate in differential mode to measure the difference signal between detection circuit pairs. The bias voltage for the test chip was generated by a simple resistive voltage divider network. It was found that 3.8V as bias voltage to the output buffers gave the least DC shift in the signal output (more headroom for output swing) and was still able to drive the output load. The circuit schematic of the test board is shown in Figure 5.27 and image of the completed test board is shown in Figure 5.28.

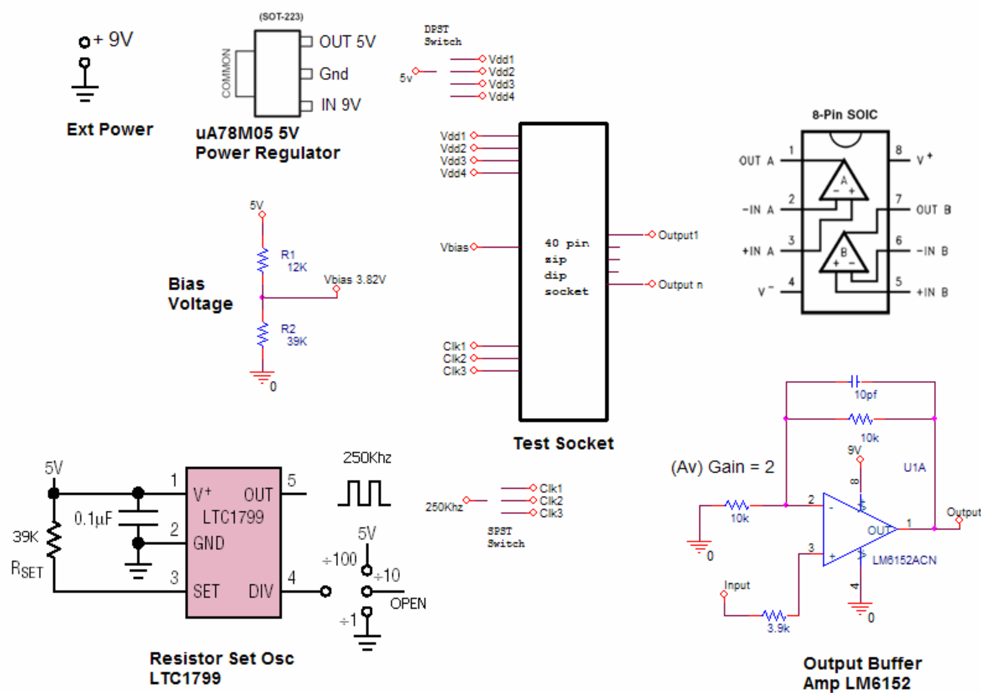


Figure 5.27: Circuit schematic of the test board.

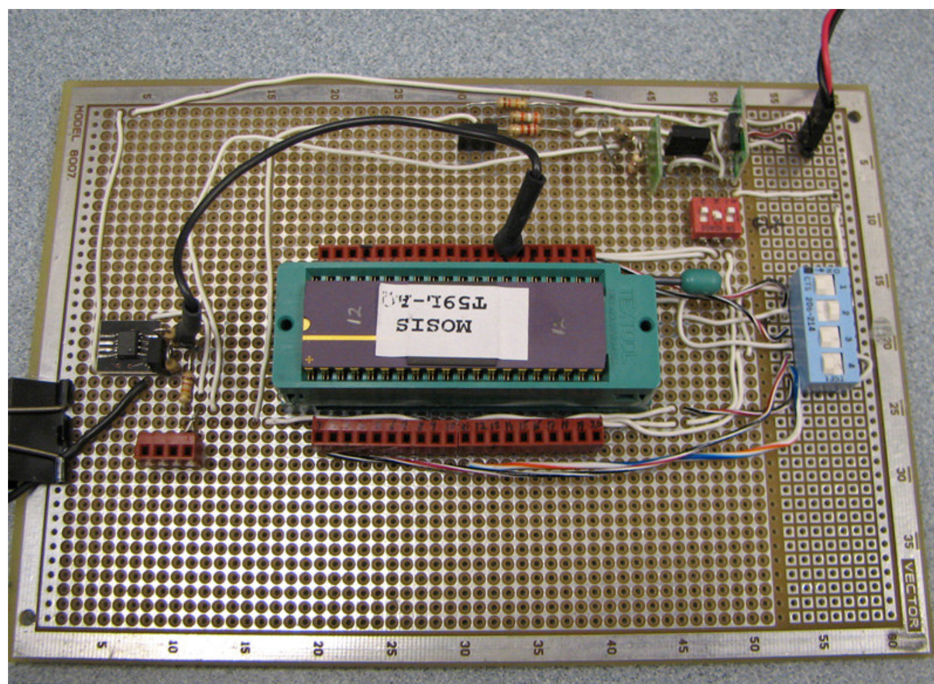


Figure 5.28: Image of completed test circuit board with test IC.

The sensor-chip hybrid was tested using the test circuit board described above without the addition of any test medium. The output AC amplitudes of each detection circuit on chip were plotted on the layout to better relate between the output values and the actual circuit topographies. This is shown in Figure 5.28. The three values of the reference capacitors, which define the gain of the detection circuits used in this generation, were 250ff, 500ff and 750ff. In the layout shown in Figure 5.29, the reference capacitor can be identified as red square structures on the outer edge of each detection circuit. Each square corresponds to 250ff of poly capacitance. The detection circuits shown in the layout can be identified to have 250ff or 500ff or 750ff reference capacitance based on the number of red squares (1 square = 250ff, 2 = 500ff, 3 = 750ff). This identification is necessary to understand the relation between the reference capacitor value and the output amplitudes plotted.

It can be noted that none of the detection circuit pairs that were designed with identical sensor sites and gains are well matched. This is due to fabrication process variations. Since the gain of the detection circuit is directly related to the reference capacitance, any small physical variation in this structure would play a major role in output mismatch.

In Figure 5.28, detection circuit pair 1 has C_{ref}=250ff, 2 has C_{ref}=500ff and 3 has C_{ref}=750ff. All three pairs have similar sensor site metal structures and we can approximate that the input capacitance seen by all the detection circuits in 1, 2 and 3 are identical by ignoring process variations. From the output values shown in the layout, it can be observed that the circuit pairs with 250ff as C_{ref} has the highest output of the three, suggesting a higher gain than the other two detection circuit pairs for the same input capacitance. 250ff-gain>500ff-gain> 750ff-gain. This is in agreement with design and simulation results.

Similar to previous designs, this chip was also tested with water to verify the circuit response to liquid test mediums. 0.5μl of water was delivered to the center of the chip and the droplet was found to be large enough to cover all four detection circuit quadrants. As expected the detection circuits with 250ff reference caps had the highest output response (average of 75mV amplitude change from air baseline). One of the detection units in circuit pair 4 does not have metal 2 sensor connect site. It has only a short length of metal 1 which is deeper than metal 2 and its response to dielectric changes above it will be less than that of

the sensor connect site made with metal 2. This result is confirmed with the water test. The detector with M2 sensor site shows a response of 74mV and the detector with only M1 shows a reduced output of 54mV (amplitude change from air baseline).

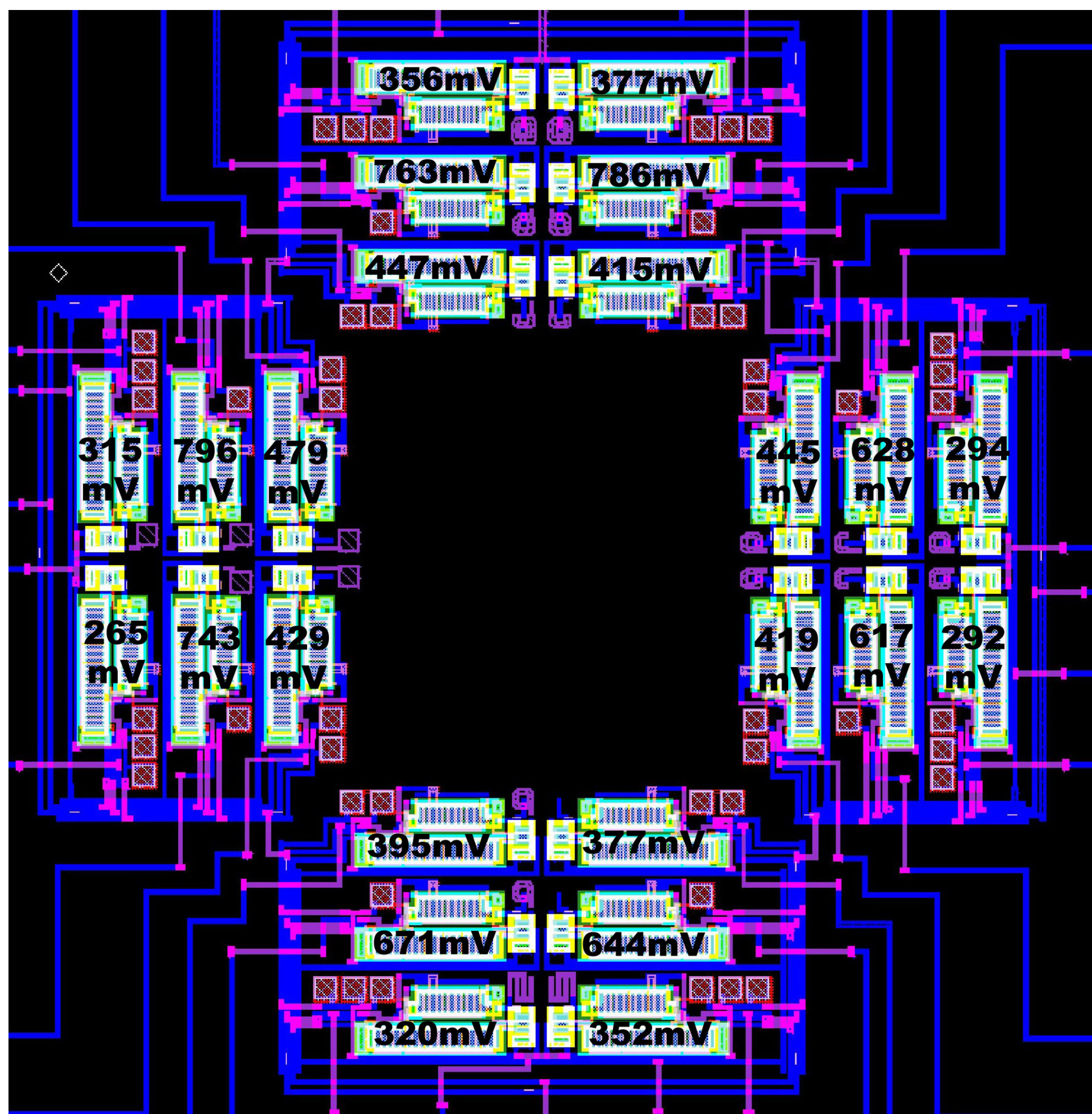


Figure 5.29: Mask layout showing output AC amplitude of multiple detection circuits without any FIB deposited sensors.

In this design there are no long sensor interconnects that may behave like sensors. The detection circuits respond only to the changes caused by the M2 structures at the sensor sites along with the response of the short length of M1 interconnect to the detection circuit.

FIB fabricated sensors are necessary to increase the input capacitance swing seen by the detection circuits. FIB sensors are necessary in this generation of chips for good sensitivity.

Platinum sensor structures were fabricated on the chip to study sensitivity improvement. It was observed that none of the detection circuits that had a sensor structure deposited by the FIB were functional. The detection circuits' outputs were saturated with maximum output amplitude, with the tops of the peaks clipped. Similar output behavior was seen in the first generation of chips when there was a leakage path between the two planes of the sensor. But, all the sensors that were fabricated using the FIB in this chip had one of the planes buried below the nitride passivation. There was no obvious direct electrical path between the two planes of the sensors. An example FIB sensor is shown in Figure 5.30. In the figure, the deposited platinum bars are connected to the M2 square in the center with a FIB machined via. This M2 square is connected to the detection circuit by a M1 line that runs below the sensor site. The central M2 square, along with the platinum bars, form one plane of the capacitor as indicated by the shaded (red) regions in the figure. The second plane of the capacitor is the concentric M2 ground plane. There is an insulating passivation layer between the FIB platinum bars and the ground plane.

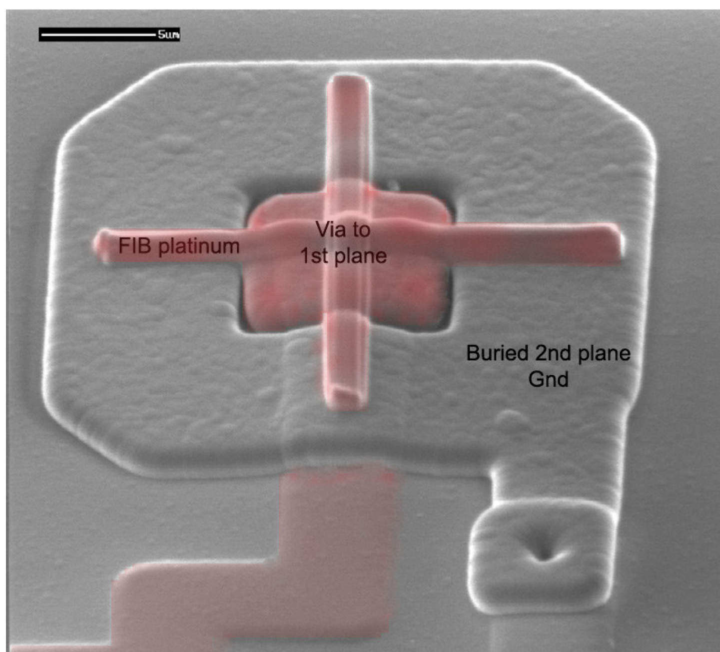


Figure 5.30: Secondary electron micrograph of FIB platinum sensor with buried 2nd plane.

It was also noted that any FIB milling or deposition activity in close proximity to the sensor sites led to the same result of output saturation. Hence, surface contamination with re-deposited platinum can be eliminated as the cause for this problem. The leakage or low resistance path could be created by implanted gallium ions from the FIB. The acceleration voltage used during normal FIB micromachining is 25KV. To determine if decreasing the accelerating voltage would reduce the number of gallium ions implanted, sensors were fabricated using 15KV and 20KV accelerating voltages. This process did not prevent the detection circuit from saturating. Various lower intensities of gallium beam (spot size in FIB) were also tried in order to minimize the implanted gallium ions with no change in circuit behavior. It can be seen from Figure 5.31, that the problem areas are most likely the regions where M2 overlaps M1 at the sensor sites. Gallium ions could get implanted in insulation regions between those two metal layers, causing the low resistance path.

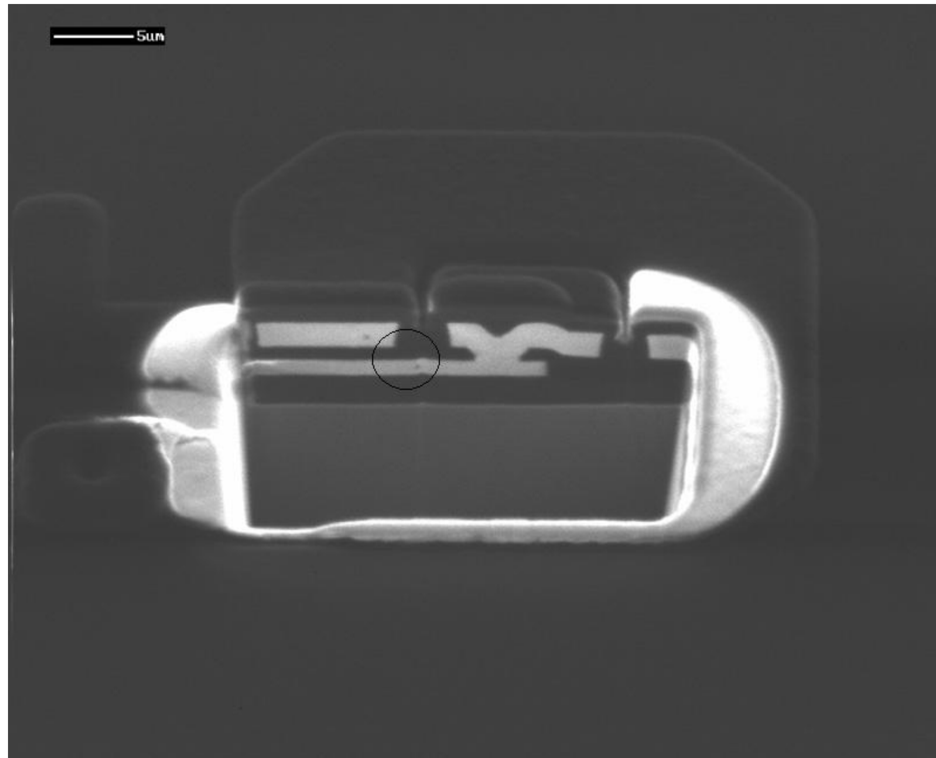


Figure 5.31: Secondary electron micrograph of FIB cross section of sensor site to show problem area.

Some of the detection circuits with the FIB sensors were observed to gradually recover with time (4-8 weeks). This could be because of the implanted gallium metal diffusing or dispersing away from the problem areas between M1 and M2 at the sensor sites. It was found through trial and error that this process of self annealing can be expedited by heat treating the chip at 200 ºC for 3hrs in an oven. The exact process of the chip recovery is unknown but the likely cause is either because of the gallium metal diffusing away from the problem regions or being oxidized in place.

The output response of one of the heat treated chips with FIB fabricated sensor similar to the one shown in Figure 5.30 to different test solutions of known dielectric constants is shown in Figure 5.32.

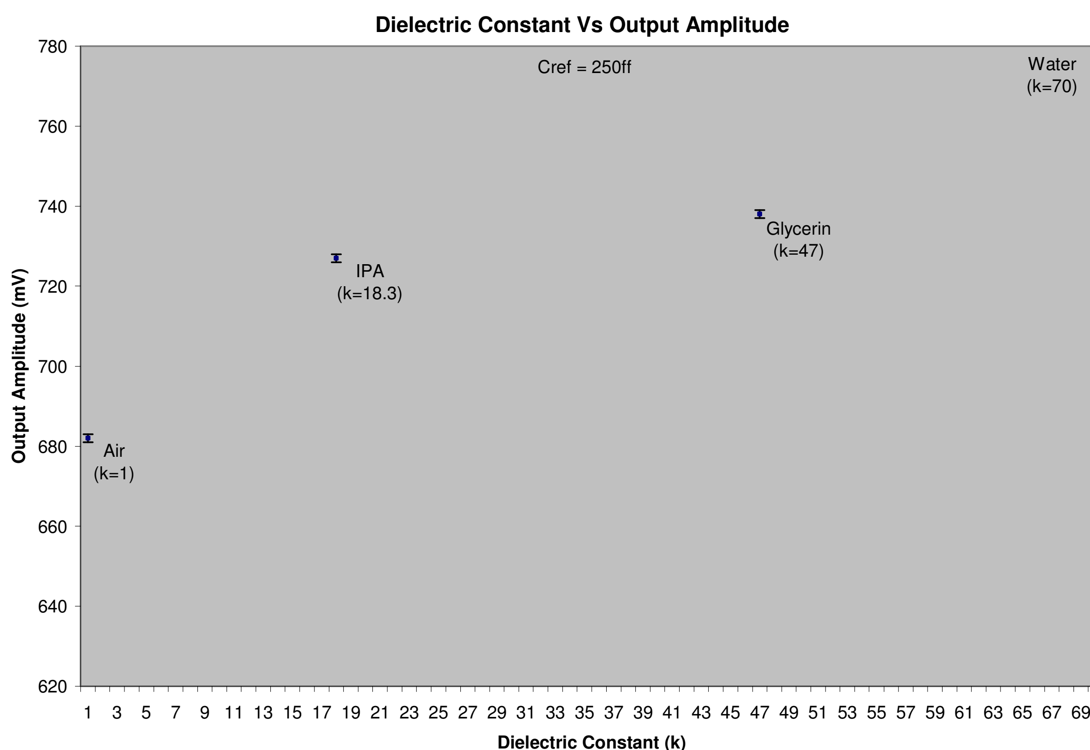


Figure 5.32: Output response of a detection circuit with Cref = 250ff for varying dielectric constants, after heat treatment.

This generation of chips does not suffer from the long sensor interconnects. Based on the response chart in the liquid tests, the detection circuit with a reference capacitor of 250ff causes an output change of 45mV for 18.3 change in dielectric constant. With the existing test setup which includes the buffer op-amp, the output signal is stable $\pm$1mV, implying this generation of design should be able to detect $\pm$0.4 changes in dielectric constant.

The IC's must be heat treated after the FIB sensor fabrication process. This step could be avoided in future designs by altering the layout of the sensor sites. The layout of the sensor sites should not use overlapping metal layers that make connections to the two planes of the sensor. Also, better matching between detection circuit pairs can be achieved by designing the layouts of the reference capacitors to not include sharp corners. Dummy capacitive structures could be used to surround the actual reference capacitance, which would help maintain the geometry of the poly capacitor during chemical mechanical planarization (CMP) fabrication step.

It was found that the supply voltage had to be reduced to 1.15 V for the first generation chips to function as designed. This was due to improperly designed output buffer stages. It was also demonstrated that the output response and hence the sensitivity of the system after the fabrication of FIB sensor was higher than just the fringing capacitance of top metal interconnects. The second generation chips were non functional due to improper sizing of the output buffer stage. It was found that the third generation of chips which had long interconnects to the sensor sites were saturated when exposed to high dielectric constant liquids. This problem was overcome by limiting the exposure area by constructing a glass tube reservoir on the chip surface. The fourth generation chips had the detection circuits in pairs and exhibited mismatch between identical circuits because of process variations. Implanted gallium ions during FIB sensor fabrication also posed a problem by creating a low resistance path between metal 2 and metal 1. This problem was overcome by heat treating the chips at 200ºC. Both the third and the fourth generation chips are sensitive to small changes in dielectric constant and can be used as a test platform for developing detection techniques to identify target molecules after the chip surface or the sensor sites are treated with the target selective materials.

6. Application Specific Research

The sensor-array chip hybrid was evaluated for its versatility in applications that dealt with liquid test mediums and also gaseous mediums. The multidisciplinary research applications that were tested using this system include: 1) detection and measurement of organophosphate neurotoxins; 2) air quality monitoring - detection of low concentrations of carbon monoxide gas; 3) aid in the study of early detection of stroke by up-regulated CART expression.

6.1. Detection and measurement of organophosphate neurotoxins

The detection principle for the measurement of organophosphate neurotoxins depends on the phosphorylation of CREB in the presence of low concentrations of OPs as explained in chapter two. CREBtide is a synthetic peptide that contains the consensus sequence for the Ser-133 phosphorylation site of CREB. It is widely used in biochemical studies of enzymatic pathways that phosphorylate CREB. Preliminary data from studies conducted at CROET-OHSU indicates that CREBtide is robustly phosphorylated in the presence of the enzyme PKA and the phos-phate donor ATP.

ATP was used in place of OPs as the phosphate donor for initial experiments. Phosphorylation of CREBtide by the phosphate group donated by ATP is driven by enzymatic catalysis (PKA). A reaction without the inclusion of enzymes is preferred for the detection of OPs, because the enzyme activity tends to get modulated by the addition of reagents and other factors that may be present in the reaction mix in a real test environment. The primary goal for this research was to determine if the CREBtide can be directly phosphorylated by OP's without enzymatic catalysis. The first step would be to check if the sensor-array chip can detect the phosphorylation of CREBtide by ATP in the presence of

enzyme PKA, and if the sensor can detect varying levels of phosphorylation, which would be evaluated by varying the concentration of ATP.

The concentration of the test solutions and reaction mixtures that were used during this test and all subsequent tests are as follows:

Reaction buffer = 10 mM $MgCl_2$, 50 mM PIPES, 1 μM DTT, ^{32}P-γ-ATP (0.03 μCi/μl).

1X ATP = 50 μM ATP.

1X PKA = 1 unit/μl PKA.

1X CREBtide = 27.5 μM CREBtide (Calbiochem, San Diego, CA).

Preliminary results from experiments performed at CROET-OHSU indicate that the reaction mixture comprising of all of the above concentrations of solutions incubated for 20mins at 30ºC, show phosphorylation of CREBtide as analyzed by Western blotting using antibodies specific for pCREB. These concentrations were kept as standards for the tests on the chips. Initially, the buffer solution with no ATP or PKA was tested. Then the buffer solution with ATP and/or PKA was tested, and the comparison of the tests was used to establish a baseline behavior. CREBtide was then added to the reaction mixture with ATP and PKA and incubated at 30ºC for 20mins for phosphorylation to progress. Then, the response of the chips using the incubated mixture was noted. If this response of the phosphorylated CREBtide mixture is different than that of the individual reacting components, the resulting difference in signal could be an indicator of the phosphorylation reaction. The same procedure can be repeated for multiple concentration of ATP to determine the chips response to varying degrees of phosphorylation.

A chip from the third generation design, with a central glass reservoir made with a section of glass capillary tube (as explained in chapter 5) with internal diameter 650μm and 1.1mm tall, was tested for the detection of phosphorylation of CREBtide. Delivering the test solutions into the glass reservoir using conventional micro pipette tips was not possible. The tips of the micro pipettes were larger than the internal diameter of the glass reservoir. Glass capillary tubes with 3 mm internal diameter were extruded into finer capillary tubes using a Bunsen burner and were used for dispensing the test solutions. A second chip with only the center of the die exposed and the rest covered with G1 epoxy was also tested. The chips were tested on a breadboard with a 500 KHz clock from a signal generator and 5V power

supply. Since the third generation chips had long interconnects between the sensor sites and the detection circuits which were acting like sensors, no FIB platinum sensor structures were fabricated on these chips. The test solutions were delivered into the glass reservoir and the output responses from the detection circuits were noted on a digital multi-meter. The chip with the central glass reservoir did not show significant difference in output signal between the individual components and the phosphorylated mixture. The output amplitude response of one of the detection circuits of the chip with G1 epoxy reservoir (which was determined to have a good output response to liquid mediums from pervious tests) is shown in Table 6.1. The values shown in the table are difference in output signal amplitude from air baseline.

Table 6.1: Output response of 3rd gen chip with G1 epoxy reservoir.

Sample	ATP	PKA	CREBtide	Output-V_{ac} (mV)	Change from Baseline-V_{ac} (mV)
Reaction buffer (Baseline)	+ (50 μM)	+	-	337	-
CREBtide 20 minute incubation	+ (50 μM)	+	+	348	11
CREBtide Non incubated	+ (50 μM)	+	+	345	8
CREBtide with 4X ATP, non-incubated	+ (200 μM)	+	+	350	13

This chip showed an increased output for phosphorylated CREBtide than the initial reaction buffer. It shows 11 mV increase for incubated phosphorylated CREBtide, and an 8 mV increase for non incubated phosphorylated CREBtide. The ATP in the reaction mixture was increased to 4 times the initial value and the resultant mixture showed an increase of 13 mV from the baseline value. This increase could be a direct result of increasing the

concentration of ATP and not because of the increased phosphorylation. The baseline reading for the reaction buffer was not noted after increasing the concentration of ATP. Later analysis of the surface of the tested chips under an optical microscope indicated protein residue build up as shown in Figure 6.1. De-ionized water was used to clean the surface of the chips after every test. The results for the chip with the G1 epoxy reservoir show a definite measurable difference between the baseline and phosphorylated CREBtide. Even though the G1 epoxy only acts like a thick insulation layer exposing only a portion of the sensor interconnects to the test solutions, the areas covered by the epoxy still have residual fringing capacitance that are sensitive to changes above them. The phosphorylated CREBtide solution may have a different surface tension property which wets the epoxy surface more than the reaction buffer causing increased output amplitude as shown in table 6.1. Also, protein residue build up could have influenced the chip response.

Figure 6.1: Optical image of protein residue build-up on die surface.

Multiple tests were conducted with more effective cleaning of the die surface after each test using 10% sodium dodecyl sulfate (SDS) solution, followed by de-ionized water cleansing. Optical observation after the tests confirmed that the SDS solution was effective in removing any residual protein from accumulating on the surface of the chip. All of the observations and tests done after employing SDS for cleansing showed no significant increase or difference in output amplitudes between phosphorylated and non phosphorrylated CREBtide. The tests were conducted using the third generation design with central glass reservoir.

The fourth generation design does not have long interconnects acting like sensors. No glass tube reservoir is necessary for this generation of design in order to limit the surface that is being exposed to the test solutions. However, the FIB had to be used to micro machine and connect platinum sensors at the sensor connect sites to enhance sensitivity. Example sensor structures are shown in Figure 6.2. The FIB was used to fabricate multiple sensor structures and the chip was heat treated in an oven at 200 ºC for 3hrs. Heat treatment was performed in order to eliminate the adverse effect of implanted gallium ions during FIB micromachining as explained in chapter five. When the chips containing FIB sensors were tested, the output responses seemed to be clamped or saturated when exposed to the reaction mixture. This behavior was not observed for all test solutions but only for those containing salts or electrolytes. It was noted that the output response was not saturated for tests with de-ionized water. Common salt (NaCl) was added to de-ionized water to make a 3% salt solution and the output response of the chip was saturated or clipped for this test solution. All of the sensors that were fabricated on this chip had only one sensor plate exposed to the test solution and the second plate was insulated by passivation, as shown in Figure 5.29. Saturated output responses observed in earlier experiments generally implied the existence of a resistive path between the exposed sensor plate and the second plate (ground).

Careful inspection of the die's surface in a scanning electron microscope showed that the die's silicon nitride (and oxide) surface insulation layer had voids or pits exposing the underlying metal layers in some areas. This was typically seen in areas where there were sharp corners in the top metal (M2). There was no clear pattern in the distribution of these faults and they seemed to occur more often at the outer edges of the detection circuits. This

is a fabrication artifact and is most likely the cause for the leakage paths. When the chip is subjected to a conductive test solution, there may be a weak current flowing between the exposed sensor plate and the metal surfaces exposed at these voids, causing the detection circuit to saturate. Figure 6.3 shows some of these flaws/pits in the nitride passivation surface.

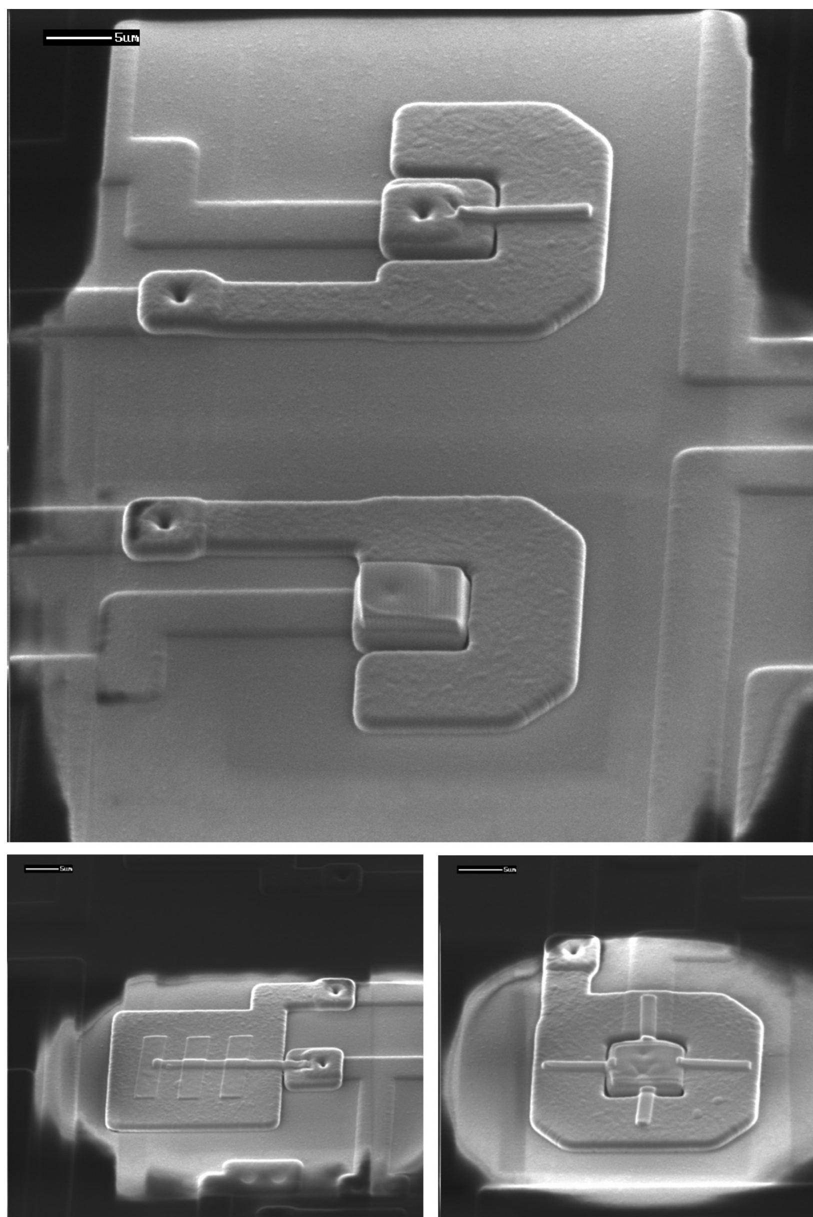


Figure 6.2: Secondary electron images of typical FIB platinum sensor structures used in test.

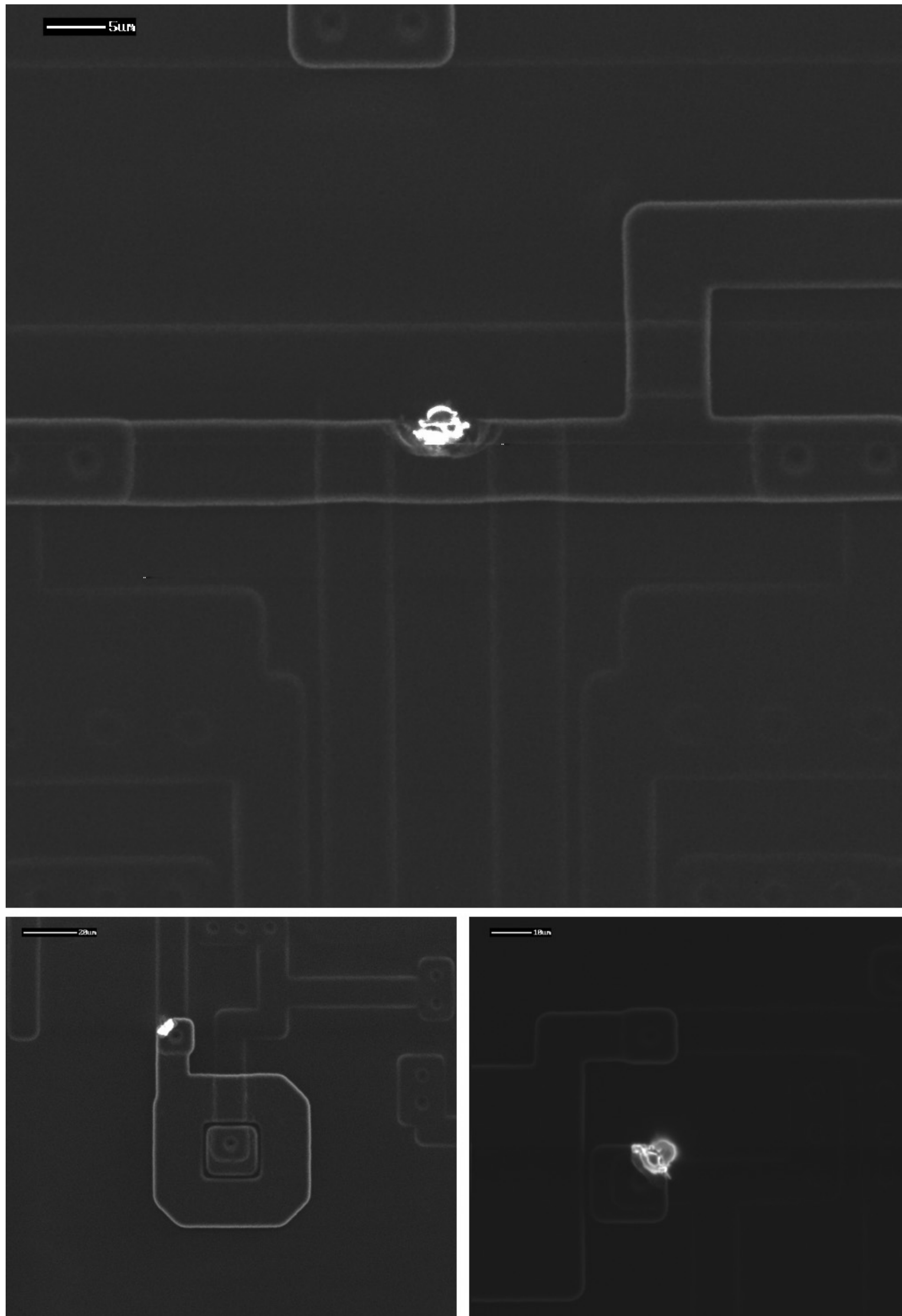


Figure 6.3: Secondary electron images of faults in silicon nitride passivation layer.

In order to mask the problem caused by the nitride pin holes that expose the top metal, it is necessary to cover these areas with a thin layer of insulating material. High current thermal evaporation was used to deposit a thin layer of Silicon oxide (SiO) as an insulating blanket layer over the whole die surface. The melting point for SiO is greater than 1775 ºC and the boiling point is 1880 ºC. A pre-measured quantity of SiO powder was heated in a boron nitride crucible in a thermal evaporator at a pressure of 6 x 10^{-6} Torr. The chip was placed about 7 cm from the crucible and the measured quantity of SiO powder required to deposit a 0.5µm thick layer was calculated to be 66.35mg. The heating current was ramped to 7 ~ 8A and the supply voltage set at 60 ~ 70V until all source material was evaporated. Some residue material, grey in color, remained in the crucible after processing. The chips were then subjected to 0.5µl of 3% salt solution delivered to the center of the die using a micro pipette. It was observed that the deposited SiO was insulating and prevented the detection circuits from saturating. But, after three or four trials with the salt solution, it was noted that the detection circuits began to saturate again. Upon inspection under an optical microscope, it was detected that the thermally deposited oxide layer was delaminating and failing. This was mostly due to the mismatch of coefficients of thermal expansion between the SiO layer and the silicon nitride passivation. The delaminated SiO layer is shown in Figure 6.4.

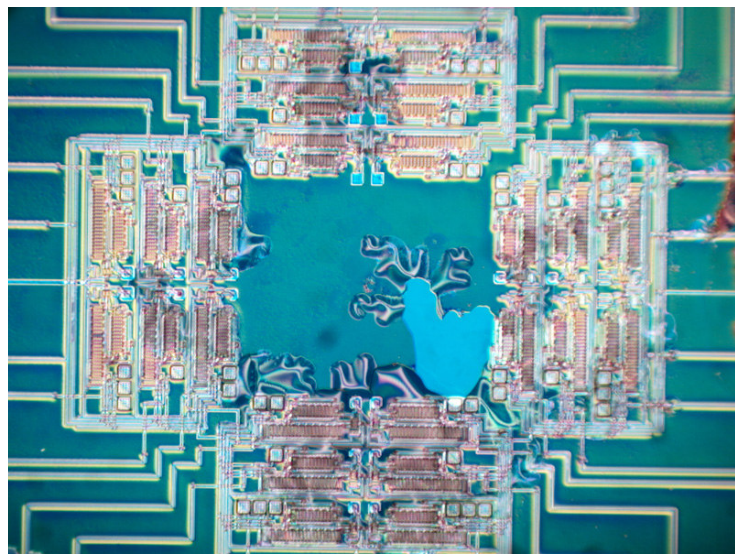


Figure 6.4: Optical image of die surface showing de-lamination of thermally deposited SiO layer.

In order to improve the adhesion of the SiO to the silicon nitride surface, a thin layer of titanium sticking layer was deposited on the chip surface before evaporating the SiO. Care was taken not to make the titanium layer thick and continuous to prevent adding to the leakage path. Metal thicknesses less than 40Å are generally discontinuous and have high electrical resistance. Titanium wire (99.9% pure) was weighed for a deposition thickness of 30Å and was evaporated using a tungsten wire crucible in the high current thermal evaporator at 6 x 10^{-6} Torr belljar pressure. The SiO evaporation process was performed immediately after the evaporation of the titanium sticking layer. This SiO layer with titanium sticking layer, however, also delaminated after a few trials with salt solution. A better sticking layer or an alternative insulation material with a coefficient of thermal expansion close to that of silicon nitride needs to be deposited to yield a stable insulation layer.

A simpler method was experimented to deposit an insulating blanket layer over the entire die. A thin layer of insulating material was deposited on the chip by evaporating cyanoacrylate tissue adhesive in a fume hood. It was determined from trial and error that evaporating the tissue adhesive in two steps, each step evaporating 80mg of adhesive, produced a continuous water resistant layer on top of the die. The evaporation of the tissue adhesive was performed by heating a pre-measured quantity of adhesive on a flat piece of aluminum foil on a hot plate (150F). The open chip was placed 5cms away from the foil containing the adhesive and the whole setup was covered by a glass belljar. The output leads of the chip were masked with foil to prevent the leads from being covered by the deposited non conductive layer. A central glass reservoir was also attached to the chip to minimize the contact of the test solutions to the nitride pin-hole defects, which tend to occur more often at the peripheries of the chip. Figure 6.5 shows the chip with the protective central glass reservoir (top photo) and also the die surface before (bottom left) and after (bottom right) the evaporation of tissue bonding adhesive. The deposited material can be clearly seen as fringes at the edges of the sensor connect structures shown (bottom right) in Figure 6.5.

The chip with the deposited adhesive layer was tested with 3% salt solution and the outputs were noted to be stable and non-saturated. The tests were repeated multiple times and the outputs remained stable with no obvious de-lamination of the insulation layer.

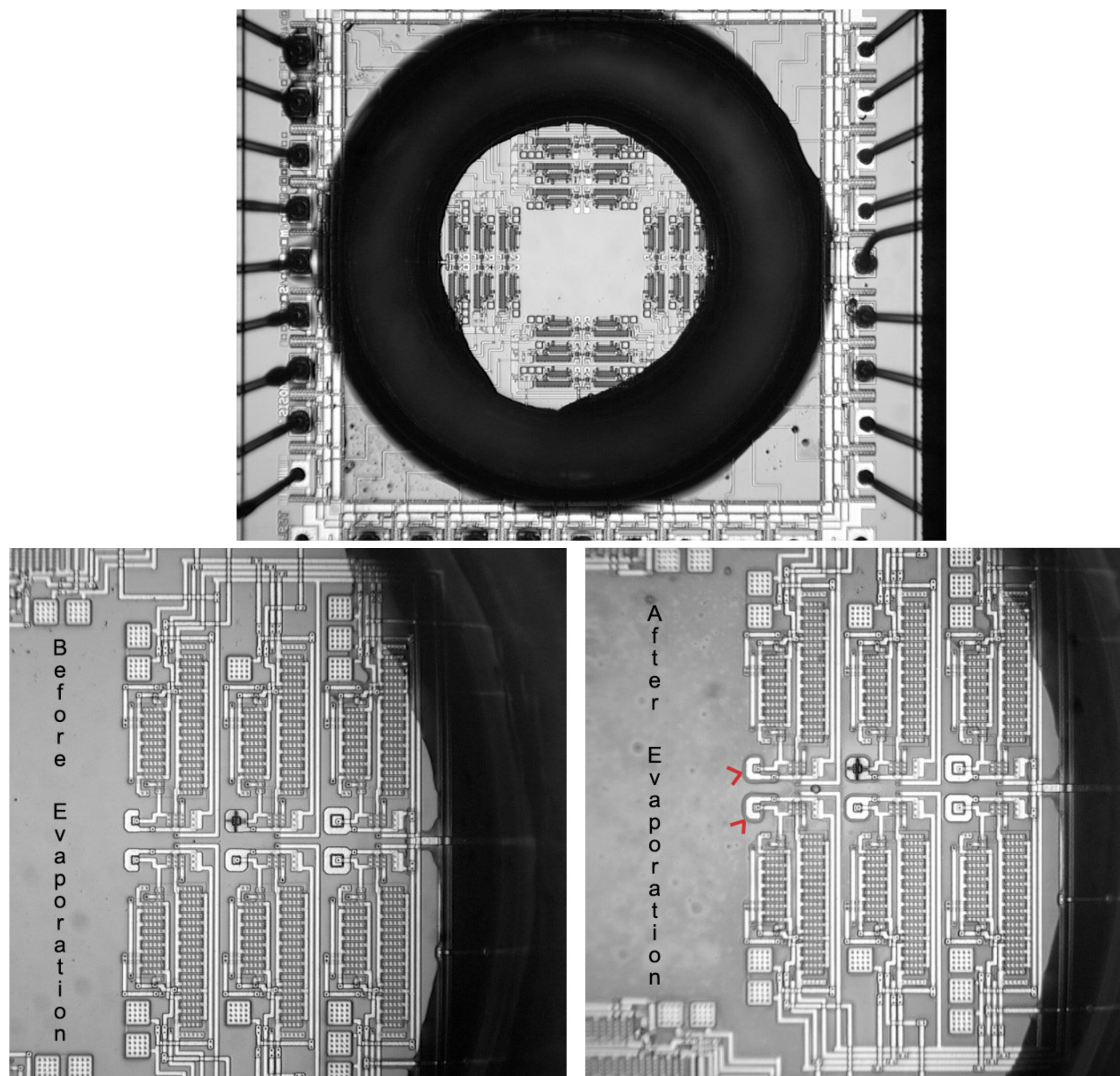


Figure 6.5: Optical image of chip with protective central glass reservoir (top) and the surface of the die before (bottom left) and after the evaporation of insulation layer (bottom right).

The chip with the deposited tissue adhesive insulation layer was tested with the reactant solutions as before and the output responses of four detection circuits with FIB deposited platinum sensors are shown in Figure 6.6. The chips were tested on the test board developed for the fourth generation chips as shown in Figure 5.27.

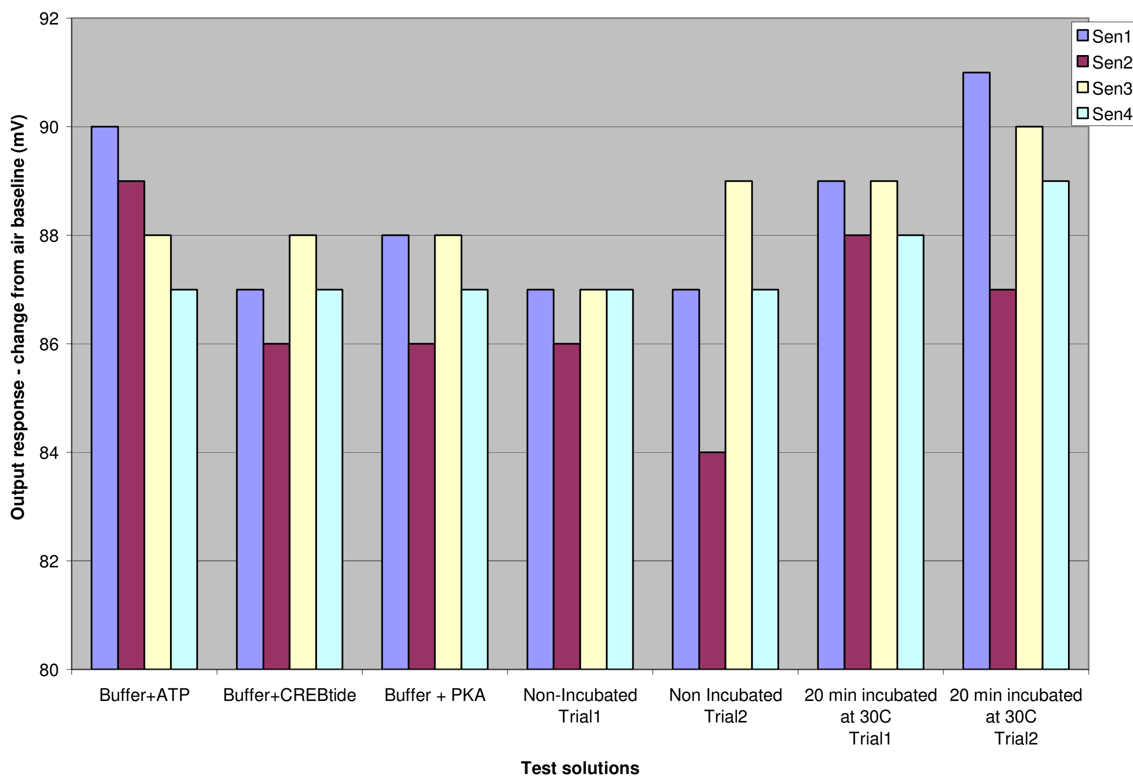


Figure 6.6: Output response of 4th gen chip with glass tube reservoir and adhesive insulation layer.

The output response of the detection circuits, as shown in Figure 6.6, indicates no clear pattern between the individual reactants before phosphorylation and the reaction mixture with the phosphorylated CREBtide. Sensors 3 and 4 show a slight increase (1 to 2 mV) in output amplitude for phosphorylated CREBtide mixture. Further, the output amplitude change from air baseline on average (80-90mV) is less than that of the third generation design with long sensor interconnects shown in Table 6.1.

The third generation design, with long interconnects acting as sensors, seems to have better sensitivity, and is also devoid of the flaws in the silicon nitride passivation. The long insulated interconnects acting as sensors may be better suited for applications that deal with conductive test solutions. A third generation device was fitted with a glass tube reservoir with a larger inner diameter (1mm) to increase the interconnect area that comes in contact with the test solution. This will increase the net capacitance swing of the sensing

interconnects when subjected to test solutions, thereby increasing the sensitivity of the system.

These chips were tested with the same concentrations of test solutions as before. The average amplitude change from the air base line was found to be 252-306mV, which is greater than 80-90mV change exhibited by the fourth generation of chips with short sensor interconnects. However, no clear output amplitude change was noted between phosphorylated and non phosphorylated CREBtide.

The concentrations of the test reactants used (micro moles) seem to be too low for the chip to detect. From previous experiments with BSA and gamma globulin proteins, the minimum detectable levels were found to be 0.01% (Wt/Vol) (Figure 5.21 and 5.22). The same minimum detectable levels cannot be generalized for all proteins as each is characterized by its own electrical behavior (dipole moment) and many other factors. The molecular weight of CREBtide used is 1717. The concentration of CREBtide used in the tests was 27.5μM, which results in Wt/Vol concentration of 0.0047%. The molecular weight of ATP is 573. The concentration of ATP used in the tests was 50μM, which results in Wt/Vol concentrations of 0.0029%. These concentrations are very small in comparison to the minimum detectable levels that were determined for BSA and gamma globulin proteins. Further tests with 2X concentrations of CREBtide shows no significant difference in output between 1X and 2X concentrations of just CREBtide in buffer solution. This means that even at 55μM, the concentration of the CREBtide used is lower than, or just close to, the minimum detectable level of the chip.

Further tests need to be performed with increasing concentrations of CREBtide, doubling the concentration for every consecutive test in order to determine a point at which a significant output difference is observed between two consecutive tests. Then, phosphorylate this higher concentration of CREBtide and determine the minimum detectable level of phosphorylation on chip and the corresponding level of phosphor donor required to phosphorylate the CREB. These experiments with higher concentrations of CREBtide will need to be verified by standard Western blot and electrophoresis based tests to confirm the phosphorylation reaction.

6.2. Detection of low concentrations of carbon monoxide gas

Standalone metal oxide semiconductor (MOS) based sensors [41] have been demonstrated to exhibit good sensitivities to carbon monoxide gas at room temperature. It was shown that a thin film stack consisting of a 25µm square of FIB deposited Pt 30nm thick on 7 nm of thermally grown oxide on a p-doped Si substrate was able to detect CO levels as low as 25ppm. The surface of the sensor-array chip's die has an oxy-nitride passivation layer. One of the buried sensor structures can act like the bottom plate and a thin layer of platinum can be deposited on top of the passivation and then wired to the detection circuit. This would result in a sensor structure with oxy-nitride passivation between the two planes of the sensor capacitor, with one plane of the capacitor thin enough to allow the diffusion of gas. This type of sensor structure is similar to the standalone MOS sensor [41] and could be sensitive to CO gas.

Figure 6.7-A shows a FIB sensor fabricated by depositing 30nm thick, 15µm×5µm rectangular platinum on top of a buried ground metal plate. The deposited thin film platinum was connected to the detection circuit by milling a via on the interconnect leading to the detection circuit and drawing a platinum trace between the via and the thin film. Figure 6.7-B shows a second sensor structure that was made by depositing two rectangular areas of 30nm platinum on either side of a 3µm tall platinum wall deposited on top of a buried ground plane. The total thickness of the passivation layer was found to be approximately 400nm from previous cross sectional analysis. The passivation layer was thinned by 250nm by FIB milling before the thin film platinum layers were deposited. This should increase the capacitance of the sensor because the layer between the two plates of the capacitor has been reduced. The deposited thin film areas and the center platinum wall were connected to the detection circuit by milling a via and running platinum traces as before. The chip with these sensors was exposed to a high concentration of 1000ppm CO gas in a test chamber in a fume hood to determine if these sensor structures were able to detect CO gas. It was found that even with these high concentrations of CO gas, the sensors' response was -1mV, which was not significant. This could be because the oxy-nitride passivation layers'

behavior may not be the same as that of thermally grown oxide used in the standalone MOS sensor [41].

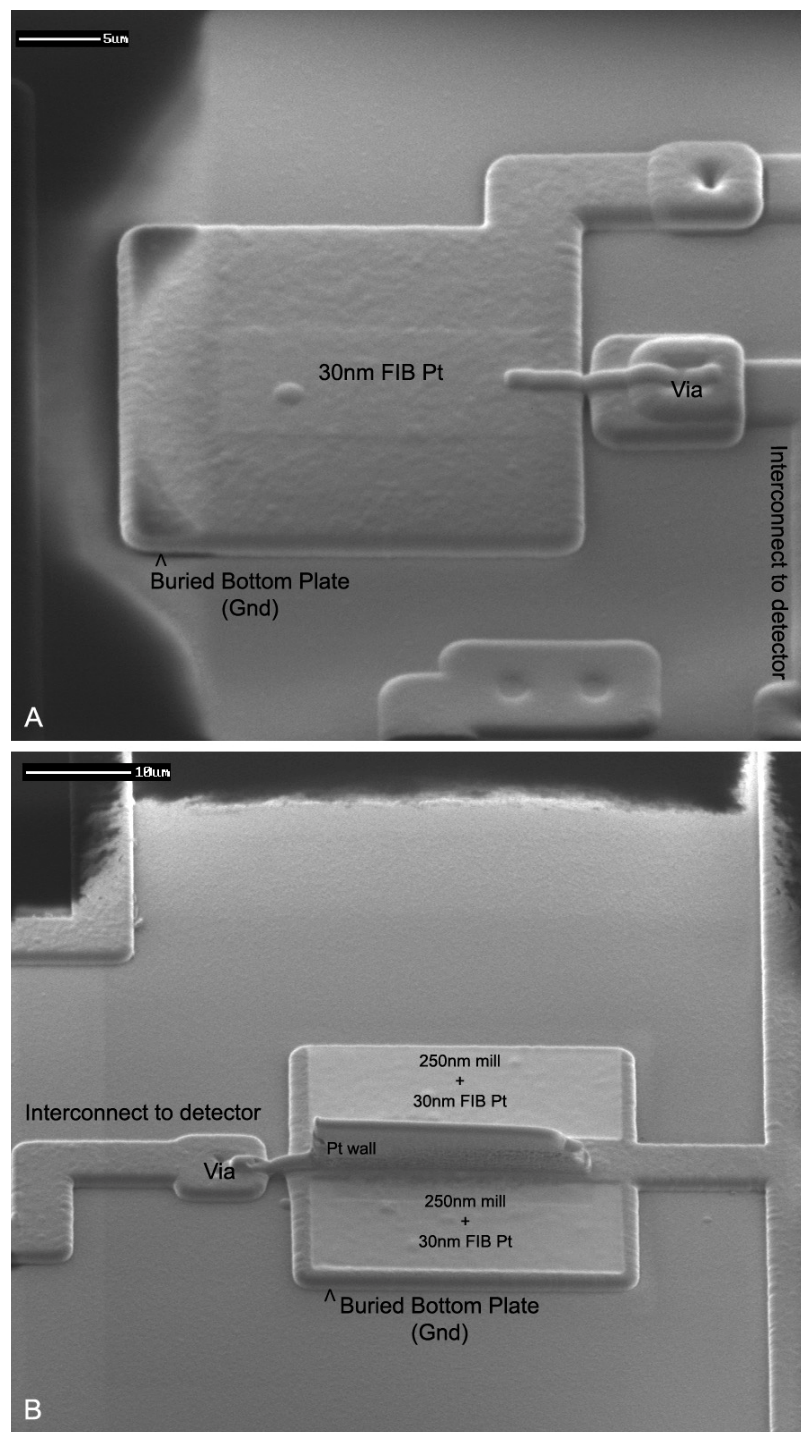


Figure 6.7: Secondary electron images of FIB deposited thin film platinum sensors for CO gas.

Since the sensors with the oxy-nitride sandwich layer were not sensitive to CO gas, a different material that is sensitive to CO gas must be used between the plates of the sensor capacitor. Due to the excellent properties of tin oxide in sensing CO gas as detailed in chapter 2, it could be used between the plates of the sensor capacitor. One method of developing a thin film SnO_2 for standalone sensors is by depositing a thin layer of tin metal and oxidizing it in a furnace at high temperatures. This method of depositing a thin film may not be possible because the chip cannot be safely heated to temperatures greater than 300ºC without causing damage to the embedded layers that constitute the integrated circuits. However, tests were performed to determine if a thin layer of tin metal can be oxidized at lower temperatures by heat treating it for longer periods.

A pre-measured amount of 99.9% pure tin metal was evaporated on a one inch square of silicon substrate with a 1μm silicon nitride layer using high current thermal evaporation to yield a tin metal thickness of 100nm. The substrate with the tin metal was heat treated in an oven at 200ºC and X-ray analysis was performed on the surface using a Scanning Electron Microscope (SEM) with EDS capability. The X-ray analysis results, over varying heat treatment times, are shown in Figure 6.8. It can be seen from Figure 6.8 that the tin metal as evaporated does not have an oxygen peak. After 40 minutes of heat treatment, an oxygen peak can be clearly seen. The peak is even higher after three hours of heat treatment. This shows that the tin metal can be oxidized at lower temperatures. A multi-meter was used to probe the electrical resistance of the deposited and oxidized tin metal. The probes were placed 5mm apart and resulting measurement showed 268Ω resistance, which indicates that the tin metal is not oxidized completely, and if used will result in a low resistance path between the capacitor sensor plates. The results were the same even after eight hours of heat treatment (200ºC), indicating that only the surface of the deposited tin is being oxidized. To facilitate complete oxidation of the tin, the heat treatment must be done at higher temperatures to yield a tin oxide surface with reasonable fabrication time. So, alternate methods of tin oxide deposition have to be employed as the chip cannot be safely heated over 300ºC.

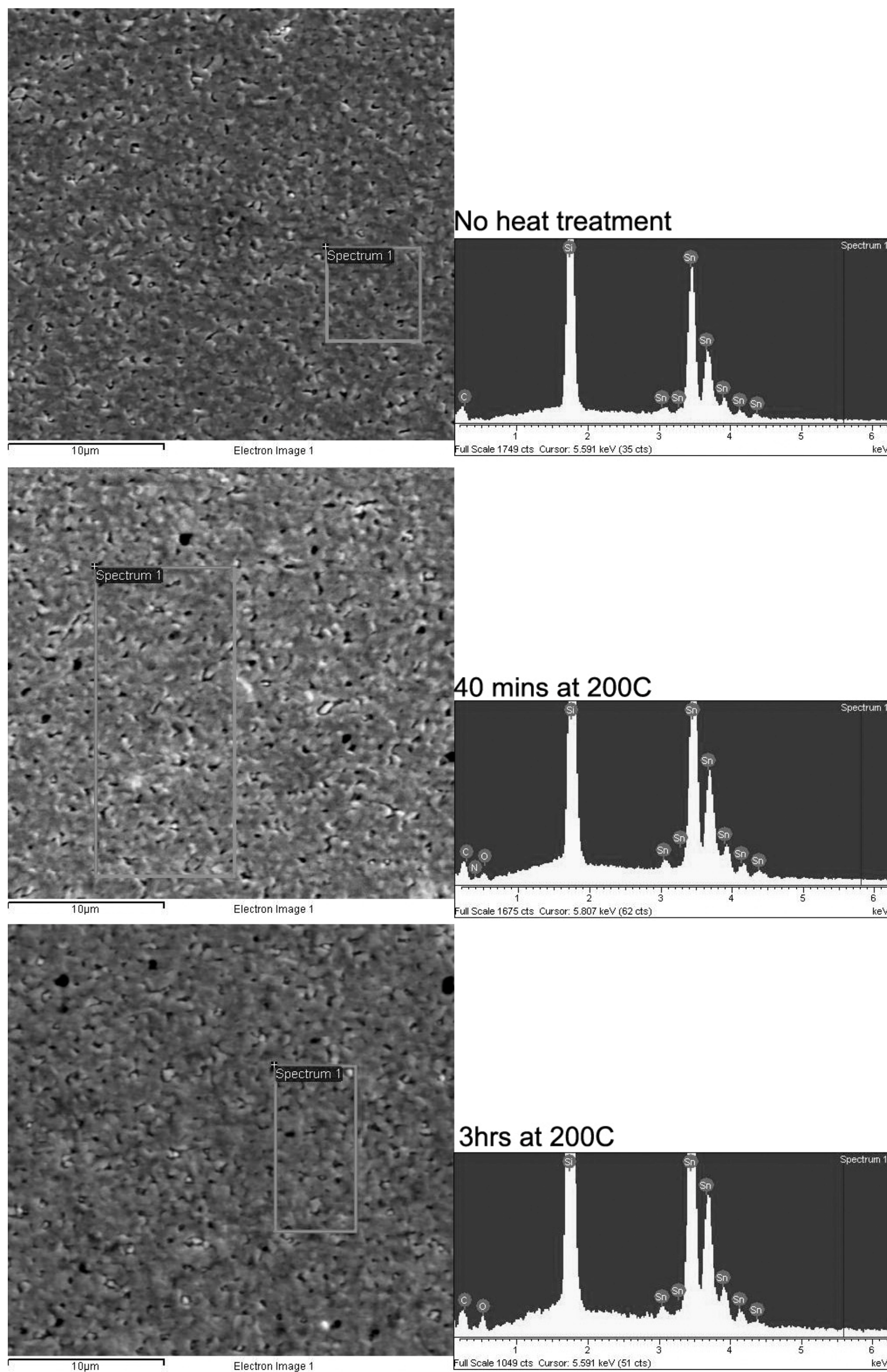


Figure 6.8: X-ray analysis of deposited tin metal surface before and after heat treatment.

Stannic oxide powder (SnO_2)-325 mesh, 99.9% (Sigma Aldrich- 244651) was thermally evaporated on chips with parallel plate platinum sensors, as shown in Figure 2.3 (Chapter-2). The SnO_2 powder (white color) was measured to yield a deposition thickness of 150nm. The pre-measured powder was thermally evaporated using a boron nitride crucible at 6 x 10^{-6} Torr belljar pressure. Along with the target chip, a TEM (Transmission Electron Microscope) carbon grid was also placed in the evaporator to evaluate the chemical composition and exact stoichiometry of the deposited film. The heating current was ramped to 8 ~ 10A and supply voltage of 60 ~ 70V. It was noted that even after prolonged heating (15mins in 3min steps) most of the powder remained in the crucible. The residue powder was grey in color. The target chips' surface had a yellowish layer, suggesting that some of the SnO_2 material did evaporate and was deposited on the surface of the die. A bright field TEM image of the deposited thin film indicates a continuous layer and is show in Figure 6.9. TEM diffraction pattern is shown in Figure 6.10.

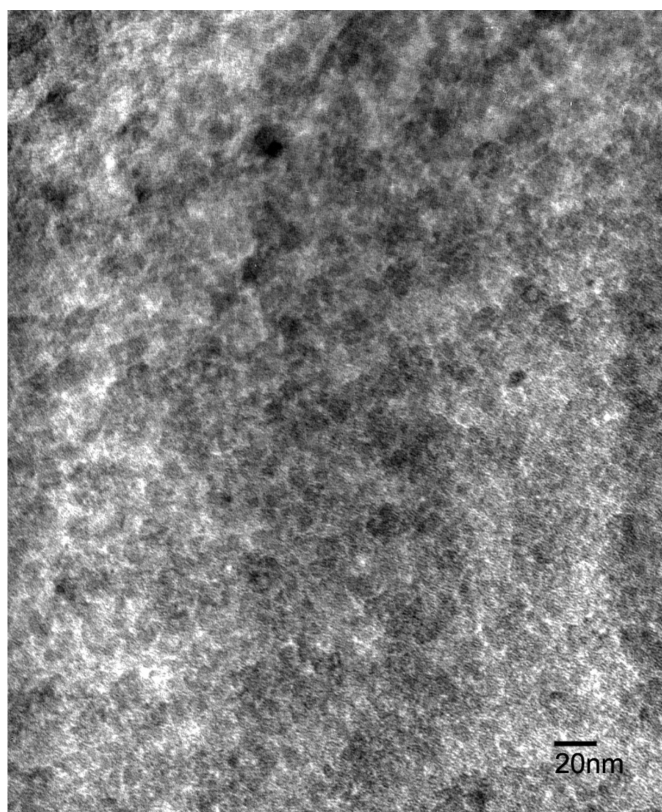


Figure 6.9: TEM bright field image of deposited SnO_x at 340KX magnification.

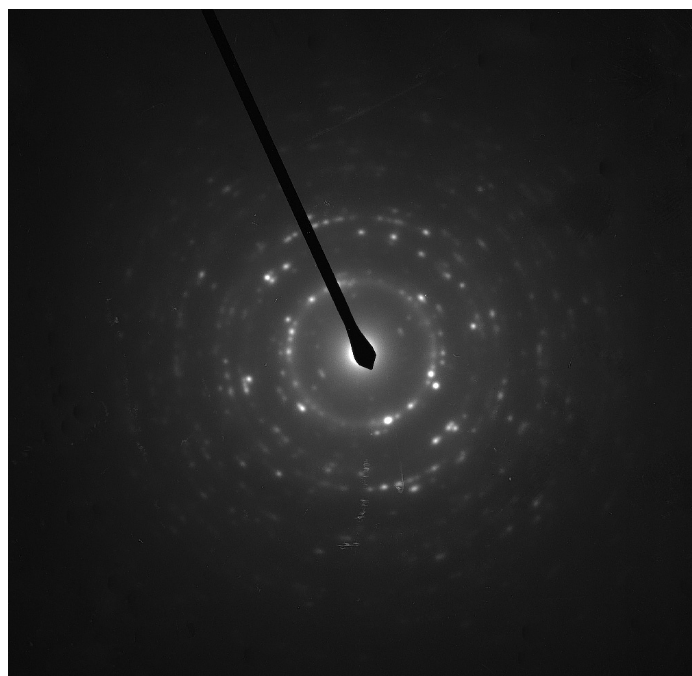


Figure 6.10: TEM diffraction pattern of thermally evaporated SnO_x.

D-spacing measurements from the TEM diffraction pattern can be used to identify the composition of the deposited material. The camera constant equals $2\lambda L$ =4.62 Å-cm. Ten rings were identified on the diffraction pattern negative and d-spacing in angstroms were calculated for each (d1=4.813, d2=3.638, d3=2.994, d4=2.695, d5=1.898, d6=1.597, d7=1.497, d8=1.342, d9=1.236, d10=1.078). The d-spacing measurements indicate a closest match to SnO with tetragonal system.

Electrical measurements of the chip after the deposition of tin oxide show an increase in the output amplitude (5-20mV) indicating that the sensor capacitance has increased after the deposition of the oxide. This was expected, as the addition of material between the plates of the sensor capacitor would increase the capacitance to a new value depending on the dielectric constant of the added material. The chip was exposed to high concentration (1000ppm) CO gas as before and the output showed no significant output response. This was likely because, the thermal evaporation done with the SnO_2 powder resulted in the deposition of SnO layer and also the deposited material was thin and

continuous. For effective CO gas sensing, the necessary stoichiometry of the deposited material should be SnO_2 and the deposited layer should have grains with large surface areas, which can generally be achieved by annealing at high temperatures. E-beam evaporation or sputtering can be used to obtain the right stoichiometry of SnO_2.

Instead of thermal evaporation, the tin oxide powder was directly used between the plates of the sensor. The commercial 325mesh stannic oxide powder was added to methanol to make a SnO_2 suspension (5mg in 5ml of methanol). The suspension was thoroughly mixed in an ultrasonicator and a few drops were added to the top of the die and allowed to air-dry for 10 minutes. The process was repeated after checking it under an optical microscope, until most of the sensor sites of the chip had a sparse distribution of tin oxide powder on top of them. Then, the FIB was used to micro-machine platinum walls to sandwich the dispersed tin oxide powder between two plates of platinum which were connected to the detection circuits. This resulted in a sensor with tin oxide powder as the dielectric material between the plates of the sensor capacitor. Examples of some of these FIB deposited sensors with tin oxide powder between the plates are shown in Figure 6.11.

Electrical testing after FIB sensor fabrication indicated that the plates have a leakage path between them. This was confirmed by X-ray analysis using the SEM. Since the tin oxide powder is porous with a spongy surface, the platinum metal from the deposition process of the FIB seemed to get re-deposited and adsorbed into the tin oxide powder resulting in a lower resistance material. This is shown in Figure 6.12 where the X-ray spectra indicate the presence of platinum metal in the tin oxide powder.

Instead of dispersing the tin oxide powder first and then fabricating the platinum bars, parallel plate platinum structures were pre-fabricated and then the tin oxide suspension was delivered to the top of the die. Figure 6.13 shows example parallel plate sensor structures prefabricated before the tin oxide powder was deposited. The suspension was allowed to dry for 10 minutes and the process was repeated until all the sensor structures with platinum walls had tin oxide powder between the plates. All the experiments with tin oxide suspension solution was performed on the fourth generation design which requires a 200ºC heat treatment for two hours after every FIB fabrication process.

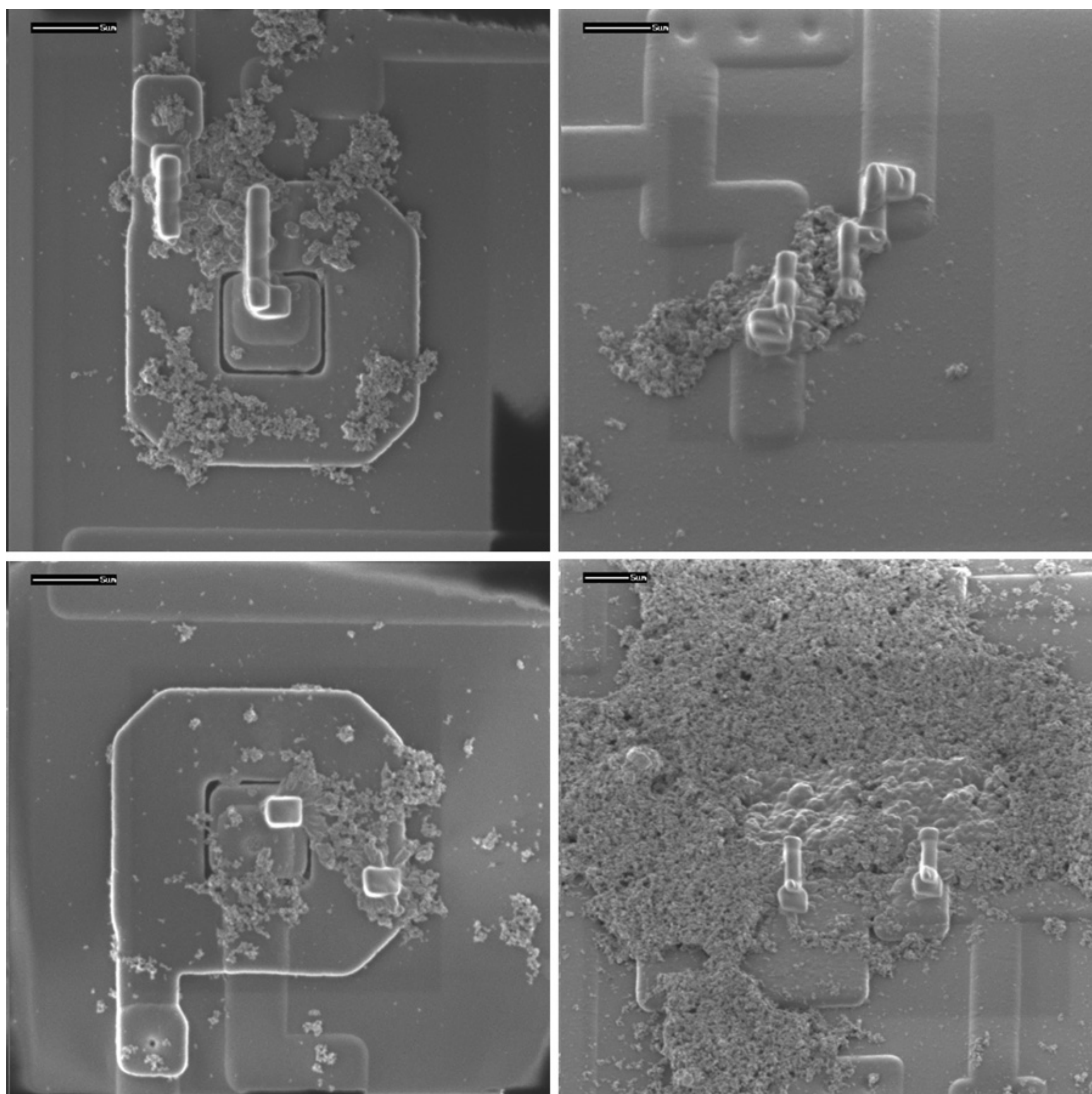


Figure 6.11: Secondary electron images of FIB deposited platinum sensor structures and electrical connections to the interconnects.

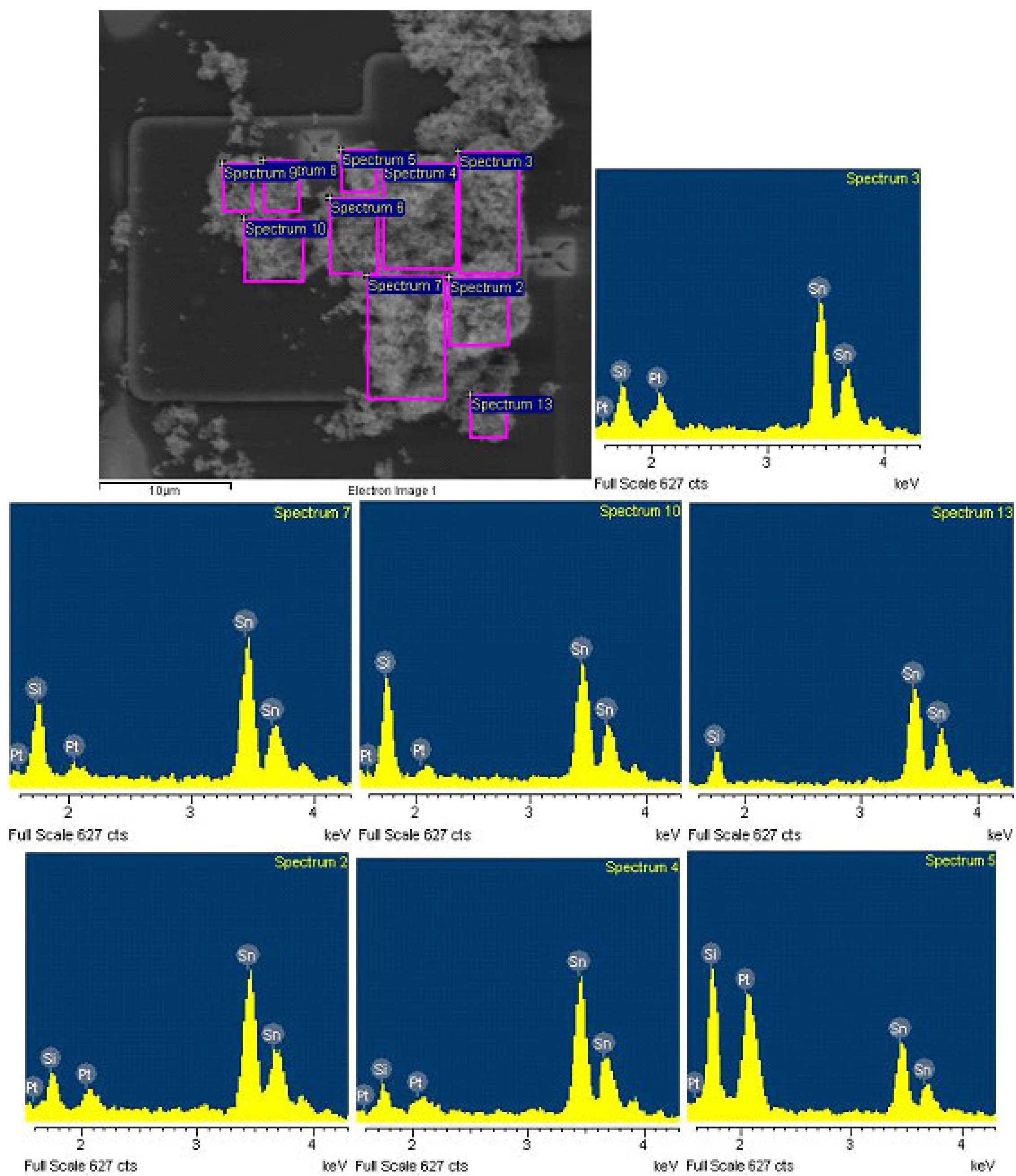


Figure 6.12: X-ray analysis of surface of tin oxide powder between FIB platinum connectors.

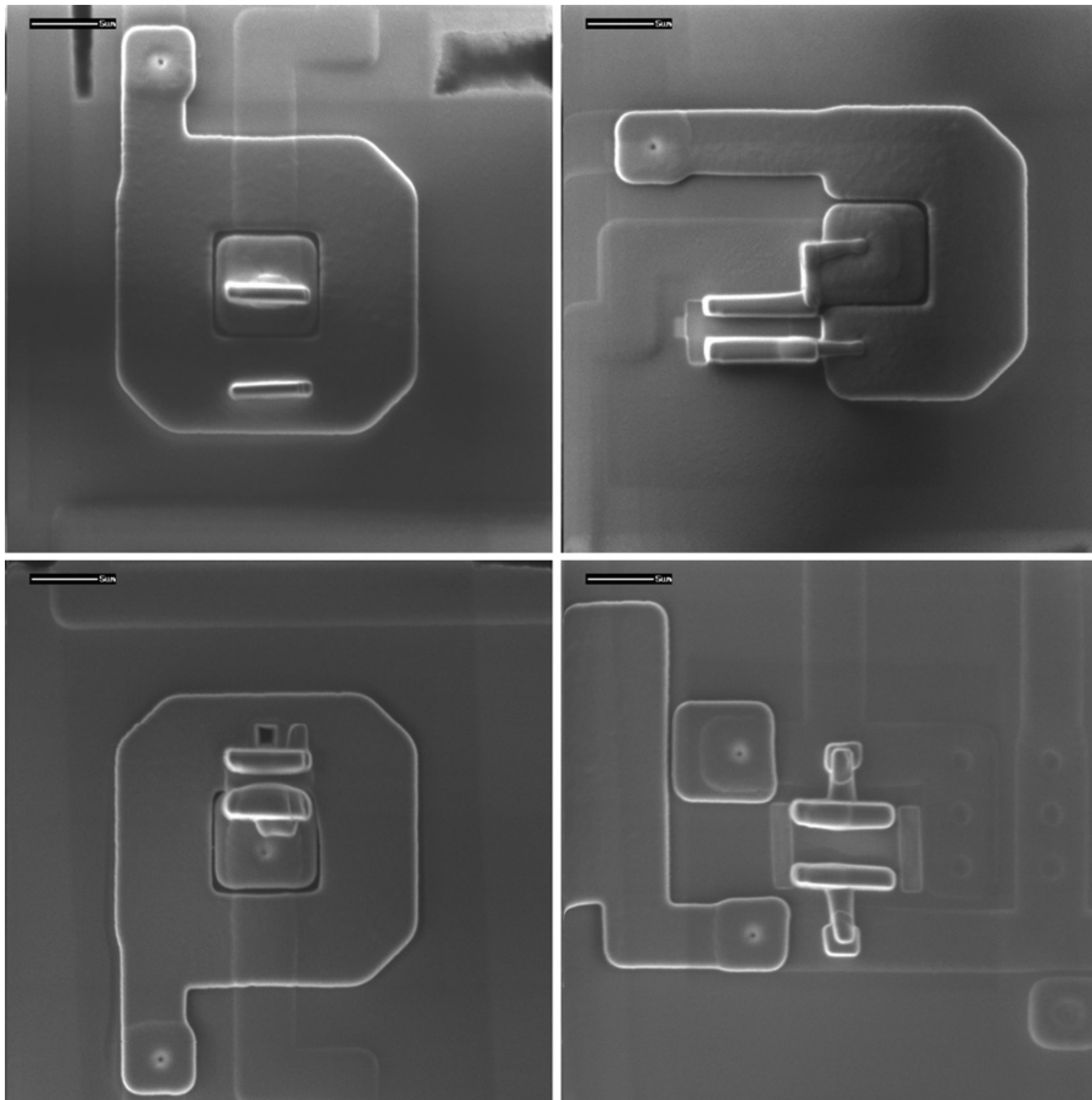


Figure 6.13: Secondary electron images of FIB pre-fabricated platinum sensor structures ready for tin oxide suspension.

The chip with these sensors is only evaluated in its ability to detect carbon monoxide at low concentrations. However, it is believed that detection of any gases known to respond to tin oxide based sensors as shown in prior experiments would also be realizable. The response of the sensor and the detection circuit to carbon monoxide gas exposure was evaluated by exposing the chip to increasing concentrations of carbon monoxide gas (mixed

with nitrogen gas for concentration control) at constant normal pressure and at room temperature. A gas flow test system was constructed consisting of a 2 liter acrylic chamber and calibrated flow meters to the measure the incoming gas flow (shown in Figure 6.14).

Figure 6.14: Digital photograph of the test setup for CO gas exposure testing.

The complete test board, including the chip under test was encased in the gas test chamber. Real time output from the chip was read by Agilent 34401A digital multi-meter and was recorded on a laptop computer using the GPIB of the multi-meter. Input sampling of the multi-meter was more rapid for DC inputs than AC inputs. In order to obtain real time measurements from the chip with 1sec sampling, the DC input option was chosen on the multi-meter, which is still representative of the output signal amplitude from the detection circuits. The concentration of the CO gas was varied by changing the flow of the mixing gas (nitrogen). A second detection circuit with no platinum sensor was also monitored using a standard multi-meter to detect any common output swing that may be

induced by noise pervasive to the whole chip. The output response of one of the sensor structure (1st sensor in Figure 6.13) with tin oxide powder between the parallel plates of the sensor capacitor is shown in Figures 6.15 and 6.16 for varying concentrations of CO gas. The output amplitude decreases when exposed to CO gas because, when the tin oxide reacts with the CO gas it generates electrons, which would increase the conductivity of the tin oxide. This increase in conductivity of the material between the plates of the sensor capacitor reduces the capacitance, which is reflected in the output of the detection circuits.

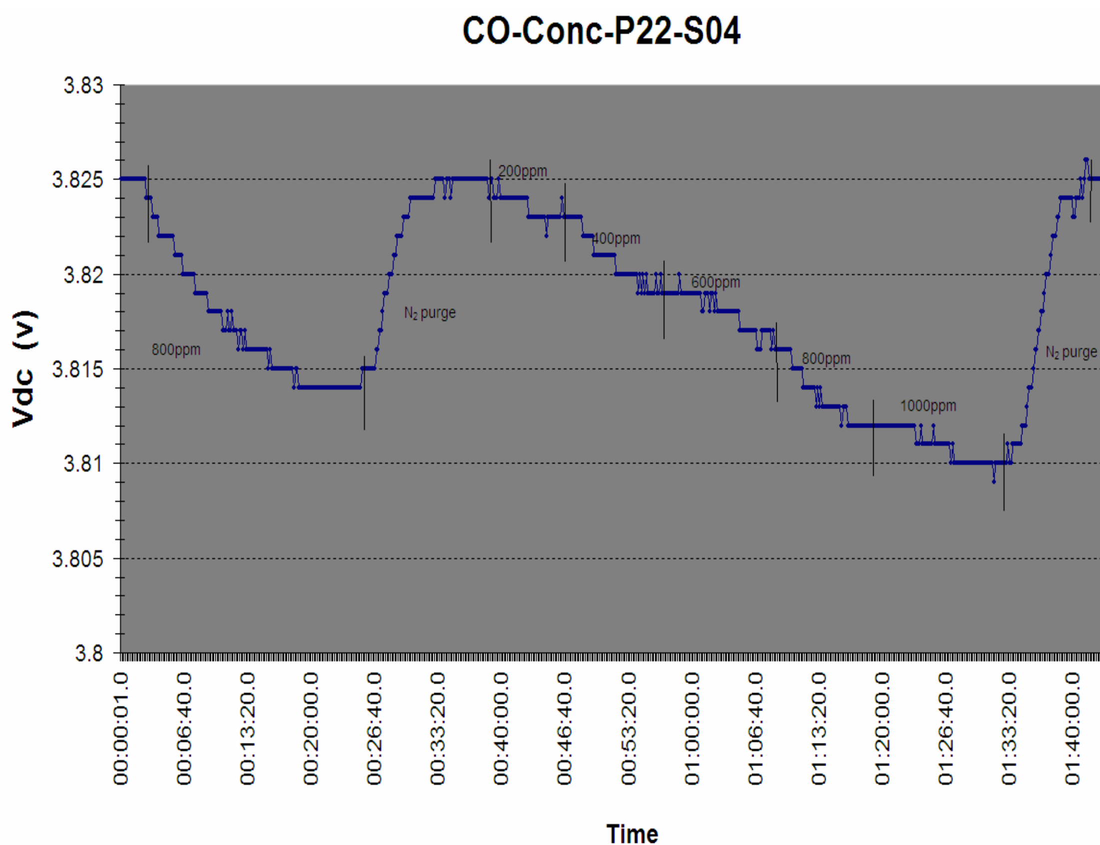


Figure 6.15: Output response of the sensor to large concentration swing followed by smaller concentration variations in CO gas.

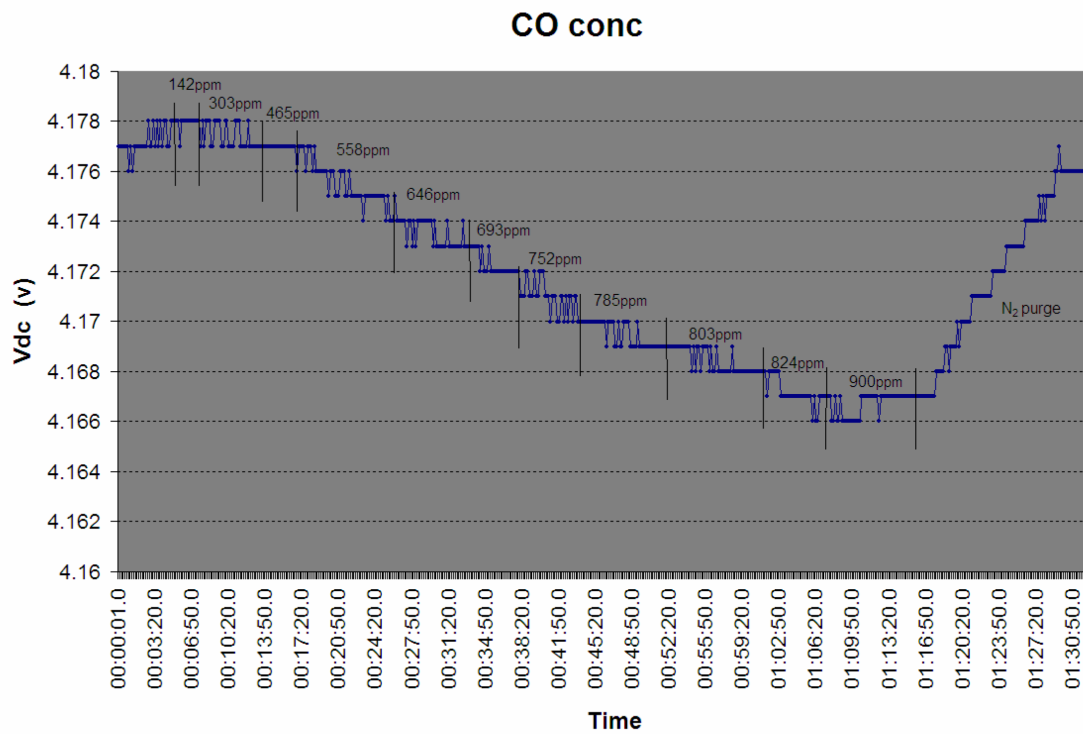


Figure 6.16: Output response of the sensor for varying CO gas concentrations.

The tin oxide platinum sensors show good detection response to CO gas. The response for higher concentrations of CO gas is almost immediate, as seen in Figure 6.15, for 800ppm CO. The volume of the test chamber was 2000cc and the flow of CO and N_2 gas mixture for 800ppm was 575 cc per minute. Assuming that the 800ppm test gas mixes and displaces the purge gas (N_2) present in the test chamber linearly, the response of the sensor to the estimated concentration of CO gas immediately after the introduction of test gas was plotted and is shown in Figure 6.17. The CO gas was introduced at t = 30 seconds and the sensor responded after 10secs with the corresponding CO gas concentration in the chamber estimated at 30ppm. The minimum detectable level for this particular sensor as per Figure 6.17 is 30ppm. Tin oxide sensors operating at room temperature are extremely sensitive to water vapor. It can be seen that the baseline or start value in Figure 6.15 is different than that in Figure 6.16. This is because the measurements were done on two different days with different relative humidity.

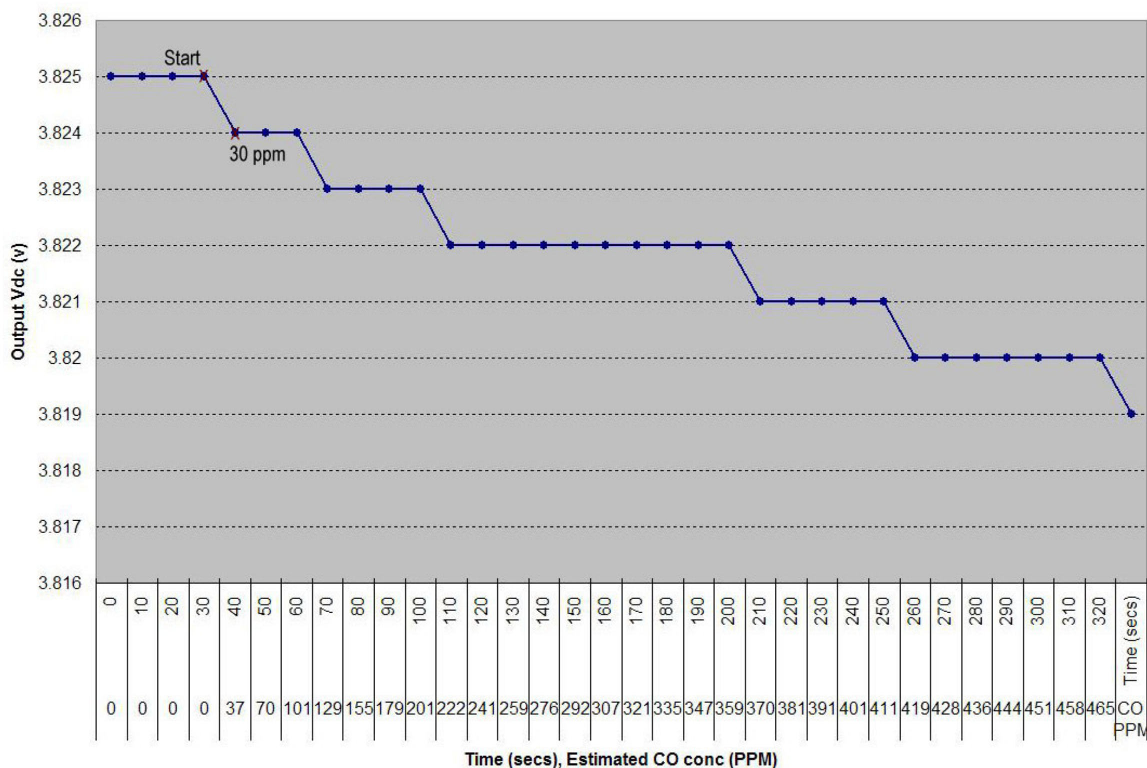


Figure 6.17: Output response of the sensor to estimated gas concentration in the test chamber during the first five minutes of 800ppm CO test gas exposure.

The minimum detectable level or the sensitivity depends on the sensor structure, the thickness of the tin oxide deposited between the sensor plates and also the surface area of tin oxide exposed to the sample gas. The scale of the sensors used was small and generally less than 10 square microns. In this application, the sensitivity can be greatly improved with minimum detectable levels much lower than 30ppm by making the sensors larger with more plates. However, it was found that longer exposure to the gallium beam in the vicinity of the sensor connect sites during FIB fabrication increased the problems caused by implanted gallium metal as explained in chapter 5 and the circuits would not revive even after heat treatment. This is a limitation of the fourth generation chips and can be easily rectified in future designs by not having overlapping metals at the sensor connect sites.

6.3. Early detection of Stroke

The detection of the neuroprotective gene is based on the principle of antigen antibody bonding between CART and anti-CART antibody. When the anti-CART peptide antibody bonds with the CART it would likely polarize differently with a different dipole moment than the individual components by themselves. The test setup for these measurements include the Agilent E3645A DC power supply, Agilent 34401A 6.5digit multi-meter, Hitachi VC-6155 Digital storage oscilloscope, and the test board to provide appropriate inputs to bias the chip. This setup is shown in Figure 6.18.

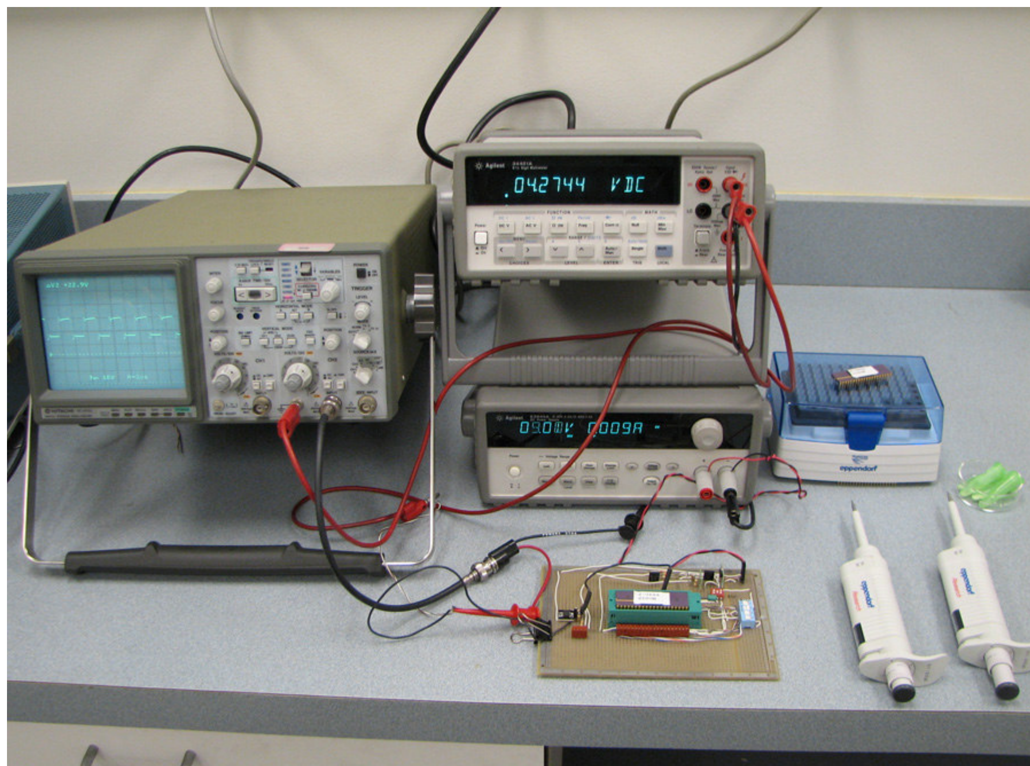


Figure 6.18: Digital photograph of the test setup for the detection of CART gene.

The third generation design has shown the best response for liquid test mediums. Since the interconnects themselves act as sensors, FIB sensor fabrication is unnecessary and also, these chips do not have flaws in the nitride passivation layer. Hence, third generation

chips with center glass reservoirs attached (Figure 5.19) were used for the detection of CART – anti-CART antibody interaction.

The two test solutions are CART (5mg in 0.1ml of saline) and anti-CART antibody (G-003-61, 1:1,000 of 200mg of rabbit IgG in 90ml PBS; Phoenix Pharmaceuticals, Belmont, CA). Since the test solutions were in saline and PBS (phosphate buffer saline solution), the chip was tested with varying concentrations of NaCl to understand the behavior of the sensors with increasing concentrations of salt in de-ionized (DI) water, and to also check where the baseline for PBS solution is with respect to DI water. An output response of one of the detection circuits is shown in Figure 6.19.

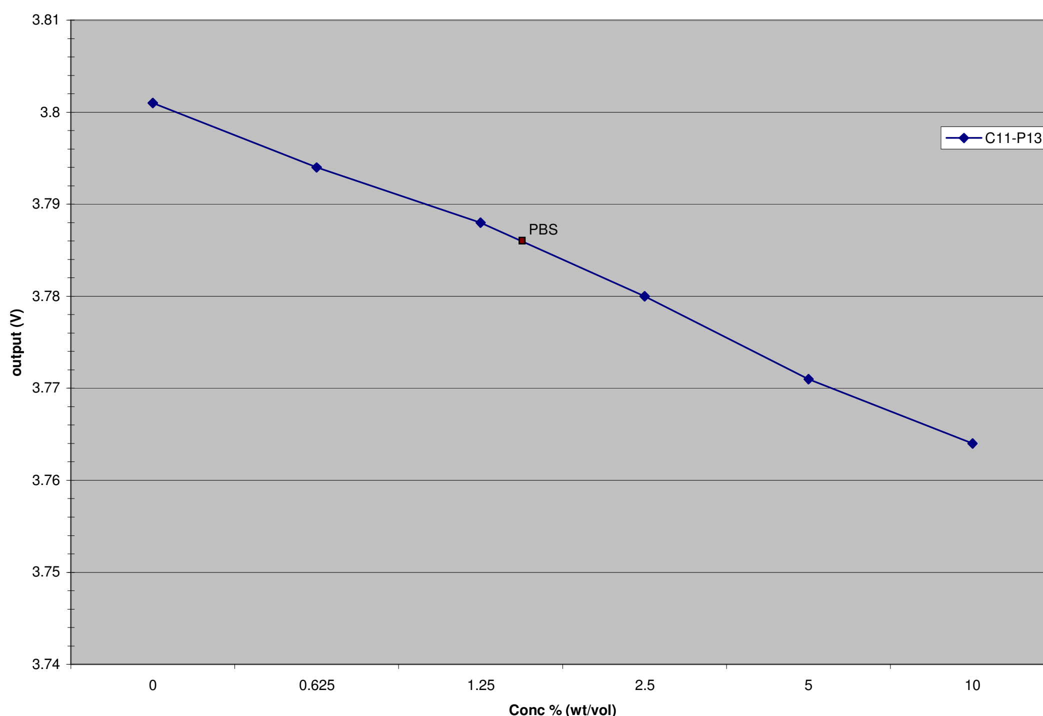


Figure 6.19: Output response of the sensor to different concentration of salt in DI water.

The output amplitude decreases with increasing concentrations of salt. This behavior is because, as the concentration of salt increases, the solution becomes more conductive and the dielectric behavior is reduced, which results in a smaller capacitance registered by the interconnect sensors. The two test solutions, CART and its antibody, were delivered

individually to the glass reservoir and their responses were noted. Equal volumes of these test solutions were mixed and incubated at room temperature for 15 minutes. The reaction mixture was then delivered to the glass reservoir in the center of the chip using a micro pipette. The output response of four detection circuits to these test solutions is shown in Figure 6.20.

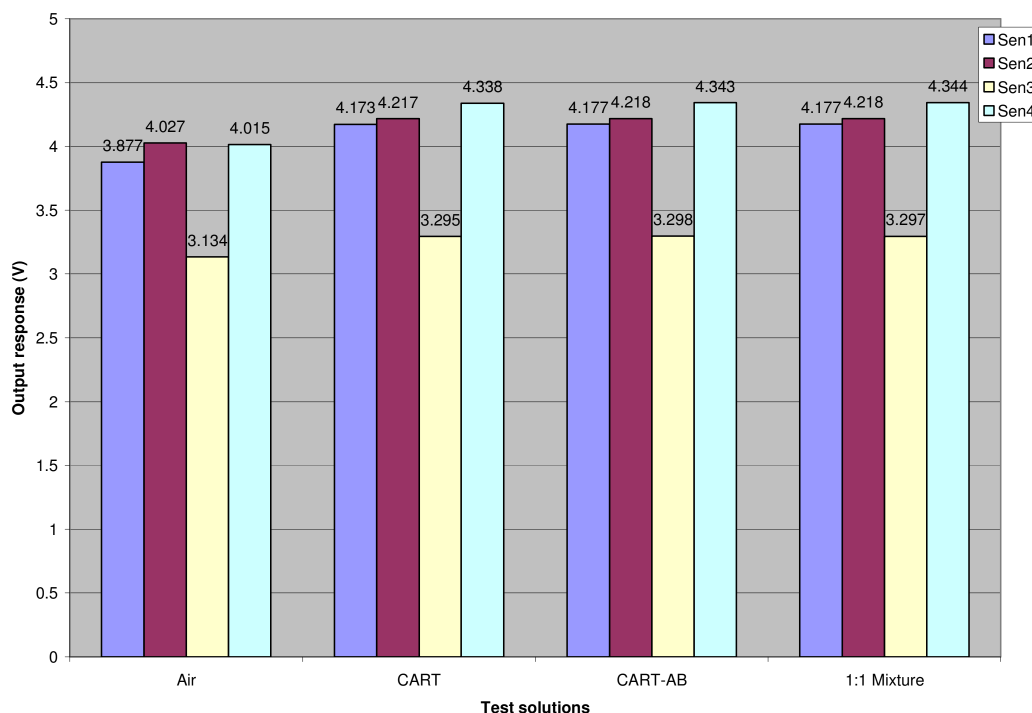


Figure 6.20: Output response of 3rd gen chip with glass tube for CART and anti-CART interaction.

The response of the system for individual test solutions shows that the anti-CART antibody generally has a higher response than CART. This means that the dielectric constant of the antibody solution is larger than that of the CART. This change could be caused by the carrier solutions alone (saline Vs PBS) and not by the active reactant components. Also, the reaction mixture does not show a significant difference from the individual components. This is either because the bonded CART and anti-CART antibody structures do not polarize differently than the individual components or the concentrations of the test solutions are not high enough to be detected by the system. Further tests need to be performed with increased

concentrations of the test solutions to confirm the application of this system for the detection of CART.

6.4 Test system calibration

The sensors, after being treated with active target specific layers will be subjected to the ambient medium containing the target molecules. Each of the components of the sensor and all the individual elements involved in the reaction at the sensor will likely polarize differently and will contribute to the overall change in the measured dielectric constant. It is necessary to measure the individual responses of the reactants and then determine a baseline for the reaction. In order to minimize measurement errors, it is imperative to measure and qualify the effects of all the elements that may be present in a real test ambient that are not active participants in the reaction. For instance, salinity of the test solutions has a direct effect on the output value as shown in Figure 6.19. So, baseline measurements for the entire salinity range expected in the real test environment have to be quantified to minimize errors. For applications involving detection in liquid mediums, it can be visualized that unattached non target molecules may be present between the plates of the sensor capacitor and cause variations in the output as they move between the plates. These variations have to be quantified over a period of time and added to the total error percentage of the system. This effect would be more pronounced and limiting if the dielectric behavior of these molecules is similar to that of the target molecule.

It was found that the output signal varies between chips from the same fabrication run. This is due to fabrication process variations and was found to be as high as 10 % of the output value in the fourth generation chips. This is not an issue, since absolute capacitance is not being measured and only change from initial value is measured as output signal. However, this means that a separate baseline reading has to be established against a known test sample for every chip.

The active capacitor charging currents of the individual detection circuits in all the generations of chips are directly related to the supply voltage. Any variations in the power supply would alter the output signal, thereby having poor Power Supply Rejection Ratio

(PSRR). Also the temperature dependencies of the detection circuits are shown in chapter 4. Immunity to variations in supply voltage, temperature variations and immunity to noises common to the whole chip can be achieved by measuring the difference signal between a well matched detection circuit pair as output signal. This can be achieved by connecting the outputs of the detection circuit pair on the chip to an external differential amplifier as shown in Figure 6.21. Identical detection circuits were designed in pairs in the fourth generation chips for this purpose.

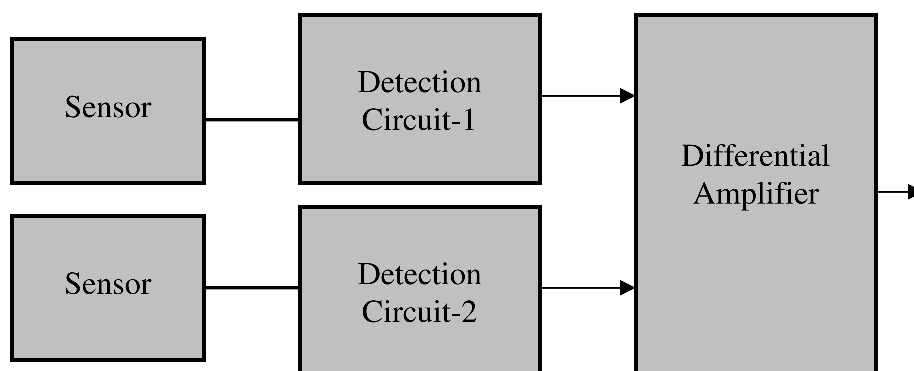


Figure 6.21: Detection circuit pair for noise immunity and good PSRR.

The differential amplifiers can also be implemented on the chip, but were left external to keep the design simple. The surface of the chips may be exposed to harsh liquid mediums while testing and have a good probability of surface insulation failure. If the differential amplifier is left external, when one channel fails, another channel can be used in its place at the sacrifice of additional offset voltage caused by mismatch between the two circuits. Only one sensor can be exposed to the test environment. If both the sensors are exposed, their responses will be common and will be cancelled by the differential amplifier.

The integrated chips can be reused with adequate cleaning between tests to remove any residue from previous experiments. It was found that cleaning the die surface with 10% SDS solution, followed by de-ionized water cleansing effectively removed protein residue (Figure 6.1). When the detection technique involves bonding of the target to the sensor surface, the sensor has to be reactivated after each trial. For example, if the sensor surface

was treated with a target specific antibody, methods have to be developed to break the antigen-antibody bond and reactivate the antibody after each test. Generally, chip failure was found to be due to silicon nitride passivation failure. This depends on the harshness of the test solution. An alternative thin blanket insulation material needs to be deposited to yield a stable insulation layer and improve reliability.

Relative permittivity of any material is generally a complex function of frequency of the applied field as explained in chapter 2. Each of the components of the sensor and all the individual elements involved in the reaction at the sensor may polarize differently at different frequencies. For the applications that were tested on the sensor array chip, the clock frequency was initially varied between 50 KHz and 800 KHz to isolate frequencies that may induce larger polarization of the target molecule which would increase sensitivity. However, no indicative gain was observed for the frequencies ranges that were tested. For any particular application, it is important to investigate the frequency response of the sensor materials and the test mediums used to capitalize on any increased sensitivity that might result due to the frequency dependency of polarization.

7. Conclusion and Future Work

With the advancement in sensor technology, a multitude of discrete stand alone sensors have been developed for the detection of very low concentrations of target molecules. Many of these sensing techniques have been modified and developed to be manufactured using integrated chip technology. This allows for miniaturization and low cost mass production. The measuring or quantifying electronics can also be integrated on the same device, which would minimize the usage of bulky and expensive instruments. This has been the basis for the development of various lab-on-chip (LOC) detection techniques, which are usually geared towards the bio-tech industry, dealing frequently with analysis of target molecules in liquid medium. Similar integrated technology has also evolved for the detection of gaseous analytes and is commonly known as electronic nose or e-nose. It would be of great advantage if multiple targets in both liquid and gaseous mediums can be identified and quantified by a single device simultaneously.

In this dissertation, I have developed a sensor-array chip hybrid for rapid parallel detection of multiple organic or inorganic target molecules in either gas or liquid mediums. The developed system is based on measuring minute changes in capacitances for detection. The sensors in the designed sensor-array chip hybrid are capacitive sensors, micro fabricated on top of a pre-designed CMOS chips with circuitry to measure small changes in capacitance. The various transduction methods (amperometric, potentiometric, etc.) used in sensors can be potentially modified to work with the proposed system. For example, a conventional amperometric system relies on the generation of current (electrons) for detection. If the same transducer material that generates current in the presence of the target molecule were incorporated in the proposed capacitor sensors, generation of current would reflect as a reduction in capacitance of the sensor capacitor. This change in capacitance would be measured by the integrated circuits on the chip.

The capacitor sensors were built using the well advanced technique of focused ion beam (FIB) micromachining and microforming. The FIB workstation has been commonly used in the micro-electronics industry for micro-fabrication, post fabrication editing and debugging. The use of the FIB workstation for fabricating the sensors shortens the development period and allows for rapid prototyping of sensor geometries for any given application. The fabrication of sensors using conventional lithography or MEMS techniques is time consuming and expensive because any small changes made to the sensor structure require the production of a new lithography mask and re-fabrication of the entire chip. The FIB workstation can be used for prototyping the sensor structures during development, and once the sensor geometry has been optimized, conventional lithography and thick film deposition techniques can replace the FIB for mass production.

I have also demonstrated two detection circuit techniques that are sensitive to sub femto farad changes in sensor capacitance. One of the designed detection circuits converts the changes in sensor capacitance to changes in frequency of a square wave output. This detection circuit scheme has the advantage of being able to detect a wide range of input sensor capacitance modulation at the sacrifice of gain. The second detection circuit technique converts the changes in sensor capacitance to amplitude variations. This detection circuit method has a maximum limit for the sensor capacitance value. So a range of detection circuits with limits varying from 250ff to 750ff were developed to preserve input dynamic range.

I have also demonstrated how the system could be used in diverse applications for the detection of target molecules in liquid or gas mediums. I have evaluated the applications of this system in aiding multidisciplinary research including, detection and measurement of organophosphate neurotoxins, air quality monitoring - detection of low concentrations of carbon monoxide gas, and aid in the study of the biochemistry of stroke. In the applications for the detection of OP neurotoxins and CART neuroprotective gene, the sensor-array system was tested with the same concentrations of test solutions that were verified by conventional biological assay techniques. It was shown that the detection system was not sensitive at those concentrations. Further research needs to be done with increased concentrations of the test solutions to evaluate the effectiveness of the proposed system in

those applications. A tin oxide based CO gas sensor system was fabricated and was verified to be sensitive to low concentrations (30ppm) of CO gas at room temperatures. Further research needs to be performed to determine the selectivity of the gas sensor. It was found that the gas sensor was sensitive to water vapor, hence effective materials and techniques need to be developed to prevent the water vapor from reaching the tin oxide layer. One possible method would be to deposit a second blanket layer of material on top of the die, which would selectively allow the diffusion of CO gas and prevent the water vapor from reaching the tin oxide surface. The tin oxide layer was deposited on the chip surface by drying a simple suspension of tin oxide powder. This paves the way for testing a myriad of indicator materials that could be sensitive to a variety of target molecules. The sensor-array chip hybrid can be effectively used in the development of new sensor technologies. Each sensor site in the array can be precisely coated with different test detection materials using drop on demand [42] or inkjet printing techniques [43]. The entire chip with the multiple detection materials can be exposed to a test environment containing the target molecules and based on the output response of each of the detection circuits, the effective sensor material can be isolated. This greatly reduces development time.

In the detection circuits developed for the third and fourth generation of chips, the gate capacitance of the output buffer stages adds to the value of the reference capacitance. This alters the gain of the circuit. A two stage output buffer with the larger transistors in the second stage needs to be incorporated in future designs to keep the gain of the circuits more predictable and stable. In the fourth generation design it was found that the outputs of two detection circuits with the same input sensor capacitor structures were not matched. This is most likely because of fabrication process variations causing dissimilarity in the poly reference capacitor geometry. The matching can be improved in future designs by avoiding sharp corners in the design of capacitor structures and also by surrounding the poly capacitor with dummy redundant poly structures which would help during chemical mechanical planarization (CMP) process of fabrication. The third generation design had long interconnects from the detection circuits to the sensor sites. These long interconnects have been shown to function as sensors without the need for FIB fabricated sensors. Future designs can exploit this property of the interconnects behaving as sensors and interconnects

can be purposely designed in a serpentine structure to increase the sensitivity. These long interconnects would act as sensors for liquid test mediums. Shorter interconnects with sites for FIB sensor fabrication can be incorporated in the same layout for sensing in gas mediums. In the demonstrated systems, the differential amplifier and the bias were left external. These can also be included in the design of future chips. The sensor-array chip hybrids were fabricated using 1.5μm process; future designs can be scaled to much smaller processes (≤0.35μm). This would allow for thinner interconnects and reduce the parasitic capacitances of the sensor interconnects which would improve system sensitivity.

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Appendix A. CO Gas Test 1 Raw Data – 10 Secs Sampling

Time	Output (V)	Time	Output (V)	Time	Output (V)	Time	Output (V)
00:00:01.0	3.825	00:06:50.0	3.82	00:13:40.0	3.816	00:20:30.0	3.814
00:00:10.0	3.825	00:07:00.0	3.82	00:13:50.0	3.816	00:20:40.0	3.814
00:00:20.0	3.825	00:07:10.0	3.82	00:14:00.0	3.816	00:20:50.0	3.814
00:00:30.0	3.825	00:07:20.0	3.82	00:14:10.0	3.816	00:21:00.0	3.814
00:00:40.0	3.825	00:07:30.0	3.82	00:14:20.0	3.816	00:21:10.0	3.814
00:00:50.0	3.825	00:07:40.0	3.82	00:14:30.0	3.816	00:21:20.0	3.814
00:01:00.0	3.825	00:07:50.0	3.819	00:14:40.0	3.816	00:21:30.0	3.814
00:01:10.0	3.825	00:08:00.0	3.819	00:14:50.0	3.816	00:21:40.0	3.814
00:01:20.0	3.825	00:08:10.0	3.819	00:15:00.0	3.816	00:21:50.0	3.814
00:01:30.0	3.825	00:08:20.0	3.819	00:15:10.0	3.816	00:22:00.0	3.814
00:01:40.0	3.825	00:08:30.0	3.819	00:15:20.0	3.816	00:22:10.0	3.814
00:01:50.0	3.825	00:08:40.0	3.819	00:15:30.0	3.815	00:22:20.0	3.814
00:02:00.0	3.825	00:08:50.0	3.819	00:15:40.0	3.816	00:22:30.0	3.814
00:02:10.0	3.825	00:09:00.0	3.819	00:15:50.0	3.815	00:22:40.0	3.814
00:02:20.0	3.825	00:09:10.0	3.818	00:16:00.0	3.815	00:22:50.0	3.814
00:02:30.0	3.825	00:09:20.0	3.818	00:16:10.0	3.815	00:23:00.0	3.814
00:02:40.0	3.824	00:09:30.0	3.818	00:16:20.0	3.815	00:23:10.0	3.814
00:02:50.0	3.824	00:09:40.0	3.818	00:16:30.0	3.815	00:23:20.0	3.814
00:03:00.0	3.824	00:09:50.0	3.818	00:16:40.0	3.815	00:23:30.0	3.814
00:03:10.0	3.824	00:10:00.0	3.818	00:16:50.0	3.815	00:23:40.0	3.814
00:03:20.0	3.823	00:10:10.0	3.818	00:17:00.0	3.815	00:23:50.0	3.814
00:03:30.0	3.823	00:10:20.0	3.818	00:17:10.0	3.815	00:24:00.0	3.814
00:03:40.0	3.823	00:10:30.0	3.818	00:17:20.0	3.815	00:24:10.0	3.814
00:03:50.0	3.823	00:10:40.0	3.817	00:17:30.0	3.815	00:24:20.0	3.814
00:04:00.0	3.822	00:10:50.0	3.817	00:17:40.0	3.815	00:24:30.0	3.814
00:04:10.0	3.822	00:11:00.0	3.817	00:17:50.0	3.815	00:24:40.0	3.814
00:04:20.0	3.822	00:11:10.0	3.818	00:18:00.0	3.815	00:24:50.0	3.814
00:04:30.0	3.822	00:11:20.0	3.817	00:18:10.0	3.814	00:25:00.0	3.814
00:04:40.0	3.822	00:11:30.0	3.817	00:18:20.0	3.815	00:25:10.0	3.814
00:04:50.0	3.822	00:11:40.0	3.818	00:18:30.0	3.815	00:25:20.0	3.815
00:05:00.0	3.822	00:11:50.0	3.817	00:18:40.0	3.814	00:25:30.0	3.815
00:05:10.0	3.822	00:12:00.0	3.817	00:18:50.0	3.814	00:25:40.0	3.815
00:05:20.0	3.822	00:12:10.0	3.817	00:19:00.0	3.814	00:25:50.0	3.815
00:05:30.0	3.822	00:12:20.0	3.816	00:19:10.0	3.814	00:26:00.0	3.815
00:05:40.0	3.821	00:12:30.0	3.817	00:19:20.0	3.814	00:26:10.0	3.815
00:05:50.0	3.821	00:12:40.0	3.817	00:19:30.0	3.814	00:26:20.0	3.815
00:06:00.0	3.821	00:12:50.0	3.816	00:19:40.0	3.814	00:26:30.0	3.815
00:06:10.0	3.821	00:13:00.0	3.817	00:19:50.0	3.814	00:26:40.0	3.815
00:06:20.0	3.821	00:13:10.0	3.816	00:20:00.0	3.814	00:26:50.0	3.816
00:06:30.0	3.82	00:13:20.0	3.816	00:20:10.0	3.814	00:27:00.0	3.816
00:06:40.0	3.82	00:13:30.0	3.816	00:20:20.0	3.814	00:27:10.0	3.817

Time	Output (V)	Time	Output (V)	Time	Output (V)	Time	Output (V)
00:27:20.0	3.817	00:34:10.0	3.825	00:41:00.0	3.824	00:47:50.0	3.823
00:27:30.0	3.818	00:34:20.0	3.825	00:41:10.0	3.824	00:48:00.0	3.823
00:27:40.0	3.819	00:34:30.0	3.825	00:41:20.0	3.824	00:48:10.0	3.823
00:27:50.0	3.819	00:34:40.0	3.824	00:41:30.0	3.824	00:48:20.0	3.823
00:28:00.0	3.819	00:34:50.0	3.825	00:41:40.0	3.824	00:48:30.0	3.822
00:28:10.0	3.82	00:35:00.0	3.825	00:41:50.0	3.824	00:48:40.0	3.822
00:28:20.0	3.82	00:35:10.0	3.825	00:42:00.0	3.824	00:48:50.0	3.822
00:28:30.0	3.82	00:35:20.0	3.825	00:42:10.0	3.824	00:49:00.0	3.822
00:28:40.0	3.821	00:35:30.0	3.825	00:42:20.0	3.824	00:49:10.0	3.822
00:28:50.0	3.821	00:35:40.0	3.825	00:42:30.0	3.824	00:49:20.0	3.822
00:29:00.0	3.822	00:35:50.0	3.825	00:42:40.0	3.824	00:49:30.0	3.822
00:29:10.0	3.822	00:36:00.0	3.825	00:42:50.0	3.823	00:49:40.0	3.821
00:29:20.0	3.822	00:36:10.0	3.825	00:43:00.0	3.823	00:49:50.0	3.821
00:29:30.0	3.822	00:36:20.0	3.825	00:43:10.0	3.823	00:50:00.0	3.821
00:29:40.0	3.823	00:36:30.0	3.825	00:43:20.0	3.823	00:50:10.0	3.821
00:29:50.0	3.823	00:36:40.0	3.825	00:43:30.0	3.823	00:50:20.0	3.821
00:30:00.0	3.823	00:36:50.0	3.825	00:43:40.0	3.823	00:50:30.0	3.821
00:30:10.0	3.823	00:37:00.0	3.825	00:43:50.0	3.823	00:50:40.0	3.821
00:30:20.0	3.824	00:37:10.0	3.825	00:44:00.0	3.823	00:50:50.0	3.821
00:30:30.0	3.824	00:37:20.0	3.825	00:44:10.0	3.823	00:51:00.0	3.821
00:30:40.0	3.824	00:37:30.0	3.825	00:44:20.0	3.823	00:51:10.0	3.821
00:30:50.0	3.824	00:37:40.0	3.825	00:44:30.0	3.823	00:51:20.0	3.821
00:31:00.0	3.824	00:37:50.0	3.825	00:44:40.0	3.822	00:51:30.0	3.821
00:31:10.0	3.824	00:38:00.0	3.825	00:44:50.0	3.823	00:51:40.0	3.821
00:31:20.0	3.824	00:38:10.0	3.825	00:45:00.0	3.823	00:51:50.0	3.821
00:31:30.0	3.824	00:38:20.0	3.825	00:45:10.0	3.823	00:52:00.0	3.82
00:31:40.0	3.824	00:38:30.0	3.825	00:45:20.0	3.823	00:52:10.0	3.82
00:31:50.0	3.824	00:38:40.0	3.824	00:45:30.0	3.823	00:52:20.0	3.82
00:32:00.0	3.824	00:38:50.0	3.825	00:45:40.0	3.823	00:52:30.0	3.82
00:32:10.0	3.824	00:39:00.0	3.825	00:45:50.0	3.823	00:52:40.0	3.82
00:32:20.0	3.824	00:39:10.0	3.824	00:46:00.0	3.823	00:52:50.0	3.82
00:32:30.0	3.824	00:39:20.0	3.824	00:46:10.0	3.823	00:53:00.0	3.82
00:32:40.0	3.824	00:39:30.0	3.824	00:46:20.0	3.824	00:53:10.0	3.82
00:32:50.0	3.824	00:39:40.0	3.825	00:46:30.0	3.823	00:53:20.0	3.82
00:33:00.0	3.825	00:39:50.0	3.824	00:46:40.0	3.823	00:53:30.0	3.82
00:33:10.0	3.825	00:40:00.0	3.824	00:46:50.0	3.823	00:53:40.0	3.82
00:33:20.0	3.825	00:40:10.0	3.824	00:47:00.0	3.823	00:53:50.0	3.82
00:33:30.0	3.825	00:40:20.0	3.824	00:47:10.0	3.823	00:54:00.0	3.82
00:33:40.0	3.825	00:40:30.0	3.824	00:47:20.0	3.823	00:54:10.0	3.82
00:33:50.0	3.825	00:40:40.0	3.824	00:47:30.0	3.823	00:54:20.0	3.819
00:34:00.0	3.824	00:40:50.0	3.824	00:47:40.0	3.823	00:54:30.0	3.82

Time	Output (V)	Time	Output (V)	Time	Output (V)	Time	Output (V)
00:54:40.0	3.819	01:01:30.0	3.819	01:08:20.0	3.816	01:15:10.0	3.813
00:54:50.0	3.82	01:01:40.0	3.819	01:08:30.0	3.817	01:15:20.0	3.813
00:55:00.0	3.819	01:01:50.0	3.818	01:08:40.0	3.816	01:15:30.0	3.813
00:55:10.0	3.82	01:02:00.0	3.819	01:08:50.0	3.816	01:15:40.0	3.812
00:55:20.0	3.819	01:02:10.0	3.819	01:09:00.0	3.816	01:15:50.0	3.813
00:55:30.0	3.819	01:02:20.0	3.818	01:09:10.0	3.816	01:16:00.0	3.813
00:55:40.0	3.819	01:02:30.0	3.819	01:09:20.0	3.816	01:16:10.0	3.813
00:55:50.0	3.819	01:02:40.0	3.818	01:09:30.0	3.816	01:16:20.0	3.812
00:56:00.0	3.819	01:02:50.0	3.818	01:09:40.0	3.816	01:16:30.0	3.812
00:56:10.0	3.82	01:03:00.0	3.818	01:09:50.0	3.816	01:16:40.0	3.812
00:56:20.0	3.819	01:03:10.0	3.818	01:10:00.0	3.816	01:16:50.0	3.812
00:56:30.0	3.819	01:03:20.0	3.818	01:10:10.0	3.816	01:17:00.0	3.812
00:56:40.0	3.82	01:03:30.0	3.818	01:10:20.0	3.816	01:17:10.0	3.812
00:56:50.0	3.819	01:03:40.0	3.818	01:10:30.0	3.815	01:17:20.0	3.812
00:57:00.0	3.819	01:03:50.0	3.818	01:10:40.0	3.815	01:17:30.0	3.812
00:57:10.0	3.819	01:04:00.0	3.818	01:10:50.0	3.815	01:17:40.0	3.812
00:57:20.0	3.819	01:04:10.0	3.818	01:11:00.0	3.815	01:17:50.0	3.812
00:57:30.0	3.819	01:04:20.0	3.818	01:11:10.0	3.815	01:18:00.0	3.812
00:57:40.0	3.819	01:04:30.0	3.818	01:11:20.0	3.815	01:18:10.0	3.812
00:57:50.0	3.819	01:04:40.0	3.818	01:11:30.0	3.815	01:18:20.0	3.812
00:58:00.0	3.819	01:04:50.0	3.818	01:11:40.0	3.814	01:18:30.0	3.812
00:58:10.0	3.819	01:05:00.0	3.817	01:11:50.0	3.814	01:18:40.0	3.812
00:58:20.0	3.819	01:05:10.0	3.817	01:12:00.0	3.814	01:18:50.0	3.812
00:58:30.0	3.819	01:05:20.0	3.817	01:12:10.0	3.814	01:19:00.0	3.812
00:58:40.0	3.82	01:05:30.0	3.817	01:12:20.0	3.814	01:19:10.0	3.812
00:58:50.0	3.819	01:05:40.0	3.817	01:12:30.0	3.814	01:19:20.0	3.812
00:59:00.0	3.819	01:05:50.0	3.817	01:12:40.0	3.814	01:19:30.0	3.812
00:59:10.0	3.819	01:06:00.0	3.817	01:12:50.0	3.814	01:19:40.0	3.812
00:59:20.0	3.819	01:06:10.0	3.817	01:13:00.0	3.813	01:19:50.0	3.812
00:59:30.0	3.819	01:06:20.0	3.817	01:13:10.0	3.814	01:20:00.0	3.812
00:59:40.0	3.819	01:06:30.0	3.817	01:13:20.0	3.813	01:20:10.0	3.812
00:59:50.0	3.819	01:06:40.0	3.817	01:13:30.0	3.814	01:20:20.0	3.812
01:00:00.0	3.819	01:06:50.0	3.816	01:13:40.0	3.813	01:20:30.0	3.812
01:00:10.0	3.819	01:07:00.0	3.816	01:13:50.0	3.813	01:20:40.0	3.812
01:00:20.0	3.819	01:07:10.0	3.816	01:14:00.0	3.813	01:20:50.0	3.812
01:00:30.0	3.819	01:07:20.0	3.817	01:14:10.0	3.813	01:21:00.0	3.812
01:00:40.0	3.819	01:07:30.0	3.817	01:14:20.0	3.813	01:21:10.0	3.812
01:00:50.0	3.819	01:07:40.0	3.817	01:14:30.0	3.813	01:21:20.0	3.812
01:01:00.0	3.818	01:07:50.0	3.817	01:14:40.0	3.813	01:21:30.0	3.812
01:01:10.0	3.818	01:08:00.0	3.817	01:14:50.0	3.813	01:21:40.0	3.812
01:01:20.0	3.819	01:08:10.0	3.817	01:15:00.0	3.813	01:21:50.0	3.812

Time	Output (V)	Time	Output (V)	Time	Output (V)	Time	Output (V)
01:22:00.0	3.812	01:28:50.0	3.81	01:35:40.0	3.814	01:42:30.0	3.825
01:22:10.0	3.812	01:29:00.0	3.81	01:35:50.0	3.815	01:42:40.0	3.825
01:22:20.0	3.812	01:29:10.0	3.81	01:36:00.0	3.816	01:42:50.0	3.825
01:22:30.0	3.812	01:29:20.0	3.81	01:36:10.0	3.816	01:43:00.0	3.825
01:22:40.0	3.812	01:29:30.0	3.81	01:36:20.0	3.817	01:43:10.0	3.825
01:22:50.0	3.812	01:29:40.0	3.81	01:36:30.0	3.817	01:43:20.0	3.825
01:23:00.0	3.812	01:29:50.0	3.81	01:36:40.0	3.818	01:43:30.0	3.825
01:23:10.0	3.812	01:30:00.0	3.81	01:36:50.0	3.818	01:43:40.0	3.825
01:23:20.0	3.812	01:30:10.0	3.81	01:37:00.0	3.819	01:43:50.0	3.824
01:23:30.0	3.811	01:30:20.0	3.81	01:37:10.0	3.82		
01:23:40.0	3.811	01:30:30.0	3.81	01:37:20.0	3.82		
01:23:50.0	3.811	01:30:40.0	3.81	01:37:30.0	3.82		
01:24:00.0	3.812	01:30:50.0	3.81	01:37:40.0	3.821		
01:24:10.0	3.811	01:31:00.0	3.81	01:37:50.0	3.822		
01:24:20.0	3.811	01:31:10.0	3.81	01:38:00.0	3.822		
01:24:30.0	3.811	01:31:20.0	3.81	01:38:10.0	3.822		
01:24:40.0	3.811	01:31:30.0	3.81	01:38:20.0	3.823		
01:24:50.0	3.811	01:31:40.0	3.809	01:38:30.0	3.823		
01:25:00.0	3.811	01:31:50.0	3.81	01:38:40.0	3.824		
01:25:10.0	3.811	01:32:00.0	3.81	01:38:50.0	3.824		
01:25:20.0	3.812	01:32:10.0	3.81	01:39:00.0	3.824		
01:25:30.0	3.811	01:32:20.0	3.81	01:39:10.0	3.824		
01:25:40.0	3.811	01:32:30.0	3.81	01:39:20.0	3.824		
01:25:50.0	3.811	01:32:40.0	3.81	01:39:30.0	3.824		
01:26:00.0	3.811	01:32:50.0	3.81	01:39:40.0	3.824		
01:26:10.0	3.811	01:33:00.0	3.81	01:39:50.0	3.824		
01:26:20.0	3.811	01:33:10.0	3.811	01:40:00.0	3.823		
01:26:30.0	3.811	01:33:20.0	3.81	01:40:10.0	3.823		
01:26:40.0	3.811	01:33:30.0	3.81	01:40:20.0	3.824		
01:26:50.0	3.811	01:33:40.0	3.811	01:40:30.0	3.824		
01:27:00.0	3.811	01:33:50.0	3.811	01:40:40.0	3.824		
01:27:10.0	3.81	01:34:00.0	3.811	01:40:50.0	3.825		
01:27:20.0	3.811	01:34:10.0	3.811	01:41:00.0	3.824		
01:27:30.0	3.81	01:34:20.0	3.811	01:41:10.0	3.825		
01:27:40.0	3.81	01:34:30.0	3.811	01:41:20.0	3.826		
01:27:50.0	3.81	01:34:40.0	3.812	01:41:30.0	3.826		
01:28:00.0	3.81	01:34:50.0	3.812	01:41:40.0	3.825		
01:28:10.0	3.81	01:35:00.0	3.812	01:41:50.0	3.825		
01:28:20.0	3.81	01:35:10.0	3.813	01:42:00.0	3.825		
01:28:30.0	3.81	01:35:20.0	3.814	01:42:10.0	3.825		
01:28:40.0	3.81	01:35:30.0	3.814	01:42:20.0	3.825		

Appendix B. CO Gas Test 2 Raw Data – 10 Secs Sampling

Time	Output (V)	Time	Output (V)	Time	Output (V)	Time	Output (V)
00:00:01.0	4.177	00:06:40.0	4.178	00:13:30.0	4.177	00:20:20.0	4.176
00:00:02.0	4.177	00:06:50.0	4.178	00:13:40.0	4.177	00:20:30.0	4.175
00:00:10.0	4.177	00:07:00.0	4.178	00:13:50.0	4.177	00:20:40.0	4.175
00:00:20.0	4.177	00:07:10.0	4.178	00:14:00.0	4.177	00:20:50.0	4.175
00:00:30.0	4.177	00:07:20.0	4.178	00:14:10.0	4.177	00:21:00.0	4.176
00:00:40.0	4.177	00:07:30.0	4.178	00:14:20.0	4.177	00:21:10.0	4.176
00:00:50.0	4.176	00:07:40.0	4.177	00:14:30.0	4.177	00:21:20.0	4.176
00:01:00.0	4.177	00:07:50.0	4.178	00:14:40.0	4.177	00:21:30.0	4.175
00:01:10.0	4.176	00:08:00.0	4.177	00:14:50.0	4.177	00:21:40.0	4.175
00:01:20.0	4.177	00:08:10.0	4.178	00:15:00.0	4.177	00:21:50.0	4.176
00:01:30.0	4.177	00:08:20.0	4.178	00:15:10.0	4.177	00:22:00.0	4.175
00:01:40.0	4.177	00:08:30.0	4.178	00:15:20.0	4.177	00:22:10.0	4.175
00:01:50.0	4.177	00:08:40.0	4.177	00:15:30.0	4.177	00:22:20.0	4.175
00:02:00.0	4.177	00:08:50.0	4.177	00:15:40.0	4.177	00:22:30.0	4.175
00:02:10.0	4.177	00:09:00.0	4.178	00:15:50.0	4.177	00:22:40.0	4.175
00:02:20.0	4.177	00:09:10.0	4.178	00:16:00.0	4.177	00:22:50.0	4.175
00:02:30.0	4.177	00:09:20.0	4.178	00:16:10.0	4.177	00:23:00.0	4.175
00:02:40.0	4.178	00:09:30.0	4.178	00:16:20.0	4.177	00:23:10.0	4.174
00:02:50.0	4.177	00:09:40.0	4.177	00:16:30.0	4.177	00:23:20.0	4.175
00:03:00.0	4.177	00:09:50.0	4.177	00:16:40.0	4.177	00:23:30.0	4.175
00:03:10.0	4.178	00:10:00.0	4.178	00:16:50.0	4.176	00:23:40.0	4.175
00:03:20.0	4.177	00:10:10.0	4.178	00:17:00.0	4.177	00:23:50.0	4.175
00:03:30.0	4.178	00:10:20.0	4.177	00:17:10.0	4.177	00:24:00.0	4.175
00:03:40.0	4.177	00:10:30.0	4.177	00:17:20.0	4.177	00:24:10.0	4.175
00:03:50.0	4.178	00:10:40.0	4.177	00:17:30.0	4.177	00:24:20.0	4.175
00:04:00.0	4.177	00:10:50.0	4.177	00:17:40.0	4.176	00:24:30.0	4.175
00:04:10.0	4.178	00:11:00.0	4.178	00:17:50.0	4.177	00:24:40.0	4.175
00:04:20.0	4.178	00:11:10.0	4.178	00:18:00.0	4.177	00:24:50.0	4.175
00:04:30.0	4.177	00:11:20.0	4.178	00:18:10.0	4.177	00:25:00.0	4.175
00:04:40.0	4.177	00:11:30.0	4.177	00:18:20.0	4.176	00:25:10.0	4.175
00:04:50.0	4.178	00:11:40.0	4.177	00:18:30.0	4.177	00:25:20.0	4.174
00:05:00.0	4.178	00:11:50.0	4.177	00:18:40.0	4.176	00:25:30.0	4.175
00:05:10.0	4.178	00:12:00.0	4.177	00:18:50.0	4.176	00:25:40.0	4.174
00:05:20.0	4.178	00:12:10.0	4.178	00:19:00.0	4.176	00:25:50.0	4.174
00:05:30.0	4.178	00:12:20.0	4.177	00:19:10.0	4.176	00:26:00.0	4.174
00:05:40.0	4.177	00:12:30.0	4.177	00:19:20.0	4.176	00:26:10.0	4.175
00:05:50.0	4.178	00:12:40.0	4.177	00:19:30.0	4.176	00:26:20.0	4.174
00:06:00.0	4.178	00:12:50.0	4.177	00:19:40.0	4.176	00:26:30.0	4.174
00:06:10.0	4.178	00:13:00.0	4.177	00:19:50.0	4.175	00:26:40.0	4.174
00:06:20.0	4.178	00:13:10.0	4.177	00:20:00.0	4.176	00:26:50.0	4.174
00:06:30.0	4.178	00:13:20.0	4.177	00:20:10.0	4.176	00:27:00.0	4.174

Time	Output (V)	Time	Output (V)	Time	Output (V)	Time	Output (V)
00:27:10.0	4.174	00:34:00.0	4.173	00:40:50.0	4.171	00:47:40.0	4.169
00:27:20.0	4.173	00:34:10.0	4.173	00:41:00.0	4.17	00:47:50.0	4.169
00:27:30.0	4.174	00:34:20.0	4.172	00:41:10.0	4.171	00:48:00.0	4.17
00:27:40.0	4.174	00:34:30.0	4.173	00:41:20.0	4.171	00:48:10.0	4.17
00:27:50.0	4.173	00:34:40.0	4.172	00:41:30.0	4.171	00:48:20.0	4.17
00:28:00.0	4.174	00:34:50.0	4.172	00:41:40.0	4.17	00:48:30.0	4.17
00:28:10.0	4.173	00:35:00.0	4.172	00:41:50.0	4.17	00:48:40.0	4.169
00:28:20.0	4.174	00:35:10.0	4.173	00:42:00.0	4.171	00:48:50.0	4.169
00:28:30.0	4.174	00:35:20.0	4.172	00:42:10.0	4.171	00:49:00.0	4.169
00:28:40.0	4.174	00:35:30.0	4.172	00:42:20.0	4.17	00:49:10.0	4.169
00:28:50.0	4.174	00:35:40.0	4.172	00:42:30.0	4.171	00:49:20.0	4.17
00:29:00.0	4.174	00:35:50.0	4.172	00:42:40.0	4.17	00:49:30.0	4.169
00:29:10.0	4.174	00:36:00.0	4.172	00:42:50.0	4.171	00:49:40.0	4.169
00:29:20.0	4.174	00:36:10.0	4.172	00:43:00.0	4.171	00:49:50.0	4.169
00:29:30.0	4.174	00:36:20.0	4.172	00:43:10.0	4.17	00:50:00.0	4.169
00:29:40.0	4.174	00:36:30.0	4.172	00:43:20.0	4.171	00:50:10.0	4.169
00:29:50.0	4.173	00:36:40.0	4.172	00:43:30.0	4.171	00:50:20.0	4.169
00:30:00.0	4.174	00:36:50.0	4.172	00:43:40.0	4.17	00:50:30.0	4.169
00:30:10.0	4.173	00:37:00.0	4.172	00:43:50.0	4.17	00:50:40.0	4.169
00:30:20.0	4.173	00:37:10.0	4.172	00:44:00.0	4.17	00:50:50.0	4.169
00:30:30.0	4.173	00:37:20.0	4.172	00:44:10.0	4.17	00:51:00.0	4.169
00:30:40.0	4.173	00:37:30.0	4.172	00:44:20.0	4.17	00:51:10.0	4.169
00:30:50.0	4.173	00:37:40.0	4.172	00:44:30.0	4.17	00:51:20.0	4.169
00:31:00.0	4.173	00:37:50.0	4.172	00:44:40.0	4.17	00:51:30.0	4.169
00:31:10.0	4.174	00:38:00.0	4.172	00:44:50.0	4.17	00:51:40.0	4.169
00:31:20.0	4.173	00:38:10.0	4.171	00:45:00.0	4.17	00:51:50.0	4.169
00:31:30.0	4.173	00:38:20.0	4.171	00:45:10.0	4.17	00:52:00.0	4.169
00:31:40.0	4.173	00:38:30.0	4.171	00:45:20.0	4.17	00:52:10.0	4.169
00:31:50.0	4.173	00:38:40.0	4.172	00:45:30.0	4.17	00:52:20.0	4.169
00:32:00.0	4.173	00:38:50.0	4.172	00:45:40.0	4.17	00:52:30.0	4.169
00:32:10.0	4.173	00:39:00.0	4.171	00:45:50.0	4.17	00:52:40.0	4.169
00:32:20.0	4.173	00:39:10.0	4.171	00:46:00.0	4.17	00:52:50.0	4.169
00:32:30.0	4.173	00:39:20.0	4.171	00:46:10.0	4.17	00:53:00.0	4.169
00:32:40.0	4.174	00:39:30.0	4.172	00:46:20.0	4.169	00:53:10.0	4.169
00:32:50.0	4.173	00:39:40.0	4.171	00:46:30.0	4.17	00:53:20.0	4.169
00:33:00.0	4.173	00:39:50.0	4.171	00:46:40.0	4.17	00:53:30.0	4.169
00:33:10.0	4.173	00:40:00.0	4.172	00:46:50.0	4.17	00:53:40.0	4.169
00:33:20.0	4.173	00:40:10.0	4.172	00:47:00.0	4.17	00:53:50.0	4.169
00:33:30.0	4.173	00:40:20.0	4.172	00:47:10.0	4.169	00:54:00.0	4.169
00:33:40.0	4.173	00:40:30.0	4.171	00:47:20.0	4.169	00:54:10.0	4.169
00:33:50.0	4.173	00:40:40.0	4.171	00:47:30.0	4.17	00:54:20.0	4.169

Time	Output (V)	Time	Output (V)	Time	Output (V)	Time	Output (V)
00:54:30.0	4.168	01:01:20.0	4.168	01:08:10.0	4.167	01:15:00.0	4.167
00:54:40.0	4.169	01:01:30.0	4.168	01:08:20.0	4.166	01:15:10.0	4.167
00:54:50.0	4.168	01:01:40.0	4.167	01:08:30.0	4.166	01:15:20.0	4.167
00:55:00.0	4.169	01:01:50.0	4.168	01:08:40.0	4.167	01:15:30.0	4.167
00:55:10.0	4.169	01:02:00.0	4.168	01:08:50.0	4.166	01:15:40.0	4.167
00:55:20.0	4.168	01:02:10.0	4.168	01:09:00.0	4.166	01:15:50.0	4.167
00:55:30.0	4.169	01:02:20.0	4.168	01:09:10.0	4.166	01:16:00.0	4.167
00:55:40.0	4.169	01:02:30.0	4.168	01:09:20.0	4.166	01:16:10.0	4.167
00:55:50.0	4.169	01:02:40.0	4.168	01:09:30.0	4.166	01:16:20.0	4.167
00:56:00.0	4.169	01:02:50.0	4.168	01:09:40.0	4.166	01:16:30.0	4.167
00:56:10.0	4.168	01:03:00.0	4.167	01:09:50.0	4.166	01:16:40.0	4.167
00:56:20.0	4.169	01:03:10.0	4.167	01:10:00.0	4.166	01:16:50.0	4.167
00:56:30.0	4.168	01:03:20.0	4.167	01:10:10.0	4.166	01:17:00.0	4.167
00:56:40.0	4.168	01:03:30.0	4.167	01:10:20.0	4.166	01:17:10.0	4.167
00:56:50.0	4.169	01:03:40.0	4.167	01:10:30.0	4.166	01:17:20.0	4.167
00:57:00.0	4.168	01:03:50.0	4.167	01:10:40.0	4.167	01:17:30.0	4.167
00:57:10.0	4.168	01:04:00.0	4.167	01:10:50.0	4.167	01:17:40.0	4.167
00:57:20.0	4.168	01:04:10.0	4.167	01:11:00.0	4.167	01:17:50.0	4.168
00:57:30.0	4.168	01:04:20.0	4.167	01:11:10.0	4.167	01:18:00.0	4.168
00:57:40.0	4.168	01:04:30.0	4.167	01:11:20.0	4.167	01:18:10.0	4.168
00:57:50.0	4.168	01:04:40.0	4.167	01:11:30.0	4.167	01:18:20.0	4.168
00:58:00.0	4.168	01:04:50.0	4.167	01:11:40.0	4.167	01:18:30.0	4.168
00:58:10.0	4.168	01:05:00.0	4.167	01:11:50.0	4.167	01:18:40.0	4.169
00:58:20.0	4.169	01:05:10.0	4.167	01:12:00.0	4.167	01:18:50.0	4.169
00:58:30.0	4.168	01:05:20.0	4.167	01:12:10.0	4.167	01:19:00.0	4.168
00:58:40.0	4.168	01:05:30.0	4.167	01:12:20.0	4.166	01:19:10.0	4.169
00:58:50.0	4.168	01:05:40.0	4.167	01:12:30.0	4.167	01:19:20.0	4.169
00:59:00.0	4.168	01:05:50.0	4.167	01:12:40.0	4.167	01:19:30.0	4.169
00:59:10.0	4.168	01:06:00.0	4.166	01:12:50.0	4.167	01:19:40.0	4.169
00:59:20.0	4.168	01:06:10.0	4.167	01:13:00.0	4.167	01:19:50.0	4.17
00:59:30.0	4.168	01:06:20.0	4.166	01:13:10.0	4.167	01:20:00.0	4.169
00:59:40.0	4.168	01:06:30.0	4.166	01:13:20.0	4.167	01:20:10.0	4.17
00:59:50.0	4.168	01:06:40.0	4.167	01:13:30.0	4.167	01:20:20.0	4.17
01:00:00.0	4.168	01:06:50.0	4.167	01:13:40.0	4.167	01:20:30.0	4.17
01:00:10.0	4.168	01:07:00.0	4.167	01:13:50.0	4.167	01:20:40.0	4.17
01:00:20.0	4.168	01:07:10.0	4.167	01:14:00.0	4.167	01:20:50.0	4.17
01:00:30.0	4.168	01:07:20.0	4.167	01:14:10.0	4.167	01:21:00.0	4.17
01:00:40.0	4.168	01:07:30.0	4.167	01:14:20.0	4.167	01:21:10.0	4.171
01:00:50.0	4.168	01:07:40.0	4.167	01:14:30.0	4.167	01:21:20.0	4.171
01:01:00.0	4.168	01:07:50.0	4.166	01:14:40.0	4.167	01:21:30.0	4.171
01:01:10.0	4.168	01:08:00.0	4.166	01:14:50.0	4.167	01:21:40.0	4.171

Time	Output (V)	Time	Output (V)
01:21:50.0	4.171	01:28:40.0	4.175
01:22:00.0	4.171	01:28:50.0	4.175
01:22:10.0	4.171	01:29:00.0	4.175
01:22:20.0	4.171	01:29:10.0	4.176
01:22:30.0	4.171	01:29:20.0	4.176
01:22:40.0	4.171	01:29:30.0	4.177
01:22:50.0	4.171	01:29:40.0	4.176
01:23:00.0	4.171	01:29:50.0	4.176
01:23:10.0	4.172	01:30:00.0	4.176
01:23:20.0	4.172	01:30:10.0	4.176
01:23:30.0	4.172	01:30:20.0	4.176
01:23:40.0	4.172	01:30:30.0	4.176
01:23:50.0	4.172	01:30:40.0	4.176
01:24:00.0	4.172	01:30:50.0	4.176
01:24:10.0	4.172	01:31:00.0	4.176
01:24:20.0	4.172	01:31:10.0	4.176
01:24:30.0	4.173	01:31:20.0	4.176
01:24:40.0	4.173	01:31:30.0	4.176
01:24:50.0	4.173	01:31:40.0	4.176
01:25:00.0	4.173	01:31:50.0	4.176
01:25:10.0	4.173	01:32:00.0	4.176
01:25:20.0	4.173	01:32:10.0	4.176
01:25:30.0	4.173	01:32:20.0	4.177
01:25:40.0	4.173	01:32:30.0	4.176
01:25:50.0	4.173	01:32:40.0	4.176
01:26:00.0	4.173	01:32:50.0	4.176
01:26:10.0	4.173		
01:26:20.0	4.174		
01:26:30.0	4.174		
01:26:40.0	4.174		
01:26:50.0	4.174		
01:27:00.0	4.174		
01:27:10.0	4.174		
01:27:20.0	4.174		
01:27:30.0	4.174		
01:27:40.0	4.175		
01:27:50.0	4.174		
01:28:00.0	4.175		
01:28:10.0	4.174		
01:28:20.0	4.175		
01:28:30.0	4.175		