Silver Metallization for
ULSI Circuit Interconnect Applications

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a	Best fit constant in time to failure model
A	Material A
A_1	Cross-sectional area of conductor of resistivity, ρ_1
A_2	Cross-sectional area of conductor of resistivity, ρ_2
A_b	cross-sectional area of barrier
A_{pc}	cross-sectional area of primary conductor
b	Best fit constant in time to failure model
B	Material B
C	Spatial concentration of species in medium
C	Arbitrary constant for electromigration median time to failure
C	Pre-exponential constant in time to failure equation
C_0	Initial concentration at time t = 0
C_{Al}	Aluminum concentration
C_{sol}	Concentration of diffusing species in host material at the solid solubility limit
D	Diffusivity
D_0	Pre-exponential term in diffusivity equation
E	Electric field
E_a	Activation energy for electromigration
E_a	Activation energy of diffusion
f	Function
h	Barrier thickness
I	Current
J	Flux of diffusing species
k	Boltzmann constant

K	Impurity resistivity constant for the solute element in the host lattice
K_{Al}	Impurity resistivity constant for Al in Ag
l	Stack thickness
M	Constant (total amount of impurity)
M_A	Total amount of barrier material available
M_d	Amount of material diffused into host
n	exponent parameter for electromigration
N	Number of layers in composite structure
q	Electron charge
Q	Field dependent diffusion activation energy
Q_0	Zero-field diffusion activation energy
R_1	Resistance at temperature T_1
R_2	Resistance at temperature T_2
R_s	Sheet resistance
R_T	Resistance at temperature T
S	linear scaling factor for device dimensions
s	width of conducting line
S_{AB}	Solid solubility of material A in material B in atomic percent
T	Temperature
t	Time
t	thickness of barrier
T_0	Temperature offset term in time to failure model
T_1	Temperature of conductor of resistance R_1
T_2	Temperature of conductor of resistance R_2
t_i	Individual layer thickness
V	Voltage
x	Distance from origin
x_d	Thickness of individual layer in composite structure
α	Best fit constant in time to failure model (field activation energy term)
α	Constant in exponential term for Shottky conduction mechanism

β	Constant in exponential term for tunneling conduction mechanism
Δx	Infinitesimal thickness of individual layer in composite structure
δ	Constant in exponential term for Poole-Frenkel conduction mechanism
λ	Lagrangian multiplier
μ	Mobility
ρ_0	Resistivity term
ρ_1	Resistivity of conductor of cross-sectional area A_1
ρ_2	Resistivity of conductor of cross-sectional area A_2
ρ_{Al}	Al impurity resistivity in silver
ρ_{Al}	Al resistivity
ρ_b	Resistivity of barrier
ρ_{eff}	Effective resistivity of composite structure
ρ_i	Individual layer resistivity
ρ_i	Temperature independent resistivity term
ρ_j	Resistivity of j^{th} layer
ρ_{pc}	Resistivity of primary conductor
ρ_{TiAl_3}	Resistivity of $TiAl_3$
ρ_{temp}	Temperature dependent resistivity term
P_A	Atomic density of material A
P_B	Atomic density of material B

List of Acronyms

ALE	Atomic Layer Epitaxy
BPSG	Borophosphosilicate Glass
BTS	Bias Thermal Stress
CMP	Chemical Mechanical Polishing
CVD	Chemical Vapor Deposition
DC	Direct Current
DMAH	Di-Methyl Aluminum Hydride
EM	Electromigration
FIB	Focused Ion Beam
IEEE	Institute of Electrical and Electronic Engineers
IMD	Inter Metal Dielectric
MLM	Multi Level Metallization
MOS	Metal Oxide Silicon
MRC	Materials Research Corporation
MTTF	Median Time To Failure
NIST	National Institute of Standards and Technology
PACVD	Plasma Assisted Chemical Vapor Deposition
PSG	Phosphosilicate Glass
PTEOS	Plasma (Enhanced) Tetra Ethyl Ortho Silicate
PVD	Physical Vapor Deposition
QMS	Quadrapole Mass Spectrometer
RBS	Rutherford Back Scattering
RC	Resistance-Capacitance
SCL	Space Charge Limited
SEM	Scanning Electron Microscope
SIA	Semiconductor Industry Association

SIMS	Secondary Ion Mass Spectroscopy
TCR	Temperature Co-efficient of Resistance
TEOS	Tetra Ethyl Ortho Silicate
TIBA	Tri-Isobutyl Aluminum
TTF	Time To Failure
UHV	Ultra High Vacuum
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration

ABSTRACT

Silver Metallization for ULSI Circuit Interconnect Applications

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As device dimensions continue to shrink into the deep sub-micron regime, the performance and reliability limitations for ultra-large scale integration (ULSI) circuits are increasingly being determined by the interconnect technology. Ag has the potential to provide superior performance and reliability over Al-based interconnect technology.

This body of work explored the feasibility of using Ag as an interconnect for deep sub-micron integrated circuits. It was determined that both Ag-based MOS structures fail under bias thermal stress, and the field and temperature dependence of the time to failure were explored. This implied a need for an effective diffusion barrier between Ag and the inter-metal dielectric in order to prevent shorting of adjacent metal lines. Of the diffusion barriers that were studied, Ta gave the best performance.

The interaction of Ag with other commonly used metallization materials was considered. It was found that Ag could be incorporated with a Ti, TiW or TiN barrier layer without any negative impact on its properties. However, Al diffused readily into Ag thus affecting the Ag resistivity. Therefore, Ag could not be used in immediate proximity to Al. A model of the Ag resistivity that considered the diffusivity of Al in Ag and the

impurity resistivity of Al in Ag was used to predict the resistivity of the Ag-Al stacks. This prediction gave good agreement with the experimental data. The adhesion of Ag to TiN, Ti, Ta and TiW was found to be adequate.

Physical vapor deposition (PVD), reflow and mechanical polishing were used to create half micron wide Ag lines in oxide. The effective resistivity was compared to that of a comparable damascene Al-based structure and proved to be considerably superior. The results showed that Ag is a promising interconnect alternative to Al.

Chapter 1
INTRODUCTION

1.1 Motivation

As device dimensions continue to shrink into the deep sub-micron regime, the performance and reliability limitations for ultra-large scale integrated (ULSI) circuits are increasingly being determined by the interconnect technology [1-3]. As the interconnect line cross-section decreases, the current density increases, placing more rigorous demands on electromigration performance. Device speed is limited by the RC constant of the metal interconnect line, where R is the metal line resistance and C is the capacitance of the surrounding dielectric medium. ULSI circuit reliability and performance are therefore inherently limited by two key intrinsic physical properties of the interconnect metal; electromigration resistance and bulk resistivity. Both Cu and Ag have significantly lower bulk resistivity than Al-Cu [4], and their electromigration performance is expected to be superior [5-6] to that of Al-Cu. Cu metallization has received considerable attention recently [7-8] and is expected by many to be the metallization choice to replace Al-Cu in future multilevel metallization (MLM) technology. However, unlike Ag, Cu does not form a self-passivating oxide. This presents a serious reliability concern for Cu-based metallization. Ag has received less interest, although its bulk resistivity is slightly lower than that of Cu at room temperature, and significantly lower at a nominal device operating temperature of 100 °C. This lack of interest is in part due to the reported tendency of Ag to agglomerate when annealed in a room ambient [9-11], and its poor electromigration performance in unpassivated lines [12-13]. This lack of interest may also be partly due to

the fact that the conservative nature of the semiconductor industry dictates the selection of materials for which there is already a considerable wealth of knowledge. Since Cu metallization has been more extensively researched than Ag metallization, the interest in Cu metallization is self-perpetuating. Recent work in Ag metallization however indicates that the agglomeration problem can be overcome by using a Ti self-passivation technique [14-15], or by refractory metal encapsulation [16]. The poor electromigration performance in unpassivated lines may not be relevant to a silver metallization scheme that employs encapsulated lines. Ag metallization may therefore be a promising candidate to replace Al, provided the significant processing challenges can be overcome.

1.2 Future Trends in ULSI Circuits

1.2.1 Scaling Trend in ULSI Circuits

Thirty years ago, Intel Chairperson Gordon Moore predicted in what has come to be known as Moore's Law, that the power and complexity of the silicon chip would double every year with proportionate decreases in cost [17]. This proved to be correct, although in recent years it has slowed to every 18 months. The corollary of Moore's Law to device dimensions implies that minimum device dimensions will shrink by 30% every 3 years. The Semiconductor Industry Association's recent technology roadmap for device dimensions is outlined in Table 1.1.

Table 1.1 Semiconductor Industry Association's technology roadmap

Year	1992	1995	1998	2001	2004	2007
Feature Size (μm)	0.5	0.35	0.25	0.18	0.12	0.10

Not only does the scaling of minimum device dimensions result in increased device density on the chip, but increased computational power demands an increase in the complexity of the interconnectivity of the devices. The degree of interconnectivity is known as the functionality. The increased functionality can only be accommodated (without using prime device area) by employing multiple interconnect levels. It is projected that up to 7 interconnect metal levels will be needed to connect devices of 0.12μm dimension within 10 years [18].

1.2.2 Al Deposition Methods for Sub Half Micron Technology

Al lines can be realized by either pattern etching or damascene. For the former, blanket Al deposition is followed by etching to define the lines. Subsequently oxide deposition fills the gaps between the patterned lines. In the case of damascene, the oxide layer is deposited and then etched to yield trenches, and the Al is deposited into the trenches. Subsequent chemical mechanical polishing (CMP) removes the excess Al, leaving behind the defined lines. (Vias however are always made by etching into the oxide and they are subsequently filled with metal, usually either W or Al.) The two approaches are outlined in Figure 1.1 and Figure 1.2. For either method of defining the lines, an appropriate deposition method (and reflow if necessary) must be selected. There is some interest in chemical vapor deposition (CVD) of Al using dimethyl-aluminum-hydride (DMAH), tri-isobutyl-aluminum (TIBA), or other precursors. There has also been some interest in high pressure filling to complement moderate temperature Al sputter deposition. In this technique the Al voids that result from partial filling of trenches and vias are essentially crushed under an Ar pressure of 60 MPa. In both the CVD and high pressure filling techniques, Al is typically deposited onto TiN. A third option is to deposit Al at high temperatures (around 400 °C) sequentially onto Ti. This method could be used for either a patterned Al line technique, or Al damascene. The Al can fill high aspect ration vias (and trenches) as deposited by this method without requiring an additional thermal process step for reflow. During deposition (or during a subsequent anneal step) the Al reacts with the Ti to form the compound $TiAl_3$ that consumes a significant portion of the

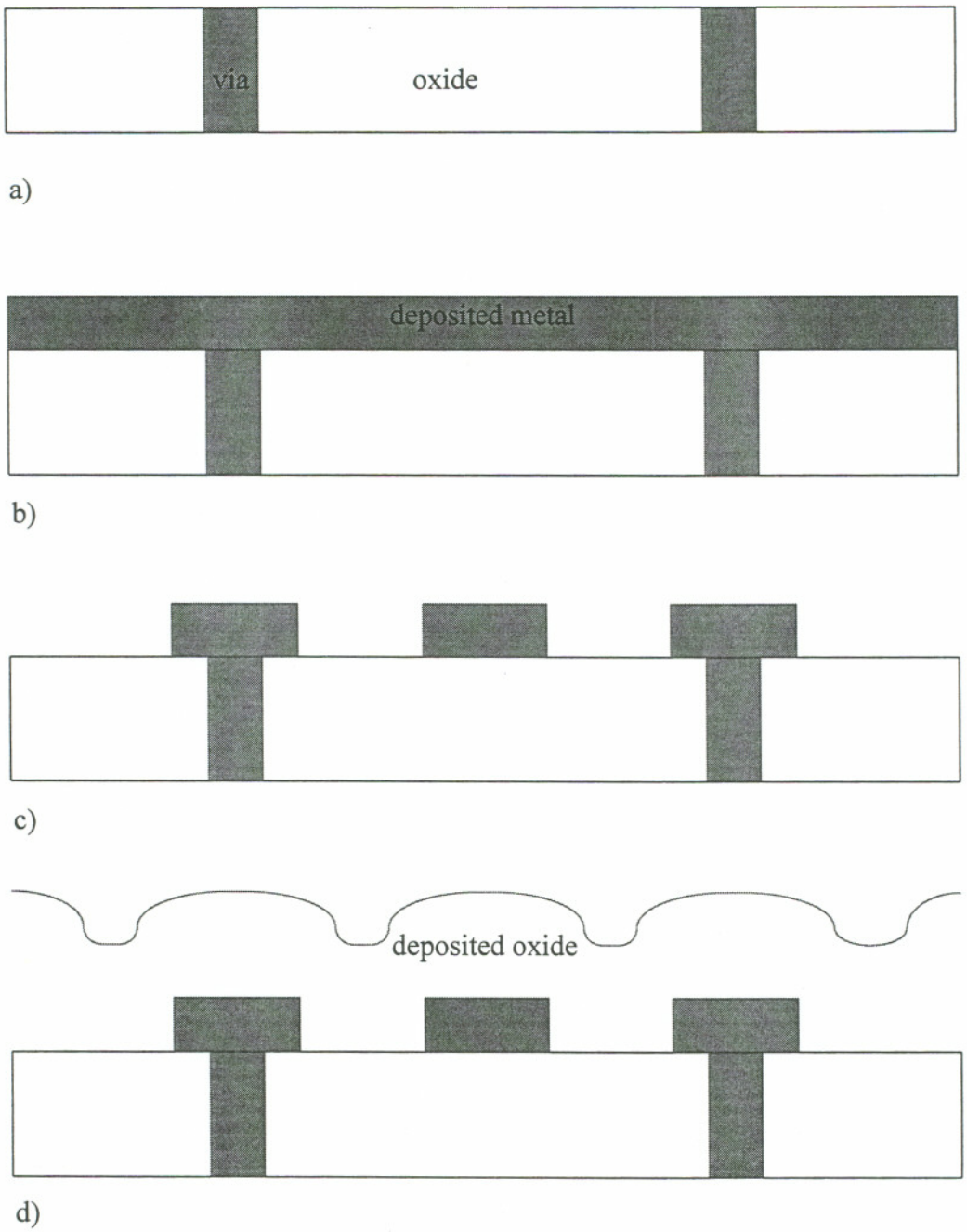


Figure 1.1 Steps for Al line realization. (a) vias are etched into oxide then filled with either W or Al, (b) blanket Al deposition, (c) Al is etched to form metal lines, (d) oxide deposition

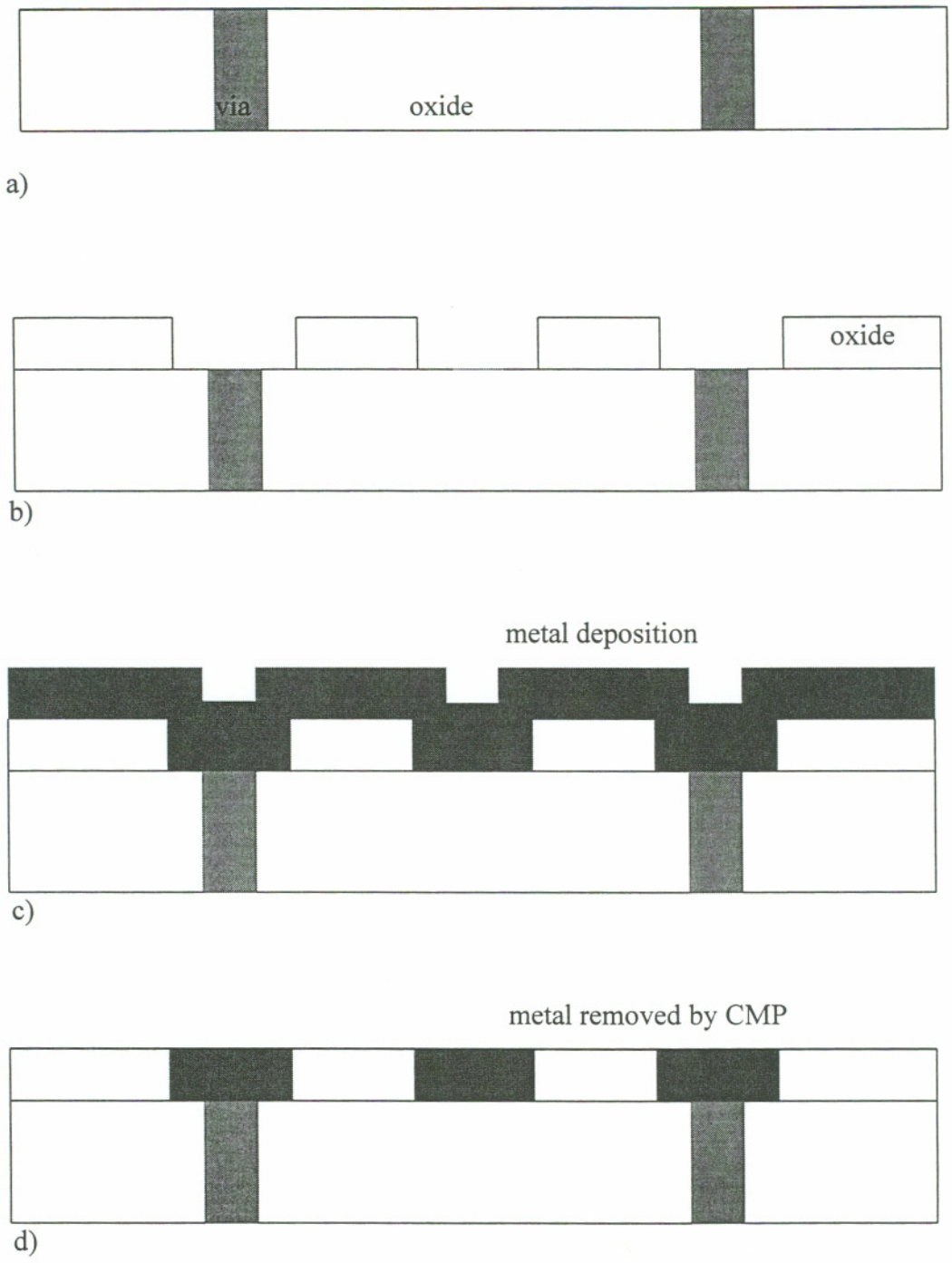


Figure 1.2 Steps for Al line realization. (a) vias are etched into oxide then filled with either W or Al, (b) oxide deposition and patterning, (c) Al deposition, (d) excess Al removed by CMP

interconnect cross-sectional area. However, the electromigration performance of the stack is much improved. This is because the $TiAl_3$ provides an alternative conduction path if the Al-Cu fails locally due to electromigration. Serious safety issues would be likely to retard the introduction of CVD Al, even if the associated contamination issues could be overcome. The high pressure filling technique requires a deposition temperature that is not sufficiently lower than that of the high temperature Al reflow technique to justify the additional process complexity. Therefore, of these three aforementioned techniques for depositing Al the higher temperature Al deposition is the one most expected to be introduced into manufacturing. There is some ambiguity as to whether this deposition technique will be used in conjunction with an Al line patterning process or a damascene process.

1.2.3 Impact of Scaling on Reliability, Electromigration Lifetime

The scaling of the metal lines has an immediate and obvious impact on both device performance and reliability. A major reliability issue is electromigration. As device dimensions are scaled by a linear scaling factor S, individual device operating voltages are generally scaled by a factor of $1/S^n$ where n has a value between 0 and 1. The product of the scaled device dimensions and the scaling factor S is equal to the original device dimensions. From the work of Donald S. Gardner et al. [2], the effect of voltage scaling on source-drain current is given in Table 1.2.

Table 1.2 Effect of Voltage Scaling on Source-Drain Current

Voltage Scaling	Transistor Current Scaling	Current Density Scaling
1	S	S^3
$1/S^{1/2}$	1	S^2
1/S	1/S	S

It can readily be seen from Table 1.2, that unless operating voltages are scaled by a factor of $1/S^{1/2}$ or greater, transistor current and therefore interconnect current, will increase. Let us assume that the transistor current remains constant with device scaling. The cross-sectional area of the interconnect lines is reduced with device scaling. Unless aspect ratios are increased, which presents processing challenges, the current density increase is proportional to the square of the interconnect scaling. Median failure times due to electromigration are generally described by Black's equation, Eqn. 1.1:

$$\mathrm{MTTF} = CJ^{n} \exp \frac{E_a}{kT} \qquad \text{Eqn. 1.1}$$

where MTTF is the median failure time, C is a constant, J is the current density, n is the exponent parameter, (which ranges from n = -1 to n = -6), E_a is the activation energy, k is the Boltzmann constant, and T is the temperature in degrees Kelvin. For electromigration in Al-based metallization, it is considered appropriate to set the exponent parameter, n, to the integer value of -2 [20-21]. It is therefore reasonable to suggest that interconnect lifetime could be affected by the fourth power of the device scaling, S, due to electromigration failure.

1.2.4 Impact of Scaling on Performance, RC delay

One aspect of device performance is the operating speed. Operating speed is limited by the RC time constant, where R is the effective resistance and C is the effective capacitance and the intrinsic gate delay. For larger dimensions, i.e. above 1μm, intrinsic gate delay is the dominant contributor to the total speed of the device. As device dimensions are scaled, the intrinsic gate delay decreases and interconnect RC delay increases. Below 0.5 μm, the device speed is almost completely limited by the interconnect RC delay [22]. The interconnect capacitance is comprised of two components, namely line to line capacitance and interlayer capacitance. For pitch below

0.5 μm, line to line capacitance dominates interlayer capacitance. What this implies, is that for deep sub-micron regime, the interconnect line resistance and the line to line capacitance are the most significant factors in the performance of the circuit.

1.2.5 Solution to Reliability Issues

If electromigration is considered to be the key reliability issue associated with scaling, then an obvious solution to the electromigration problem is to use an interconnect material of superior electromigration performance. However, the selection of materials is constrained by resistivity. The electromigration performance of Al based metallization has been greatly enhanced by the addition of small amounts (0.5% - 2%) of Cu. Although this adversely affects the resistivity, the electromigration performance is sufficiently superior to justify its use. Considerable work in the area of electromigration has shown that factors such as deposition parameters can influence electromigration performance. Electromigration performance of Al has been enhanced by stringent control of properties such as grain size and residual stress. The electromigration performance of Ag however is expected to be much better than that of Al-Cu, based on simple melting point arguments [6].

1.2.6 Solution to Performance Issues

Interconnect RC can be reduced by lowering C or R. C can be reduced by using a low-k dielectric in place of SiO_2. Considerable research efforts are being made in this area with materials such as polyimide [23] and parylene. C can also be lowered by increasing the line spacing, but this is counter to the thrust of increasing device density. Alternatively, one can lower the line resistance, R. Interconnect line resistance is directly proportional to the length of the interconnect line and inversely proportional to the cross-sectional area. The constant of proportionality is the bulk property called resistivity, ρ. To some extent, the interconnect length can be reduced, therefore lowering the line resistance, R, by increasing the number of metal levels, and by clever spatial design. However, this results in an increased complexity that cannot necessarily be justified by the

performance gain for each proposed additional level. Line resistance can also be reduced by increasing the cross-sectional area. However, linewidth must be reduced with scaling, and unless the aspect ratio is increased, height must also be reduced. The only remaining option is to select a metal that has a lower resistivity than that of Al-Cu. Since the resistivity difference between Au and Al-Cu is relatively small, Cu and Ag are the only serious metallization alternatives to Al-Cu. However, the effective resistivity of the metal stack, rather than simply the bulk resistivity, must be considered when comparing metallization options. This is described in the following section.

1.2.7 Effective Resistivity of a metal stack, comparison of Ag and Al

Since the adhesion of Ag and Cu to silicon dioxide is poor, and both are reported to diffuse into silicon dioxide under bias thermal stress, Ag-based and Cu-based metallization schemes would incorporate some combination of adhesion, wetting, and barrier layers that would require some of the cross-sectional area designated for the conducting metal interconnect line. Similarly, Al-Cu metallization schemes typically use a combination of Ti wetting and TiN barrier layers thereby reducing the cross-sectional area of the conducting Al-Cu, and increasing the line resistance. In comparing alternative metallization schemes in the sub-micron regime, it is not sufficient to consider the resistivity of the primary conducting metal alone, since the adhesion, wetting, and barrier layers consume an increasingly significant proportion of the cross-sectional area. It is useful therefore to consider the effective resistivity of the metal stack. The effective resistivity of an interconnect structure can be calculated using:

$$\rho_{\text{eff}} = t\left(\sum_{i=1}^{N}\frac{t_i}{\rho_i}\right)^{-1} \qquad \text{Eqn. 1.2}$$

where ρ_{eff} and t are the effective interconnect resistivity and thickness of the complete interconnect structure, and t_i and ρ_i are the thickness and resistivity of each of the N layers

within the interconnection. This is analogous to the effective resistance of resistors in parallel. As mentioned earlier, it is expected that Al-Cu interconnect technology will incorporate a Ti wetting layer that will be reacted with the Al to form $TiAl_3$. The $TiAl_3$ will consume a considerable portion of the interconnect cross sectional area, thus lowering the effective resistivity of the interconnect line. Assuming the thickness of the Ti wetting layer is held constant, the effective resistivity of this stack will increase with decreasing linewidth and thickness, as the proportion of Al in the interconnect line becomes smaller. Similarly for Ag metallization, which may for example use Ta as a diffusion and wetting layer, the effective resistivity will increase with decreasing linewidth. Ta might be used in a Ag metallization scheme as a necessary diffusion barrier, to prevent the diffusion of Ag into SiO_2 [24]. The effective metal line resistivity of any metallization scheme therefore depends not only on the bulk resistivity of the conducting metal, but also on the bulk resistivity of any adhesion, wetting or barrier layers and their relative volumetric proportions. It should also be noted that as dimensions shrink below one tenth of a micron, the line width becomes comparable to the mean free path of the electrons and therefore the bulk properties of the conducting metal are no longer appropriate in determining the line resistance. The conduction becomes increasingly a surface conduction phenomenon, with the properties of the interfaces becoming more important. Considering that the mean free path of the electron in Ag is approximately 0.05 μm at room temperature [25], this effect can be ignored in the 0.5 μm to 0.18 μm regime. A graph of effective resistivity vs. linewidth for $Ti/TiAl_3/Al$-Cu, Ta/Ag, and Ta/Cu metal stacks, with the wetting, adhesion, diffusion barrier thickness being held constant, is given in Figure 1.5. This was derived in Appendix 1, assuming a Ti layer of 200 Å being used on three sides for the Al-Cu stack (an Al-Cu damascene technique rather than a patterned line technique was assumed). The $TiAl_3$ layer was assumed to be 3 times the cross-sectional area of the deposited Ti. A 40 nm Ta barrier on three sides was assumed for the Cu and Ag. A one to one aspect ratio was assumed. As can be readily seen from Figure 1.3, a significant resistivity gain might be realized by employing a Ag metallization scheme as an alternative to Al-Cu. Based on the room temperature resistivity of both Ag and Cu,

there is only a small difference in effective resistivity between the two metals. However, due to the difference in temperature coefficient of resistance, a Ag-based metal stack has a significantly lower effective resistivity than the Cu-based metal stack at a nominal device temperature of 100 °C. Effective resistivity at 100 °C vs. linewidth is shown in Figure 1.4.

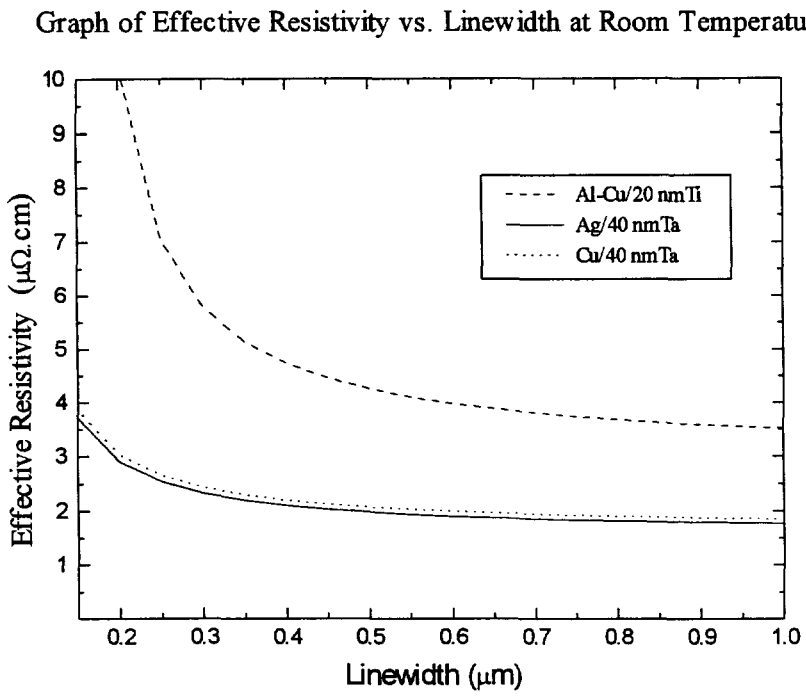


Figure 1.3 Graph of effective line resistivity at room temperature vs. linewidth for Al-Cu with 200 Å Ti wetting layer, Cu with 40 nm Ta diffusion barrier, and Ag with 40 nm Ta diffusion barrier

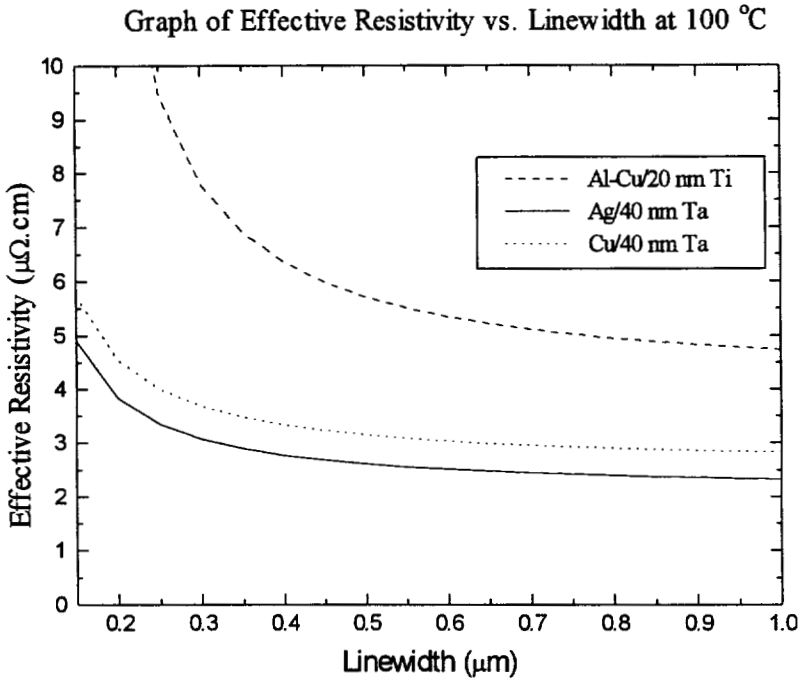


Figure 1.4 Graph of effective line resistivity at 100 °C vs. linewidth for Al-Cu with 200 Å Ti wetting layer, Cu with 40 nm Ta diffusion barrier, and Ag with 40 nm Ta diffusion barrier

1.3 Requirements of an Interconnect Metallization

The applicability of any metallization scheme to ULSI circuits depends on several properties that are outlined in Table 1.3.

Table 1.3 Desirable properties of an interconnect metallization scheme

1.	Low resistivity.
2.	Amenable to a manufacturable deposition process.
3.	Easy to pattern.
4.	Resistant to electromigration failure.
5.	Chemically stable with surrounding materials under normal operating conditions and during thermal processing steps.
6.	Mechanically stable with good adhesion and low stress.
7.	Stable with surroundings during operating lifetime.
8.	Highly resistant to corrosion.

Low resistivity and high electromigration resistance are of course the key performance and reliability metrics. However, if a metallization scheme lacks any of these eight properties, its implementation will be impeded. Physical vapor deposition (PVD) using Ar sputtering is generally favored over chemical vapor deposition (CVD), which is considered to be more costly and more hazardous. PVD is also favored over electroless deposition, which is associated with contamination and impurity issues. Poor step coverage and incomplete via and trench filling are serious concerns with PVD. Via and trench filling is improved by annealing. This process step is called reflow. For a metallization scheme to have a manufacturable deposition process, the metal must reflow to a sufficient extent as to completely fill all of the trenches and vias at temperatures below 500 °C, due to thermal

budget constraints. This problem is compounded by the increasing number of thermal cycles required as a result of additional metal levels. For integration with low-k materials, maximum anneal temperatures must be kept below 450 °C. Al metal lines can be defined by either patterning or damascene as outlined in section 1.2.2. However, for both Ag and Cu, dry-etching is generally considered very difficult, and a damascene approach is the only realistic option.

Chemical corrosion of the interconnect is a major concern. Cu oxidizes readily, and unlike that of Ag, its oxide is not self-passivating. Ag is known to corrode in the presence of Cl and S [26]. Passivation of the metal lines must therefore be used to protect the metal from the atmospheric species that contribute to the degradation of the metal.

1.4 Dissertation Overview

This thesis is divided into six chapters including this introduction. Chapter 2 contains details about the experimental apparatus used for the deposition of metals and dielectrics, the polishing equipment and procedures, and the UHV annealing chamber. In Chapter 3 reliability issues are addressed: the diffusion of Ag and Cu through oxide is presented and the electromigration data is given. Chapter 4 addresses the physical vapor deposition of Ag, the realization of a Ag interconnect line and the comparison of the effective resistivity of a Ag damascene line with an Al-Cu damascene line. Chapter 5 addresses the diffusion barrier selection and its associated integration issues. Chapter 6 contains conclusions and recommendations for future work.

Chapter 2

Experimental Details

2.1 Ultra High Vacuum (UHV) System

Samples for experiments outlined in Chapter 5, section 5.2 were annealed in a UHV system as described in this section.

2.1.1 UHV Chamber and Equipment

Thermal annealing experiments were carried out in an ultra high vacuum system. The system evolved from a Perkin-Elmer PHI Model 545 Scanning Auger Microprobe. Several additions were made to the base system. These additions include a UTI 100C quadrapole mass spectrometer (QMS), a custom built sample holder and feed through manipulator, and a sample heater. The sample manipulator was used to rotate the samples between the load lock entry position, the Auger optics axis, the QMS entrance slit and the Ar sputter gun. The sample manipulator had translational movement capability also. However, the system was arranged so that the sample could be easily rotated between the load lock entry position and the desired locations inside the chamber. The sample holder consisted of a boron nitride ceramic block, a Union Carbide 12 Ω thin film heating element and a thin pyrolytic graphite sheet which was used to evenly distribute the heat across the sample. The system layout is shown in Figure 2.1. A review of vacuum technology is given by John F. O' Hanlon [27].

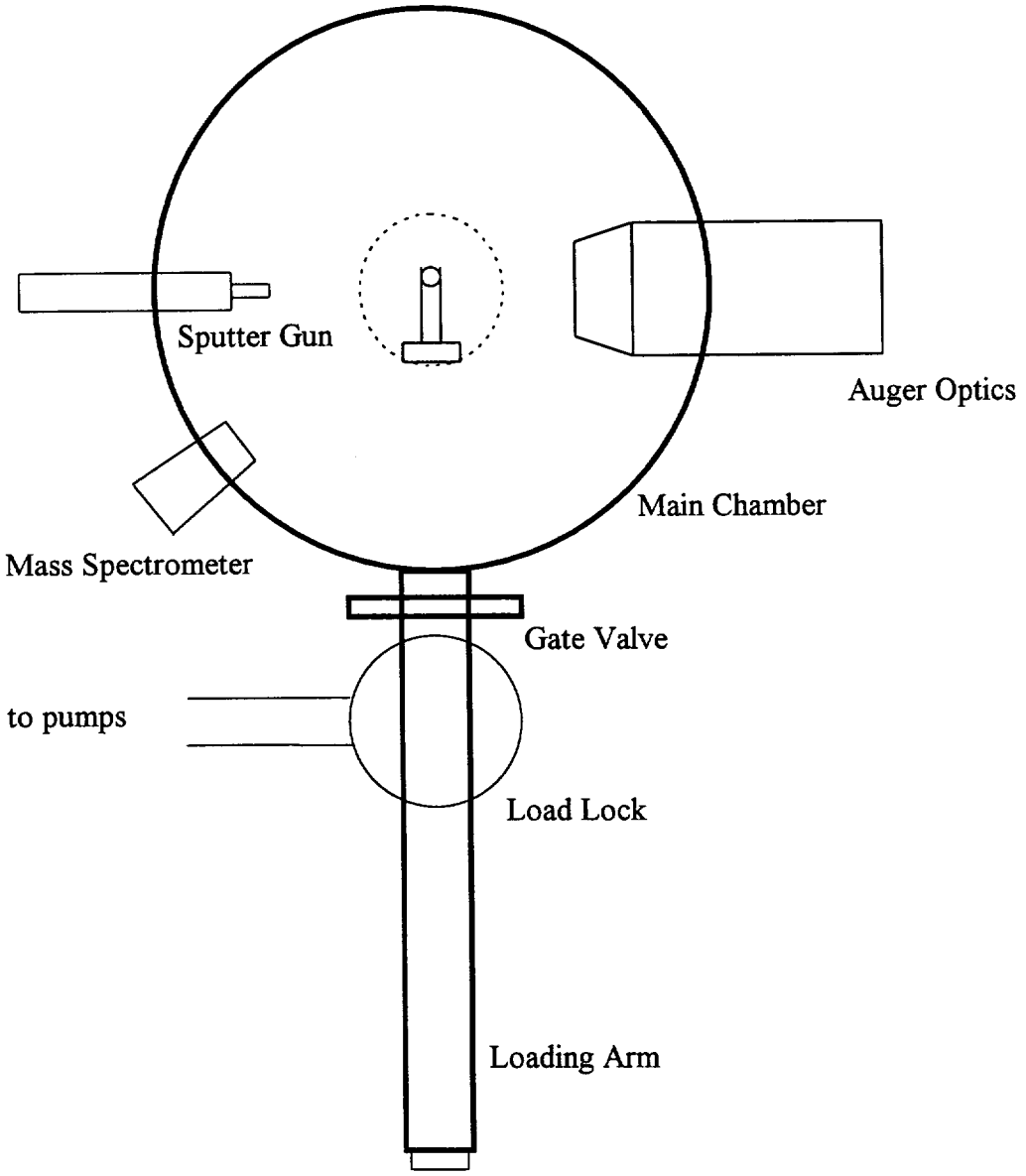


Figure 2.1 Ultra-High Vacuum System Set-Up

2.1.2 Sample Introduction

A sample introduction system was added in order to keep the upper half of the main chamber at low pressure during specimen exchange. The load lock was pumped by a combination of a Leybold Trivac roughing pump and a Leybold 50 liter turbo pump, and vented using pure nitrogen controlled by a Nupro leak valve. The pressure inside the loadlock was monitored by a Pirani gauge and a cold cathode gauge. The Pirani gauge was useful in the pressure range of atmospheric down to the low 10^{-2} Torr. The cold cathode gauge was useful in the mid 10^{-3} to low 10^{-7} range. The sample was held by a mechanical pincer at the end of a telescopic arm. A vacuum sample holder was used to either position or remove the sample from the pincer.

Sample introduction and removal is outlined as follows. The load lock chamber was pumped using the roughing pump only from atmospheric pressure down to 5×10^{-2} Torr. The turbo pump was then switched on. Once the turbo pump had reached full speed the cold cathode gauge was turned on. When the pressure in the load lock was below 1×10^{-6} Torr the gate valve to the main chamber could be opened. Sample introduction occurred by manipulation of the telescopic arm, sample holder and pincer. Once the sample was in the sample holder, the telescopic arm was retracted and gate valve closed. The loadlock was kept under low pressure while the sample was in the main chamber. For removal of the sample, the telescopic arm was placed back in the main chamber so that the pincer could clamp onto the sample. The sample holder was then lowered so that the sample could be retracted from the main chamber. The load lock was brought up to atmospheric pressure by first switching off the roughing pump, then switching off the turbo pump, and then slowly introducing pure nitrogen into the load lock as the turbo wound down. This sequence was followed to best reduce back streaming of oil from the roughing pump into the load lock and associated plumbing.

2.1.3 Sample Heating

Sample heating was achieved by using a thin 12 Ω resistive heating element powered by a Hewlett-Packard 6012A DC power supply which was controlled by an RKH Technology 310M temperature controller. The temperature of the heating block was monitored by a type K thermocouple which was mounted behind the graphite sheet at the center of the block. This provided the feedback loop for the temperature controller. The temperature of the sample was calibrated to the heater block temperature by attaching a thermocouple to a Si sample and recording the sample temperature during ramp up. Approximately 8 minutes after the heater block reached its temperature set point, the temperature of the sample surface as measured by the thermocouple would level off. This leveling off temperature of the sample surface would be below the set point of the heater block. The sample temperature would level off to 100 °C below the heater temperature for a heaterblock setpoint of 300 °C, and the sample surface temperature would be approximately 300 °C below the sample surface temperature for a heaterblock setpoint of 800 °C. For each ramp up one sample temperature vs. heater block temperature data point was obtained. A representative sample surface temperature vs. heater block temperature is given in Figure 2.2. This procedure was repeated several times and for several values of heater block temperature to obtain the sample heating calibration curve. This is given in Figure 2.3. During sample heating the pressure in the main chamber typically rose from a base pressure of around 3×10^{-10} Torr to 2×10^{-9} Torr for anneal times of less than 1 hour.

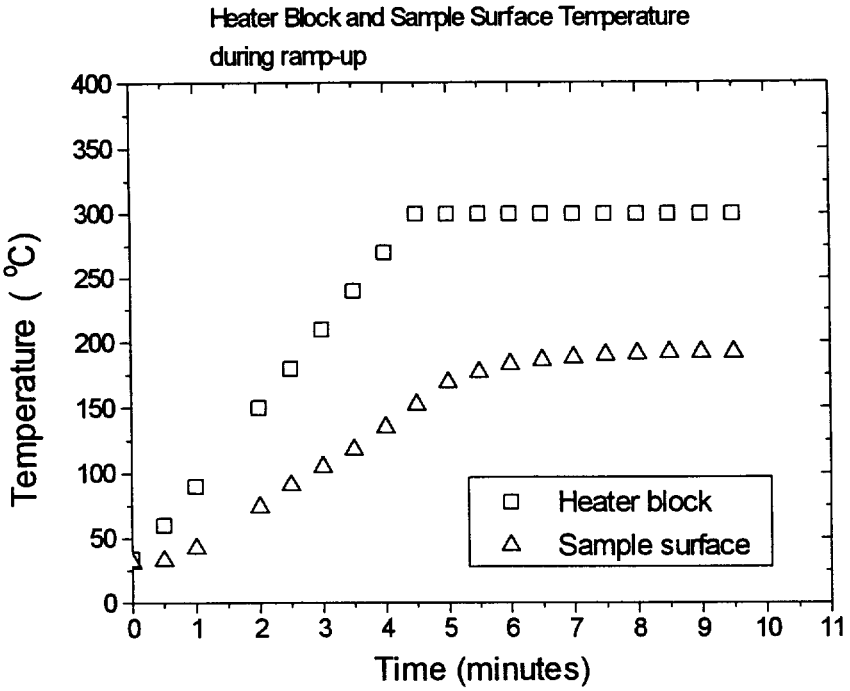


Figure 2.2 Temperature of Heater Block and Sample Surface During Ramp-Up

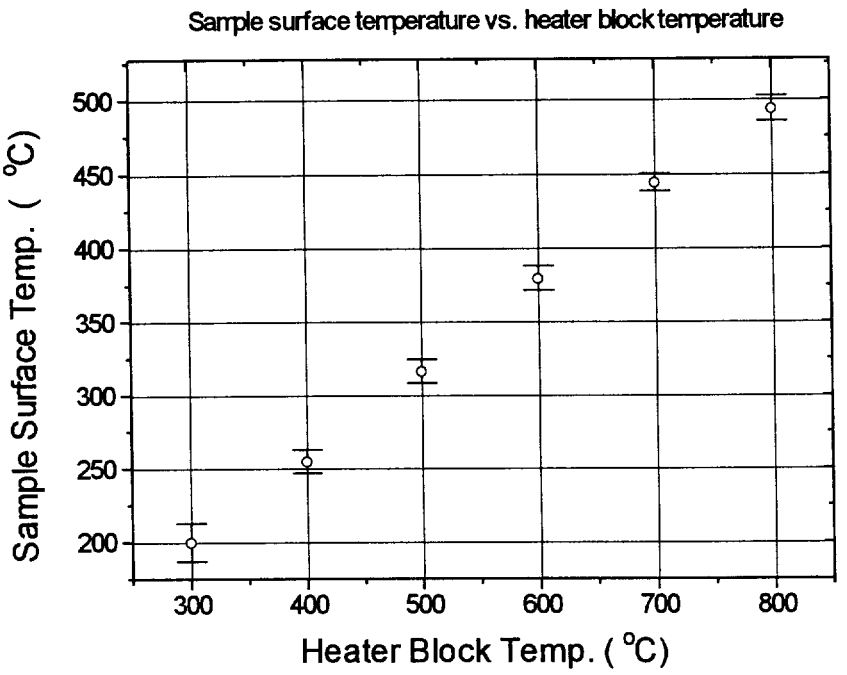


Figure 2.3 Sample Surface vs. Heater-Block Calibration.

2.2 Physical Vapor Deposition of Thin Films

Thin films were deposited using sputter deposition and evaporation. Metal films were deposited by sputtering at outside vendor sites and were also deposited using an evaporator. Sputtered oxide was deposited to form a passivation layer for the electromigration experiments. The sputtered oxide deposition conditions are outlined in section 2.4. Wafers were sent to vendors in different batches, as outlined below.

2.2.1 External Wafer Deposition: Batch 1

Samples from this batch were used in the experiments outlined in Chapter 5, section 5.2. A batch of 25 wafers of 150-mm-diameter were sent to Thinfilms Inc. for metal deposition [28]. The wafers were p-type Si with a 1 μm silicon dioxide layer. Various composite layers were deposited. Some of the composite stacks were deposited sequentially, whereas others were deposited with a break in vacuum between layers. Of the latter group, Ar sputter cleaning using 0.35 kW power was sometimes used prior to deposition. The sputter equipment was a Materials Research Corporation, 900 series machine. The composite film stacks are outlined in Table 2.1. All films were deposited onto silicon dioxide. All films were deposited in DC magnetron mode. The layer listed first was deposited first. Ag layers were 1 μm thick. Ti, TiN, and TiW layers were 400 Å thick. One slash mark between layers indicates that the layers were deposited sequentially. Two slash marks between the layers indicates that vacuum was broken and the wafers were removed from the chamber. The wafers were then stored in room ambient for 10 hours prior to deposition. Three slash marks between layers indicates that vacuum was broken, the wafers were exposed to atmosphere for ten hours, but the wafers were sputter cleaned in situ just prior to deposition. The deposition parameters for this split are given in Table 2.2.

Table 2.1 Wafer Deposition Recipes: Batch 1

Experiment Number	Recipe (top layer/middle/bottom/substrate)	Wafer Number
1	TiN	1
2	Ag / TiN	5
3	TiN / Ag	24
4	TiW	7
5	TiN / Ag [Hi power] / TiN	15, 16
6	TiN / Ag / TiN	10, 11, 12
7	TiN / Ag // TiN	2, 3
8	Ag /// TiN	4
9	Ti / Ag / TiN	17, 18
10	Ag / Ti / TiN	19, 20
11	Al / Ag / Al	21, 22
12	Ag / Al	23
13	TiN / Ag / TiW	13, 14
14	TiN / Ag // TiW	8
15	TiN / Ag /// TiW	9
16	TiW // Ag / TiN	6

Table 2.2 Wafer Deposition Parameters for Batch 1

	TiW	Ti	TiN	Al	Ag
System base pressure (Torr)	2×10^{-7}	2×10^{-7}	2×10^{-7}	2×10^{-7}	2×10^{-7}
Argon flow (SCCM)	50	50	50	50	50
Reactive gas			N_2		
Reactive gas flow			2 SCCM		
Target material and purity	TiW 99.9%	Ti 99.9%	Ti 99.9%	Al 99.999%	Ag 99.99%
Target size (inches)	$14^7/_8 \times 4^3/_4$	$14^7/_8 \times 4^3/_4$	$14^7/_8 \times 4^3/_4$	$14^7/_8 \times 4^3/_4$	Inset
Target to substrate spacing (inches)	2	2	2	2	2
Target power (kW)	0.6	1.2	3.0	1.65	1.8 (2.8)*
Scan speed inches/minute	5.5	15	21	30	2.75 (4.4)*
Sputtering rate (nm/kW.minute)	83.5	85.0	50.0	120.0	250.0
Substrate temperature (° C)	100 ± 15	100 ± 15	100 ± 15	100 ± 15	100 ± 15
Sputter etch power (for pre-cleaning)	0.35		0.35		
Sputter etch time	30 seconds		30 seconds		

* A higher power and faster scan speed was used in experiment 5.

2.2.2 External Wafer Deposition: Batch 2

In order to select the deposition conditions for the second batch of wafers, the effect of deposition power on resistivity was studied. A 200 mm oxide wafer was broken into four quarters, and 0.5 microns of Ag was deposited on each of the four pieces using the same MRC 900 series dc magnetron equipment as described in section 2.2.1. Four power levels were selected, ranging from 0.7 kW to 4.32 kW. The scan speed was adjusted to compensate for the increased deposition rate at higher power levels. The as-deposited resistivity was determined from four point probe sheet resistance measurements using a Magne-Tron Model M-800 Test Station along with thickness measurements obtained by using a Sloan Dektak II profilometer. The profilometer measurements were made on slide samples placed alongside the wafer sample during deposition. It was assumed that the thickness of the Ag film on the slide was equal to that of the wafer sample. In order to verify the validity of this assumption, wafer sample thickness measurements were made directly by making a cross-section with an ion milling machine and using an SEM to determine the Ag film thickness. The SEM magnification factor was determined from micrographs of NIST standard parallel lines of known separation. The micrographs of the NIST standard parallel lines and the cross-section micrographs were taken under identical SEM conditions.

The thickness measurements made by SEM were consistent with those made by the profilometer. The resistivity vs. deposition power is presented in Figure 2.4. In the first series the resistivity is derived from thickness measurements made using the SEM. In the second series the resistivity is derived from thickness measurements made using the profilometer. A best fit quadratic line using the resistivity data derived from the profilometer thickness measurements is given as a visual aid. This is done to illustrate the trend of decreasing resistivity with decreasing deposition power. The deposition power vs. as deposited resistivity data is also presented in Table 2.3. In this particular table, the resistivity data presented is derived using only the profilometer measurements. The error is estimated to be 5% based on the uncertainty of the auto leveling and local surface height variation. As can readily be seen from either Table 2.3 or Figure 2.4, the resistivity

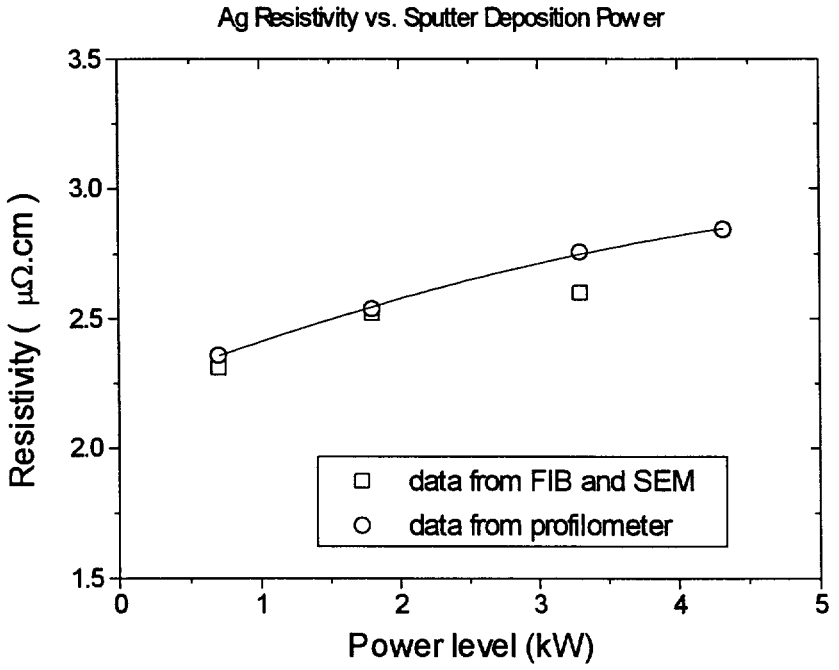


Figure 2.4 Graph of Resistivity of Ag Film vs. Sputter Deposition Power

decreases with decreasing sputter power (forward power on target) over the range of the experiment. Deposition power, pressure, substrate temperature, substrate to target spacing and substrate biasing can all influence the properties of the deposited film. Ideally the sputtering equipment should be characterized for all of the aforementioned parameters. However, since each sputter machine has its own unique characteristics, a more rigorous study of the deposition characteristics of this particular machine was not thought to be sufficiently worthwhile. A sputter deposition power of 0.7 kW was selected for the subsequent batch of wafers. The deposition conditions for the second batch of wafers is outlined in Table 2.4. The wafer deposition recipes for batch 2 are shown in Table 2.5.

Table 2.3 Resistivity of Ag films as a Function of Deposition Power

Power (kW)	Scan speed (inches/min)	Deposition rate (Å/min)	Resistivity (μΩ.cm)
0.70	2	175	2.36 ± 0.12
1.8	5.5	450	2.54 ± 0.13
3.3	10	825	2.76 ± 0.14
4.32	13	1080	2.84 ± 0.14

Table 2.4 Wafer Deposition Parameters for Batch 2

	TiW	Ti	TiN	Ag
System base pressure (Torr)	1×10^{-7}	1×10^{-7}	1×10^{-7}	1×10^{-7}
Argon flow (SCCM)	50	50	50	50
Reactive gas			N_2	
Reactive gas flow			2 SCCM	
Target material and purity	TiW 99.9%	Ti 99.9%	Ti 99.9%	Ag 99.99%
Target size (inches)	$14^7/_8 \times 4^3/_4$	$14^7/_8 \times 4^3/_4$	$14^7/_8 \times 4^3/_4$	Inset
Number of Scans	1	1	1	2
Scan speed (inches/minute)	5.5	15	21	2 (1st scan) 3 (2nd scan)
Target power (kW)	0.6	1.2	3.0	0.7
Target to substrate spacing	2 inches	2 inches	2 inches	2 inches
Sputtering rate (nm/kW.minute)	83.5	85.0	50.0	250.0
Substrate temperature (° C)	100 ± 15	100 ± 15	100 ± 15	100 ± 15
Sputter etch power (for pre-cleaning)	0.35		0.35	
Sputter etch time	30 seconds		30 seconds	

Table 2.5 Wafer Deposition Recipes: Batch 2

Wafer ID	Recipe top layer/middle/bottom/(substrate)
KV1	Ti/Ag//TiN
KV 2	Ti/Ag/Ti//TiN
KV 3	TiW/Ag/Ti//TiN
KV 4	Ti/Ag/TiN
KV 5	Ag
KV 6	TiW/Ag/TiW
KV 7	TiW/Ag/TiW
LY1	Ag//TiN
LY2	Ti/Ag/Ti//TiN
LY3	TiW/Ag/Ti//TiN
S1B	Ag(//SiO_2)

2.2.3 External Wafer Deposition: Batch 3

Patterned wafers were sent to International Wafers Service [29]. These wafers were used in the second batch of reflow experiments outlined in section 4.2.4 and in the silver interconnect line experiments of section 4.3. These wafers were also used in the electromigration experiments outlined in section 3.2. Ag of thickness 2.0 μm was sequentially deposited onto a 250 Å thick Ti layer without any break in vacuum. Wafer deposition parameters are outlined in Table 2.6.

Table 2.6 Wafer Deposition Parameters for Batch 3

	Ti	Ag
System base pressure	2×10^{-7} Torr	2×10^{-7} Torr
Deposition time	2 minutes	47 minutes
Substrate temperature	350 °C	350 °C
Substrate bias	150 V	150 V
Thickness	250 Å	20, 000 Å
Target Power	1 kW	0.7 kW

2.2.4 External Wafer Deposition: Batch 4

MOS structures were made by the sputtering of metal through a shadow mask. Wafers from batch 4 were used in the barrier effectiveness study outlined in section 5.3. Wafers from batch 4 were also used in the Cu and Ag diffusion experiments in section 3.1.5 and section 3.1.6. Wafers were sent out to International Wafer Service for deposition of Ag and barrier material. Barrier material was sputtered through a shadow mask of 5 mm diameter. Ag and Cu was subsequently sputtered through a shadow mask of 1 mm diameter. Vacuum was broken between the barrier layer and Ag or Cu layer. This was done to improve the barrier performance. A previous attempt using barrier material that was sputtered through a 1.5 mm diameter dot failed due to alignment

problems which resulted in part of the Ag dot being deposited directly onto the oxide. The backside of the wafer was first sputtered with Al-Si-Cu (1.0%, 0.5%) to ensure good electrical contact to the backside of the wafers. Wafer deposition parameters are outlined in Table 2.7.

Table 2.7 Wafer Deposition Parameters for Batch 4

	Ti	TiN	Ag	Ta	Al	Cu	Si_3N_4
System base pressure	2×10^{-7} Torr	2×10^{-7} Torr	2×10^{-7} Torr	2×10^{-7} Torr	2×10^{-7} Torr	2×10^{-7} Torr	2×10^{-7} Torr
Deposition time	1.3 minutes	1.6 minutes	2.5 minutes	2.0 minutes	9.0 minutes	5.4 minutes	10 minutes
Substrate temp.	unheated	unheated	unheated	unheated	unheated	unheated	unheated
Thickness (nm)	5.0	40.0	1,000	40.0	1,000	1,000	10.0
Target Power	0.25 kW	4 kW	7 kW	1 kW	7 kW	7 kW	1 kW

2.2.5 Evaporation of Ag Dots

Silver was evaporated through an Al shadow mask using a bell-jar evaporator. The system was pumped to base pressure prior to evaporation. Silver pellets were evaporated from a resistively heated crucible. The quality of the Ag film (resistivity for example) was not important, since the Ag dot was simply a source of Ag for diffusion into oxide. Therefore an extensive description of the evaporator equipment and procedures will be omitted.

2.3 Polishing Equipment and Procedure

2.3.1 Polishing Equipment

Samples were polished using the techniques outlined in this section in order to make Ag damascene structures for the line resistance experiments in section 4.3 and for the electromigration experiments in section 3.2. Polishing of Ag samples was done using a Buehler Ecomet III Polishing wheel, a felt pad, an Ultra Test Lapping Tool, and Buehler 0.05 μm alumina slurry. Film thickness was monitored by a modified four point probe using a Hewlett-Packard HP 6186C DC current source and a digital voltmeter. Post-polish rinsing utilized a Branson 1200 ultrasonic bath. The polishing wheel set-up is shown in Figure 2.5. The pressure of the sample against the polishing wheel was controlled by the micrometer screw gauge. Increasing the pressure on the sample increased the polishing rate but resulted in uneven polishing of the samples. The method outlined in the instruction manual was adhered to rigorously.

2.3.2 Removal Rate

The removal rate was monitored using a modified 4-point probe. The reciprocal of the V/I measurements were used to infer the thickness of the Ag film, since the initial film thickness and film sheet resistance were known. A representative thickness versus time plot is given in Figure 2.6. The wheel speed was set to give 80 rpm. The sample jig rotation speed of 20 rpm was used. The jig rotated counter to the rotation of the wheel as indicated in Figure 2.5.

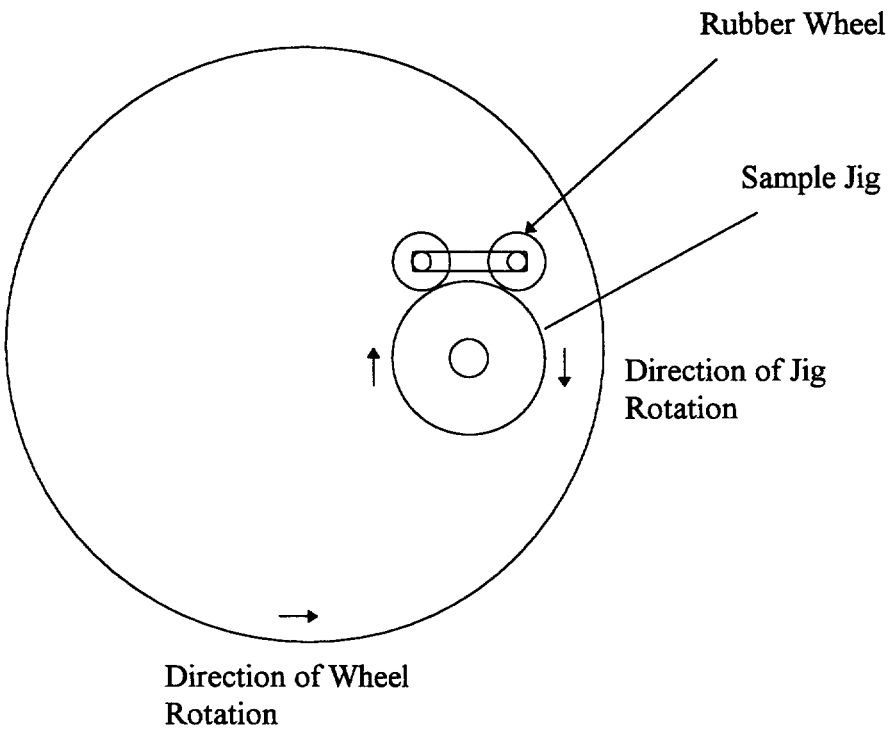


Figure 2.5 Polishing Wheel Set-Up

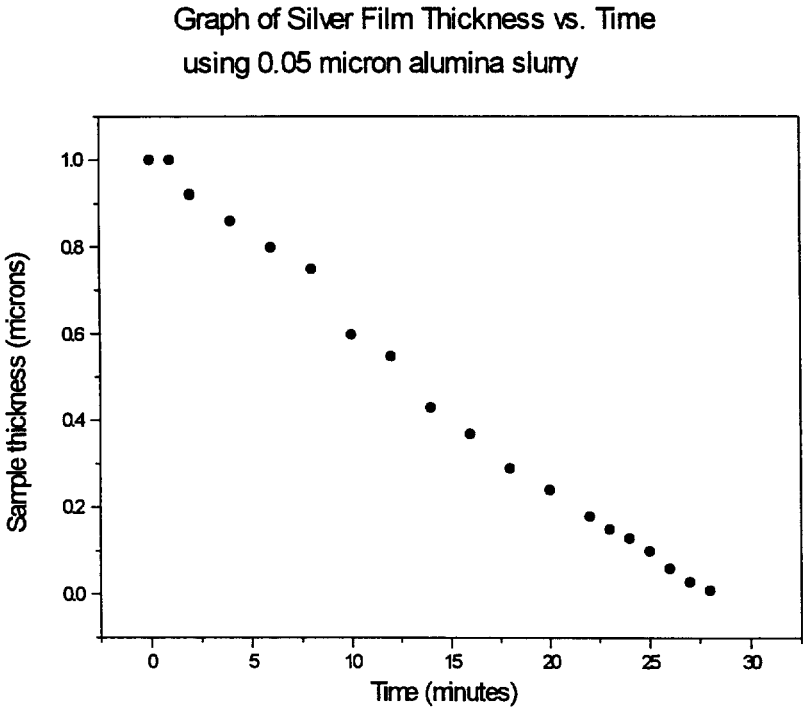


Figure 2.6 Thickness of Ag Film vs. Time

2.4 Passivation of Damascene Lines

Damascene lines were passivated using an Anatech Ltd. Hummer XII-1tm RF/DC Research sputtering system. A silicon dioxide sputtering target was used. Deposition conditions are outlined in Table 2.8.

Table 2.8 Deposition Conditions for Sputtered Silicon Dioxide Passivation

Power	200 Watts
Pressure	4 mTorr
Voltage (Gun/Stage)	200 V (25 Watts)
Angle	90 °
Sample to target separation	4 inches
Approximate deposition	3,000 Å

The physical properties of the oxide from this sputter oxide tool were not characterized.

2.5 Bias Thermal Stress Experiments

Metal Oxide Silicon (MOS) structures were fabricated using Ag as the electrode for the experiments of section 3.1.2 and for the diffusion barrier effectiveness experiments of section 5.3. During BTS the leakage current through the MOS structure was monitored using a Kiethly™ picoammeter, controlled by a 286 computer using a IEEE bus with lab windows. BTS was done in room ambient utilizing a Micro-manipulator™ probe station. Electrical contact was made to the Ag dot using a 40 mil tungsten probe tip. Leakage current density was calculated using the measured leakage current and the

estimated cross-sectional area of the Ag dot. The cross-sectional area of each dot was estimated based on the actual measurement of one of the dots of each group. The cross-sectional area of the dots were measured using a Dektak® profilometer. It was assumed that the dimensions of the measured dots were representative of the entire group.

2.5.1 Evaporated Ag-based MOS structures

The experiment in section 3.2 was broken into two parts. In the first part, MOS structures were fabricated by evaporation of Ag pellets (section 2.2.5) through a stainless steel mask onto a 1.0 μm thick oxide layer grown on p-type silicon. The oxide was grown by plasma assisted chemical vapor deposition using tetra-ethyl-ortho-silicate (TEOS) as the precursor. Oxide grown by this technique and using this precursor is called PTEOS. The PTEOS films were deposited in an Applied Materials 5000 series dual frequency plasma reactor. The Ag dots were 1 mm in diameter, and their centers were separated by 10 mm. Samples were back-coated using a platinum coater for electrical contact.

2.5.2 Sputtered Ag-based MOS structures

MOS structures were fabricated by sputtering of either Cu or Ag through a shadow mask onto 0.5 μm thick PTEOS film on 150 mm Si wafers (section 2.2.4). The PTEOS films were deposited in an Applied Materials 5000 series dual frequency plasma reactor. Dots were 1 mm in diameter and spaced by 10 mm. The back sides of the wafers were coated with 1 micron thick sputtered Al-Cu-Si. Preliminary Cu experiments (not reported here) were unsuccessful due to the oxidation of Cu and subsequent loss of electrical contact. This occurred at temperatures as low as 200 °C. In order to prevent oxidation of Cu, a thin (200 Å) Si_3N_4 capping layer was used . The capping layer was sputter deposited through a 5 mm shadow mask. The mask was aligned so that the metal dots and the Si_3N_4 dots would be concentric. The capping layer was applied to both Ag and Cu MOS structures to provide symmetry in the experiment.

2.5.3 Ag-based MOS Structures Using Diffusion Barriers

Barrier material was deposited through a shadow mask to yield 5 mm diameter dots whose centers were separated by 10 mm. Ag was subsequently deposited through a different shadow mask to yield dots of 1 mm diameter. The deposition conditions are outlined in section 2.2.4. The shadow mask was carefully aligned to ensure that none of the Ag was in contact with the underlying oxide. These structures were used in the diffusion barrier effectiveness study, section 5.3.

Chapter 3

Reliability

3.1 Field Assisted Diffusion of Ag into SiO_2

3.1.1 Motivation

Oxide integrity is known to be compromised by metallic impurities. Thin gate oxides are especially susceptible to impurities and defects at the Si-SiO_2 interface, and considerable work has been done in this area [30-50]. Uniformly scattered impurities lower the barrier height of the Si-SiO_2 interface, and also induce weak spots in the SiO_2, where the electric field is strengthened and local tunneling currents are enhanced. Both Cu and Ag are known to diffuse through SiO_2 as positive ions, from the frequently cited work of McBrayer [51]. Further studies of the diffusion of Cu in oxide have since confirmed these findings [52-53]. Table 3.1 shows the diffusivity constants for Cu and Ag diffusion through oxide that have been reported in the literature. The temperature dependence of the diffusivity, D, is given by:

$$D = D_0 \exp\left(-\frac{E_a}{kT}\right) \qquad \text{Eqn. 3.1}$$

where D_0 is the pre-exponential factor, E_a is the activation energy in eV, k is Boltzmann's constant in eV per degree Kelvin, and T is the temperature in degrees Kelvin. There is a large discrepancy between the pre-exponential term reported by the first reference (D_0 =

2.5×10^{-8} cm^2/s and that of the second reference (D_0 = 0.025 cm^2/s) in Table 3.1. The authors of the first reference commented that a comparison was not valid because data was collected in different temperature regimes.

Table 3.1 Comparison of measured diffusivity constants for Ag and Cu diffusion through SiO_2.

Oxide type and thickness	Metal	E_a (eV)	D_0 (cm^2/s)	BTS conditions	Reference
Thermal oxide 300 nm-550 nm	Cu	0.93 ± 0.2	2.5×10^{-8}	150 °C - 300 °C 1 MV/cm	52
Thermal oxide 500 nm	Cu	1.82	0.025	350 °C - 500 °C 0.05 MV/cm	51
Thermal oxide 500 nm	Ag	1.24	0.025	250 °C - 500 °C 0.05 MV/cm	51
CVD undoped oxide	Cu	1.2	(not given)	500 °C - 800 °C no field	54
Phosphorous-doped (4 mole percent) CVD oxide	Cu	1.6	(not given)	500 °C - 800 °C no field	54
Thermal oxide 100 nm	Cu	1.2	(not given)	100°C-225°C 4 MV/cm	53

The diffusion of either Ag or Cu through oxide is a reliability concern for two reasons. Firstly, metal contamination of the SiO_2 can compromise the oxide integrity. Secondly, both Ag and Cu are reported to form localized states in the band gap of Si [55]. Ag has a trap at 0.79 eV below the conduction band. Cu induces 2 trap states at 0.53 eV and 0.72

eV below the conduction band. These mid-gap trap levels can contribute to device leakage current. Cu is considered to be more of a threat than Ag due to the fact that Cu diffuses more readily through Si than does Ag [56]. The diffusion of both Cu and Ag through oxide has been a major obstacle to the realization of either Cu or Ag as an alternative metallization for ULSI circuit applications. However, Cu is reported to diffuse less readily through oxide when the oxide is doped with phosphorous [54, 57]. It is proposed that the mechanism of Cu diffusion suppression is similar to that of Na ion gettering [58]. More encouragingly yet, there have been no reported failures due to Cu contamination in metallization schemes that employ Al-Cu based alloys (although it is recognized that there is considerably less available free Cu in Al-Cu alloy based metal lines than there would be in Cu lines). This suggests that the reliability concerns associated with the diffusion of Cu through oxide may be over-rated. In order to determine the viability of Ag as an alternative metallization candidate, the reliability of interlayer dielectrics when in intimate contact with Ag must be evaluated. Such an evaluation should seek to estimate dielectric lifetime under normal operating conditions.

3.1.2 Experimental Outline

The experiment is broken into two parts. In the first part Ag-based Metal Oxide Silicon (MOS) structures were made using evaporated Ag as the contact metal. The oxide thickness was 1 μm. This is outlined in Chapter 2, section 2.5. The capacitors were then subjected to bias thermal stress (BTS) at fields of 0.1 to 0.6 MV/cm and at temperatures ranging from 200 °C to 300 °C. The leakage current through the MOS capacitor was measured as a function of time.

In the second part of the experiment Ag-based and Cu-based MOS structures were made using either sputtered Ag or sputtered Cu as the contact metal. The oxide thickness was 0.5 μm. The experimental details are described in Chapter 2 section 2.5. The capacitors were then subjected to bias thermal stress (BTS) at fields of 0.1 to 1.0 MV/cm and at temperatures ranging from 200 °C to 350 °C. Samples were stressed in groups of 4. Leakage current through the capacitor was measured as a function of time.

3.1.3 Experimental Results: Evaporated Ag

Representative leakage current density vs. time curves for evaporated Ag-based MOS structures are given in Figures 3.1 - 3.5. The time to failure of the device is considered to be when the leakage current is limited by the circuit. This value corresponds to a leakage current density on the order of 1 x 10^{-2} A/cm^2. Using this criterion, a time to failure under BTS was determined for a matrix of field and temperature conditions. The results are summarized in Table 3.2.

3.1.4 Experimental Analysis: Evaporated Ag

The leakage current curve of Figure 3.5 can be divided into 3 regions. In the first region there is a small leakage current. The second region shows an increasing leakage current indicating a significant pre-failure conduction mechanism. In the final stage the oxide is completely shorted and the leakage current is limited only by the measuring circuit.

3.1.4.1 Initial Stage of Leakage Current

During the initial stage the leakage current density is on the order of 10^{-6} μA/cm^2 - 10^{-8} μA/cm^2 under an applied electric field ranging from 0.1 MV/cm to 0.5 MV/cm, and in the temperature range of 225 °C to 300 °C. The resistivity range of the oxide is therefore between 10^{11} Ω-cm and 10^{13} Ω-cm. Oxide resistivity is typically in the range of 10^{14}-10^{16} Ω-cm at room temperature [59]. The conduction mechanism during the initial stages of bias thermal stress is most likely to be a combination of Poole-Frenkel emission, Fowler-Nordheim tunneling, and Space Charge Limited conduction, which is discussed later in this chapter. Table 3.3 shows the current-voltage dependence for several conduction mechanisms, taken from Ohring [60].

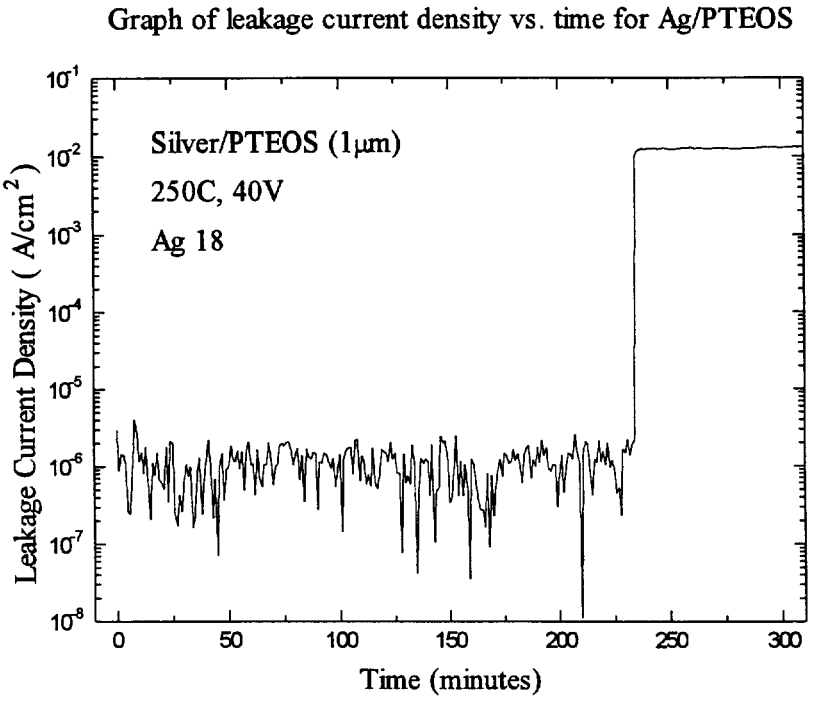


Figure 3.1 Leakage current density vs. time curve for BTS of 250 °C, 0.4 MV/cm (evaporated Ag/1 μm PTEOS oxide/Si)

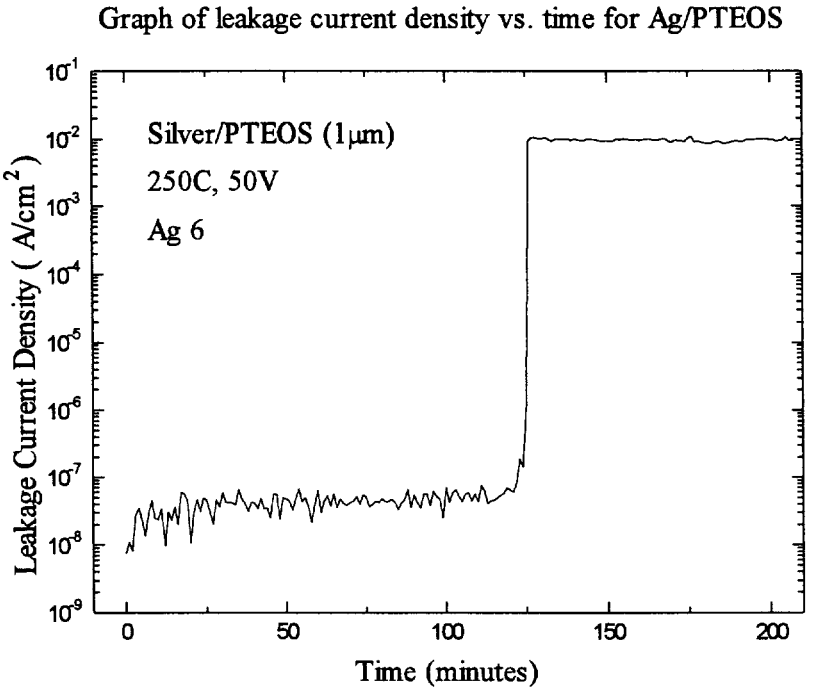


Figure 3.2 Leakage current density vs. time curve for BTS of 250 °C, 0.5 MV/cm (evaporated Ag/1 μm PTEOS oxide/Si)

Graph of leakage current density vs. time for Ag/PTEOS

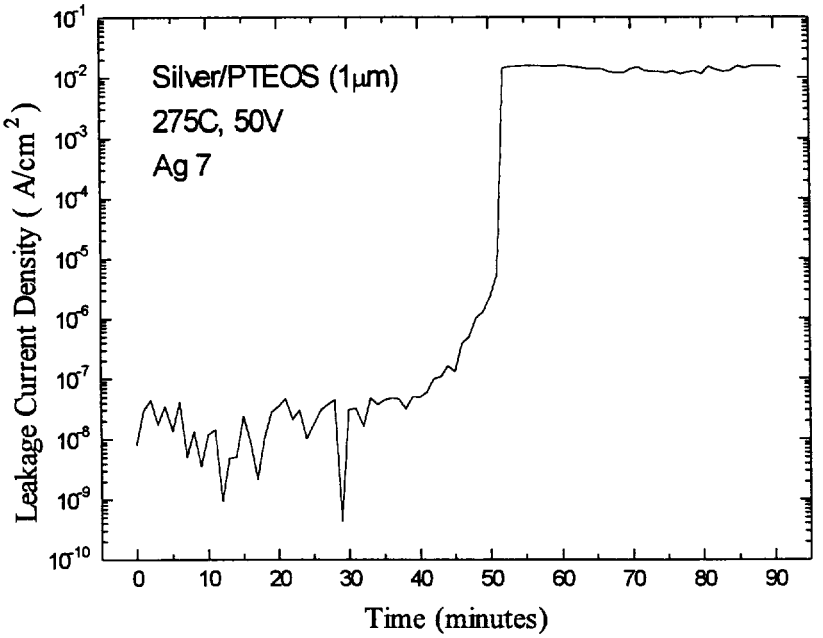


Figure 3.3 Leakage current density vs. time curve for BTS of 275 °C, 0.5 MV/cm (evaporated Ag/1 μm PTEOS oxide/Si)

Graph of leakage current density vs. time for Ag/PTEOS

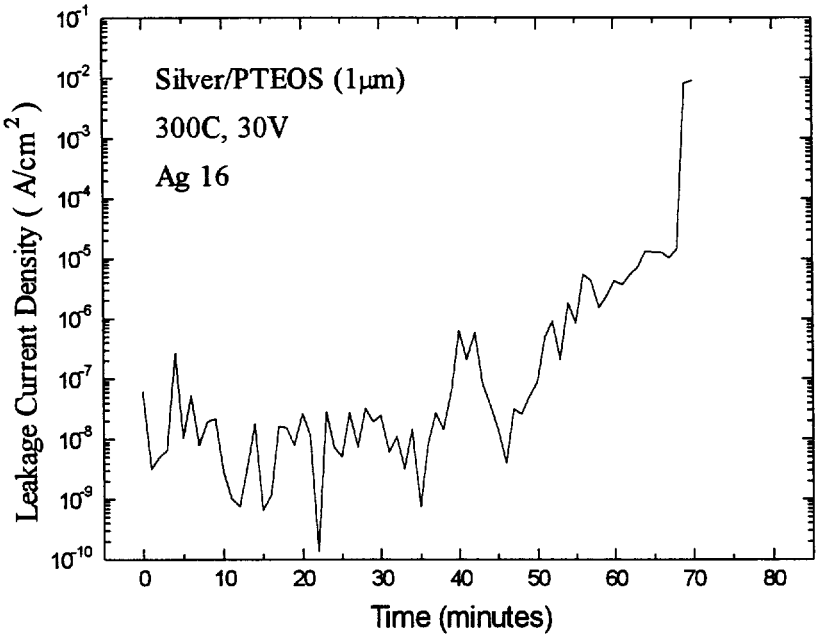


Figure 3.4 Leakage current density vs. time curve for BTS of 300 °C, 0.3 MV/cm (evaporated Ag/1 μm PTEOS oxide/Si)

Graph of leakage current density vs. time for Ag/PTEOS

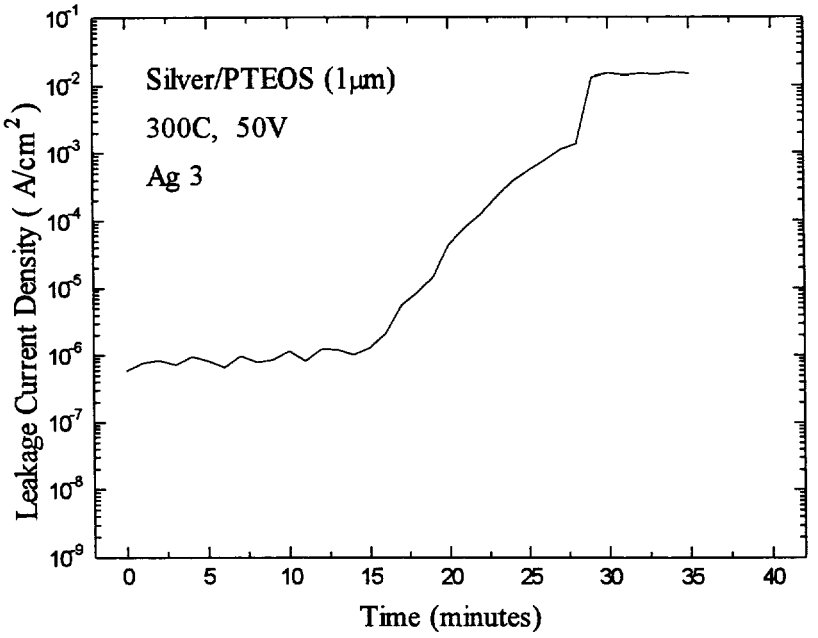


Figure 3.5 Leakage current density vs. time curve for BTS of 300 °C, 0.5 MV/cm (evaporated Ag/1 μm PTEOS oxide/Si)

Table 3.2 Time to Failure Data for Evaporated Ag on PTEOS

Time to Failure Data for evaporated Ag on 1 micron thick PTEOS								
(sort by temp)					(sort by run)			
	T	V	TTF(mins)			T	V	TTF(mins)
Ag1	200	50	3600		Ag 1	200	50	3600
Ag2	200	50	2520		Ag 2	200	50	2520
Ag10	225	50	512		Ag 3	300	50	29
Ag 34	225	40	2028		Ag 4	300	50	20
Ag14	225	50	655		Ag 5	250	50	115
Ag5	250	50	115		Ag 6	250	50	126
Ag6	250	50	126		Ag 7	275	50	52
Ag23	250	30	730		Ag 8	275	50	31
Ag17	250	30	1750		Ag 9	275	50	36
Ag18	250	40	236		Ag 10	225	50	512
Ag19	250	20	6100		Ag 11	275	40	84
Ag24	250	60	52		Ag 12	275	30	237
Ag33	263	30	616		Ag 13	poor contact		no data
Ag30	268	20	1595		Ag 14	225	50	2028
Ag22	275	20	694		Ag 15	300	40	24
Ag7	275	50	52		Ag 16	300	30	69
Ag8	275	50	31		Ag 17	250	30	1750
Ag9	275	50	36		Ag 18	250	40	236
Ag11	275	40	84		Ag 19	250	20	6100
Ag12	275	30	237		Ag 20	300	20	435
Ag29	275	20	1208		Ag 21	300	25	219
Ag25	275	60	19		Ag 22	275	20	694
Ag31	287	20	623		Ag 23	250	30	730
Ag32	287	30	209		Ag 24	250	60	52
Ag27	300	55	24		Ag 25	275	60	19
Ag26	300	60	8		Ag 26	300	60	8
Ag20	300	20	435		Ag 27	300	55	24
Ag21	300	25	219		Ag 28	300	10	1398
Ag16	300	30	69		Ag 29	275	20	1208
Ag15	300	40	24		Ag 30	268	20	1595
Ag3	300	50	29		Ag 31	287	20	623
Ag 28	300	10	1398		Ag 32	287	30	209
Ag4	300	50	20		Ag 33	263	30	616
					Ag 34	225	40	2028

Table 3.3 Current-voltage dependence for various conduction mechanisms

Mechanism	Current-voltage relation
Shottky Emission	$I \propto \exp(\alpha V^{1/2})$
Tunneling	$I \propto V^2 \exp(-\beta/V)$
Space Charge Limited	$I \propto V^2$
Poole-Frenkel Emission	$I \propto V \exp(\delta V^{1/2})$
Ionic Conduction	$I \propto V$

An excellent overview of these conduction mechanisms is given in Ohring [60]. It is theoretically possible to distinguish between the different mechanisms by the field and temperature dependence, providing there has been no perturbation by the BTS. However, due to the low signal-to-noise ratio in the current measurement, the variability in dot dimensions, and the variation of the physical properties between samples, the J vs. E curves (current density vs. electric field) that were generated using the values of current density during the initial stage were inconclusive, and will not be presented here. The conduction mechanism responsible for current flow during the initial stages of bias thermal stress cannot be determined from the data.

3.1.4.2 Second Stage of Leakage Current

The second stage is characterized by an increase in leakage current. The leakage current is not sufficiently large that it is limited by the measuring circuit. Many samples exhibited a very small transitional stage from a low leakage current to complete oxide failure. The conduction mechanism during the second stage may be very complex. It is assumed that immediately prior to failure, the oxide contains a considerable amount of Ag impurity. The Ag may be interstitial and acting as a trap center. Conduction could be occurring by hopping between sites. The current could therefore be resulting from

Fowler-Nordheim tunneling between impurity sites. The amount of current would increase as more Ag is diffused into the oxide.

It is also possible that ionic conduction is occurring. For this to occur a Ag ion would diffuse through the oxide and pick up an electron when it reached the Si-oxide interface. The component of the leakage current due to ionic conduction could be determined if the Ag ion flux through the oxide was known. For example, a flux of 6.3×10^{11} cm^{-2}/sec of Ag ions would correspond to a leakage current of 1×10^{-7} A/cm^2 ($1/e = 6.3 \times 10^{18}$). This amount of flux is approximately half of the Ag flux reported by McBrayer for Ag-based MOS structures under BTS of 300 °C and 0.04 MV/cm as measured by RBS [51]. It is also possible that Ag atoms are forming centers for Poole-Frenkel emission. Another possible mechanism is oxide thinning whereby the Ag could drift through the oxide until it reaches the oxide silicon interface. Build up of Ag would therefore occur, with the Ag accumulating at the Si-oxide interface and protruding into the oxide. This would result in effective thinning of the oxide in local regions, resulting in enhanced local fields. The enhanced local fields would result in further Ag diffusion and build-up of the Ag protrusions. Eventually the oxide would be sufficiently thinned, at least in local regions, for the onset of Fowler-Nordheim tunneling. Very large Ag protrusions would have to build up at the Si-oxide interface for there to be a significant thinning of the oxide. Ag build-up at the Si-oxide interface was observed by McBrayer [61], where Ag spheres were identified at the Si-oxide interface. However, the diameter of the Ag spheres was only approximately 50 Å. Oxide thinning by this mechanism does not therefore seem likely in this case, considering that the oxide thickness is 1 μm.

Another mechanism whereby the oxide is effectively thinned is described by Raghavan et al. [53]. The increasing metal concentration in the region of the oxide closest to the metal-oxide interface will result in the lowering of the potential drop across that region. Therefore, as the metal concentration increases near the metal-oxide interface, the electric field across the remainder of the oxide increases. This results in more electron leakage current, resulting in further injection of Ag ions, further oxide thinning, and eventual breakdown. This type of mechanism is reported to be responsible for the failure

of Cu-based MOS structures (0.1 μm thick oxide) under bias thermal stress as reported by Raghavan [53].

In the work of McBrayer [51], it was reported that the Ag build-up at the Si-oxide interface was 2 orders of magnitude less when the BTS experiments were performed in vacuum. It was concluded that an additional species plays a role in the diffusion of Ag under bias thermal stress. It is possible that moisture plays an important role in the diffusion mechanism. The ionization potential of Ag is 4.7 eV. The amount of Ag that would be ionized by thermal excitation in the 200 °C - 300 °C temperature range is negligible. Distortion of the coulomb potential well by an electric field of 0.5 MV/cm, (which is 0.005 V/Å) is also negligible. However, the Ag can lose an electron readily depending on the matrix of species which surround it. It is likely that the high impurity levels in the oxide contribute to the ease with which the Ag neutral is ionized. This would essentially mean that there was a chemical reaction of the Ag with the oxide matrix. The Ag ion would then diffuse more readily through the oxide than a neutral as a result of the electric field. It is also possible that an ion drifts through the oxide and regains and loses its electron many times in its interaction with the oxide matrix. Moisture evolution from similar PTEOS films has previously been studied [62]. The results of the study concluded that moisture can be readily absorbed into the oxide film if the wafer is not kept in an ultra dry environment. The amount of moisture that can subsequently be evolved by thermal desorption for PTEOS films (deposited in an Applied Materials 5000 series reactor) is in the order of 4 mg of H_2O per cubic centimeter of oxide film. High moisture content is associated with poor oxide integrity.

3.1.4.3 Third Stage of Leakage Current

The third and final stage is characterized by a leakage current that is limited only by the measuring circuit. A combination of the conduction mechanisms outlined in the previous section could be responsible for the leakage current. It may also be worthwhile to consider the Ag as a dopant contributing to additional band levels, much the same way as B and P contribute to the energy bands of Si. The interaction of Ag, moisture and Na

in the oxide may contribute additional bands that allow for conduction in the oxide. (Na is a common impurity than can readily be incorporated into the samples by poor handling practices.) In the work of DeStafeno [37], the oxide failure was considered to be a result of Na induced barrier reduction at the Si-oxide interface. The reduced barrier results in enhanced electron tunnel injection leading to breakdown by local heating or by electron avalanche. When the leakage current is limited by the measuring circuit the field across the oxide drops. Therefore the electrical component of the driving mechanism for further diffusion no longer exists. The activation energy of diffusion of Ag through oxide was determined by measuring the build-up of Ag at the Si-oxide interface in the work of McBrayer. However, if the oxide integrity has been compromised, the electrical component of the driving force for further diffusion no longer exists. Therefore the method used by McBrayer [51] is only valid if the oxide has not failed.

An interesting observation was made that it was possible to "heal" the oxide by applying a reverse bias. Sample Ag33 was subject to BTS at 30 V, 263 °C. Following failure, the bias was reversed so that -30 V was applied to the gate. The leakage current dropped several orders of magnitude before the first current measurement was made. After 3,155 minutes of reverse bias, the gate was again given a 30 V positive bias. Within 7 minutes of positive bias, the leakage current was again limited only by the measuring circuit. Leakage current density vs. time for sample Ag33 is given in Figure 3.6 This observation supports the idea that Ag sites, either neutral or charged, act as local hopping sites which contribute to the leakage current. Under reverse bias the Ag is swept away from the Si-oxide interface into the oxide, thus the "bridge" is broken. This observation is not consistent with the explanation that the conduction mechanism is simply Fowler-Nordheim tunneling across a locally thinned oxide where Ag had built up. It would be unlikely that the Ag build-up at the interface could be swept away so readily. The lifetime of a healed sample was also observed to be short. Under forward bias both the electric field and the concentration gradient drive diffusion toward the Si-oxide interface. Under reverse bias however, (assuming that the Ag does not build up at the interface), the electric field forces diffusion in the opposite direction to the concentration gradient.

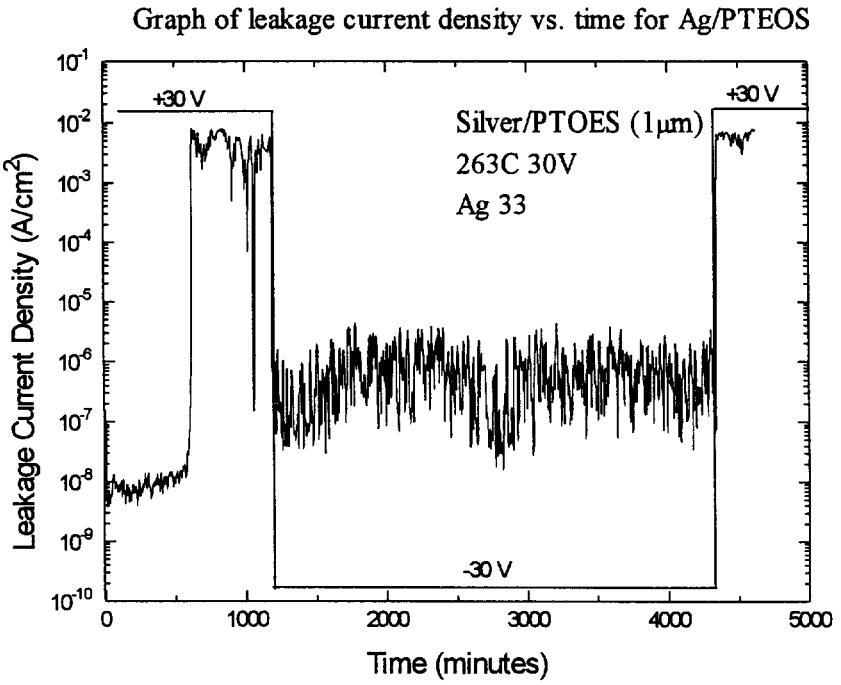


Figure 3.6 Leakage current density vs. time curve for BTS of 263 °C, 0.3 MV/cm. Sample was then reverse biased and subsequently forward biased (evaporated Ag/1 μm PTEOS oxide/Si)

Failure analysis on the Ag dots was performed by Auger Electron Spectroscopy and Gallium SIMS. An Auger depth profile was performed using a Fisons 310 system. The data was collected using at least 50 levels so that information could be gathered at the Si-oxide interface. The detection limit for Ag was 1 atomic percent. Ag was not detected in the bulk of the oxide or at the Si-oxide interface. Gallium SIMS was performed on a sample using a FEI focused ion beam (FIB) system. Compared to other SIMS techniques, the FIB is crude. However, the detection limit is in the order of 0.1 atomic percent for Ag, which is more sensitive than Auger. Prior to analysis the Ag was peeled from the oxide using Scotch tape. Again, Ag was not detected in the oxide or at the Si-oxide interface. It is known therefore that the level of Ag impurity in the oxide is 0.1 % or lower after failure. If there had been a considerable build-up of Ag at the Si-oxide interface, it would have been detected by the aforementioned techniques, unless the build up was extremely localized. Considering that the oxide was 1.0 μm thick, a very large build-up would be required to cause noticeable oxide thinning. The fact that Ag was not detected suggests that the oxide thinning explanation is not valid in this case.

3.1.4.4 Extrapolation of Time to Failure Data

A plot of the natural log of the failure time vs. 1/kT for several values of field strength is given in Figure 3.7. For each value of field strength an activation energy can be obtained assuming that the time to failure is given by the Arrhenius equation of Eqn. 3.2.

$$\text{ttf} = C\exp\left(\frac{Q}{kT}\right) \qquad \text{Eqn. 3.2}$$

where ttf = time to failure, Q is the field dependent activation energy, C is an arbitrary constant, and kT has the usual meaning. Using a least squares fit, the value for the activation energy, Q, is determined. The results are given in Table 3.4.

Table 3.4 Activation Energy Determined for Each Field Strength

Field Strength (MV/cm)	Activation Energy (eV)
0.2	1.37 ± 0.22
0.3	1.37 ± 0.24
0.4	1.18 ± 0.10
0.5	1.18 ± 0.07
0.6	0.97 ± 0.02

A plot of activation energy vs. field strength is given in Figure 3.8. The activation energy for each field strength was calculated using a least-square fit. The standard deviation was also calculated, and this is shown by the error bars in Figure 3.8. It can be seen that the effective activation energy is lower for higher values of electric field. It is recognized that the failure mechanism is not necessarily a single step process, and a single activation energy may therefore not necessarily be strictly appropriate. The basis of the model for diffusion is the isotropic one-dimensional random walk [63-64], which lead to Fick's first law (Eqn. 3.3).

$$J(x,t) = -D\frac{\partial C}{\partial x} \qquad \text{Eqn. 3.3}$$

However, in the presence of an external force, the jump frequencies to the right and to the left are not equal. When the external force is an electric field, the flux of charged particles, J, is given by:

$$J(x,t) = -D\frac{\partial C}{\partial x} + \mu CE \qquad \text{Eqn. 3.4}$$

with:

$$\mu = \frac{q}{kT}D \qquad \text{Eqn. 3.5}$$

where μ is the mobility, q is the charge on an electron, D is the diffusivity and kT has the usual meaning. When the concentration gradient is small compared to the electric field, these equations can be used to determine the diffusivity if the flux, J, is known. However, there is not a simple relationship between time to failure and flux density. There is no immediately obvious way to relate time to failure to the above equations. The field dependent activation energy, Q, in Eqn. 3.2 is not necessarily the diffusion activation associated with the diffusivity, D of Eqn. 3.3, even though, based on the data, the time to failure is a thermally activated process. Great care must be taken when assigning physical significance to an activation energy. Concern about implying physical meaning to the activation energy derived from a natural log of time to failure vs. 1/kT has been expressed by others [53].

It is interesting to estimate the zero-field activation energy for this system. By extrapolating the effective activation energy vs. field data in Figure 3.8, a zero-field activation energy estimate of 1.6 eV is obtained. However, it may be incorrect to assume that this value is the activation energy of thermal diffusion of Ag in SiO_2. It is also observed that the time to failure has an exponential dependence on field. This can be seen in the time to failure vs. electric field (at constant temperature) curves at 250 °C, 275 °C and 300 °C, that are given in Figures 3.9-3.11.

Graph of ln (time to failure (mins)) vs. 1/kT
for Ag/PTEOS (1μm)

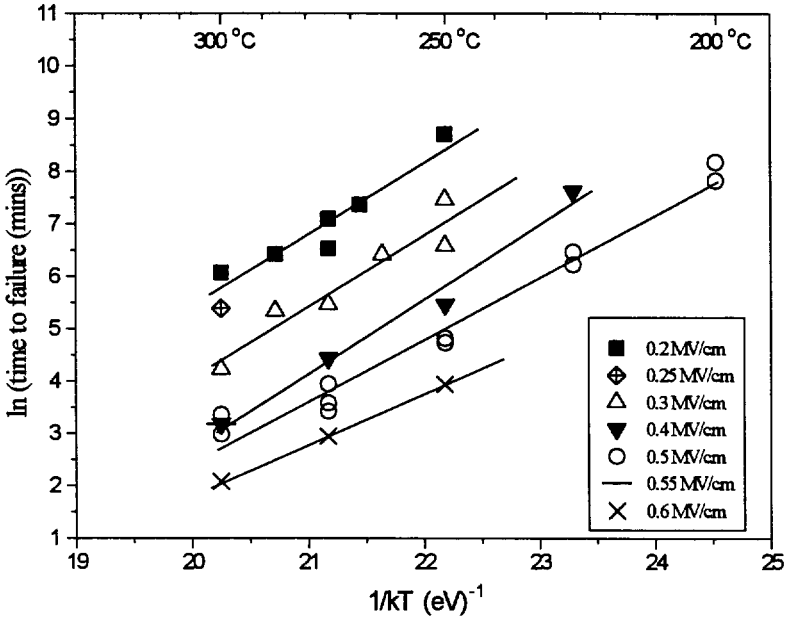


Figure 3.7 Graph of natural log of time to failure vs. 1/kT
(evaporated Ag/1 μm PTEOS oxide/Si)

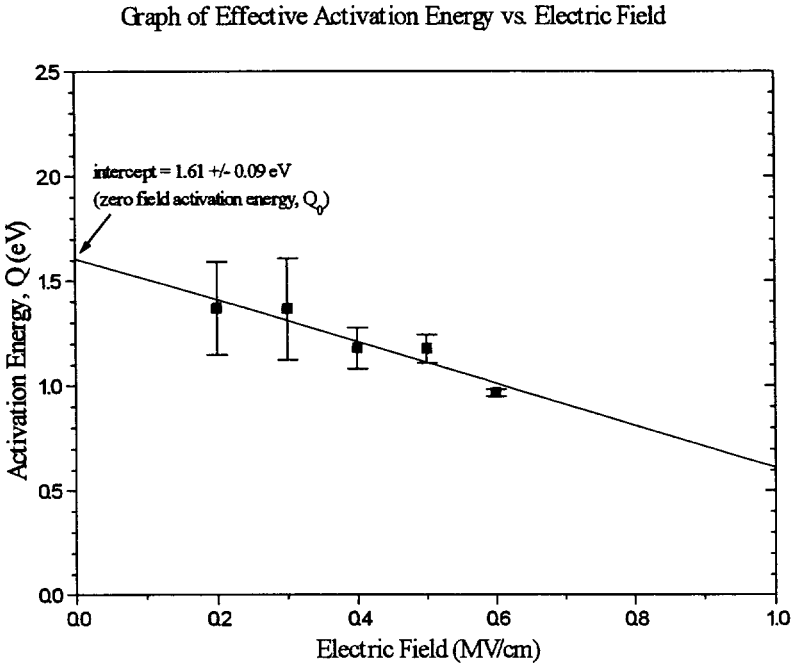


Figure 3.8 Graph of effective activation energy vs. electric field (evaporated Ag/1 μm PTEOS oxide/Si)

Using the data available, an empirical equation that predicts the time to failure can be derived. This equation is valid for the field range of 0.2 MV/cm to 0.6 MV/cm, and for temperatures ranging from 200 °C to 300 °C. The constants may have no physical significance as the equation is derived empirically. The equation has the form:

$$\ln(\text{ttf}) = (a - bE) + \left(\frac{Q_0 - \alpha E}{kT - kT_0}\right) \qquad \text{Eqn. 3.6}$$

where ttf is the time to failure in minutes, a, b, and α are constants, E is the electric field, and Q_0 is the zero field activation energy. The data collected fits well to this formula. The constants were set to give the best fit to the data. The values of the constant are given in Table 3.5.

Table 3.5 Best Fit Constants for Eqn. 3.6

Q_0	1.61 eV
α	0.99 eV.cm/MV
a	8.77
b	9.66 cm/MV
T_0	275 °C

The data fits well to the functional form of Eqn. 3.6 for the range of temperature and electric field of the experiment. Using the values of Q_0, α, a, and b that best fit the data, we can estimate the failure time of the dielectric between adjacent Ag interconnects in devices operating at 2V. In doing so it is implied that the semi-empirical equation (Eqn. 3.6) is valid outside the range of the experiment, which may not be true. This is recognized however as one of the potential shortcomings of accelerated testing. Assuming a line spacing of 0.25 μm (the production target for 1998 according to SIA roadmap, Table 1.1), corresponding to a field of 0.06 MV/cm at 2 V, and an operating

temperature of 150 °C, failure time would be 112 years, and at 200 °C it would be 1 year without any diffusion barrier. A comparison of the collected data and the extrapolated data using the best fit constants is given in Table 3.6. Some oxide degradation may occur before failure, as is suggested by the increased pre-failure leakage current in some of the samples tested. Although there is no similar prediction for Ag-based MOS structures in the literature, a comparable analysis for Cu-based MOS structures by Raghavan [53], who measured time dependent leakage current under BTS using thermal oxide, estimated a lifetime of 2 weeks for a device operating at 200 °C and 10 years for a device operating at 100 °C (assuming an operating voltage of 2.5 V, and a dielectric thickness of 0.12 μm).

Table 3.6 Table of Measured and Predicted Time to Failure of Ag Samples

Sample	Electric Field	Temperature	Time to Failure	Predicted Time To Failure
	(MV/cm)	(C)	(minutes)	(minutes)
Ag1	0.5	200	3600	2169
Ag2	0.5	200	2520	2169
Ag10	0.5	225	512	550
Ag 34	0.4	225	2028	1783
Ag14	0.5	225	655	550
Ag5	0.5	250	115	159
Ag6	0.5	250	126	159
Ag23	0.3	250	730	1340
Ag17	0.3	250	1750	1340
Ag18	0.4	250	236	461
Ag19	0.2	250	6100	3890
Ag24	0.6	250	52	55
Ag33	0.3	263	616	661
Ag30	0.2	268	1595	1372
Ag22	0.2	275	694	932
Ag7	0.5	275	52	51
Ag8	0.5	275	31	51
Ag9	0.5	275	36	51
Ag11	0.4	275	84	135
Ag12	0.3	275	237	355
Ag29	0.2	275	1208	932
Ag25	0.6	275	19	20
Ag31	0.2	287	623	491
Ag32	0.3	287	209	196
Ag27	0.55	300	24	12
Ag26	0.6	300	8	8
Ag20	0.2	300	435	253
Ag21	0.25	300	219	163
Ag16	0.3	300	69	106
Ag15	0.4	300	24	44
Ag3	0.5	300	29	18
Ag 28	0.1	300	1398	607
Ag4	0.5	300	20	18
interconnect	0.06	150		112 years
interconnect	0.06	200		1 year

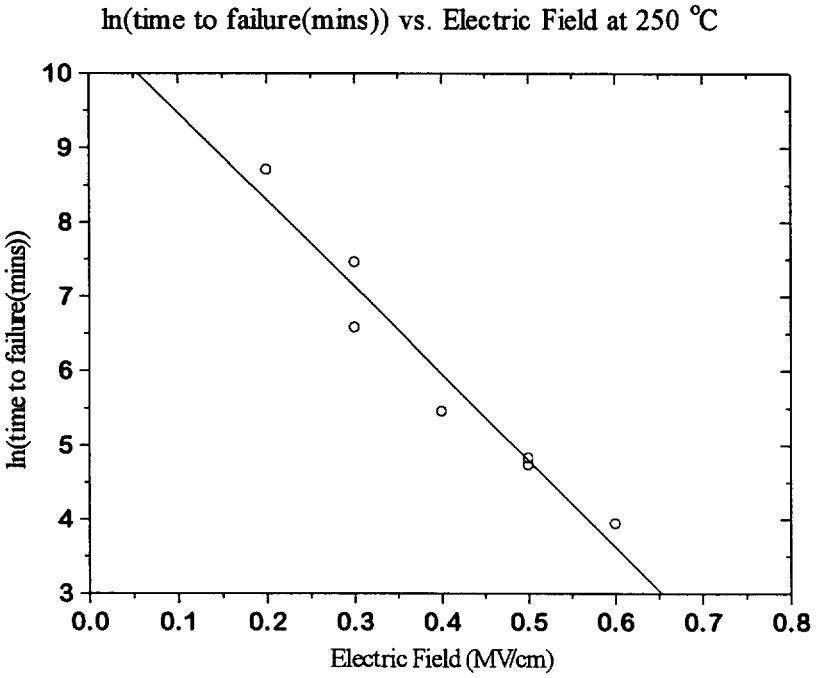


Figure 3.9 ln(time to failure(mins)) vs. electric field at 250 °C (evaporated Ag/1 μm PTEOS oxide/Si)

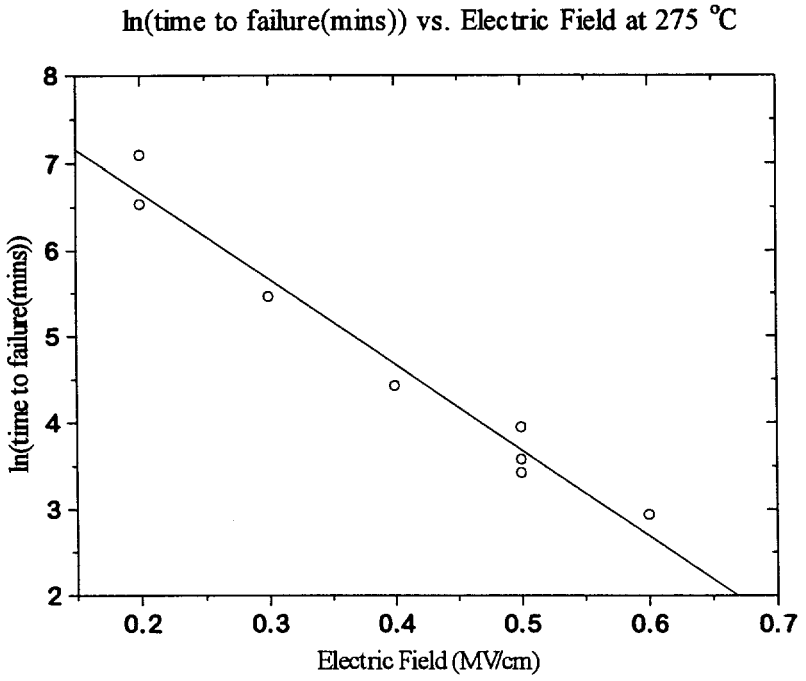


Figure 3.10 ln(time to failure(mins)) vs. electric field at 275 °C (evaporated Ag/1 μm PTEOS oxide/Si)

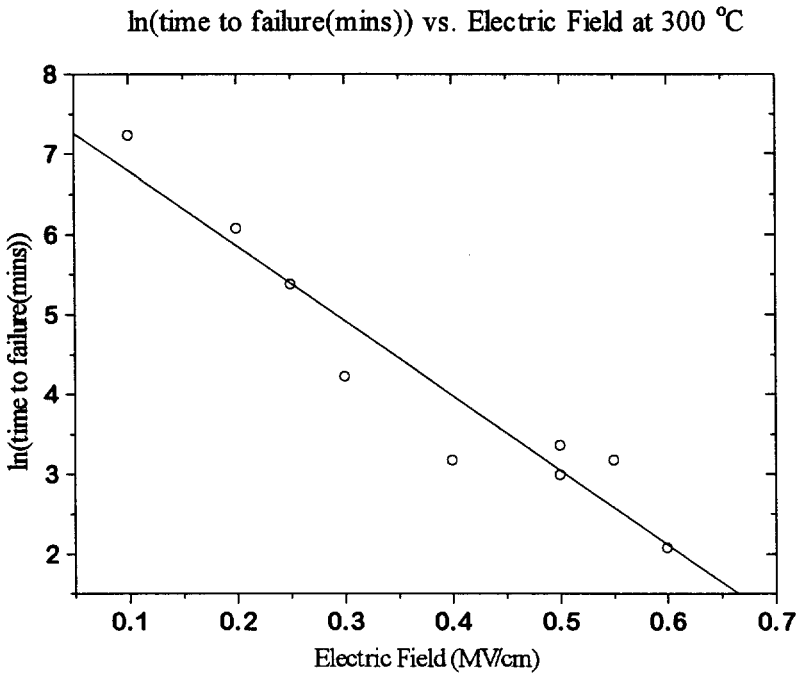


Figure 3.11 ln(time to failure(mins)) vs. electric field at 300 °C (evaporated Ag/1 μm PTEOS oxide/Si)

3.1.5 Experimental Results: Sputtered Ag and Cu

Time to failure data for sputtered Ag-based and sputtered Cu-based MOS structures on 0.5 μm PTEOS is given in Figure 3.12, and the data are summarized in Table 3.7. Representative leakage current vs. time curves for Ag-based MOS structures are given in Figures 3.13 - 3.17. Representative current vs. time curves for Cu-based MOS structures are given in Figure 3.18 and Figure 3.19.

3.1.6 Experimental Analysis: Sputtered Ag and Cu

The leakage current density curves for the sputtered Ag-based MOS structures are similar to those of the evaporated Ag-based MOS structures described in section 3.1.4. Greater care had been taken in measuring the pre-failure leakage current and the signal to noise ratio is considerably better for the sputtered Ag data compared to the evaporated Ag data. This was done by using coaxial cables throughout the measuring circuit and eliminating any ground loops. The leakage current curve can now be split into 4 regions as indicated in Figure 3.15. The voltage was ramped to its final voltage in 25% increments for the first 4 data points. This was done so that the initial leakage current could be observed carefully. It was observed that there is an initial decrease in leakage current density in region 1. In region 2 the leakage current is approximately constant. In region 3 there is an increase in leakage current corresponding to a significant pre-failure leakage mechanism. In region 4 the leakage current is limited by the measuring circuit and the oxide is said to have failed. The leakage current in the 1st region is attributed to Space-Charge-Limited (SCL) conduction. Following Raghaven [53], the SCL conduction mechanism is described as follows: Ag ions are injected from the metal into the oxide at the metal oxide interface when there is a positive bias at the gate. As more ions are injected into the oxide there is a build up of positive charge that creates a field which opposes further injection. SCL conduction is therefore characterized by an initially high leakage current which drops as the space charge region builds up. When the rate at which ions are injected into the oxide is equal to the rate of electron injection at the Si-oxide

interface the leakage current levels out. The electrons that are injected from the Si-oxide interface neutralize some of the Ag ions, reducing the field in the space charge region, and subsequently allowing for more ion injection from the metal-oxide interface. This corresponds to the beginning of the second region. In the second region the leakage current is limited by the Fowler-Nordheim tunneling of electrons from the Si into the oxide. The third region begins with the onset of a significant pre-failure mechanism similar to that described in section 3.1.4. In the fourth region the leakage current is limited by the measuring circuit. The possible conduction mechanisms have been described in section 3.1.4.

From Figure 3.12, it can be seen that time to failure for Cu-based MOS structures is exponentially dependent upon 1/kT, with a single associated activation energy. However, in the case of Ag-based MOS structures, the data does not suggest a single straight line fit. Median time to failure vs. 1/kT is given in Figure 3.20. This allows for any trends to be more readily seen. Based on the median time to failure, a single activation energy for failure of Cu-based MOS structures in the temperature range of 275 °C to 325 °C of 2.15 ± 0.18 eV is obtained. However, the Ag data suggest two regimes, with the cross-over temperature at 237 °C. In the temperature range of 212 °C to 237 °C the activation energy for failure of Ag-based MOS structures is 2.23 ± 0.12 eV and in the temperature range of 237 °C to 325 °C the activation energy is 0.64 ± 0.06 eV. The activation energy in the 237 °C to 325 °C temperature range is consistent with the evaporated Ag data in that it lies on the best fit line for the activation energy vs. field strength (Figure 3.8) for a field of 1 MV/cm. It is known that Cu diffuses more readily through Si than does Ag. The activation energy for diffusion in Si is 1.6 eV for Ag and 0.43 eV for Cu, and the pre-exponential is 2×10^{-3} (cm^2/s) for Ag and is 4.7×10^{-3} (cm^2/s) for Cu [59]. Diffusivity of Cu and Ag in Si vs. 1/kT is shown in Figure 3.21. It is likely that some Cu would continue to diffuse into the Si beyond the Cu/SiO_2 interface, whereas the Ag would be less prone to do so. Therefore, if the metal build-up at the metal/SiO_2 interface is a significant factor in the failure of the oxide, one would expect the Ag-based MOS structure to have a shorter lifetime, simply because all of the flux through the oxide

would pile up at the interface. Experimental data from J. D. McBrayer indicated the presence of Cu (using RBS) in Si following BTS of Cu-based MOS capacitors, but no Ag was found in the Si following BTS of Ag-based MOS structures [51].

More time to failure data was collected for the Ag-based MOS structures than for the Cu-based MOS structures. This was done because of the larger spread in the Ag data. A Weibull plot of the Ag data for selected temperatures (temperatures for which 8 or more data points were collected) is given in Figure 3.22. The Weibull plot suggests that there are two failure mechanisms for the 250 °C data. This is consistent with the leakage current vs. time data curve of Figure 3.13. Here it appears that 3 of the 7 samples have failed prematurely. The data from the samples that failed prematurely was therefore not used in determining the median time to failure. The nature of the premature failure is unknown, but it is speculated that it could be caused by either rapid diffusion of Ag through pinholes in the oxide, or by punch through of the probe tip directly to the Si through the oxide.

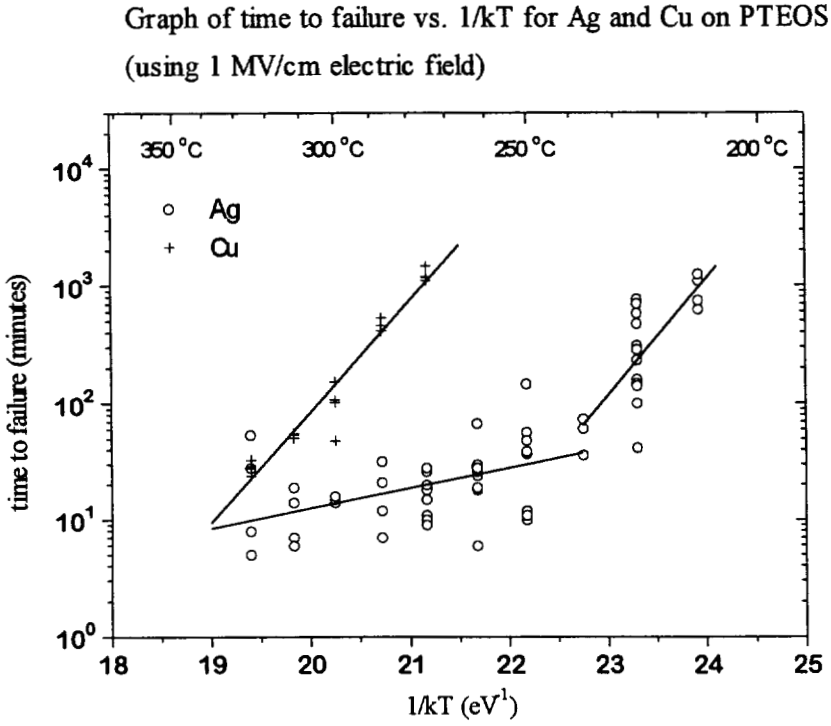


Figure 3.12 Graph of time to failure vs. 1/kT for Ag and Cu (1 MV/cm, 0.5 micron PTEOS)

Table 3.7 Summary of Ag and Cu Data (1 MV/cm Electric Field)

Cu data				Ag data		
Sample #	Temperature	Time to Failure		Sample #	Temperature	Time to Failure
	(C)	(minutes)			(C)	(minutes)
IWD7053	300	155		IWD6077	275	18
IWD7054		103		IWD6078		26
IWD7055		48		IWD6079		28
IWD7056		108		IWD6080		20
IWD7057	325	24		IWD6081	287	7
IWD7058		29		IWD6082		21
IWD7059		33		IWD6083		32
IWD7060		28		IWD6084		12
IWD7061	275	1187		IWD6085	300	14
IWD7062		1479		IWD6086		15
IWD7063		1109		IWD6087		0
IWD7064		1196		IWD6088		16
IWD7065	312	54		IWD6089	312	19
IWD7066		56		IWD6090		14
IWD7067		51		IWD6091		7
IWD7068		0		IWD6092		6
IWD7069	287	462		IWD6093	325	28
IWD7070		0		IWD6094		54
IWD7071		533		IWD6095		8
IWD7072		416		IWD6096		5
				IWD6097	262	68
				IWD6098		24
				IWD6099		6
				IWD6100		18
				IWD6101	250	12
				IWD6102		148
				IWD6103		10
				IWD6104		11
				IWD6105	250	37
				IWD6106		39
				IWD6107		57
				IWD6108		48
				IWD6109	262	26
				IWD6110		30
				IWD6111		19
				IWD6112		28
				IWD6113	275	11
				IWD6114		10
				IWD6115		9
				IWD6116		15
				IWD6117	237	74
				IWD6118		74
				IWD6119		36
				IWD6120		61
				IWD6121	225	762
				IWD6122		582
				IWD6123		473
				IWD6124		236
				IWD6125	225	161
				IWD6126		101
				IWD6127		149
				IWD6128		310
				IWD6129	225	287
				IWD6130		42
				IWD6131		700
				IWD6132		142
				IWD6137	212	1100
				IWD6138		625
				IWD6139		743
				IWD6140		1243

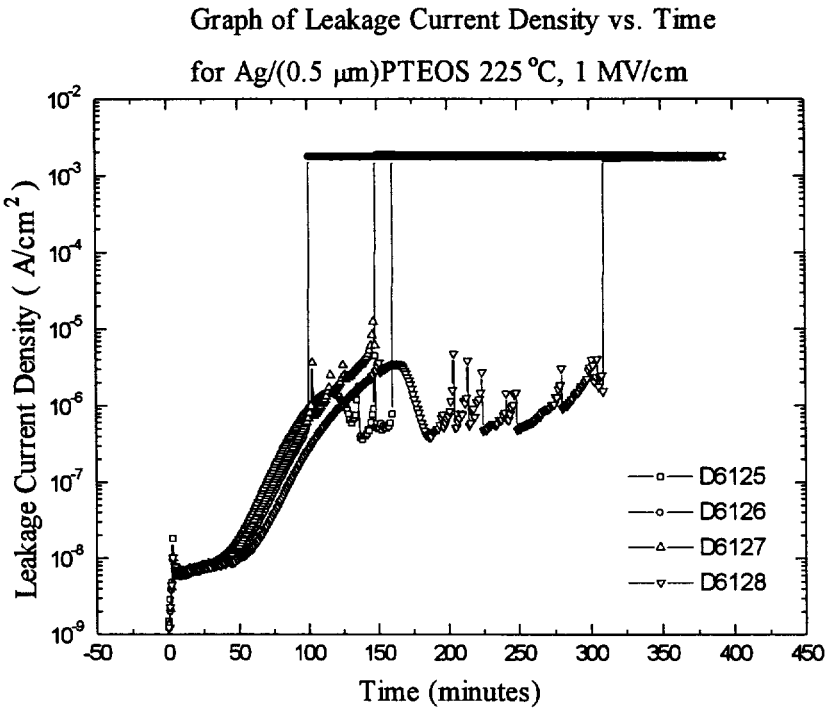


Figure 3.13 Representative leakage current density vs. time curves for Ag/PTEOS (BTS of 225 °C, 1 MV/cm)

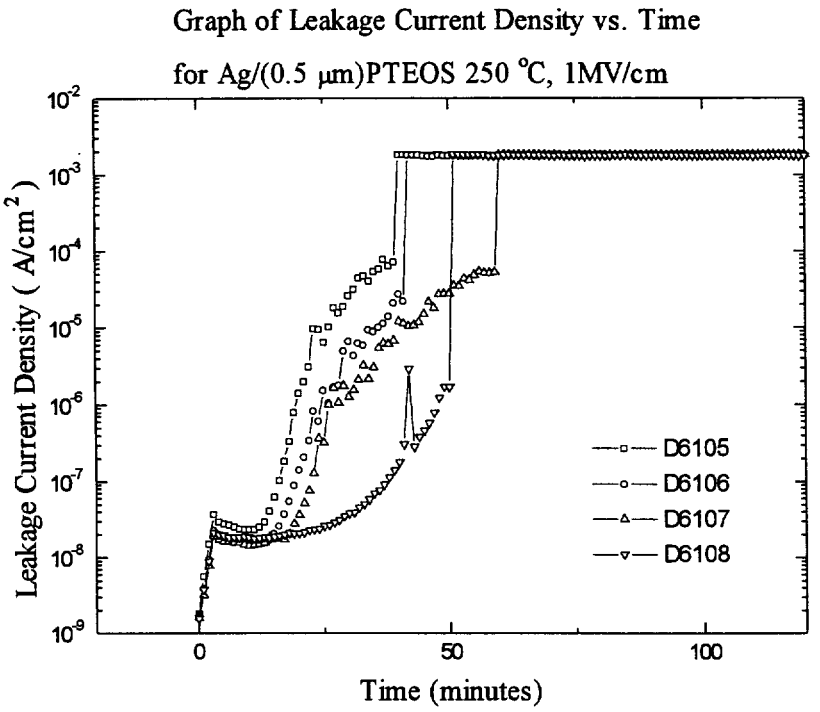


Figure 3.14 Representative leakage current density vs. time curves for Ag/PTEOS (BTS of 250 °C, 1 MV/cm)

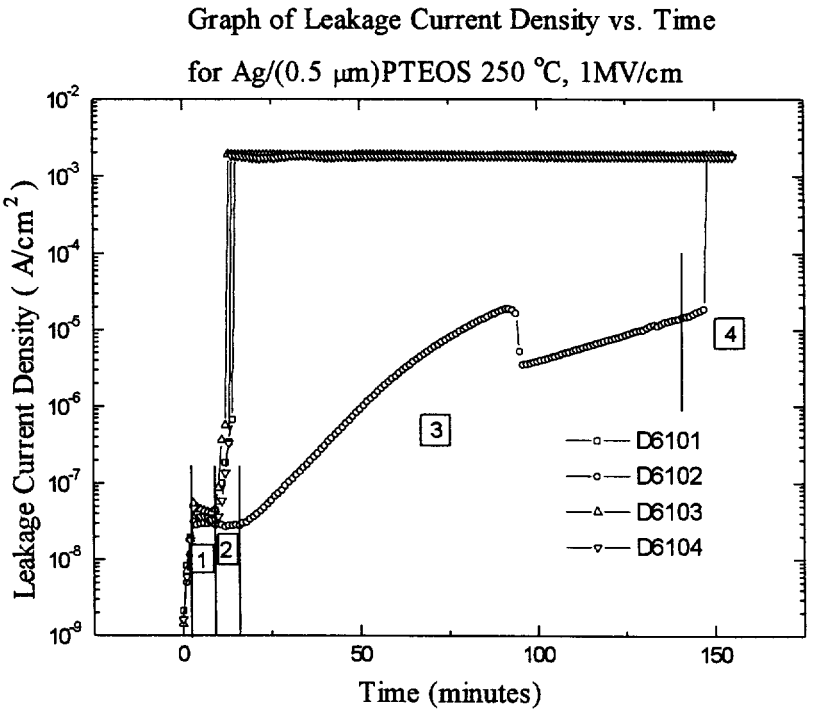


Figure 3.15 Representative leakage current density vs. time curves for Ag/PTEOS (BTS of 250 °C, 1 MV/cm)

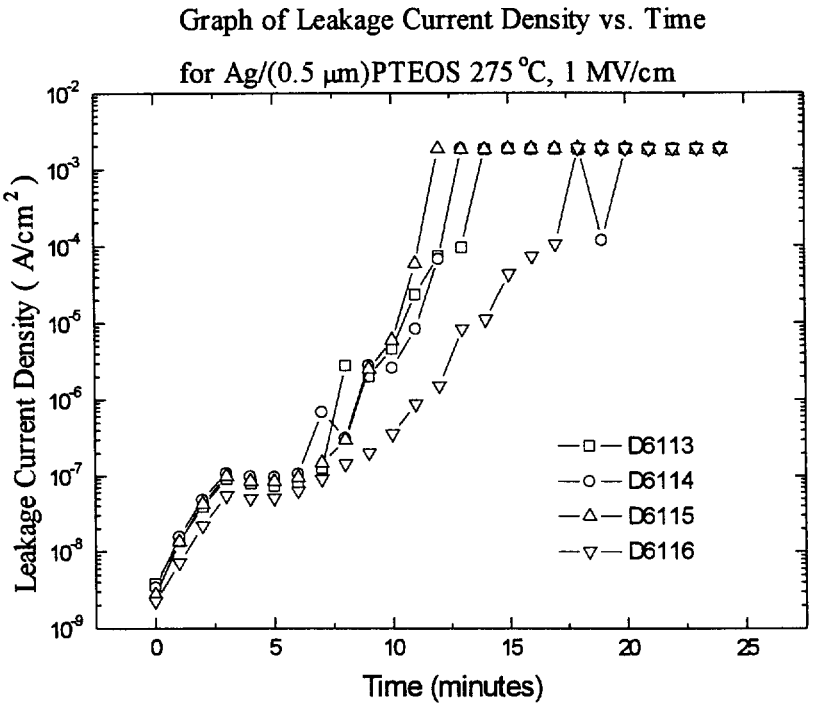


Figure 3.16 Representative leakage current density vs. time curves for Ag/PTEOS (BTS of 275 °C, 1 MV/cm)

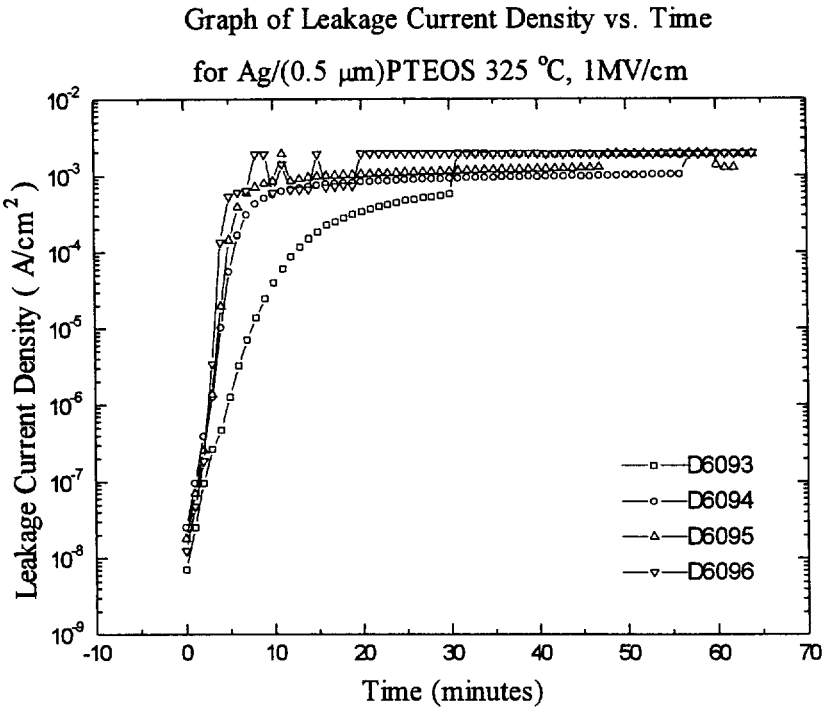


Figure 3.17 Representative leakage current density vs. time curves for Ag/PTEOS (BTS of 325 °C, 1 MV/cm)

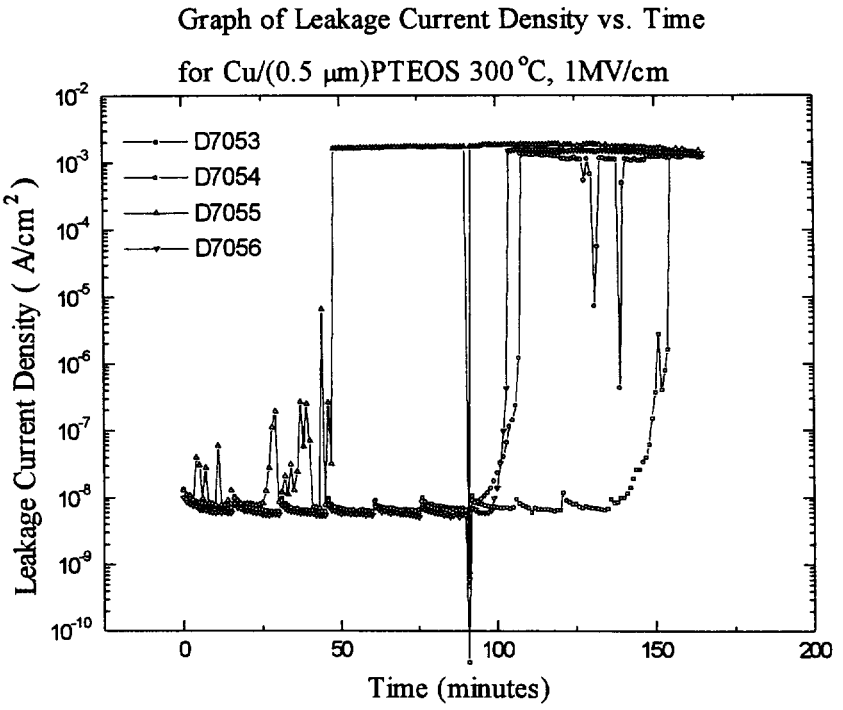


Figure 3.18 Representative leakage current density vs. time curves for Cu/PTEOS (BTS of 300 °C, 1 MV/cm)

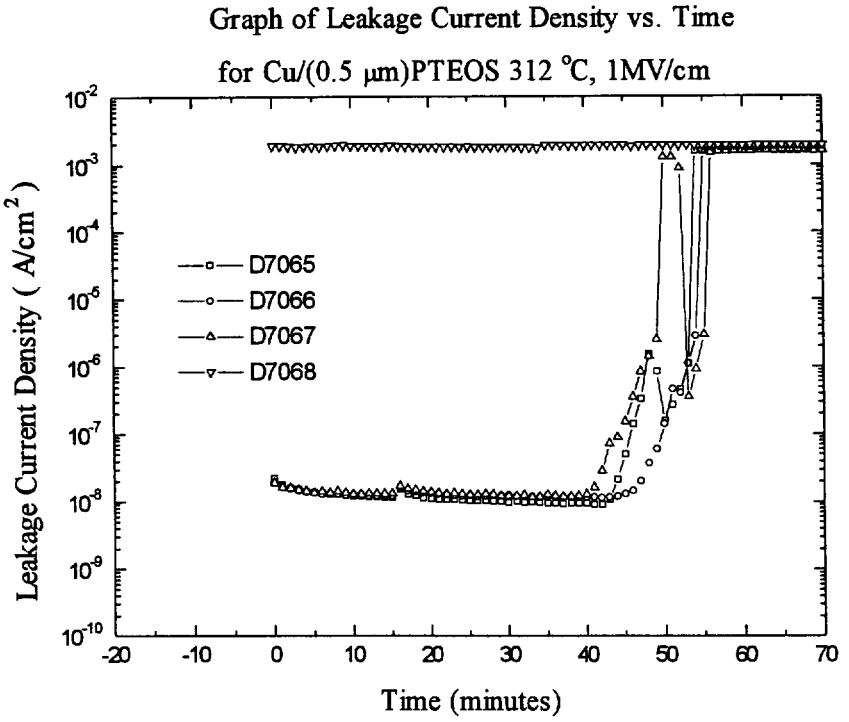


Figure 3.19 Representative leakage current density vs. time curves for Cu/PTEOS (BTS of 312 °C, 1 MV/cm)

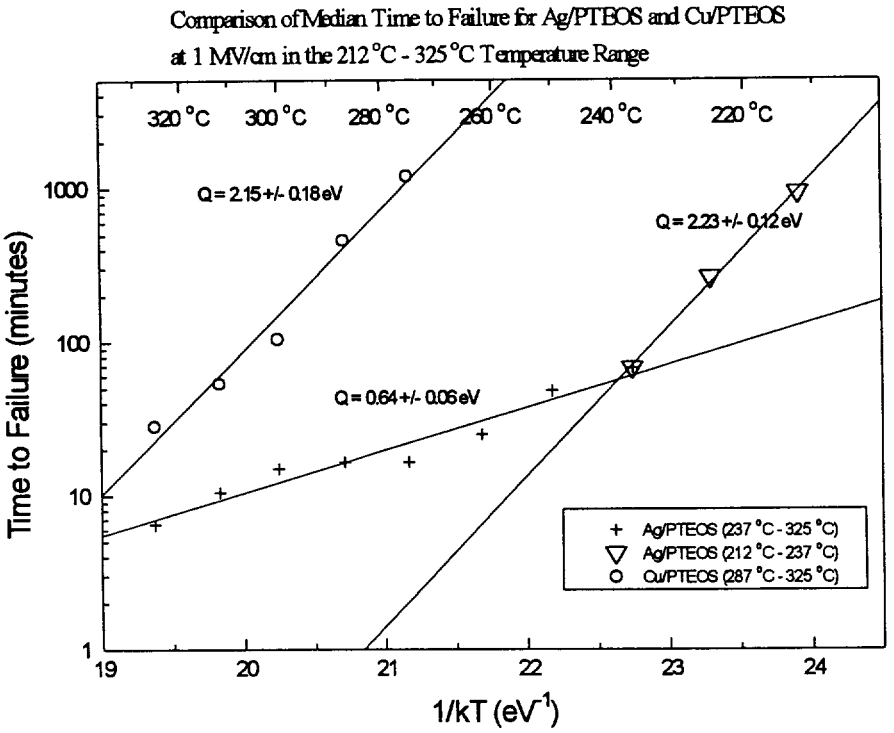


Figure 3.20 Median time to failure vs. 1/kT for Ag/PTEOS and Cu/PTEOS

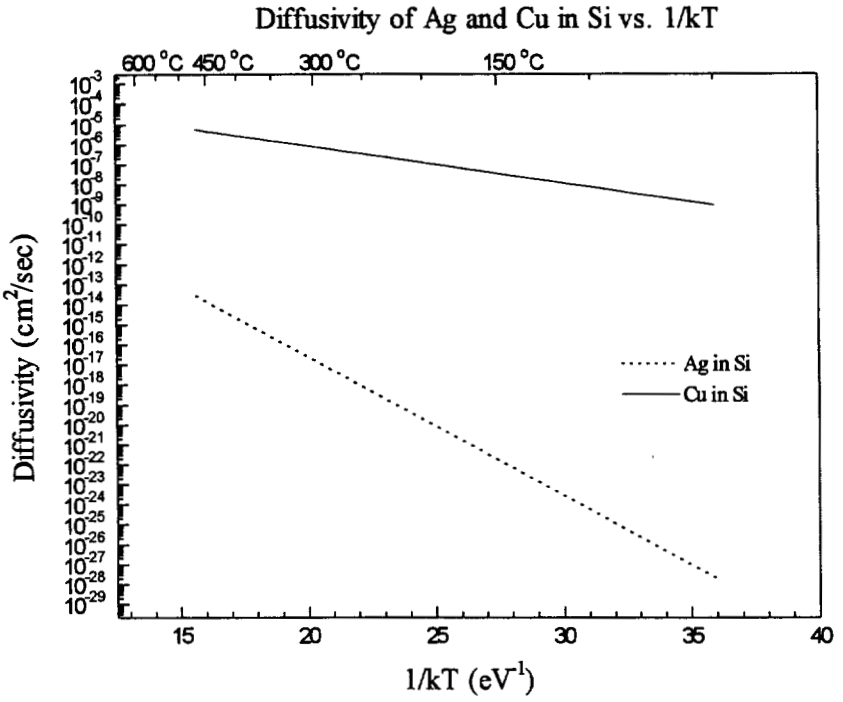


Figure 3.21 Diffusivity of Cu and Ag in Si

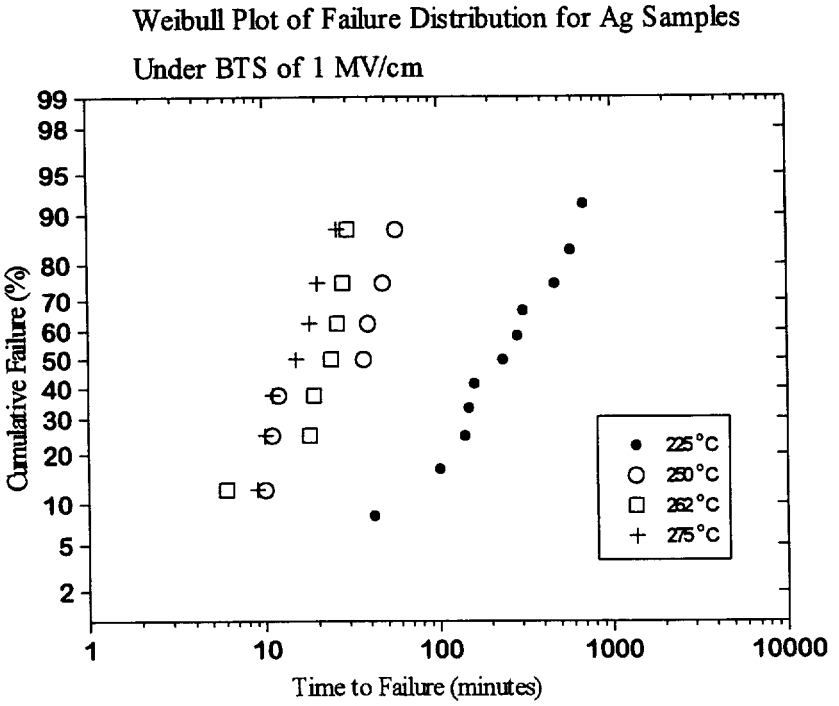


Figure 3.22 Weibull plot of cumulative failure vs. time for Ag-based MOS structures.

3.2 Electromigration of Ag lines

3.2.1 Motivation

Electromigration [EM] in aluminum lines has been a reliability concern since it was first associated with failure of aluminum interconnecting lines in the literature in the late 1960's [66]. Electromigration is the transport of atoms through a conducting metal line resulting from the passage of current through the line. The transport is caused by the direct influence of the electric field and by the momentum exchange between the electrons and the atoms of the host crystal. The latter is sometimes referred to as the bombardment of atoms by the electron wind. Electromigration failure of metal lines is a random process that is described statistically by the well known Black's equation (Eqn. 1.1), which describes the relationship of the mean time to failure of the line in terms of the current density and an activation energy. As outlined in Chapter 1, the trend of scaling down the minimum device dimensions results in increased current density. The effect of device scaling on electromigration induced failure is shown in Table 1.2. Improved electromigration resistance is therefore required of an alternative metallization.

3.2.2 Experimental Outline

The preferred method of measuring electromigration lifetimes involves using a Kelvin structure such as indicated in Figure 3.23. The advantage of this structure over a simple line structure is that by applying a constant current through the line and measuring the voltage drop across the line, a value of line resistance can be determined. This value does not include any contribution due to contact resistance (i.e. the contact resistance between the bond pad and the bond wires). Although the definition of electromigration failure is arbitrary, it is commonplace to define electromigration lifetime as the time taken for the resistance of the line to increase by 30 %. Using such a criteria for failure, it is important that an accurate value of line resistance is obtained.

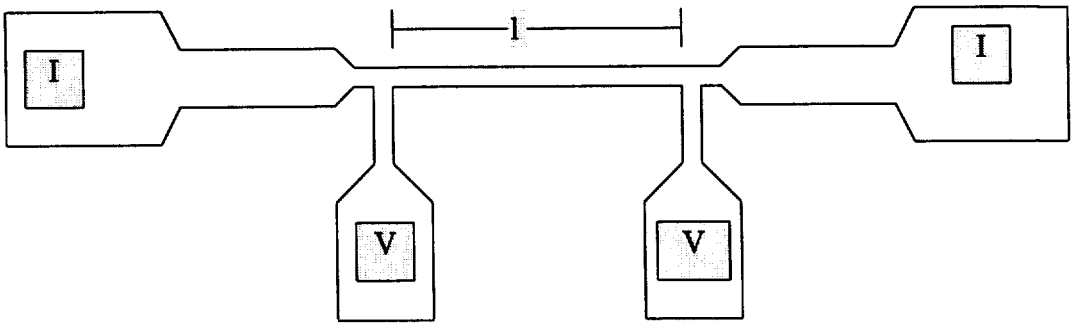


Figure 3.23 Electromigration (EM) test structure

In order to begin electromigration testing, several preliminary steps were required. For making the electromigration device these steps included: identifying a suitable electromigration structure, damascene and passivation of the sample, opening up of the passivation at the bond pads, and making electrical contact from the bond pad to the outside world. For testing the electrical device the steps included, making electrical contact to the circuit and providing a high temperature environment for electrical stressing.

First of all, a testing structure needed to be identified. For observable electromigration to occur the product of line length and current density must exceed a predetermined quantity, which is a function of temperature. This was found by Blech [67]. According to Zhao, "it is now understood that the physical origin of such a threshold current density is the counteracting mass flow induced by inhomogeneities such as gradient of mechanical stress, atomic concentration uniformity, and temperature gradient [68]." The current density must also be sufficiently high that electromigration failure will occur within a reasonable time.

The structure used in the Ag electromigration experiment here was a modified line structure, rather than the ideal Kelvin structure of Figure 3.23. The structure was a common ground loop line that linked many pads and structures. In order to make a single line structure, the line was severed in several places by using a focused ion beam (FIB). Thus a structure like the one shown in Figure 3.24 was obtained. The EM line ran between 2 rows of bond pads, and was connected to the package by wire bonding at the bond pads. The structure was packaged using a standard 400 dip package. The 2 strong black lines in Figure 3.23 indicate the connection from the sample to the package. The numbers correspond to pin numbers on the package. The Ag line used for EM testing is indicated by an arrow. Gold wire was used to make contact with the bond pads to the package. Packaging was required so that several samples could be stressed simultaneously. A 10 μm wide, 2400 μm long line was selected which met the minimum current density requirements under the electromigration stress conditions of 200 °C and

20 $mA/\mu m^2$. The damascene and passivation steps are described in detail in Chapter 2, sections 2.3 and 2.4. Three Al-Cu damascene samples were also prepared for comparison. The Al-Cu EM lines were serpentine structures and no circuit modification by FIB was used. Al-Cu lines were bonded using Al wire bonding. Ag serpentine structures were shorted due to a lithography problem and could not be used. The difference in structure dimensions explains the large difference in line resistance. However, the current density was kept the same for both sample sets.

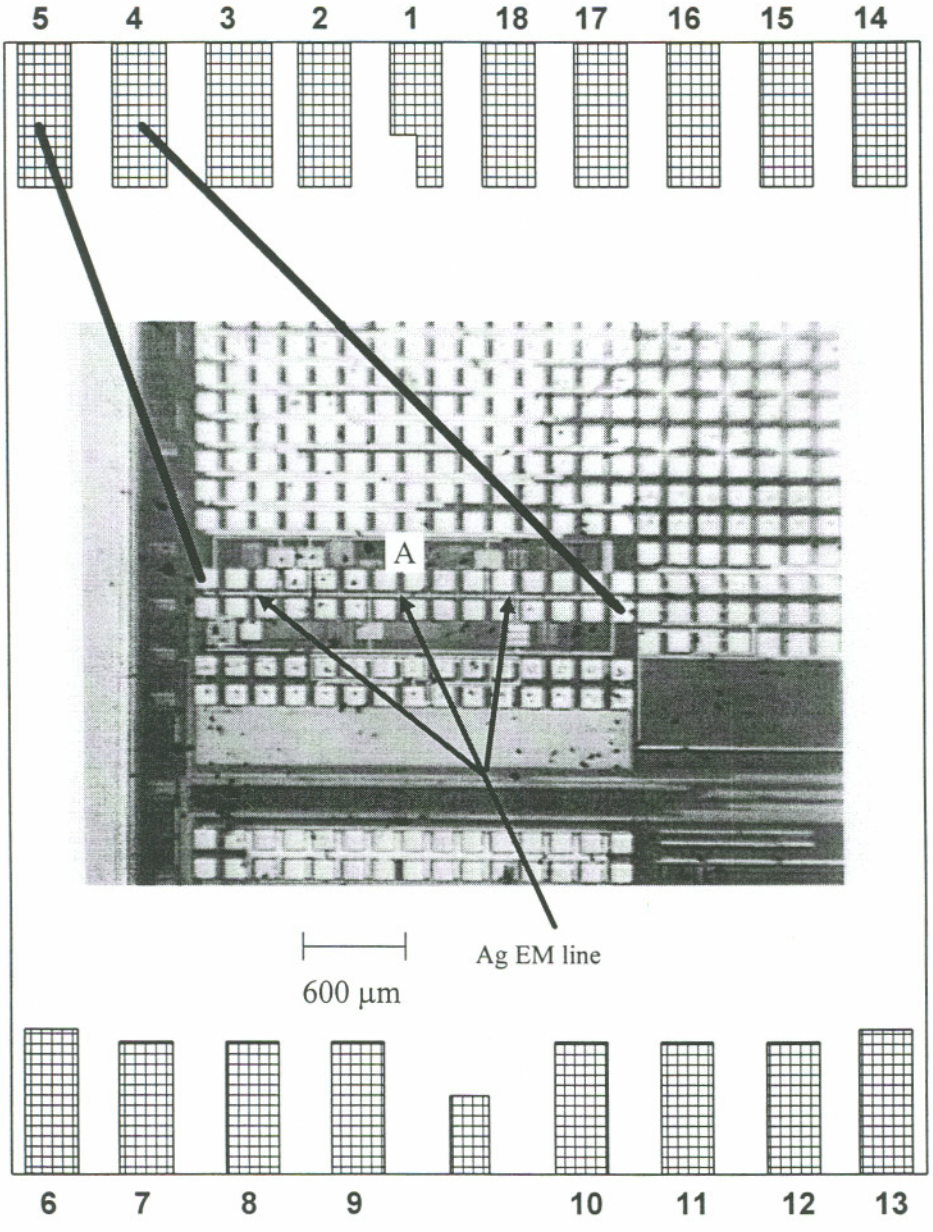


Figure 3.24 Micrograph of the EM test structure

3.2.3 Results

Electromigration curves are shown in Figure 3.25. The Ag and Al-Cu results are summarized in Table 3.7. The sample numbers are given in column 1. Following passivation by sputtered silicon dioxide (section 2.4) and FIB etching of the bond-pad, the line resistance was measured using a micromanipulator probe station. This is given in column 2. The Ag lines were packaged using gold bond wire contacts. The Al-Cu lines were packaged using Al bond wire contacts. (Au rather than Al was selected for the bond wire to Ag based on the work in section 5.2. This work showed that the resistivity of Ag/Al samples increased fourfold after a 2 hour anneal at 500 °C.) The line resistance was then measured using an ohmmeter across the appropriate pins of the package. This is given in column 3. The difference between column 3 and column 2 is therefore the initial contact resistance due to packaging. After the sample was heated to the stress temperature and current, the initial line resistance was measured. The samples were stressed at 200 °C and 20 $mA/\mu m^2$ current density. This corresponds to t = 0 in Figure 3.25. The line resistance for the initial stress conditions (at t = 0) is given in column 4. The line resistance of the packaged sample was measured after EM testing and cool-down. This is shown in column 5. The Ag packages were opened and the line resistance was measured using the micromanipulator probe station. This is shown in column 6. This was only done for the Ag samples. The data from columns 3 and 4 were used to determine the temperature coefficient of resistance (TCR) of the Ag and Al-Cu. This is shown in column 7.

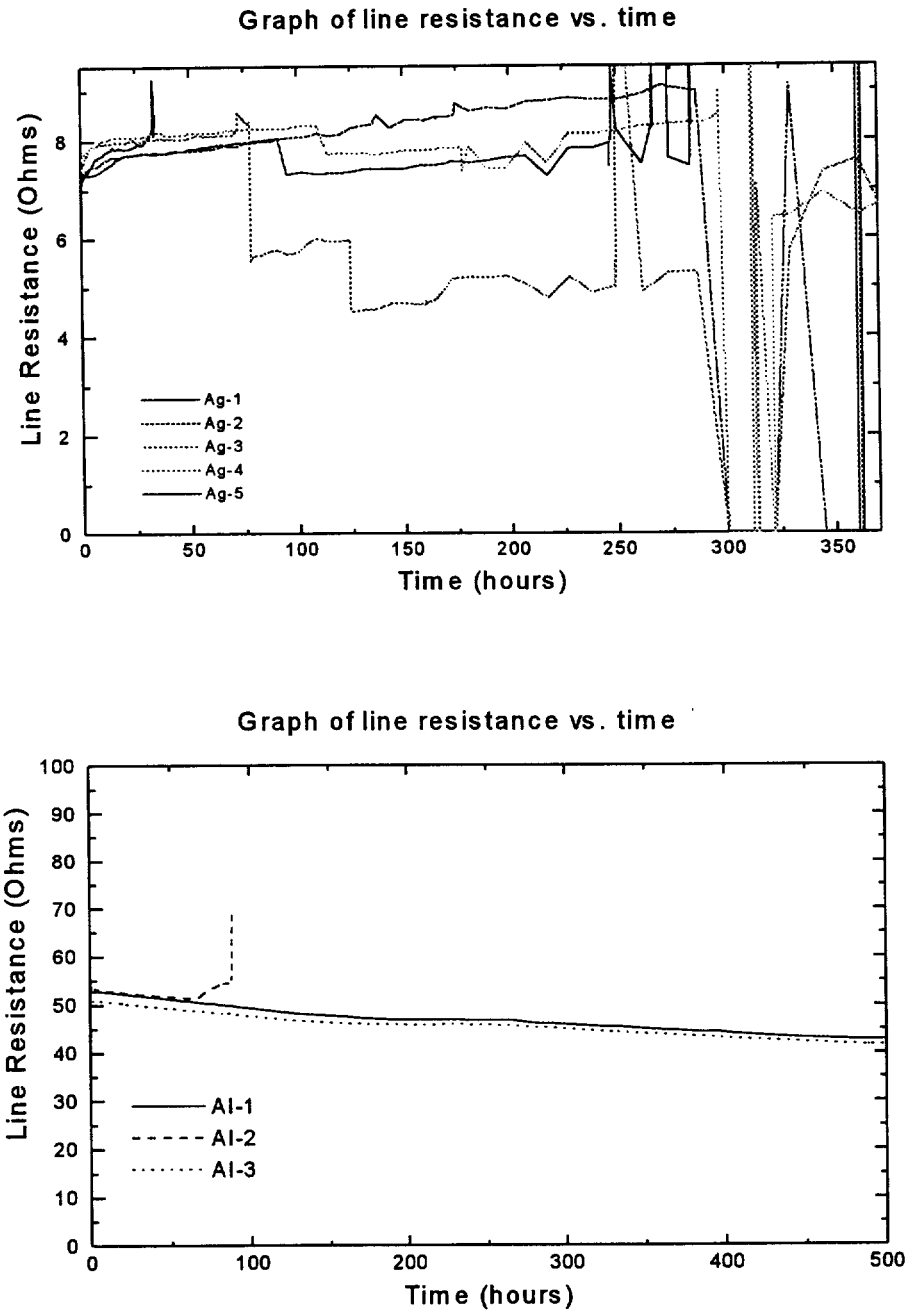


Figure 3.25 a) Ag line resistance data, 200 °C, 20mA/μm^2

b) Al line resistance data, 200 °C, 20mA/μm^2

Table 3.8 Ag and Al-Cu EM data

1	2	3	4	5	6	7
Sample number	Line resistance prior to packaging (Ohms) 20 °C	Line resistance after packaging (Ohms) 20 °C	Initial stressed line resistance (Ohms) 200 °C	Packaged post-EM line resistance (Ohms) 20 °C	Unpack-aged post-EM resistance (Ohms) 20 °C	TCR (times 1,000)
Ag-01	3.70	4.40	7.12	open	-	3.43
Ag-02	4.08	4.63	7.29	open	2.84	3.19
Ag-03	4.13	4.73	7.44	open	4.61	3.18
Ag-04	4.31	4.66	7.63	open	2.90	3.54
Ag-05	4.11	4.58	7.22	open	4.50	3.20
Al-01	29.4	31.8	53.2	24.6	-	3.65
Al-02	30.3	33.1	53.8	open	-	3.47
Al-03	29.4	30.8	51.1	24.2	-	3.66

3.2.4 Discussion

The experiment was not successful in determining electromigration performance of the Ag structures. The measurement of the resistance of the EM lines following removal of the sample from the package indicates that the reason for open circuit failure was loss of contact at the bond pad. It is commonplace to use a pre-specified increase in resistance, nominally 30%, as a failure criteria. However, when a significant portion of the line resistance comes from the contact, and this resistance varies throughout the run, it is not possible to use such a criteria for failure. Since we were unable to eliminate the effect of contact resistance on the total line resistance it is not possible to draw any conclusion about the electromigration performance of the EM lines.

The temperature co-efficient of resistance (TCR) is defined as:

$$\mathrm{TCR} = \frac{R_1 - R_2}{R_T(T_1 - T_2)} \qquad \text{Eqn. 3.7}$$

where $T_1 > T_2$ and R_1, R_2, R_T are the resistance at temperatures T_1, T_2 and T respectively. Using the data in Table 3.7 an estimate of the TCR can be readily determined. T_1 = 200 °C, $T_2 = T$ = 20 °C. Based on the data, averaging the TCR for each sample, the TCR of Al is 0.0036 and the TCR of Ag is 0.0033. The TCR values reported in the literature are approximately 20 % more than what was determined from this data.

The 5 Ag samples were studied after EM stressing using optical microscope, and SEM. Large clumps of material were found in several locations. A representative region which has a large mound of material is shown in Figure 3.26. This shows the EM line structure. The adjacent bondpads can be seen at the edge of the micrographs. This is location A in Figure 3.24. By moving the sample into the focal plane of the microscope, it can be seen that the darkened area is higher than the surrounding material. This suggests that material has been thrust up through the passivating oxide. It can also be readily observed that the oxide is not adhering well to the Ag EM line or the isolated Ag bond pads. Figure 3.27 shows a Ag bond pad with passivating oxide coating. The bond pad is

adjacent to the EM line. The oxide appeared to flake off the pad and there appeared to be voids underneath the oxide. The Ag pad of Figure 3.28 was electrically isolated but there was voiding in both the EM line and the adjacent bond pads. A cross section of the EM line is given in Figure 3.29. The box in the bottom half of the micrograph is from the FIB deposited Pt, which was necessary for charge dissipation during the ion-milling process. It is also observed that there is voiding in the bond pads adjacent to the EM line. This suggests that the voiding is primarily thermally induced. It is possible that thermal effects were enhanced locally due to Joule heating. However, voiding appeared all across the die, indicating a chemical or thermal cause of voiding rather than electromigration.

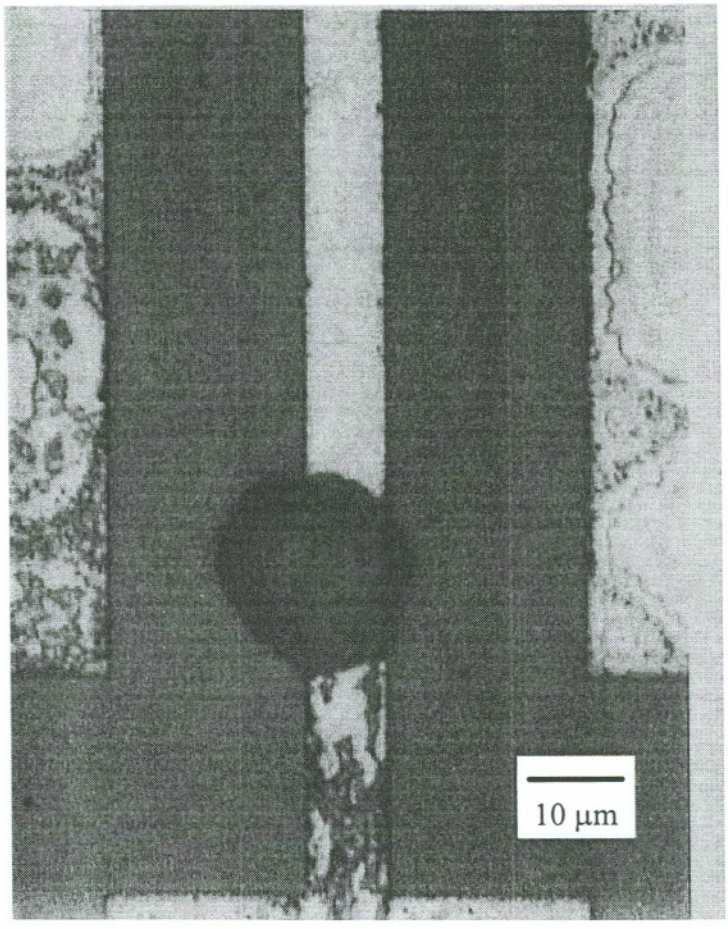


Figure 3.26 Ag protrusion on EM structure

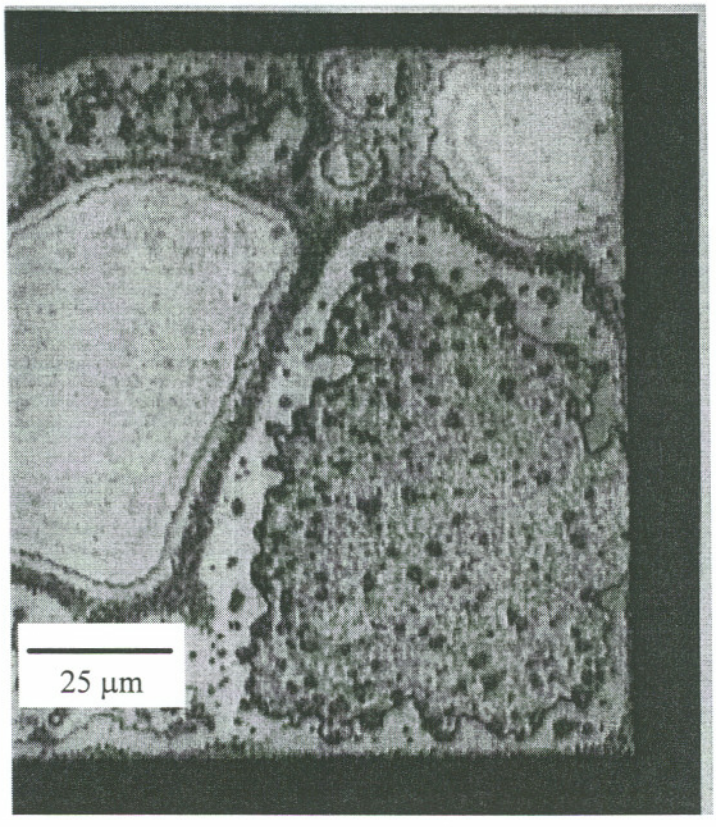


Figure 3.27 Adjacent bondpad to EM structure

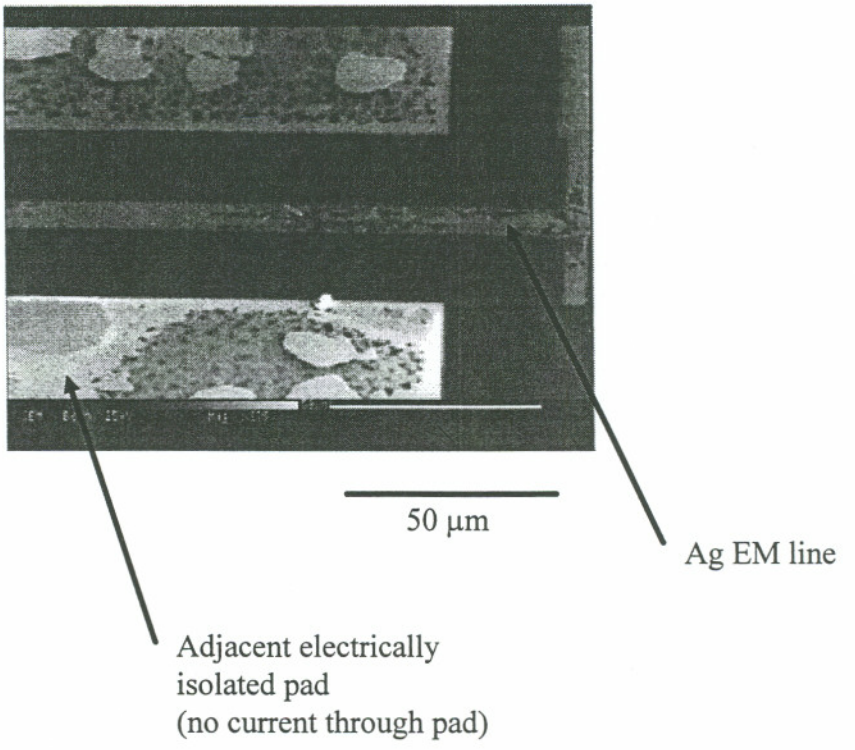
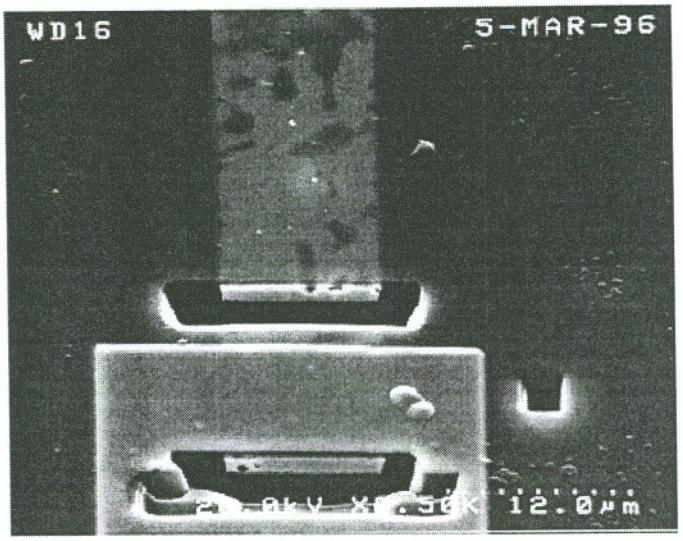


Figure 3.28 Ag EM structure and adjacent bondpads



12.0 µm

Figure 3.29 Cross-section of EM structure

Chapter 4

Realization of a Silver Interconnect Line

4.1 Deposition and Reflow of Silver

The scaling of minimum device dimensions results in increased device density on the chip. Multiple metal layers are needed to connect the devices together. The increased interconnectivity requires the use of multiple metal layers. Levels are connected together by plugs. A plug is formed by etching the inter layer dielectric and filling the resulting via with metal in order to connect to a lower level. Due to the shortage of available space on the chip and the number of levels being connected, high aspect ratio metal plugs are often required. Similar considerations result in an increased demand for interconnect lines that also have high aspect ratios. Metal lines can be made by either depositing blanket metal and subsequent patterning, or by etching lines into the dielectric and depositing metal into the trenches. The latter is referred to as the damascene method. Theses two approaches were discussed in section 1.2.2. For Ag there is no dry etch chemistry available. Therefore the damascene method must be used. The key to the success of the damascene method is the complete filling of the trenches and vias. The potentially available deposition options are; plating, CVD, and sputter deposition.

4.1.1 Deposition of Silver by Plating Techniques

Both Ag and Cu can be deposited by either electroplating or an electroless process. In electroplating, two electrodes, one of which (the cathode) is the sample, are immersed into a plating solution that contains metal ions. A voltage is applied between the electrodes resulting in the plating of the metal on the sample surface [69]. The

electroless process can be considered to be comprised of two simultaneous reactions, one of which is an oxidation reaction which produces electrons and a spontaneous metal reduction which consumes the electrons. Electroless deposition of Ag using formaldehyde, silver sulfate, and aldose solution has been used to deposit near bulk resistivity Ag onto 2 cm^2 samples of Si wafers that had been covered with a TiN barrier [70]. Electroless deposition of Cu for ULSI circuit applications has been reported in the literature [71-77]. Typical resistivity of the deposited Cu films is 2.0 $\mu\Omega$.cm. IBM has also reported copper/polyimide-based interconnect systems for VLSI applications [78-79].

The advantages of plating techniques include the low cost of equipment, low deposition temperature, high quality of the deposited film, and good via and trench fill potential. However, electroplating requires an external current source and a thick uniform seed layer. One of the major concerns with electroplating or electroless deposition is the reliability of the seed layer which is generally required to initiate deposition. The catalytic properties of the seed layer may be lost due to exposure to the atmosphere. Another concern with electroless deposition is that the NaOH or KOH that is sometimes used to control the pH of the solution might introduce Na or K ions at the Si-SiO_2 interface. This could effect the Si device characteristics. Therefore, an electroless deposition process that does not require a seed layer, and that does not use either Na or K based solutions, would be most desirable. Such a process is currently being developed at Oregon Graduate Institute of Science and Technology [80].

4.1.2 Chemical Vapor Deposition of Silver

CVD can provide excellent trench-fill capability that is dependent on factors such as the mean free path of the incoming species, the sticking coefficient, and the surface mobility. Excellent conformal step coverage can occur when reactants adsorb on the surface and migrate along the surface prior to reaction and incorporation into the film. This is the case for TEOS based SiO_2 for example. However, when surface migration is low, the relative thickness at any point on the trench is dependent on the incoming flux distribution and the arrival angle of the incoming species. The incoming flux distribution

will depend on the mean free path and the sticking coefficient (since reflections change the distribution). The arrival angle will depend on the geometry of the trench, specifically the aspect ratio. These concepts are well understood and described in standard VLSI textbooks [81-82]. Poor step coverage has been seen for silane-based films of SiO_2, due to the low surface mobility and high sticking coefficient. CVD Cu is reported to have excellent step coverage due to the very low sticking coefficient (0.015) of the Cu precursor [83]. There has been considerable interest in the chemical vapor deposition of Cu for ULSI applications [84-85]. Plasma assisted CVD (PACVD) of copper films has been reported in the literature to be very successful. Copper films have been deposited with resistivities as low as 1.7 $\mu\Omega$.cm [86]. The interest in CVD Cu has been driven by the anticipation of the eventual introduction of Cu into mainstream ULSI manufacturing. However, CVD of Ag has received considerably less interest, and no articles were found in any of the semiconductor industry related publications. There are no reports on step coverage of Ag films deposited by CVD. The blanket deposition of Ag by PECVD has been reported to yield Ag films with resistivities as low as 2.0 $\mu\Omega$.cm [87]. The deposition rate, which was only 20 Å per minute, has an upper limit based on the onset of gas phase nucleation. Such a deposition rate is unacceptable for high volume manufacturing.

4.1.3 Sputter Deposition of Silver

Sputter deposition has been the fabrication technique of choice for Al-based interconnect lines. Since the sputtering process is so well understood by the semiconductor industry, it is natural that this technique would be examined for low resistivity metal interconnect lines. The use of sputtered Cu for VLSI applications has been reported in the literature [88-89].

One of the key problems of sputter deposition is step coverage. Step coverage is dictated by the incoming flux distribution, the mean free path, the sticking coefficient, the surface diffusion, and preferential re-sputtering effects. The relative deposition rate at any point on the feature depends on the incoming flux and the arrival angle. The latter is

dictated by the geometry of the feature. The former depends on how the material is removed from the target. Generally, the flux distribution leaving a target can be described as a cosine distribution, depending on the incident ion energy [90]. The angular distribution of material sputtered from a point on a polycrystalline surface will have an under-cosine, cosine, or over-cosine distribution for low power, moderate power and high power, respectively [91]. The angular distribution of sputtered atoms from metal targets is well described in the literature [92]. As a result of the flux distribution and geometric shadowing, voids (or tunnels) are formed in the high aspect ratio trenches. There are several models which can be used to predict the conformality of the sputtered metal over any feature. SIMSPUD is a 3D Monte Carlo simulator which provides a detailed description of flux distributions within a PVD system [93]. This information can be used in conjunction with growth simulators such as GROFILMS [94] and SIMBAD [95], to predict the surface and microstructure of the deposited film over a feature [96-99]. The incoming flux distribution can be randomized by collisions. Typical operating pressures for commercial sputtering systems are in the order of. 0.5 Pa, and the mean free path is in the order of 3 cm , which is approximately half the target to substrate spacing [100]. The incoming flux distribution can also be changed by the use of a collimator [101]. This is particularly useful for improving bottom coverage of sputtered barriers for plug-fill applications. A low sticking coefficient favors good step coverage. However, sticking coefficients for sputtered metals are typically in the 0.6 to 1.0 range.

Poor conformality of the deposited film may be lessened during film growth by surface diffusion and re-sputtering. There will be a driving force in favor of diffusion away from areas of positive curvature (convex), toward areas of negative curvature (concave). This will help material to move from the top corners of the trench to the sidewall of the trench thus improving step coverage. The extent to which diffusion occurs will depend on the surface diffusivity, which will in turn depend on the substrate temperature and the condition of the surface. Oxidation of the surface will lower the diffusivity. Conformality can therefore be improved by heating the sample during deposition, and by reducing the residual impurity in the deposition chamber. Another way

in which the conformality may be improved is by surface re-sputtering during deposition. Surface re-sputtering can occur when energetic Ar ions bombard the surface and sputter some of the material that has been deposited. What is interesting about this phenomenon is that the sputter yield is dependent on the ion incident angle with respect to the wafer surface [102]. For Al the maximum ion yield is at an incident angle of about 70 °, and is approximately 2.3 times the yield at normal incidence. Similarly, the maximum ion yield is at an incidence angle of about 60 ° for Ag and is about 1.3 times the yield at normal incidence. If the incident ion flux is normal to the substrate, there will be a preferential etch at the corner of the trench where the breadloafing occurs. By controlling the etch-to-deposition rate at the top corner of the trench it is possible to improve the conformality of high aspect ratio trenches. This simultaneous "dep and etch" technique has been used to fill high aspect ratio (3:1) trenches in volume manufacturing in a commercial high density plasma reactor for CVD of SiO_2 [103-104].

In sputter deposition of metals, the impinging Ar can be incorporated into the film, thus lowering the film purity and resistivity. The problem of Ar incorporation can be overcome by a technique known as sustained self-sputtering [105-108]. In this technique metal is sputtered using ions of the same element, although the plasma is initially struck using Ar. Both Cu and Ag are good candidates for this technique because they each have a high self-sputtering yield [106].

4.1.4 Post-deposition Reflow of Silver

Once deposition is complete, an additional thermal step known as reflow is used to completely fill the trenches. Post-deposition reflow techniques have been used successfully in Al-based metallization for planarization and complete trench and via filling [109]. Diffusion can occur by surface diffusion, bulk diffusion or grain boundary diffusion. At lower temperatures surface diffusion is the dominant mechanism [99].

4.2 Deposition and Reflow Experiments with Ag

4.2.1 Experimental Outline

The experiment was broken into two parts. Trenches were processed onto wafers so that the initial fill and reflow characteristics of sputter-deposited Ag could be studied. In the first part of the experiment a matrix of adhesion and capping layers was used. The Ag film target thickness was 1.0 μm. Adhesion and capping layer nominal thickness was 40 nm. The Ti/TiN composite adhesion layer was comprised of a 5 nm Ti layer sequentially deposited onto a 40 nm TiN layer. The initial fill was examined by cross-sectional SEM. Samples were subsequently annealed in forming gas (5% H_2 and 95 % N_2) at 500 °C for 2 hours. Cross-sectional SEM was used again to determine the effect of the anneal on the topography of the samples. In the second part of the experiment 2.0 μm of Ag was deposited onto a Ti adhesion layer of 25 nm target thickness. No capping layer was used. This was motivated by the results of the first part of the experiment. The deposition conditions and further experimental details were described in Chapter 2, sections 2.2.3 and 2.2.4.

4.2.2 Experimental Results: First Batch

Representative scanning electron micrographs are given in Figures 4.1 - 4.5. The sample structures are summarized in Table 4.1, column 2. SEM micrographs for annealed samples are shown in Figures 4.6 - 4.15. Step coverage can be described quantitatively by measuring the deposition at the sidewall at a distance of half the trench height from the bottom of the trench, and dividing this by the thickness measured at the top surface. As-deposited step coverage for 0.4 micron wide, 0.6 micron deep trenches is shown in Table 4.1, column 3. Step coverage after anneal is shown in Table 4.1, column 4. Agglomeration was observed along the sidewall of several samples after anneal.

Table 4.1 Step-coverage of samples before and after anneal

1	2	3	4	5
Sample ID	Recipe (cap/Ag/adhesion)	as deposited step coverage	annealed step coverage	figure
KV1	Ti/Ag//TiN	0.05	agglomeration	4.15
KV2	Ti/Ag/Ti//TiN	0.05	agglomeration	
KV3	TiW/Ag/Ti//TiN	0.05	0-0.05 agglomeration	4.4, 4.12, 4.13
KV4	Ti/Ag/TiN	0.05	agglomeration	4.1, 4.8, 4.11, 4.14
KV5	Ag	0.05	0-1	4.3, 4.7
KV6	TiW/Ag/TiW	0.05	0.05	4.2, 4.6
KV7	TiW/Ag/TiW	0.05	0.05	4.5, 4.9, 4.10

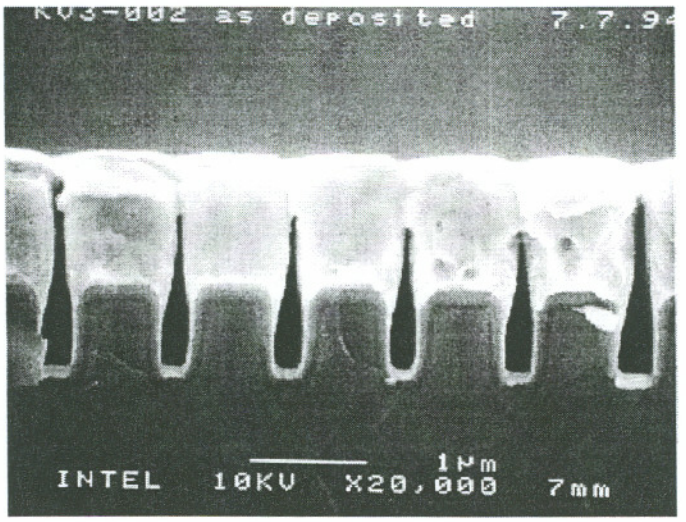


Figure 4.1 Sample KV3-002 as deposited (TiW/Ag/Ti//TiN//oxide)

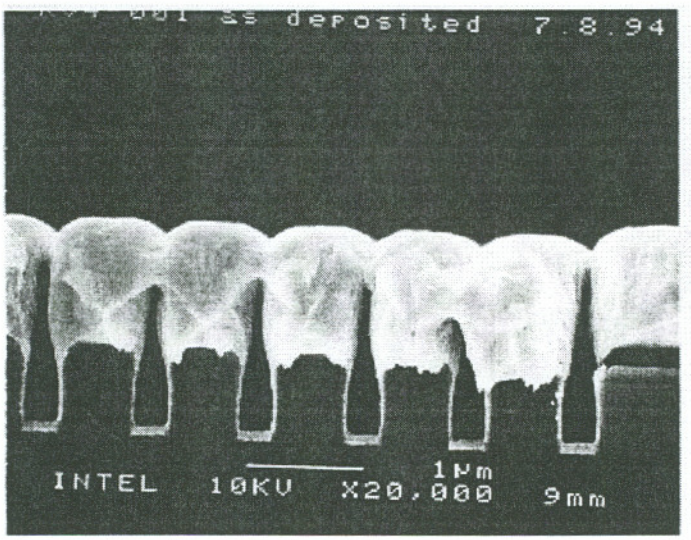


Figure 4.2 Sample KV4-001 as deposited (Ti/Ag/TiN//oxide)

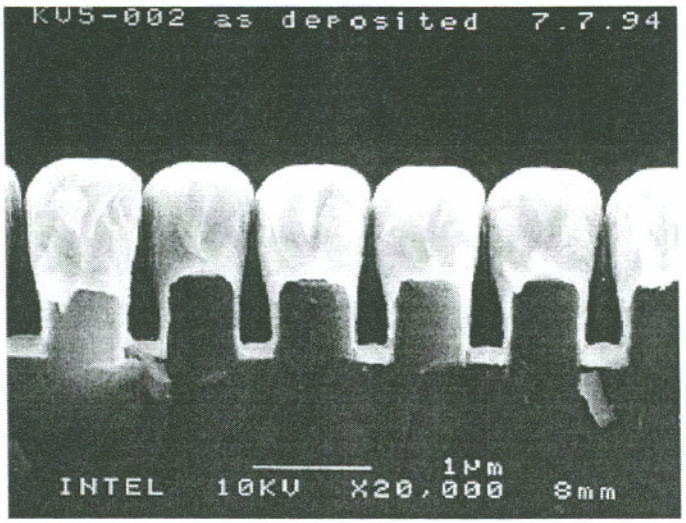


Figure 4.3 Sample KV5 as deposited (Ag//oxide)

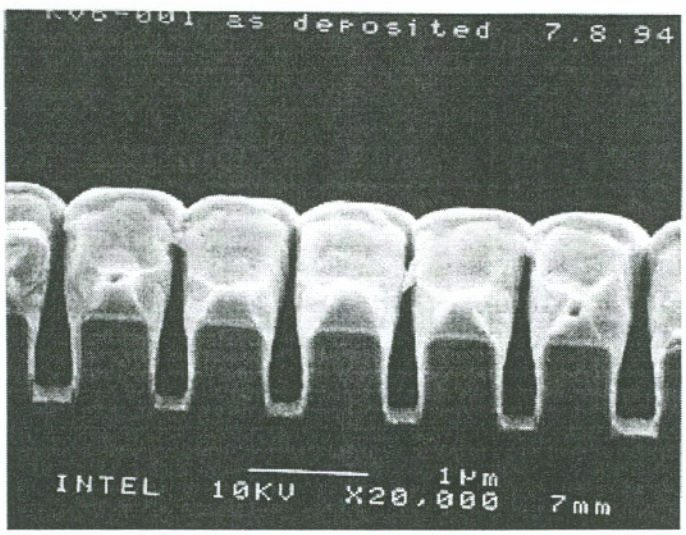


Figure 4.4 Sample KV6 as deposited (TiW/Ag/TiW//oxide)

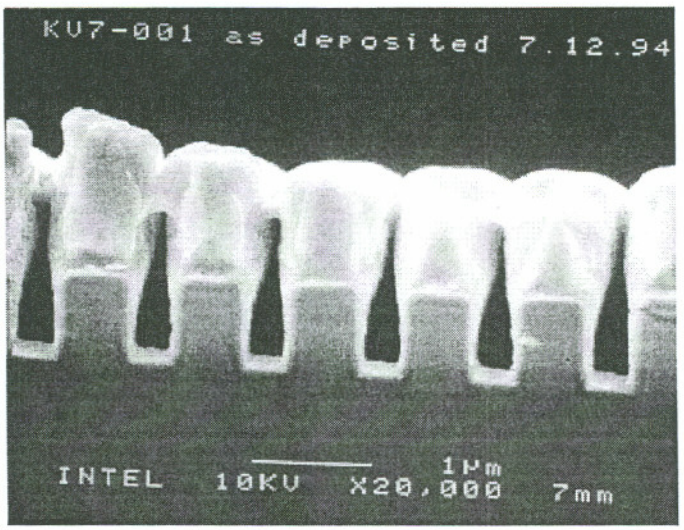


Figure 4.5 Sample KV7-001 as deposited (TiW/Ag/TiW//oxide)

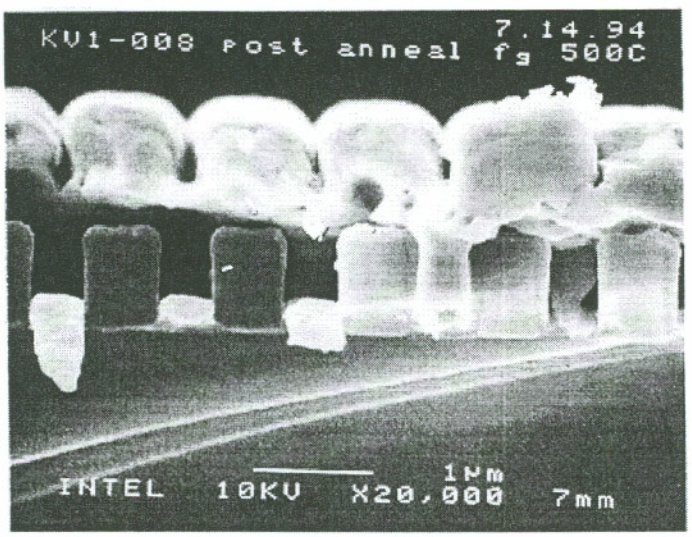


Figure 4.6 Sample KV1-008 annealed (Ti/Ag//TiN)

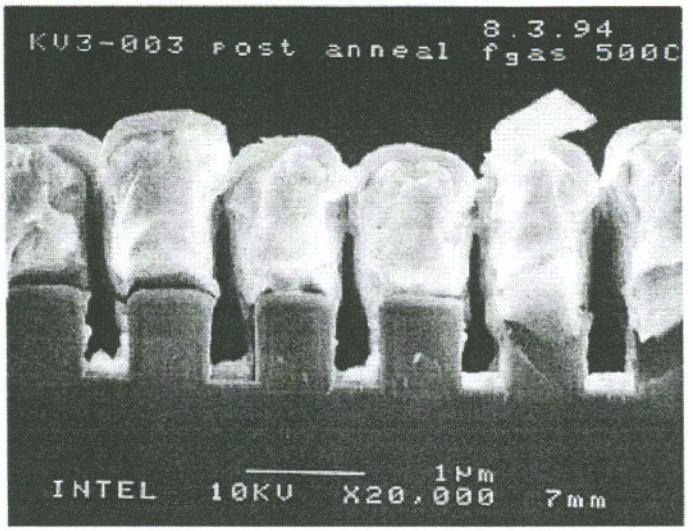


Figure 4.7 Sample KV3-008 annealed (TiW/Ag/Ti//TiN//oxide)

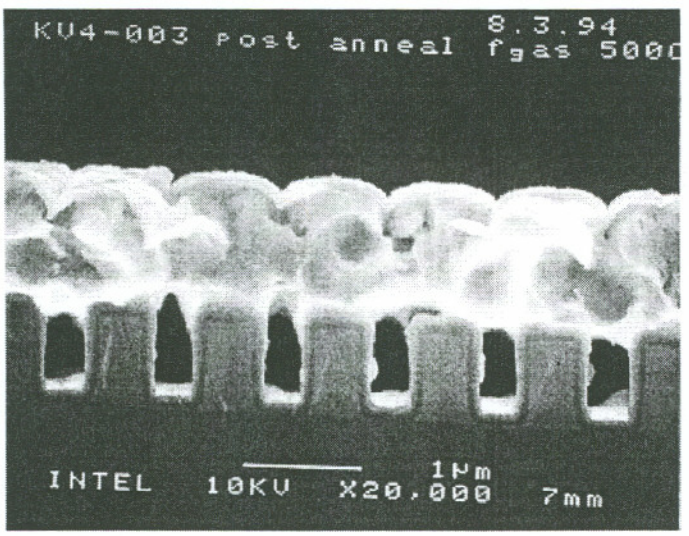


Figure 4.8 Sample KV4-003 annealed (Ti/Ag/TiN//oxide)

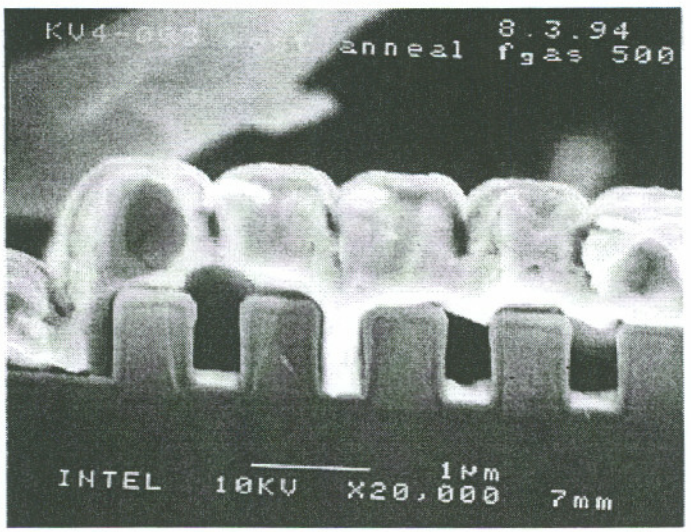


Figure 4.9 Sample KV4-003 annealed (Ti/Ag/TiN)

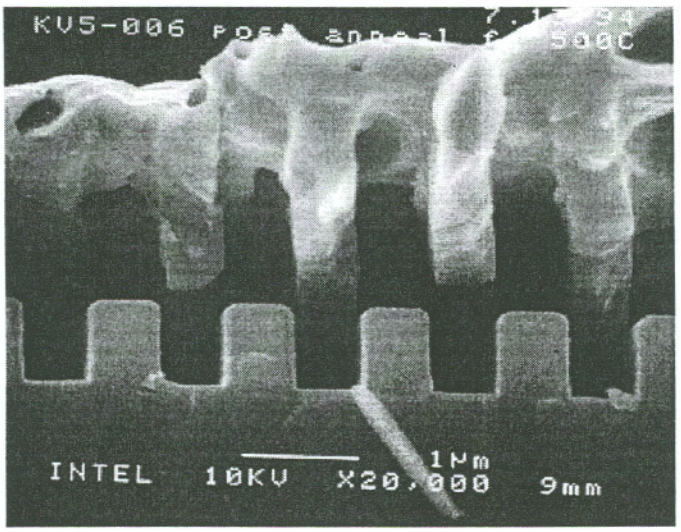


Figure 4.10 Sample KV5-006 annealed (Ag//oxide)

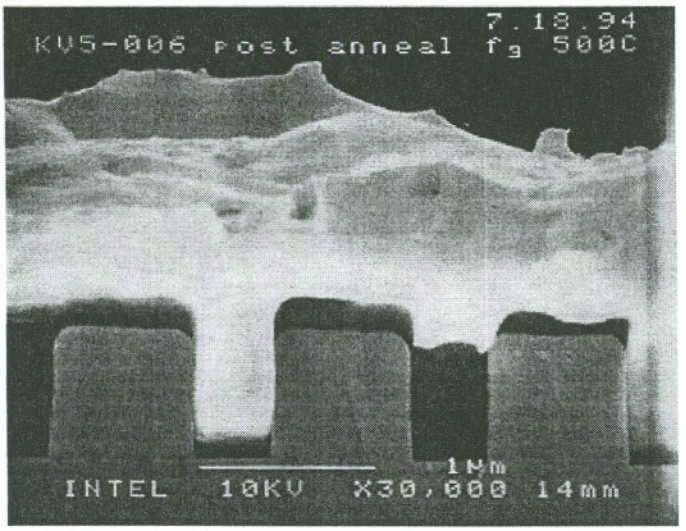


Figure 4.11 Sample KV5-006 annealed (Ag//oxide)

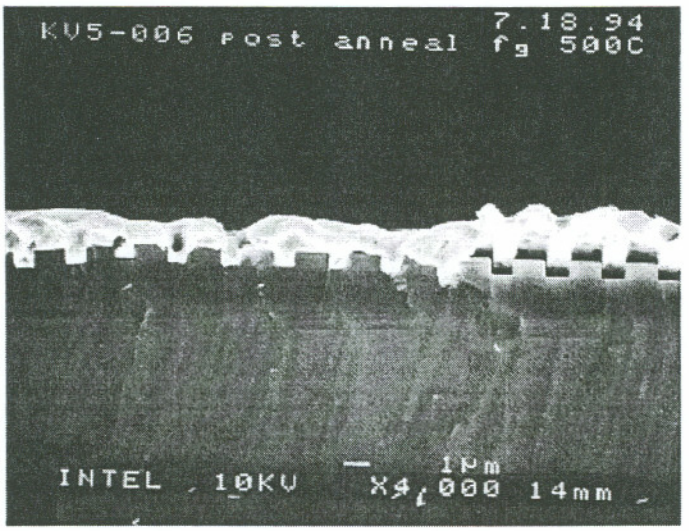


Figure 4.12 Sample KV5-006 annealed (Ag//oxide)

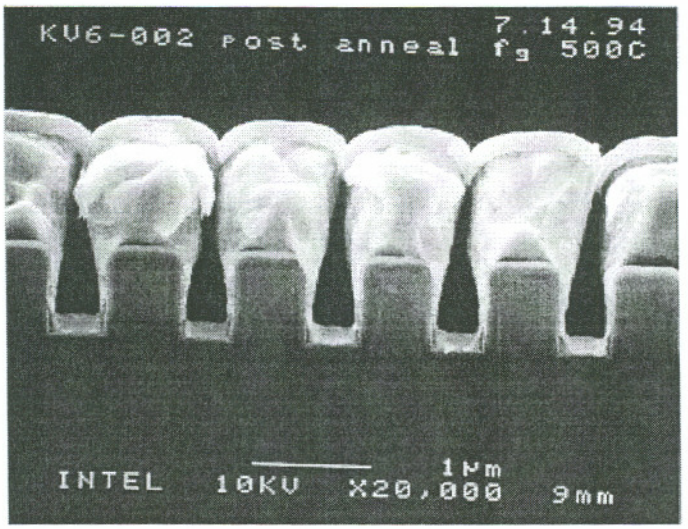


Figure 4.13 Sample KV6-002 annealed (TiW/Ag/TiW//oxide)

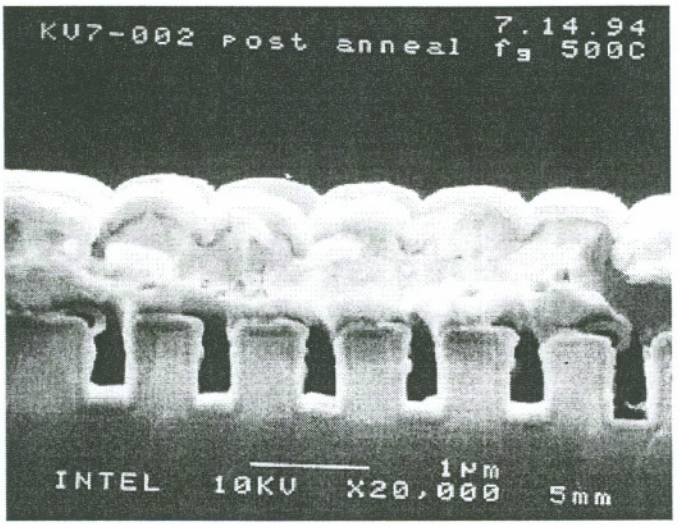


Figure 4.14 Sample KV7-002 annealed (TiW/Ag/TiW//oxide)

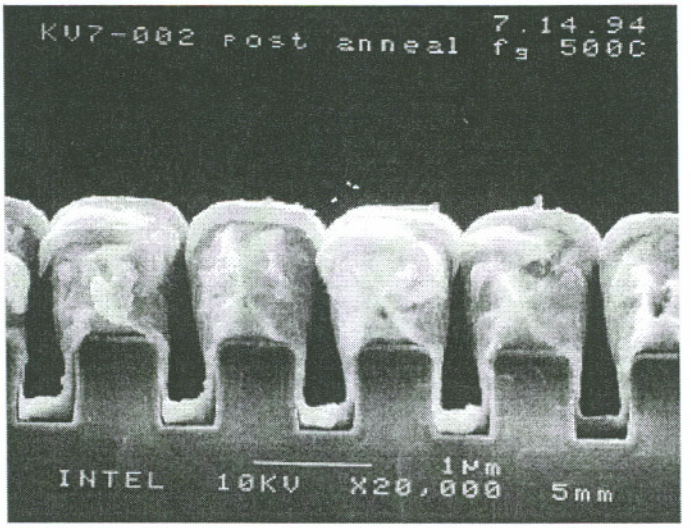


Figure 4.15 Sample KV7-002 annealed (TiW/Ag/TiW//oxide)

4.2.3 Experimental Analysis: First Batch

Figures 4.1 - 4.5 show that the as-deposited sidewall coverage, approximately 5%, is extremely poor for all samples, regardless of the choice of barrier layer. Several factors contribute to the quality of the as-deposited film. These include the substrate temperature during deposition, process conditions, and geometry of the sputtering system. The breadloafing effect can be reduced by increasing the surface mobility of the depositing species, and by reducing the deposition rate. Substrate bias and heating will increase the surface mobility of the depositing species, resulting in better step coverage. Step coverage of the as-deposited samples was poor. Subsequent annealing of the samples did not generally result in filled trenches. There are primarily two reasons for this. The first reason is that the use of a capping layer prevented the surface migration of Ag. The KV5 wafer was the only one for which Ag was deposited without a capping layer. Sample KV5-002 is the only sample that showed a significant change in post-anneal topography. Cross-section SEM micrographs of KV5-002 are shown in Figures 4.10 - 4.12. An adhesion layer was not used in the KV5 samples. The snap cleave process caused separation of the Ag from the underlaying oxide film. This can be seen most clearly in Figure 4.11. The second reason for poor reflow is that many samples were completely pinched at the top. Under the condition that a key-hole void has not formed, surface diffusion will drive material in the direction that will lead to planarization. However, in the event that a key-hole void has occurred, surface diffusion cannot fill the hole. Filling of the void must therefore occur by grain boundary diffusion or volume diffusion. SEM micrographs are shown from samples that were annealed in forming gas at 500 °C. Samples were also annealed in UHV at 500 °C, and in forming gas at 600 °C. Similar results were obtained for the other annealed samples, hence they will not be shown here. Figures 4.6 - 4.15 show that sidewall coverage was often less after anneal. The trenches shown in Figures 4.6 - 4.15 are representative of the many SEM micrographs that were taken. However, for almost each type of composite structure (Table 4.1 column 2), there was at least 1 trench that showed good fill alongside unfilled trenches. Some examples of

micrographs that indicated good reflow in at least one trench are given in Figures 4.6 and 4.9. Reflow as a means to provide voidless filling of topography has been successfully demonstrated for Cu [88-89]. Agglomeration can easily occur when the deposition on the sidewall is very thin. This results in a discontinuity of the metal film that prevents reflow from occurring.

Based on the results of the first batch it was concluded that the use of a capping layer prevented the surface migration of Ag which was necessary for the filling of the trenches. It was also concluded that an adhesion layer was needed between SiO_2 and Ag based on the lifting that occurred when KV5 samples were snap cleaved for SEM cross-sectioning.

4.2.4 Experimental Results: Second Batch

A metal stack using a Ti barrier and no capping layer was selected for the reflow experiments. Due to a processing error in either the etch or lithography steps, the trenches were wider at the top. The as-deposited and post anneal samples are shown in Figures 4.16 and 4.17 respectively.

4.2.5 Experimental Analysis: Second Batch

The micrographs clearly show far better sidewall coverage in the as-deposited sample than for the samples of the first batch. However, the tapering of the sidewall offered a considerable advantage for initial fill. What is important from this result, is that it shows that reflow of Ag can occur at relatively low temperatures providing that there is sufficient initial sidewall coverage. The reflow time however is 10 hours. This is far too long for any commercial application. No experiments were done to determine the reflow window. These samples were subsequently polished to realize sub-micron Ag damascene interconnect lines.

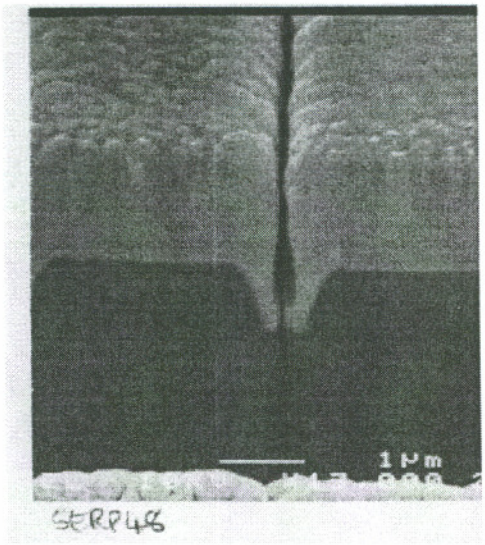


Figure 4.16 As deposited Ag

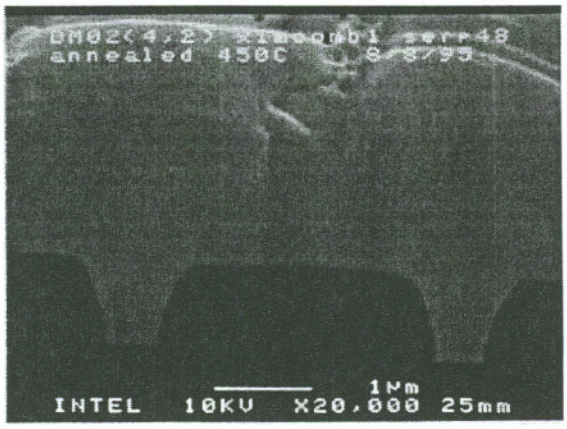


Figure 4.17 Annealed Ag

4.3 Silver Interconnect Line Experiments

The Ag samples from the second batch of reflow experiments (section 4.2.4) were polished following reflow. The Ag damascene lines were not passivated after polishing. The effective resistivity of the lines were compared to that of damascene Al-Cu lines.

4.3.1 Experimental Outline

Al-Cu damascene structures using a Ti wetting layer were fabricated at Intel. The structures consisted of oxide encapsulated Al-Cu based interconnect lines. The length of the lines was 3.2×10^{-2} cm. An SEM micrograph of a cross-section of the structure prepared by FIB is shown in Figure 4.18. (The SEM settings required to obtain resolution of the $TiAl_3$ from the Al-Cu resulted in a loss of overall picture quality.) The reacted $TiAl_3$ layer can be seen along the sidewalls and bottom of the trench.

Four Ag samples were fabricated by polishing samples from batch 2. Following anneal in a nitrogen furnace at 450 °C for 10 hours the samples were polished using an Ultra Test Lapping tool. Samples were mechanically polished on a slurry wheel which was rotated at a speed of 80 rpm using 0.05 μm Beuler™ alumina slurry. Polish rate was monitored from measurements of the sheet resistance, made by using a 4-point probe. Electrical measurements on both Al damascene and Ag damascene structures was made using a Micromanipulator probe station. The resistance was determined by measuring the voltage drop across the line. A constant current source was used across the line.

4.3.2 Results

A cross-sectional micrograph of a Ag damascene structure is shown in Figure 4.19. Electrical measurements were made on one Al damascene and 4 Ag damascene structures. The data is given in Table 4.2. The cross-sectional area of each line was determined from SEM micrographs. NIST standard lines were used as a calibration standard. Based on the line resistance and cross-sectional area measurements, an effective line resistivity for each stack was determined.

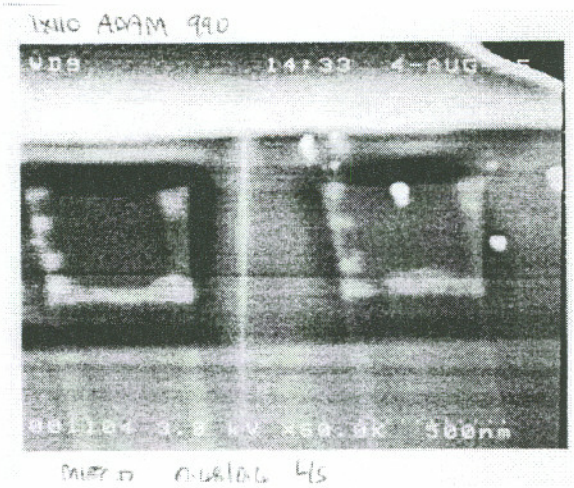


Figure 4.18 Al-Cu damascene structure

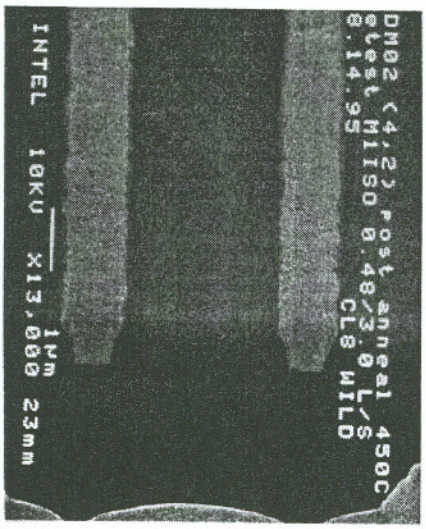


Figure 4.19 Ag damascene structure

Table 4.2 Line Resistance and Effective Resistivity

Sample	Barrier	line resistance (Ohms)	cross-sectional area (cm^2)	effective resistivity ($\mu\Omega$.cm)
Ag	Ti	5.38	1.34×10^{-8}	2.25
Ag	Ti	5.80	1.40×10^{-8}	2.53
Ag	Ti	5.88	1.27×10^{-8}	2.34
Ag	Ti	1.76	3.58×10^{-8}	1.97
Al-Cu(0.5%)	Ti	25.9	0.69×10^{-8}	5.66

4.3.3 Experimental Analysis

The SEM micrograph showed some surface roughening. It is possible that the use of chemical-mechanical polishing may result in a smoother surface. CMP with alumina-based acid slurry has been used to realize Cu interconnect structures [110-111].

The effective line resistivity for the Al was 5.66 $\mu\Omega$.cm. The cross-sectional area micrograph indicates that only 54% of the line is Al-Cu, with the remainder being $TiAl_3$. The resistivity of Al-Cu is around 3 $\mu\Omega$.cm, and the resistivity of $TiAl_3$ is 19 $\mu\Omega$.cm. Using these values an estimate can be made of what the effective resistivity should be using:

$$\rho_{eff} = \frac{1}{\frac{A_1}{\rho_1} + \frac{A_2}{\rho_2}} \left(A_1 + A_2\right) \qquad \text{Eqn. 4.1}$$

where ρ_{eff} is the effective resistivity of the interconnect, A_1 and ρ_1 are the cross-sectional area and resistivity of the $TiAl_3$ respectively, and A_2 and ρ_2 are the cross-sectional area and

resistivity of the Al respectively. Based on the measured cross-sectional area and the assumed values of resistivity for both metal films, the effective resistivity is predicted to be 4.9 μΩ.cm. This is in reasonable agreement to the measured effective resistivity of 5.66 μΩ.cm. Ti is used in the Al-based metallization scheme for 2 reasons. One reason is that it provides a wetting layer for Al reflow. The second reason is that $TiAl_3$ provides a shunt should the Al fail locally due to electromigration. An alternative conduction path would be available to prevent open circuit failure. Although this is a higher resistance path, the total increase in line resistance is negligible assuming the void dimension is small compared to the length of the line. The requirement of the shunt later highlights the importance of the electromigration performance. There is an increase in the line resistance due to the requirement that a shunt layer is used to address the electromigration reliability concern. However, in the case of both Cu and Ag, the integrity of the IMD could be compromised by diffusion into the dielectric. This integrity concern is addressed by the use of a diffusion barrier. The use of either a shunt layer or a diffusion barrier layer would therefore result in increased line resistance. The line resistance increase for the Al-based structure due to the chemical reaction of Al with Ti is considerable. The use of the $TiAl_3$ shunt layer, whilst providing improved reliability, therefore results in a significant loss of performance. For this reason, the Ag damascene structure that uses a Ta barrier offers a considerable performance advantage over Al-based damascene that utilizes a Ti wetting layer (see Appendix 1).

CHAPTER 5
BARRIER DESIGN

5.1 Barrier Design Overview

5.1.1 Motivation

Ag is known to diffuse into SiO_2 from previous studies. It has been shown in Chapter 3 that the diffusion of Ag into SiO_2 leads to a deterioration of the dielectric properties of the SiO_2. For interconnect applications, failure of the dielectric that separates adjacent interconnect lines could result in a short circuit conduction path between the interconnect lines with catastrophic consequences on the circuit. Even a relatively small leakage current could induce circuit malfunction. Ag is also known to form traps in Si resulting in degradation of the transistor performance. It is therefore imperative to ensure that Ag does not come into direct contact with either the active Si device areas or the SiO_2. It is necessary to use a diffusion barrier when using Ag as the interconnect metal.

5.1.2 Requirements of a Barrier

An excellent general overview of diffusion barriers is given by Nicolet [112]. Let us consider a diffusion barrier between Ag and SiO_2. The barrier must meet several requirements. First and foremost of course it must be effective in preventing the transport of Ag across it. It must be stable under both normal operating conditions and thermal processing steps. Ideally the barrier must adhere well to both the oxide and the Ag. If this

is not the case an additional adhesion layer must be used between the non-adherent layers. This is undesirable since it adds to the complexity of the structure and also increases the effective resistivity of the metal line since it reduces the cross-sectional area available for the conducting Ag. The barrier (and its adhesion layer if necessary) must not affect the resistivity of the Ag. The resistivity of Ag is adversely affected by impurities, and this will be discussed later in this chapter.

5.1.3 Impact of Barrier on Effective Resistivity

One of the reasons for using Ag as an alternate interconnect metal to Al, is its lower resistivity. Interconnect resistivity is becoming the bottleneck to improved device performance. A barrier must not only be effective, but it must also be sufficiently thin that it does not significantly impact the overall resistivity of the interconnect line. The effect of diffusion barrier thickness on effective resistivity is covered in Appendix 1. It is anticipated that if Ag were introduced as an interconnect metal it would be used with a damascene process. The barrier must be deposited with good sidewall coverage. If the sidewall coverage of the barrier is not conformal, cusping could occur. This would make it more difficult during the subsequent deposition process, for the Ag to fill the trench or via. The use of a relatively new technique, atomic layer epitaxy (ALE), may be necessary to achieve thin yet conformal diffusion barriers.

5.2 Barrier Integration

A good barrier material candidate is one that has good adhesion to both oxide and Ag. The barrier material must have only a minimal impact on the resistivity of the Ag.

5.2.1 Adhesion

Adhesion between two films is a measure of the degree to which the two films are held together by their mutual interaction. The forces that hold the films together can be categorized as either physical or chemical. The physical forces are electrostatic in nature. Strong electrostatic forces hold oppositely ionized atoms, whereas somewhat weaker Van der Waals forces hold polarized atoms. Strong chemical bonding leads to good adhesion. Adhesive strength is difficult to quantify experimentally, and the Scotch tape test that was first suggested by Strong in 1935 is still used extensively in the industry to qualify the adhesion of a film to a substrate [113]. In this test a piece of adhesive tape is pressed against the film. The tape is then removed. If some or part of the film is attached to the tape after stripping then the film-substrate couple is said to fail the Scotch tape test. Researchers have made numerous attempts to develop more quantitative techniques to measure adhesion. The scratch test method first described by Heavans [114], and subsequently developed by others [115] is the most commonly employed technique to obtain quantitative data. A review of adhesion measurement techniques is given by Benjamin and Weaver [116], and more recently by Valli [117].

Adhesion of metals to SiO_2 has been studied by many researchers [118-120]. A relationship between the affinity of a metal for oxygen and the adhesion strength that was found by Benjamin and Weaver has been confirmed by others. In terms of IC applications, the lowest resistivity metal that has good adhesion to SiO_2 is Al. The room temperature free energies of formation of several oxides is given in Table 5.1 [121]. As can readily be seen from Table 5.1, Ta, Al and Ti can reduce SiO_2, resulting in a chemical bond that provides good adhesion. However, since neither Cu nor Ag can reduce SiO_2, the adhesion of these metals to SiO_2 is poor.

Table 5.1 Room Temperature Free Energies of Formation

Oxide	Free Energy of Formation (kcal/mole)
Ta_2O_5	-471
Al_2O_3	-377
TiO_2	-204
SiO_2	-192
Cu_2O	-35
Ag_2O	-2.6

5.2.2 Effect of Impurity on Bulk Resistivity of Metal

One of the primary motivating factors for developing Ag for ULSI circuit applications is its low resistivity. However, the resistivity is especially sensitive to impurities. Solute scattering is the primary cause of increased resistance due to the presence of impurities. Impurity resistivity is given for different solutes in both Ag and Cu in Figure 5.1. The data is taken from the *CRC Handbook of Electrical Resistivities*, [122], Koike [123], and Murarka [124]. The impurity resistivity of Ti in Cu is given as 11 μΩ.cm based on the assumption that the value is similar to that of Zr [125], although it is given elsewhere as 16 μΩ.cm [126]. There is no data for the Ta impurity resistivity in Ag. This is because Ta is not soluble in Ag. Ti has a high impurity resistivity in Ag, but its solubility in Ag is less than 3 atomic percent at 600 °C. Table 5.2 shows the impurity resistivity, the diffusivity at 500 °C, and the solid solubility at 500 °C of Al, Ta, and Ti in Ag [127-128].

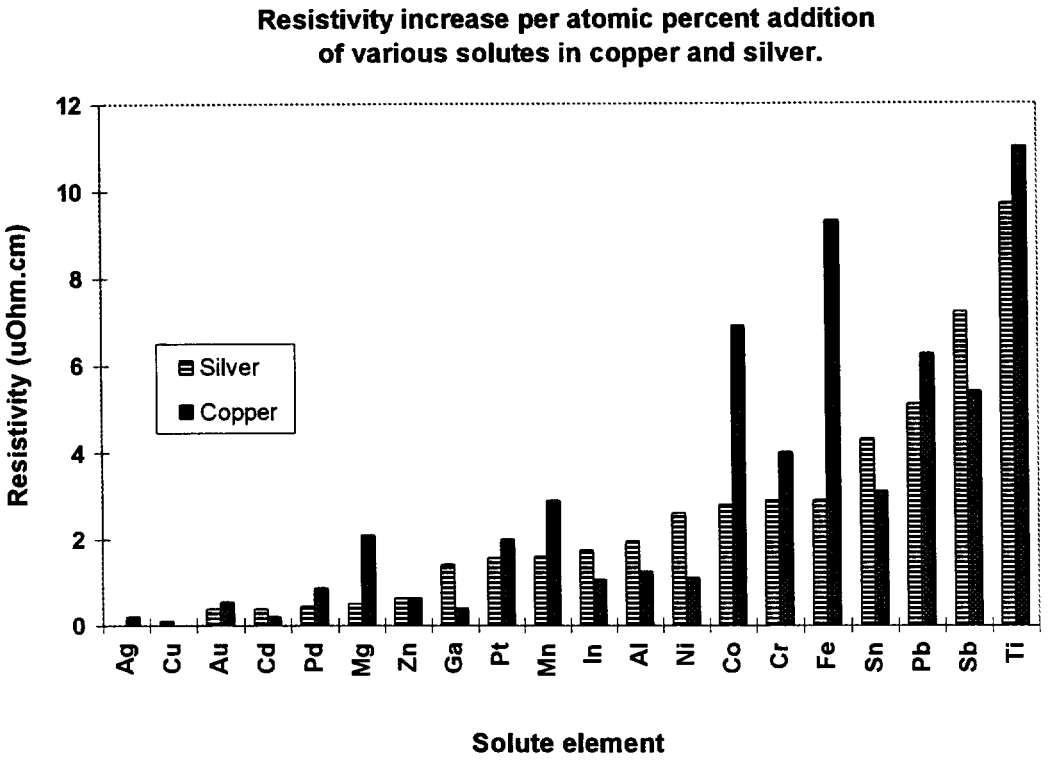


Figure 5.1 Resistivity increase per atomic percent addition of various solutes in copper and silver

Table 5.2 Impurity resistivity, diffusivity, and solid solubility of Ti, Ta and Al in Ag

Metal	Impurity Resistivity ($\mu\Omega$.cm/at. %)	Diffusivity at 500 °C (cm^2/s)	Solid Solubility at 500 °C (at. %)
Ti	9.7	3.59×10^{-14}	~2
Ta	-	-	negligible
Al	1.95	1.96×10^{-12}	20.4

Although the impurity resistivity of Ti in Ag is high, which at first might suggest that Ti should not be considered as a candidate barrier, its low bulk diffusivity and solubility in Ag might be such that Ti (or TiN) could still be a good barrier material candidate. The impurity resistivity of Ta in Ag is not given because Ta is insoluble in Ag.

5.2.3 Experimental Outline

Composite structures were deposited as outlined in Chapter 2, section 2.2.1 for batch 1, and Chapter 2, section 2.2.2 for batch 2. The deposition conditions for batch 2 were optimized to provide a low resistivity Ag film. The resistivity was optimized with respect to deposition rate (section 2.2.2), and the Ag targets were pre-sputtered prior to deposition to remove any surface contamination. Ti was sputtered into the chamber prior to deposition to getter impurities.

The adhesion of the films was tested using the Scotch tape test. Samples were annealed in UHV, and in an anneal furnace. Sheet resistance measurements were made using a 4-point probe. Resistivity was determined using the sheet resistance data and thickness data obtained by SEM using a NIST calibrated standard.

Anneals were done using a UHV system at a base pressure of 2×10^{-10} Torr, and in a forming gas environment using a furnace oven, as described in Chapter 2, section 2.1.

5.2.4 Experimental Results: Adhesion

The adhesion data is presented in Table 5.3. As-deposited adhesion was good for Ag-Ti, Ag-Al, and some of the Ag-TiN and Ag-TiW stacks. Using a 600 °C forming gas anneal (5% H_2 and 95% N_2), good adhesion was obtained for all samples except the Ag-SiO_2 (no barrier) samples.

Table 5.3 Adhesion Data From Scotch Tape Test

		as deposited	forming gas			UHV		
	Recipe		325C	500C	600C	300C	400C	500C
BATCH 1								
Wafer 12	TiN/Ag/TiN	pass				pass	pass	pass
Wafer 02	TiN/Ag//TiN	fail	fail	pass	pass			
Wafer 04	TiN/Ag///TiN	fail	fail	pass	pass			
Wafer 15	TiN/Ag(hi power)/TiN	fail	pass	pass	pass			
Wafer 17	Ti/Ag/TiN	fail		pass	pass			
Wafer 05	Ag/TiN	fail		fail	pass			
Wafer 06	TiW//Ag/TiN	fail	fail	pass	pass			pass
Wafer 19	Ag/Ti/TiN	pass				pass	pass	pass
Wafer 14	TiN/Ag/TiW	pass	pass	pass				
Wafer 08	TiN/Ag//TiW	fail	fail	fail	pass			
Wafer 09	TiN/Ag///TiW	pass	pass	pass	pass			
Wafer 23	Ag/Al	pass						
Wafer 22	Al/Ag/Al	pass	pass					
BATCH 2								
KV1	Ti/Ag//TiN	fail		pass	pass			
KV2	Ti/Ag/Ti//TiN	pass		pass	pass			
KV3	TiW/Ag/Ti//TiN	pass		pass	pass			
KV4	Ti/Ag/TiN	fail		pass	pass			
KV5	Ag	fail		fail	fail			
KV6	TiW/Ag/TiW	pass		pass	pass			
KV7	TiW/Ag/TiW	pass		pass	pass			

5.2.5 Experimental Results: Resistivity

5.2.5.1 Resistivity Results: Batch 1

The resistivity of several composite structures was measured as a function of temperature and anneal time. Resistivity data from the TiN/Ag/TiN stack for UHV anneals is given in Figure 5.2. Resistivity data for Ag/Ti/TiN stack for UHV anneals is given in Figure 5.3. Data for samples annealed in forming gas is shown in Figure 5.4, and is shown again using an expanded scale in Figure 5.5.

5.2.5.2 Resistivity Results: Batch 2

The as-deposited resistivity data for wafer S1B (Ag//SiO_2) is given in Table 5.4. The standard deviation is based on 9 readings across the wafer. Micrographs of a cross-section of the Ag film and a NIST standard (parallel lines of known separation) were used to accurately determine the thickness of the Ag film.

Table 5.4 As-deposited resistivity of S1B (Ag//SiO_2)

Average sheet resistance	21.6 mΩ/□
Standard deviation	1.2 %
Micrograph sample thickness	68 ± 3 mm
Micrograph NIST separation	79.5 ± 3 mm
Actual NIST separation	1.134 μm
Ag film thickness	0.970 ± 0.056 μm
Resistivity (as-deposited)	2.10 ± 0.12 μΩ.cm

The four point probe V/I measurements of samples before and after anneal were used to determine the post-anneal resistivity. The resistivity following a 60 minute anneal in UHV

for 4 samples is shown in Table 5.5. The as-deposited resistivity of the Ag film of all other samples was assumed to be the same as that determined for wafer S1B (Ag//SiO_2).

Table 5.5 Post-anneal resistivity (60 minutes, UHV) for samples from Batch 2

Recipe	Sample ID	pre-anneal V/I (mΩ)	post-anneal V/I (mΩ)	post-anneal resistivity (μΩ.cm)
Ag//TiN	LY1-008	5.75	4.30	1.57 ± 0.09
Ti/Ag/Ti//TiN	LY2-002	5.50	4.82	1.84 ± 0.11
TiW/Ag/Ti//TiN	LY3-008	5.53	4.10	1.56 ± 0.09
Ag//SiO_2	S1B-003	6.00	4.44	1.55 ± 0.09

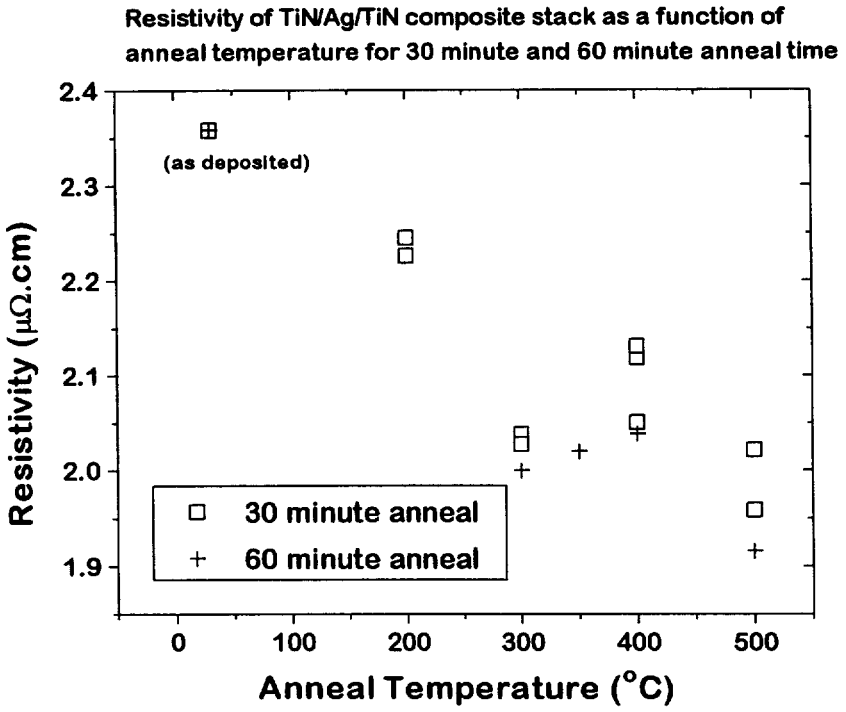


Figure 5.2 Resistivity of TiN/Ag/TiN (W12) samples for UHV anneal

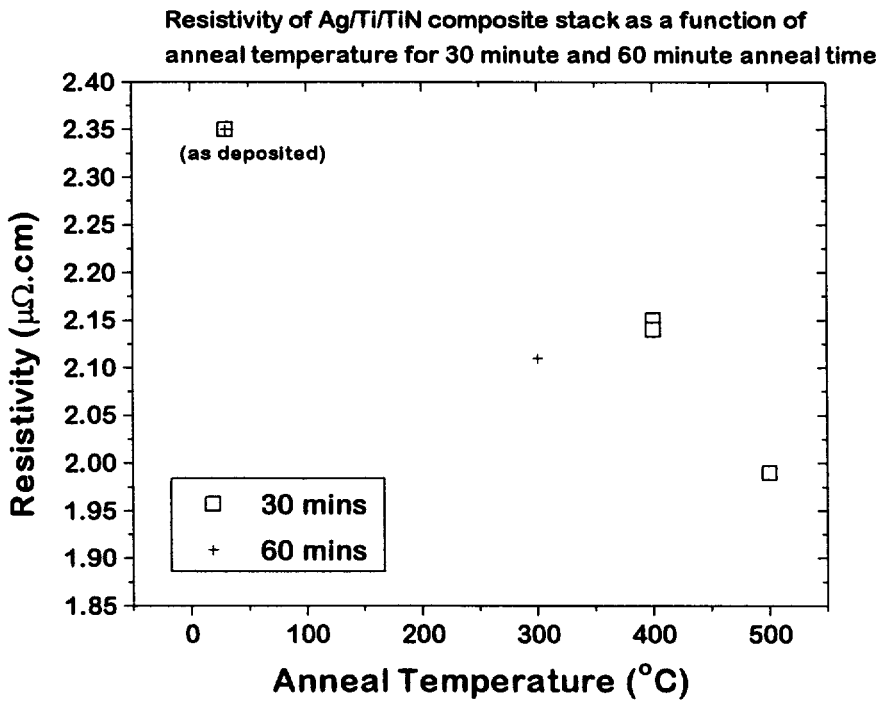


Figure 5.3 Resistivity of Ag/Ti/TiN (W19) stacks for UHV anneal

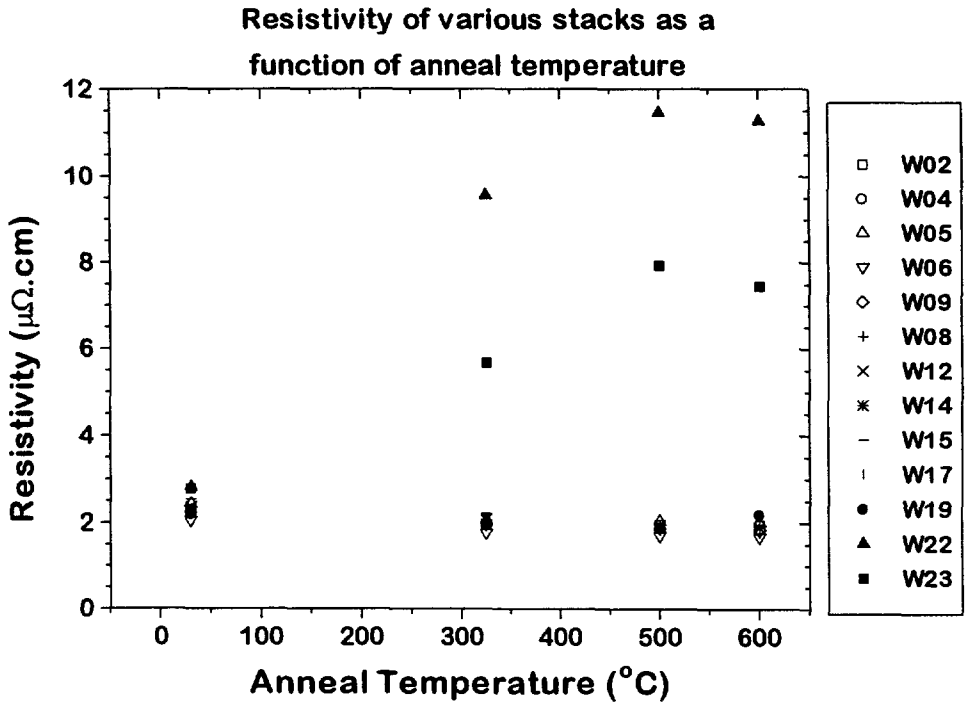


Figure 5.4 Resistivity of various stacks after 2 hour forming gas anneal (recipes of wafer numbers are given in Chapter 2, Table 2.1)

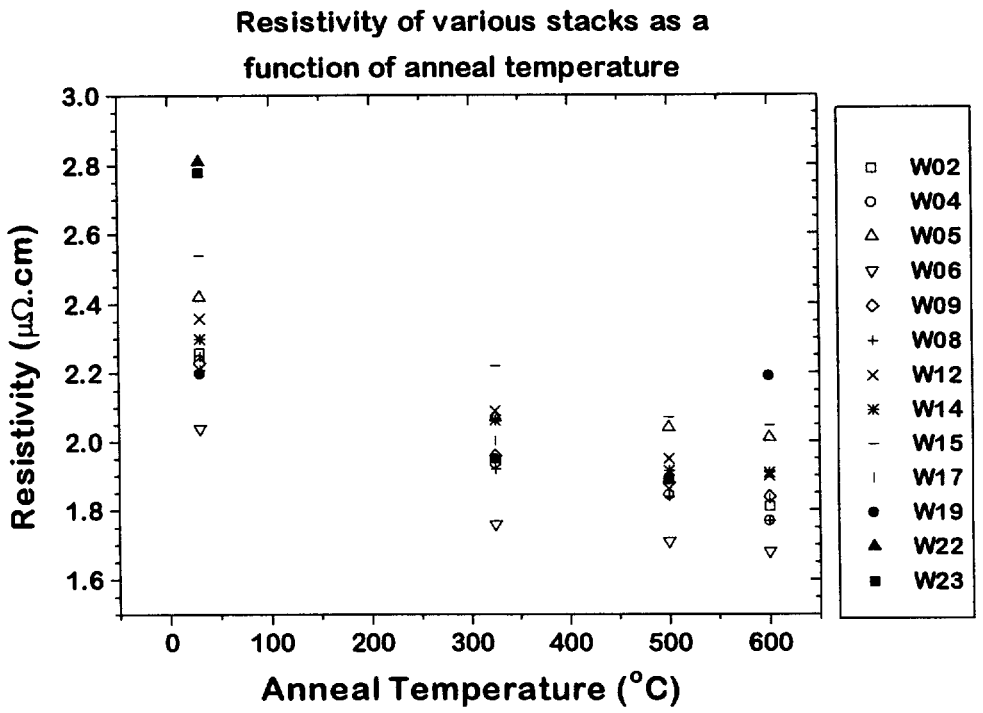


Figure 5.5 Resistivity of various stacks after 2 hour forming gas anneal. Expanded scale.
(recipes of wafer numbers are given in Chapter 2, Table 2.1)

5.2.6 Experimental Analysis

The trend of decreasing resistivity with increasing anneal temperature was present for most stacks. Annealing in UHV did not provide any significant benefit in terms of resistivity compared to the forming gas anneal. The post-anneal resistivity was not compromised for all but the Al-based barrier and capping layers. This indicates that TiN, Ti, and TiW are all good candidate barrier layers in terms of their effect on the resistivity of the Ag. However, the Ag/Al (W23) and Al/Ag/Al (W22) stacks were notably different. As can be seen from Figure 5.4, the resistivity of the Al stacks increased dramatically with annealing. The increase in resistivity can be understood by considering the diffusion of Al into Ag, the impurity resistivity of Al in Ag, the solubility of Al in Ag, and the resistivity effect of a solute whose concentration in a host material varies with depth.

The data from batch 2 shows that thin films of Ag can be obtained by sputter deposition with resistivity as low as that of bulk Ag (1.59 μΩ.cm). It was also shown that TiN, Ti, and TiW can all be used without significantly effecting the resistivity of the Ag during subsequent thermal steps.

5.2.6.1 Solutions to the Diffusion Equation for Al

First consider the diffusion of Al into Ag for the Ag/Al stack. The stack is represented in Figure 5.6. The diffusion equation is solved for the appropriate boundary conditions in Appendix 2. The boundary condition that the Al is confined between $0 < x < l$ was used. The concentration of Al as a function of distance, x, in the region $0 < x < l$ is given by:

$$C = \frac{C_o}{2} \sum_{n=-\infty}^{\infty} \operatorname{erf} \frac{x + h - 2nl}{2\sqrt{Dt}} + \operatorname{erf} \frac{2nl - x + h}{2\sqrt{Dt}} \qquad \text{Eqn. 5.1}$$

where C is the distance/time dependent Al concentration, C_0 is the initial Al concentration (100%), D is the diffusivity, x is the distance, h is the Al barrier thickness, l is the composite stack thickness, and t is the time.

The Al barrier thickness is 40 nm, which is represented by h, the Al barrier thickness, is 40 nm. The anneal time is 2 hours. Using these values the Al concentration was calculated and is given in Figure 5.6. Now let us consider the Al/Ag/Al stack represented in Figure 5.7. Here we have a 40 nm barrier layer and a 40 nm capping layer. The solution is also derived in Appendix 2. The concentration of Al as a function of distance, x, in the region $0 < x < l$ is given by:

$$C = \frac{C_o}{2} \sum_{n=-\infty}^{\infty} \operatorname{erf} \frac{x + h - nl}{2\sqrt{Dt}} + \operatorname{erf} \frac{nl - x + h}{2\sqrt{Dt}} \qquad \text{Eqn. 5.2}$$

The Al concentration is shown in Figure 5.9, for different values of the diffusivity of Al in Ag.

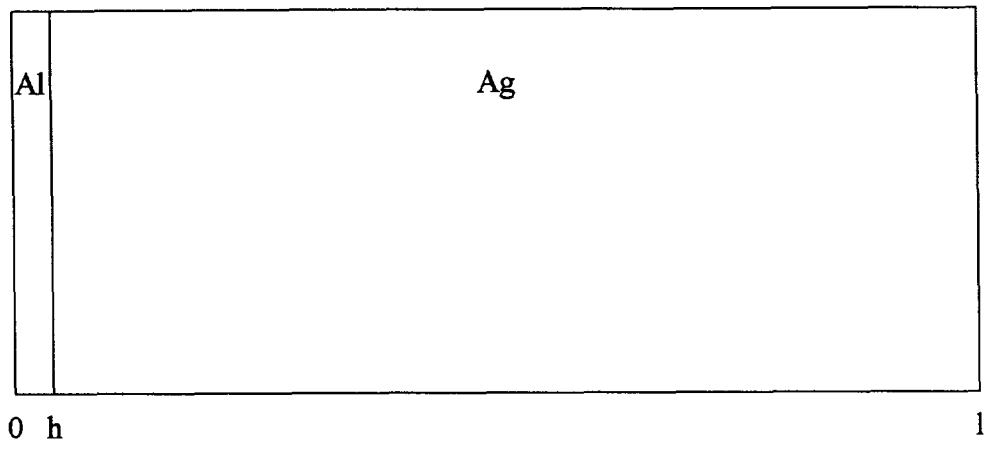


Figure 5.6 Schematic representation of Ag/Al structure
$h = 0.04$ μm, $0 \leq x \leq l$, $l = 1.04$ μm

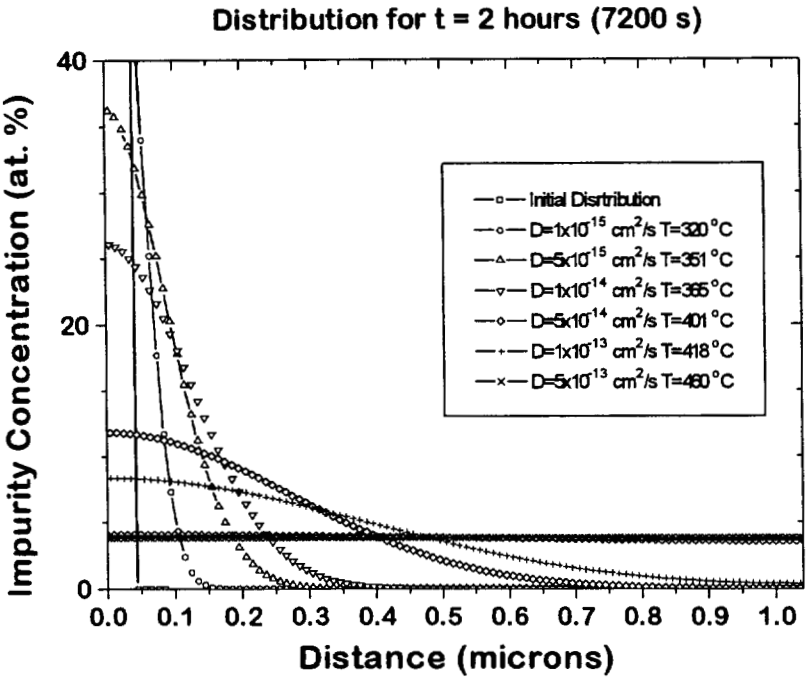


Figure 5.7 Solution to the diffusion equation for a 40 nm barrier layer for a 2 hour anneal.

$h = 0.04$ μm, $0 \le x \le l$, $l = 1.04$ μm

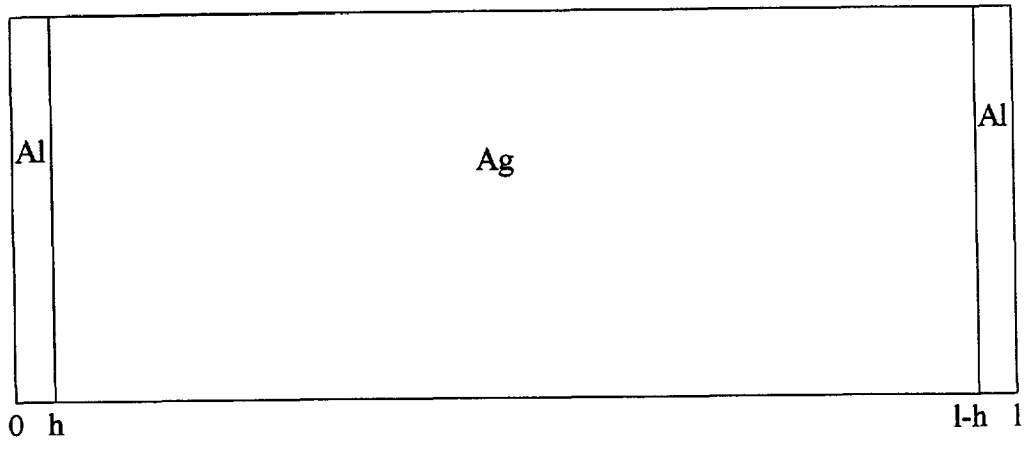


Figure 5.8 Schematic representation of Al/Ag/Al structure.
$h = 0.04$ μm, $0 \leq x \leq l$, $l = 1.08$ μm

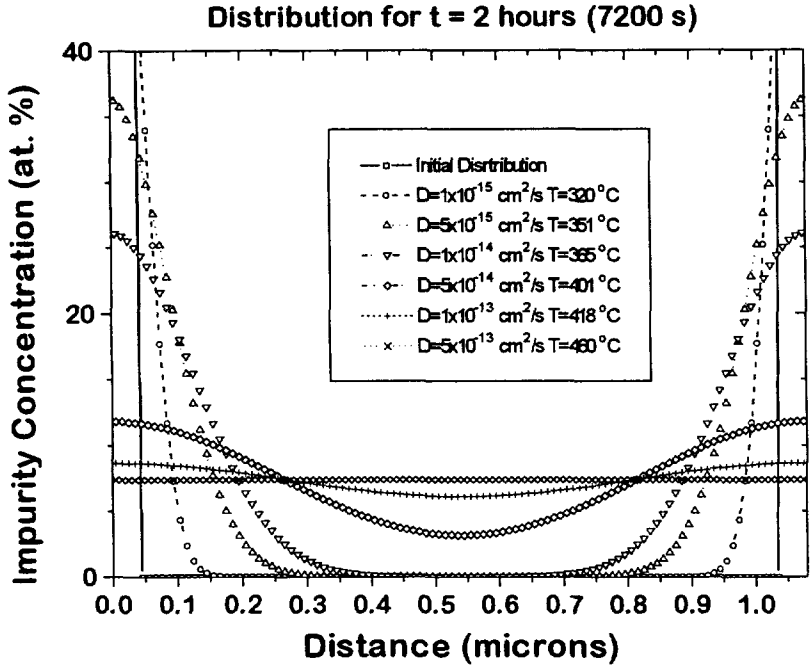


Figure 5.9 Solution to the diffusion equation for a 40 nm barrier layer and 40 nm capping layer for a 2 hour anneal

$h = 0.04$ μm, $0 \le x \le l$, $l = 1.08$ μm

5.2.6.2 Model of the Resistivity of the Ag Film

Now that we have solved the diffusion equation, we are able to estimate the Al concentration in the Ag. Using this we can estimate the effective resistivity of the Ag film by considering the film to be comprised of multiple slabs. Each slab will make a contribution to the resistivity. We can estimate the resistivity of each slab by considering the Al concentration in each slab, and determining the resistivity of each slab based on the Al impurity resistivity. First of all we consider the case of a conducting metal film of sheet resistance, R_s as given in Figure 5.10. For a film whose resistivity, ρ, is constant with respect to depth (i.e. all slabs have the same resistivity), R_s is simply given by Eqn. 5.3:

$$R_s = \frac{\rho}{x_d} \qquad \text{Eqn. 5.3}$$

where x_d is the thickness of the film. However, for a film whose resistivity is not constant with depth, the film can be considered to be made up of multiple slabs. The resistivity of each slab has a value of ρ_j. The sheet resistance of each slab contributes to the effective sheet resistance of the entire film much like resistors in parallel. The sheet resistance, R_s, is given by Eqn. 5.4.

$$\frac{1}{R_s} = \sum_{j=1}^{n} \frac{\Delta x}{\rho_j} \rightarrow \int_0^{x_d} \frac{dx}{\rho(x)} \qquad \text{Eqn. 5.4}$$

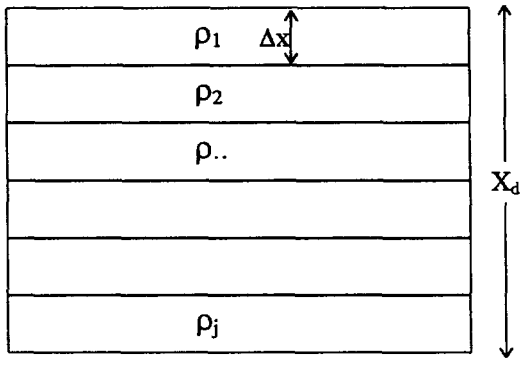


Figure 5.10 Cross-section of a conducting film

The resistivity of each slab is given by Matthienssen's rule

$$\rho = \rho_{temp} + \sum_i \rho_i \qquad \text{Eqn. 5.5}$$

where ρ_{temp} is the temperature dependent term and ρ_i is the temperature independent term due to the i^{th} factor. The sum of the temperature independent terms is referred to as the residual resistivity. The residual resistivity is associated with numerous factors, *i*, such as defects, stresses, and impurities. If we assign the Al impurity resistivity as the first factor and sum over all *i* except $i = 1$, then we have:

$$\rho = \rho_{temp} + \sum_{i \neq 1} \rho_i + \rho_{Al} \qquad \text{Eqn. 5.6}$$

and by defining ρ_0 such that:

$$\rho_0 = \rho_{temp} + \sum_{i \neq 1} \rho_i \qquad \text{Eqn. 5.7}$$

we have:

$$\rho = \rho_0 + \rho_{Al} \qquad \text{Eqn. 5.8}$$

For small concentrations (i.e. 5 atomic percent or less) of solute impurity in a host metal, the impurity resistivity, ρ_i, is given by:

$$\rho_i(C) = KC \qquad \text{Eqn. 5.9}$$

where C is the atomic percent concentration and K is the impurity resistivity constant for the solute element in the host lattice. For Al in Ag the impurity resistivity constant, K_{Al}, is 1.95 μΩ.cm per atomic percent. We then have:

$$\rho_{Al} = K_{Al} C_{Al} \qquad \text{Eqn. 5.10}$$

Inserting this into Eqn. 5.8 and noting that C_{Al} is function of x, where x is the distance into the Ag from the Al/Ag interface we have:

$$\rho = \rho_0 + K_{Al} C_{Al}(x) \qquad \text{Eqn. 5.11}$$

Using this with Eqn. 5.4 and Eqn. 5.3, and then taking the integral we finally arrive at an expression for the effective resistivity of the Ag film:

$$\frac{1}{\rho} = \frac{1}{x_d} \int_0^{x_d} \frac{dx}{\rho_0 + K_{Al} C_{Al}(x)} \qquad \text{Eqn. 5.12}$$

Eqn. 5.12 allows the effective resistivity to be determined, given the Al concentration distribution, $C_{Al}(x)$, from Eqn. 5.1 or Eqn. 5.2.

Eqn. 5.12 is valid under the following assumptions. It is assumed that the impurity resistivity is a linear function of the concentration, C. This is approximately true for small impurity concentrations only. For impurity concentrations above a few percent (typically 5%), the resistivity will be overestimated. This shortcoming could be corrected by using the experimental values of the resistivity of the binary metal alloy from the *CRC Handbook of Electrical Resistivities of Binary Metallic Alloys* cited earlier [122], for each slab. The added complexity is not considered worthwhile by the following reasoning. If the impurity concentration is high in one region then only a small amount of diffusion has occurred. This means that there is very little impurity in other regions. The pristine

regions will contribute far more significantly to the overall effective conductivity than the regions containing a high amount of impurity. The overestimating of the highly resistive region will therefore not significantly effect the overall resistivity estimate. It is also assumed that all of the available Al is dissolved into the Ag. This requires that the Al concentration be less than the solid solubility of Al in Ag. However, the maximum solid solubility of Al in Ag is 20.4 at. % at 450 °C, and approximately 10 at. % at 200 °C [128]. This assumption is therefore valid when the diffusion is complete but not valid in the initial stages of diffusion. Once again, the argument that the pristine regions will make the most significant contribution to the conductivity could be made. It is also recognized that the diffusion equation is solved for a single crystal film, whilst recognizing that the Ag film is polycrystalline.

5.2.6.3 Maximum Resistivity of the Ag Film

It can be shown that for an arbitrary impurity distribution function, $C(x)$, in a film of thickness x_d, given the condition that total amount of impurity in the film is constant, as expressed mathematically by:

$$\int_0^{x_d} C(x)dx = M \qquad \text{Eqn. 5.13}$$

The conductivity is a minimum if the impurity concentration is equal throughout the film. To prove this we begin with Eqn 5.12 and let I be equal to the reciprocal of the resistivity, ρ, and using Eqn. 5.13 we have:

$$\frac{1}{\rho} = I = \frac{1}{x_d}\int_0^{x_d} \frac{dx}{\rho_0 + KC(x)} + \lambda \int_0^{x_d} C(x)dx - \lambda M \qquad \text{Eqn. 5.14}$$

which can be rearranged to give:

$$I = \frac{1}{x_d}\int_0^{x_d}\left(\frac{dx}{\rho_0 + KC(x)} + \lambda x_d C(x)\right)dx - \lambda M \qquad \text{Eqn. 5.15}$$

Defining the function f as:

$$f = \frac{1}{\rho_0 + KC(x)} + \lambda x_d C(x) \qquad \text{Eqn. 5.16}$$

and using calculus of variations [18] it can be shown that for the integral, I, to be an extrema with respect to $C(x)$, requires the condition:

$$\frac{\partial f}{\partial C} = 0 \qquad \text{Eqn. 5.17}$$

From Eqn. 5.17 we arrive at:

$$0 = \frac{-K}{\left(\rho_0 + KC(x)\right)^2} + \lambda x_d \qquad \text{Eqn. 5.18}$$

Eqn. 5.18 implies that $C(x)$ is constant. The reason that this is significant is that the film will have the highest resistivity when the diffusion process has been driven to completion.

5.2.6.4 Comparison of Measured and Predicted Resistivity for Al

The diffusion of Al through the Ag film, the impurity resistivity of the Al in the Ag film, and the effective resistivity of a film comprised of multiple slabs of not necessarily the same resistivity has been considered. It is now possible to predict the effective resistivity

of the of the stack after anneal, provided the diffusivity of Al in Ag is known. The values of the diffusivity, D, are obtained from:

$$D = D_0 \exp(\frac{-Q}{kT}) \qquad \text{Eqn. 5.19}$$

with $D_0 = 0.13$ cm^2/s and $Q = 1.66$ eV from Smithells [127]. Using the value of diffusivity derived from Eqn. 5.19, a prediction of the resistivity can be made using the solution to the diffusion equations of Eqn. 5.1 and Eqn. 5.2 in the resistivity equation, Eqn. 5.12. The integrals were evaluated numerically using Mathcad software. A table of the predicted results and the experimental data is given in Table 5.6

Table 5.6 Effective Resistivity after 2 hour anneal: Predicted and Experimental

	Diffusivity, D (cm^2/sec.)	Effective Resistivity Ag/Al (μΩ.cm)		Effective Resistivity Al/Ag/Al (μΩ.cm)	
		measured	predicted	measured	predicted
325 °C	1.35×10^{-15}	5.7	2.2	9.6	2.5
500 °C	1.96×10^{-12}	7.9	9.5	11.5	16.4
600 °C	3.41×10^{-11}	7.5	9.5	11.3	16.4

The predicted resistivity varies according to the value of diffusivity that was used to estimate the Al concentration. Predicted and measured resistivity vs. 1/kT, where T is the annealing temperature, is plotted in Figure 5.10.

There is qualitative agreement between the predicted and the measured resistivities of the Ag/Al stacks. Based on single crystal diffusion, the Al will be completely homogenized in the Ag following a 2 hour anneal for a diffusivity greater than approximately 3×10^{-13} cm^2/sec., which, for the values of D_0 and Q, corresponds to a temperature of around 450 °C. It is therefore predicted that annealing above this

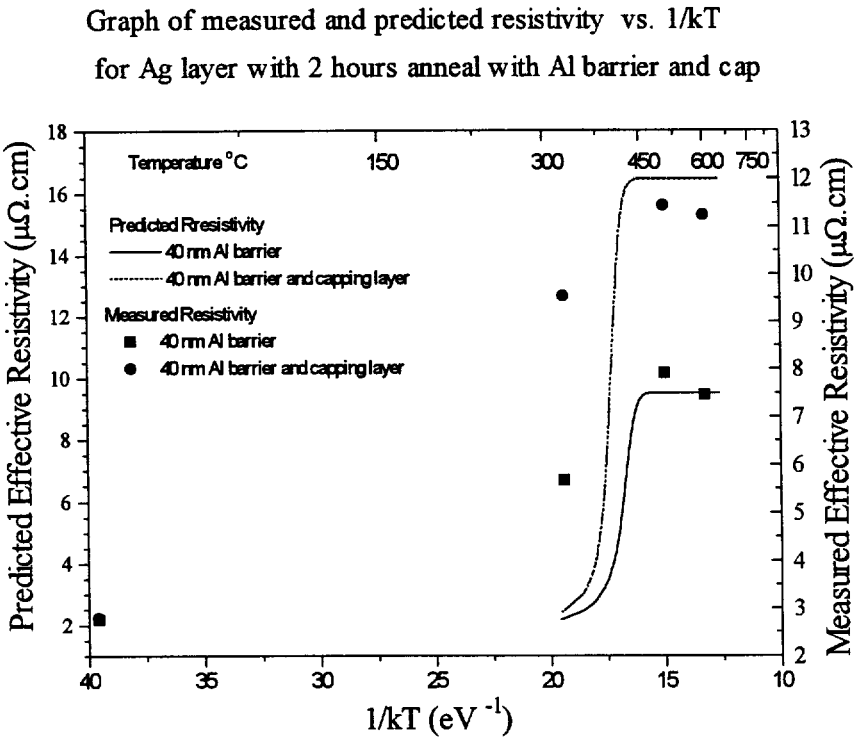


Figure 5.11 Graph of predicted and measured effective resistivity vs. 1/kT for 2 hour anneal, Ag with i) Al barrier ii) Al barrier and cap

temperature (for 2 hours) will not result in increased resistivity. This is consistent with the data. In fact, the data shows that the effective resistivity is actually slightly lower for the 600 °C anneal than for the 500 °C anneal for both Ag/Al and Al/Ag/Al stacks. There is not as good a quantitative agreement for the 325 °C anneal data. This could be due to the following reason. The Ag film is polycrystalline. It is known that for polycrystalline materials grain boundary diffusion is dominant at lower temperatures, but at higher temperatures the volume diffusion contribution is more significant. Therefore considerably more diffusion than predicted could have occurred via grain boundary diffusion at lower temperatures, i.e. 325 °C. Taking the grain boundary diffusion into consideration is non-trivial. An excellent chapter on high diffusivity paths is given by Shewmon [129].

5.2.6.5 Solutions to the Diffusion Equation for Ti

The stacks that utilized either TiN, TiW or Ti as a barrier or capping layer showed low resistivity even after a 2 hour anneal at 600 °C. First consider the Ag/Ti/TiN (W19). Ti has low solubility in Ag. At 600 °C, the solid solubility of Ti in Ag is 2.8 atomic percent. A 40 nm barrier could not be fully depleted into a 1 μm thick Ag film. It is therefore appropriate to use the boundary condition that there is a constant concentration of Ti at the Ti/Ag interface, C_0, which is equal to the solid solubility limit of Ti in Ag. The structure is represented in Figure 5.12. From Crank [130], the solution to the diffusion equation for a plane sheet thickness $2l$, whose surfaces are maintained at constant concentration, C_0, with zero initial concentration throughout the sheet is given by:

$$C = C_0 \sum_{n=0}^{\infty} (-1)^n \operatorname{erfc} \frac{(2n+1)l - x}{2\sqrt{Dt}} + C_0 \sum_{n=0}^{\infty} (-1)^n \operatorname{erfc} \frac{(2n+1)l + x}{2\sqrt{Dt}} \quad \text{Eqn. 5.20}$$

where the sheet occupies the region $-l \le x \le l$.

The boundary conditions for the structure represented in Figure 5.12 in the region $0 \leq x \leq l$ is:

$$C = C_0, \quad x = 0, \quad t \geq 0$$
$$\frac{\partial C}{\partial x} = 0, \quad x = l, \quad t \geq 0 \qquad \text{Eqn. 5.21}$$

and the solution is:

$$C = C_0 \sum_{n=0}^{\infty} (-1)^n \operatorname{erfc} \frac{(2(n+1))l - x}{2\sqrt{Dt}} + C_0 \sum_{n=0}^{\infty} (-1)^n \operatorname{erfc} \frac{2nl + x}{2\sqrt{Dt}} \qquad \text{Eqn. 5.22}$$

The impurity distribution of Ti in Ag is given in Figure 5.13, using D_0 = 1.33 cm^2/second and Q = 2.06 eV from Smithells [127]. The solutions to the diffusion equation predicts very little diffusion of Ti into the Ag until an anneal temperature of 500 °C is reached. Therefore, it is not expected that a 2 hour anneal would cause an increase in resistivity unless the anneal temperature was above 500 °C. This is consistent with the data. Table 5.5 shows the resistivity of Ag/Ti/TiN samples following a 2 hour anneal at different temperatures.

Table 5.7 Resistivity of Ag/Ti/TiN stacks after anneal

	20 °C	325 °C	500 °C	600 °C
Ag/Ti/TiN (W19)	2.20 μΩ.cm	1.95 μΩ.cm	1.89 μΩ.cm	2.20 μΩ.cm

Following an anneal at 600 °C for 2 hours, the Ti should be evenly distributed throughout the Ag, based on the solution to the diffusion equations, and its resistivity effect should be limited by the room temperature solid solubility limit. Using an impurity resistivity value

of 10.5 μΩ.cm/at.%, the effective resistivity of the Ag would be approximately 30 μΩ.cm if 2.8 at.% of Ti was dissolved into the Ag. Since the resistivity after the 2 hour, 600 °C anneal was only 2.20 μΩ.cm (0.7 μΩ.cm above bulk), then the maximum dissolved Ti in the Ag was less than 0.07 at.% assuming an impurity resistivity of 10.5 μΩ.cm/at.%. Either the Ti did not diffuse into the Ag to the extent predicted by the solution to the diffusion equations, or it subsequently precipitated out at the grain boundaries during cool-down.

5.2.7 Barrier Integration Conclusions

It was shown that Al could not be used as a barrier material due to its effect on the resistivity of the Ag. The diffusivity of Ti in Ag is much lower than that of Al in Ag in the temperature range of the experiment. Based on the diffusivity from Smithells [127], a sufficient amount of Ti would be diffused into the Ag to effect the resistivity of the Ag film for a 2 hour anneal if the temperature were above 500 °C. However, the data suggested that only a very small amount of Ti was distributed throughout the Ag film. Ti did not effect the resistivity of Ag as much as the Al did, even though Ti has a much higher impurity resistivity than Al. This was due to the low solid solubility of Ti in Ag. The product of the impurity resistivity and the room temperature solid solubility provides an upper bound for resistivity of the Ag after anneal. It was also shown that Ti provided good adhesion. The adhesion of Ag to TiN was adequate. It was therefore decided to investigate TiN as a candidate barrier. Ta is virtually insoluble in Ag, and its adhesion on SiO_2 is good based on energy of formation arguments (Table 5.1). It was therefore decided that Ta should also be investigated as a candidate barrier.

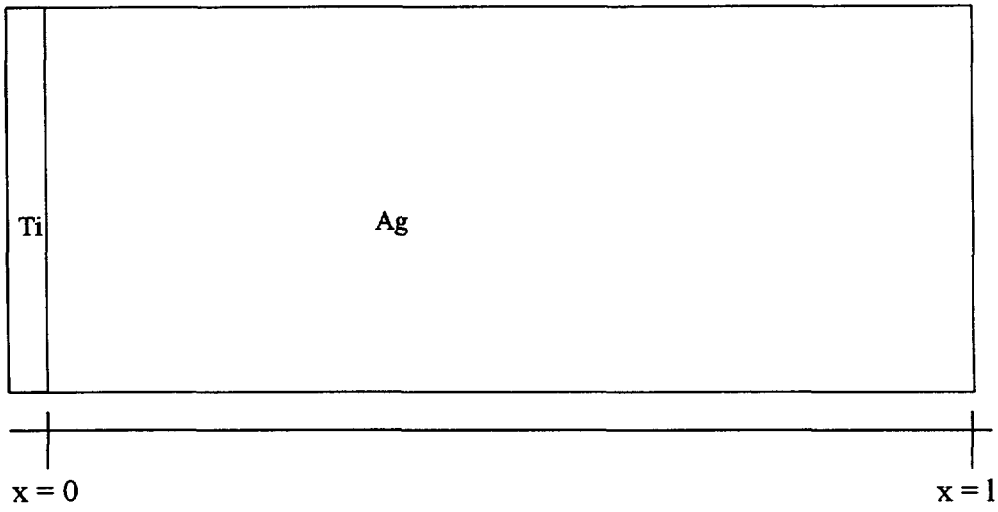


Figure 5.12 Schematic of Ti/Ag structure
$0 \leq x \leq l$, $l = 1.0$ μm

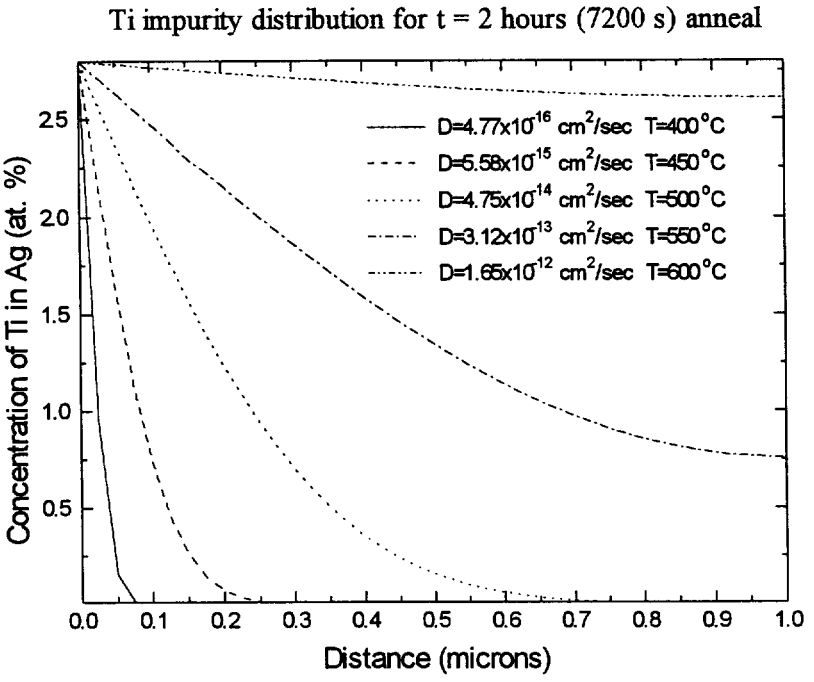


Figure 5.13 Ti impurity distribution for a 2 hour anneal

$0 \leq x \leq l$, $l = 1.0$ μm

5.3 Diffusion Barrier Effectiveness

TiN was selected as a barrier candidate based on the work outlined in Chapter 5, section 5.2. Ta was selected as a barrier candidate based on encouraging unpublished data that demonstrated the effectiveness of Ta in preventing diffusion in Cu-based MOS structures and its low solid solubility in Ag. The adhesion of Ta to oxide was expected to be good for reasons outlined in Chapter 5, section 5.2.1.

5.3.1 Experimental Outline

MOS structures using Ag as the electrode were sputter deposited as outlined in Chapter 2, section 2.2.4. A total of 3 barriers were selected. The first barrier was 400 Å of TiN, the second barrier was 400 Å of TiN with an additional 50 Å of Ti (for adhesion promotion), and the third barrier selected was 400 Å of Ta. A comparison of the relative barrier performance of all 3 barriers was done under BTS of 1 MV/cm, and 300 °C. The Ta barrier performance was also evaluated in the temperature range of 275 °C to 325 °C under the same bias conditions of 1 MV/cm.

Ta had not been included in the candidate barrier experiments of Chapter 5, section 5.2. Therefore, blanket Ta samples were annealed at 500 °C for 2 hours in forming gas. Pre-anneal and post-anneal sheet resistance measurements were made to determine if the anneal had any effect on the resistivity of the Ag film. Also, adhesion was qualified using the Scotch tape test.

5.3.2 Experimental Results

The pre-anneal and post-anneal four point probe measurements, and the adhesion test results, are given in Table 5.8.

Table 5.8 Pre-Anneal and Post-Anneal Sheet Resistance Measurements

	Pre-anneal	Post-anneal
Sheet Resistance	22.9 mΩ/□	22.6 mΩ/□
Scotch tape test	pass	pass

Time to failure data for all 3 barriers studied under bias thermal stress of 1 MV/cm, 300 °C is summarized in Table 5.9. Cumulative failure vs. time for all 3 barriers (under bias thermal stress of 1 MV/cm, 300 °C), is given in Figure 5.14. The data for Ag with no barrier (under the same BTS conditions) that was reported in section 3.1.5 is also given again for comparison. Time to failure data for Ta barrier under BTS of 1 MV/cm and temperatures ranging form 275 °C to 325 °C is given in Table 5.10. Cumulative failure vs. time for Ta barrier data is given in Figure 5.15. A plot of 50 % time to failure and 80 % time to failure is given in Figure 5.16.

5.3.3 Experimental Analysis

It can be seen from Figure 5.14 that the Ta barrier gives an order of magnitude greater performance than the TiN barrier, and 2 orders of magnitude greater performance than no barrier at all. Ta has been shown to be an effective diffusion barrier to prevent Cu diffusion into SiO_2 [132]. It can be seen from Figure 5.15 that there is a trend of decreasing lifetime with increasing temperature for the structures tested in the 300 °C to 350 °C temperature range. However, the Weibull plot of the structures tested at 275 °C suggests a bimodal failure mechanism at that temperature. Since the barriers used here are highly conductive, there should not be any field across the barrier. The Ag would have to diffuse thermally through the barrier before being able to drift through the oxide. The failure mechanism would therefore not be a singly thermally activated mechanism.

Table 5.9 Time to Failure Data for Ag barriers under BTS of 1 MV/cm, 300 °C

Sample	Time to Failure (mins)	Barrier
2wd2-01	51	TiN
2wd2-03	43	TiN
2wd2-05	108	TiN
2wd2-07	142	TiN
2wd1-01	98	Ti/TiN
2wd1-03	100	Ti/TiN
2wd4-05	<1	Ta
2wd4-07	360	Ta
2wd2-09	8	TiN
2wd2-11	75	TiN
2wd2-17	154	TiN
2wd2-18	102	TiN
2wd2-19	139	TiN
2wd2-20	31	TiN
2wd4-09	<1	Ta
2wd4-10	1359	Ta
2wd4-11	1531	Ta
2wd4-12	<1	Ta
2wd1-05	<1	Ti/TiN
2wd1-06	<1	Ti/TiN
2wd1-07	638	Ti/TiN
2wd1-08	245	Ti/TiN
2wd4-13	2256	Ta
2wd4-14	1972	Ta
2wd4-15	1844	Ta
2wd4-16	1774	Ta
2wd4-41	1561	Ta
2wd4-42	480	Ta
2wd4-43	2526	Ta
2wd4-44	3001	Ta

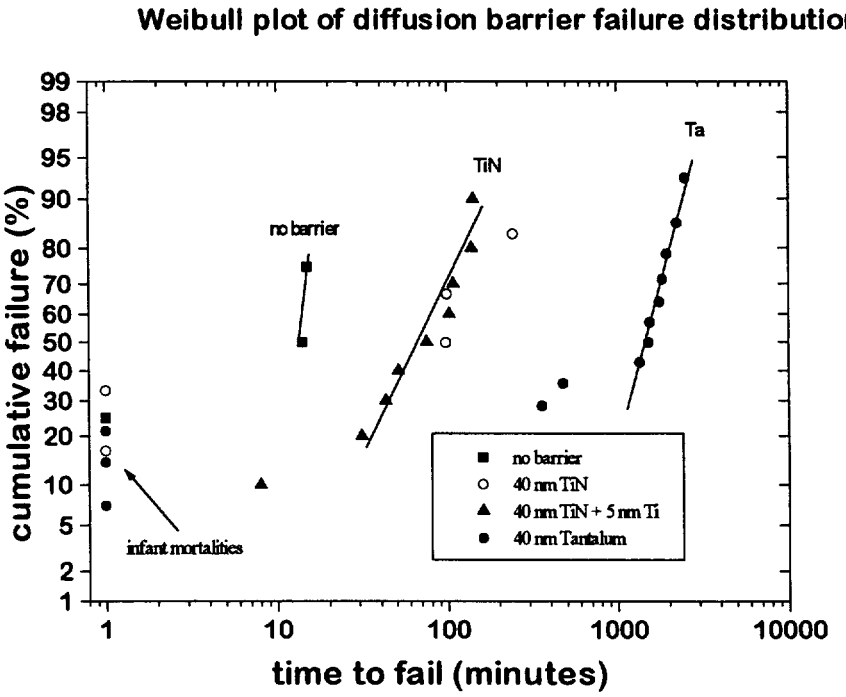


Figure 5.14 Cumulative failure vs. time for Ag barriers under BTS of 1 MV/cm, 300 °C.

Table 5.10 Time to failure for Ta barrier under BTS of 1 MV/cm

Sample	Temperature	Time to Failure (mins)
2wd4-05	300 °C	<1
2wd4-07	300 °C	360
2wd4-09	300 °C	<1
2wd4-10	300 °C	1359
2wd4-11	300 °C	1531
2wd4-12	300 °C	<1
2wd4-13	300 °C	2256
2wd4-14	300 °C	1972
2wd4-15	300 °C	1844
2wd4-16	300 °C	1774
2wd4-17	325 °C	836
2wd4-18	325 °C	<1
2wd4-19	325 °C	901
2wd4-20	325 °C	1018
2wd4-21	350 °C	529
2wd4-22	350 °C	535
2wd4-23	350 °C	114
2wd4-24	350 °C	882
2wd4-25	350 °C	186
2wd4-26	350 °C	<1
2wd4-27	350 °C	109
2wd4-28	350 °C	535
2wd4-29	325 °C	732
2wd4-30	325 °C	2567
2wd4-31	325 °C	1104
2wd4-32	325 °C	1649
2wd4-33	275 °C	559
2wd4-34	275 °C	653
2wd4-35	275 °C	709
2wd4-36	275 °C	1001
2wd4-37	275 °C	1704
2wd4-38	275 °C	2464
2wd4-39	275 °C	2905
2wd4-40	275 °C	6800
2wd4-41	300 °C	1561
2wd4-42	300 °C	480
2wd4-43	300 °C	2526
2wd4-44	300 °C	3001
2wd4-73	350 °C	459
2wd4-74	350 °C	208
2wd4-75	350 °C	291
2wd4-76	350 °C	<1
2wd4-77	350 °C	21
2wd4-78	350 °C	<1
2wd4-79	350 °C	8
2wd4-80	350 °C	135

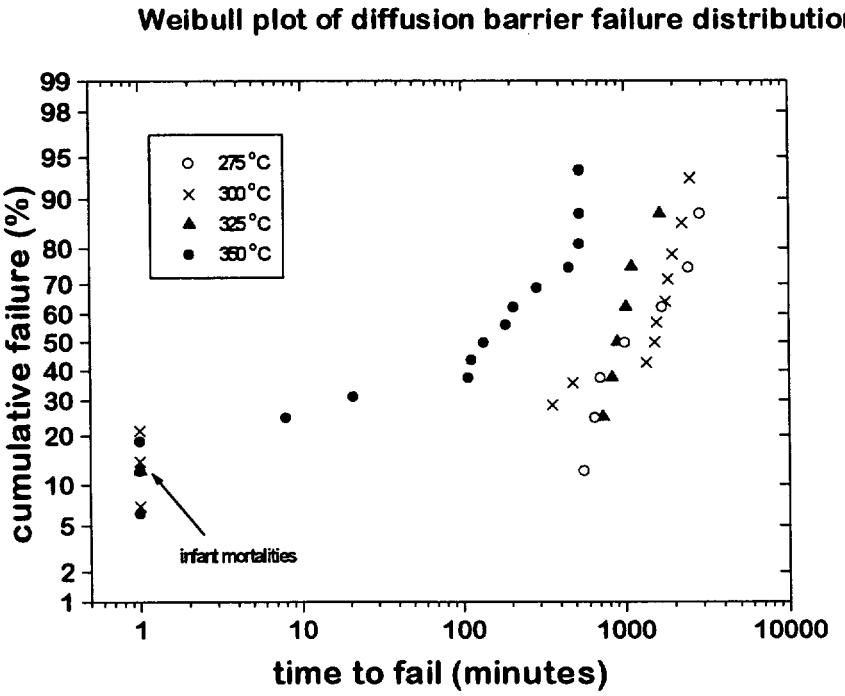


Figure 5.15 Cumulative failure vs. time for Ta barriers under BTS of 1 MV/cm, in the range of 275 °C to 350 °C.

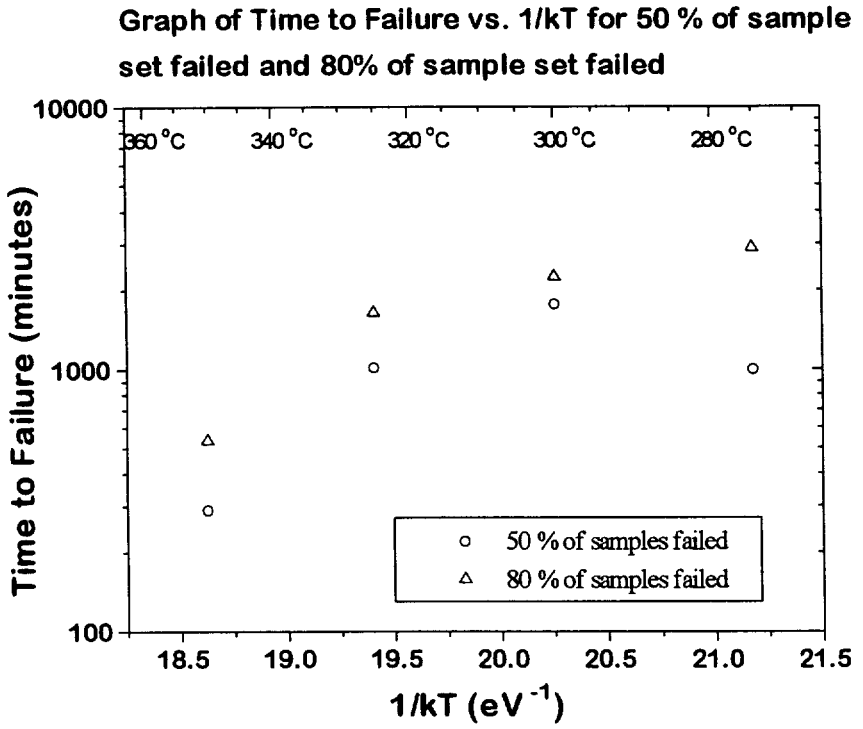


Figure 5.16 50 % time to failure and 80 % time to failure vs. 1/kT for Ta barrier, 1 MV/cm

Chapter 6
Conclusions

6.1 Future Interconnect Technology

The performance limitations for ULSI circuits will be increasingly determined by the interconnect technology. Specifically, the limiting factor with respect to device speed will be the RC delay associated with the interconnect line and adjacent inter-metal dielectric. The R component of the RC delay is fundamentally limited by the resistivity of the metallization. There are only 2 metals that have sufficiently lower resistivity than Al, i.e., Cu and Ag. The C component of the RC delay can be lowered by the introduction of low-k dielectrics, of which there are many alternatives. It is possible that both low-resistivity-metal-based interconnects and low-k dielectric materials will simultaneously be incorporated into future ULSI circuits.

6.2 Ag-based Interconnect for Future Technology

It has been shown in this work that Ag interconnect lines can be made using a damascene method for the 0.5 micron regime, using sputter deposition and mechanical polishing. A reflow temperature of 450 °C was used following deposition. Ag-based damascene interconnects offer a 2x superior effective resistivity compared to Al-based damascene technology. It was also shown that adequate adhesion can be obtained with the use of either TiN, Ti, Ta, or TiW without affecting the resistivity of the metal stack.

Although Ag can diffuse into silicon dioxide under bias thermal stress, the use of a Ta barrier can provide 2 orders of magnitude better performance than no barrier at all. The techniques outlined here should assist future researchers in obtaining electromigration data.

6.3 Suggestions for Further Work

The use of low-k dielectrics for ULSI circuit applications is receiving considerable attention [133]. The compatibility of Ag with materials whose permittivity is lower than that of silicon dioxide (k=4.0) should be studied. Two examples of low-k materials are parylene (k=2.7), and flourinated silicon dioxide (k=3.5). Low temperatures are desirable for back end processes. Therefore, the minimizing of the temperature requirement for reflow should be researched. The deposition of Ag using self-sputtering should also be investigated as a means to provide optimal initial fill of high aspect ratio trenches and vias. The deposition of Ag by electroless/electrochemical techniques should also be pursued. Based on the work done here, it is recommended that EM data is collected using Kelvin structures so as to eliminate the effect of the contact resistance. The diffusion of Ag under BTS through silicon nitride and phosphorous-doped silicon dioxide (PSG) may also be an area of interest to future researchers.

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Appendix 1

A1.1 Effective Resistivity of a Metal Stack

Consider the cross-sectional area of a square conducting line of width, *s*, with a barrier of thickness, *t*.

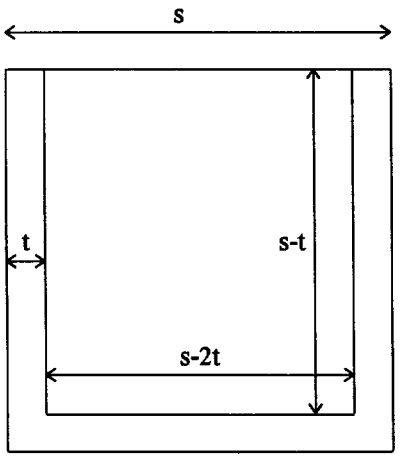

Figure A1.1 Conducting line with barrier thickness, *t*

It is trivial to show that the cross-sectional area of the barrier, A_b, and the conductor, A_{pc} is given by:

$$A_b = 3ts - 2t^2 \qquad \text{Eqn. A1.1}$$

and:

$$A_{pc} = s^2 - [3ts - 2t^2] \qquad \text{Eqn. A1.2}$$

The effective resistivity of the metal line, ρ_{eff}, is then given by:

$$\rho_{eff} = \frac{s^2}{[\frac{A_b}{\rho_b} + \frac{A_{pc}}{\rho_{pc}}]} \qquad \text{Eqn. A1.3}$$

For the case of the Al primary conductor using a Ti barrier of thickness, t, which subsequently reacts with the aluminum to form $TiAl_3$, the effective resistivity is given by:

$$\rho_{eff} = \frac{s^2}{[\frac{A_{TiAl_3}}{\rho_{TiAl_3}} + \frac{A_{Al}}{\rho_{Al}}]} \qquad \text{Eqn. A1.4}$$

where, due to the reaction of Ti consuming 3 times its cross-sectional area in Al, the cross-sectional area of $TiAl_3$ is given by:

$$A_{TiAl_3} = 3[3ts - 2t^2] \qquad \text{Eqn. A1.5}$$

Using these equations, the effective resistivity vs. linewidth is given in Figures 1.3 - 1.4.

Appendix 2

A2.1 Considerations for Al-Ag Diffusion Boundary Conditions

The solution to the diffusion equation used to estimate the Al concentration in the Ag is solved in this appendix. This is used to predict the effective resistivity of the Ag film in section 5.2.6. In solving the diffusion equation it is assumed that the diffusivity of Al in Ag is independent of the Al concentration. It is also assumed that at time zero there is a perfectly smooth interface and no intermixing has taken place. Fast diffusion paths, i.e. grain boundaries, are not considered in this treatment. A solution to the diffusion equation is first derived ignoring the physical limitation imposed by the maximum solid solubility of Al in Ag. However, it might be appropriate to relax this condition, given that the Al concentration might exceed this value due to the existence of non-equilibrium conditions following sputter deposition, and the possibility of high Al concentration at the grain boundaries. This approach is appropriate when the diffusing species has a high solid solubility in the host material. The diffusion equation is also solved assuming that there is a constant concentration at the Ag-Al interface that is equal to the solid solubility limit. This is an appropriate until all the Al has diffused into the Ag. Once this has occurred, the diffusion equation must be solved again under new boundary conditions. Therefore, the second approach is more involved if the solid solubility is sufficiently high that all the barrier material could have dissolved into the host material. The outcome of both methods is similar in terms of the resistivity calculations.

A2.2 Solution to the Diffusion Equation

We seek to find a solution to the following diffusion problem. Two metal layers are brought together and it is assumed that at time zero no diffusion has taken place. All material is confined to $0 < x < l$. This is represented in Figure A2.1. The concentration independent diffusion equation is given by:

$$\frac{\partial C(x,t)}{\partial t} = D\frac{\partial^2 C}{\partial x^2} \qquad \text{Eqn. A2.1}$$

where $C(x,t)$ is the concentration of the diffusing species, x is the distance from the origin, t is the time, and D is the diffusivity.

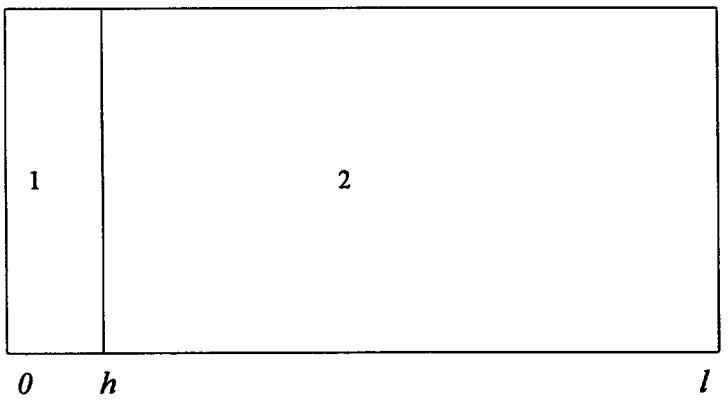

Figure A2.1 Two Finite Layers Brought Together.

Following Crank [130], the solution to the diffusion equation is derived as follows. First we start by considering the system outlined in Figure A2.2.

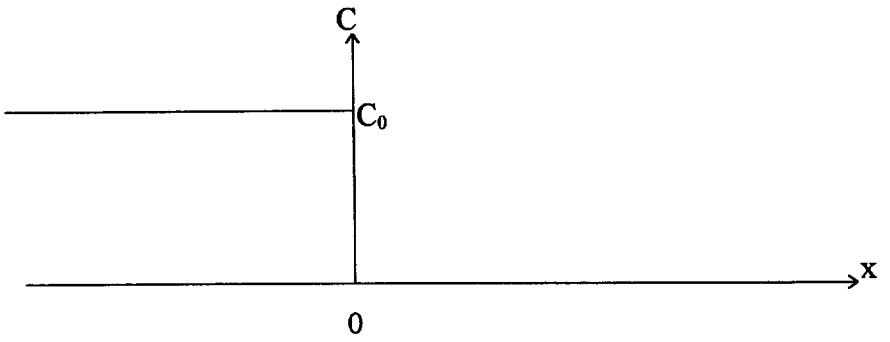

Figure A2.2 Initial conditions of an Interface.

In this example the initial conditions are given by:

$$C = C_0, \quad x < 0, \quad : C = 0, \quad x > 0, \quad t = 0 \qquad \text{Eqn. A2.2}$$

It is trivial to show that the solution is given by:

$$C(x,t) = \frac{1}{2} C_0 \operatorname{erfc} \frac{x}{2\sqrt{(Dt)}} \qquad \text{Eqn. A2.3}$$

Similarly, if the diffusing substance is initially confined to the region $-h < x < +h$, as shown in Figure A2.3, then the solution is given by:

$$C(x,t) = \frac{1}{2} C_0 \left\{ \operatorname{erf} \frac{x+h}{2\sqrt{(Dt)}} - \operatorname{erf} \frac{x-h}{2\sqrt{(Dt)}} \right\} \qquad \text{Eqn. A2.4}$$

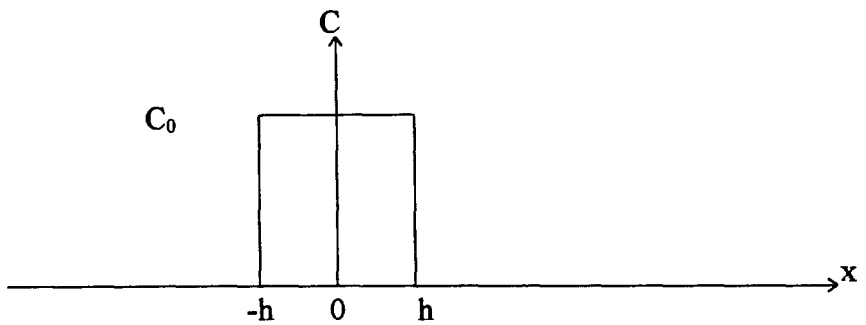

Figure A2.3 Initial concentration of diffusion species confined in the region $-h < x < +h$

Now let us consider the case where the diffusing species is confined for all time in the region $0 < x < l$, as in Figure A2.4.

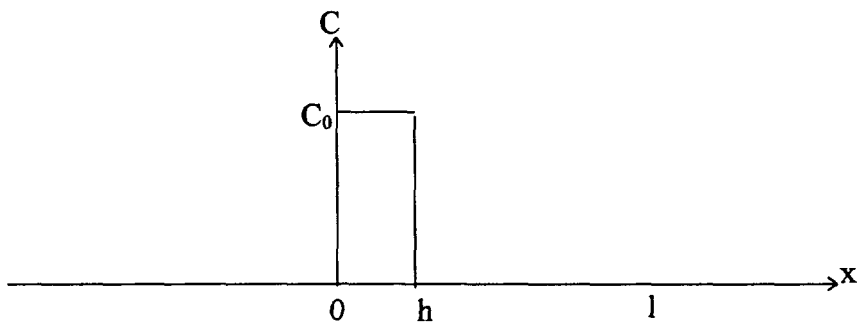

Figure A2.4 Initial concentration distribution.

This is equivalent to the mathematical boundary conditions of Eqn. A2.5.

$$\frac{\partial C}{\partial x} = 0, \qquad x = 0, \qquad x = l \qquad \text{Eqn. A2.5}$$

The condition of no flux through a boundary can be met if the flux is reflected at the boundary. The concentration distribution is therefore a superposition of the original solution and the solution for all the reflections. Therefore the concentration is given by:

$$C = \frac{1}{2} C_0 \left\{ \begin{array}{l} \operatorname{erf}\dfrac{x+h}{2\sqrt{Dt}} - \operatorname{erf}\dfrac{x-h}{2\sqrt{Dt}} \\ +\operatorname{erf}\dfrac{x+h-2l}{2\sqrt{Dt}} - \operatorname{erf}\dfrac{x-h-2l}{2\sqrt{Dt}} \\ +\operatorname{erf}\dfrac{x+h+2l}{2\sqrt{Dt}} - \operatorname{erf}\dfrac{x-h+2l}{2\sqrt{Dt}} \\ +\operatorname{erf}\dfrac{x+h-4l}{2\sqrt{Dt}} - \operatorname{erf}\dfrac{x-h-4l}{2\sqrt{Dt}} + \ldots \end{array} \right\} \qquad \text{Eqn. A2.6}$$

This can be simplified to:

$$C = \frac{C_o}{2} \sum_{n=-\infty}^{\infty} \operatorname{erf}\frac{x+h-2nl}{2\sqrt{Dt}} + \operatorname{erf}\frac{2nl-x+h}{2\sqrt{Dt}} \qquad \text{Eqn. A2.7}$$

This technique can be expanded to solve the diffusion problem in which a thicker material is bounded by two thinner materials as outlined in Figure A2.5.

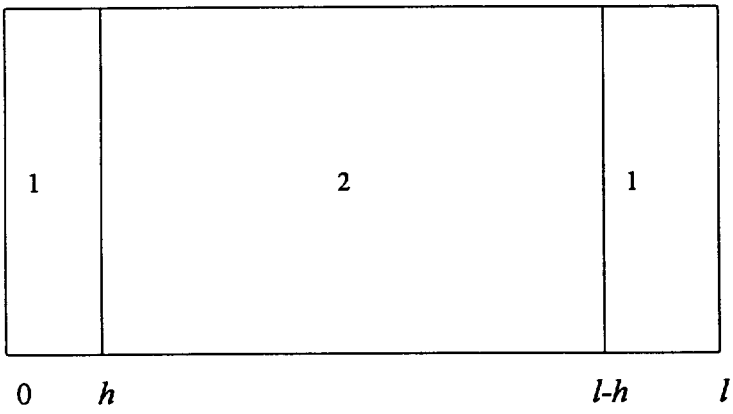

Figure A2.5 Thicker material bounded by two thinner materials.

The solution is given by:

$$C(x,t)=\frac{1}{2}C_0\left\{\begin{array}{l}\operatorname{erf}\dfrac{x+h}{2\sqrt{(Dt)}}-\operatorname{erf}\dfrac{x-h}{2\sqrt{(Dt)}}+\operatorname{erf}\dfrac{x+h-l}{2\sqrt{(Dt)}}-\operatorname{erf}\dfrac{x-h-l}{2\sqrt{(Dt)}} \\ +\text{succesive}\quad\text{reflections}\end{array}\right\} \quad \text{Eqn. A2.8}$$

This can be simplified to:

$$C=\frac{C_o}{2}\sum_{n=-\infty}^{\infty}\operatorname{erf}\frac{x+h-nl}{2\sqrt{Dt}}+\operatorname{erf}\frac{nl-x+h}{2\sqrt{Dt}} \qquad \text{Eqn. A2.9}$$

A2.3 Solution to the Diffusion Equation Considering Solid Solubility

Again consider the problem of a thin layer of material A, of thickness h brought together with material B, of thickness l where $h << l$. An alternative approach to this problem is to consider the concentration at the boundary to be equal to the solid solubility limit until there is no more material A available to diffuse into material B. This assumes that an equilibrium condition exists at the interface, and does not take into account any material at the grain boundaries. Once the diffusion source (material A) has completely diffused into material B, the initial boundary conditions will no longer apply. The new boundary conditions will be such that all the material A is confined between the sides of material B. This is more cumbersome than the first approach. The problem is presented in Figure A2.6.

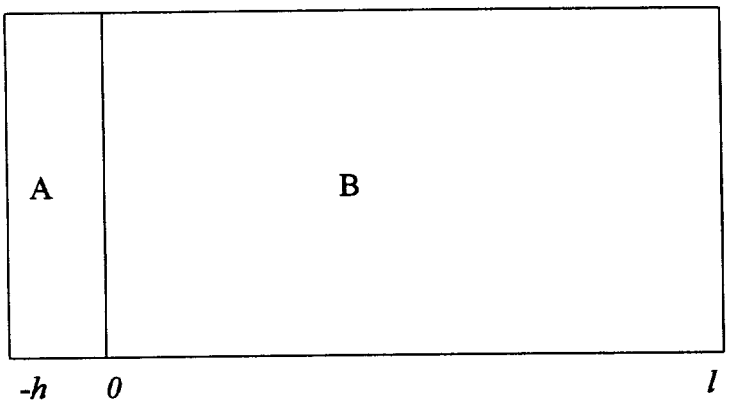

Figure A2.6 Two Finite Layers Brought Together.

The initial boundary conditions are:

$$C(x,0) = 0, \quad t = 0$$
$$C(0,t) = C_{sol}, \quad C(\infty,t) = 0 \qquad \text{Eqn. A2.10}$$

where C_{sol} is the concentration (atoms per cm^3) at the solid solubility limit of the diffusing species in the host material.

For $l >> \sqrt{Dt}$ the solution is:

$$C(x,t) = C_{sol}\ \text{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \qquad \text{Eqn. A2.11}$$

The total amount of material, M_d, diffused into is given by:

$$M_d = 2C_{sol}\sqrt{\frac{Dt}{\pi}} \qquad \text{Eqn. A2.12}$$

The total amount of material A available, M_A, is given by:

$$M_A = \mathrm{P}_A h \qquad \text{Eqn. A2.13}$$

where P_A is the density of material A in atoms/cm^3 and h is the thickness in cm. The concentration, C_{sol}, at the solid solubility limit is given by:

$$C_{\mathrm{sol}} = \frac{S_{AB}}{100}\mathrm{P}_B \qquad \text{Eqn. A2.14}$$

where S_{AB} is the solid solubility limit in atomic percent, and P_B is the atomic density of material B. The material will be exhausted when the following condition is met:

$$\mathrm{P}_A h = \frac{2S_{AB}}{100}\mathrm{P}_B\sqrt{\frac{Dt}{\pi}} \qquad \text{Eqn. A2.15}$$

The diffusion equation would then have to be solved again given the boundary conditions that there is no flux across $x = 0$ or $x = l$, and the initial concentration is that given by Eqn. A2.11.

For the Al diffusion problem discussed in 5.2.6.1, the 40 nm Al barrier would be diffused into the Ag after 7,200 seconds of anneal if the temperature was 403 °C. The Al concentration distributions given by Eqn. A2.7 and Eqn. A2.11 are similar for an anneal at this temperature. For anneal temperatures lower than 403 °C, Eqn. A2.10 will predict a lower concentration of Al in the Ag than will that of Eqn. A2.7, and hence a slightly lower effective resistivity. For anneal temperatures above 403 °C, both approaches will yield very similar results.

Vita

The author, Straford Wild, was born in Liverpool, England on April 21, 1964. He moved to the United States of America in June of 1985. He received a Bachelor of Science degree in Physics from Eastern Illinois University in 1991, and a Master of Science degree in Applied Physics from Oregon Graduate Institute of Science & Technology in 1993. He was admitted to Ph.D. candidacy at the Oregon Graduate Institute in June of 1993. He has been employed as a field process engineer by Novellus Systems, Inc., since March of 1996.