A STUDY OF EFFECT OF PRECIPITATES AND LATTICE DEFECTS ON THE ELECTRICAL PERFORMANCE OF P-N JUNCTIONS

KUNKUL RYOO

B.S., Seoul National University, 1976
M.S., Korea Advanced Institute of Science, 1978

A dissertation submitted to the faculty
of the Oregon Graduate Center
in partial fulfillment of the
requirements for the degree
Doctor of Philosophy
in
Materials Science

August, 1986

The dissertation "A study of effect of precipitates and lattice defects on the electrical performance of P-N junctions" by KUNKUL RYOO has been examined and approved by the following Examination Committee:

William E. Wood, Thesis Adviser
Professor

Robert M. Drosd, Thesis Adviser
Adjunct Professor

John S. Blakemore, Professor

Nicholas G. Eror, Professor

ACKNOWLEDGEMENTS

I would like to gratefully acknowledge the people who have made this dissertation possible. These include all of my friends, fellow students, and faculty.

In particular, I thank professor William E. Wood for providing his general expertise, the wonderful experimental equipment and financial support.

Heartily, I thank Dr. Robert M. Drosd for his continuous and great guidance with expertise and for encouragement along the way.

I thank professor John S. Blakemore and professor Nicholas Eror for their efforts to improve this dissertation.

I thank all TEKTRONIX ICO people for helping me to fabricate and test diodes. I thank ICO manager Jon Schieltz. Especially, I thank Engineer Ann Witkovski for growing epitaxial layers and helping me to finish this work.

Finally, I thank fellow students who helped me to finish this dissertation completely and to keep myself always bright.

CONTENTS

ABSTRACT

A Study of the Effect of Precipitates and Lattice Defects on the Electrical Performance of P-N Junctions

KUNKUL RYOO
Oregon Graduate Center

Supervising Professor : William E. Wood

Ion implantation when used as a doping technique introduces damage to the surface of a silicon wafer. This damage in turn may result in formation of dislocation loops or stacking faults, depending upon the subsequent heat treatment. These defects in turn may degrade electrical properties in a P-N junction. The importance of the location of defects on the P-N junction performance has not been studied in detail. In this work, P-N junctions have been fabricated, tested electrically and analysed with transmission electron microscopy (TEM).

Two types of defects, dislocation loops and stacking faults, were introduced into P-N junctions. Sometimes "dog-bone" shape stacking faults were produced. TEM analysis revealed that the "dog-bone" fault is a stacking fault decorated by precipitates. High magnification (200K) revealed two kinds of precipitates, individual plates and colony clusters. Colonies exhibited Moire fringes which were used to characterize their crystallographic structures. X-ray Energy Dispersive Spectroscopic data from these two precipitates showed that colonies consisted of Ni, Cu and Si, while the plate contained Ni and Si only. It was concluded that the plate type is pure $NiSi_2$ and that the colonies are metastable $(Ni_x,Cu_{1-x})Si_2$ due to Cu alloying.

Diodes containing stacking faults or dislocation loops were fabricated by implanting boron into N-type silicon wafers. Cross section TEM analysis showed that the desired configurations, diodes containing stacking faults in the P-region or extended into the depletion region, or diodes containing dislocation loops in the P-region, the depletion region or the N-region, were obtained.

Diodes containing stacking faults or dislocation loops in the P-region acted as diodes without defects except for increased resistance due to hole scattering. The scattering mechanism for stacking faults was found to be different from that for perfect dislocation loops in the P-region.

Diodes containing stacking faults extending into the depletion region were degraded since partial dislocations surrounding stacking faults provided leakage paths. Diodes containing dislocation loops in the depletion region or N-region still acted as ideal diodes except for higher current levels. In reverse bias, N-region defects showed lower generation current than those in the depletion region. This proved that point defects introduced into the diode may or may not affect the electrical property of P-N junctions depending upon their locations.

I. INTRODUCTION

Integrated circuit complexity of silicon has advanced from small-scale integration, to medium-scale integration, to large-scale integration, and now to very large-scale integration. It tells that the trend is the device miniaturization to less than 1 um, resulting in the ultra large-scale integration which aims the complexity of over 1E8 components per chip before 2000 calendar year(1-3). Even though there are electrical and physical limitations for miniaturization, continuous efforts are being given for this trend(3), one of which is ion implantation. This technology has been substituted for the diffusion technology for doping impurity atoms. However, there exists wafer surface damage problem due to the high energy or dose ion beam. The damage generated normally induces crystallographic defects such as stacking faults or dislocation loops during the subsequent heat treatment stage of device fabrication(4). Defect sizes vary from 10 um to less than 0.01 um. Device miniaturization calls for micro-scale techniques to analyze the physical or chemical properties of submicron device and defect structures.

There are several applicable techniques used for microelectronic purposes shown in Table. 1. AEM(Analytical Electron Microscopy), which includes conventional TEM(Transmission Electron Microscopy) function, EDS(X-ray Energy Dispersive Spectroscopy), and EELS(Electron Energy Loss Spectroscopy) is one of the strongest techniques to analyze the physical and chemical properties of devices or defects. Even

Analytical Techniques	Morphology Analysis	Chemical Analysis	Crystallographic Structure Analysis
Auger Electron Spectroscopy(AES)		●	
Rutherford Backscattering Spectroscopy(RBS)		●	
Seconary Ion Mass Spectroscopy(SIMS)		●	
Scanning Electron Microscopy(SEM)	●	●	
Transmission Electron Microscopy(TEM)	●		●
Analytical Electron Microscopy(AEM)	●	●	●

Table 1. Analytical techniques for planar devices(1)

though difficulties in specimen preparation were the main factor limiting the application of AEM to devices, it is now appreciated that this is a very useful technique and will become an integral part of device fabrication as specimen preparation techniques are improved(1).

The crystallographic structure of stacking faults and dislocation loops in silicon, induced by ion implantation, are well understood(4-5). The electrical impact of dislocations on diodes has been modeled (6), tested(7-8), and summarized(9). The effect of dislocations on minority charge carrier lifetime was studied(10-12) and lifetime was reported with respect to dopant concentrations(13). The energy level of dislocation traps within the silicon bandgap was measured(14-15). The primary dislocations which were produced during crystal growing were believed to provide paths for locally enhanced diffusion of the phosphorous impurities, which caused leakage in the diodes(16). In another work, the high leakage currents was assumed to be related to the presence of dislocations in and near the N^+-region of N^+-P junction(17). The shorts due to dislocations were, also, studied for bipolar junction transistors(18-20) and for MOSFET(21).

Most studies about dislocation effects on diodes were done in connection with ion implantation damage. Generally implantation damage induces dislocation loops in the annealing process of damaged wafers. The distribution of implantation damage has a shape of a Gaussian along the depth direction of a silicon wafer. Dislocation loops are generated at the highest damaged region which is slightly shallower than the highest ion concentration peak(22). Therefore, since loops

are buried at a particular depth, they may be confined within the P-region if boron ions are implanted onto the N-substrate. Growth of an epitaxial layer of single crystal silicon allows loops to be located at or below the P-N junction depending upon the thickness of the epitaxial layer. J. B. Lasky(23) located dislocation loops in the P^+-region and observed the leakage current due to them. Even though there existed a high density of dislocation loops in the P^+-region, it did not degrade the diode characteristics because the junction was far enough from the loops from which the charge carriers were generated. Another study was to locate loops on the metallurgical junction boundary, which showed a significant increase of leakage current did occur (24).

The effects of stacking faults on the electrical properties of diodes were studied by K.V. Ravi, et al(25-26). Boron atoms were diffused to fabricate P^+-N junction with faults already present so that P^+-N junction boundary shape was assumed to be modified by faults. Also, the stacking faults were assumed to be decorated by silicon oxide and boron precipitates which caused the electrical activation of faults that were described as the current multiplication sites(25). In order to fabricate the P^+-region containing faults, a 4.6 um P^+-epitaxial layer was grown. However, there was no consideration about the quality of the epitaxial layer(26). Junction transistors were fabricated to study the effects of faults(27). The leakage current of the emitter-base junction was observed in connection with faults which were not decorated by any detectable precipitate. Faults were also

studied in CMOS and MOS structures. In the CMOS structure the faults extended into the depletion region and caused the leakage current in cooperation with precipitates(28). In the simple MOS capacitor, faults were also found to cause leakage in cooperation with precipitates(29). It can be summarized from the above surveys that there exists a controversy over the effects of precipitates on the P-N junctions and there is no direct comparison study on the junction properties in terms of the defect locations. Also there is no clear explanation as to how defects affect the electrical properties of the junction.

In this work P-N junction diodes have been fabricated with defects such as stacking faults and dislocation loops which are located in the P-region, the depletion region, or the N-region. Boron ions were implanted into the N-substrate. In order to reduce the likely effects due to the different junction depth, junction depths were fixed and circular diodes were fabricated. In order to develop defects, silicon ions were implanted, which induces the formation of dislocation loops or stacking faults depending upon the subsequent heat treatments. Here, the reason why silicon atoms were selected is to reduce the possible side effect such as gas formation if argon atoms used. An epitaxial layer of single crystal silicon having the same resistivity as the substrate has been grown to embed the dislocation loops deeply, which allows loops to be located at or below the P-N junction depending upon the thickness of the epitaxial layer. Stacking faults were located in the P-region or extended into the depletion region by changing the

oxidation time of the damaged wafers due to implantation. Current(I)-Voltage(V) characteristics of all the diodes containing defects has been compared to the defect free control diode and correlated to the defect locations which are identified by TEM.

II. BACKGROUND

II. 1. Ion Implantation

Ion implantation has been a commonly accepted technique for introducing dopant atoms into the silicon crystal lattice. A beam of dopant ions accelarated through a potential of typically 20-200 KeV is allowed to impinge on the silicon wafer surface. The different types of available ion sources provide a wide variety of beams produced with sufficient concentration. Usually 1E12-1E16 ions/cm^2 is a representative dose range, which is the amount equivalent to that required for doping purpose(30).

There are several important aspects of ion implantation to the semiconductor technology in contrast to the thermal diffusion process. The dopant atom dose is easily and accurately controlled by the external control system. Dopants are implanted at lower temperatures at which the conventional thermal diffusion is completely negligible. The dopant concentration is not limited by the ordinary solubility concept and so it allows the investigation of the properties of species which cannot be introduced into the silicon wafer by the thermal diffusion process. Other features are the uniformity of dopant distribution implanted into the wafer and the shallow penetration by controlling the accelerating voltage. These two properties match the recent trend of semiconductor industries to reduce the size of devices. The typical implantation depths are less than 1 um, whereas the thermal diffusion process produces about 1-10 um depths(22,30-31).

Implanted ions have a Gaussian distribution along the depth of the substrate, which may be characterized by a mean distribution range(r_p) as shown in Fig. 1. r_p is the projected distance for the travelling distance(r) of ions. However, in a single crystal substrate, the range distribution depends strongly upon the orientation of the crystal with respect to the implantation direction since crystal structure offers the channeling effect of implantation species. For example, the exact [100] direction for ion implantation provides the channels between atoms like an open honeycomb structure, while the crystal appears to be much more closely packed and channels are much less evident if the crystal is tilted. An ion entering the crystal tilted a few degrees with respect to the [100] axis will accordingly lose a significant fraction of its energy quickly in a series of nuclear collisions and so the tilted crystal can be assumed to be amorphous(30-31). As a result, the theory developed for the amorphous substrate may be applied to estimate the range distribution for the tilted crystal.

Range distribution which is called LSS theory was modelled by Lindhard, Scharff and Schiott. LSS theory assumes that there are two kinds of mechanisms for stopping ions in the substrate. The nuclear stopping is more dominant at lower implantation energy, whereas the electronic stopping is important at higher energy. In the case of boron ions, for example, the electronic stopping dominates for an energy larger than 10 KeV for the silicon substrate. As the atomic number increases, the energy for electronic stopping also increases(30, 32).

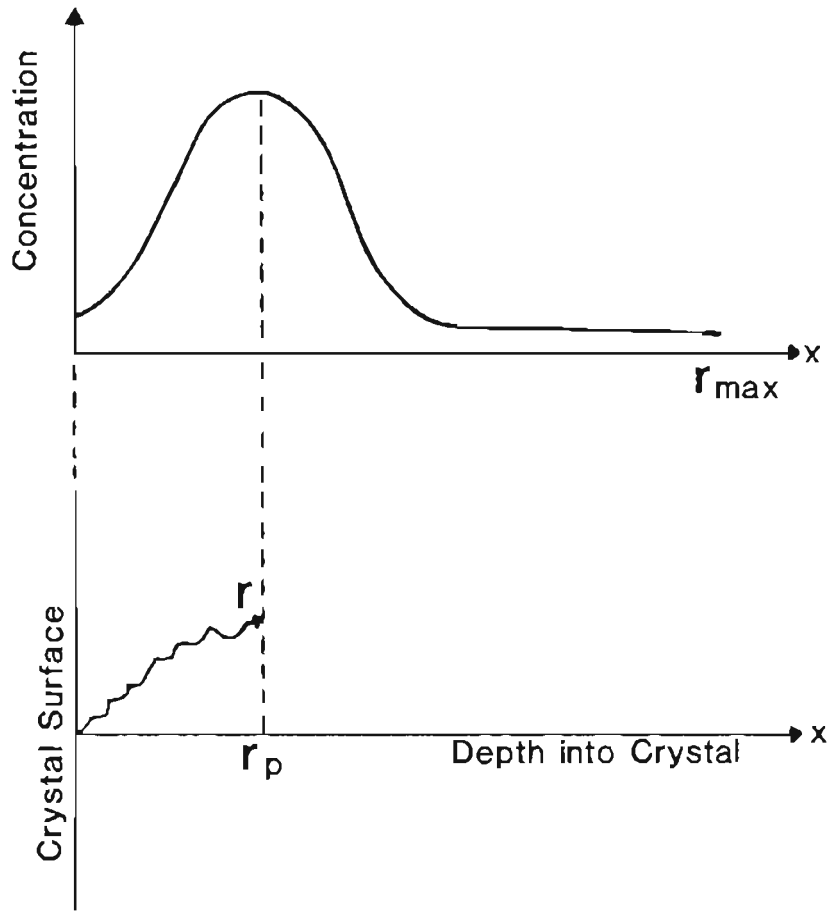


Figure 1. Distrbution of implanted atoms in the crystal(31)

The disadvantage of ion implantation is that it results in the formation of a large number of interstitial atoms and vacant sites. If the dose exceeds a critical level, an amorphous layer may develope. Two possible theories have been proposed to explain this. The first proposes that near the end of each ion track a small amorphous zone is created. As the number of implanted ions increases the density of these zones reaches a point where they overlap and a continuous amorphous layer is created. The second theory assumes that although the individual ions creates a high density of point defects near the end of their paths, the silicon wafer remains crystalline. When a critical density of defects is reached, the lattice transforms to an amorphous structure as a transformation to a metastable state(5). Depending upon the implantation temperature, the resulting crystallographic structure can be separated into two categories. If implantation is performed at low temperature such as liquid nitrogen temperature, the damaged surface remains as an amorphous structure. However, if implantation is performed at an elevated temperature such as room temperature, some in-situ annealing occurs due to heat generated during implantation, and the amorphous structure re-transforms to the crystalline structure(33-35). Point defects generated by ion implantation may also result in the formation of dislocation loops or stacking faults depending upon the subsequent heat treatment which may cause electrical problems for semiconductor structures.

II. 2. Annealing of ion implanted silicon wafers

Ion implantation introduces various types of lattice disorder. In order for doped silicon to be electrically activated, dopant atoms should be in substitutional positions, which is usually accomplished by thermal annealing. A typical defect which is induced by annealing of the amorphous silicon layer is the dislocation loop. Dislocation loops form at a particular depth from the wafe surface where the damage is most severe. This is slightly shallower than the maximum of concentration profile(22). When the dislocation loops are smaller than a few hundred angstroms, they generally have Frank partial burgers vector(b) which is 1/3[111]. It is reasonable to assume that they are a result of condensation of vacancies or interstitial atoms. This condensation occurs on {111} planes as a disc which is surrounded by the Frank partial dislocation(36). During further annealing the existing loops may grow by condensing more point defects and eventually intersect other loops resulting in a stable dislocation network. Perfect dislocations in silicon are dissociated and so they consist of two partial dislocation lines with the dissociation distance of about 50 A(37).

Dislocation loops induced by ion implantation are difficult to avoid and may cause the degradation of the electrical properties of a P-N junction depending upon their position within the diode. Particularly, dislocation loops induced by ion implantation form a band structure at a particular depth where the damage is maximized and so the exact location of this band can be defined. The scope of this work is that the dislocation band is located in a certain depth with

respect to P-N junction boundary and the electrical effect is observed. The location of dislocation bands is the P-region, the depletion region, or the N-region. To locate the dislocation band in the depletion region or the N-region requires growing an epitaxial layer.

II. 3. Oxidation of ion implanted silicon wafers

An oxide layer on a silicon wafer is very important for silicon technology since it takes on a role as a diffusion barrier, implantation barrier, and electrical insulator in the device structure. Silicon dioxide can be formed by chemical vapor deposition or by thermal oxidation. The growth of silicon oxide by thermal oxidation is very important since it provides oxides of greater physical and electrical stability, compared to deposited oxides.

There are five different phases of silicon oxide(38). The properties of silicon oxide have been summarized(39). Thermal oxidation kinectics have been examined in detail by Deal and Grove(40), even though some modification was proposed(41). They assumed that, first, oxidizing gases were transported to the silicon surface and then oxidizing gases diffused through the growing oxide layer to reach the fresh inner silicon surface. Finally an oxidation reaction took place at the silicon surface. The derived equation can reduce to the well-known parabolic oxidation law for relatively long periods(a) and to the linear law for relatively short periods(b) as shown in Fig. 2.

Experiments have shown that the oxidation rate is higher in a steam ambient than in dry oxygen(42), the oxidation rate for a (111) wafer

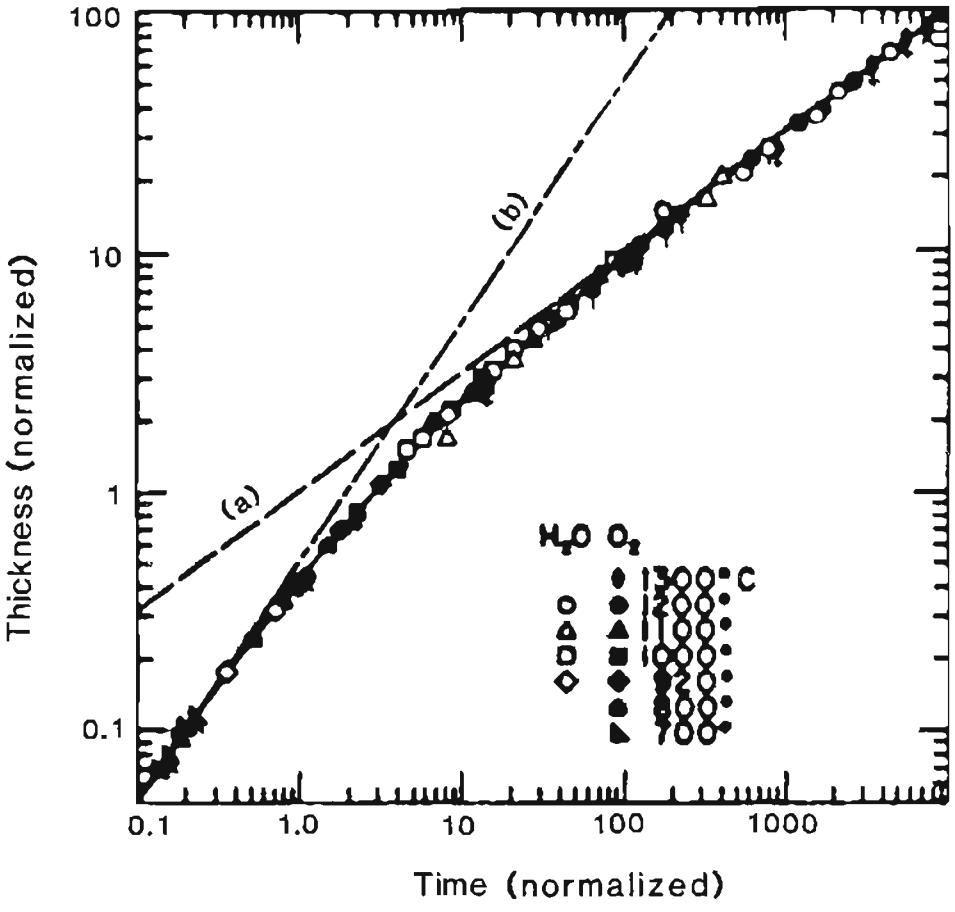


Figure 2. Thermal oxidation rate of silicon(40)

is higher than a (100) wafer, and the oxidation rate is higher with a slight halogen ambient than without. Also, as the halogen concentration increases, the oxidation rate increases and a oxide of higher dielectric property may be obtained(4).

During oxidation, stacking fault generation at the wafer surface takes place as a result of surface damage by ion implantation. Stacking faults in silicon crystal have habit planes of {111}. Stacking faults are surrounded by the Frank partial dislocation which has burgers vector of 1/3[111](43). Oxidation-induced stacking faults in silicon are always found to be extrinsic in nature. It means that they are composed of the extra planes of atoms condensed and bounded by Frank partial dislocation(44).

When oxidation-induced stacking faults nucleate and grow, they are relatively uniform in size. This makes it possible to control the depth of stacking faults with respect to the P-N junction boundary, by controlling temperature and time of oxidation. In this work stacking faults are located in the P-region and extended into the depletion region by simply prolonging the oxidation time.

II. 4. Transmission Electron Microscopy (TEM)

TEM is one of the most powerful techniques to characterize the microstructure of silicon wafer. Whereas scanning electron microscope has a capability of 100K magnification, 50 A resolution and surface observation , TEM has a capability of 1000K magnification, 2 A resolution and bulk observation. This allows TEM to characterize the fine

structure in silicon technology. Another strong point of TEM is that electron diffraction can be used to analyze very fine precipitates or very fine structure. AEM can give chemical analysis of very fine precipitates.

The basic mechanical components of TEM are electron gun, condenser lens and aperture, specimen holder, objective lens and aperture, intermediate lens and aperture, project lens and screen. Each lens is capable of magnifying and focusing the image, but also has optical aberrations such as astigmatism as well as chromatic and spherical aberration. These can be reduced by using the stigmator and the high acceleration voltage of electrons.

Silicon has a diamond structure with four covalent bonds as shown in Fig. 3(45). Eight atoms per unit cell are residing at

$$000 + \text{face-centering translation and}$$

$$\frac{111}{444} + \text{face-centering translation,} \qquad \text{——————————(1)}$$

where the face-centering translation is 000, $0\frac{11}{22}$, $\frac{1}{2}0\frac{1}{2}$, and $\frac{11}{22}0$(46). The incident electron beam entering into the silicon crystal reacts with silicon atoms, resulting in atomic scattering. Structure factor calculation with eq. (1) shows that {111}, {220}, {311}, {400}, {331}, {422}, ——— planes are allowed to make the diffraction spots. Here structure factor is a measure of the scattering ability of the unit cell and calculated from the atomic scattering amplitude of the indi-

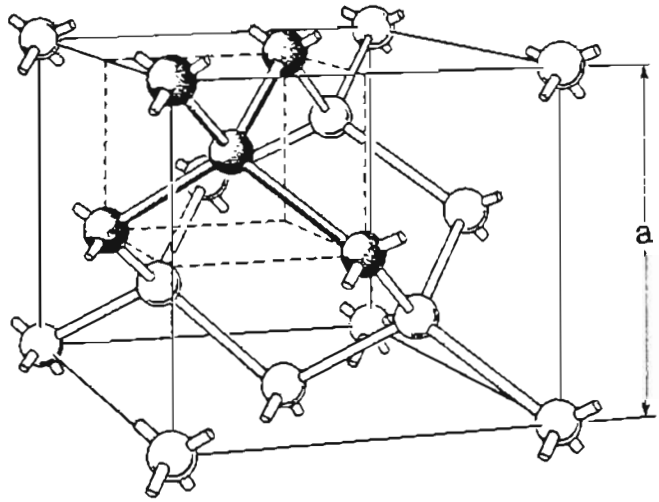


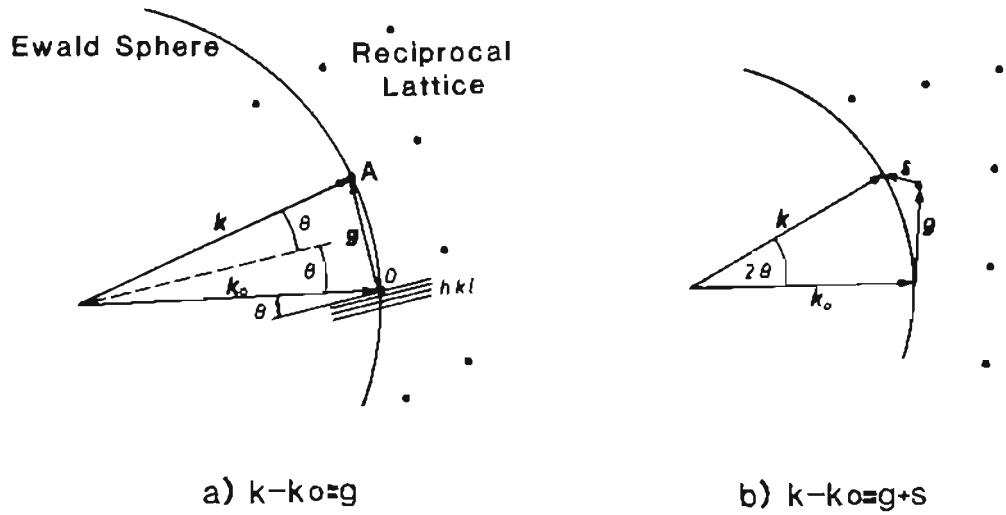
Figure 3. Diamond cubic structure of silicon unit cell(45)

vidual atoms in the unit cell of eq. (1). If the structure factor for a certain plane is zero, then that plane does not produce a diffraction spot. If the structure factor has a nonzero value, a diffraction spot is produced.

The Ewald sphere has a radius($|k|$) in reciprocal space of $1/\lambda$(λ is the electron wavelength) and is 40/A, if the accelaration voltage is 200 KeV. The plane spacing of (111) in silicon is 3.13556 A which gives the smallest spacing of 0.32/A in reciprocal space. Therefore, the radius of a Ewald sphere is very large compared to the reciprocal lattice spacing. Thus the segment of Ewald sphere cutting two reciprocal lattice points(OA) in Fig. 4, a) can be approximated to be straight line(36,47-48). Bragg's law is derived from this configuration to be $\lambda=2d\sin\theta$, where d is the plane spacing and θ is the Bragg angle. Since λ is so small, θ will generally be less than 0.5 degree. Thus, it is approximated that the only planes nearly parallel to the incident electron beam direction will generate diffraction spots. If the incident electron beam direction of [uvw] is the zone axis of (hkl) planes parallel to that axis, the dot product of two vectors should be zero.

$$hu + kv + lw = 0 \qquad \text{——————————————————————(2)}$$

If the beam direction, for example, is [111], then only $(\bar{2}20)$, $(20\bar{2})$, $(0\bar{2}2)$,$(\bar{4}22)$, $(\bar{2}\bar{2}4)$, $(2\bar{4}2)$, ——— planes are allowed in the electron diffraction of silicon.



a) k−ko=g

b) k−ko=g+s

Figure 4. Diffraction conditions for electron microscopy(36)

The general diffraction condition can be expressed with wave vector concept from Fig. 4 as

$$K - K_o = g + s \qquad (3)$$

and the exact Bragg's condition is expressed by eliminating s which is the deviation from the Bragg's condition and is controlled by tilting the specimen.

$$K - K_o = g \qquad (4)$$

The electron beam is sometimes scattered inelastically from the crystal. If the inelastically scattered electron beam meets the Bragg condition with a particular planes, it is also diffracted. Since electron energy loss due to inelastic scattering is small, the Bragg angle of a electron beam suffering inelastic scattering is almost equal to the elastically scattered beam. So planes which produce the diffraction spots, also, produce the diffracted lines having a conical shape the curvature of which is so large that the image of this cone on the film can be considered as straight line as shown in Fig. 5. The beam scattered inelastically towards the transmitted beam direction has higher intensity so that it causes the bright line far away from and the dark line near the transmitted beam spot. These are called Kikuchi lines and obtained in the thicker specimen, since there is a higher probability that the inelastic scattering takes place in

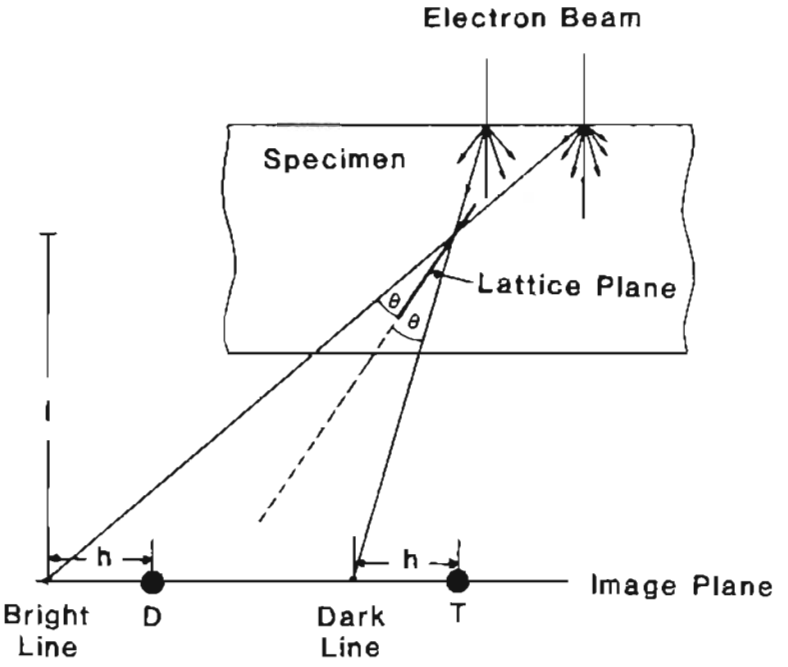


Figure 5. Formation of Kikuchi lines(36)

the thicker specimen. If Kikuchi lines of a given g-vector are superimposed on the diffraction spot of a same g-vector, the exact Bragg condition is satisfied and s equals to zero, where s may be expressed as $|s|=|g|h/l$. Here h is the distance from the diffration spot to Kikuchi line of a given g-vector on the film and l is the camera length.

Stacking faults on the {111} planes of silicon have the displacement vector $b=1/3[111]$, surrounded by a Frank partial dislocation as mentioned previously. Selection of a particular g-vector allows groups of stacking faults to be visible and other groups of them to be invisible due to the different orientations of displacement vectors. Thus the dot product of g and b vectors can characterize stacking faults. The investigation of the fringe configuration inside the stacking fault also gives the informations of its inclination with respect to the wafer surface and of extrinsic or intrinsic status of the stacking fault.

There are two (amplitude and phase) main contrast mechanisms in the TEM image formation. First, there is a contrast due to the scattering difference for different materials or different thickness. This is called the amplitude contrast. If some electrons are intercepted by the object aperture, their absence from the transmitted beam, also, produces amplitude contrast. This is caused by the diffraction and produces the contrast in the image. Therefore, the smaller an object aperture size becomes, the more the diffracted electrons are intercepted and higher contrast is obtained. This is the normal amplitude contrast mechanism. Secondly, in the high resolution contrast mecha-

nism, more than two beams emerging from specimen react to generate the phase contrast on the film. A specimen may be characterized by the change in amplitude and phase between the incident electron wave and the emergent wave at any point. The instrument may be characterized by the amount of defocus and the spherical aberration of the object lens. Two beams passing the specimen through the objective lens, therefore, have a particular property and construct a particular image on the screen depending upon the specimen and the objective lens condition. Here a crystalline specimen acts as a diffraction grating for the incident electron beam, giving rise to the diffracted beams whose spatial distribution is the Fourier transformation of the specimen. Then the objective lens system allows the diffracted beams and the transmitted beam confined in the objective aperture to interact on the screen, thereby performing the inverse Fourier transformation which is the high resolution lattice imaging. If no objective aperture is used, then too many beams interact together and the background noise is too high to resolve lattice images(49-52).

There are three techniques to confine the transmitted beam and the diffracted beams using the objective aperture to obtain lattice imaging. The first is to confine the transmitted and one diffracted beam evenly inside the aperture without tilting the beam. The second is to confine the transmitted beam and one diffracted beam evenly with tilting the beams. The third is to obtain the zero Laue zone axis which is coincident with a Kikuchi pole in the thicker specimen(53-54).

A brief mathematical expression gives a clearer idea of the phase

contrast mechanism. The phase shift (γ) due to the instrument is expressed as

$$\gamma = \frac{\pi}{\lambda}\left[\frac{C_s}{2}\left(\frac{y}{f}\right)^4 - \triangle\left(\frac{y}{f}\right)^2\right] \qquad (5)$$

where C_s is the spherical aberration of objective lens, y is the distance perpendicular to the beam direction on the aperture plane, f is the focal length of objective lens, and $\triangle$ is the amount of defocus. The form of intensity variation(H) on the screen due to the inverse Fourier transformation is expressed in terms of γ.

$$H = 1 - 2a\cos\gamma - 2\beta\sin\gamma \qquad (6)$$

where a and β are the amplitude and phase changes due to the specimen, repectively. The microscope response is characterized by the amplitude contrast transfer function($\cos\gamma$) or by the phase contrast transfer function($\sin\gamma$). Since high resolution specimens are very thin and uniform, the amplitude change(a) is very small and consideration is focused only on the phase contrast transfer function. The phase contrast transfer function obtained at 200 KeV with the H-800 Hitachi microscope shows that there exists a broad high value of phase contrast transfer function corresponding to the faithful transmission of information at the range of spatial frequency or reciprocal space as shown in Fig. 6. If $|\sin\gamma|$ exceeds about 0.2, lattice imaging of

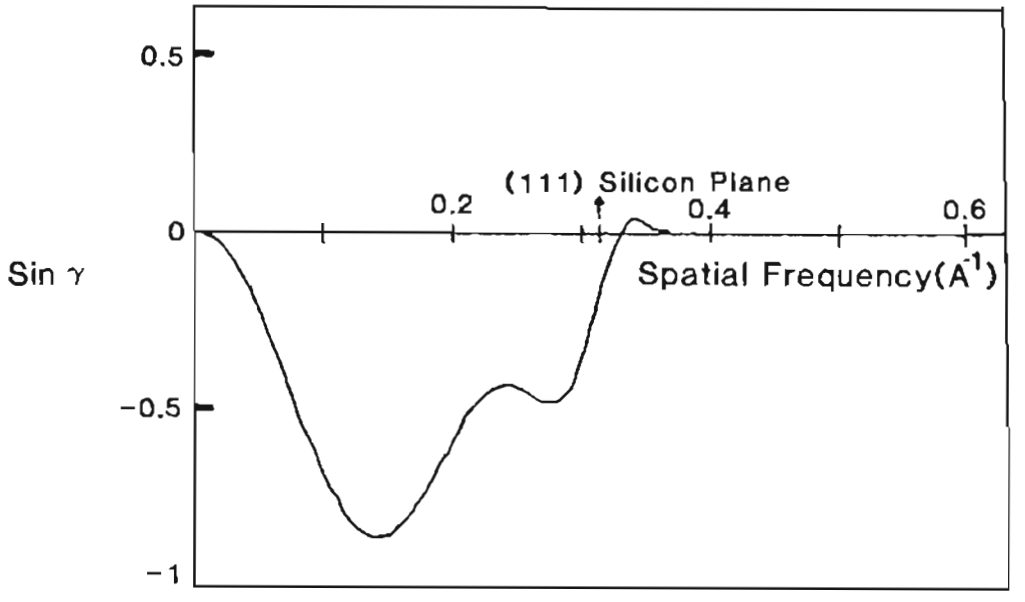


Figure 6. Phase contrast transfer function of H-800 Hitachi AEM at 200 KeV with 1000 A overfocus

3.14 A (111) silicon planes can be obtained. However, 2 A is near the limit of resolution with 200 KeV in silicon as pointed by Ourmazd, et al(55).

There is another topic to be discussed which is Moire fringes. The mechanism for formation of Moire fringes is essentially identical to that for lattice imaging in terms of phase contrast. A difference is that the fringe spacing is normally much greater than the lattice imaging case. For example, if precipitation occurs in silicon there are extra diffraction spots from precipitates around the silicon matrix diffraction spots. The extra spots interact with silicon spots to form phase contrast which results in Moire fringes on the viewing screen. There are two types of Moire fringes, translational and rotational, depending upon the locations of precipitate diffraction spots with respect to the silicon matrix spots in the back focal plane of the objective lens. By tilting the specimen, particular g-vectors can be exited and different spacings of Moire fringes can be obtained. Therefore, based on this concept combined with tilting the specimen, the crystal structure of precipitates can be characterized.

II. 5. Current(I)-Voltage(V) characteristics of diodes

Since the diffusion current theory of a P-N junction was introduced by Shockley(56), it has been well developed and summarized(42,57-59). This theory is based on the diffusion of charge carriers due to the concentration gradient and the drift of charge carriers due to the

subsequently developed electric field at the P-N junction. Joining P and N type silicon materials induces a current by the diffusion of charge carriers, because a large density gradient of charge carriers exists at the junction. Electrons diffusing from the N to P-region leave behind the donor ions(N_d^+) in the N-region which are immobile, resulting in a positive space charge region, and vice versa for holes in the P-region. The developed space charge region is also called the depletion region. The electric field (E) formed by the space charge subsequently creates a drift current from the N to P-region, opposing the diffusion current. Since no net current[$I_p(x)$] flows across the unbiased junction, the drift and diffusion currents of holes must exactly cancel.

$$I_p(x) = qA[up(x)E(x) - D\frac{dp(x)}{dx}] = 0 \qquad \text{---------- (7)}$$

(drift) (diffusion)

where q is the electrical charge, A is the cross-sectional area of a junction, u is the hole mobility, p(x) is the hole concentration along the x-direction perpendicular to the junction boundary, and D is the hole diffusivity. Rearranging with the Einstein relation, qD=ukT, and integrating eq. (7) gives the following result.

$$\frac{p_p}{P_n} = EXP[\frac{qV_o}{kT}] \qquad \text{---------- (8)}$$

where p_p is the hole concentration in the neutral P-region, p_n is the hole concentration in the neutral N-region, V_o is the contact potential which is the potential difference between the N-region potential (V_n) and the P-region potential(V_p), k is the Boltzmann's constant and T is the absolute temperature.

It is assumed that the space charge within the depletion region comes from only the uncompensated donors and acceptors, because there are very few mobile charge carriers left within the depletion region due to the high electric field developed. The positively uncompensated charge density in the N-side of the depletion region is, then, just q times the concentration of donors and the negative charge density in the P-region is -q times the concentration of acceptors, if all the dopants are assumed to be ionized. The neutrality condition for the total uncompensated charges in the either side gives the condition.

$$qAx_{po}N_a = qAx_{no}N_d \qquad (9)$$

where x_{po} is the penetration of the depletion region into the P-region and x_{no} is the penetration into the N-region from the metallurgical junction. The total width of the depletion region (W) is the linear sum of these two penetrations.

Poisson's equation describes the electrical field developed by donors and acceprors in the depletion region.

$$\frac{dE(x)}{dx} = \frac{q}{\epsilon} N_d \quad \text{for } 0<x<x_{no}$$

$$\frac{dE(x)}{dx} = -\frac{q}{\epsilon} N_a \quad \text{for } -x_{po}<x<0 \qquad \text{——————————(10)}$$

where ϵ is the permitivity of silicon. This equation tells that there is a absolute maximum value of the electric field(E_{max}) at x=0; and E(x) is negative everywhere within the depletion region. E_{max} is evaluated by integration of eq.(10).

$$E_{max} = -\frac{q}{\epsilon} N_d x_{no} = -\frac{q}{\epsilon} N_a x_{po} \qquad \text{——————————(11)}$$

Conceptually the electric field is the gradient of potential.

$$E = -\frac{dV}{dx} \qquad \text{——————————(12)}$$

Therefore, the contact potential can be derived as follows.

$$V_o = \frac{1}{2} E_{max} W \qquad \text{——————————(13)}$$

Combining eq. (9), (11) and (13), x_{no} and W values are obtained as follows, if N_a is much greater than N_d.

$$W = x_{no} = [\frac{2\epsilon V_o}{qN_d}]^{1/2} \qquad \text{——————————————————(14)}$$

When an external bias is applied to the P-N junction, a voltage drop will occur across the junction. In most P-N junctions, the lengths of P and N neutral regions are so small and the doping is usually so heavy that it is asssumed that the resistance, and therefore the voltage drop, is low in each neutral region and thus an applied voltage drops entirely across the depletion region. The electrostatic potential barrier at the junction changes due to the external bias(V), since an external bias raises or lowers the electrostatic potential in the P neutral region relative to the N side, and the width of the depletion region decreases or increases. Integration of eq. (12) between V_n and V_p+V gives the mathematical result of the depletion region for the external bias.

$$V_n - (V_p+V) = V_o - V = -\frac{1}{2} E_{max} W \quad \text{and} \qquad \text{——————————(15)}$$

$$W = [\frac{2\epsilon(V_o-V_f)}{qN_d}]^{1/2} \qquad \text{——————————————————(16)}$$

This equation tells that the forward bias allows the depletion region to shrink and the reverse bias allows the depletion region to expand.

The carrier concentration of the depletion region boundaries at the P-region and the N-region for the biased conditions can be expressed in a similar manner to zero bias condition of eq. (8).

$$\frac{p(-x_{po})}{p(x_{no})} = EXP[\frac{q(V_o-V)}{kT}] \quad \text{----------(17)}$$

Assuming $p(-x_{po})=P_p$, dividing eq. (8) by (17) gives the excess hole concentrations in the N-region for biased conditions.

$$\frac{p(x_{no})}{p_n} = EXP[\frac{qV}{kT}] \quad \text{----------(18)}$$

This exponential increase of hole density from an equilibrium value at x_{no} with forward bias is called the minority carrier injection. The excess hole density(Δp_n) at x_{no} from value is the difference between $p(x_{no})$ and p_n.

$$\triangle p_n = p(x_{no}) - p_n = p_n[EXP(\frac{qV}{kT}) - 1] \quad \text{----------(19)}$$

For steady state, the diffusion equation for holes becomes

$$\frac{d^2\delta p}{dx^2} = \frac{\delta p}{L^2} \qquad \text{——————————————————————(20)}$$

where δp is the distribution of excess holes in the neutral N-region and L is the hole diffusion length. Combining eq. (19), (20) and (21) gives the distribution of injected holes.

$$\delta p = \triangle p_n \mathrm{EXP}(-\frac{x}{L}) = p_n[\mathrm{EXP}(\frac{qV}{kT}) - 1]\mathrm{EXP}(-\frac{x}{L}) \qquad \text{————————(21)}$$

And the final diffusion current of the injected holes at x_{no} due to the external bias is;

$$I_p(x_{no}) = -qAD\frac{d\delta p(x_{no})}{dx_{no}} = \frac{qADp_n}{L}[\mathrm{EXP}(\frac{qV}{kT} - 1] \qquad \text{————————(22)}$$

This equation is called the diode equation and means that holes are injected by bias and recombine with electrons in the N neutral region causing a diffusion current(I_d). Therefore, if V is positive and large, then eq. (22) further reduces its form.

$$I_d = \frac{qADp_n}{L}\mathrm{EXP}(\frac{qV}{kT}) \qquad \text{——————————————————————(23)}$$

If V is negative, eq. (22) becomes to be independent of the applied

voltage, and the reverse current approaches the saturation current(I_s).

$$I_s = - \frac{qADp_n}{L} \qquad (24)$$

Since the actual data do not always follow this theory precisely, Shockley has introduced the concept of generation and recombination of electron-hole pairs(EHP) within the depletion region(60). There are three regions where EHP generation and recombination occur. These are the P neutral region, the depletion region or the N neutral region. If EHP generation or recombination occur in the neutral regions, it is a diffusion current as mentioned previously and if EHP generation or recombination occurs in the depletion region, it is defined as the generation or recombination current.

For reverse bias the concentration of charge carriers within the depletion region is reduced well below their equilibrium concentration because of a high electric field across the depletion region. Due to the reduction in charge concentration the generation process is more important than the recombination process. So every EHP generated will be swept to the two neutral regions and thus produce a generation current. For forward bias the case is reversed and the recombination process which produces recombination current is more important.

The generation rate (U) was derived based on the SRH(Shockley-Read-Hall) model(61).

$$U = -\frac{n_i}{2t} \qquad (25)$$

where n_i is the intrinsic concentration of charge carriers and t is the effective lifetime of charge carriers within the depletion region. The generation current(I_g) can be expressed in terms of n_i and W.

$$I_g = qA|U|W = \frac{qAn_iW}{2t} \qquad (26)$$

It is shown that the generation current is proportional to n_i and W. I_g increases with n_i, which is an exponential function of temperature, and with the depletion region,W, which is proportional to the square root of the applied voltage. The ratio of the generation current to the saturation current for the reverse bias gives a clear comparison of two values.

$$\frac{I_g}{I_s} = \frac{Ln_iW}{2Dtp_n} = \frac{N_dW}{2Ln_i} \qquad (27)$$

At room temperature with a 2 Ω-cm N-type silicon wafer, $N_d=1000n_i$ and so $I_g=1000I_s$, assuming W=L since they are in the range of micron based on calculation. However, as temperature increases, n_i increases exponentially and so eventually I_s exceeds I_g.

In forward bias the diffusion current which is caused by the recom-

bination of injected holes from the P neutral region to the N neutral region is dominant at high forward bias. However, if recombination occurs within the depletion region it produces a recombination current. At lower forward bias the injection level is relatively low and the depletion region is not shrunk much. Therefore, the recombination current will dominate the diffusion current. The recombination current(I_r) within the depletion region is approximated using the recombination rate which equals the generation rate of a reverse bias case multiplied by the exponential factor.

$$I_r = -\frac{qAn_iW}{2t}\ EXP(\frac{q|V|}{2kT}) \qquad (28)$$

The ratio of I_r to I_d for forward bias shows that for silicon at room temperature the recombination current generally dominates at lower forward bias while the diffusion current dominates at higher bias. From eq. (23) and (28) the diode equation can be generalized for forward bias as follows.

$$I = I_o\ EXP(\frac{qV}{nkT}) \qquad (29)$$

Here, I_o is a constant and n is the ideality factor. n equals one for the diffusion current and two for the recombination current.

Finally, there exist three types of measurable currents from the

silicon P-N junction, which are the diffusion current, the generation current and the recombination current as shown in Fig. 7. For reverse bias the saturation current and the generation current compete each other but for forward bias the diffusion current and the recombination current compete each other, depending upon the bias, temperature and the doping level.

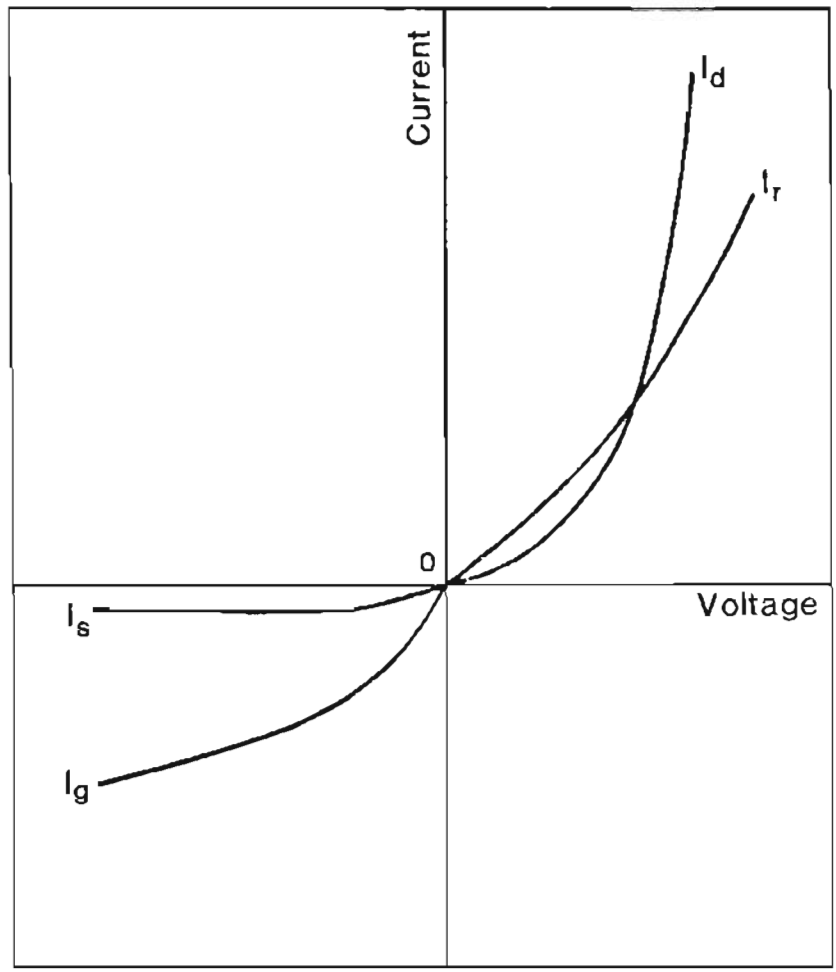


Figure 7. Current-Voltage characteristics of P-N junction

III. EXPERIMENTAL PROCEDURES

III. 1. Fabrication of P-N junctions containing dislocation loops

A schematic diagram for the fabrication of a P-N junction containing dislocation loops is shown in Fig. 8. The starting materials were N-type (111) silicon wafers having 2-6 Ω-cm resistivity selected from a commercial supplier such as Wacker or Monsanto. Wafers of 3 inch diameter and of 250 um thickness were cleaned using a commercial FSI cleaner, in which H_2O_2, H_2SO_4, HCl, NH_4OH, HF acids and DI water flowed in a programmed sequence. The wafers for fabricating P-N junction diodes were, first, oxidized at 1000 C for 4 hours in steam to grow a 1 um thick oxide layer which would be a barrier for the subsequent silicon ion implantation. Photoresist was deposited on the silicon oxide, exposed, and developed using the mask which left circular openings of 200 um diameter. Oxide within these openings was etched away (4 parts DI water and 1 part HF) at an etch rate of 1200 A/min at 25 C, and then the photoresist was removed. Wafers were again oxidized at 1000 C for 40 minutes in steam to grow a 3000 A oxide layer within the openings, which was subsequently etched away leaving behind 1500 A deep basins from the substrate surface. In order to confine defects within the diode, the mask with circular openings of 210 um diameter was used to fabricate P-N junctions later. When photoresist was developed using this mask, the reference positions were needed to align two different size openings. However, since thermal oxide was etched away, it had not been possible to identify the locations of the

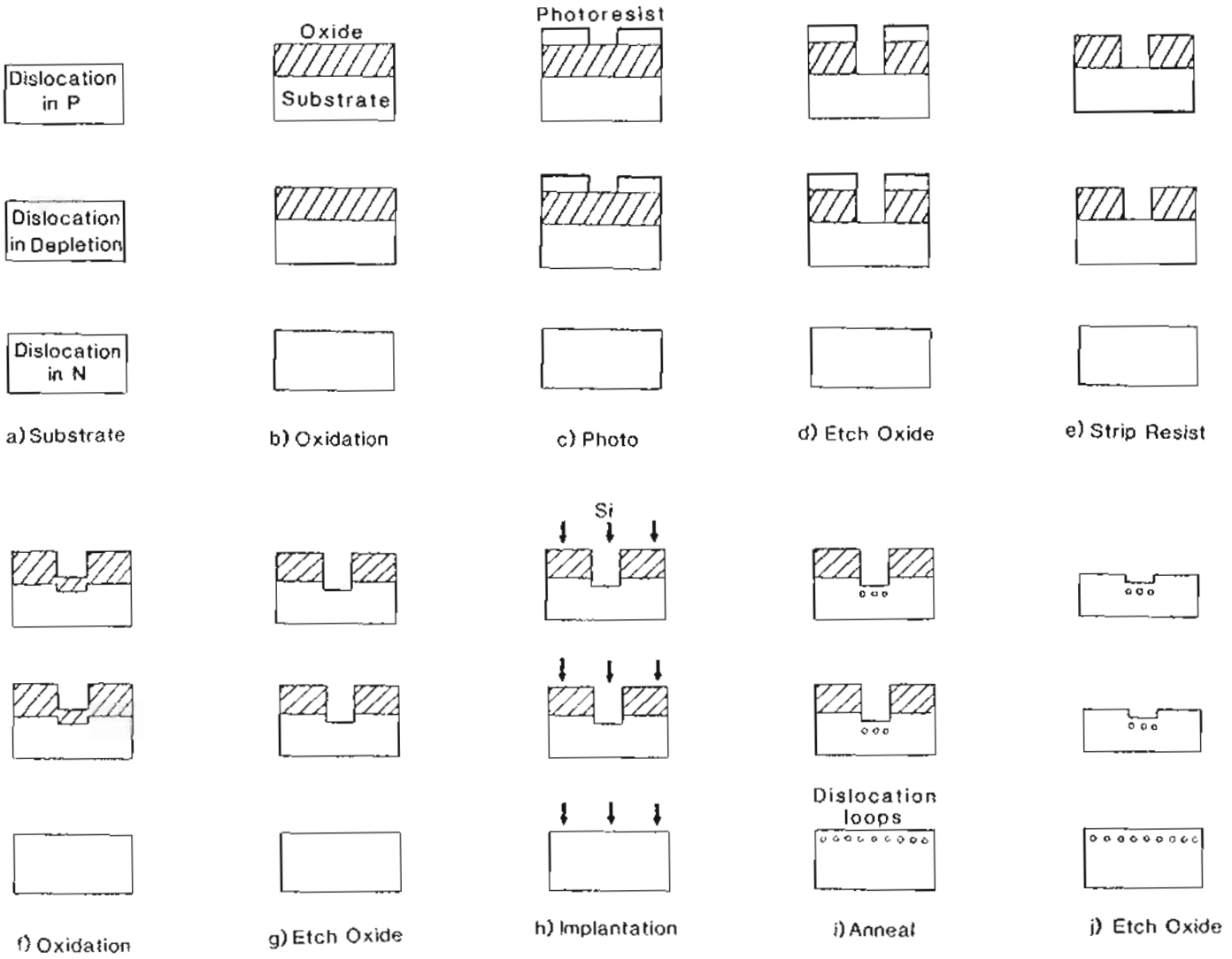
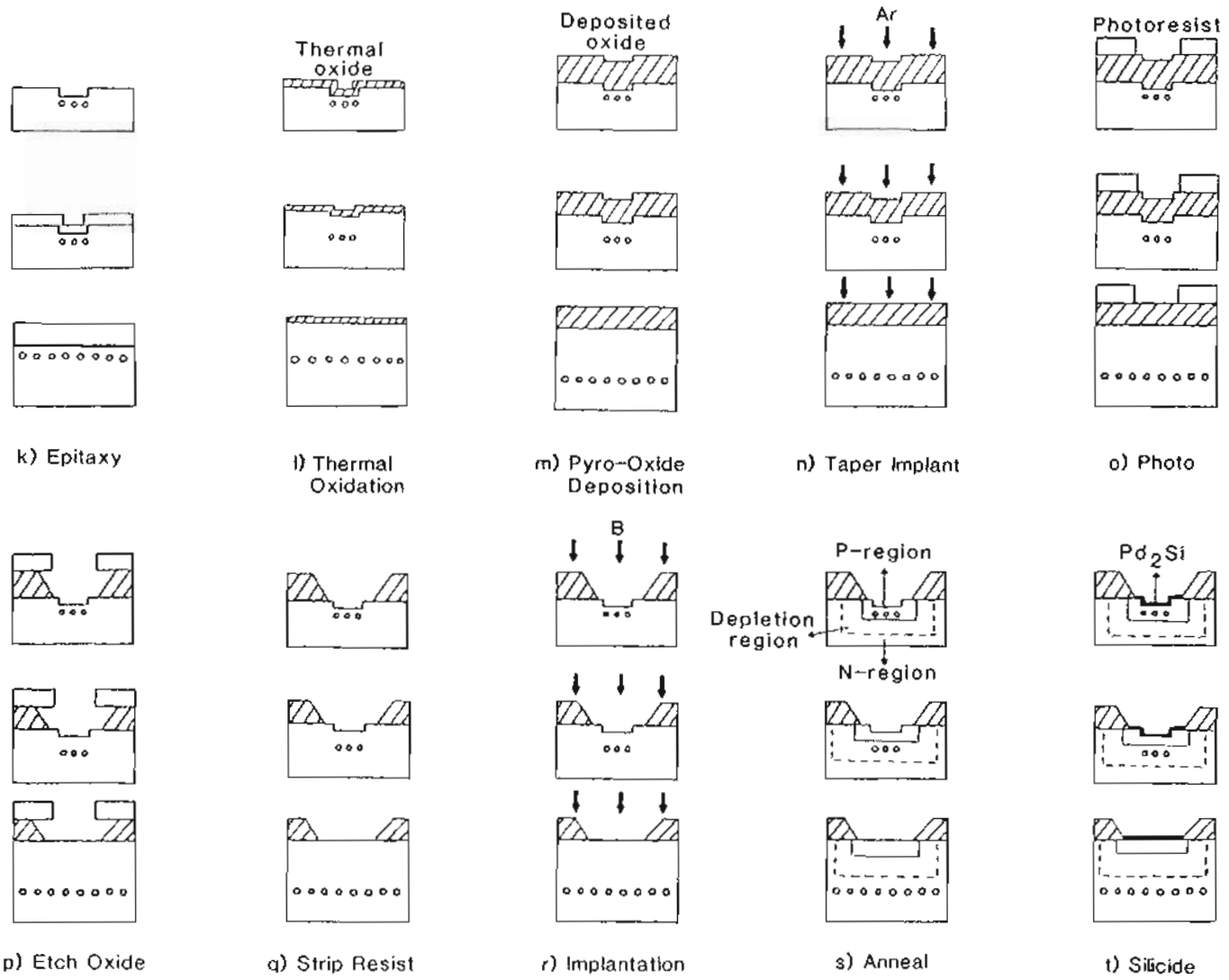


Figure 8. Fabrication process of P-N junction containing dislocation loops


Thermal oxide
Deposited oxide
Ar
Photoresist
k) Epitaxy
l) Thermal Oxidation
m) Pyro-Oxide Deposition
n) Taper Implant
o) Photo
B
P-region
Depletion region
N-region
Pd_2Si
p) Etch Oxide
q) Strip Resist
r) Implantation
s) Anneal
t) Silicide

previous 200 um openings without basins. So these basins provided the reference for a subsequent mask. The implantation was performed using 180 KeV silicon ions with 100 uA beam current and 5E15 doses at liquid freon temperature. Wafers were annealed at 900 C for 1.5 hours with a nitrogen atmosphere to induce dislocation loops. Then all the oxide layers left were entirely etched away. The N-type epitaxial silicon single crystal layers of 0.8 um and 3 um thickness having 2-6 Ω-cm resistivity were grown on the wafer substrate for 3 or 10 minutes at 1080 C to bury dislocation loops in the depletion region or the N-region, respectively. Also, 20 minutes at 1080 C was used for prebaking and cleaning before growing epitaxial layer. These thicknesses were chosen using eqs. (8) and (14). From eq. (8) the contact potential was calculated and the depletion width was calculated to be about 1 um from eq. (14). So 0.8 um epitaxial layer buries dislocation loops in the depletion region and 3 um epitaxial layer buries dislocation loops in the N-region. All wafers were again oxidized at 800 C for 30 minutes in steam to grow a 300 A thick oxide layer which provides better electrical insulation of a surface than the subsequent pyrolytic oxide. Pyrolitic oxide of 9000 A thickness, which is needed as a barrier for the subsequent boron implantation and electrical insulation, was then deposited, followed by a taper implantation of argon ions with 25 KeV energy and 2.5E13 dose. One more photo step with openings of 10 um larger in diameter than the first was introduced. Here the alignment was performed using the previous basins. The oxide layer within these openings was etched away, which automatically shaped the oxide edge to

be wedged due to the taper implantation. Photoresist was then stripped, followed by boron ion implantation with 10-12 uA beam current, 70 KeV energy, and 3E13 dose to form the P-region of the diode. After the wafers were annealed at 800 C for 30 minutes in nitrogen to activate the boron atoms, palladium of 100 A thickness was deposited and annealed to develop palladium silicide(Pd_2Si) which provides ohmic contact to the P-region. The control diodes, which contained no dislocation loops, were fabricated for reference with the same procedures as above except the absence of the silicon implantation step.

III. 2. Fabrication of P-N junctions containing stacking faults

The schematic diagram for fabrication of P-N junction diodes containing stacking faults is shown in Fig. 9. The procedure was identical to the dislocation case up to step (h) except that the silicon implantation conditions were 6E14 or 1E15 dose and 50 KeV energy. At this point the wafers were oxidized at 1100 C in steam for 15 minutes or 2 hours to induce stacking faults that grow into the P-region or extend into the depletion region, respectively. Oxide was then etched away followed by a second oxidation at 800 C for 30 minutes in steam to grow a 300 A thick oxide layer. The last part of procedure from step (l) is identical to the dislocation case procedure from step (m) as shown in Fig. 9.

III. 3. Electrical measurement of diodes

I-V characteristics were measured with HP 4145 Semiconductor Para-

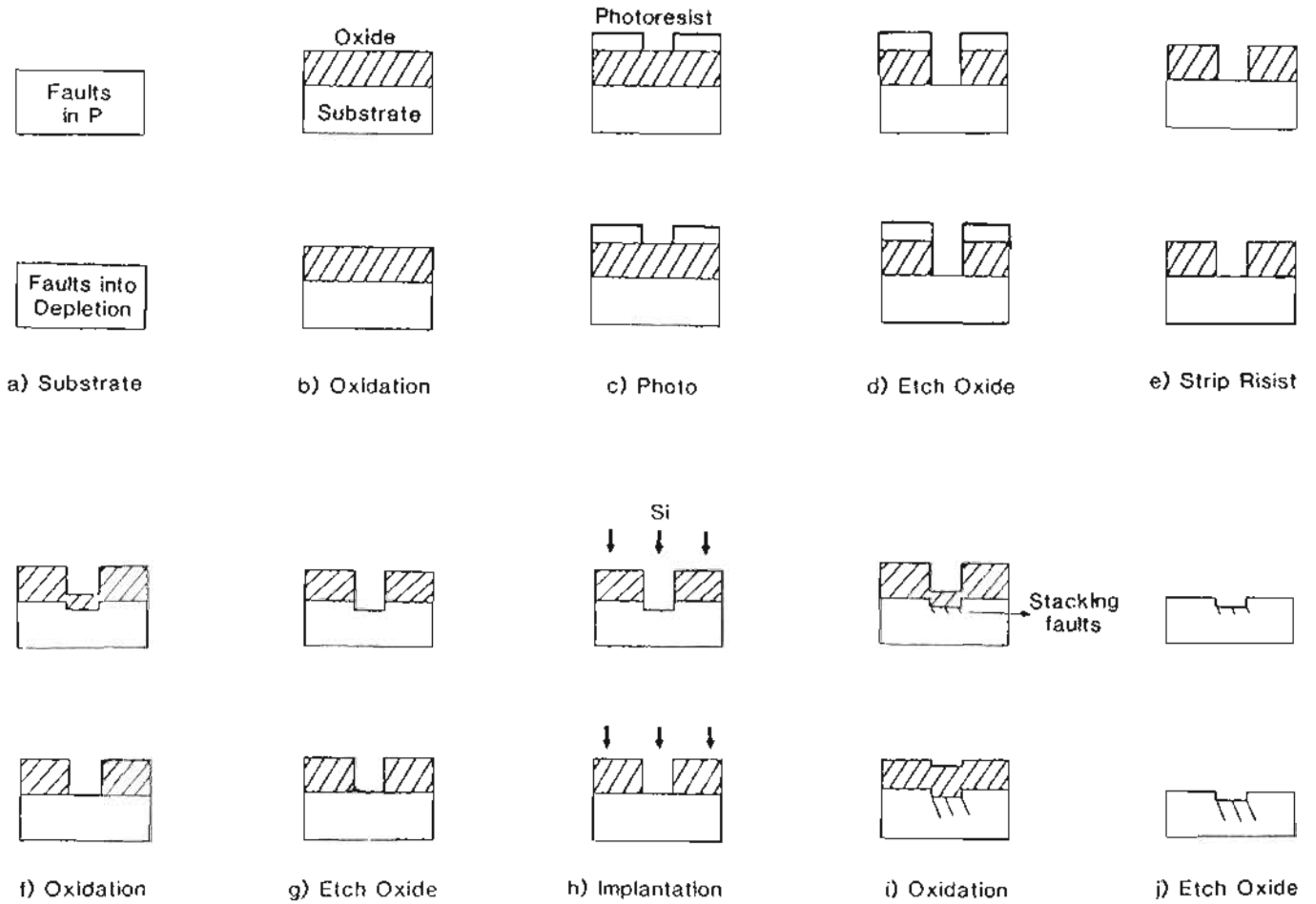
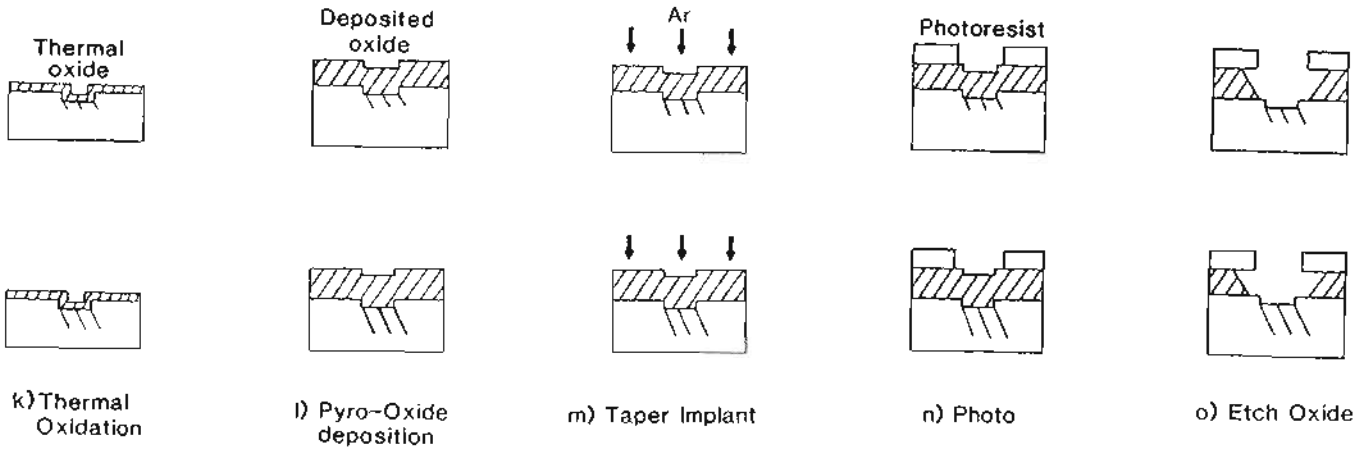


Figure 9. Fabrication process of P-N junction containing stacking faults


Thermal oxide
Deposited oxide
Ar
Photoresist
k) Thermal Oxidation
l) Pyro-Oxide deposition
m) Taper Implant
n) Photo
o) Etch Oxide
B
P-region
Depletion region
N-region
Pd_2Si
p) Strip Resist
q) Implantation
r) Anneal
s) Silicide

meter Analyzer. The forward bias up to 1 volt and the reverse bias down to -100 volts were applied and current was measured from 0.1 pA to 10 mA. The slopes of curves at 0.3 volt were measured to obtain the ideality factor. Measurement was performed in the dark room to prevent the effect of light. In order to observe the temperature effect on the junction behaviour, diodes were heated up from room temperature to 150 C.

III. 4. Electron microscopic observation

A Hitachi H-800 AEM equipped with LaB_6 filament as shown in Fig. 10 was used to observe the configurational structures of diodes and the defects by TEM mode, and to analyze the crystal structures and the chemical compositions of precipitates by STEM mode in assistance with a Tracor/Northern TN 5500 EDS system. The acceleration voltage of 200 KeV and filament current of 15 uA were the observation conditions. In order to obtain lattice imaging a beam size of 3 um diameter and the condenser aperture size of 150 um diameter were selected and the objective aperture was used to confine three beams.

III. 5. TEM specimen preparation

III. 5. 1. Top-view specimen preparation

This technique is described in Dr. Drosd's Ph. D. thesis(5) and the schematic diagram is shown in Fig. 11. The wafers were cut into 3 mm discs. For chemical thinning, the 3 mm discs were placed with the

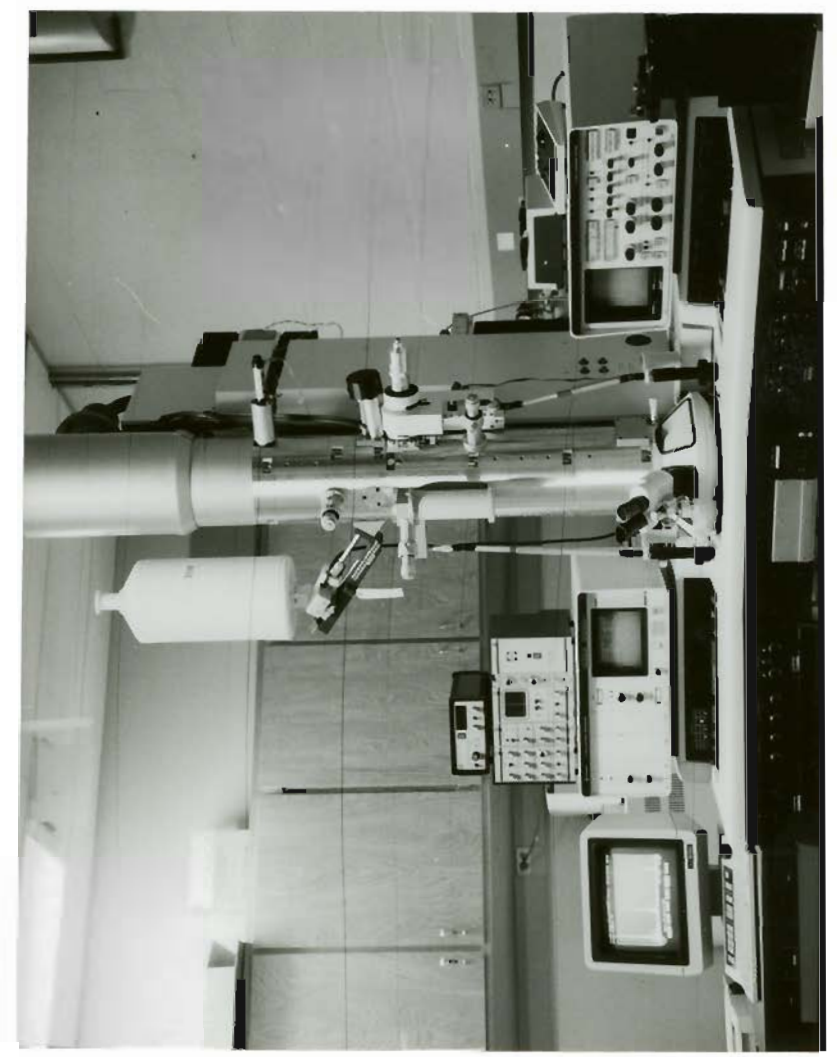


Figure 10. Hitachi H-800 AEM

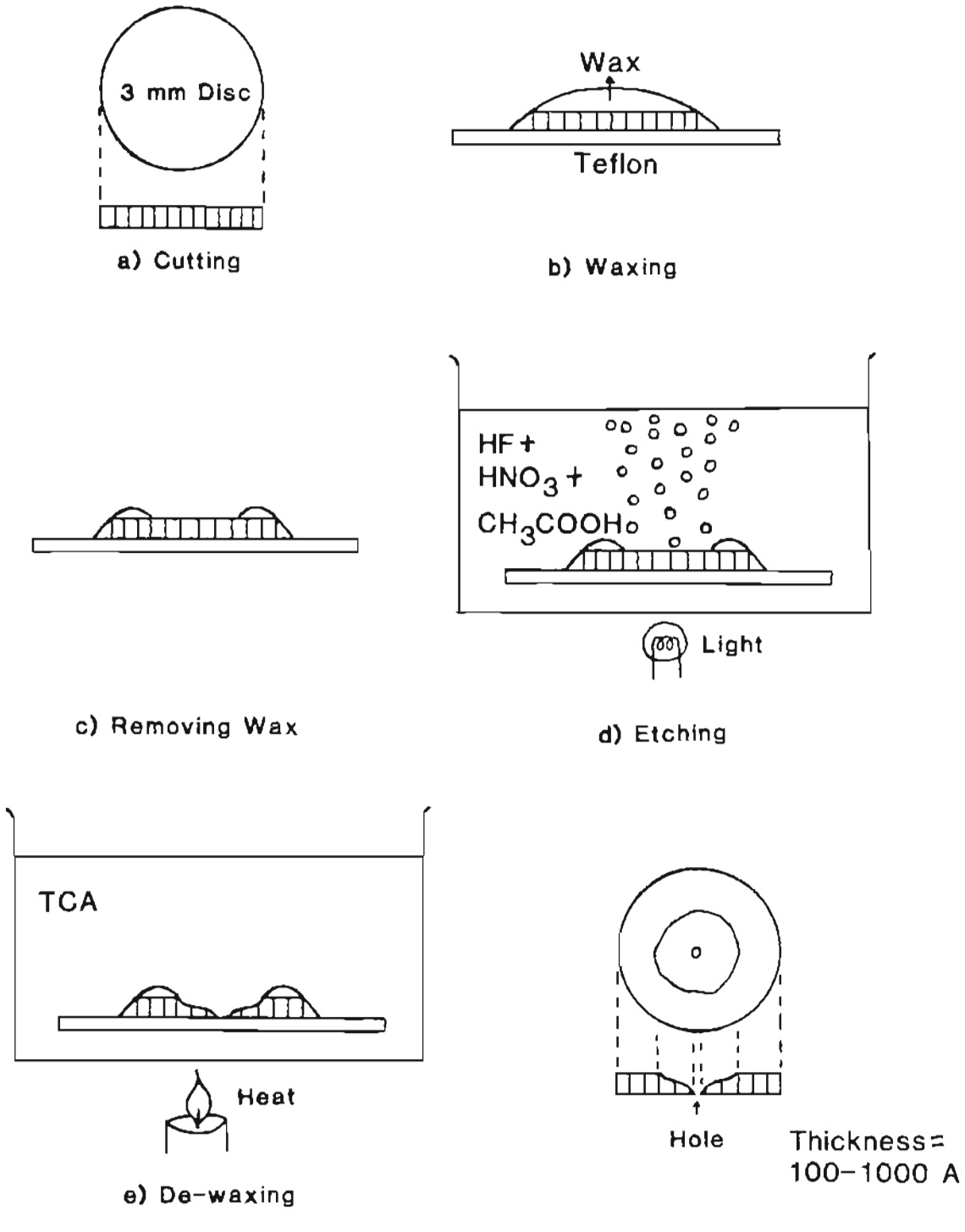


Figure 11. Top-view TEM specimen preparation technique

surface of interest down on a thin piece of teflon sheet and covered with molten wax. Immediately after solidification, the center area was scratched free of wax leaving behind the wafer backside exposed. The teflon sheet was then immersed in a transparent plastic beaker containing an acid of 5 parts HNO_3, 3 parts HF and 3 parts CH_3COOH solution, and a light was placed below the beaker. As the silicon reached a thickness of about 1 um at the center, it transmitted enough red light to be visible thus warning that perforation is imminent. As soon as a small hole, which had about 100 um diameter, appeared the teflon was rapidly placed in water and rinsed. The specimen was then taken out from the teflon using boiling trichloroethane solvent which dissolves the wax.

III. 5. 2. Cross-section specimen preparation

Even though a minor modification has been done for this work as shown in Fig. 12, the basic technique is being commonly accepted by electron microscopists in the electronic industry(62-67). Two wafers were stacked face to face using the commercial epoxy mixture of 16 parts EPOX812 resin, 15 parts NMA and 1 part DMP30 manufactured by Ernest F. Fullam and then baked for 8 hours. Stacks were cut cross-sectionally into 600 um thick square disc using a Isomet low speed saw with 150 um thick high concentration diamond blade manufactured by Buehler. Square discs were again cut to 3 mm round discs. They were bonded on the Gatan grinder using Crystalbond supplied by Aremco Product and ground to about 20 um thickness with 600 mesh Buehler grin-

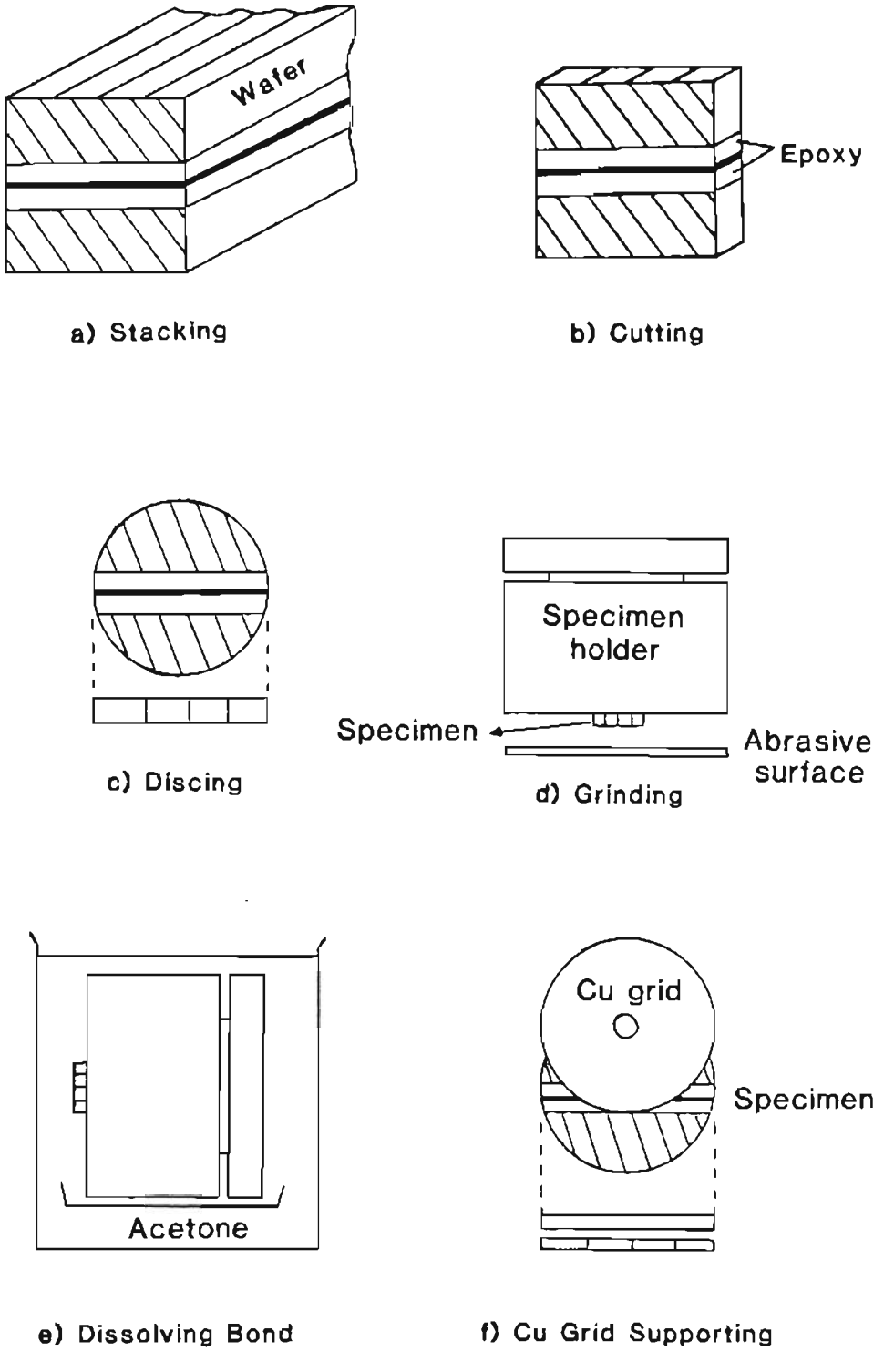


Figure 12. Cross-section TEM specimen preparation technique

ding paper. Crystalbond was dissolved using acetone. At this moment the discs were so fragile that it was almost impossible to pick them up using tweezers and filter paper was, then, inserted below the Gatan grinder before dissolving Crystalbond in acetone. The discs, then, dropped slowly on the paper when the Crystalbond dissolved. The paper was then removed from the acetone and dried in air. A tiny amount of epoxy was smeared on the 3 mm Cu grid which has a 1 mm hole at the center. The Cu grid was picked up using tweezers and laid softly on the disc. The disc with grid was dried for 3 hours and milled using a ion milling machine supplied by VCR Group as shown in Fig. 13.

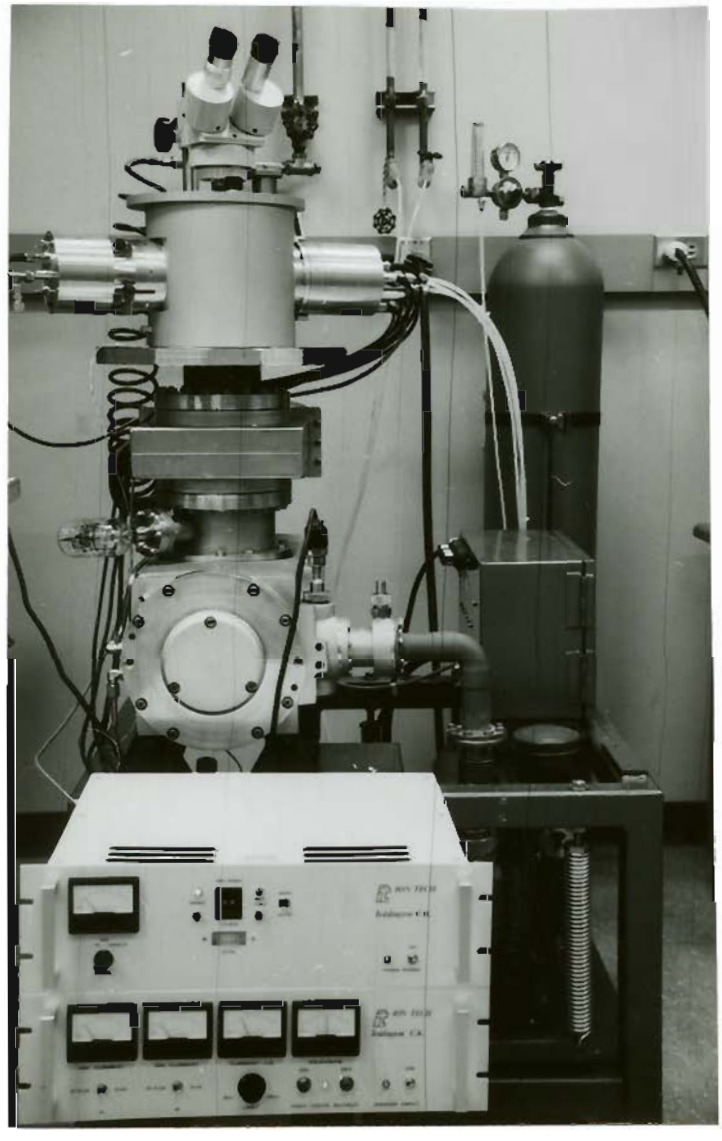


Figure 13. VCR ion milling machine

IV. RESULTS AND DISCUSSIONS

IV. 1. Defect generation

The main objective of this work is to study the electrical effect of crystallographic defects such as stacking faults and dislocation loops on the P-N junction. So defect generation should be controlled by temperature, atmosphere, time and ion implantation energy and dose.

Figs. 14-16 show the as-implanted cross section TEM micrographs of (111) wafers. Fig. 14 and 15 are for 1E15/cm^2 and 5E15/cm^2 dose cases implanted by an implanter equipped with a rotating wafer stage (type A) like a carrousel so that several wafers are implanted in one batch. Fig. 16 is for a 5E15/cm^2 dose case implanted by an implanter equiped with a fixed wafer stage (type B) so that one wafer is implanted in one batch. It is shown that microstructures are varied depending upon the doses and implanters. Initially a type A implanter was used to generate defects. There was no problem in generating stacking faults. However, for the case where dislocation loops were to be buried below an epitaxial layer, high density stacking faults were produced in the epitaxial layer during its growth. They would give some ambiguity to electrical data for the case of dislocation loop effect on the P-N junction. When a Type A implanter was switched to Type B, this problem was eliminated. Since it is out of scope of the work to study this phenomenon, this study did not go further. However, stacking fault generation in the epitaxial layer seems to be due to the as-implanted crystal structure difference.

a)

b)

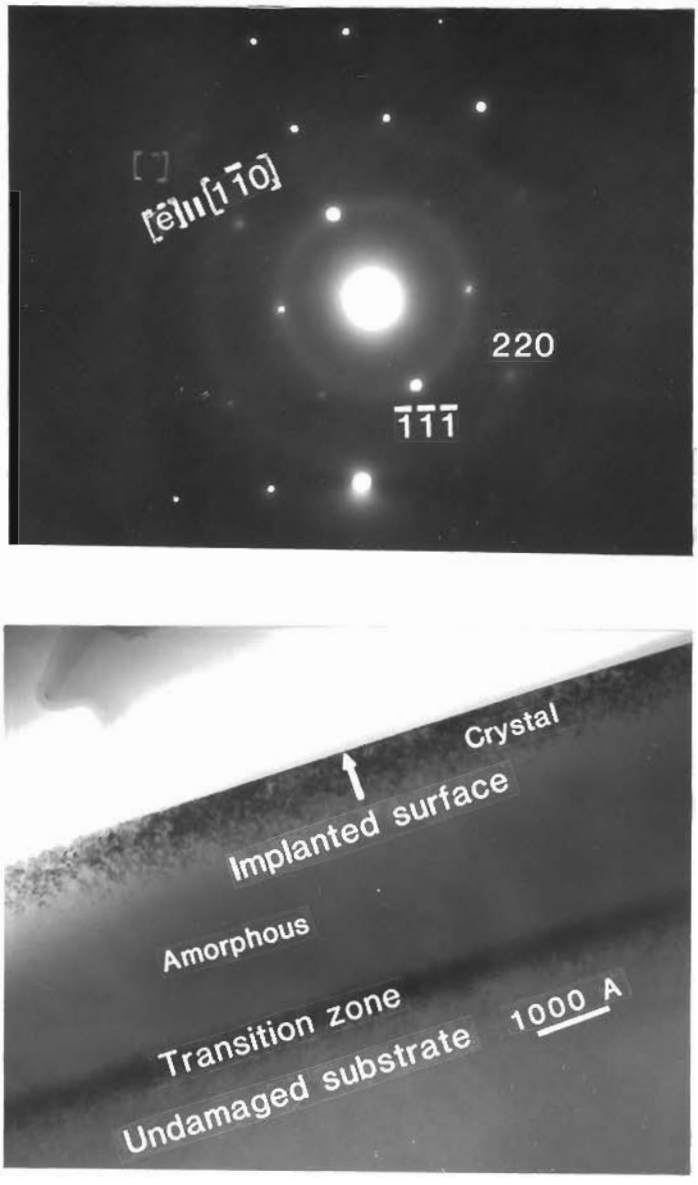


Figure 14. Cross-section TEM micrographs of as-implanted silicon wafer with 1E15 dose using Type A implanter

a) SAD pattern, showing spot and ring patterns overlapped, which indicates the formation of armophous layer.

b) BF image

a)

b)

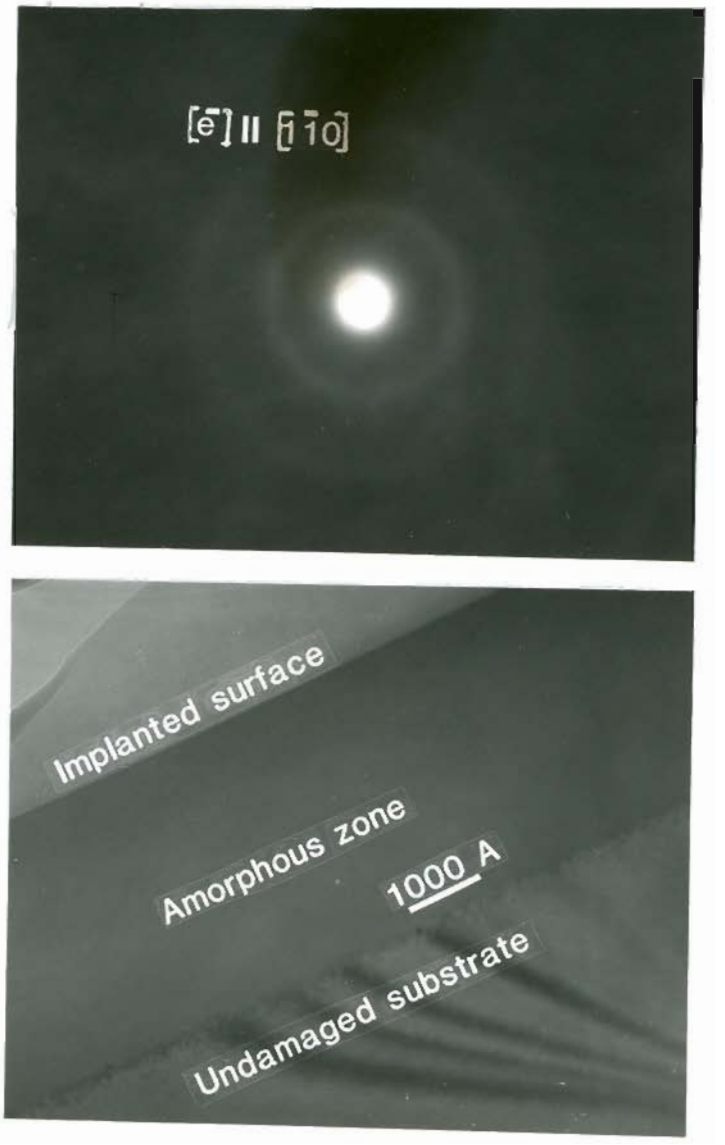


Figure 15. Cross-section TEM micrographs of as-implanted silicon wafer with 5E15 dose using Type A implanter

a) SAD pattern, showing only ring pattern that indicates the formation of complete armophous layer.

b) BF image

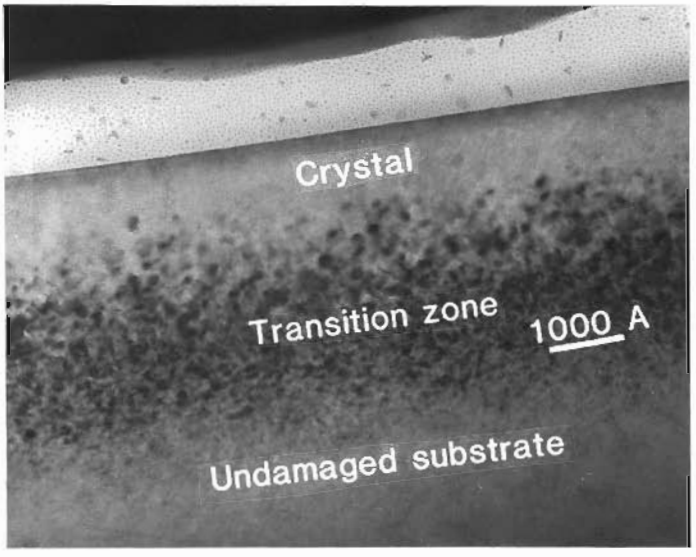


Figure 16. Cross-section TEM micrograph of as-implanted silicon wafer with 5E15 dose using Type B implanter, showing completely crystallized layer.

Fig. 17 shows the stacking fault density variation depending upon the implantation doses. The stacking fault density drops abruptly from 1E7/cm^2 to 1E6/cm^2 for 1E15/cm^2 to 6E14/cm^2 doses, respectively. To observe the electrical dependence on the fault density variation, 6E14/cm^2 and 1E15/cm^2 doses were selected arbitrarily because 1E6/cm^2 is in a range of minimum density in terms of TEM observation.

Oxidation time was controlled to vary the depth of the faults so that they could be located in just the P-region or extended into the depletion region. Fig. 18 shows that the faults grew 0.45 um or 1.0 um deep for a 15 minute or 2 hour oxidation with steam at 1100 C, respectively.

Silicon ions (180 KeV energy) were used to induce dislocation loops. Similarly to fault generation, dislocation loop density drops abruptly from 1E10/cm^2 to an undectectable level as the dose is decreased from 1E15/cm^2 to 1E14/cm^2 as shown in Fig. 19. A 5E15/cm^2 dose was selected to induce dislocation loops.

Based on defects generated by methods mentioned above, P-N junctions were fabricated by boron implantation into N-type wafers. Defect generation due to boron implantation was not desirable, since defects at controlled depths had already been generated by silicon implantation. Hence, boron dose of 3E13/cm^2 and energy of 70 KeV were chosen since they were low enough not to produce defects as shown in Fig. 20. Also, defect locations were controlled with respect to a fixed P-N junction depth. Fig. 21 shows the junction depth variation depending upon the implantation energy after subsequent annealing at 800 C for

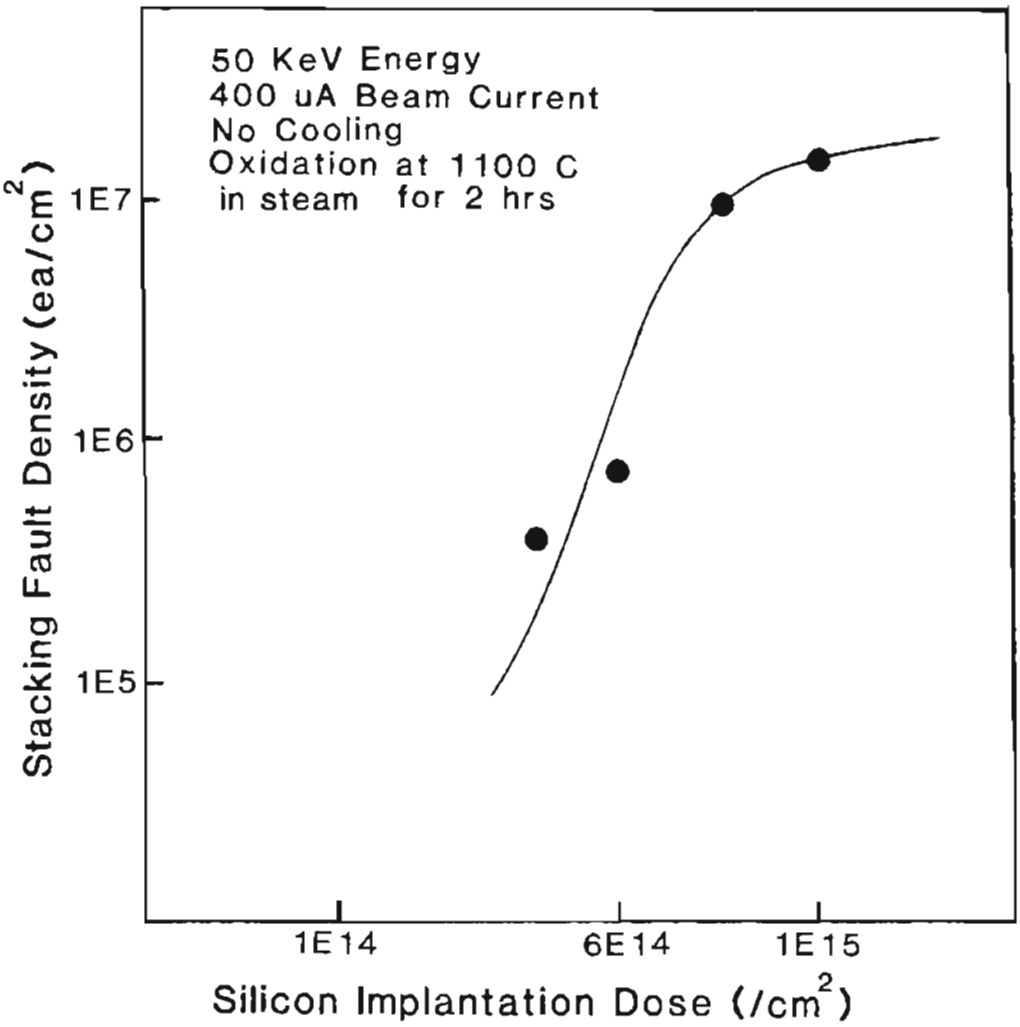


Figure 17. Dependence of stacking fault density on the silicon implantation dose

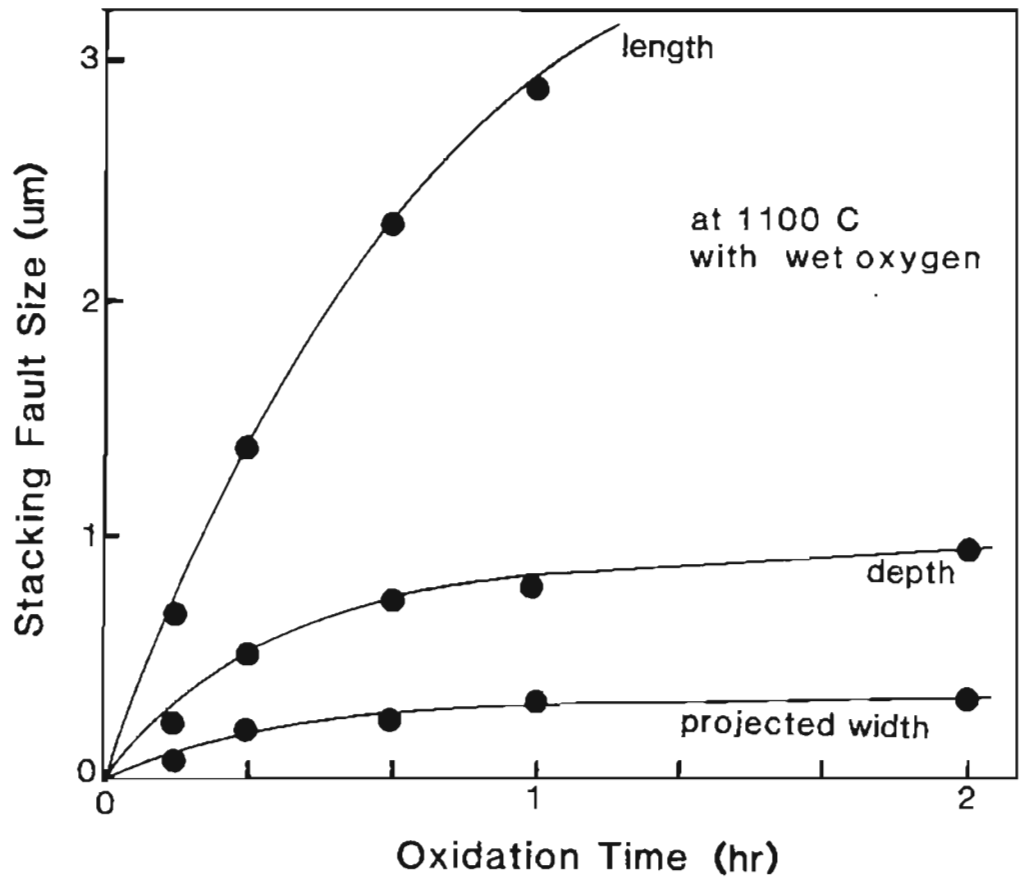


Figure 18. Dependence of stacking fault size on the oxidation time

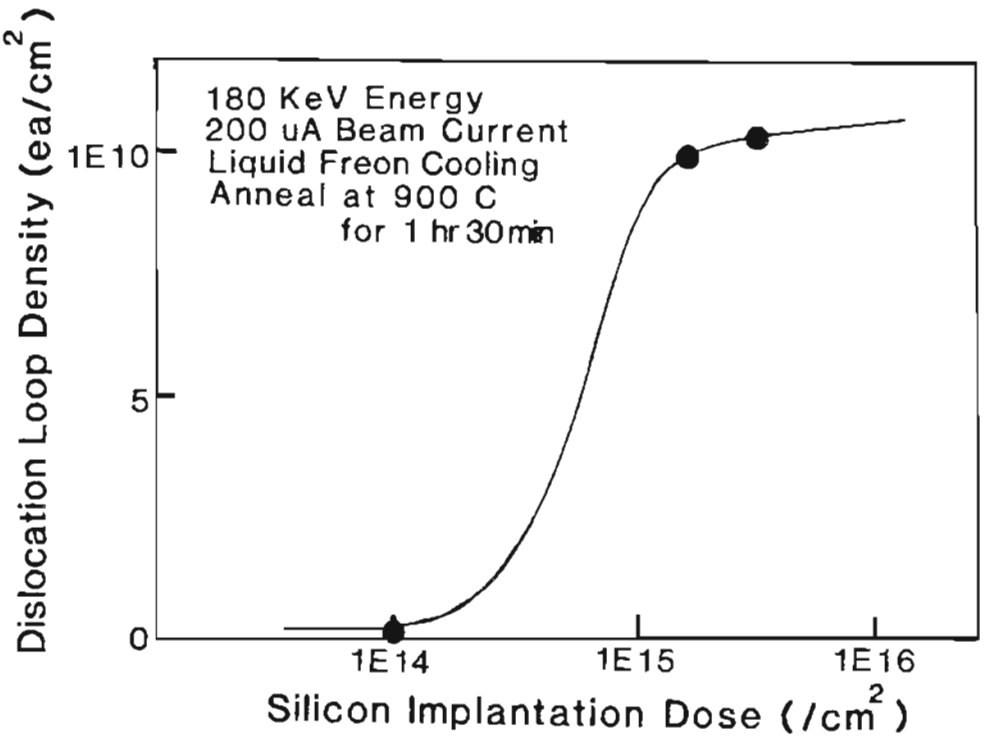


Figure 19. Dependence of dislocation loop density on the silicon implantation dose

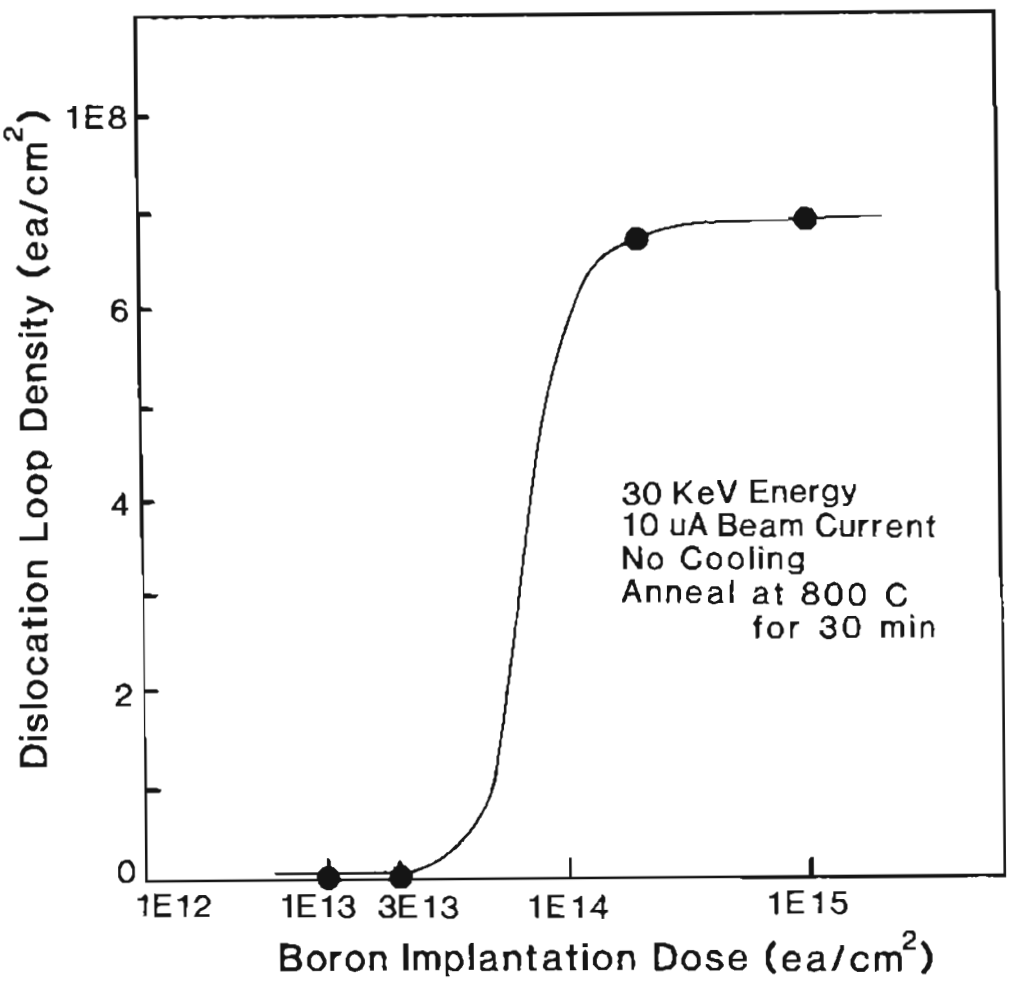


Figure 20. Dependence of dislocation loop density on the boron implantation dose

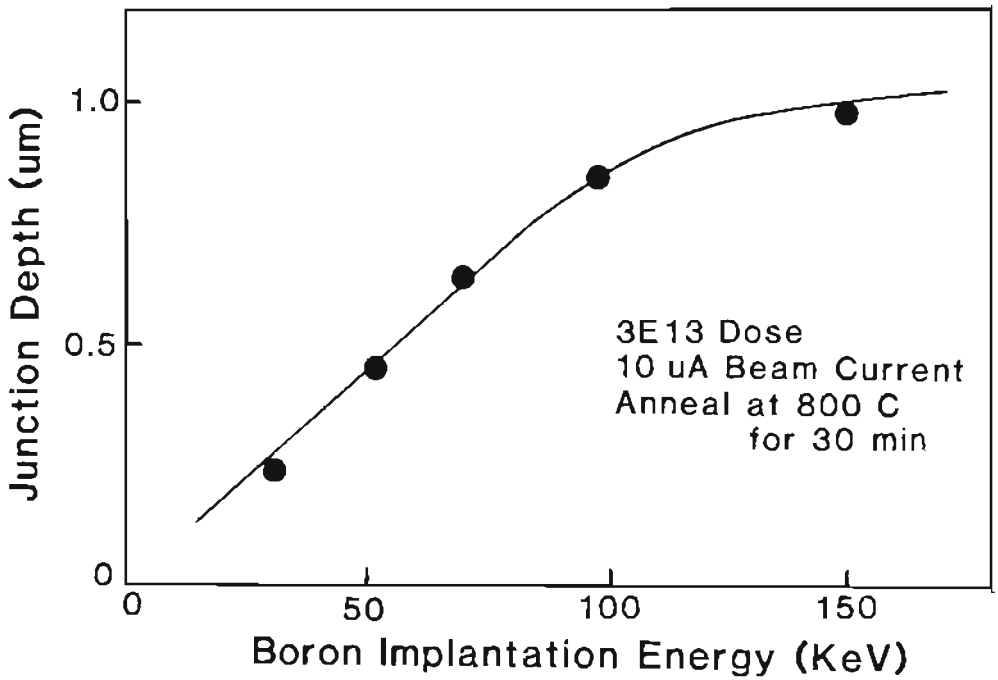


Figure 21. Dependence of P-N junction depth on the boron implantation energy

30 minutes. This annealing condition is a minimum requirement for activating implanted boron atoms without changing junction depth(68).

IV. 2. Characterization of precipitates decorating stacking faults

During generating stacking faults to locate them in the P-N junction, "dog-bone" shaped stacking faults, as observed in the optical microscope, sometimes were found to be generated by thermal oxidation of implantation-damaged surfaces of silicon single crystals,as shown in Fig. 22. They were investigated by AEM to study the structural difference between normal and dog-bone stacking faults and to differentiate their effects on the P-N junction. However, the frequency at which they appeared was so low that they were not found in the diodes. Hence it was not possible to differentiate their effect but the crystallographic structure was characterized here.

Such dog-bone stacking faults have been previously reported[69-70], but with little mention of their crystallographic structure. Even low magnification (10K) TEM observations of these Dog-bone stacking faults indicate that the stacking faults are decorated by precipitates along their edges,as shown in Fig. 23.

Higher magnification (200K) of one precipitate in Fig. 23,(a) with g=[220] showed that it was composed of two distinct types of precipitates, colonies of small discs and a single larger "plate" as shown in Fig. 24 and 25. The precipitate colonies spread about 2,000 A across and located on the edges of the oxidation induced extrinsic stacking faults. By tilting the (111) fault plane edge-on to the [211] orien-

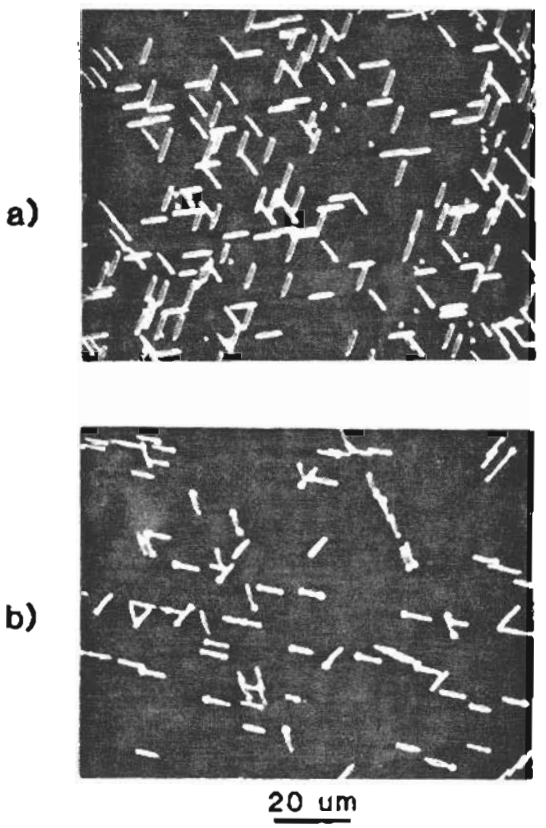
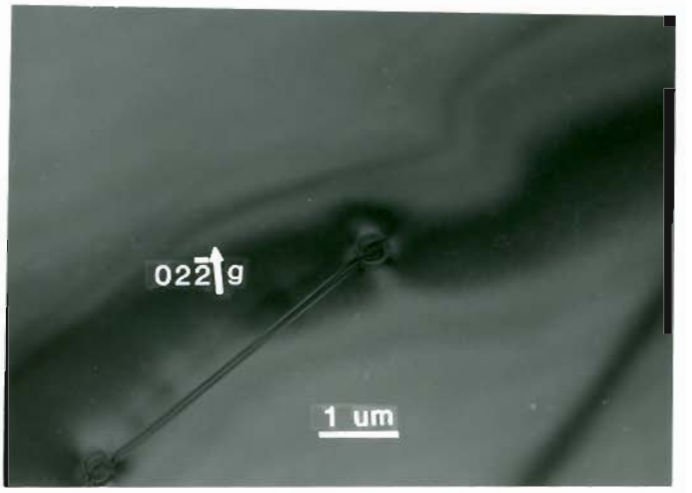


Figure 22. Optical micrograph of "Dog-bone" stacking faults

a) normal SF b) Dog-bone SF

a)



b)

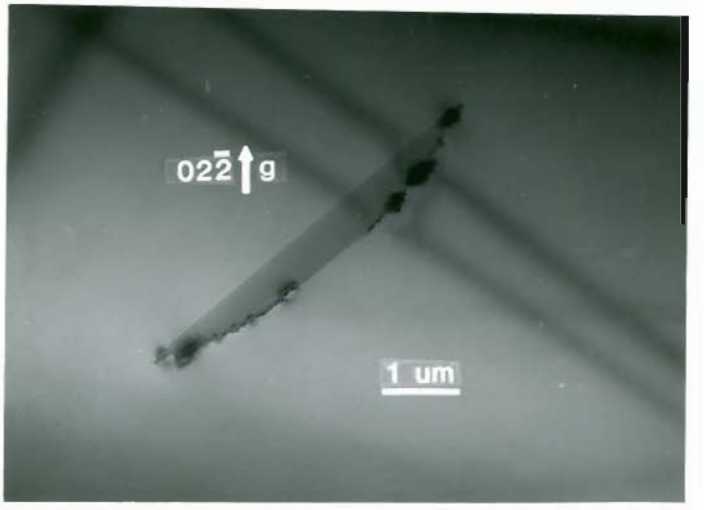
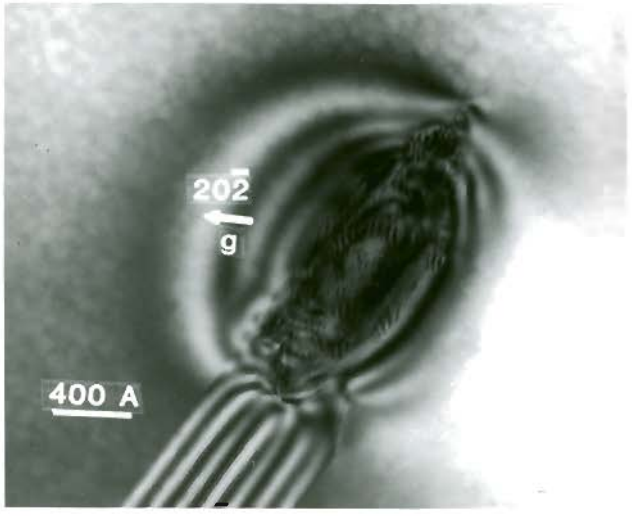


Figure 23. Low magnification TEM micrograph of Dog-bone stacking fault from {111} orientation

a) thinner area b) thicker area

a)



b)

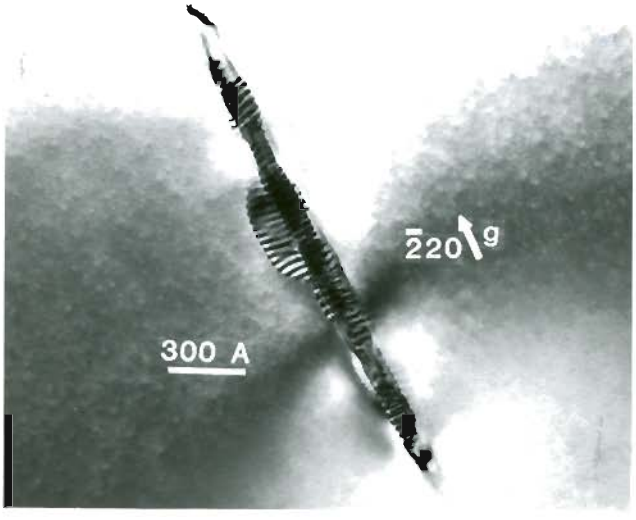


Figure 24. High magnification TEM micrograph of precipitate colonies on the stacking fault

a) observed from [111] orientation

b) observed from [112] orientation

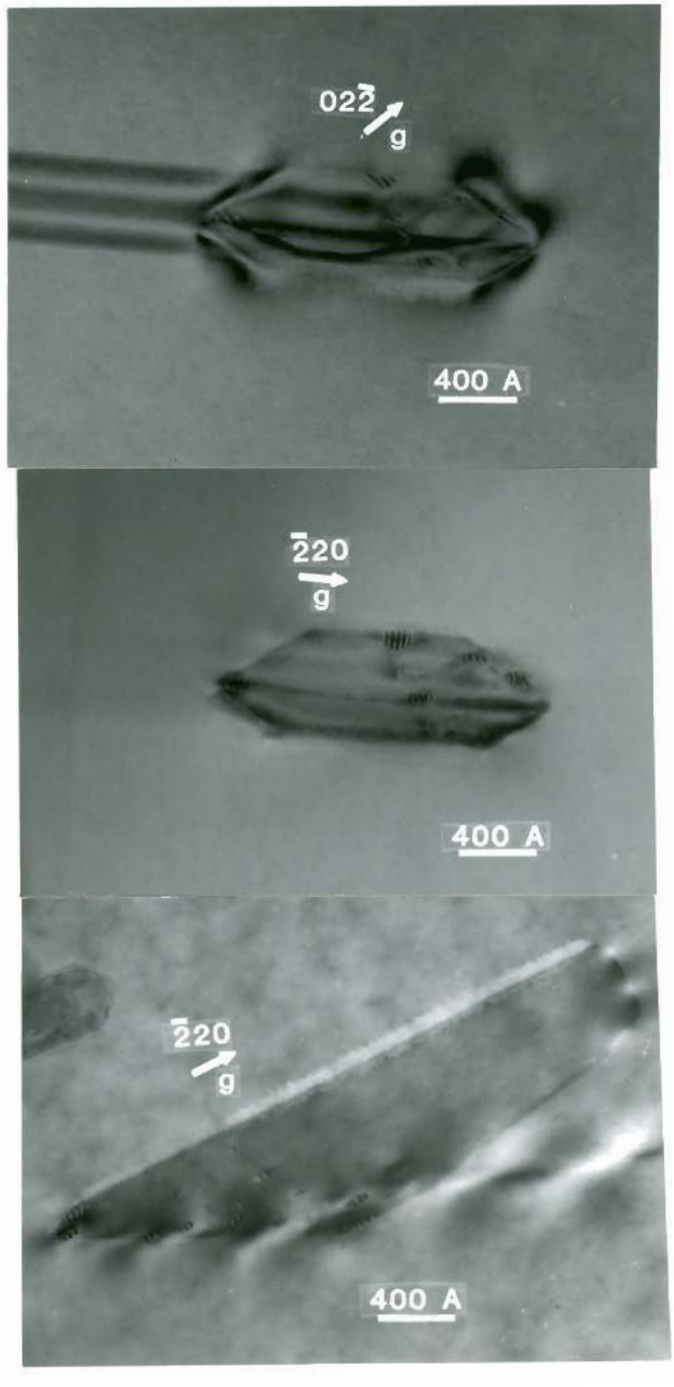


Figure 25. Variation of colony density from [111] orientation

a) g = [02$\bar{2}$]

b) g = [$\bar{2}$20], hexagonal shape of large disc observed

c) g = [$\bar{2}$20], from different wafer

tation the colony was also found to be edge-on with a thickness of about 100 A as shown in Fig.24, (b). Hence the colony is distributed over the fault plane adjacent to the bounding Frank dislocation. The individual precipitates within the colony were roughly disc shaped with their faces also on the fault plane. The discs were about 100 to 300 A across with a thickness of about 100 A. A typical colony contains tens of precipitates, but there was much variation from wafer to wafer as shown in Fig. 25. Here the two types of precipitates overlapped each other. The large plate generally had a hexagonal shape and did not exhibit Moire fringes. Also, it can be clearly shown from Fig. 24,(b) that Moire fringes were produced not by reaction between large disc and colonies but by reaction between silicon matrix and colonies.

First, let us discuss colony type precipitates. Due to the small volume fraction of the precipitates no extra spots in the selected area diffraction patterns were observed. To our surprise, micro-diffraction patterns yielded no clearly visible extra spots either. The presence of Moire fringes in the image indicates that a separate precipitate diffraction pattern does exist but lies very near to the matrix silicon spots. Hence, the analysis of the precipitate crystal structure was carried out by tilting the specimen to several low index orientations following the Kikuchi map as shown in Fig. 26 and by subsequent analysis of the presence or absence of Moire fringes, when a variety of g-vectors were excited. At the Si [111] pole it was observed that all the surrounding [220] type g-vectors gave purely transla-

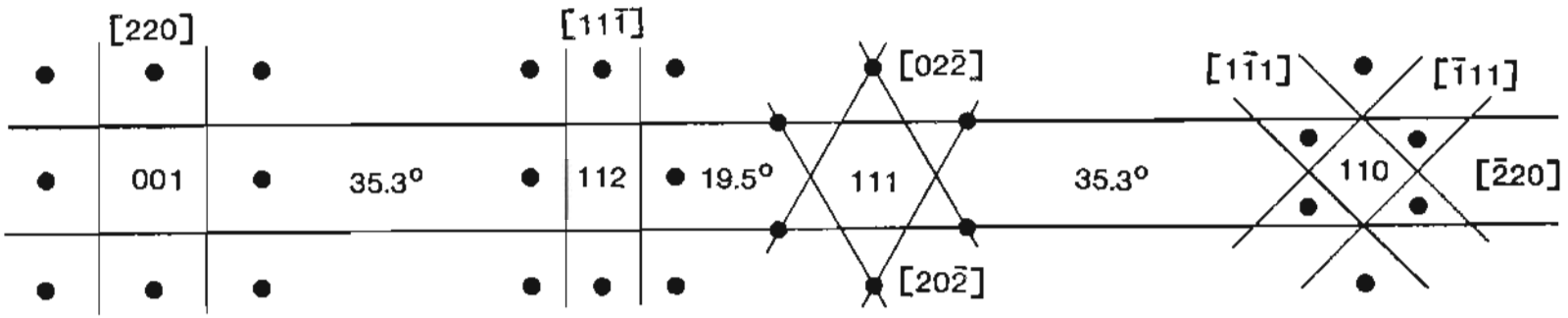


Figure 26. Kikuchi map of diamond cubic structure of silicon

tional (perpendicular to the g-vector) Moire fringes with a spacing of 40 A, as shown in Fig. 27. This result might imply a precipitate structure that is either perfectly aligned cubic, or hexagonal with the c-axis parallel to the Si [111] direction. To resolve this situation [100] silicon specimens were investigated, the result of which is shown in Fig. 28. At this pole the translational Moire fringes were formed for any of the surrounding $[\bar{2}20]$ and [040] g-vectors, with a spacing of 40 A and 25 A, respectively. Thus, at both the [100] and [111] silicon poles the silicon and precipitate diffraction patterns are nearly identical. This situation can only occur if the precipitate has a cubic structure. Upon tilting the specimen to the [110] orientation it was found that $[1\bar{1}1]$ g-vectors also produced Moire fringes with a spacing of approximately 30 A, although they were very faint, as shown in Fig. 29. This value is about half that expected, based on the fringe spacing obtained from the [220] g-vectors, but this can be explained due to double diffraction. No Moire fringes were observed for any other g-vectors at least up to [331], as shown in Table 2. It should be mentioned that the accuracy with which these fringe spacings can be measured is not very good (+/- 20 %) since each precipitate contains only 4 or 5 fringes at best. Based on the spacing of the strongest Moire fringes due to [220] g-vectors, the precipitate lattice parameter is about (5+1) % different from that of silicon.

When the objective aperture was placed in several likely locations in the silicon diffraction patterns where "extra" precipitate spots might appear alone, such as [200] or [110], no strong dark field image

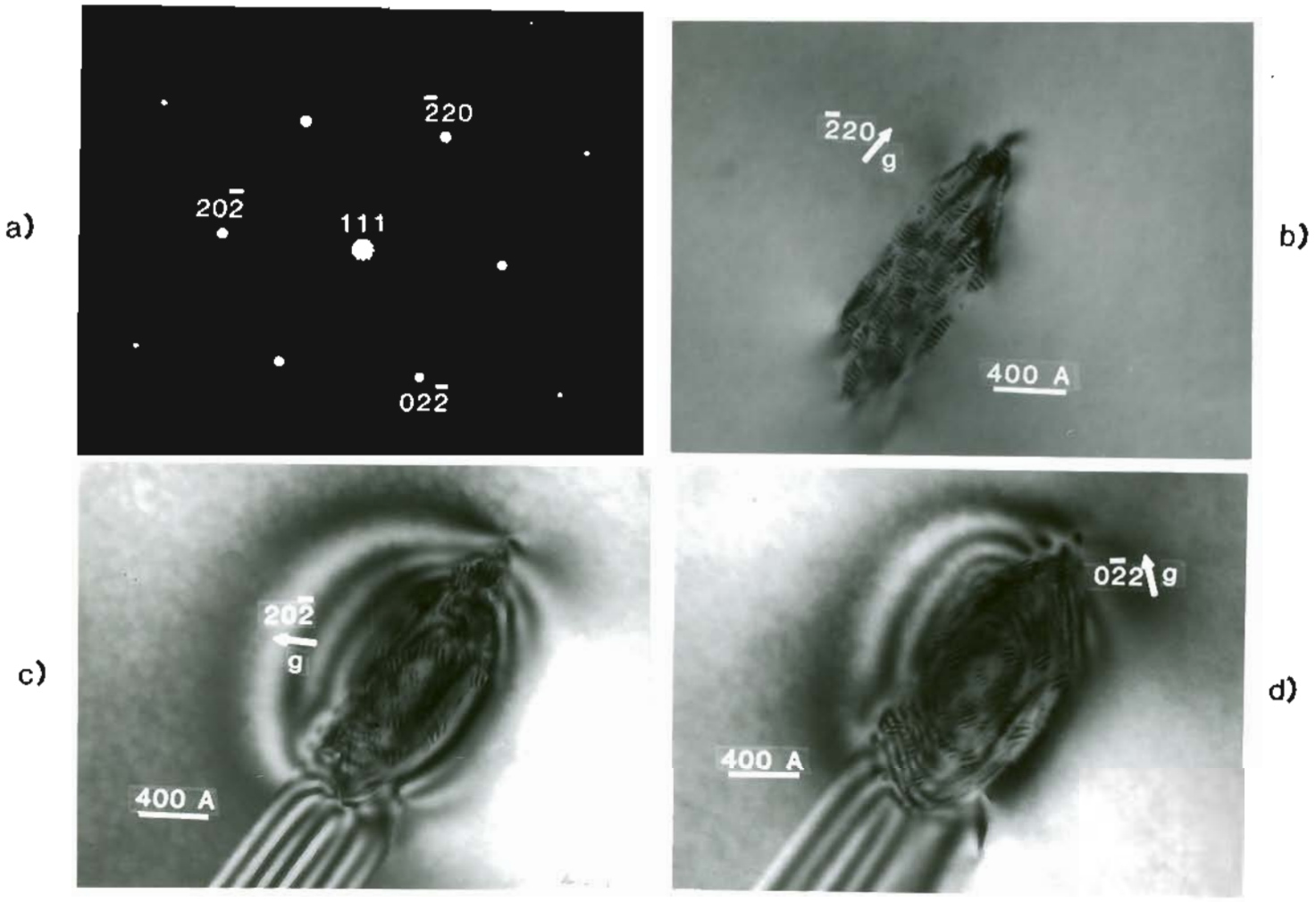
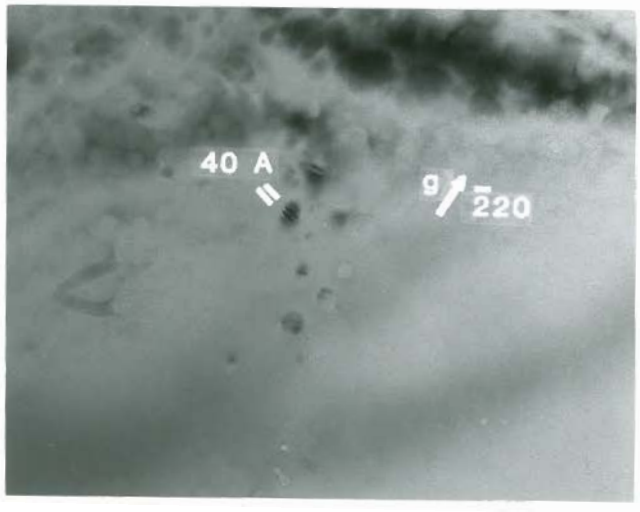


Figure 27. Translational Moire fringes for colonies observed from [111] orientation

a) SAD pattern b) g=[$\bar{2}20$] c) g=[$20\bar{2}$] d) g=[$0\bar{2}2$]

a)



b)

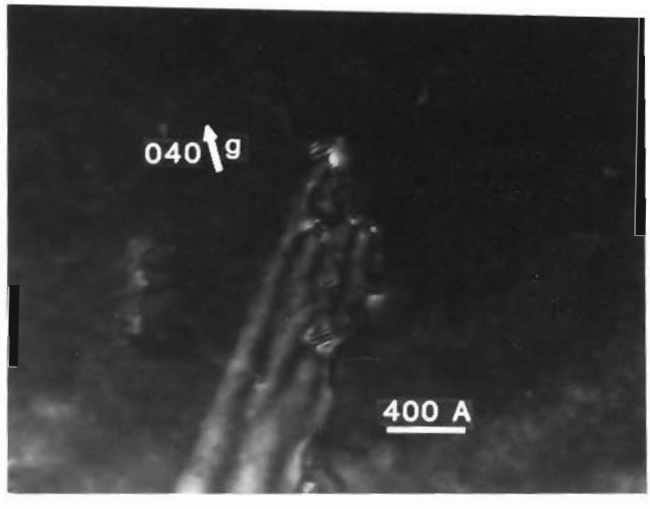


Figure 28. Colonies observed from [001] orientation

a) g=[$\bar{2}$20] b) g=[040]

a)

b)

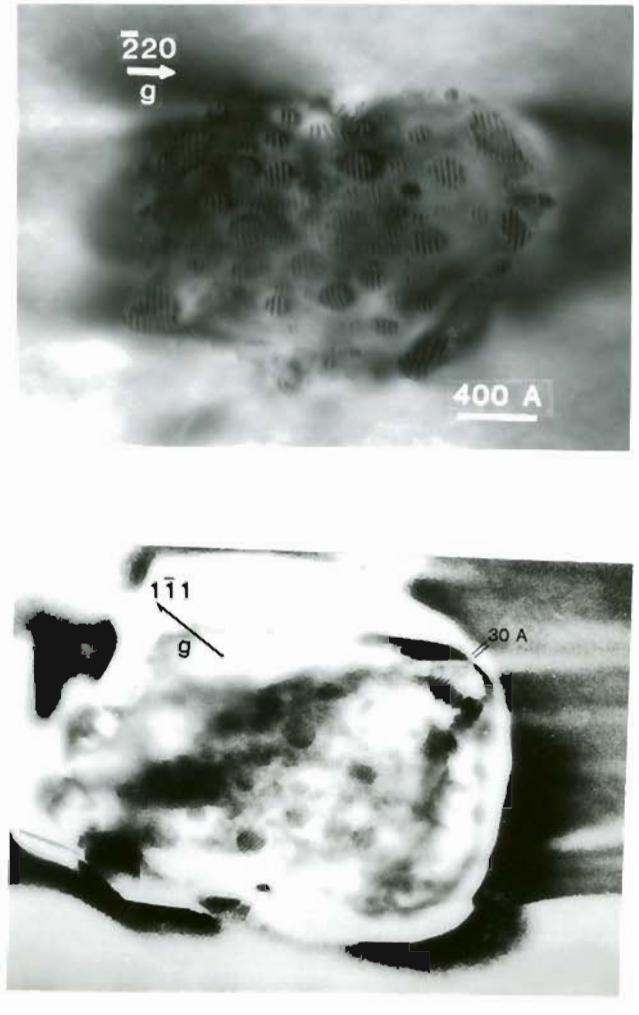


Figure 29. Colonies observed from [110] orientation

a) g=[$\bar{2}$20] b) g=[1$\bar{1}$1]

PLANE	F_{hkl}	I/I_{220} (%)	OBSERVED MOIRE FRINGES
(111)	$4f_{Ni} = 4.1$	38	medium
(200)	$4(f_{Ni} - 2f_{Si}) = 2.0$	9	—
(220)	$4(f_{Ni} + 2f_{Si}) = 6.6$	100	strong
(311)	$4f_{Ni} = 2.5$	14	—
(222)	$4(f_{Ni} - 2f_{Si}) = 0.5$	1	—
(400)	$4(f_{Ni} + 2f_{Si}) = 4.2$	40	medium
(331)	$4f_{Ni} = 1.9$	8	—

Table 2. Calculated and observed intensity ratio of precipitate diffraction beams

of the precipitates was formed. Thus no other spots in addition to those normally allowed for in diamond cubic exist for the precipitate.

To determine the sense of the lattice mismatch, lattice images of the (111) planes at the [211] orientation were taken, using the 3-beam technique[54]. A slight increase of the precipitate planar spacing compared to the silicon was measured. In addition a single edge dislocation was found at the Si/precipitate interface with the extra half plane lying in the matrix, as shown in Fig. 30, confirming that the precipitate has a larger lattice parameter.

X-ray analysis of precipitates in Fig. 24 indicates that both Cu and Ni are present in significant quantities in the precipitates, as shown in Fig. 31. Here the Mo peak comes from the Mo grid which is supporting the Si substrate. The above observations indicate that the precipitates are cubic with $a_o = 1.05 * a_{Si} = 5.70$ A. Due to the presence of Moire fringes it is known that the precipitate structure factor definitely allows diffraction on the {111}, {220}, and {040} planes, with {220} being the strongest. All other g-vectors appear to be forbidden or too weak to be observed. A likely candidate for the precipitate structure might be that of a (Cu,Ni) silicide. Some forms of both Cu[20,71-72] and Ni[73] silicide precipitates have been reported in silicon but their morphology and structure are quite different from what we have observed. Precipitates reported by Lin et al[74] appear very similar, but the structural characterization was not performed. The high temperature $NiSi_2$ silicide has not been previously reported as a precipitate in bulk silicon but rather as a thin film

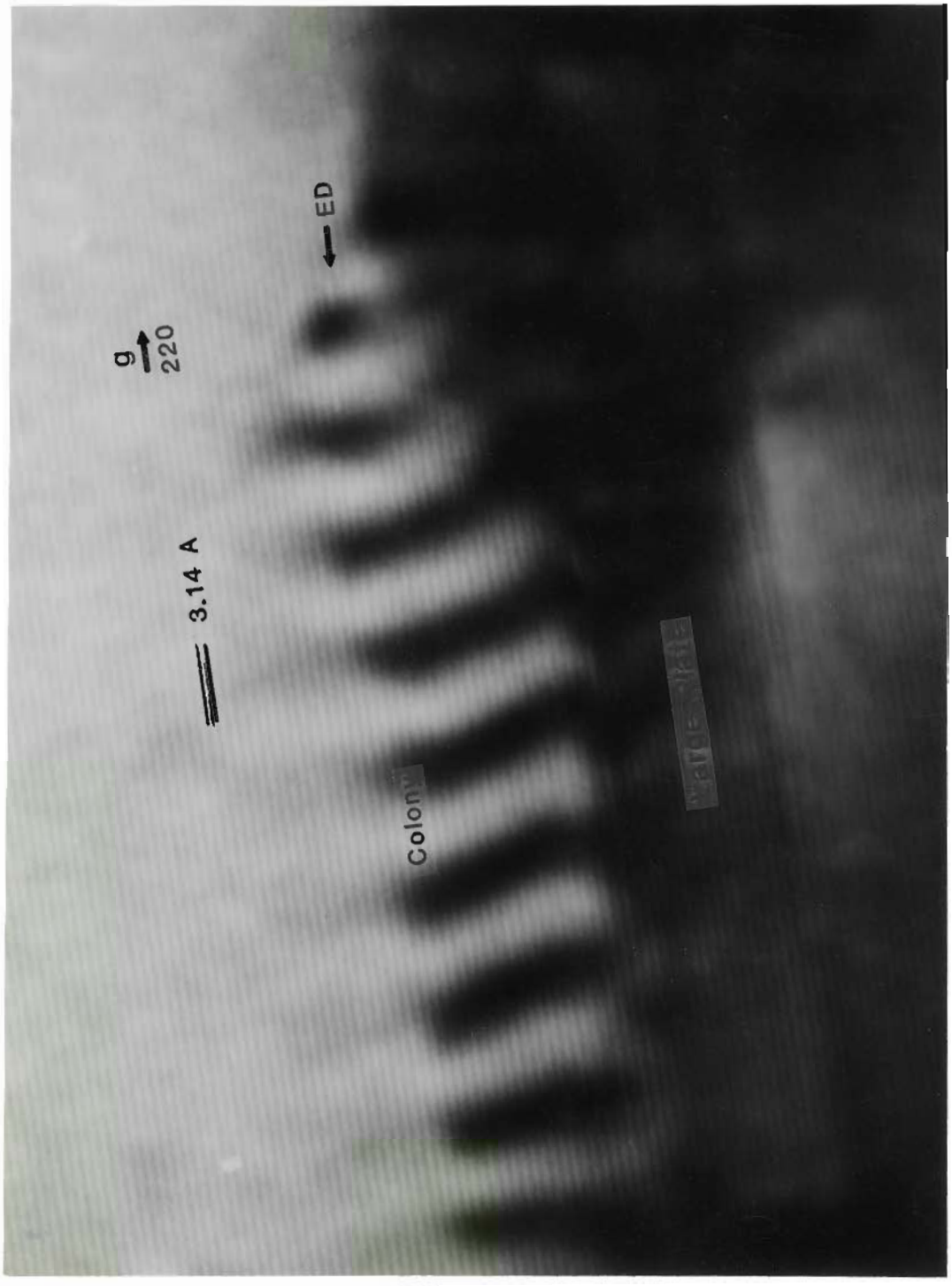
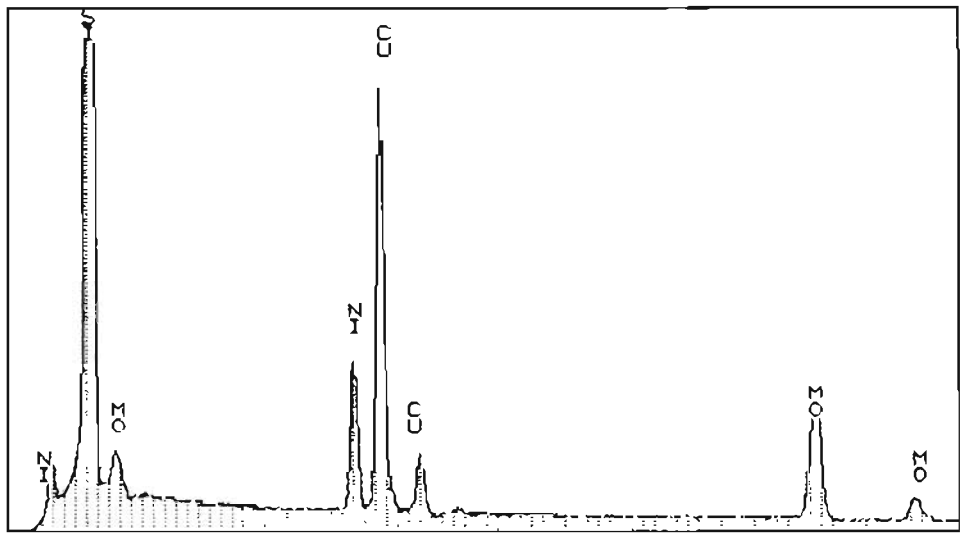


Figure 30. Lattice imaging for precipitates from area A of Fig. 24, b)



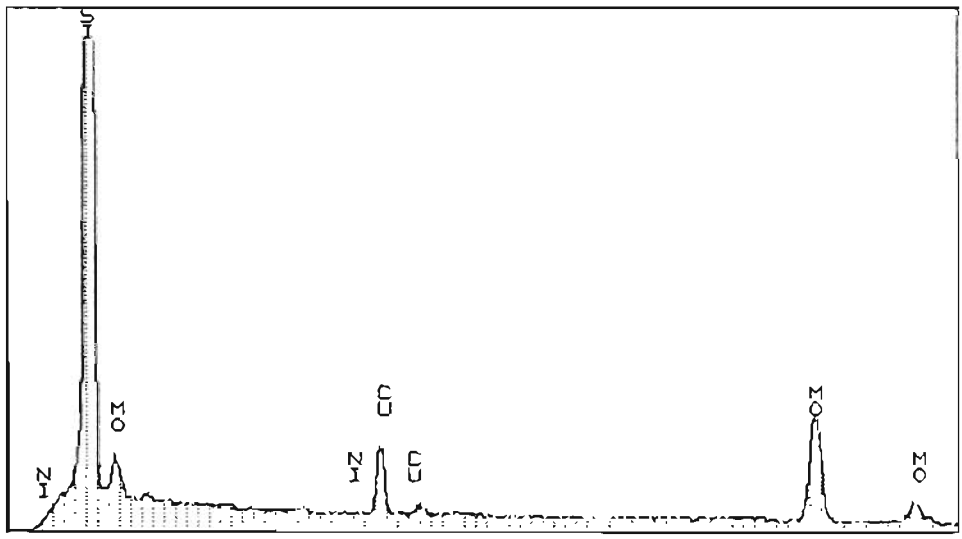


Figure 31. EDS data for colonies

a) from colonies b) from silicon matrix

(14,75-77). In addition $NiSi_2$ has the CaF_2 structure(78-79) whose structure factor closely matches our estimate of the allowed diffraction planes, as shown in Table 2. However, the lattice parameter of $NiSi_2$ is 5.406 A. Possibly the presence of Cu can account for this discrepency since the lattice parameter of pure Cu is slightly larger than that for Ni. Since Cu and Ni are very soluble in one another it seems reasonable to assume that the CaF_2 structure of $NiSi_2$ is preserved but slightly expanded by the substitution of some Cu atoms for Ni.

Secondly, let us consider the large plate type precipitate of 50 A thickness which is confirmed by tilting to the [211] orientation where it is edge-on. There exist two possible reasons for the absence of Moire fringes. The first is that the difference of plane spacings between a silicon matrix and this precipitate for g=[220] is very small, i.e., 0.1 %, so that the anticipated Moire fringe spacing is about 2000 A. Since this is larger than the plate itself, no fringes will be observed. Also, the extreme thinness of the plate is believed to reduce the intensity of Moire fringes. A possible example of a closely matched silicide is pure $NiSi_2$. The second case is that the difference of plane spaces between silicon and the precipitate for g=[220] is greater than 30 %, thus, resulting in Moire fringe spacing of less than 3 A, which cannot be easily resolved. A possible candidate for this is the Ni_3Si precipitate which has a $AuCu_3$ structure and lattice parameter of 3.50 A. Precipitate planes parallel to (111) silicon planes also match closely in spacing as shown in Fig. 30. Therefore,

if it has a cubic structure the lattice parameter will be very close to silicon. If it has a hexagonal structure, then only (0001) planes would match to (111) silicon planes and the other plane spaces of precipitate would generally have large differences from those of silicon.

However, returning back to Fig. 24,b), it is clear that Moire fringes were produced inside the plate with [220] g-vector and that Moire fringes are the result of reaction between diffracted electrons from colonies and those from plate(not from silicon matrix), since the specimen thickness at this area is less than thousand angstrom which is about the same as a plate diameter and so it can be said that there is no silicon matrix materials left within the plate area during specimen preparation. Also the Moire fringe spacing inside the plate is almost the same as outside. Hence it is concluded that plate also has a cubic structure.

In the STEM mode the beam size is a few tens of angstrom. To obtain EDS data from plate precipitates this small beam was placed on the very midplane position of the plate precipitate as shown in Fig. 25 where no colony precipitates exist. EDX data for this precipitate in Fig. 32 also shows Cu and Ni. However, the Ni concentration increases appreciably, compared to that of colony precipitate in Fig. 31. Hence it is concluded that both have the same (CaF_2) structure but differ in chemical composition.

The source of the Ni and Cu contamination are of practical importance to the electronics industry. Wafers from different vendors like Monsanto and Wacker were processed through different locations like

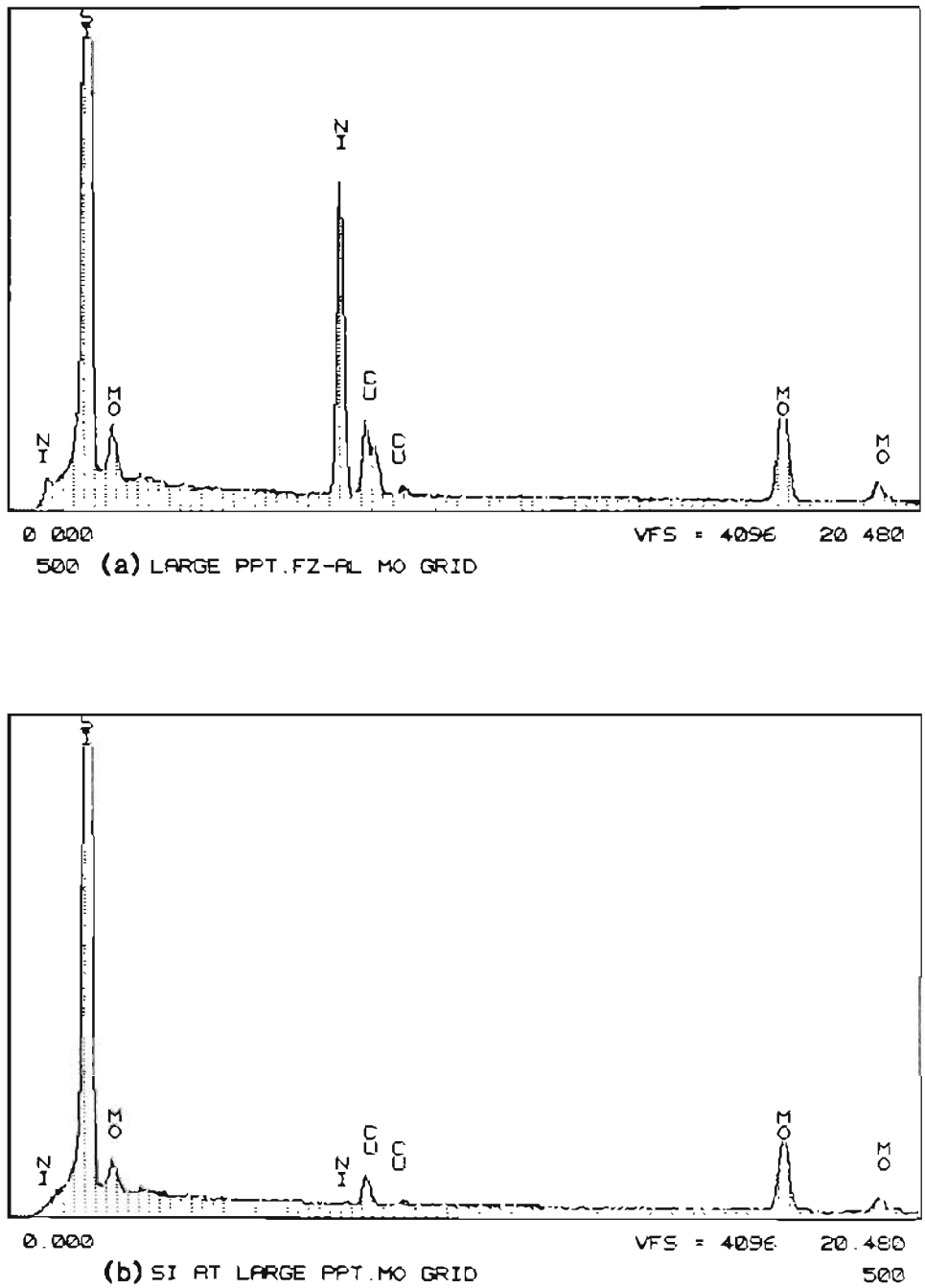


Figure 32. EDS data for large precipitate

a) from large disc b) from silicon matrix

Wacker and Tektronix, and no difference on the precipitate structure was obtained. Even changing oxidation conditions and furnaces did not make any significant difference. This leads us to believe that the basic poly-silicon starting material may be the source. "Pure" silicon wafers normally contain metallic impurities to the level of about 1 part per billion. In addition, Cu and Ni have extremely high diffusion coefficients(D = 1E-5 cm/sec) at 1,100 C [69]. They can be expected to diffuse millimeters in an hour. Hence, these metals can travel through the entire thickness of the wafer to precipitate on the wafer surface during oxidation. Given this condition 1 ppb Cu and Ni is more than sufficient to produce the precipitate density observed ($1E6/cm^2$).

IV. 3. Electrical performance of P-N junctions containing stacking faults

Fig. 33 and Fig. 34 show the TEM cross-sections of diodes containing faults in the P-region and the depletion region, respectively. A step in the silicon surface is seen at about 5 um distance from the SiO_2 at the diode edge. This is where faults start to occur and is due to that the diode delineation oxidation as is discussed in section III. 1. Hence faults were always prevented from being at the edge of the diode where they would cut through the P-N junction no matter how shallow they might be. A 200 A thick Pd_2Si silicide layer is seen at the top surface of the diode.

Forward and reverse bias conditions of ideal and fault containing

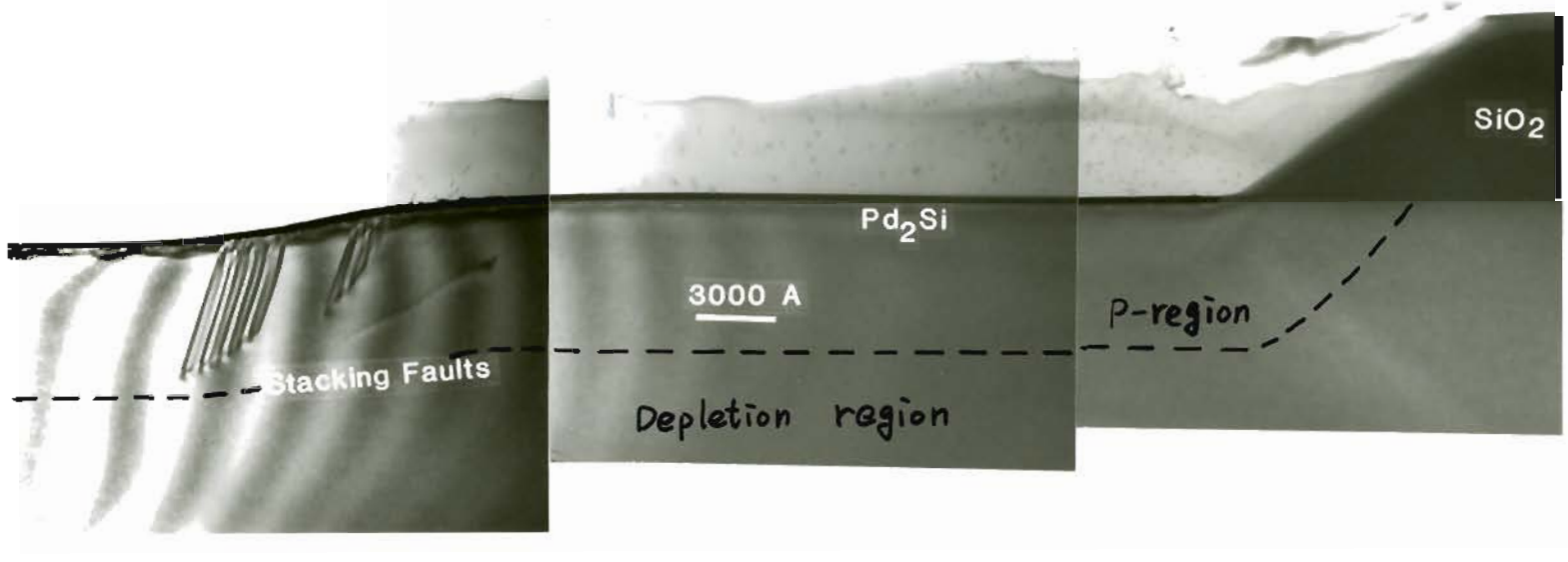


Figure 33. Cross-section TEM micrograph of diode containing stacking faults in the P-region

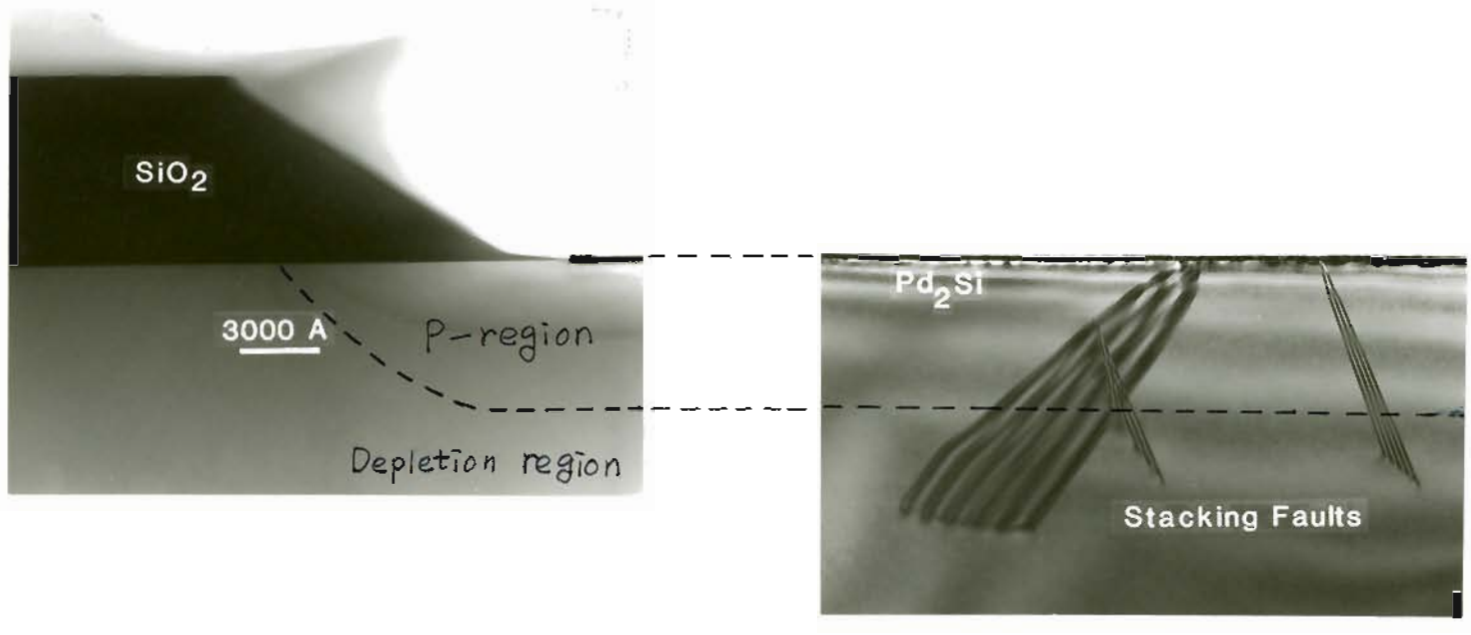


Figure 34. Cross-section TEM micrograph of diode containing stacking faults extended into the depletion region

diodes were investigated. The semi-logarithm plot of current(I)-voltage (V) for forward bias is shown in Fig. 35, and in more detail in 36 and 37. It is seen from Fig. 36 that the control diode, which has no fault, shows the expected exponential dependence of current on voltage over seven orders of magnitude of current for forward bias. The slope of this linear relationship when plotted on a semi-log graph is the theoretically expected room temperature value of 1 decade of current per 60mV increased forward bias. Therefore, from eq. (29), the diode ideality factor,n equal to 1.01, indicates a high quality diode. At higher current levels, the experimental data deviate from the linear relationship due to the ohmic resistance of the N and P-regions. However, the diodes containing stacking faults showed two significant changes for forward bias; higher series resistance for all diodes containing faults, as shown in Fig. 36, and n changes from 1.01 to 1.7 for diodes containing faults extended into the depletion region as shown in Fig. 37.

Let us first consider the diodes containing stacking faults within the P-region. The I-V characteristics follow exactly the ideal diode behaviour at low forward bias of less than 0.5 V as shown in Fig. 36, which indicates that the diffusion current of diodes containing stacking faults does not change due to stacking faults. Here I_o is a function of mobility(u) and lifetime(t) as shown in eq. (23). These are parameters for holes in the N-region, and faults are within the P-region. Therefore, it is anticipated that stacking faults in the P-region do not change these parameters and I_o, which agrees well with the

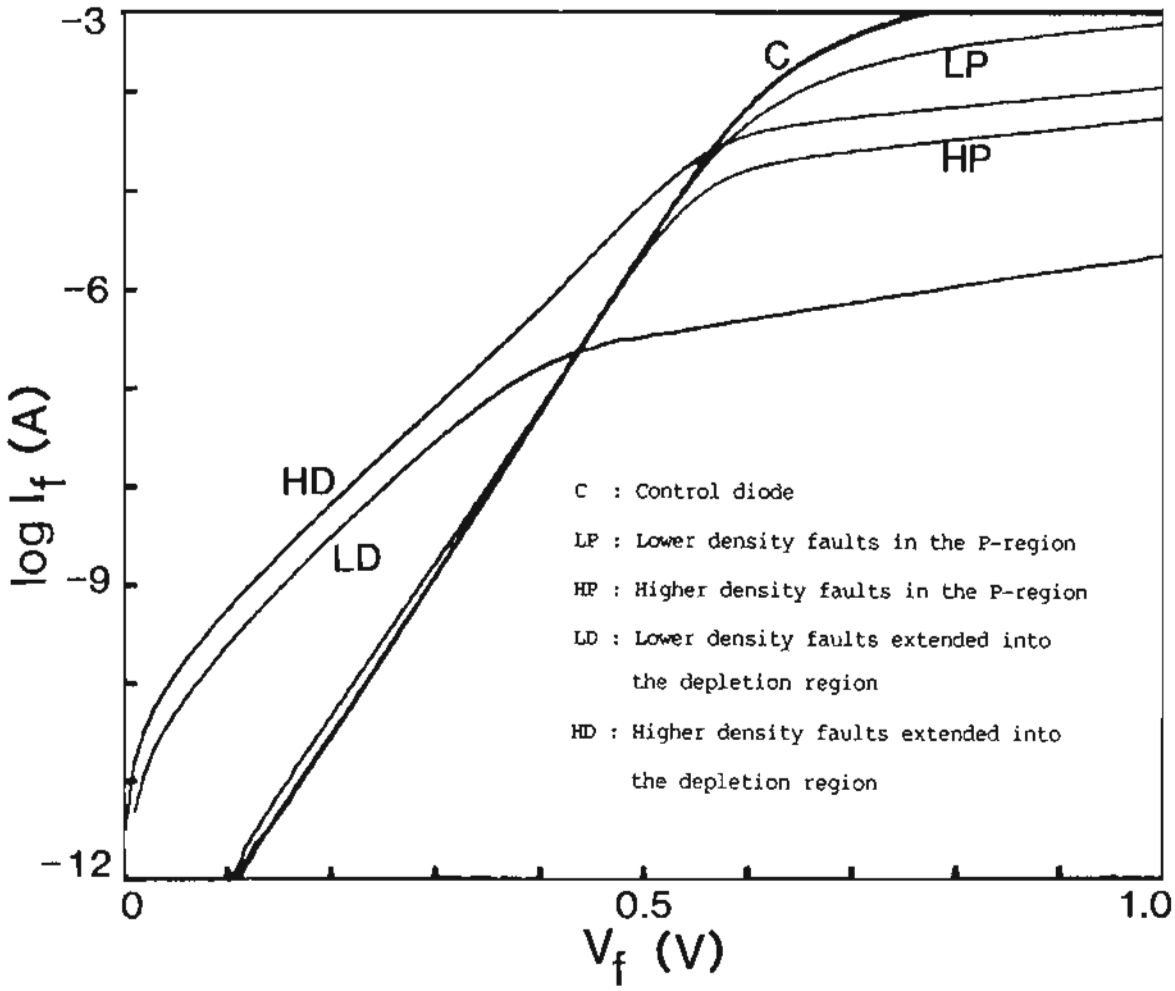


Figure 35. Current(I)-Voltage(V) characteristics of diodes containing stacking faults for forward bias

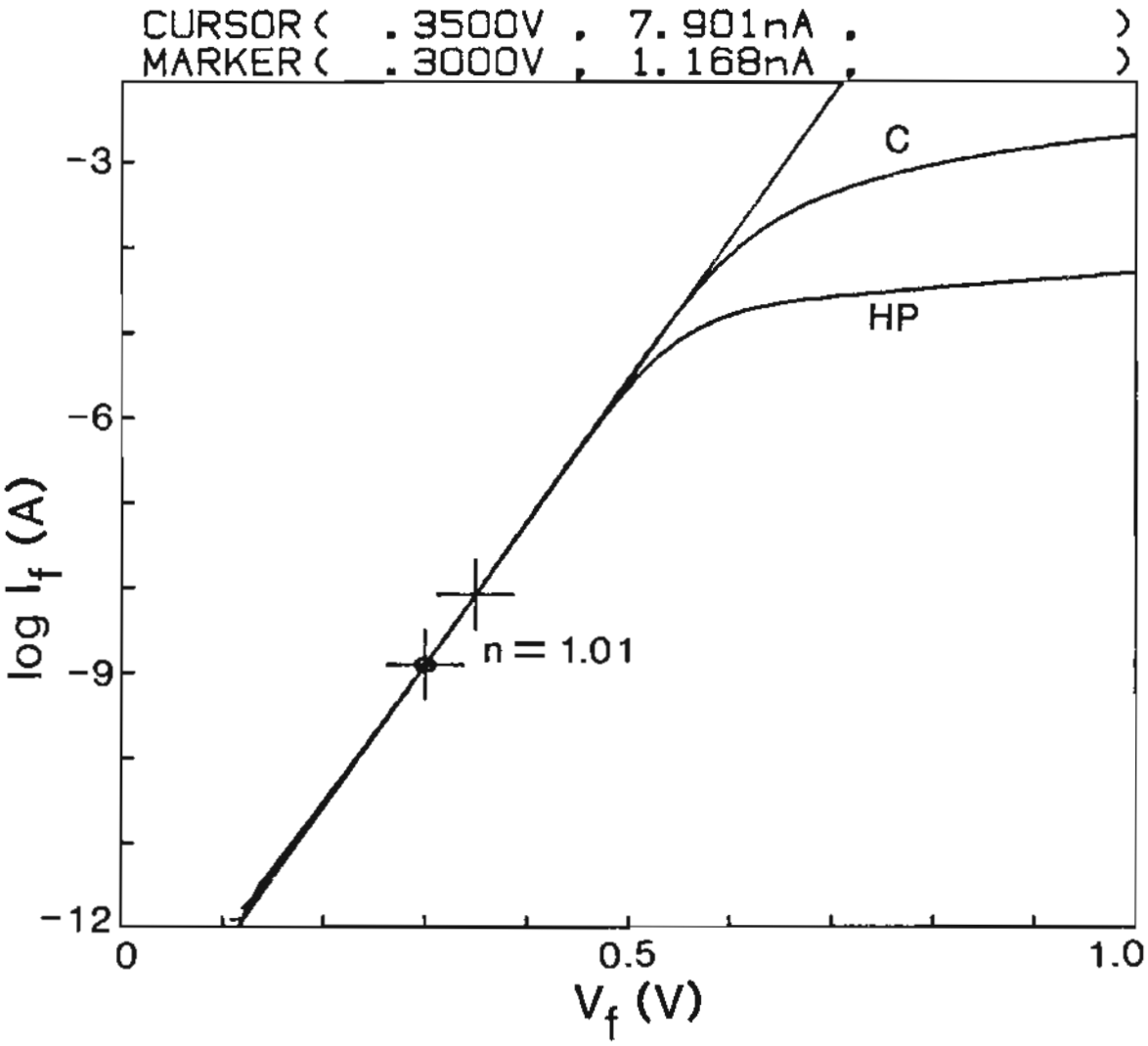


Figure 36. Comparison of diode containing faults in the P-region with control diode

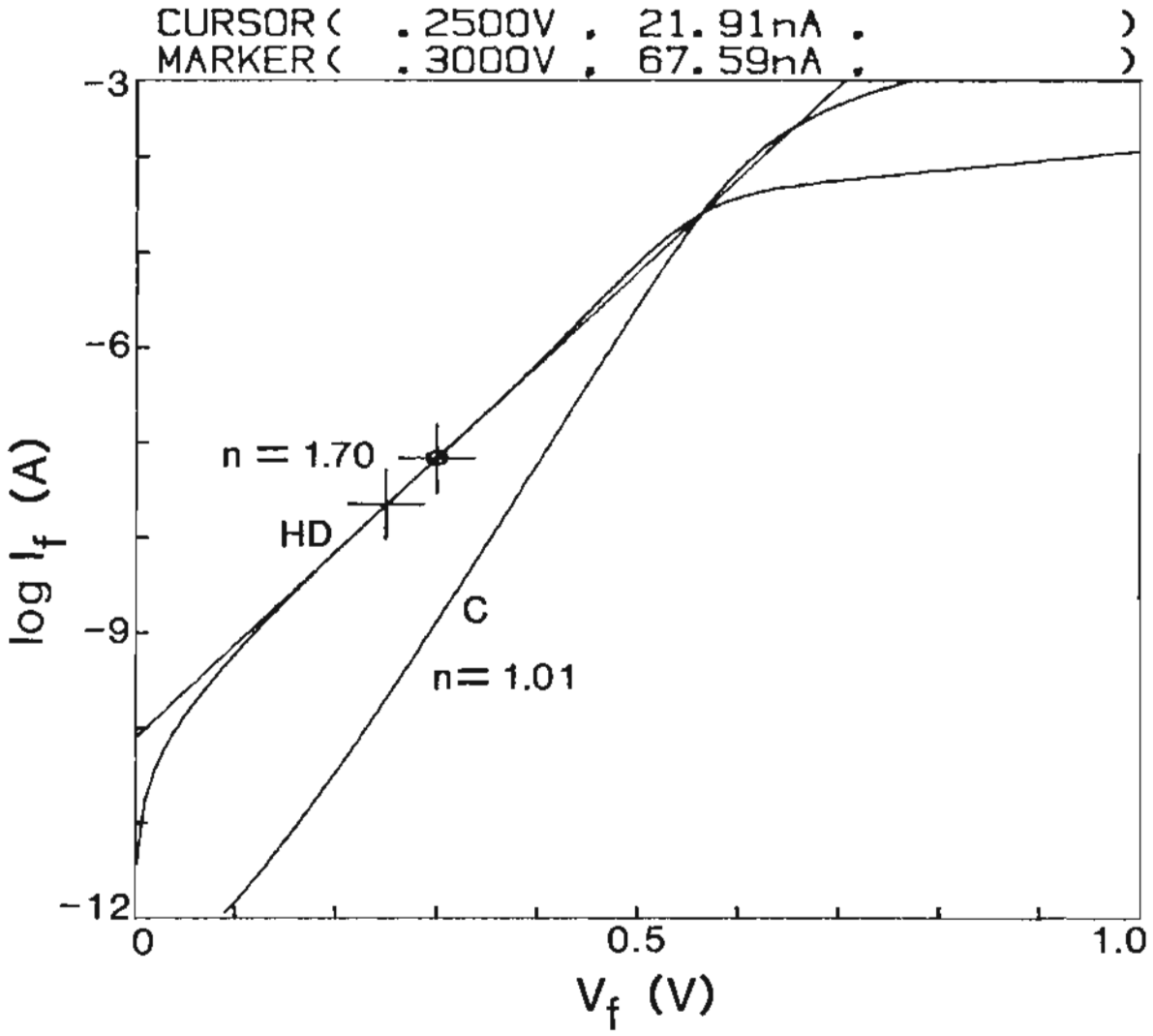


Figure 37. Comparison of diode containing faults extended into the depletion region with control diode

experimental data. There are SRH trap sites in the N-region which produce diffusion current by recombining holes. However, the number of sites or their energy level in the forbidden gap may not be affected since stacking faults are generated in the P-region, which, also, predicts no change of I_o. Therefore, it is concluded that at lower forward bias the electrical properties of diodes containing faults in the P-region follow exactly the control diodes without any change in lifetime, mobility and ideality factor, as predicted.

At the higher forward bias, diodes containing faults in the P-region show a higher series resistance (7000 Ω) than the control diodes (200 Ω). The only difference is that the former contains faults and so it is concluded that the higher resistance is directly related to faults in the P-region. There are several parameters, such as P-region mobility and effective diode area(A), which may be affected by faults. Let us assume that there exists a space charge region around the partial dislocation of a fault due to strain field or impurities. Calculation shows that the space charge region has a radius of about 100 A (9,26). This neither significantly reduces the diode cross section area(A) nor reaches down to the P-N junction space charge region below the faults. If the fault did touch the space charge region there would occur a large leakage current. However, diode containing faults in the P-region exactly follows the control diode behaviour and shows no leakage at lower bias, which proves that the faults do not "short-circuit" a P-N junction and that they do not reduce the diode cross section area. Therefore, the only explanation for the increased

resistance is that there is a reaction, i.e., scattering, between the hole movement and faults from the top surface of P-region to the 0.45 um depth of P-region where fault extension terminates, which is believed to affect the hole mobility. The reason why this phenomenon was not shown at lower forward bias is due to the "dynamic resistance" of a diode, as shown in Fig. 38. Using eq. (29) diode resistance is expressed as following equation because of R=V/I.

$$R = \frac{V}{I_o} \, EXP(- \frac{qV}{nkT}) \qquad \text{----------(30)}$$

Eq. (30) shows that diode resistance dereases almost exponentially as voltage increases, whereas P & N-region series resistance is constant. Since the diode resistance is very large at lower forward bias, diode resistance is dominant at lower forward bias and the series resistance only becomes dominant at higher forward bias. This results in unchanged current level at lower bias even though the series resistance increases from 200 Ω to 7000 Ω due to stacking faults.

Assuming that t is in the range of 1E-7 to 1E-4 second and u is 150 cm^2/Vsec for p = 1E18 from Fig. 39, L is calculated to be 6 to 200 um using the Einstein relationship and L^2=Dt. The fault density of 1E6 to 1E7/cm^2 provides the fault space of 10 to 3 um, respectively. Therefore, it can be assumed that holes generated in the P-region cross over the P-N junction to the N-region without recombining in the P-region since the diffusion length is long enough compared to a junction

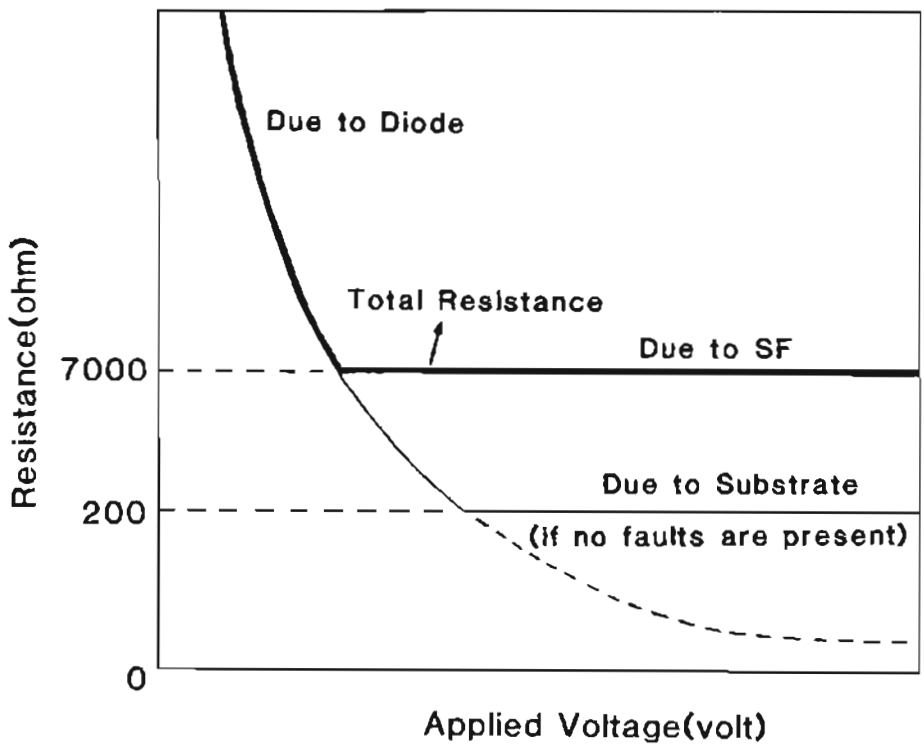


Figure 38. Schematic diagram of voltage dependence of diode resistance

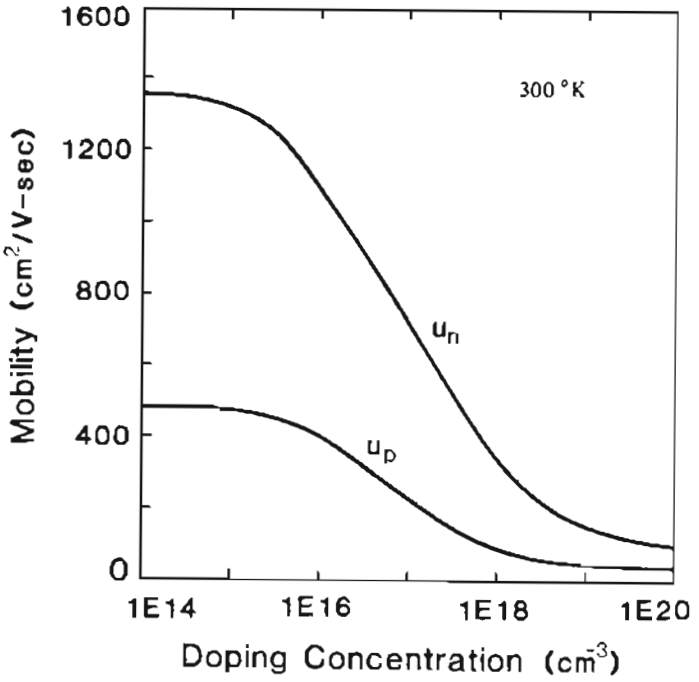


Figure 39. Variation of charge carrier mobility with doping concentration(59)

depth of 0.6 um and that holes near stacking faults experience severe scattering.

In order to discuss scattering the mean free path of holes which is defined as the distance between two elastic scattering events has to be estimated. The mean free path is deduced to be about 100 A based on the mobility, being about 200 $cm^2/V\text{-}s(80)$. In the P-region holes drift randomly toward the junction because there is a very weak electric field there. Therefore, holes near and distant from stacking faults will experience scattering from stacking faults before crossing the P-N junction. Thus the sum of these scattering events is measured in the form of a resistance increase (R_F). Stacking faults are essentially an extra plane stacked among regular (111) planes such as ABCABC$\bar{C}$ABCABC. This is a planar lattice disturbance which provides the scattering sites for holes together with a strain field and a partial dislocation surrounding it.

In order to understand the diode/defect interaction more completely the effect of temperature (25 C to 150 C) on the diode behaviour was studied. Fig. 40 shows the forward bias currents of control diodes as a function of voltage at different temperatures. In the resistor region of the curve, above 0.7 V, the current is nearly independent of temperature while in the diode region, below 0.3 V, a 4 orders of magnitude change is seen for the control diodes, as expected theoretically. However,the current levels of diodes containing faults in the P-region, and diodes containing faults extended into the depletion region show lower currents in the resistor region that increase sharply

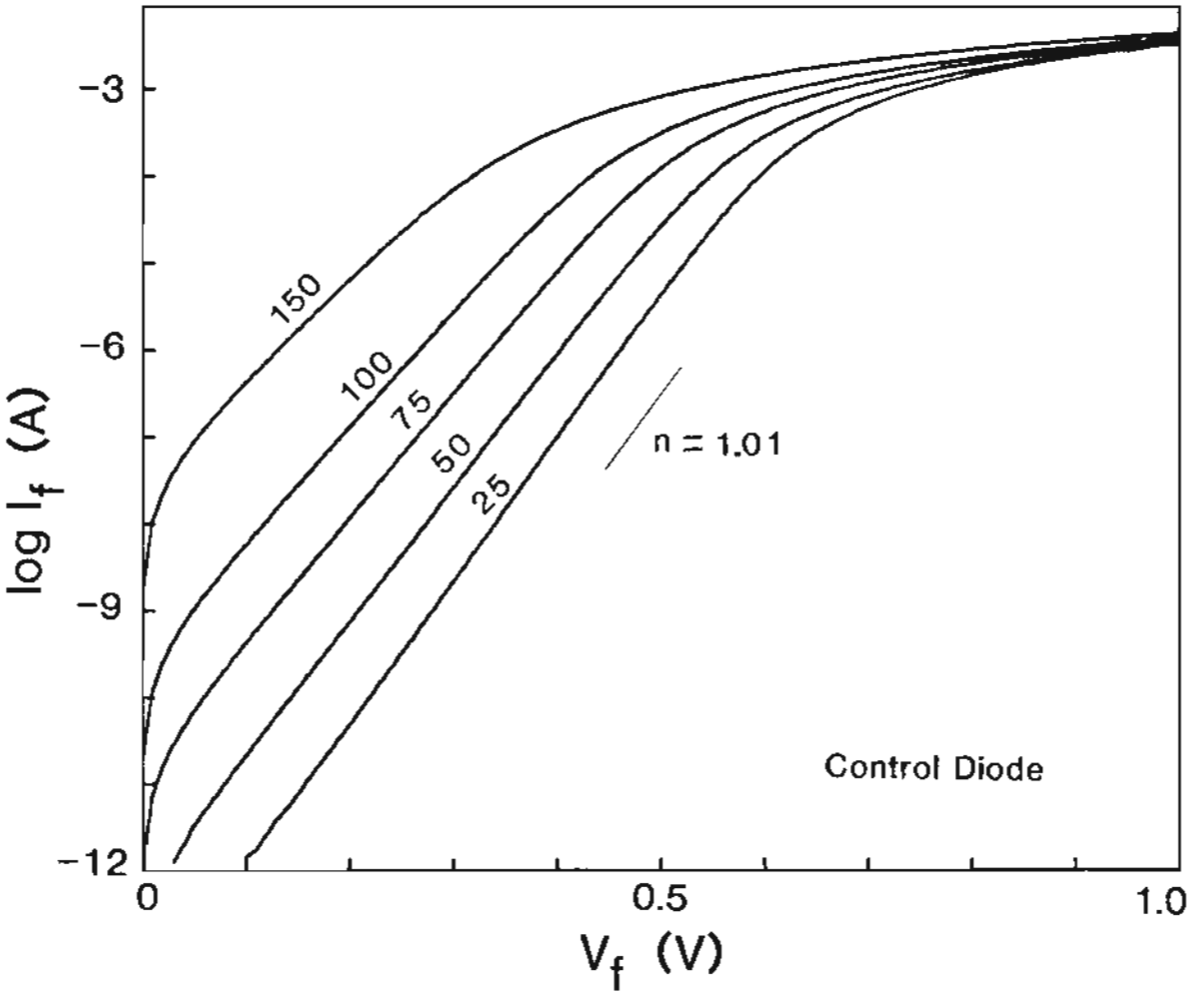


Figure 40. Temperature dependence of I-V characteristics for control diode

with temperature as shown in Fig. 41 and 42, respectively, until reaching 5E-3 Ampere at 1 Volt which is the about maximum value of the control diode.

Diode model is developed considering R_F connected serially to R as shown in Fig. 43. The method used to evaluate $R=R_n+R_p$ is shown in Fig. 44. Here, in the resistor region(above 0.7 V) the slope tells this value because of I=V/R. $R=R_p+R_n$ was measured to be about 200 Ω at room temperature, which is believed to be mostly contributed by R_n since the N-region length is the wafer thickness. Likewise, R_F, which is a resistance increase due to stacking faults, was measured to be 7000 Ω at room temperature. Hence, the resistance increase from R = 200 Ω to R_F = 7000 Ω is due to stacking faults of 1E7/cm^2. Also, it is shown from Fig. 35 that resistance decreases with the density of stacking faults from 7000 Ω to 1000 Ω for 1E7/cm^2 to 1E6/cm^2, respectively, because of less scattering. It is shown from Fig. 41 that R_F for 1E7/cm^2 density decreases as the temperature increases by 7000 Ω, 3200 Ω, 1700 Ω and 500 Ω for 25 C, 50 C, 75 C and 100 C, respectively.

In case of a diode containing faults extended into the depletion region, two things should be mentioned for forward bias from Fig. 35. First, the recombination current dominates the diffusion current(i.e., n=1.7). The higher value of n implies that the current is produced by recombination of charge carriers at the faults that now exist in the depletion region. Faults in the depletion region provide the recombination sites and so the higher fault density produces the higher current level.

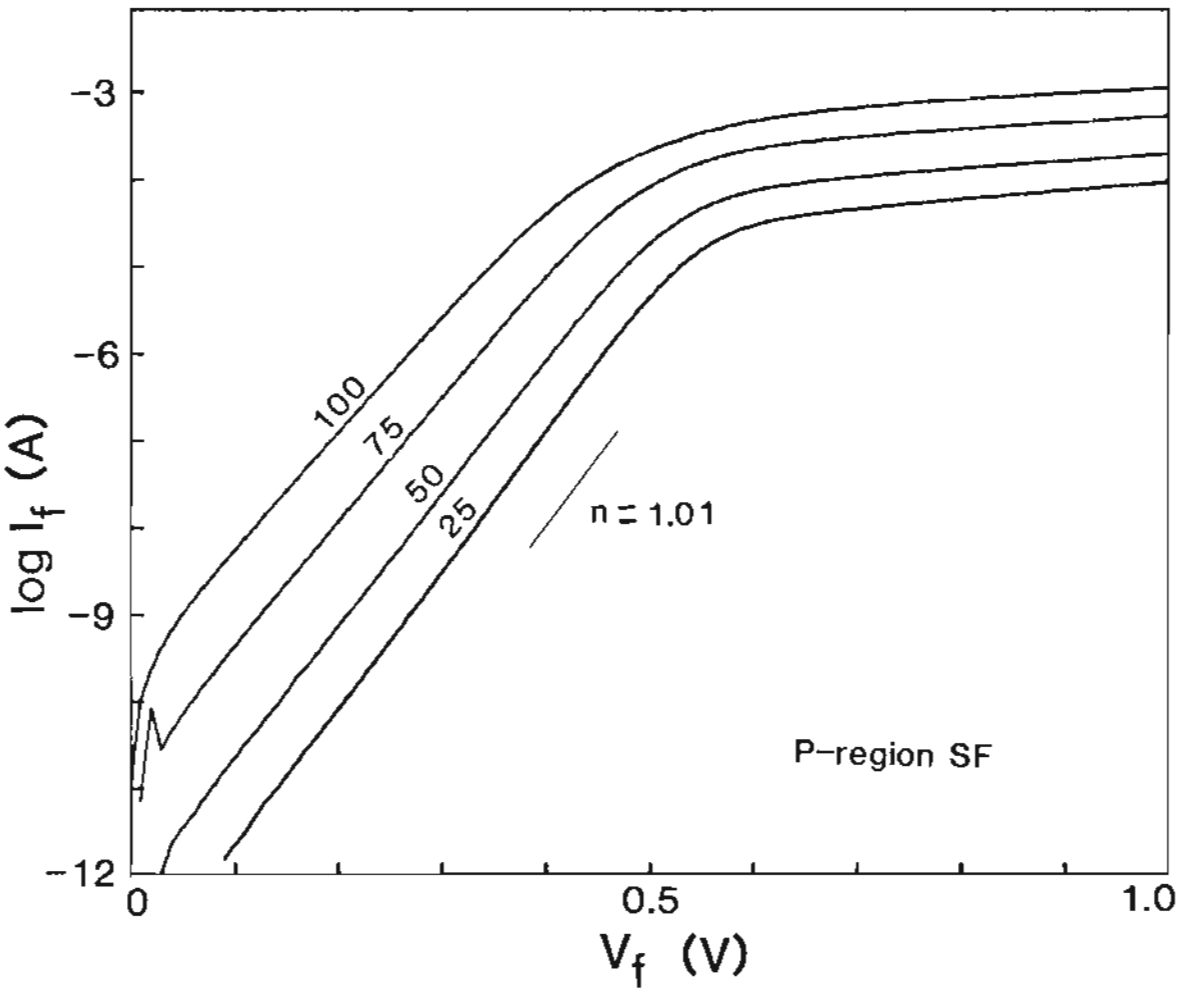


Figure 41. Temperature dependence of I-V characteristics for diode containing faults in the P-region

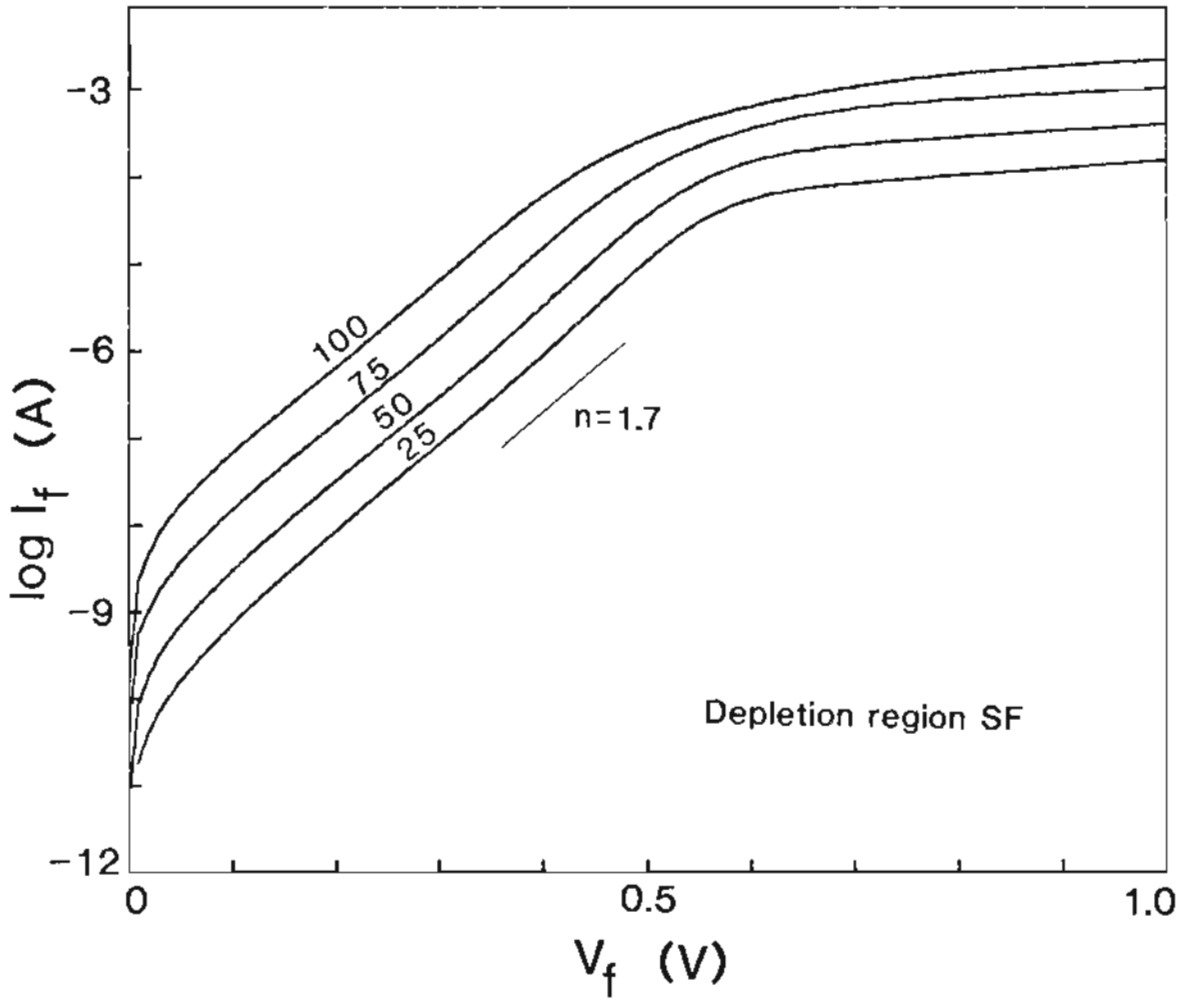


Figure 42. Temperature dependence of I-V characteristics for diode containing faults extended into the depletion region

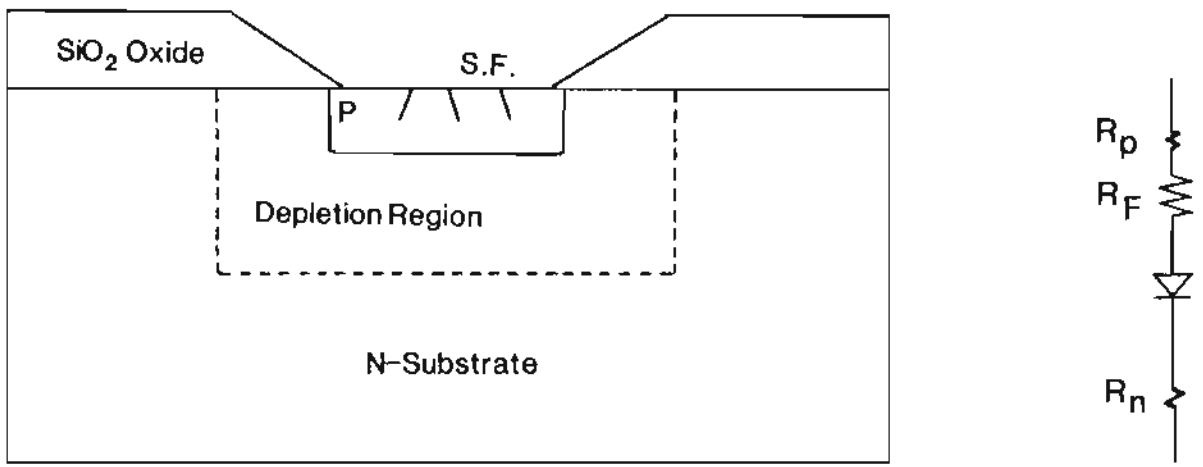


Figure 43. Model of equivalent circuit for P-N junction containing faults in the P-region

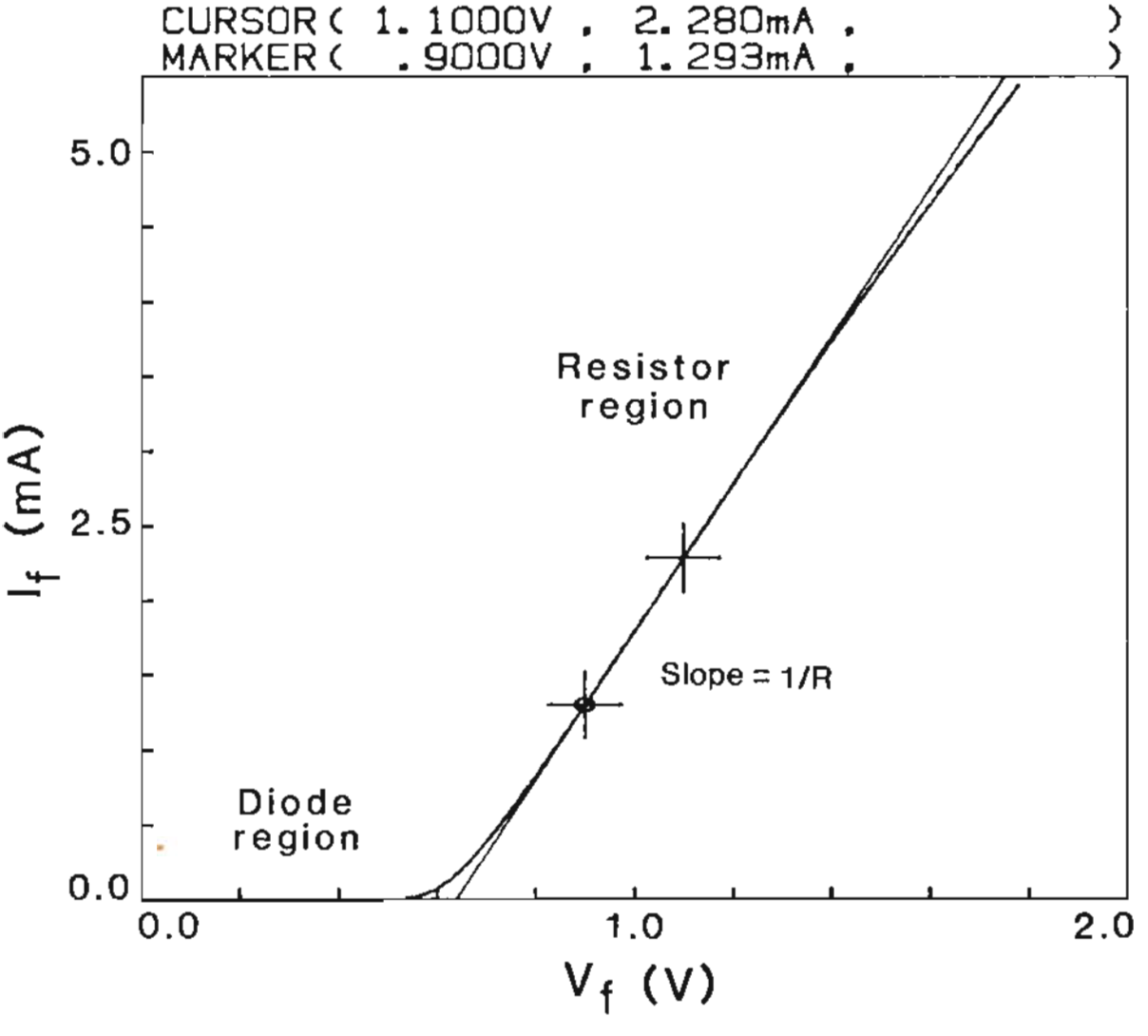


Figure 44. Resistance measurement for control diode

Second, an opposite effect of the fault density on series resistance is found for faults in the P or the depletion regions. This can be explained by introducing the concept of current pipes through dislocation lines surrounding the faults. The partial dislocation around a fault penetrates through the boundary between the P and the depletion regions. Along dislocation pipes holes can travel easily from the P-region to the N-region via the depletion region so that the higher fault density provides the higher leakage current level as shown in a model of Fig. 45. However, there is still a higher value of resistance with these faults when compared to the control diode, presumably due to the increased series resistance in the P-region, just as for the case of the shallow stacking faults considered earlier.

In reverse bias, as shown in Fig. 46, diodes containing faults in the P-region follow the control diode behaviour except for an earlier breakdown. Stacking faults may cause the depletion layer boundary to be less planar as proposed by Ravi, et al(25). The increased curvature of boundary will lower its breakdown voltage due to a local increase in the electrical field. Finally, the soft breakdown occurs with diodes containing faults extended into the depletion region which also may be caused by local variations in breakdown voltage due to stacking faults. Another possible cause for these is due to point defects produced during P-N junction fabrication process. DLTS (Deep Level Transient Spectroscopy) study is recommended to identify if point defects are present(81).

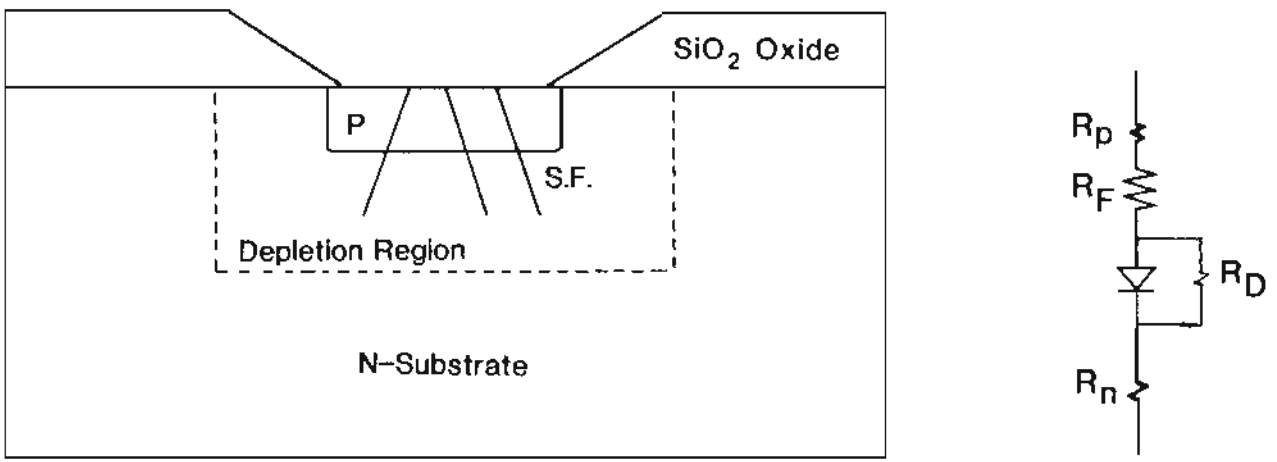


Figure 45. Model of equivalent circuit for P–N junction containing faults extended into the depletion region. R_D is resistance through partial dislocations.

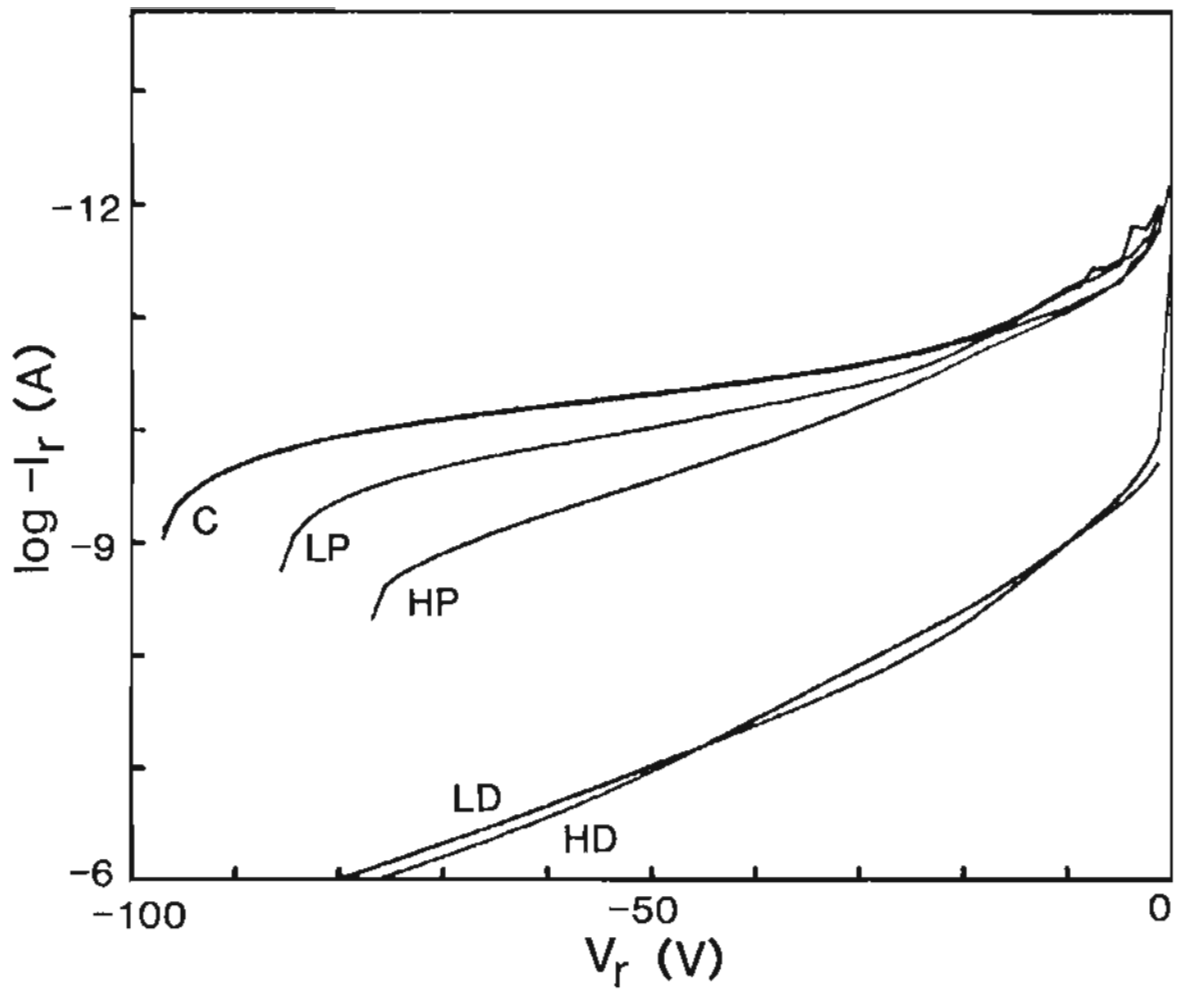


Figure 46. I-V characteristics of diodes containing stacking faults for reverse bias

IV. 4. Electrical performance of P-N junctions containing dislocation loops

Figs. 47-49 show the cross section TEM micrographs of diodes containing dislocation loops in the P, depletion and N-regions. As for the stacking fault case, dislocation loops start to appear at about 5 um from the SiO_2 at the diode edge. Dislocation loop density for the depletion and the N-region cases are nearly equal but much lower than for the P-region case. This is due to the high temperature anneal during epitaxial growth.

In order to locate dislocation loops well below the depletion layer a N-type epitaxial layer of silicon was grown on top of these defects. The electrical performance of the defect free P-N junction (CE) due to the epitaxial layer was changed slightly from the control diode (C) as shown in Fig. 50. Here, CE is the control diode containing no dislocation loops with the epitaxial grown and C is the control diode without the epitaxial grown. This effect should be subtracted from diode data that contain dislocation loops buried by the epitaxial layer. CE shows slightly higher current at a given voltage and increased ideality factor, n. This change implies a higher recombination rate in the depletion region which now exists in an epitaxial layer rather than in the substrate. The source of this effect is not understood but may be due to impurities in the epitaxial layer.

At lower forward bias where the diode controls the I-V characteristics, as long as dislocation loops are located in the P-region, the

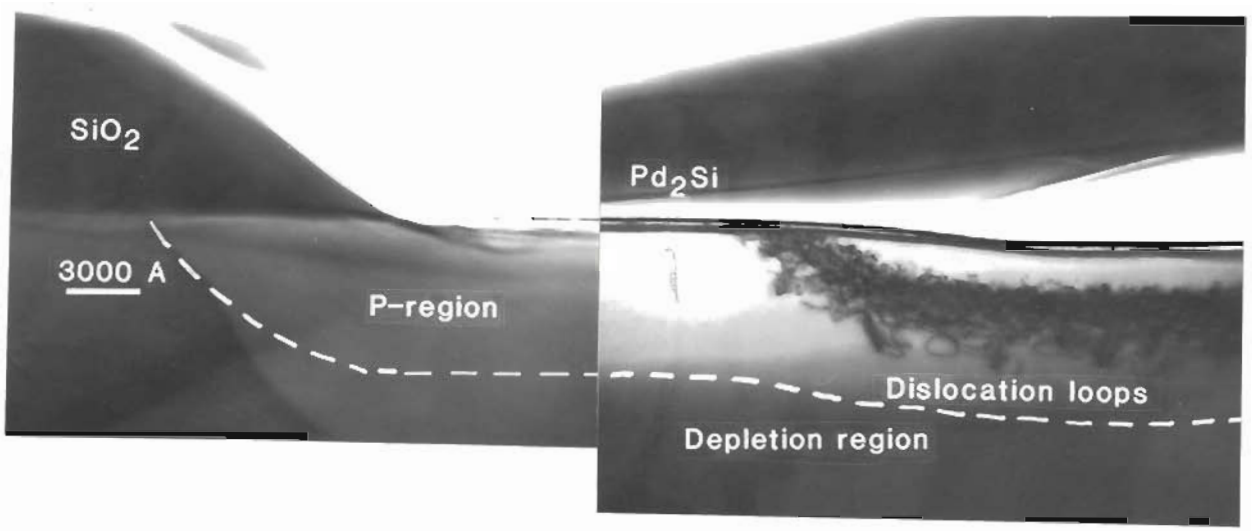


Figure 47. Cross-section TEM micrograph of diode containing dislocation loops in the P-region

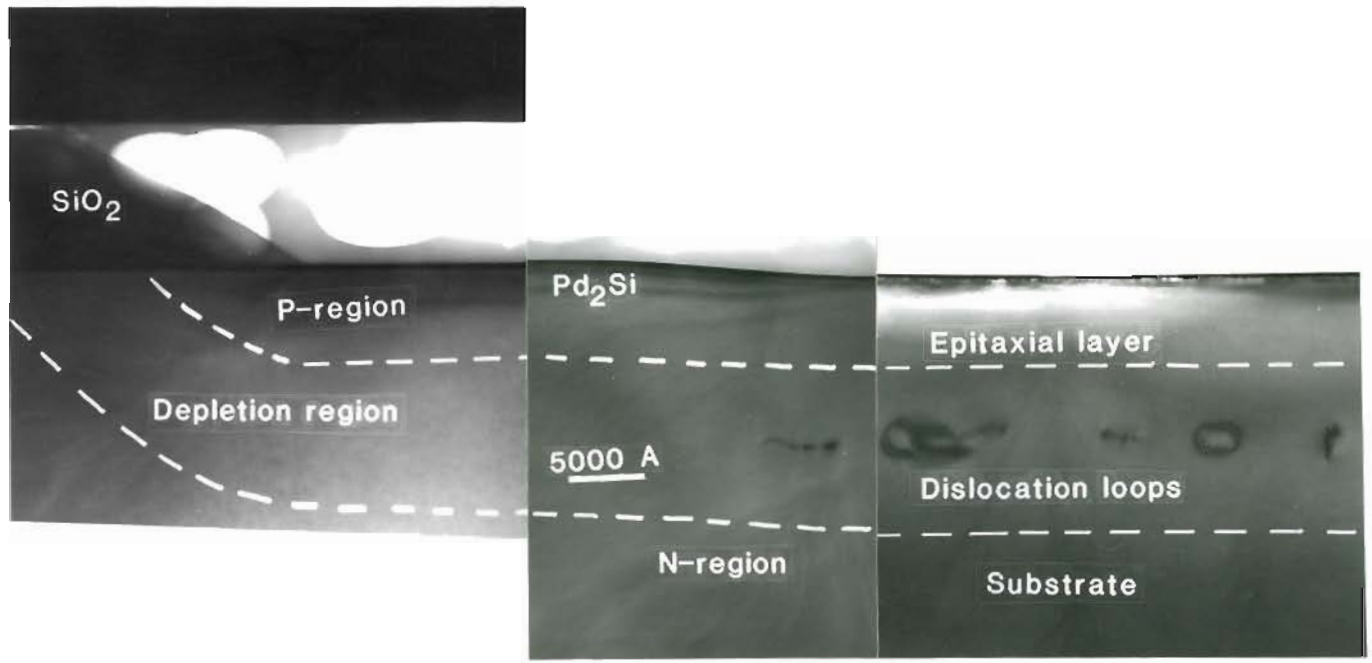


Figure 48. Cross-section TEM micrograph of diode containing dislocation loops in the depletion region

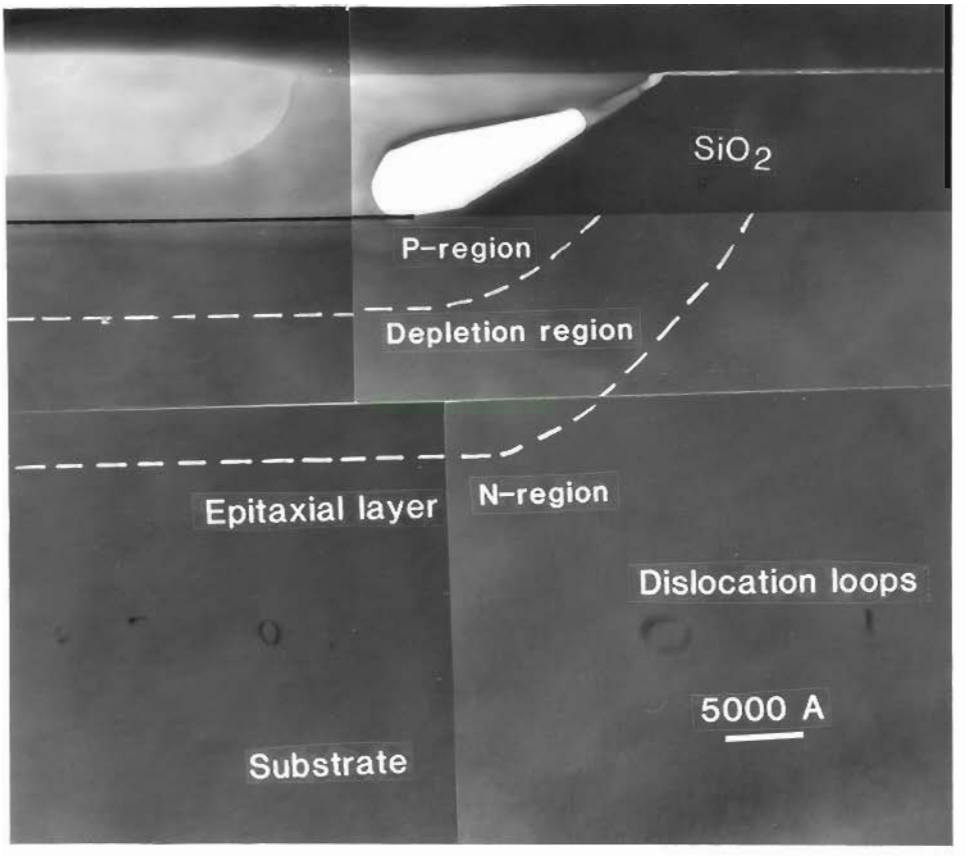


Figure 49. Cross-section TEM micrograph of diode containing dislocation loops in the N-region

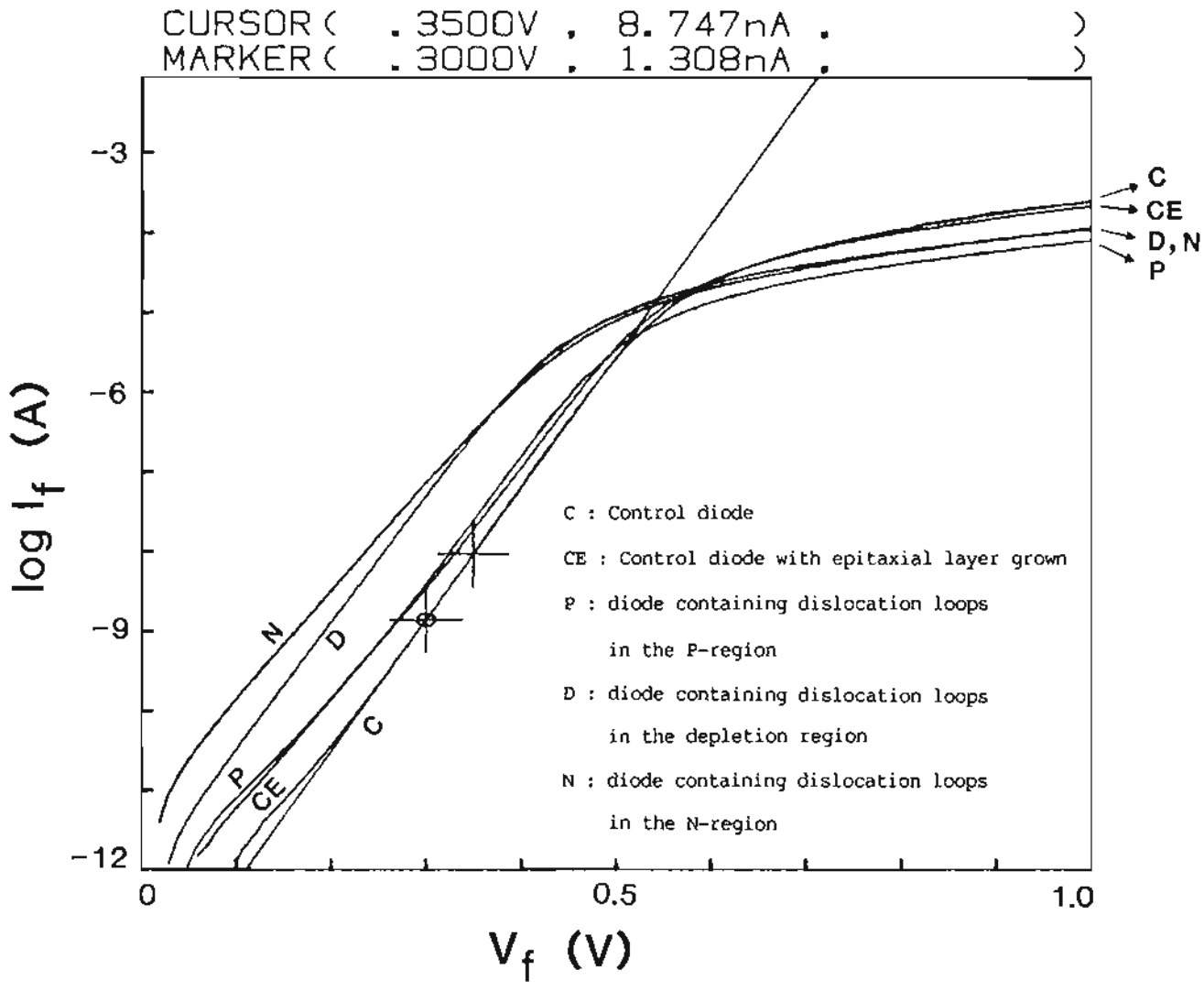


Figure 50. I-V characteristics of diodes containing dislocation loops for forward bias

I-V plot is identical to that of the defect free diode. Even though dislocation loops of very high density exist (Fig. 47), they do not affect the minority carrier (hole) concentration (on the N-region of the diode), which is the same result as for the stacking fault case. However, dislocation loops in the depletion region (D) and the N-region (N) create a higher diffusion current (n is close to 1) which is verified by the slopes of those two curves. The N-region dislocation loops were separated from each other by a few microns and were at about 1.5 um below the N-side depletion region boundary; a shorter distance than the diffusion length because L is typically about 50 um. Hence, L will be reduced to about 1.5 um and recombination of injected holes from a P-region will be enhanced by dislocation loops causing the lifetime of holes to decrease, which increases I_o and the diffusion current based on eq. (29) and (31).

$$I_o = \frac{qADp_n}{L} = \frac{qAp_n\sqrt{D}}{\sqrt{t}} \qquad \text{(31)}$$

The depletion region dislocation loops should act as recombination sites and thus give rise to recombination current(i.e. n⇒2.0). The electric field in the depletion region is about 10^4-10^5 V/cm so carriers will be moving at their maximum thermal velocity. They must be able to provide enough EHP recombination sites to trap the rapidly moving carriers. However, their density is so low that the recombination current is not dominant and n is close to 1. Also, the diffusion

current level increases subtantially. This may be due to some of the loops being deep enough to get into the N-region since the depletion region shrinks at forward bias increase.

At higher forward bias, Fig. 50 shows a slight increase of resistance due to dislocation loops from 1000 Ω to 3000 Ω regardless of their locations. Contrary to the stacking fault case in the P-region (HP) in Fig. 36, P-region loops show less increase of resistance with respect to the control diode even though the loop density is very high. Therefore, the scattering mechanism of dislocation loops seems to be different from that of stacking faults. Fig. 51 shows the DF TEM micrographs of dislocation loops inside the diode from the [111] orientation. A loop designated as A dissapears with g=[022] and B loop dissapears with g=[202]. Fig. 52 shows the weak beam DF image of dislocation loops with (g,2g) condition of g=[220] from the [111] orientation which reveals that there are no stacking fault fringes inside the loop (A). Combining this with g*b calculations from Fig. 51, it is concluded that the dislocation loops are not Frank partial dislocation loops like stacking faults but perfect dislocation loops. This may indicate why the dislocation loop case shows lower resistance. Namely, stacking faults provide the planar type scattering sites due to extra $\overline{B}$ plane whereas perfect dislocation loops provide only the line type scattering sites. Therefore, even though P region loops are higher in density compared to the high density P-region stacking faults, they provide less resistance.

Fig. 53 shows the reverse biased condition for diodes containing

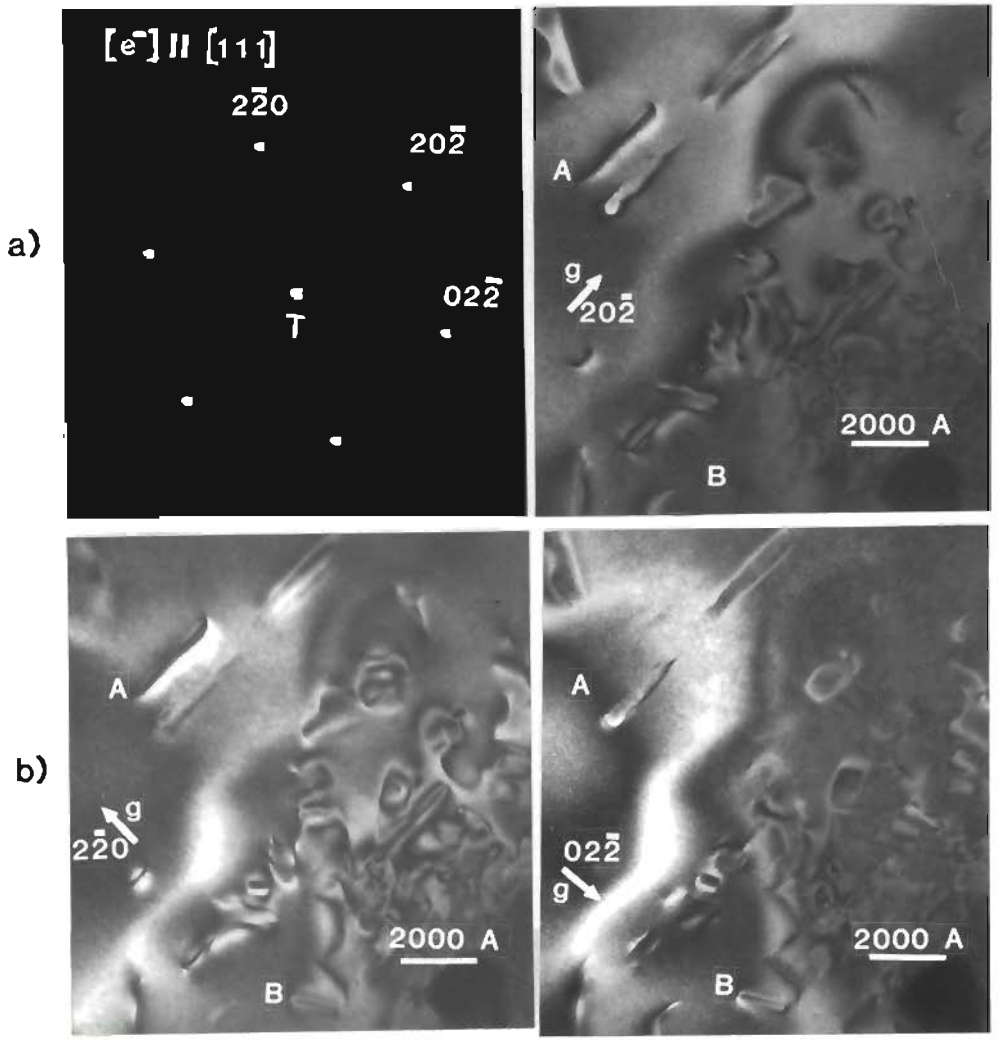


Figure 51. Two beam case DF images of dislocation loops with three different [220] g-vectors from [111] orientation. A is shown with [2$\bar{2}$0] and [20$\bar{2}$]. B is shown with [2$\bar{2}$0] and [02$\bar{2}$].

a) SAD pattern b) g=[2$\bar{2}$0] c) g=[20$\bar{2}$] d) g=[02$\bar{2}$]

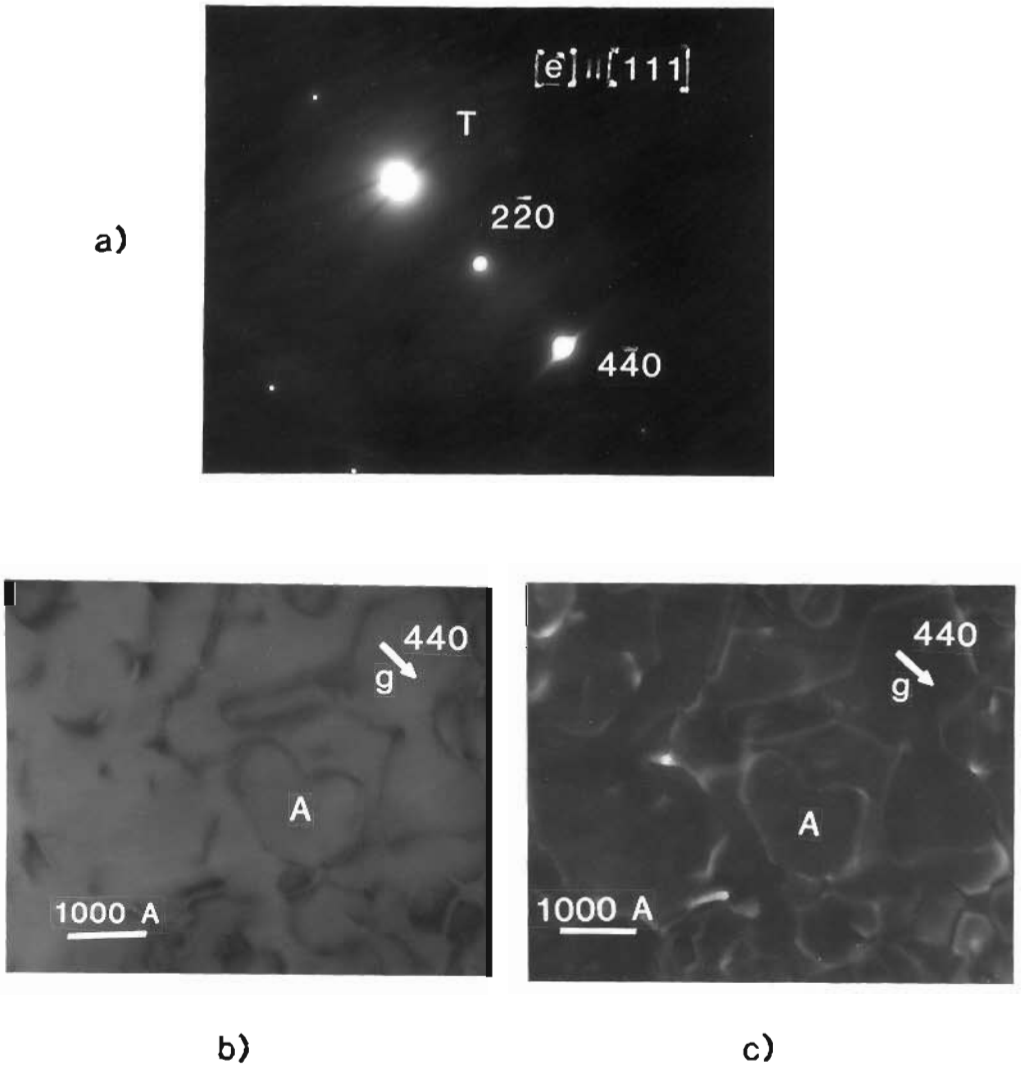


Figure 52. Weak beam DF image of dislocation loops with (g,2g) condition where g=[2$\bar{2}$0]. There is no fringe observed in the loops.
a) SAD pattern b) BF with 2g c) DF with g

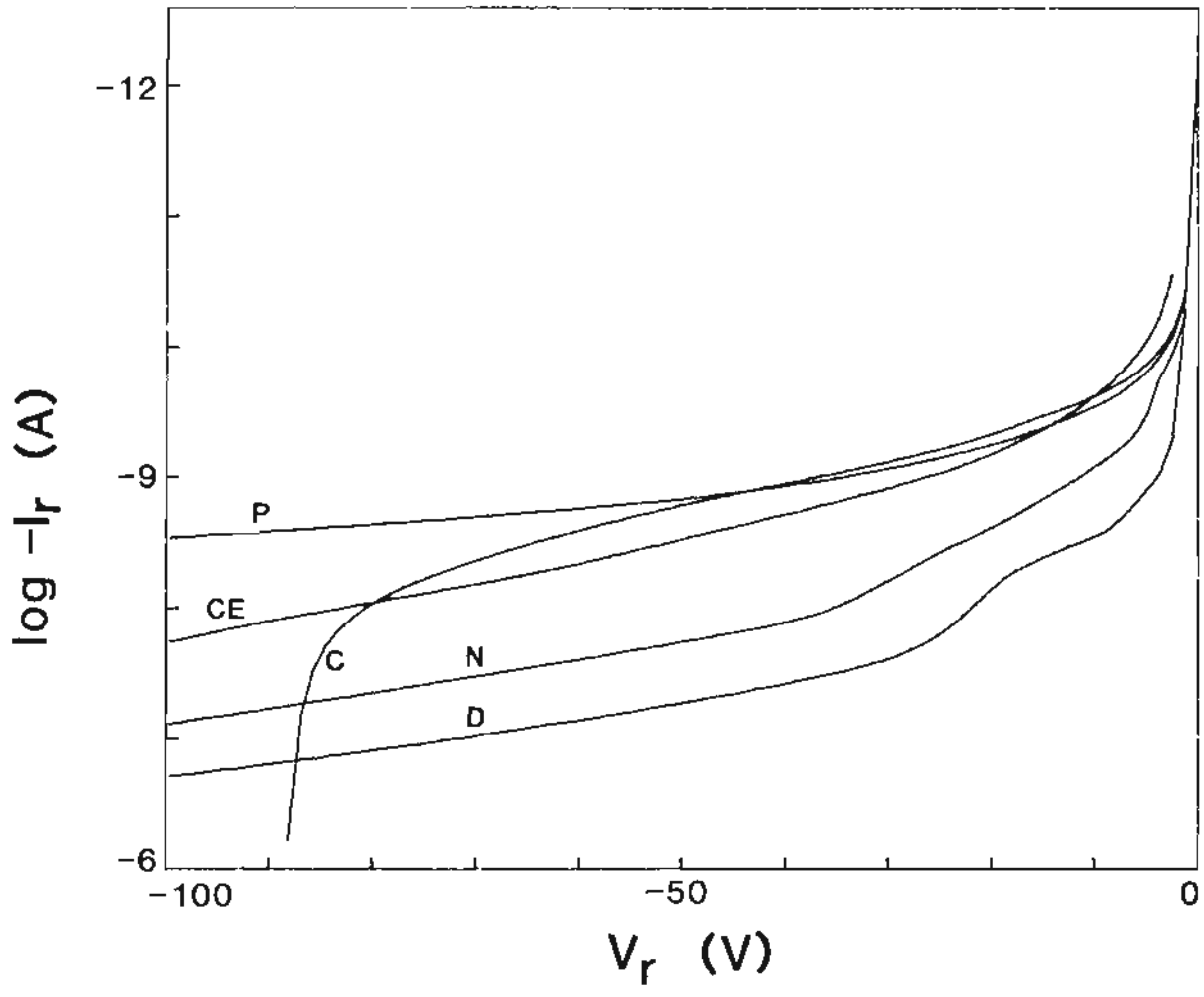


Figure 53. I-V characteristics of diodes containing dislocation loops for reverse bias

loops. CE shows higher generation current than C, similar to a forward bias case. D and N show even higher generation current which is believed to be caused by defects. Dislocation loops in the N-region for zero bias are encompassed in the depletion region as the reverse bias increases to just -1 V. Therefore, it can be assumed that dislocation loops in the N-region for zero bias are in the depletion region for this measurement range of reverse bias. Hence, D and N show higher generation current than CE. Also N shows less generation current than D, which is caused by the dislocation loop density decrease due to the longer self-annealing at 1080 C during the epitaxial growing.

C has a lower breakdown voltage than the other curves which have defects and/or an epitaxial layer. At this moment, it is not clear why they show the higher breakdown. One possibility is that dislocation loops and an epitaxial layer subtract the N-substrate dopants during dislocation generation annealing after silicon implantation and /or during growing epitaxial layer because these are relatively high temperature operation steps. The reduced doping level will increase the breakdown voltage.

V. CONCLUSIONS

1. Dog-bone stacking faults are stacking faults decorated by precipitates.
2. Two kinds of precipitates were observed decorating stacking faults, colonies and plates. Both have $NiSi_2$ structure which is cubic.
3. The chemical composition for colony precipitates is Ni, Cu and Si, and Ni and Si only for the plate type. The colony type has an unstable $NiSi_2$ structure due to Cu substituting on the Ni sites which leads to 5 % increase in lattice parameter. The plate type has the pure $NiSi_2$ structure.
4. The contamination source may be the basic poly-silicon starting material.
5. Diodes containing stacking faults and dislocation loops in the P-region basically act as defect free diodes for lower forward bias where series resistance is not observed.
6. The scattering mechanism of stacking faults is different from that of perfect dislocation loops when these defects are in the P-region. A fault acts as a scattering plate whereas a dislocation loop acts as a scattering line, so that stacking faults provide higher scattering and therefore higher resistance.
7. Diodes containing stacking faults extended into the depletion region have n=1.7 because partial dislocations surrounding stacking faults provide efficient recombination sites.

8. Diodes containing dislocation loops in the depletion region or in the N-region still have n=1 indicating the density and/or efficiency of these traps is too low to affect the current. However, they do show an increased I_o which is due to recombination at dislocation loops.
9. Dislocation loops and epitaxial layers seem to gather the substrate dopants and increase the breakdown voltage.

REFERENCES

1. S. M. Sze, VLSI Technology, McGraw-Hill, New York, 1983
2. G. Moore, Electron. Aust., 42, 14(1980)
3. J. D. Meindl, IEEE Trans. Electron Devices, Vol. ED-31, No. 11 1555(1984)
4. K. V. Ravi, Imperfections and Impurities in Semiconductor Silicon John Wiley & Sons, New York, 1981
5. R. M. Drosd, Ph. D. Thesis, UC Berkeley, November, 1979
6. W. T. Read Jr., Phil. Mag., 45, 775(1954)
7. R. C. Newman, J. Wakefield and J. B. Willis, Solid-State Electronics, Vol. 8, 180(1965)
8. H. F. Matare and C. W. Laakso, J. Appl. Phys., Vol. 40, No. 2 476(1969)
9. H . F. Matare, Defect Electronics in Semiconductors, Wiley-Interscience, New York, 1971
10. P. De Pauw, R. Merteus, R. Van Overstraeten and S. C. Jain, Solid-State Electronics, Vol. 27, No. 6, 573(1984)
11. H. S. Bennett, Solid-State Electronics, Vol. 27, No. 10, 893(1984)
12. D. J. Mbewe, D. J. Thomson, R. D. McLeod and H. C. Card, IEEE Trans. Electron Devices, Vol. ED-31, No. 5, 523(1984)
13. ASTM STP 712
14. W. Schroter, Defects and Radiation Effects in Semiconductors 1978 Conf. Series No. 46, The Institute of Physics, Bristol and London 114(1979)

15. J. R. Patel and L. C. Kimerling, Defects in Semiconductors, North-Holland, 273(1981)

16. G. H. Plantinga, IEEE Trans. Electron Devices, Vol. ED-16, No. 4 394(1969)

17. M. V. Whelan, Solid-State Electronics, Vol. 12, 963(1969)

18. A. C. M. Wang, IEEE Trans. Electron Devices, Vol. ED-21, No. 11 667(1974)

19. L. C. Parrillo, R. S. Payne, T. E. Seidel, M. Robinson, G. W. Reutlinger, D. E. Post and R. L. Field, IEEE Trans. Electron Devices IEDM, 348(1979)

20. M. E. Lunnon, D. F. Allison and W. T. Stacy, Proc. Symposium on Defects in Silicon, The Electrochem. Soc., 463(1983)

21. C. W. Pearce and D. S. Yaney, IEEE Trans. Electron Device Letters Vol. EDL-6, No. 7, 326(1985)

22. S. T. Picraux and P. S. Pearcy, Scientific American, 102(1985)

23. J. B. Lasky, J. Appl. Phys., Vol. 54, No. 10, 6009(1983)

24. A. Kamgar, W. Fichtner, T. T. Sheng and D. C. Jacobson, J. Appl. Phys. Lett., Vol. 45, No. 7, 754(1984)

25. K. V. Ravi, C. J. Varker and C. E. Volk, J. Electrochem. Soc., Vol. 120, No. 4, 533(1973)

26. C. J. Varker and K. V. Ravi, J. Appl. Phys., Vol. 45, No. 1, 272 (1974)

27. T. E. Seidel, S. E. Haszko and D. M. Maher, J. Appl. Phys., Vol. 48, No. 12, 5038(1978)

28. J. M. Dishman, S. E. Haszko, R. B. Marcus, S. P. Murarka and T. T.

Sheng, J. Appl. Phys., Vol. 50, No. 4, 2689(1979)

29. P. S. D. Lin, R. B. Marcus and T. T. Sheng, J, Electrochem. Soc., Vol. 130, No. 9, 1878(1983)
30. J. F. Gibbons, IEEE Proceedings, Vol. 56, No. 3, 295(1968)
31. G. Carter and W. A. Grant, Ion Implantation of Semiconductors, Edward Arnold, London, 1976
32. J. Lindhard and M. Scharff, Phys. Rev., Vol. 124, 128(1961)
33. G. A. Rozgonyi, Proc. Symposium on Defects in Silicon, The Electrochem. Soc. Inc., 29(1983)
34. E. Gabilli, R. Lotti, G. Lulli, P. G. Merli and M. V. Antisari, Japanese J. Appl. Phys., Vol. 24, No. 1, L15(1985)
35. K. Wang, W. G. Spitzer, G. K. Hubler and D. K. Sadana, J. Appl. Phys., Vol. 58, No. 12, 4553(1985)
36. M. Von Heimendahl, Electron Microscopy of Materials, Academic Press, New York, 1980
37. I. L. F. Ray and D. J. H. Cockayne, Phil. Mag., Vol. 22, 853(1970)
38. E. M. Levin, H. F. McMurdie and F. P. Hall, Phase Diagram for Ceramists, Amer. Cer. Soc., 1956
39. M. M. Atalla, Properties of Elemental and Compound Semiconductors, Vol. 5, Interscience, New York, 1960
40. B. E. Deal and A. S. Grove, J. Appl. Phys., Vol. 36, No. 12, 3770 (1965)
41. Y. Z. Lu and Y. C. Cheng, J. Appl. Phys., Vol. 56, No. 6, 1608 (1984)

42. S. M. Sze, Physics of Semiconductor Devices, John Wiley and Sons, New york, 1981

43. J. M. Silcock and W. J. Tunstall, Phil. Mag., Vol. 10, 361(1964)

44. G. R. Bocker and W. J. Tunstall, Phil. Mag., Vol. 13, 71(1966)

45. W. Shockley, Electrons and Holes in Semiconductors, Van Nostrand, New York, 1950

46. B. D. Cullity, Elements of X-Ray Diffraction, Addison-Wesley Publishing Company, Massachusetts, 1956

47. M. H. Loretto and R. E. Smallman, Defect Analysis in Electron Microscopy, Chapman and Hall, London, 1975

48. L. E. Murr, Electron and Ion Microscopy and Microanalysis, Marcel Dekker, New York, 1982

49. J. W. Goodman, Introduction to Fourier Optics, Stanford University, 1968

50. U. Valdre, Electron Microscopy in Materials Science, Academic Press, New york, 1971

51. P. W. Hawkes, Electron Optics and Electron Microscopy, Taylor and Francis, London, 1972

52. D. L. Misell, Practical Methods in Electron Microscopy Vol. 7, North-Holland Publishing, Amsterdam, 1978

53. J. W. Edington, Practical Electron Microscopy in Materials Science, Van Nostrand Reinhold, New York, 1976

54. J. C. H. Spence, Experimental High-Resolution Electron Microscopy, Clarendon Press, Oxford, 1981

55. A. Ourmazd, K. Ahlborn, K. Ibeh and T. Honda, J. Appl. Phys.

Lett., Vol. 47, No. 7, 685(1985)

56. W. Shockley, Bell System Tech. J., Vol. 28, 435(1949)

57. J. L. Moll, Proc. the IRE, Vol. 46, 1076(1958)

58. A. S. Grove, Physics and Technology of Semiconductor Devices, John Wiley and Sons, New York, 1967

59. Ben G. Streetman, Solid State Electronic Devices, Prentice Hall, Englewood Cliff, N. J., 1980

60. C. Sah, R. N. Noyce and W. Shockley, Proc. the IRE, Vol. 45, 1228 (1957)

61. W. Shockley and W. T. Read Jr., Phys. Rev., Vol. 87, September, 835(1952)

62. M. S. Abrahams and C. J. Buiocchi, J. Appl. Phys., Vol. 45, No. 8, 3315(1974)

63. J. Vanhellemont,H. Bender, C. Claeys, J. Van Landuyt, G. Dederick, S. Amelinckx and R. Van Overstraeten, Ultramicroscopy, Vol. 11, 303(1983)

64. K. N. Ritz, M. C. Arst, A. L. Mendonca and M. H. Norcott, Scanning Electron Microscopy, Vol. 1, 121(1984)

65. J. C. Bravman and R. Sinclair, J. Electron Microscopy Technique, Vol. 1, 53(1984)

66. S. N. G. Chu and T. T. Sheng, J. Electrochem. Soc., Vol. 131, No. 11, 2665(1984)

67. T. T. Sheng and R. B. Marcus, J. Electrochem. Soc., Vol. 128, No. 4, 881(1981)

68. S. Solmi, E. Landi and P. Negrini, IEEE Electron Device Letters,

Vol. EDL-5, No. 9, 359(1984)

69. W. Zulehner and D. Huber, Czochralski-grown Silicon, Springer-Verlag Berlin Heidelberg, Crystals 8, 1982

70. M. Wright Jenkins, J. Electrochem. Soc., Vol. 124, 1757(1977)

71. E. Nes and J. Washburn, J. Appl. Phys., Vol. 44, 3682(1973)

72. G. Das, J. Appl. Phys., Vol. 44, 4459(1973)

73. W. T. Stacy, D. F. Allison and T. C. Wu, Semiconductor Silicon, Proc. Electrochem. Soc., 344(1981)

74. P. S. D. Lin, R. B. Marcus and T. T. Sheng, J, Electrochem. Soc., Vol. 130, No. 9, 1878(1983)

75. J. M. Poate, K. N. Tu and J. W. Mayer, Thin Films-Interdiffusion and Reactions, Wiley-Interscience, New York, 1978

76. S. S. Lan and W. F. van der Weg, Solid Phase Epitaxy, Wiley-Inter science, New York, 1978

77. G. Ottaviani, Mat. Res. Soc. Symp. Proc., Vol. 25, 21(1984)

78. J. M. Gibson, R. T. Tung, J. M. Phillips and J. M. Poate, Mat. Res. Soc. Symp. Proc., Vol. 25, 405(1984)

79. S. P. Murarka, Silicides for VLSI Applications, Academic Press, London, 1983

80. J. S. Blakemore, Solid State Physics, Cambridge University Press, Cambridge, 1985

81. D. V. Lang, J. Appl. Phys., Vol. 45, No. 7, 1974

BIOGRAPHICAL NOTE

The auther was born August 28, 1952 in rural area of Seoul, Korea where he spent most of his childhood. He graduated from Kyungbok High School in Seoul, Korea in 1972.

The auther's university career began in 1972 when he attended Seoul National University in Seoul, Korea. There he received his Bachelor of Science degree in Metallurgical Engineering in February, 1976.

He continued his study attending Korea Advanced Institute of Science in Seoul, Korea in 1976 where he received his Master of Science degree in Materials Science in February 1978.

In March 1978, he joined Korea Atomic Energy Research Institute in Seoul, Korea, where he accumulated his career working on Nondestructive Testing field of nuclear power plants for four years. In order to improve his experiences on this field, he visited Southwest Research Institute in San Antonio, Texas for three months in 1979. He accomplished his project engineer responsibility for testing a nuclear power plant in Korea in 1982.

Finally, he began to study at Oregon Graduate Center in Beaverton, Oregon, U.S.A., where he completed the requirements for Doctor of Philosophy degree in Materials Science in August, 1986. During his study, he presented a paper at Materials Research Society Symposium held in Boston in December, 1985. Also, he received NSF scholarship for attending Convergent Beam Electron Diffraction Workshop held in Champaign, Illinois in July, 1986.

The auther is married to Miyoun and has three children who are Minhee of age 5, Sara of age 3 and Ilhee of age 1 and have grandmother, Insun Kim.

He is now leaving the Oregon Graduate Center to accept a Characterization Engineer position at Wacker-Siltronics in Portland, Oregon.

PUBLICATIONS

1. K. Ryoo, R. Drosd and W. Wood, "Characterization of precipitates decorating stacking faults in single crystal silicon", Materials problems solving with the transmission electron microscope, Volume 62, Materials Research Society Symposia Proceedings, Materials Research Society, Pittsburgh, 1986
2. K. Ryoo, R. Drosd and W. Wood, "Characterization of Colony and plate precipitates in silicon with analytical electron microscope", to be published in J. Materials Research