CHARACTERISTICS OF N-CHANNEL ACCUMULATION MODE THIN

FILM POLYSILICON MOSFETS

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Acknowledgements

Several people played important roles in the production of this thesis. I would like to express my deep gratitude to Professor Russ Kremer for guidance and support. Also I would like to give special thanks to Dr. Shahriar Ahmed who gave me insight into the problem and helped me through it. Also I would like to thank Dr. Kim for being very helpful.

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ABSTRACT

Characteristics of N-Channel Accumulation Mode Thin
Film Polysilicon MOSFETs

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The electrical characteristics of N-channel accumulation-mode MOSFETs have been calculated using a model of the conduction process in polysilicon that is based on drift and diffusion of carriers as opposed to earlier models based primarily on thermionic emission. In this model the polysilicon grain boundary is treated as a highly resistive, but conducting medium. Segregation of dopant atoms to the grain boundary due to annealing is taken into account

There are two routes by which polysilicon MOSFETs are fabricated. Polysilicon films can be recrystallized to achieve a device quality single crystalline substrate using several techniques. The other method uses as-deposited films in conjunction with hydrogen passivation of the grain boundary. The model presented here is for these as-deposited films.

This model takes into account the shielding of uncompensated ionized dopants in the channel, when a gate voltage is applied. Current-voltage characteristics are discussed in the three regimes of device operation: leakage, weak accumulation, and drive. Channel electron mobility, grain boundary barrier potential and surface potential are calculated as a function of applied gate voltage for

different film properties. The properties considered are average grain size, doping density, grain boundary trap density and trapping level. Finally the current-voltage relations for a polysilicon MOSFET are calculated and compared to the reported experimental results.

CHAPTER 1

INTRODUCTION

Polycrystalline silicon has recently found an increasing number of important applications in integrated circuit technology. Low pressure chemical vapor deposition (LPCVD) techniques for film deposition and ion implantation or diffusion for doping techniques have given polysilicon many advantages such as lower cost, greater stability and improved yield.

Heavily doped polysilicon films are commonly used as gate electrodes in self aligned Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and as interconnect conductors. For high density MOS integrated circuits polysilicon is used with refractory metal silicides. Lightly doped films are used as high-value load resistors in static memory circuits[1] and as single or double level gates[2] in erasable programmable read only memory (EPROM) and[3] (E^2PROM). They have also been used as the fuse[4] in the fusible-link PROM.

They have been used in bipolar transistors as emitter contacts to improve the gain[5] and as isolation layers in I^2L devices[6]. Polysilicon films have also been used to decrease device size and accompanying parasitic capacitances and resistances. Large-grain polycrystalline silicon has potential for large-volume production of low-cost solar cells. Other passive element applications are also possible.

In the last decade by virtue of device scaling, silicon MOS integrated circuits have improved drastically. Both the circuit density and speed have increased

several fold. To continue these advances, the devices must be scaled down even further. Ideal scaling calls for thinner oxides, higher doping density, shallower junctions, shorter channel length and lower power supply voltages. For several reasons these requirements have not all been met. Needs for TTL compatibility, adequate noise margin, higher speed and functionality over a large temperature range prevent power supplies from being properly scaled. This has put a limit on both the oxide thickness scaling and moat to moat spacing. In complementary MOS (CMOS) technology, this isolation is very important to prevent latch up and other second order problems; thus improvement due to device scaling in MOSFETs is limited.

One way to solve the problems of increased scaling of the devices while still using present technology is adding a new dimension to IC technology. Three-dimensional integrated circuits can decrease the short channel effects, increase packing density and make latch-up a problem of the past.

One of the factors that make polysilicon attractive for use in high-speed bipolar devices is the short carrier lifetime. However problems do exist such as high leakage currents and threshold voltages, reduced transconductance, short carrier lifetime, etc. in the unipolar device structures.

Additional ways exist to make better polysilicon active devices. Present technology is capable of recrystalizing polysilicon producing larger grains. Another way is to passivate the grain boundary. Both of these solutions reduce the problems mentioned before. Finally, polycrystalline silicon also shows promise for making devices on non-crystalline substrates such as sapphire or other insulators using silicon-on-sapphire (SOS) or silicon-on-insulator (SOI) technology.

CHAPTER 2

THEORIES OF ELECTRICAL CONDUCTION IN POLYSILICON

2.1. Previous Models

Polycrystalline silicon films are typically obtained by high temperature decomposition of silane SiH_4 and deposited onto amorphous SiO_2[7,8]. These films are composed of small randomly oriented single crystal islands or grains separated by a region of disorder - called the grain boundary. This structure endows polycrystalline silicon i.e. polysilicon films, with unique electrical properties. Here it is the grain boundaries that play a very important role in governing the electrical conduction process.

One of the pioneering works that provided tremendous physical insight to the electrical conduction process in polysilicon was proposed by Kamins[9]. When performing Hall-mobility measurements on chemical vapor deposited (CVD) polycrystalline silicon films, Kamins observed that the mobility versus dopant concentration behaves in a non-monotonic way and proposed that since the grain boundary is a region of disorder, a substantial number of electrical traps exists at the grain boundary. These traps result from uncompensated bonds, defects, etc. In undoped polysilicon films these traps are initially neutral. When dopants are gradually introduced, carriers contributed by the dopant atoms are trapped at the grain boundary, producing space charge regions on each side of the grain boundary. This space charge region gives rise to a barrier potential qV_B that is naturally a

function of doping density N and the depletion width. Since the density of the traps at the grain boundary is fixed, increasing the doping density eventually saturates the traps. This is accompanied by a decrease in the width of the space charge region, thereby decreasing the barrier potential as shown Fig. 2.1 Kamins used the N-dependent barrier potential as well as scattering of charge carriers by impurities to explain the non-monotonic behavior of mobility versus doping density.

To explain the electrical transport properties of polycrystalline silicon, Seto[10] extended this charge trapping model. To simplify the model several assumptions were made. Seto considered polysilicon to consist of identical crystallites, each having the same grain size L. Within the crystalline regions, the energy band diagram was that of the single crystalline silicon. The material contains only one type of impurity atom and these impurities are totally ionized. Each grain boundary has a negligible thickness and contains both acceptor and donor traps, Q_T/cm^2, located at energy E_T with respect to the intrinsic Fermi level. As in the earlier Kamins model, the traps are initially neutral and become charged by trapping a carrier only when dopants are introduced into the film. Using the abrupt depletion approximation and the above assumptions, Seto calculated the energy band diagram in the crystallites as shown in Fig. 2.1. As the figure shows, all the mobile carriers in the region $(L/2-l)cm$ from the grain boundary are trapped, resulting a depletion region. Here l is the width of the undepleted region on one side of the grain boundary.

Seto introduced the concept of a critical doping density N*, below which the grain is totally depleted. This means that all the mobile carriers are trapped. By
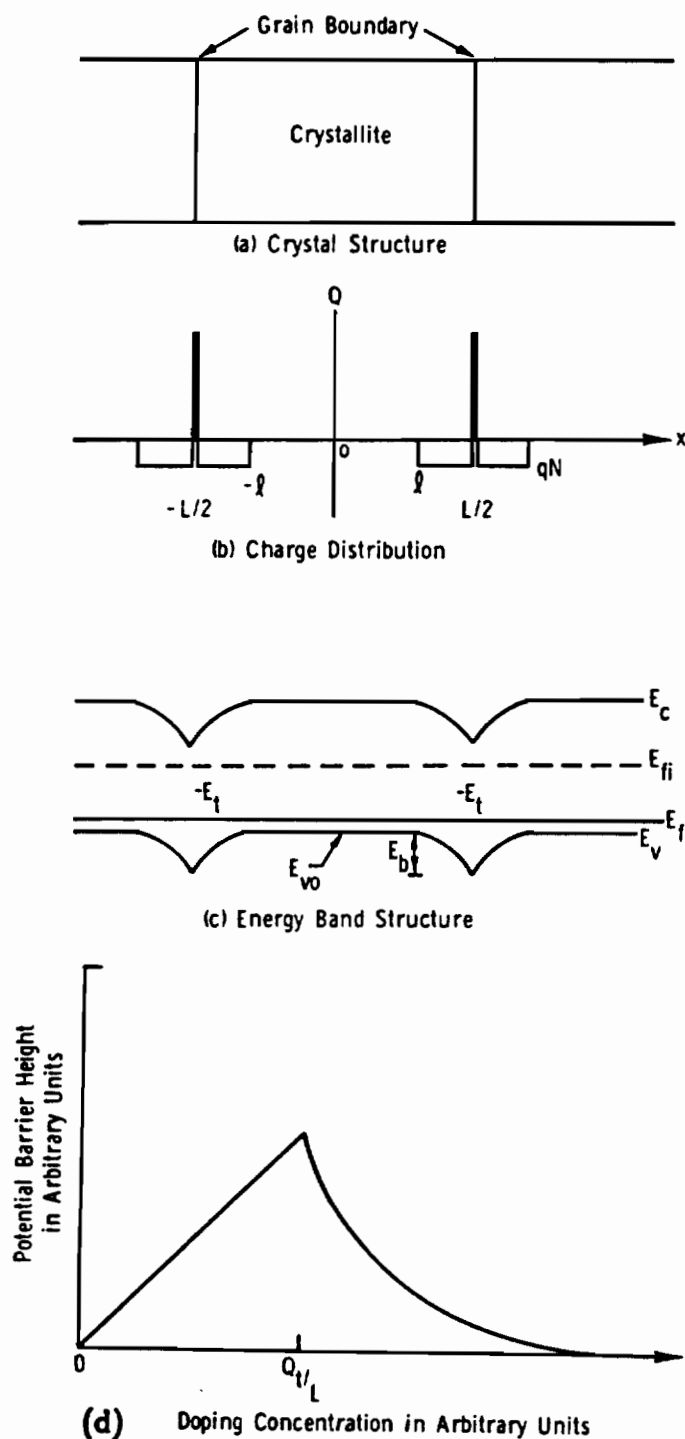
Fig. 2.1 Schematic showing (a) the crystal structure of polysilicon films, (b) charge distribution within the crystalline and the grain boundary, (c) the energy band structure and (d) the grain boundary barrier potential as a function of doping density[10].

solving Poisson's equation and taking the intrinsic Fermi level to be the reference point, the grain boundary barrier potential below N*, was expressed as :

$$V_B = qL^2N/8\epsilon_s, \text{ and } E_B = qV_B \qquad N < N^* \qquad (2.1)$$

where ϵ_s is the permittivity of silicon. The Fermi level was found by equating the number of carriers trapped to the total number of trapping states.

As the doping density N increases, the barrier potential increases linearly until the critical doping density N*, is reached. If the doping density is increased further, so that N is greater than the critical doping density N*, only a part of the grain will be depleted since now not all of the carriers are trapped. The potential barrier height in this case is given by :

$$V_B = qQ_T^2/8\epsilon_s N \qquad N > N^* \qquad (2.2)$$

where Q_T is the density of trapping states within the grain boundary. Thus, in this doping region, the barrier potential V_B will decrease rapidly as $1/N$.

Thermionic emission is the main mode of carrier transport in polysilicon in Seto's model. Thermionic emission results when carriers have a thermal energy, high enough to surmount the grain boundary potential barrier. To fit the experimental data, Seto used a model for the barrier resistivity that had two extra parameters: f, which was a simple scaling factor, and n, the ideality factor. The barrier resistivity is expressed, then, by

$$\rho_B = \frac{1}{f} \frac{(2\pi m^* KT)^{1/2}}{q^2 LP_c} \exp(\frac{qV_B}{nKT}) \qquad (2.3)$$

where P_a is the average carrier concentration and m^* is the effective mass of holes. This model while fitting the experimental results for small grain polysilicon, was not adequate for grain sizes larger than 600Å .

A different aspect of polysilicon behavior was brought forward by Mandurah et al. [11] This early model tried to explain the electrical properties of polysilicon with a dopant segregation effect. This model, however, does not explain the mobility minimum at the critical doping level shown in Fig. 2.2. An important result of this model is that it suggests dopants incorporated into polysilicon films exhibit a tendency to segregate, and for different dopants, the amount of this segregation is not the same. Dopant segregation leads to the apparent lowering of carrier concentration in polysilicon. With some of the dopant atoms trapped at the surface or at grain boundaries, fewer of them are available to dope the remaining bulk of the material. Research has shown that by annealing doped polysilicon samples at different temperatures, the effect of this segregation can be modified, and different carrier concentrations are measured[11]. Hall measurements were used by Mandurah et al. to study this phenomenon, because it can give the number of carriers with reasonable accuracy. Including this segregation will force us to make a correction in our mobility calculation by using an effective carrier concentration instead of the original implemented concentrations.

Segregation can best be discussed by first considering the thermodynamics involved when dopant atoms are introduced into polysilicon. Heat of segregation is defined as the enthalpy difference between an atom at the grain boundary and one in the bulk. Positive heat of segregation in single crystal silicon means that dopant will segregate to the "free silicon surface", In polysilicon grain boundaries are very
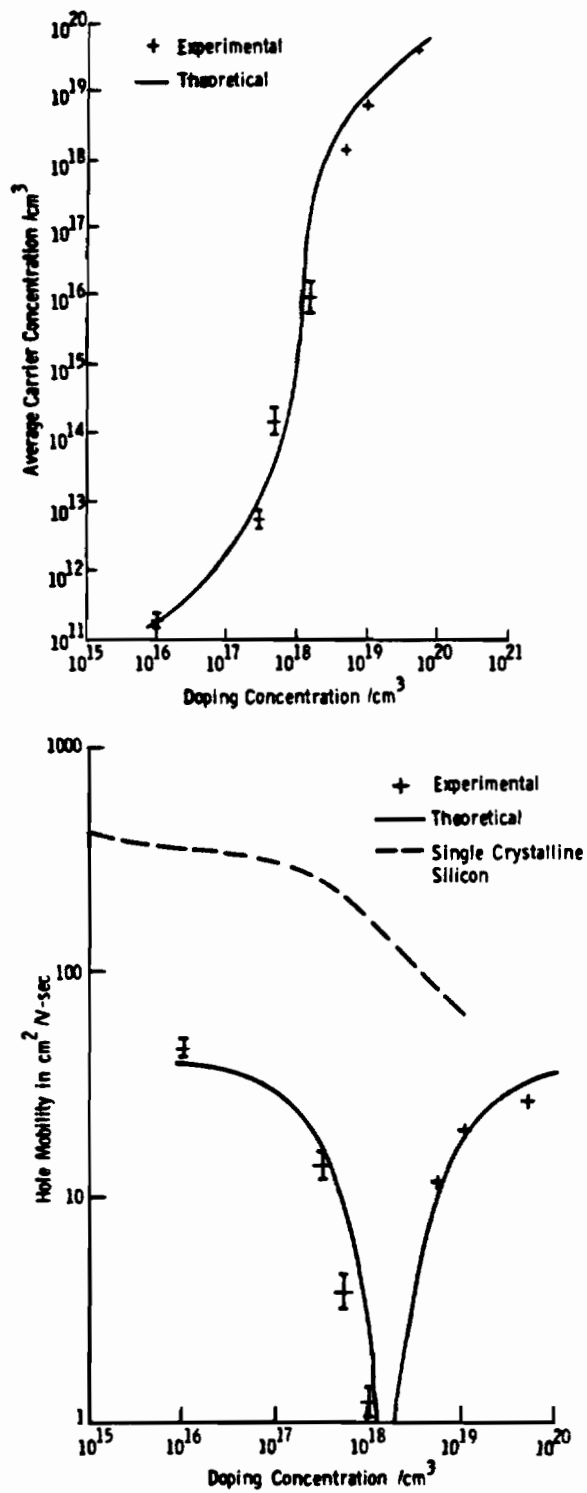
Fig. 2.2 Measured average carrier concentration and room temperature hole mobility vs. doping density [10]. Both data sets were obtained from Hall measurements.

similar to the free silicon surface because of dangling bond, defects, etc. So in polycrystalline silicon dopants will segregate to the grain boundaries also. The only noted difference between the free silicon surface and the grain boundaries is that the magnitude of the heat of segregation is higher for the surface.

Arsenic and phosphorus have lower heats of sublimation than does silicon and thus doping with them lowers the melting point. This means that these dopants have a positive heat of segregation and will segregate to the free silicon surface and grain boundaries. Boron, on the other hand has a higher heat of sublimation and increases the melting point of silicon. Therefore it has a negative heat of segregation which means that instead of segregation to the free silicon surface it will migrate away. An additional factor which may contribute slightly to the heat of segregation is the difference in size between the dopant atoms and the host silicon atoms. However, for the case of arsenic doping, this contribution should be negligible since silicon and arsenic in a tetrahedral configuration are nearly the same size.

As mentioned above, annealing experiments have demonstrated this dopant segregation in polysilicon. Mandurah et al. show in Fig. 2.3 a plot of carrier concentration as a function of annealing temperature for different doping levels. We can see that higher resistivity, and therefore lower effective concentration is achieved by annealing the doped sample st lower temperatures. At higher annealing temperatures the dopant atoms are more free to move, and the effect of segregation is less noticeable. In Fig. 2.4 we can see that these changes in resistivity are reversible if the sample is annealed in a sequence of different temperatures.

We have included the effect of dopant segregation in our model of n-channel accumulation mode polysilicon MOSFETs. The segregation effects were calculated

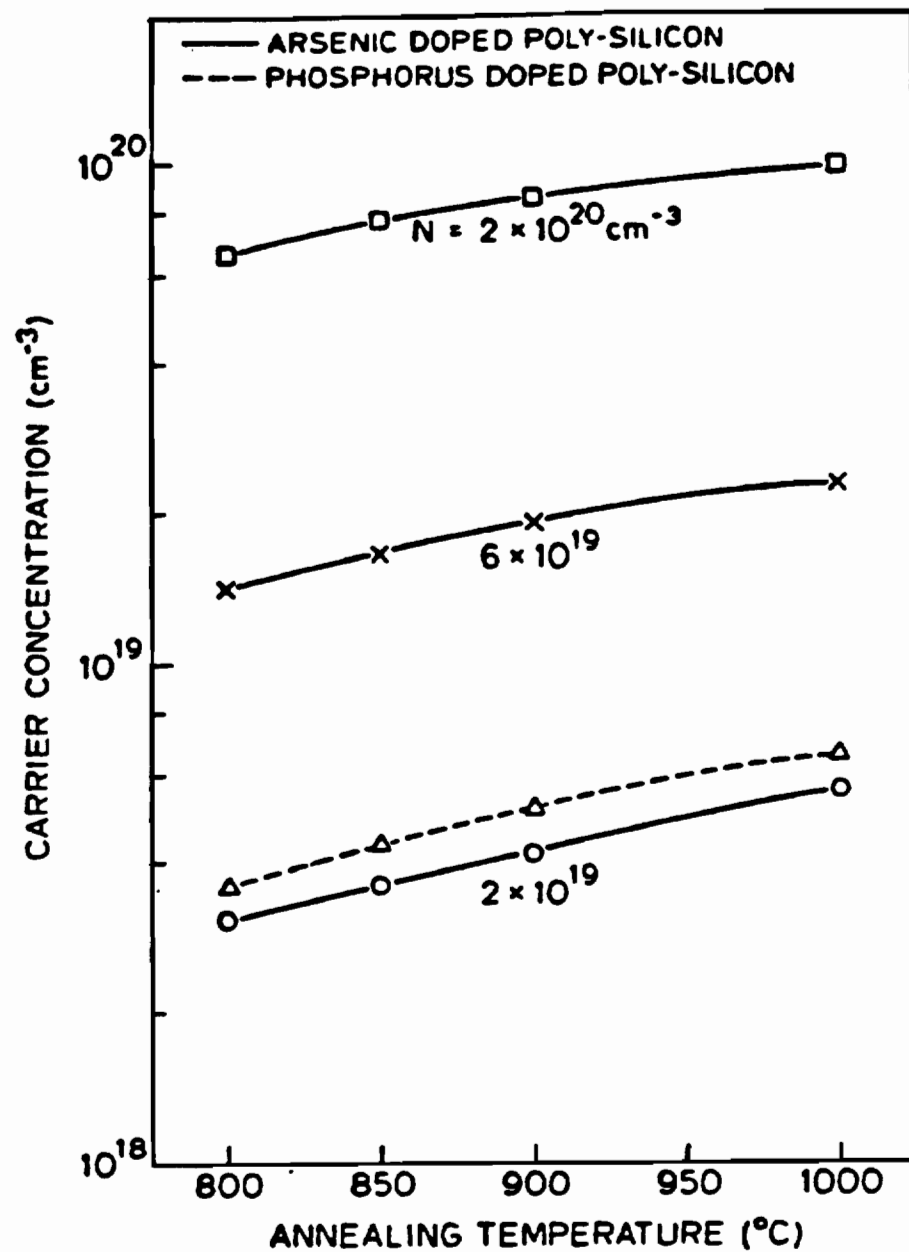Fig. 2.3 Carrier concentration in polysilicon films as a function of final annealing temperature for average carrier concentrations of 2×10^{19}, 6×10^{19}, and $2 \times 10^{20} cm^{-3}$ for arsenic and $2 \times 10^{19} cm^{-3}$ for phosphorus.[11]
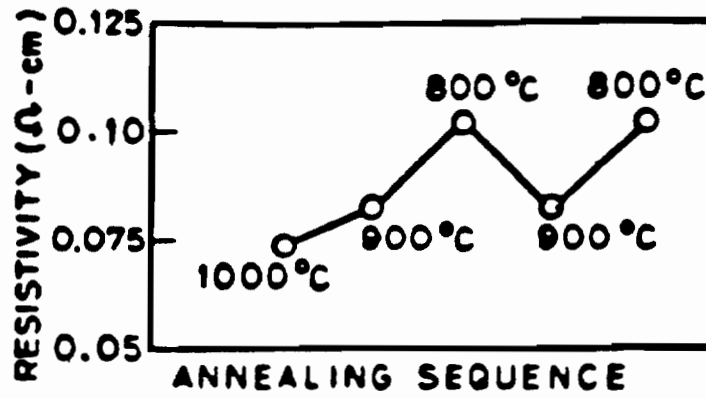
Fig. 2.4 Resistivity of the polycrystalline-silicon film implanted with 10^{15} arsenic ions/cm^2, after successive annealing at different temperatures. [11]

by modifying already existing models for surface or interface segregation in multicomponent systems and segregation of solute atoms to grain boundaries for metal systems. Several assumptions were made in the analysis. It was assumed that most of the inactive atoms segregate to the grain boundaries. Also, to simplify equations, an average grain length was used. The result for dopant segregation is shown in the following equation[11]:

$$\ln \frac{(N-N_G)}{N_G} = \frac{AQ_s}{N_{si}} + \frac{Q_0}{KT_A} \tag{2.4}$$

where Q_0 is the dopant heat of segregation, Q_s is the density of the segregation sites, N_{si} is the total number of silicon bulk and grain boundary sites, A is an entropy factor characteristic of the dopant, K is Boltzman's constant, T_A is annealing temperature, N is total dopant concentration and N_G is the average or effective dopant concentration remaining in the grain. In the model N_{si} and T_A are known, and A and Q_0 are parameters which are allowed to vary to fit the experimental data. Data is currently available only for high doping concentrations, therefore, extrapolation was used to find the segregation at the lower dopant concentration. The two parameters that depend on dopant concentration are A and Q_0 ,but Q_0 is only a weak function of concentration and it usually remains close to 10 kcal/mol. By plotting $\dfrac{AQ_s}{N_{si}}$ against the log of concentration we can see that it changes linearly with the log of concentration, therefore extrapolation will cause only small changes in that factor. And as mentioned above, annealing temperature must be included in the model because for higher annealing temperatures, the vibrational entropy is higher and thus segregation tends to decrease.

Lu et al. [12] extended Seto's model by considering a comprehensive charge neutrality. The voltage drops on both the barrier V_{ba} and the crystalline bulk V_{ca} respectively. Lu's model postulates a phonon-assisted scattering potential which is added on top of the grain boundary barrier potential qV_B. This is done to suppress the over-estimation of current and also to account for the temperature coefficient of resistance. By modeling the grain boundary as a semiconductor to semiconductor junction Lu et al. expressed the current density J, as

$$J = 2qP\left(\frac{KT}{2\pi m^*}\right)^{1/2} exp\left(\frac{-qV_B}{KT}\right) sinh\left(\frac{qV_{ba}}{2KT}\right) \tag{2.5}$$

and the resistivity

$$\rho = \rho_c\left(1 - \frac{2W}{L}\right) + \rho_b\left(\frac{2W}{L}\right) \tag{2.6}$$

where

$$\rho_c = \frac{V_{ca}}{J(L-2W)} \tag{2.7}$$

and

$$\rho_b = \frac{V_{ba}}{J(2W)} \tag{2.8}$$

In this model, ρ is polysilicon resistivity, ρ_c is crystalline bulk resistivity, ρ_b is barrier resistivity, and W is width of the depletion region. In Lu's model carrier transport in the neutral region is limited by lattice and impurity scattering, as in the single crystalline case. In the depleted region carriers can move via thermionic emission or field emission (tunneling). Note that this model does not have Seto's

ideality factor n, but it still has a scaling factor, which indicates that thermionic emission overestimates the current, in this case by as much as a factor of 20. Even Lu's improved version of the Seto model agrees with experimental results only for relatively small grain sizes.

To solve the problem of overestimation of current and to eliminate the f-factor, Lu et al. [13] and Mandurah et al. [14] suggested that there is a scattering potential, χ , in addition to the barrier potential due to the depletion region, V_B. The nature of the grain boundary has been described[14] as between that of a completely ordered single crystalline and that of a highly disordered amorphous material. The optical energy gap of amorphous silicon has been measured to be 1.5-1.6 eV, due to the high concentration of broken bonds, thus, it could be considered to be a wide-gap intrinsic semiconductor with a heterojunction formed at the interface between the crystalline region and the grain boundary. In order to simulate the phonon scattering in the grain boundary, Lu et al. treated both χ and the thickness of the grain boundary δ as parameters that varied with temperature. The band diagram corresponding to this model is shown in Fig. 2.5. This temperature dependence of both δ and χ, however, has been questioned by other researchers[15].

Another attempt to eliminate the over-estimation of current was made by Wu et al. [16] They used Rutherford scattering of charge carriers from a two dimensional array of fixed charge centers. They suggested that the coulombic scattering is much more important than phonon scattering at room temperature. The attenuation factor resulting from this model, however, still was not sufficient to explain the size of the f-factor reported earlier.
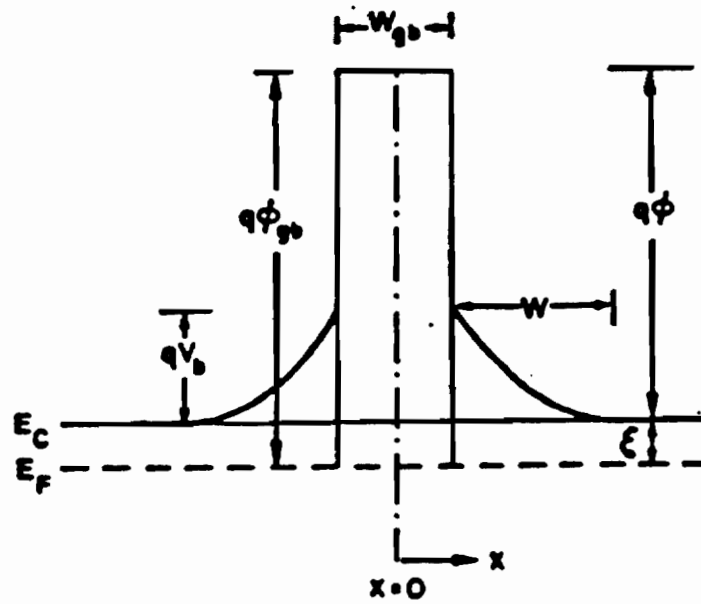
Fig. 2.5 Energy band diagram near a grain boundary under zero applied voltage.
[14]

2.2. ~~Previous~~ Models

There are two schools of thought explaining the carrier transport in polysilicon. One is the thermionic emission approach discussed earlier, and the other, discussed here, considers drift and diffusion to be the methods by which carriers are transported in the material. One formulation of the drift and diffusion theory is by Wu et al. [17] In this formulation the conductive nature of grain boundaries is not taken into consideration and drift and diffusion are taken to be the transport mechanism for the majority carriers through the crystalline regions only. Wu et al. describes transport of carriers through the grain boundary by using quantum mechanical tunneling. The energy band diagram used in this model is shown in Fig. 2.6. Current across the grain boundary is described as being proportional to the mobile carrier densities and hence is proportional to the difference of the quasi-Fermi levels on both sides of the grain boundary. In this mode it is not clear where this non zero value of current across the grain boundary comes from, if the voltage drop across the grain boundary is neglected.

A more complete model which does include grain boundary conductivity, was formulated by Kim et al. [15] This model is the one used to calculate the mobility of polycrystalline silicon for this thesis. In this model polycrystalline silicon is a distributed resistive system where the grain boundary is taken to be a highly resistive, but conducting medium. As mentioned above, current is due to drift and diffusion of carriers through this medium.

To explain this model and understand the charge transport through the grain boundary we first must consider the conduction channels existing in amorphous
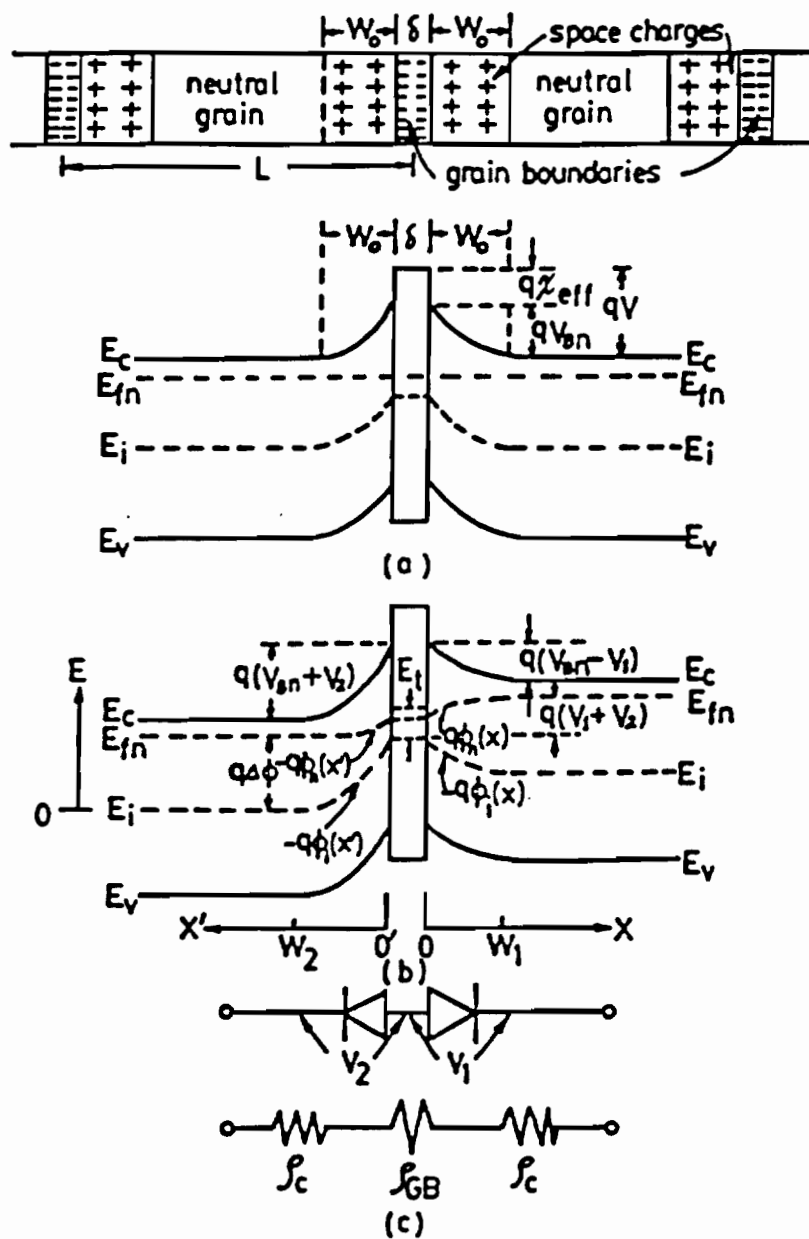
Fig. 2.6 (a) One dimensional grain structure, (b) the energy band diagram of a n-type polycrystalline grain at thermal equilibrium, (c) energy band diagram of a n-type polycrystalline grain at nonequilibrium, (d) equivalent circuits of a polycrystalline grain. [17]

semiconductor materials. The energy band diagram describing these conduction processes can then be combined with that for crystalline silicon to form a base for explaining conduction in polysilicon. In amorphous semiconductor material, electrical conduction occurs through three channels. The effect of each of these processes on the carrier mobility can be summerized as follows: 1) Extended states mobility; carriers in the extended state, beyond the mobility shoulder, move via diffusive or Brownian motion. 2) Hopping mobility; localized charge carriers in the band tails can be transported via phonon assisted - thermally activated - hopping. 3) Tunneling mobility; carriers localized in the defect states near mid-gap can move between states via phonon assisted tunneling. The energy band diagram associated with this conduction model was postulated by Mott et al. [18]

In this formulation, the trapping model is also used to describe the effect of the defect states near the mid-gap with a trap density $Q_T(cm^2)$ and a trapping level E_T. At the interface between crystalline and amorphous semiconductors, a heterojunction is formed, making the energy band diagram of polysilicon consist of both crystalline and amorphous semiconductors as shown [15] in Fig. 2.7. The current density is then expressed as :

$$J = q\mu_{gb}P_{gb}(V_{gb}/\delta)$$

(2.9)

or

$$J = qP(-L/2)\mu(V_a/L)$$
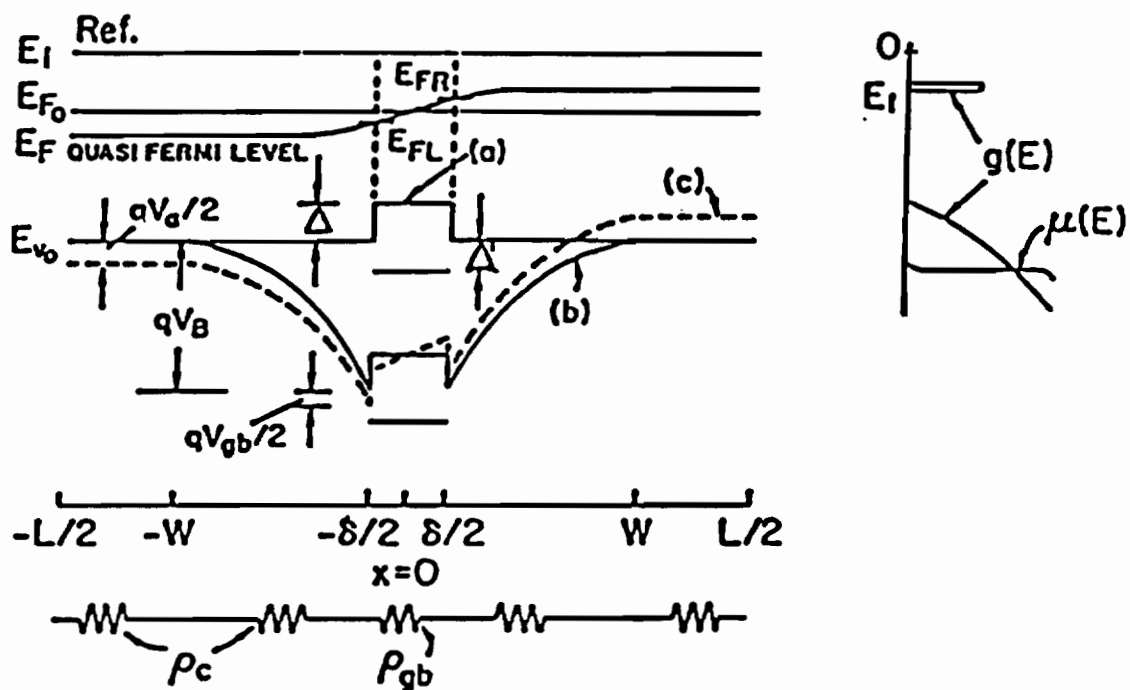
(2.10)

Fig. 2.7 Energy band diagram of a unit cell in polysilicon under (a) undoped, (b) doped, and (c) doped and biased conditions. [15]

where V_a is the applied voltage across the grain, V_{gb} is the portion of V_a that drops across the grain boundary, μ_{gb} is the effective mobility and P_{gb} is the total hole concentration within the boundary. Also,

$$\mu = \mu_c / [F_c^{(0)} + F_{gb}^{(0)}] \qquad (2.11)$$

$$P(-L/2) = n_i \exp - [E_F / KT] \qquad (2.12)$$

where μ_c is the single crystalline mobility, and F_c and F_{gb} are different parameters to be determined. The detailed algebraic expressions are given by Kim et al. [15] And finally the resistivity is in the form,

$$\rho = [F_c^{(0)} + F_{gb}^{(0)}] / \mu_c P(-L/2) \qquad (2.13)$$

This model model agrees with the experimental data and is free of fitting parameters. A more detailed discussion of this conduction model is given elsewhere[15].

CHAPTER 3

MOSFETS FABRICATED IN POLYCRYSTALLINE SILICON FILMS

There are essentially two routes by which MOSFETs can be fabricated in polysilicon. One is where the film is recrystallized prior to device fabrication. The other alternative is to fabricate MOSFETs in as-deposited films in conjunction with grain boundary hydrogen passivation. Each approach has strengths and weaknesses, and will be discussed in the following subsections.

3.1. Recrystallized Polysilicon Films

Initial problems with low carrier mobility and high threshold voltages in MOSFETs fabricated in polysilicon films directed research efforts toward recrystallizing the films. This is done to achieve device quality crystalline substrate material, since the grain boundaries which are the cause for some of the problems have been mostly removed. The recrystallized films have much larger grain size than the as-deposited films.

Several methods have been used to recrystallize polysilicon. One of the methods is laser annealing of the substrate. A CW-Argon ion laser having 11-14 W power was used by Kamins et al. [19] to scan over the polysilicon film causing it to recrystallize. Comparison of the results from recrystallized polysilicon MOSFET and the equivalent as-deposited device showed considerable improvement made by recrystallization. Dynamic RAM cells made using a similar laser-recrystallization

method showed dramatic improvement as well. These recrystallized dynamic RAM cells, fabricated by Jolly et al. [20] had almost double the storage capacity, increased storage time by completely isolating the storage region, and reduced soft error problems due to collection of charges injected into the substrate or by alpha particles. Three-dimensional folded dynamic RAM has also been fabricated in recrystallized polysilicon by Sturm et al. [21] They reported even longer storage times than Jolly et al. [20]

In order to achieve a specific crystal orientation Lam et al. [22] performed a laser enhanced lateral seeding of the polysilicon film. Single crystal silicon on oxide with { 100 } orientation was achieved by using a modified LOCOS (local oxidation of silicon) process. By melting polysilicon on a silicon wafer with the desired orientation and slowly scanning away the beam, molten silicon crystallizes epitaxially, converting the polysilicon on silicon into a single crystal epitaxial layer. Further, when the molten zone is moved into the polysilicon on an oxide region, the molten silicon recrystallizes, using the epitaxial layer as the seed.

Electron-beams have also been used for the purpose of recrystallization. Kamins et al. [23] used an electron-beam generated by a tungsten filament source, similar to that used in scanning electron microscopes, focused by a magnetic lens. An electrostatic octupole deflection system directly above the sample scanned the beam in one direction. The motion in the other direction was done mechanically. The quality of substrate achieved using this method of heating was very similar to the results of laser-annealing method. The potential for good control of an electron-beam and the lack of need for excessive substrate heating, make this technique preferable to some others.

Another recrystallization technique used for zone melting of polysilicon films has been achieved by Maby et al. [24] This technique employs a moving graphite strip heater that passes slowly over the substrate. In this technique a 1 μm thick oxide layer is thermally grown on both sides of the wafer, to protect the wafer from the graphite heater on the bottom. Then a 0.5μm polysilicon film was deposited on 1μm thick SiO_2 and capped with 2μm of SiO_2, and 500Å Si_3N_4 layer. The single crystals achieved using this method were about (2mm x 1cm) but within these large crystals there are smaller regions of about 25$\mu m \times 1 mm$ dimensions.

Arc lamp zone melting has also been used for the purpose of recrystallization[25]. This is done by using a high pressure mercury arc lamp which is focused into a narrow ribbon shaped beam by an elliptical reflector. The focused light creates a molten zone in the thin film, which is slowly scanned across the material. The sample is preheated on a graphite heater to $1000 - 1200°C$. The samples were 0.6μ LPCVD silicon films deposited on a thermally oxidized single crystalline wafer and were encapsulated. Grain sizes as large as .5 to 1 mm were achieved using this technique.

The main advantage of using recrystallized polysilicon films, as mentioned earlier, is that achievement of device quality material for the substrate improves the performance of the device and makes them more reliable. There are also problems associated with this approach, however. Fabrication of devices becomes more costly, the processing technique becomes more complicated, and thermal stresses are placed on the underlying substrate. Also increased throughput time further degrades the applicability of recrystallization. In addition to these problems, the production yield is low, and must be improved if the process is to be cost-effective.

Unfortunately the recrystallization techniques described earlier bring about the growth of large grain polysilicon films instead of single crystalline silicon films. Therefore some grain boundaries can be left in the active region of devices. These few boundaries will lower the performance of some of the devices in the same die, leading to a non-uniformity problem as well.

3.2. As deposited small-grain LPCVD polycrystalline silicon films

Fabrication of MOSFETs in as-deposited small-grain thin film polysilicon offers important technological advantages over devices fabricated in recrystallized films. Since the step-height associated with the addition of a layer of film to the process is small, the process topology is not drastically affected. Unlike the recrystallization methods discussed earlier, this method does not subject the amorphous substrate or the crystalline wafer to thermal stress, hence the devices built in the lower layers are left uneffected. The performance of polysilicon MOSFETs is a function of the number of grains existing between the source and the drain. Therefore fluctuations in the number of grains lead to a spread of device performance over the wafer. The small grain size ensures a large number of grains along the channel, so the percentage change in the number of grains is minimal. This will result in more uniform device performance over the same die. The growth of small-grain polysilicon films is well established in silicon processing and if MOS-FETs with high ON/OFF current ratio can be fabricated, a simple 3-D manufacturing process with better yield and lower cost than the recrystallization method can result.

The presence of the grain boundary states has a dramatic effect on the electrical properties of polysilicon. Reducing these states would improve the performance of the devices fabricated in as-deposited polysilicon. One well established technique is passivation of the grain boundaries by atomic hydrogen[26].

The origin of the grain boundary barrier potential has been discussed earlier. When passivating, atomic hydrogen diffuses along the grain boundary and ties up with some of the uncompensated "dangling" bonds. This results in a smaller number of grain boundary states and a lower grain boundary barrier potential. This mechanism is best explained with help of the Fig 3.1.

Another beneficial effect of the grain boundary passivation is the lowering of the leakage current of MOSFETs. One of the components of the leakage current[27] is generative current. Defects at the grain boundary act as possible electron hole pair (EHP) generation centers. Thus reducing these defect sites by grain boundary passivation results in a dramatic reduction in the leakage current.

Substantial success has been achieved with regard to fabrication of MOSFETs in as deposited thin film of fine-grain polysilicon. In addition the simplest and the most cost effective strategy to acquire an entry level 3-D capability would be to develop a process that requires no non-standard materials and tools. Small-grain LPCVD polysilicon is a well established material in silicon processing. Therefore this implies that the first adaptation of a three-dimensional integration maybe stacked CMOS VLSI memory chips in which one of the transistors is fabricated in a layer of LPCVD polysilicon on silicon dioxide[28, 29]. To improve the performance of polysilicon MOSFETs, as described above, grain boundary passivation via hydrogenization is done. In order to be able to design circuits using polysilicon
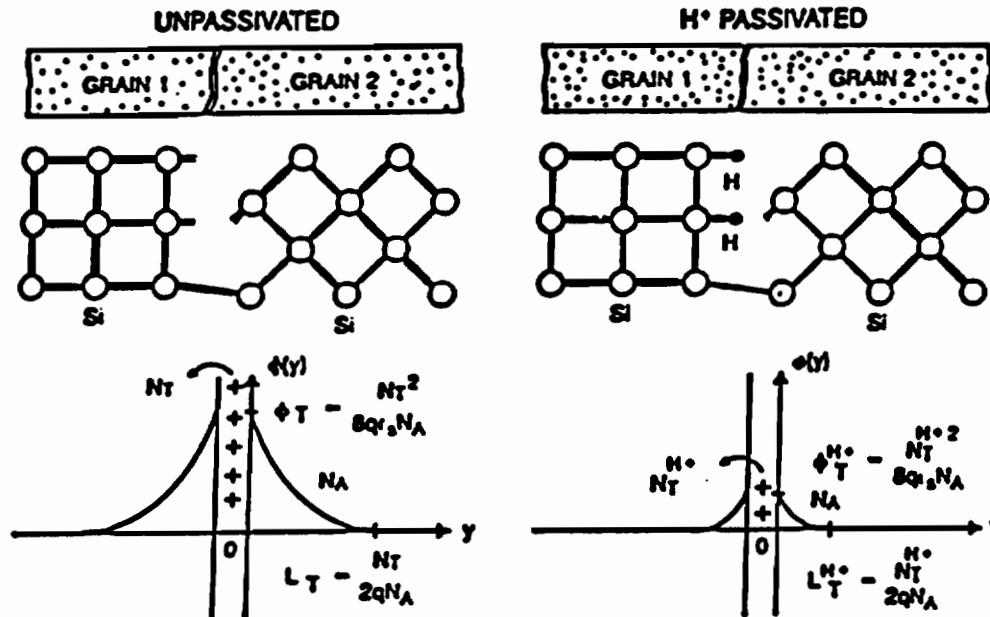
Fig. 3.1 Schematic showing the grain boundary structure between two neighboring polysilicon grains and the potential barrier due to the grain boundary. After the hydrogen passivation, atomic hydrogen ties up with most of the dangling bonds, resulting in a lower potential barrier.[34]

MOSFETs an electrical model is needed that can adequately explain the experimental I-V characteristics of the device with a fair degree of accuracy. High-voltage MOSFETs have also been fabricated[30] in polysilicon with a breakdown voltage of about 200 V. Efforts have been made to develop an analytical model that can predict the behavior of these devices. Some of these models are described in the following chapter.

CHAPTER 4

ELECTRICAL MODELS OF POLYSILICON MOSFETS

4.1. Previous Models

One of the earlier attempts toward the characterization of polysilicon MOS transistors was undertaken by Onga et al. [31] Measurements were performed on both N and P channel enhancement-type polysilicon MOSFETs. A U-shaped $I_D - V_G$ curve was observed as the gate was swept from accumulation to inversion. This high current in the accumulation region was qualitatively ascribed to junction breakdown around the drain region precipitated by the crystalline imperfections inherent in the as deposited polysilicon films. The primary intent of Onga's work was not toward the development of a comprehensive device model itself; it was rather directed toward a general qualitative understanding of the channel mobility as a function of the gate voltage and various other processing parameters. The carrier mobility discussed was a combination of space charge scattering mobility μ_{sc}, bulk mobility μ_{bulk}, dislocation scattering mobility μ_D and was given as,

$$\frac{1}{\mu} = \frac{1}{\mu_{bulk}} + \frac{1}{\mu_D} + \frac{1}{\mu_{sc}} \tag{4.1}$$

Comparisons were made with the SOS film properties and device behavior.

An attempt to model the characteristics of polysilicon devices in the leakage regime was made by Fossum et al. [32] In this model, leakage current of accumula-

tion mode devices was assumed to originate from field emission from grain boundary traps at the drain junction. For positive gate voltages the channel region is left completely depleted. A negative drain voltage now further enhances and increases the electric field near the drain, consequently it was suggested that this emission occurred under the gate near the drain gate oxide interface. The shortcoming of the model is the various assumptions that have gone into it. Specifically, the use of an abrupt depletion approximation in a polysilicon junction system, and the use of the WKB approximation in calculating tunneling time constants in the presence of a large number of acceptor/donor trap states are questionable. In addition, fitting parameters α and β, so called "field fringing factors" were used. The model however is insightful.

In more recent work done by the same group[33] subthreshold behavior of thin film polysilicon MOSFETs has been characterized. This work considers both the effect of the grain boundaries and the charge coupling between the front and back gate. The results are in terms of the front and back gate voltages, the device parameters, and the grain boundary properties. This work is based on the following: it is assumed that the grain boundaries in the small-grain polysilicon can be analyzed as traps uniformly distributed in silicon. A numerical solution of the 1-dimensional Poisson's equation is used with mixed boundary conditions at the front and back interfaces, which accounts for charges trapped at the grain boundaries. The description of the subthreshold drain current, which is assumed to be predominantly diffusion for drain voltages higher than $\dfrac{KT}{q}$, and the characterization of the threshold voltage are obtained from the derived dependence of the channel charge density on the gate voltage. The analysis points out that the charge

coupling effect diminishes as either the grain boundary trap density, the thickness of the film, or the film doping density increases. Here, the drain current is governed by only the front surface conduction and the back surface is assumed to be either depleted or inverted. The expression for the drain current is given by,

$$I_D \approx \frac{Z}{L} \mu_{pf} \frac{kT}{q} Q'_{pf} \tag{4.2}$$

where Z is the channel width, L is channel length, μ_{pf} is hole mobility, and Q'_{pf} is the excess hole accumulation layer. Although, this model agrees fairly well with the experimental results, it is based on a numerical solution rather than a simple analytical expression.

A device model for circuit simulation was suggested by Malhi et al. [34] This model used simple existing MOSFET models plus the effect of charge coupling between the front and back gates, which can cause the threshold voltage of one gate to depend on the bias on the other gate. In the linear region the drain current expression is given as,

$$I_D = \frac{W}{L} \mu C_{ox1} [(V_G - V_T)V_D - (1 + \frac{C_{bb}}{C_{ox1}})\frac{V_D^2}{2}] \tag{4.3}$$

and the drain current in the saturation region is given by,

$$I_D = \frac{W}{2L} \mu C_{ox1} \left[\frac{(V_G - V_T)^2}{(1 + \frac{C_{bb}}{C_{ox1}})} \right] \tag{4.4}$$

In these expressions, V_T is the threshold voltage, C_{ox1} is the oxide capacitance per

unit area, C_b is polysilicon film body depletion capacitance per unit area and C_{bb} is the series combination of C_b and C_{ox1}. Since these expressions resemble the expressions for bulk transistors, a SPICE model was generated to see how close a fit could be obtained. Because the mobility of the channel tends to increase when a voltage is applied, the following expression was used to fit this changing mobility:

$$\mu = \frac{\mu_0}{1 + \theta(V_G - V_T)}.$$ (4.5)

In bulk transistors θ is a positive number because mobility decreases with higher vertical fields, but in polysilicon MOSFETs it is a negative number.

The subthreshold current is said to be strongly determined by the trap energy level and the fast interface state density at the front gate and is expressed as

$$I_D = \beta_s exp[N_S \frac{q}{KT}(V_G + \phi_S - 2\phi_F)][1 - exp(-N_S \frac{qV_D}{KT})].$$ (4.6)

The values for all the parameters used in the above expression are given by Malhi et al. [34] The drawback of this model is that it uses curve fitting instead of strong physical expressions that use polysilicon parameters and properties.

4.2. Present Theory

A comprehensive analytical model of accumulation mode MOSFETs in polysilicon thin films has been suggested by Ahmed et al. [35] This model has been used here to calculate the I-V characteristics of a normally ON, N-channel, polysilicon MOSFET. A qualitative explanation of this model is given here. The device

under consideration here, has $n^+ - n - n^+$ source, channel and drain as shown in Fig. 4.1. This model is based on the following assumptions and simplifications. i) Polycrystalline silicon films consist of columnar rectangular grains of uniform size. ii) The size of these grains depends on a number of parameters such as annealing temperature, annealing time, doping density, thickness of the film etc. Nevertheless it has been shown that the grain size approaches the thickness of the deposited film. iii) The grain boundary has a thickness δ ranging between 10-20 Å and contains uniform trap density Q_T/δ. iv) Electrical conduction takes place via the model of Kim[15] et al. described earlier. v) The grain boundaries are considered to be perpendicular to the gate electrode. vi) The interface states Q_{sf} are represented as a fixed sheet of charge just below the gate oxide. vii) The abrupt depletion approximation is used to calculate the potential within the space charge regions. viii) By averaging the variations of surface potential ϕ along the y-direction in Fig. 4.2, the 2-D Poisson's equation is reduced to a 1-D equation. ix) The concept of electrostatic shielding is introduced to correct for the underestimation of mobile carrier density from a y-independent ϕ. x) The channel mobility is only a fraction of the bulk mobility because of the scattering due to the interface states.

In the present model, application of a gate voltage will cause surface band bending to occur. Here we examine the relationship of an applied gate voltage to band bending at the surface of the channel, under the gate oxide. To simplify the explanation consider a unit cell that consists of a grain boundary in the center and crystalline grain regions, one on each side of the grain boundary. Perpendicular to this grain boundary is the oxide layer separating the channel from the gate. At the interface are the usual interface states. To begin with, we assume that the channel
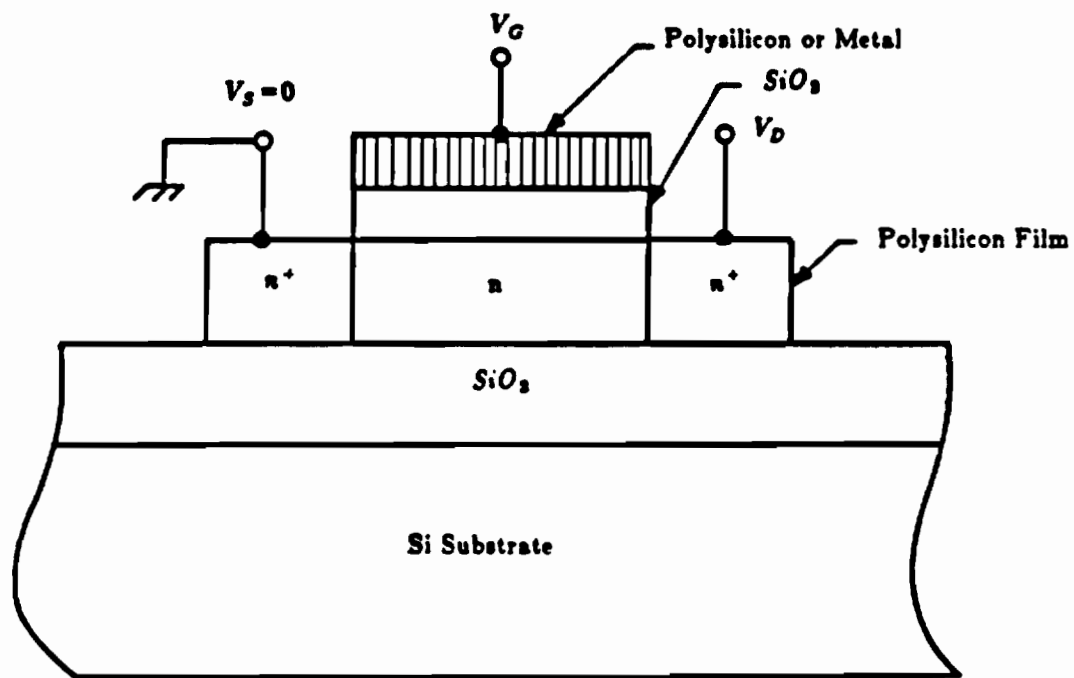
Fig. 4.1 Schematic showing the cross section of the device.[32]

doping density N is greater than the critical doping N*; hence the grain will be only partially depleted. This condition forces us to consider both the neutral and the depleted regions as shown in Fig. 4.2. With no voltage applied to the gate and temporarily neglecting the interface states, the grain is in equilibrium situation. Because of the charges trapped at the grain boundary, an electric field exists in the depletion region. The E-field lines start from the ionized dopants and terminate on the trapped charges at the grain boundary. If a positive voltage is applied to the gate, electrons will be injected into the grain. These electrons will be injected into both the neutral region at the center of the grain, which is at the edges of the unit cell defined above, and into the grain boundary. Here lies the first difference from the crystalline devices. Because of the symmetry at the center of the grain and most of the neutral region, the electric field lines will be in the x direction and they terminate in the bulk. In the depletion region, however, field lines start in the x direction and bend toward the grain boundary in the y direction to terminate at the grain boundary, because of the existence of the injected charges there. Fringing can take place at the edges of the depletion region.

Band bending is caused by the need to supply charges either to provide or to terminate electric field. Because there is a higher population of electrons at the center of the grain, (in the neutral region), the band bending $q\phi$ is smaller than in the depletion region which has a lower population of electrons. We can see from the above argument that the band bending $q\phi$ is inhomogeneous along y, i.e., ϕ is a function of both x and y.

To obtain an exact numerical solution a two dimensional Poisson's equation must be solved. It has been suggested[27] that this problem can be solved to a great
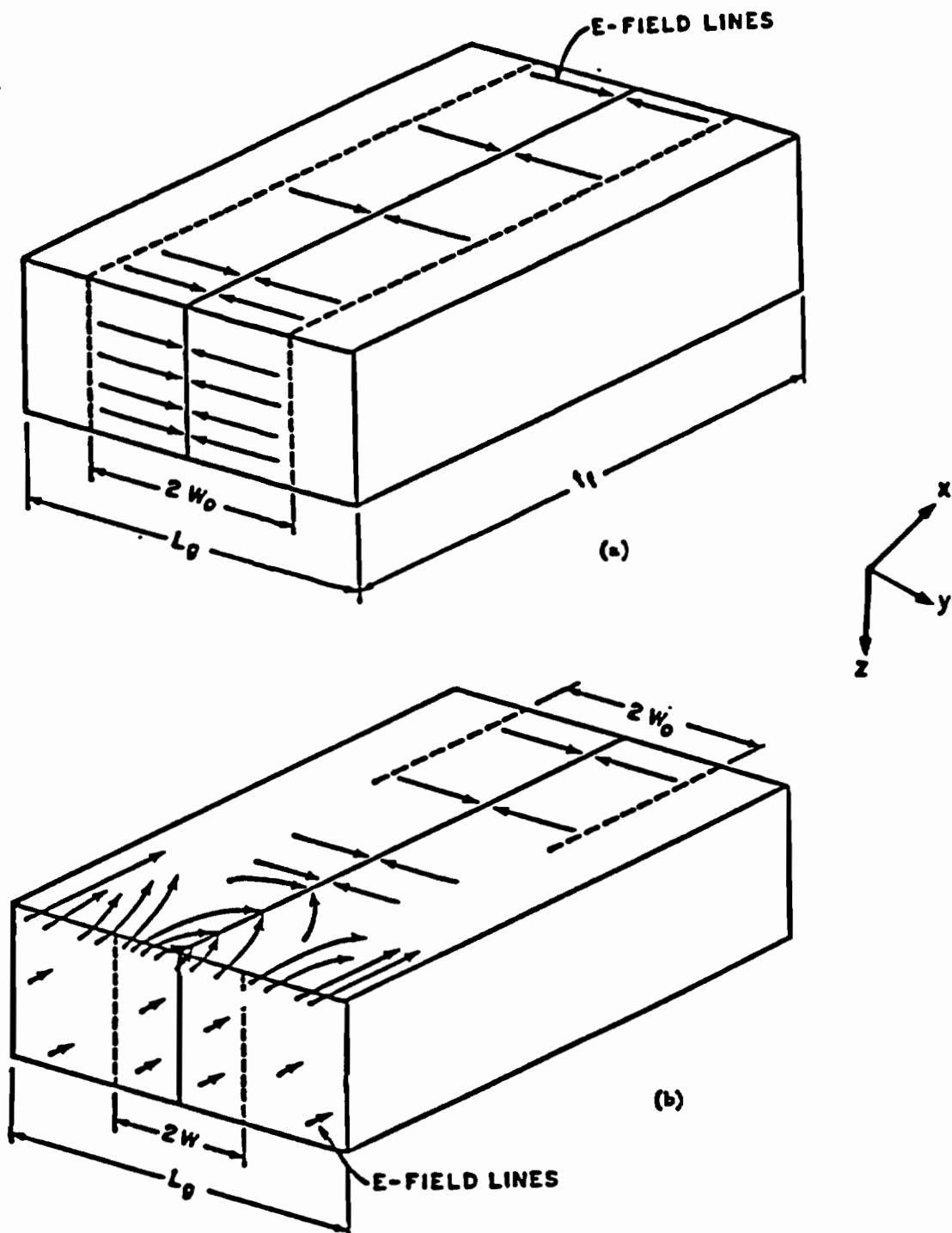
Fig. 4.2 Electric field lines, at the surface and in the bulk (a) at equilibrium and (b) with a positive gate voltage applied to the gate within a unit cell of length L_g.

degree of accuracy by introducing some physically reasonable assumptions. The variations of ϕ along y could be eliminated by performing an averaging in the y direction. The 2-dimensional Poisson equation then reduces to a 1-dimensional Poisson equation :

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{q}{\epsilon_o} \left\{ \bar{p} e^{-\beta \phi} - p_o - \bar{n} e^{\beta \phi} + n_o + \frac{Q_T}{L_g} [f(+) - f_o(+) - f(-) + f_o(-)] \right\}$$

(4.7)

where $\bar{p}$, $\bar{n}$ are the average carrier concentrations, f-factors represent the Fermi occupation factors for electron and hole traps, L_g is the average grain size, and β represents $\frac{q}{kT}$. Using this simplified Poisson's equation and integrating from the bulk to any surface potential ϕ, results the following expression:

$$E = -\frac{\partial \phi}{\partial x} = -\frac{\sqrt{2}}{L_D} \frac{kT}{q} F (1 + \frac{G}{F^2})^{1/2}$$

(4.8)

where L_D is the Debye length,

$$F^2 = e^{\beta \phi} - 1 - \frac{\bar{n}_o}{\bar{n}} \beta \phi + \frac{\bar{p}}{\bar{n}} (e^{-\beta \phi} - 1 + \frac{\bar{p}_o}{\bar{p}} \beta \phi)$$

(4.9)

and

$$G = \frac{Q_T}{L_g \bar{n}} \left[\beta \phi \frac{(1-A)}{(1+A)} + \ln \left(\frac{2 + A e^{\beta \phi} + A^{-1} e^{-\beta \phi}}{2 + A + A^{-1}} \right) \right]$$

(4.10)

with

$$A = e^{(E_F - E_T - qV_B)/kT}. \tag{4.11}$$

The average carrier concentration $\bar{n}$ is a function of depletion depth and the grain boundary barrier potential and is expressed as

$$\bar{n} = n\left(\frac{L_g}{2}\right)\left[\left(1 - \frac{2W}{L_g}\right) + \left(\frac{\pi}{-\beta V_B}\right)^{1/2} \frac{W}{L_g} erf\left(-\beta V_B\right)^{1/2}\right]. \tag{4.12}$$

Here erf represents the error function, W is the width of the depletion region and $n\left(\frac{L_g}{2}\right)$ is the equilibrium electron concentration at the grain center. Finally,

$$\bar{p} = \frac{n_i^2}{\bar{n}} \tag{4.13}$$

where n_i is the intrinsic carrier concentration.

A positive voltage applied at the gate of an N-channel polysilicon MOSFET causes injection of mobile carriers - in this case electrons - into the region at the surface of the channel. As mentioned before, the distribution of these carriers along the y-direction is not uniform and the barrier potential is reduced as a result of this injection of carriers. This reduction is caused by electrostatic shielding of the uncompensated ionized dopants by injected carriers. The shielding effect causes the equilibrium depletion width W_o to decrease to a new value W. An expression for this new depletion depth has been calculated by considering charge neutrality over a unit volume bounded by the length of the unit cell L_g, unit width of the channel and the channel thickness t_f . The expression for this new depletion depth is given as

$$N(W_o - W) = n\left(\frac{L_g}{2}\right)\left(\frac{L_g}{2} - W_o + t\right)\sqrt{2}L_D\, e^{-\beta\phi_s/2}(e^{\beta\phi_s} - 1). \qquad (4.14)$$

In the above expression t is the tailing of excess carriers into the depletion depth and is given as $t = (2\epsilon_s/q\beta N)^{1/2}$, ϵ_s is the permittivity of silicon and ϕ_s is the surface potential. This new depletion depth is used to calculate the corresponding barrier potential by using the following expression,

$$V_B = qNW^2/2\epsilon_s \qquad (4.15)$$

Now these new values of the barrier potential and depletion depth can be used to find the average carrier concentration without the problem of underestimation due to the shrinking depletion depth. By using the equations 4.7-4.12 for any given surface potential ϕ_s, a corresponding surface electric field can be calculated.

The expression for the carrier mobility in polysilicon as shown in Eq. 2.11 is a composite quantity and is very dependent on the grain boundary barrier potential V_B. As discussed before, an applied gate voltage causes changes in V_B. These changes must be taken into account when calculating bulk polysilicon mobility.

Interface states are known to cause additional scattering of carriers. As a result of this scattering, the bulk mobility is reduced by a factor η , known as the surface scattering factor, therefore

$$\mu_{channel} = \eta\mu_{bulk} \qquad (4.16)$$

A positive voltage applied at the gate electrode of the N-channel MOSFET can be partitioned in the following way.

$$V_{GS} = \frac{\epsilon_s E_s}{C_{ox}} + V_{FB} + \phi_s \qquad (4.17)$$

here V_{FB} is the flat band voltage, expressed as,

$$V_{FB} = -\frac{Q_{sf}}{C_{ox}} + \Phi_{ms}. \qquad (4.18)$$

Here, Q_{sf} is the density of interface states , C_{ox} is the gate oxide capacitance and Φ_{ms} is the work function difference between the gate electrode and the substrate. In summary, for any given surface potential a surface electric field is evaluated using Eq. 4.7-4.15. The corresponding gate voltage is evaluated using Eq. 4.17.

4.2.1. I-V Relationship

The operation of a polysilicon MOSFET can be divided into three distinctive regions depending on the magnitude of the gate voltage V_{GS}. These regions are

1) Leakage, where $V_{GS} = 0$

2) Weak accumulation, where $V_{GS} < V_{DS} + V_{FB}$

3) Drive, where $V_{GS} > V_{DS} + V_{FB}$.

The gate and drain voltages are measured with respect to the source voltage, and are expressed as V_{GS} and V_{DS} respectively. We will now discuss these modes of operation in some detail.

4.2.1.1. Leakage Regime

Consider first a P-channel accumulation mode device. Because the flat band voltage is negative and the gate voltage sweep is negative, at zero gate voltage the top of the channel is depleted. The bottom interface charges also cause the bottom of the channel to deplete. Two cases must be considered here: one when the two depletion depths meet and the other when they do not meet. In the first case, the leakage current is caused by the generation of carriers in the depletion region that are swept across when a drain voltage is applied. In the second case there is an additional resistive current that leaks through the neutral region between the two depletion depths. This current is very similar to the current in JFETs. Now for N-channel devices, even at zero gate voltage the channel is already accumulated. This accumulation layer at the surface gives rise to other types of current which are assumed to be of greater magnitude than the resistive-generative leakage currents. So for this analysis of N-channel devices, leakage current is not important. A detailed analysis of the resistive-generative leakage current has been given by Ahmed et al. [27]

4.2.1.2. Weak Accumulation

The behavior of the drain current as a function of applied gate voltage in this operation regime is similar to the subthreshold conduction observed under weak inversion in MOSFETs fabricated in single crystal silicon. In this case, the source is grounded; therefore the source side of the channel is accumulated when a gate voltage is applied. The drain side of the channel is still depleted, however, because

$(V_{GS} - V_{FB} < V_{DS})$. This concentration gradient in the channel gives rise to a diffusive current. The current density is expressed as[36]

$$J = qD_n e^{\beta\phi_s(x)}(1 - e^{\beta V_D})$$ (4.19)

where D_n is the diffusion constant for electron. When J is integrated over the cross sectional area of current flow, taking into account the variations of ϕ_s with x, an expression for current is found in the form,

$$I_D = (\frac{kT}{q})\mu_{ch}\frac{Z}{L}q\bar{n}e^{\beta\phi_s}(1 - e^{\beta V_D})t_z$$ (4.20)

where, $t_z = \sqrt{2}L_D e^{\beta\phi_s/2}$.

This t_z represents the spatial extent over which the electric field at the surface decreases by $\frac{kT}{q}$.

4.2.1.3. Drive

There are some physical differences between accumulation-mode and inversion-mode devices. The accumulation-mode device turns ON once the flat band voltage is exceeded. While the channel is accumulated, in the absence of any drain voltage, no uncompensated dopants exist in the channel. Application of a drain voltage causes the majority carrier imref to split and the appearance of uncompensated dopants in the channel. This can be explained with the help of Fig. 4.3. As is shown in that figure, a voltage applied at the drain lifts the band edges and splits the majority carrier - electron - imref. In the region where the imref is
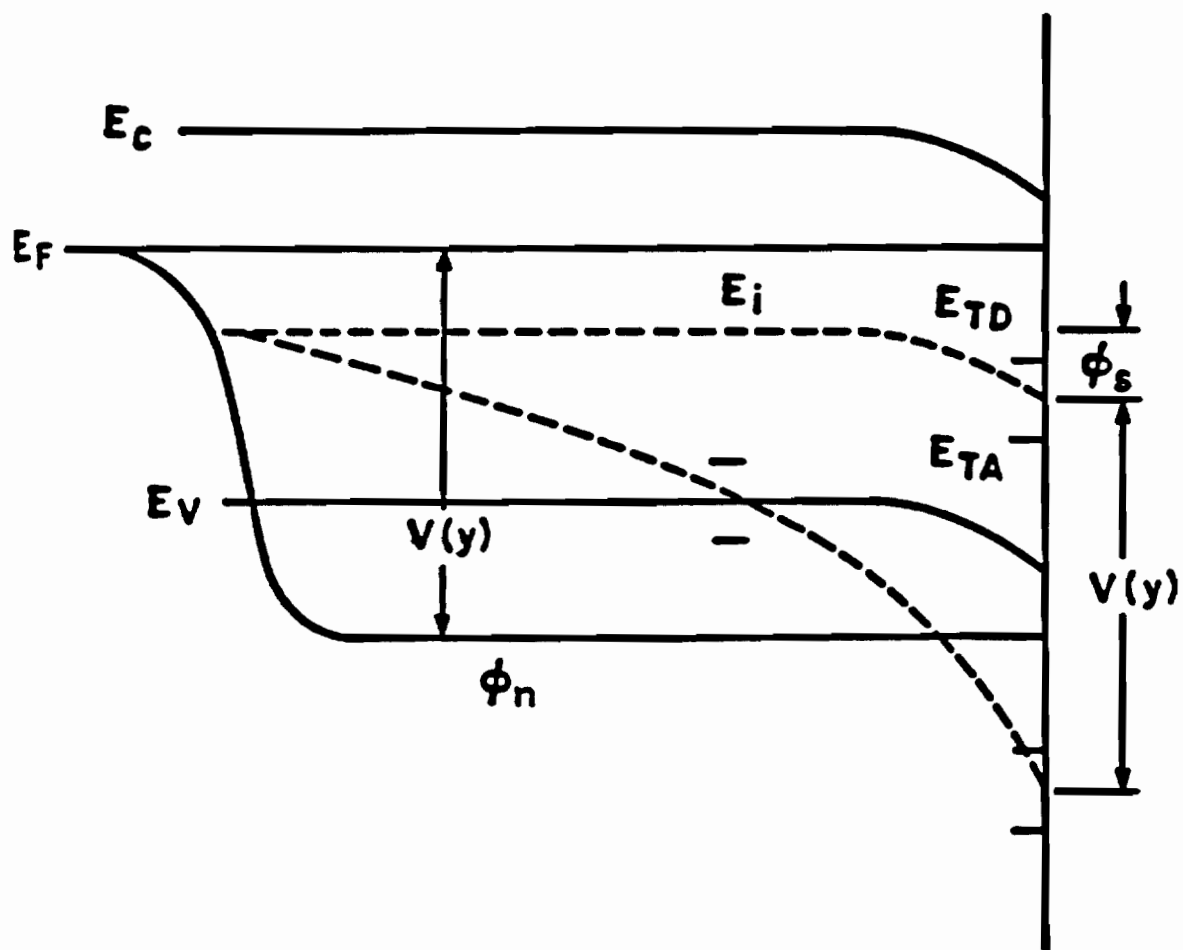
Fig. 4.3 Energy band diagram within the accumulated channel arising from the application of a drain voltage. [35]

below the intrinsic level, the channel depletes. The imref meets the Fermi level in the bulk with the splitting occurring in the depletion region. Because there is no current in the x-direction, the imref has appreciable slope only where there is only a negligible number of majority carriers. In the depletion region the splitting of the imref ensures that both the electron and hole traps are empty. Therefore the depletion depth can be calculated using the abrupt depletion approximation. By applying Gauss' law and charge conservation the electron density can be expressed as,

$$Q_n = - C_{oz}(V_{GS} - \phi_s - V(y) - V_{FB}) + \sqrt{2Nq\epsilon_s(V(y) + \phi_s)} \qquad (4.21)$$

where, V(y) is the channel voltage at any given y. Some of these charges are trapped within the grain boundary. In order to find the total number of mobile charges, one must subtract the number of the trapped charges from the total charge. The gate flux lines emanate from the grain boundary only within a few Debye lengths from the surface, therefore, we can express these trapped charges as $Q_{nt} = qQ_T \alpha L_D/L_g$, where α is the number of Debye length from the surface where the traps are full. The total mobile charge can now be expressed as

$$Q_{nm} = \sqrt{2Nq\epsilon_s(V(y) + \phi_s)} - C_{oz}(V_{GS} - \phi_s - V(y) - V_{FB}) + q\alpha \frac{L_D}{L_g} Q_T . EQ(4.22)$$

and the expression for the drain current becomes[37]

$$I_D = \frac{Z}{L}\mu C_{oz} \left\{ (V_{GS} - \phi_s - V_{FB} - \alpha \frac{L_D}{L_g} q \frac{Q_T}{C_{oz}}) V_D \right.$$
$$\left. - \frac{V_{DS}^2}{2} - \frac{2}{3}(\frac{2Nq\epsilon_s}{C_{oz}^2})^{1/2} [(V_{DS} - \phi_s)^{3/2} - \phi_s^{3/2}] \right\}$$

$$(4.23)$$

4.2.2. Theoretical Results

4.2.2.1. Mobility, Barrier Potential and Surface Potential

In this section we will study the effects of different average grain size L_g, trapping density $Q_T(cm^{-2})$, doping density $N(cm^{-3})$ and trapping level $E_T(eV)$ on the variations of surface potential ϕ_s, grain boundary barrier potential V_B and channel mobility μ due to the applied gate voltage. In this section "V" denotes $V_{GS} - V_{FB}$.

Using the Eqn. 4.7-4.18, we show the behavior of channel mobility, band bending and barrier potential when gate voltage is increased in Fig 4.4. We must note again that in this section the gate voltage is with respect to the flat band voltage. In this set of data the critical doping density $N^* = 1.58 \times 10^{17} cm^{-3}$. The channel doping density $N = 3 \times 10^{17}$ is above the critical doping density: $N > N^*$. This means that the channel is only partially depleted. Application of a gate voltage causes injection of carriers to the surface, hence the barrier potential starts to shrinks as soon as the gate voltage is applied. The dependence of channel mobility on the barrier potential has been discussed earlier. In Fig. 4.4 we can see that when the barrier potential is decreased to about a fourth of its original value (V=3.0-4.0 volts) the channel mobility starts to saturate. The surface band bending is similar to the single crystalline case. At voltages around 3.0-4.0 volts, the channel strongly accumulates and further increase of the gate voltage does not cause much additional band bending.
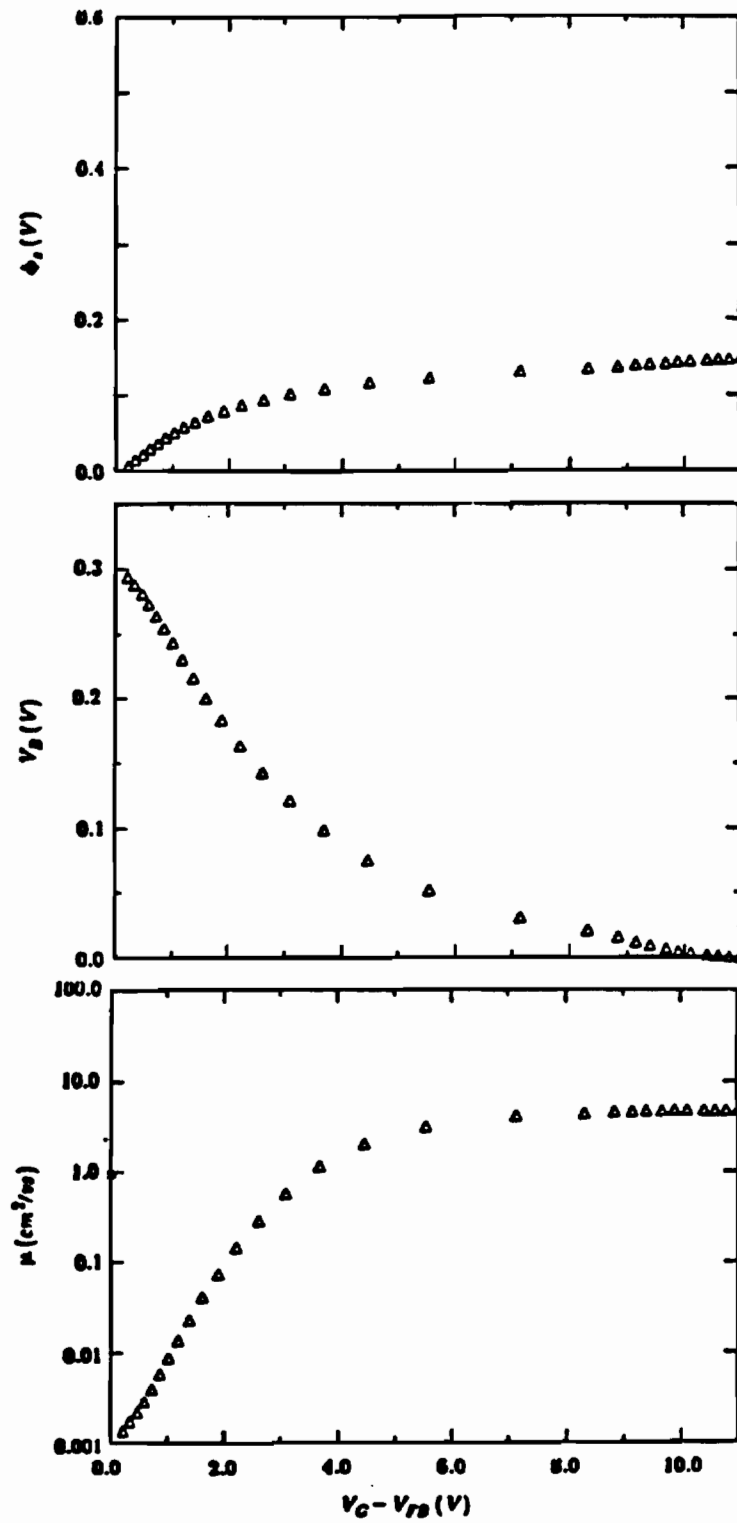
Fig. 4.4 Surface potential, grain boundary barrier potential and channel electron mobility as a function of $V_{GS} - V_{FB}$, for doping levels above N*.

The next case, shown in Fig. 4.5, is for the doping density less than the critical doping density: $N<N^*$. In this case the grain is completely depleted but the traps are not completely filled. The injected carriers, first will have to fill all the traps. As the gate voltage is increased to about 2 volts, the injected carriers are only getting trapped at the grain boundary and no significant change in the barrier potential is observed. At voltages larger than 2 volts we can see the barrier potential starts to decrease and approaches zero. Because the doping density is low, the band bending is more significant. Some of this band bending goes toward compensating the traps. As mentioned before, the mobility is a strong function of barrier potential. At flat band the barrier potential is not as large as in the previous case when the doping was above the critical doping, hence the mobility enhancement will not be as great as the previous case where $N>N^*$.

The variations of μ, V_B and ϕ_s as a function of V for films with different average grain size are shown in Fig. 4.6. The doping density, trap density and level are respectively $N=2\times10^{17}cm^{-3}$, $Q_T=2\times10^{12}cm^{-2}$ and $E_T=0.1eV$. The average grain sizes used here are $L_g=500, 1000$, and $1500\text{\AA}$, and the calculated critical doping densities are 3.98×10^{17}, 1.57×10^{17}, and $0.72\times10^{17}cm^{-3}$. The different average grain sizes cause the critical doping level to change, which effectively moves the doping level with respect to N^*. This can be observed in Fig. 4.6. Let us first consider the case where the average grain size is $500\text{\AA}$. The doping level is below the critical doping $N<N^*$. Therefore, the behavior of this case is similar to the case discussed earlier. When the average grain size is about $1000\text{\AA}$ the doping level falls slightly above the critical doping level. Thus the film is partially depleted and the grain boundary barrier potential is almost at its maximum value. The
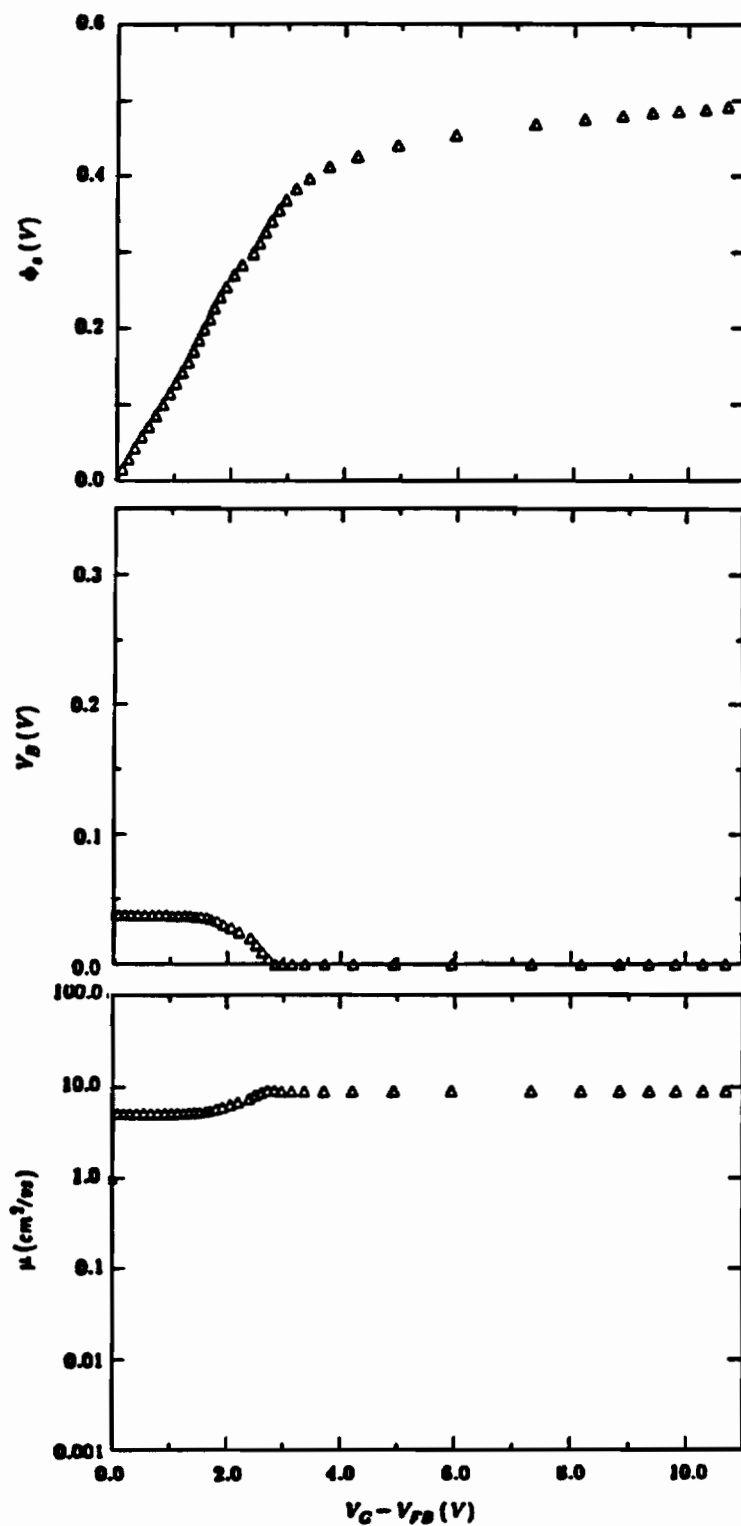
Fig. 4.5 Surface potential, grain boundary barrier potential and channel electron mobility as a function of $V_{GS} - V_{FB}$, for doping levels below N*.
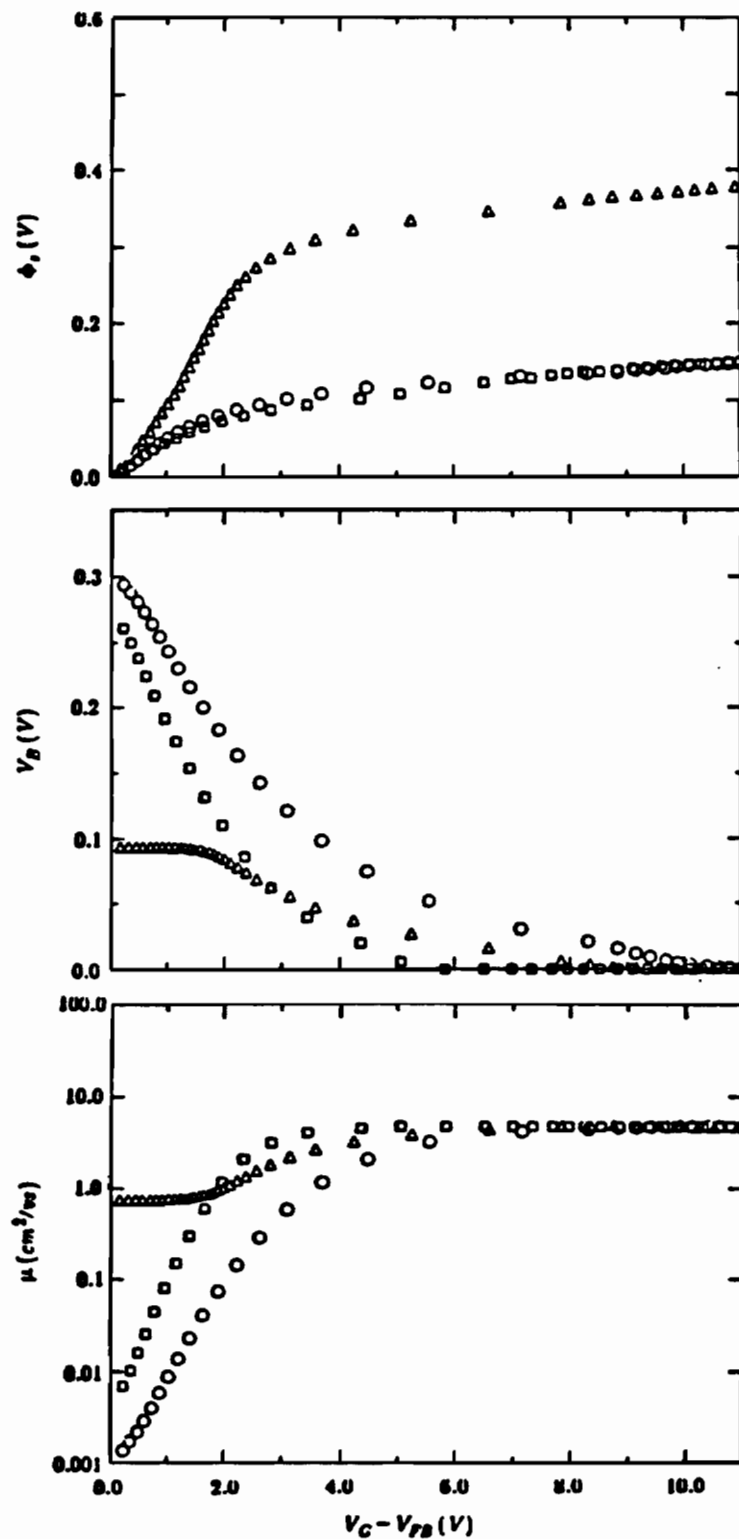
Fig. 4.6 Surface potential, grain boundary barrier potential and channel electron mobility as a function of $V_{GS} - V_{FB}$, for different average grain sizes. Triangles ($\triangle$) denote $L_g = 500\text{Å}$, circles ($\bigcirc$) denote $L_g = 1000\text{Å}$ and squares ($\square$) denote $L_g = 1500\text{Å}$.

mobility then should be very small at flat band (V=0 volt). In this case, as the gate voltage is increased from the flat band the maximum swing in the mobility results. At $L_g=1500$Å the doping level falls even further above N*. The barrier potential decreases at flat band, hence the mobility is higher. The swing in the mobility is less than the case where the doping density is closer to the critical doping. We should note that the different average grain sizes only places us in different positions (above or below) with respect to the critical doping and the same analysis used for different doping levels also holds here.

The effect of the trapping level E_T on the variations of ϕ_s, V_B and μ with V is shown in the Fig. 4.7. The trapping level is measured from the intrinsic Fermi level, so a larger value of E_T refers to a shallower trap. The doping density, trapping density and the average grain size used are respectively $2\times10^{17}cm^{-3}$, $2\times10^{12}cm^{-2}$ and 1000Å. The trapping levels considered here are 0.05, 0.1 and 0.2 eV and the respective critical doping densities are 1.76×10^{17}, 1.57×10^{17} and 1.14×10^{17}. The variations in the trap level can be caused by differences in film deposition, differences in thermal processing, and hydrogen passivation. Fermi statistics dictates that the movement of the Fermi level with increased doping level is decreased the deeper the trap level lies. It also means that more of the traps are full when the trap level is closer to the intrinsic level (deeper). At the trap level 0.05 eV the critical doping is the largest. Because the trap level is the deepest, more carriers are trapped. Consequently the barrier potential is higher. A large barrier potential makes the mobility smaller and when a voltage is applied the largest enhancement in the mobility is observed. When the trapping level is shallower, $E_T=0.1$ eV, at flat band V=0.0 volt the barrier potential is smaller, because the
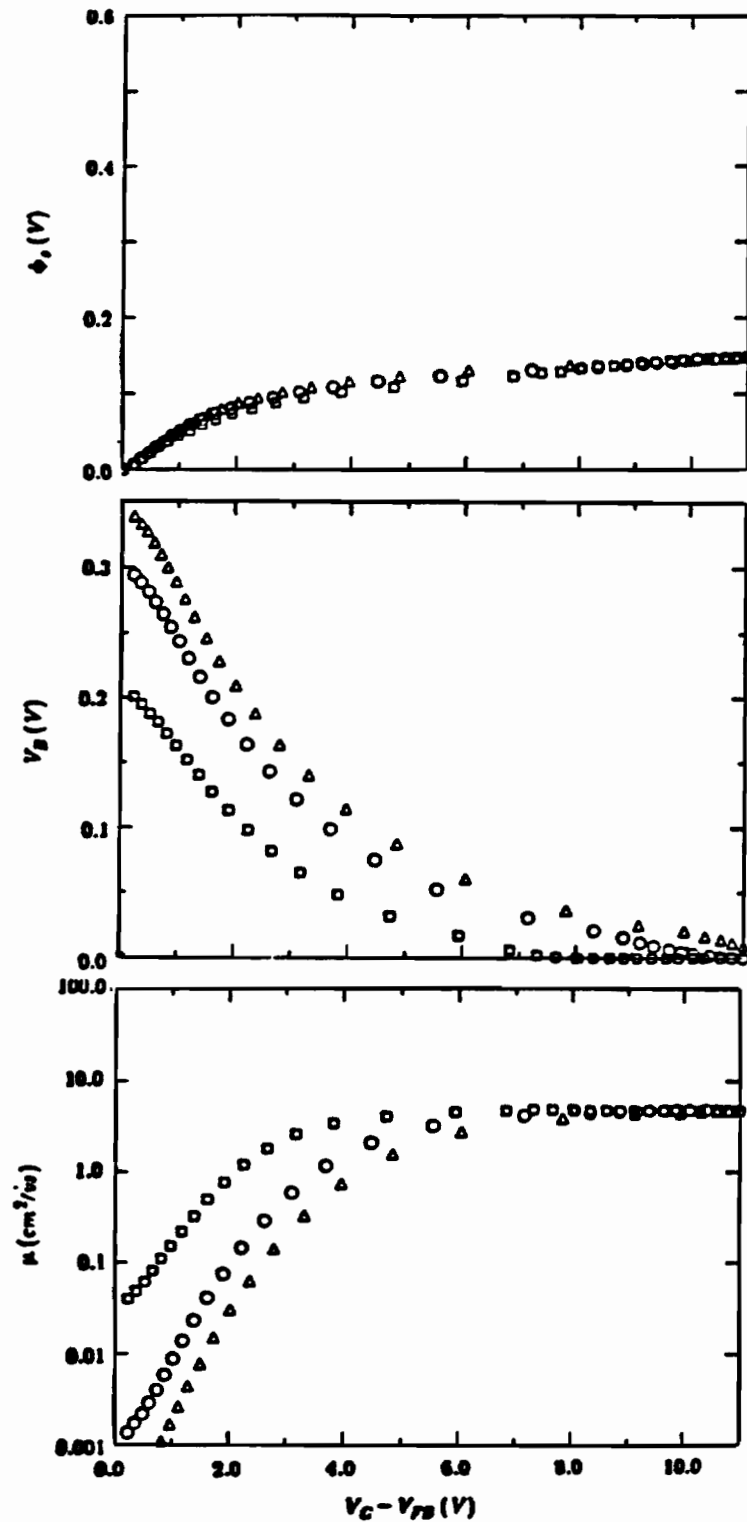
Fig. 4.7 Surface potential, grain boundary barrier potential and channel electron mobility as a function of $V_{GS} - V_{FB}$, for different trap levels. Triangles ($\triangle$) denote $E_T = 0.05\,eV$, circles ($\bigcirc$) denote $E_T = 0.10\,eV$ and squares ($\square$) denote $E_T = 0.20\,eV$.

trap is less effective. The mobility enhancement is also less than in the 0.05eV case. The traps are even less effective when E_T=0.2 eV. The critical doping density is smallest, the barrier potential is lower than the other two cases and the mobility enhancement is least. Note that at strong accumulation the final value for the channel mobility is the same regardless of the trap level, and the largest mobility enhancement is for the deepest trap level.

In Fig. 4.8 the effect of the trapping density on ϕ_s, V_B, μ are presented. It has been noted by Ahmed et al. [27] that the surface scattering factor varies with different trapping density. But due to lack of experimental data we cannot predict the surface scattering factors for trapping densities other than $2 \times 10^{12} cm^{-2}$. The factor η used here is 0.008. The typical values for η are around 0.01-0.02. In Fig. 4.8 the trapping densities presented are 1×10^{12}, 4×10^{12} and $8 \times 10^{12} cm^{-2}$. The corresponding critical doping densities are 5.91×10^{16}, 7.91×10^{16} and $8.44 \times 10^{16} cm^{-3}$. As the critical doping density decreases, the barrier potential also decreases. Consequently the mobility enhancement due to the shielding of the uncompensated ionized dopants decreases.

4.2.2.2. Diffusion Current

A weak accumulation current or diffusion current occurs when there is a concentration gradient in the channel. The source side of the channel is grounded. Therefore any gate voltage greater than the flat band voltage causes the accumulation of mobile carriers in the channel. At the drain side the gate voltage has to be
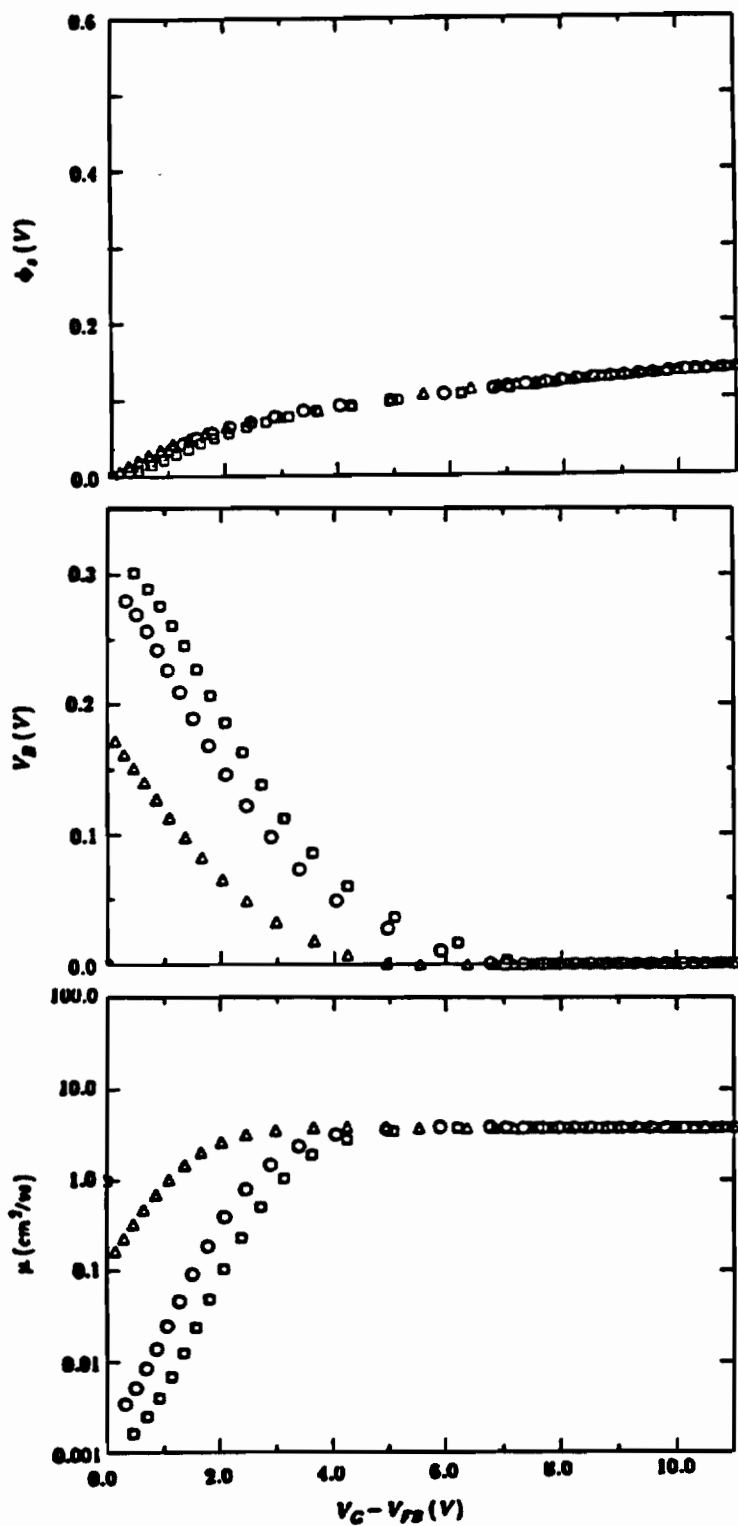
Fig. 4.8 Surface potential, grain boundary barrier potential and channel electron mobility as a function of $V_{GS} - V_{FB}$, for different trap density. Triangles ($\triangle$) denote $Q_T = 1 \times 10^{12} cm^{-2}$, circles ($\bigcirc$) denote $Q_T = 4 \times 10^{12} cm^{-2}$ and squares ($\square$) denote $Q_T = 8 \times 10^{12} cm^{-2}$.

greater than the sum of flat band voltage and the drain voltage in order for an accumulation layer to exist. When the source side is accumulated and the drain is not, a diffusive current flows through the channel.

In Fig. 4.9 the dependence of this diffusion current on gate voltage is presented when the doping density N is varied. The results shown are for the case where $N^*=7.22\mathrm{x}10^{16}cm^{-3}$, $E_T=0.1eV$, Lg=1500Å, $Q_T=2\mathrm{x}10^{12}cm^{-2}$ and the surface states $Q_{sf}=3\mathrm{x}10^{11}cm^{-2}$. These are typical values for the film and device parameters. The first doping considered is $N=5\mathrm{x}10^{16}cm^{-3}$ which is below N*. The barrier potential is relatively large and this makes the mobility to be small. We can see that until $V_{GS}=0.0$ volt there is no enhancement in the drain current and after that voltage we see it increase. As explained earlier this is because below the critical doping we first must fill all the traps before shrinking of the depletion region can occur. At gate voltages larger than 0.0 volts, carriers get injected and the barrier potential decreases causing the mobility to increase. For the doping below the critical doping, as observed before, that the mobility enhancement is not very high but this enhancement in conjunction with the injection of carriers, gives rise to about two orders of magnitude increase in the drain current. The next doping level $N=8\mathrm{x}10^{16}cm^{-3}$, is slightly above the critical doping. At flat band the barrier potential is high causing the mobility to be very small. As a result of low mobility and low gradient in carrier density the drain current is very small: $\approx10^{-10}A$. Above N*, shielding takes place as the gate voltage is increased. Therefore the mobility will increase and carriers injected to the surface will increase the gradient in concentration causing the current to rise. When V_{GS} reaches about 2 volts, the barrier potential is gone and the band bending is at a maximum, thus
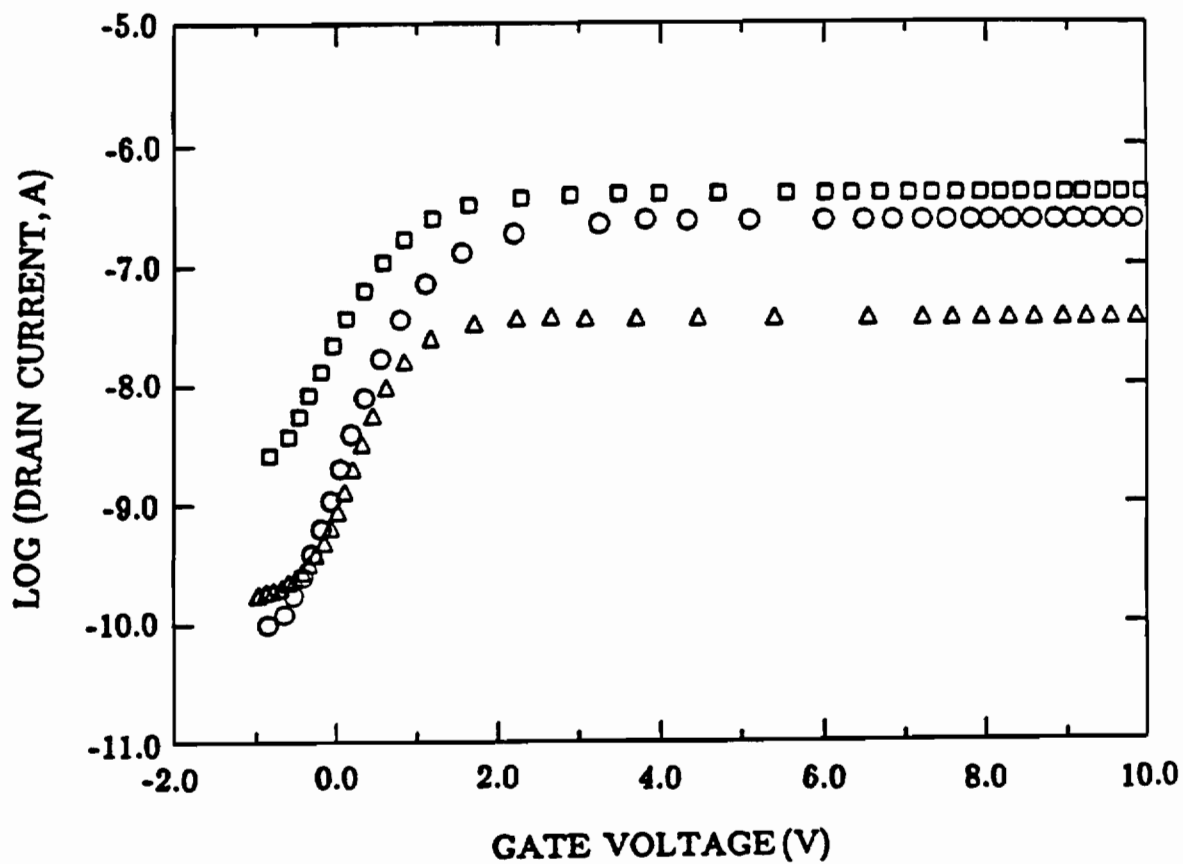
Fig. 4.9 Diffusion current as a function of gate voltage, for different doping levels. Triangles ($\triangle$) denote $N = 5 \times 10^{16} cm^{-3}$, circles ($\bigcirc$) denote $N = 8 \times 10^{16} cm^{-3}$ and squares ($\square$) denote $N = 1.5 \times 10^{17} cm^{-3}$.

forcing the current to saturate. When the doping concentration is further increased to $N=1.5 \times 10^{17} cm^{-3}$, the barrier potential is reduced giving rise to a higher mobility. Also the average carrier concentration is increased. These result in a higher drain current at flat band. As before the mobility is increased when gate voltage is increased. At a gate voltage of about 2 volts, the drain current reaches its maximum value because both the mobility and the band bending have reached their maximum values.

Next we look at the dependence of the diffusion current on the grain boundary trap level as the gate voltage is varied. The results are presented in Fig. 4.10. The trap levels used are 0.05, 0.1 and 0.2 eV measured from the intrinsic Fermi level. The doping density used here is above the critical doping density and all the other parameters used here are the same as the ones used for Fig. 4.7. The effect of the trap level on the barrier potential was discussed earlier and we see that the highest barrier potential results when the trap is deepest. The deepest trap level used here is 0.05 eV, and at flat band the diffusion current is very close to $10^{-11}A$. Again, as noticed earlier, different trap levels do not effect the shielding of the uncompensated ionized dopants. The diffusion current saturates at a gate voltage close to 2 volts and becomes about $10^{-7}A$, that is, four orders of magnitude change from the flat band value. The shallower trap levels effect the value of the barrier potential at flat band. Looking at the shallowest trap we can see that the swing of the current changes but the subthreshold slope remains the same and does not change with E_T. This can be seen in the Fig. 4.10, the current saturates at lower voltages for shallower traps.

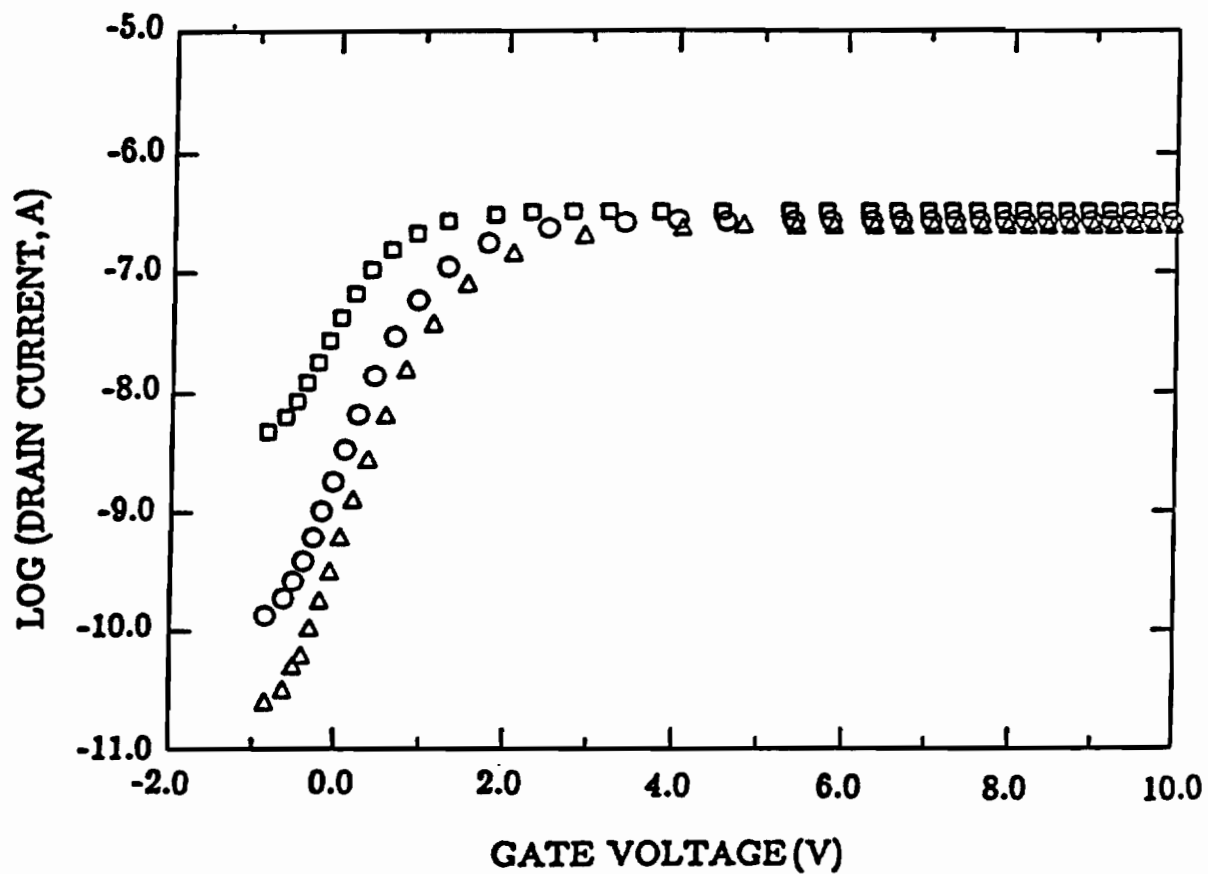Fig. 4.10 Diffusion current as a function of gate voltage, for different trap levels. Triangles ($\triangle$) denote $E_T = 0.05 eV$, circles ($\bigcirc$) denote $E_T = 0.10 eV$ and squares ($\square$) denote $E_T = 0.20 eV$.

The dependence of diffusion current on the average grain size of polysilicon is shown in Fig 4.11. The grain sizes used are 500, 1000, and 1500 Å. All the parameters are the same as the parameters used in Fig. 4.6. For L_g of 1000 and 1500 Å the doping level is above the critical doping N*. The only difference is that the subthreshold slope is improved for the 1500Å grain size. This is because of the improved shielding. Below the N* the situation is different; the ineffective shielding caused by slow accumulation and the small enhancement of the mobility cause the subthreshold slope to be very high, which is not desirable. Thus the best results are achieved at doping levels above the critical doping density.

As mentioned before, the grain boundary trap density has been reported to effect the surface scattering η and Q_{if} the interface states. Lower Q_T is said [27] to result in a lower value for the surface states and a higher surface scattering factor. More experimental data is required to confirm these results.

4.2.2.3. Drive Current

Drive current flows in the channel when the gate voltage is larger than $V_{DS} + V_{FB}$. This condition causes both the source and the drain side of the channel to be accumulated. Here we will analyze this current for different polysilicon and device properties.

The dependence of variation of the drive current versus gate voltage on doping density is shown in Fig. 4.12. These results are for doping densities above the critical doping. Below N* the drive current is small in magnitude, because the gate voltage is used to fill the traps. The first doping level, $N=8x10^{16}cm^{-3}$, that is

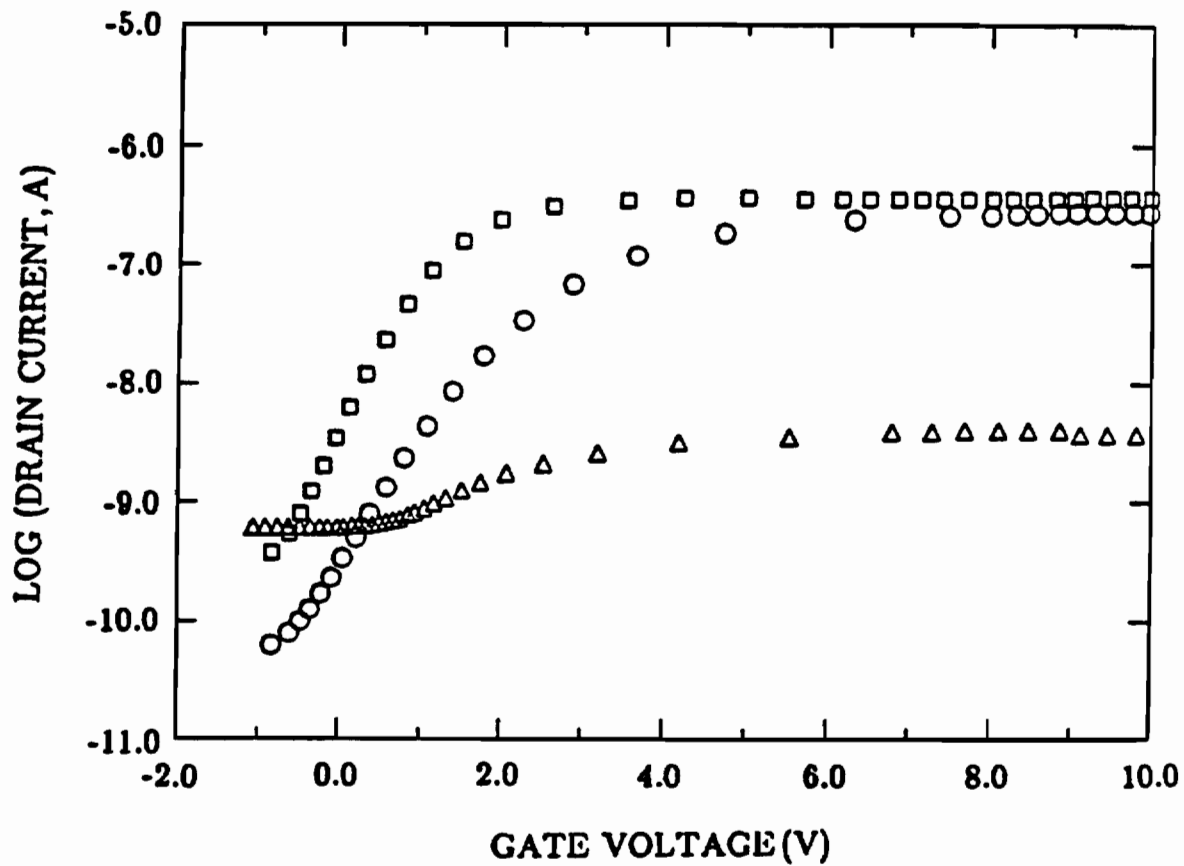Fig. 4.11 Diffusion current as a function of gate voltage, for different average grain sizes. Triangles ($\triangle$) denote $L_g = 500$Å, circles ($\bigcirc$) denote $L_g = 1000$Å and squares ($\square$) denote $L_g = 1500$Å.
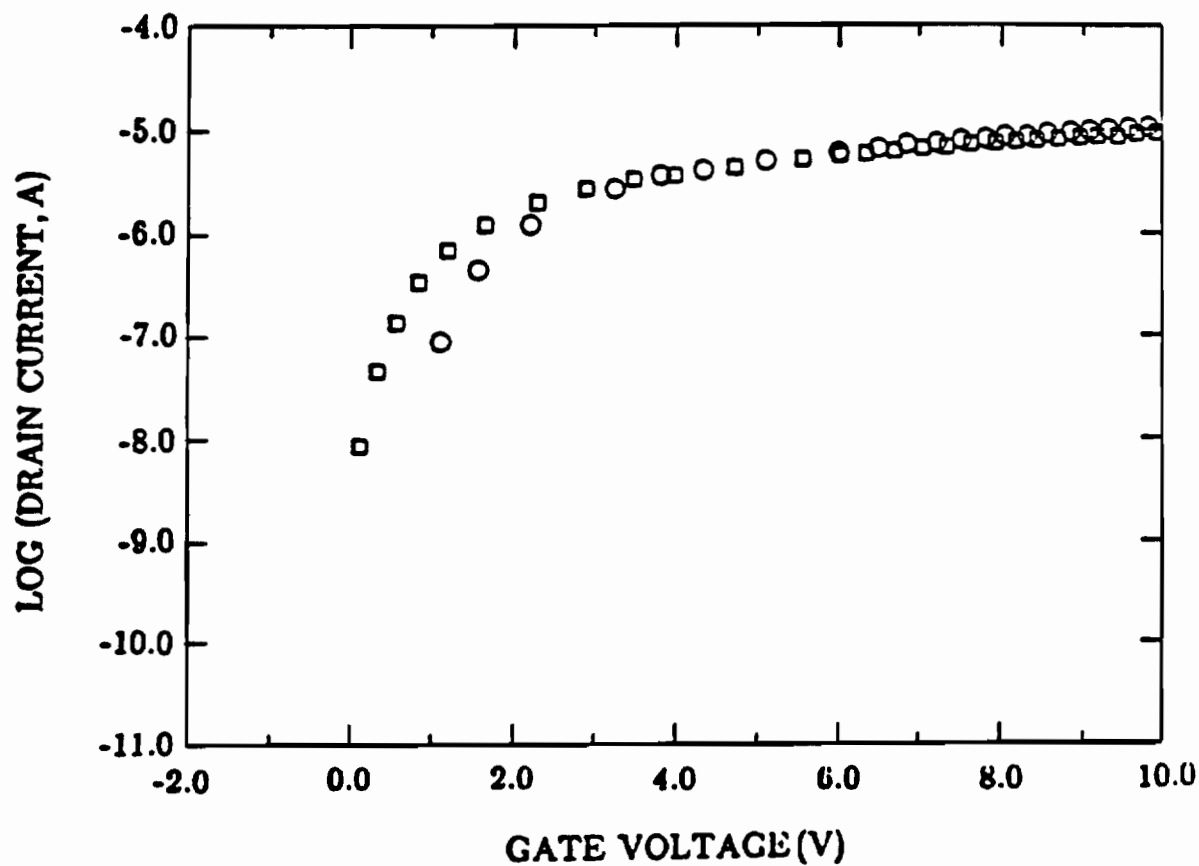
Fig. 4.12 Drive current as a function of gate voltage, for different doping levels. Circles (○) denote $N = 8 \times 10^{16} cm^{-3}$ and squares (□) denote $N = 1.5 \times 10^{17} cm^{-3}$.

above N^*, which is $7.22 \times 10^{16} cm^{-3}$. The parameters are the same as the ones used for Fig. 4.9. This behavior is very similar to the single crystalline device. The Debye length is different for different doping, therefore the contribution of the term $\alpha \dfrac{L_D}{L_G} q \dfrac{Q_T}{C_{oz}}$ decreases as the doping is increased. This can be observed in the case of the next doping level $N=1.5 \times 10^{17} cm^{-3}$.

In Fig. 4.13 we can see the effect of different average grain sizes on the drive current. Again in this case, for a small grain size of 500Å, the doping falls below the critical doping, and the drive current will be very small. The parameters used here are the same as the ones used for Fig. 4.11. The main difference between the two curves is that in the case of the larger grain size, the contribution of the trapped charges at the surface is less. Therefore, the drive current will flow at a smaller gate voltage. Other than that, the variations are due to the physical mechanisms explained earlier, such as mobility enhancement.

Fig. 4.14 shows the behavior of the drive current when the trap level is varied. Basically if we refer to Fig. 4.7 where the variations of mobility with trap level are shown, the same kind of behavior is observed. The physical explanation for that has already been discussed.

The dependence of drive current-gate voltage relationship on the trap density is not shown here. The trap density is said to effect the surface scattering factor and the surface states. A lower trap density gives rise to a higher scattering factor therefore higher mobility will result. Also lower surface states are said to result from lower trap density. In order to confirm these results more experimental data is needed.

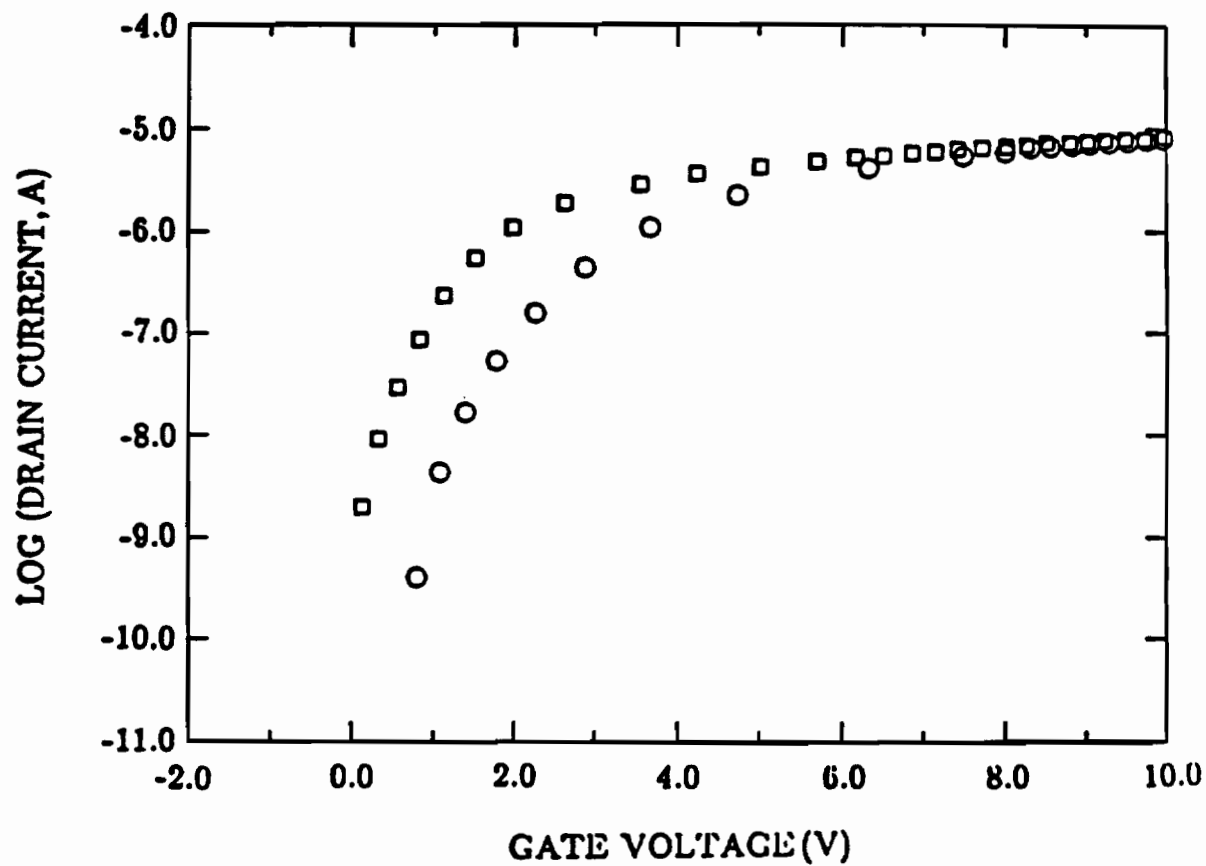Fig. 4.13 Drive current as a function of gate voltage, for different average grain sizes. Circles (O) denote $L_g = 1000\text{Å}$ and squares (□) denote $L_g = 1500\text{Å}$.

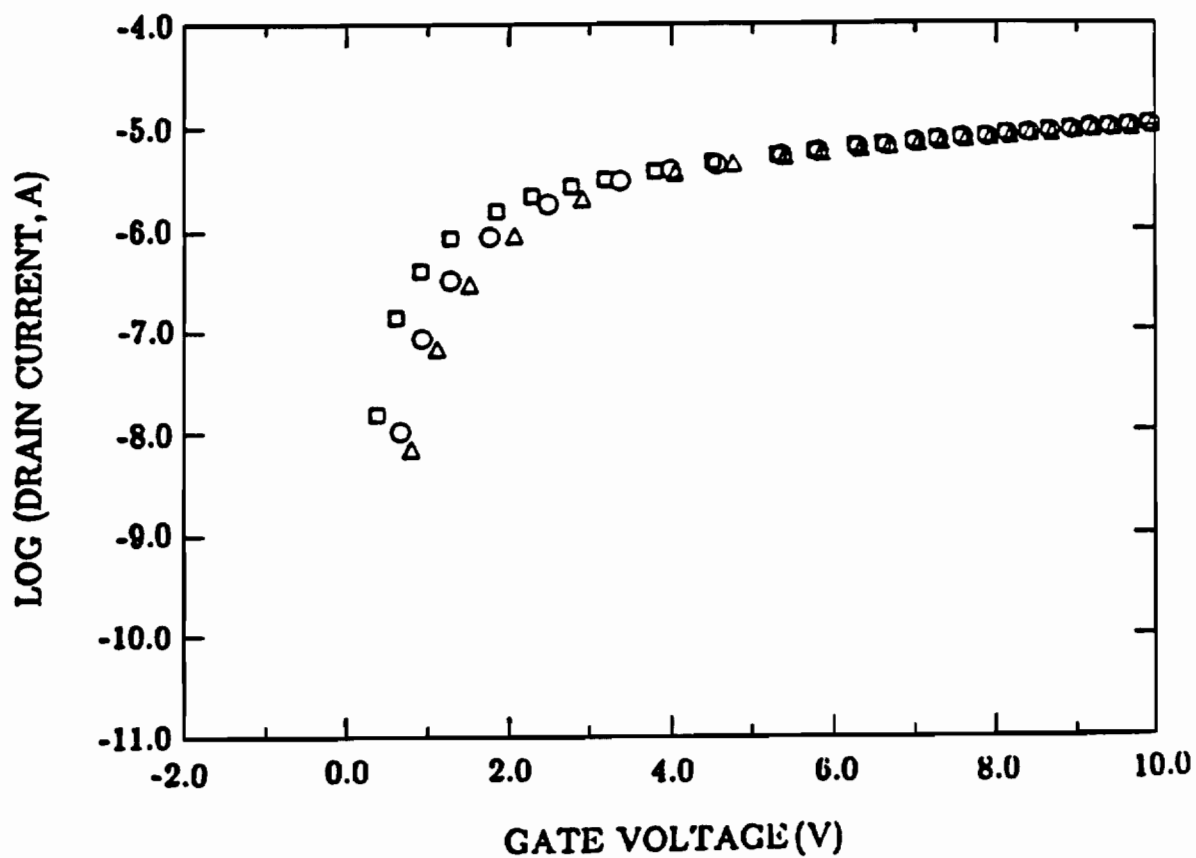Fig. 4.14 Drive current as a function of gate voltage, for different trap levels. Triangles ($\triangle$) denote $E_T = 0.05\,eV$, circles ($\bigcirc$) denote $E_T = 0.10\,eV$ and squares ($\square$) denote $E_T = 0.20\,eV$.

4.3. Comparison With Experiment

In this section we make an attempt to compare the experimental results obtained by Malhi et al. [34] with the theoretical results based on the formulation which were described earlier in this thesis. Table 1 gives the polysilicon parameters and the device dimensions for the device measured by Malhi et al. [34] The device is an accumulation-type N-channel top-gated polysilicon MOSFET operating at room temperature.

As mentioned in section 2.1, dopant incorporated into polysilicon films have a tendency to segregate. This segregation is a function of annealing temperature, dopant species, and the length of time at which it is annealed. Generally, segregation is less at higher annealing temperature and shorter annealing time. The devices under consideration here were annealed at $950°C$ for 25 minutes. It has been shown that annealing at $900°C$ requires 12 hours for complete segregation. Therefore it is logical to assume that for this short anneal, only a small fraction of dopants will segregate, probably about 10%. Consequently, in this analysis where the polysilicon films were annealed at a relatively high temperature, $950°C$ for 25 minutes the effect of segregation is assumed to be very small.

In Fig. 4.15 the barrier potential, mobility and the band bending under a gate voltage is presented. The thickness of the polysilicon film used in this device is 1500Å. As discussed earlier, the average grain size approaches the thickness of the film and here, as a result, L_g is assumed to be 1400Å. This is also in agreement with previously reported data[27]. The doping level is calculated from the

Table 1

Device dimensions and polysilicon film properties that are used to explain the experimental data.

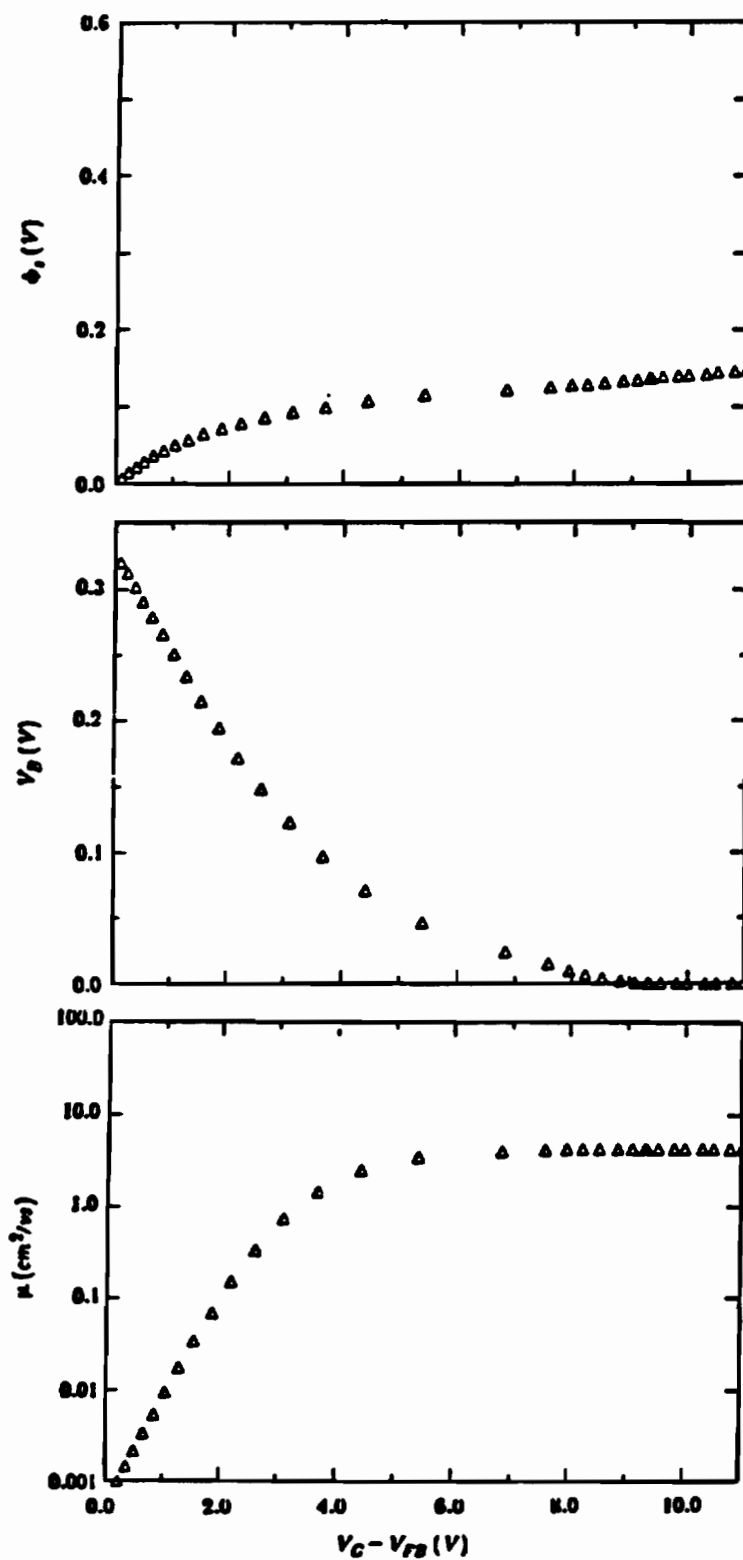| Parameter	Value
L	$2.0\mu\text{m}$
Z	$52.0\mu\text{m}$
t_{ox}	500Å
Q_{sf}	$3.0\times10^{11}cm^{-2}$
N_D	$2.6\times10^{17}cm^{-3}$
α	0.5
L_g	1400Å
Q_T	$2.0\times10^{12}cm^{-2}$
E_T	$0.05eV$
t_f	1500Å
η	0.008

Fig. 4.15 Surface potential, grain boundary barrier potential and channel electron mobility as a function of $V_{GS} - V_{FB}$. The device and the polysilicon film parameters are the same as ones given in Table 1.

reported[34] implant dose of $4 \times 10^{12} cm^{-2}$ into films of 1500Å thickness, and considering 10% reduction for segregation, we calculate the doping to be $N = 2.4 \times 10^{17} cm^{-3}$. The critical doping density for $L_g = 1400$Å, $Q_T = 2 \times 10^{12} cm^{-2}$, and $E_T = 0.05 eV$, is $N^* = 9.5 \times 10^{16} cm^{-3}$. Consequently, the grain is only partially depleted.

Figure 4.16 presents the drain current I_D as a function of gate voltage V_{GS} for the drain voltage $V_{DS} = 0.1 V$. The surface state density is reported to be small but not as small as the reported values for the single crystalline device. Q_{sf} is assumed to be $3.0 \times 10^{11} cm^{-2}$, which is a typical value for polysilicon MOSFET interface states, and seems to give fair results. This value of Q_{sf} has been reported[27] to occur when the trapping density is relatively small in magnitude. In our case the trap density is taken to be $2.0 \times 10^{12} cm^{-2}$, which is a reasonable number and agrees with the small Q_{sf}. The flat band voltage is $V_{FB} = -0.82$V.

Before giving any further explanation of figure 4.16, it should be pointed out that Fig. 4.15 shows the mobility, barrier potential and the surface potential corresponding to the film properties and parameters of this device. The grain is partially depleted. Therefore, a gate voltage greater than the flat band will cause injection of carriers to the surface, in effect, shrinking the barrier potential. The mobility is a strong function of barrier potential, and it increases when the barrier potential decreases. The mobility reaches a maximum value when the barrier potential disappears. These effects were explained in more detail in Sec. 4.2.2.1. In the single crystalline case for the accumulation type device the channel forms when the flat band voltage is exceeded and the drive current will start to flow. From the linear plot shown in Fig. 4.16, we observe a positive threshold voltage instead of a
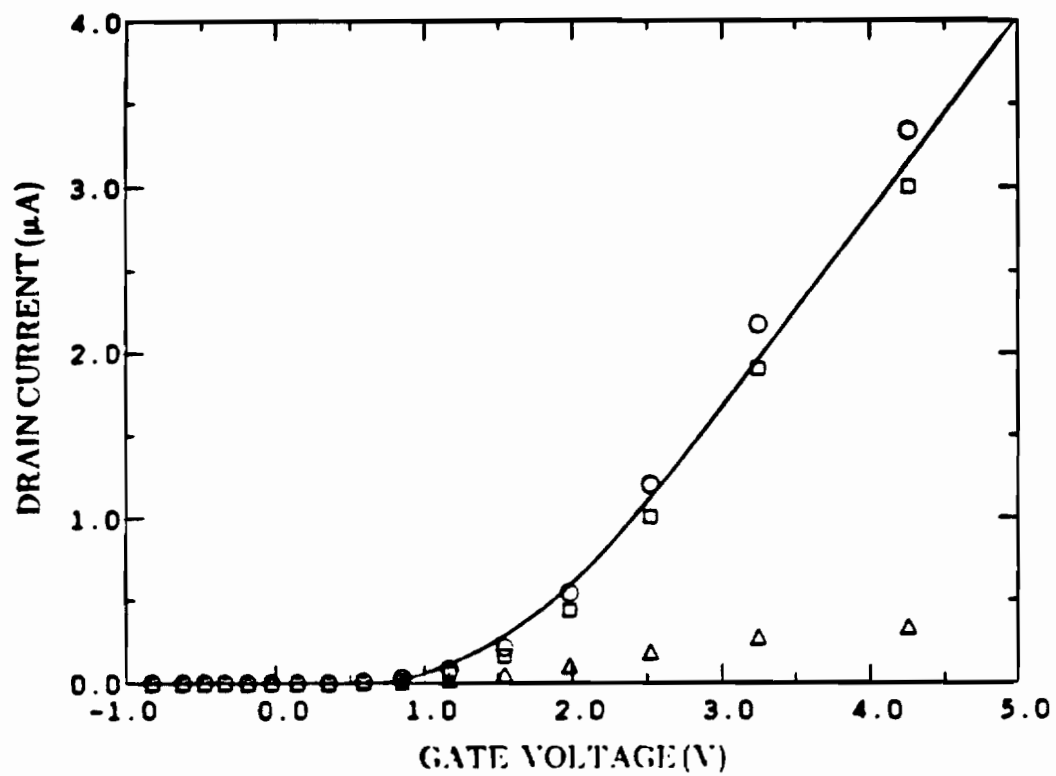
Fig. 4.16 Linear plot of drain current as a function of gate voltage for $V_D = 0.1$ Volt. Solid line (-) represents the experimental result, triangles ($\triangle$) represent the theoretical diffusion current, squares ($\square$) represent the theoretical drive current and circles ($\bigcirc$) represent the total theoretical current.

negative one. This is caused by a unique characteristic of polysilicon MOSFET: that is mobility enhancement caused by the applied gate voltage.

In order to get a better understanding of the physics of conduction operating in the device, consider Fig. 4.17 which represents the logarithm of drain current as a function of gate voltage. At flat band the mobility is very small: $\approx 0.001 cm^2/Vs$. As the gate voltage increases, band bending occurs and the mobility starts to increase. This creates a gradient in concentration within the channel, which gives rise to a diffusion current. The diffusion current remains the dominant term up to $V_{GS} \approx 0.3 V$. As the gate voltage is further increased, the traps are now filled up and a channel exist at the surface extending from source to drain. Drive current becomes the dominant term at this gate voltage and above, as shown in Fig. 4.17. The diffusion current keeps increasing until the gate voltages reaches 2.5V because, as discussed before, the mobility enhancement still exists. For gate voltage above 2.5V, the diffusion current is saturated. Fig. 4.17 shows that the ON/OFF ratio is a little more than three orders of magnitude which is not quite sufficient for high performance applications. For comparison purpose, the desired ON/OFF ratio for single crystalline devices is greater than seven orders of magnitude.

The variations of square root of drain current as a function of gate voltage for $V_D = 5.0$ Volt is shown in Fig. 4.18. This type of curve is used for measuring the threshold voltage of MOSFETs. The threshold voltage is obtained from where a line through the straight part of the curve crosses the horizontal axis. To understand how this works one should refer to the saturation current equation for single crystalline MOSFETs and taking its square root. The result will be square root of

Fig. 4.17 Logarithm of drain current as a function of gate voltage for $V_D = 0.1$ Volt. Solid line (-) represents the experimental result, triangles ($\triangle$) represent the theoretical diffusion current, squares ($\square$) represent the theoretical drive current and circles ($\bigcirc$) represent the total theoretical current.
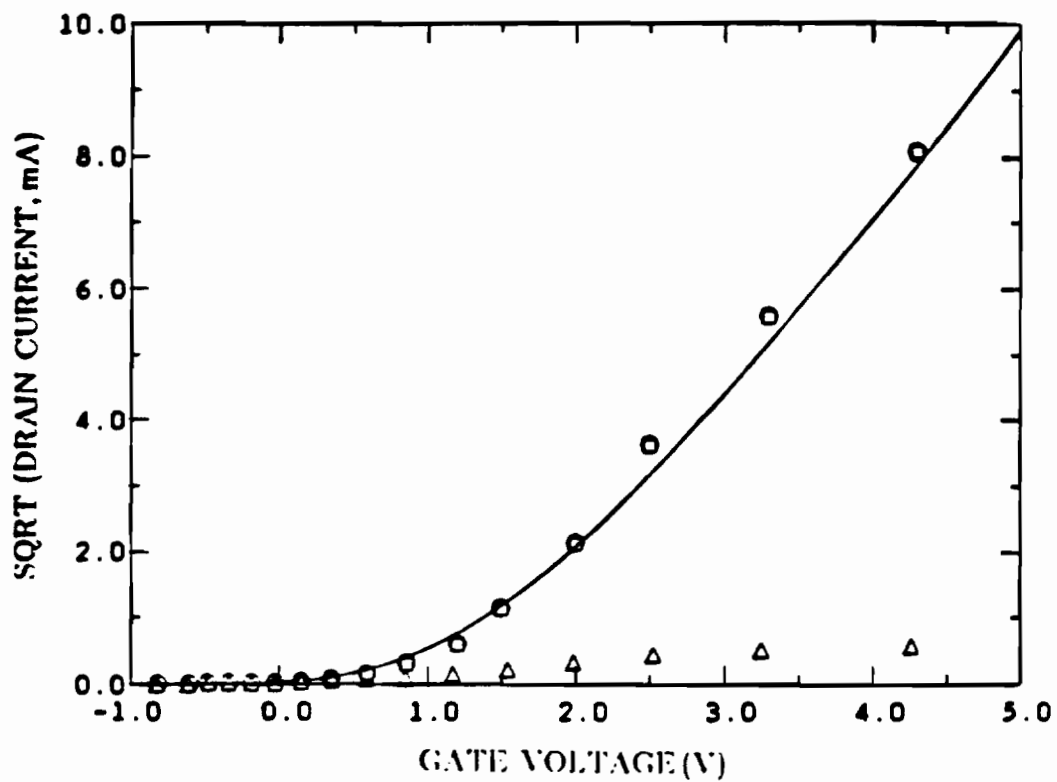
Fig. 4.18 Square root of drain current as a function of gate voltage for $V_D = 5.0$ Volt. Solid line (-) represents the experimental result, triangles ($\triangle$) represent the theoretical diffusion current, squares ($\square$) represent the theoretical drive current and circles ($\bigcirc$) represent the total theoretical current.

drain current versus some constant times $(V_{GS} - V_T)$. At zero drain current the gate voltage is equal to the threshold voltage. Finally, in Fig. 4.19, the logarithm of drain current as a function of gate voltage is shown for drain voltage $V_D = 5.0$ Volt.
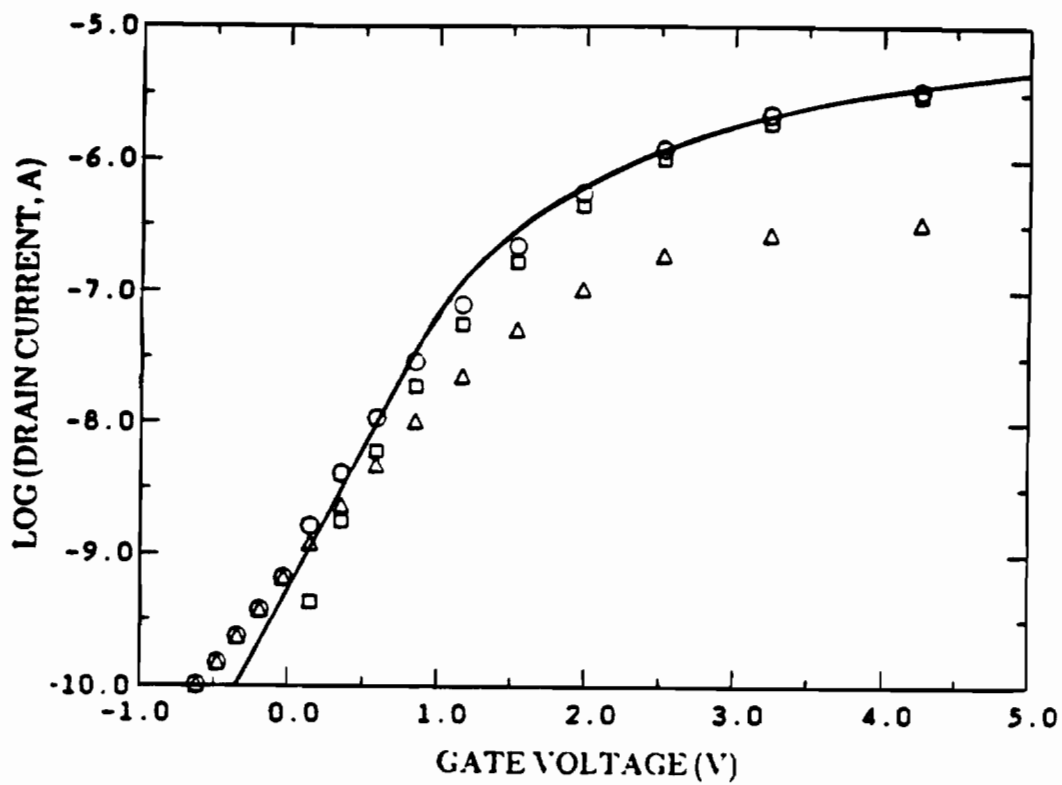
Fig. 4.19 Logarithm of drain current as a function of gate voltage for $V_D = 5.0$ Volt. Solid line (-) represents the experimental result, triangles ($\triangle$) represent the theoretical diffusion current, squares ($\square$) represent the theoretical drive current and circles ($\bigcirc$) represent the total theoretical current.
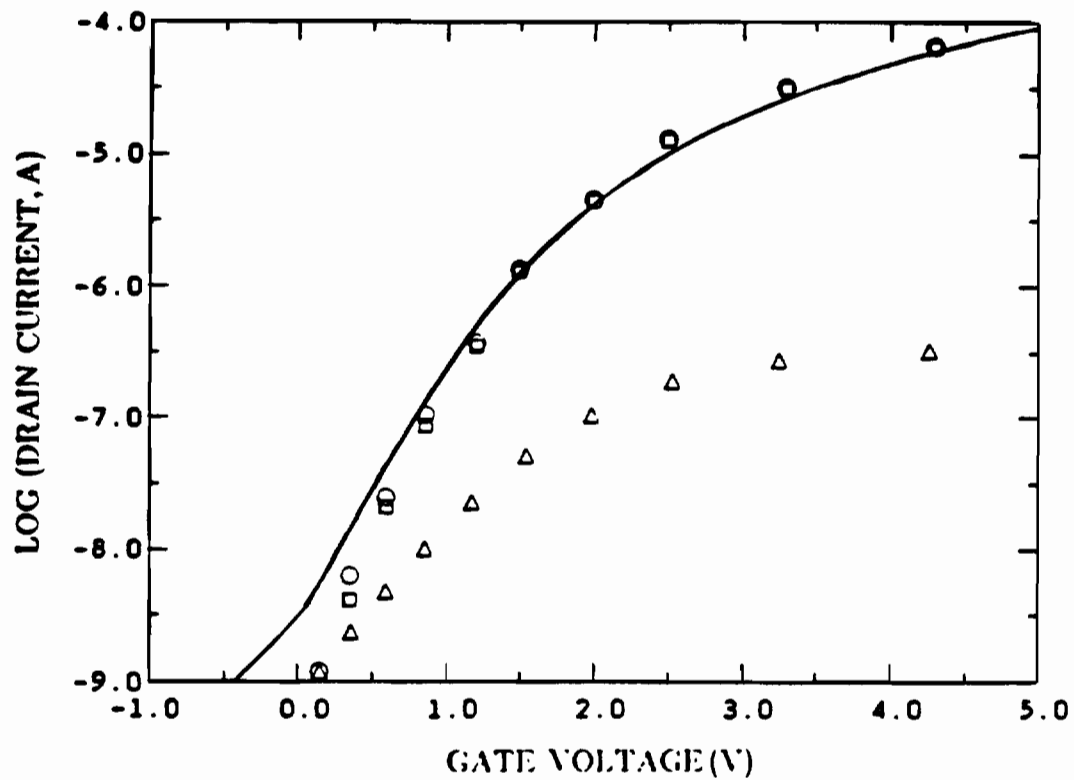
CHAPTER 5

CONCLUSIONS

AND SUGGESTIONS FOR FURTHER RESEARCH

In this thesis we have discussed the electrical characteristics of N-channel accumulation mode MOSFETs fabricated in polysilicon thin films. The carrier transport process is via drift and diffusion. This carrier transport is taken to occur through a hetero-junction formed between crystalline-amorphous-crystalline silicon regions and holds for different grain sizes, doping density, film thickness, grain boundary trap density and level. Segregation of dopant atoms to the grain boundary is taken into account. This segregation is a function of the dopant species, annealing temperature and annealing time. This model takes into account the shielding of uncompensated ionized dopants by the mobile carriers which are injected under the gate when a gate voltage is applied. This shielding causes a mobility enhancement which takes place when a positive voltage is applied at the gate. A positive threshold voltage results from the mobility enhancement. This enhancement is only significant for the channel doping levels beyond a critical doping N^*. The increase in mobility can be as much as three orders of magnitude.

There are three regimes of device operation but only two main ones. At small gate voltages the dominant component of current that flows through the channel is a diffusive current. This current is caused by the concentration gradient of carriers induced by application of a drain voltage. The drive current which is similar to the drive current in single crystalline MOSFETs becomes the dominant term at about

two volts above the flat band. This is partly because a portion of mobile charges under the gate get trapped at the grain boundary.

The model agrees fairly well with the experimental results, and the positive threshold voltage is verified with a plot of square root of drain current versus the gate voltage. A discrepancy exists between theory and experiment only at high drain voltage and low gate voltage. There are two reasons for this. First, the resistive leakage current that was assumed to be negligible becomes more significant at higher drain voltages. And second, because the drain and source extend all the way the the insulating substrate, conduction might occur at that interface. These two components of current could be investigated in the future, and then incorporated into the model. Finally, the channel length of the device discussed here was 2 μm, so the device can be considered a short channel device. Therefore the inclusion of some short channel effects also might be a good topic for future research.

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