Electrical Characterization of High-κ Gate Dielectrics For High Frequency Application

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Dedication

To my wife and to my children, Amanda, Estelle.

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Abstract

Electrical Characterization of High-κ Gate Dielectrics For High Frequency Application

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The aggressive scaling of CMOS devices is driving SiO_2-based gate dielectrics to its physical limits as stated in the International Technology Roadmap for Semiconductors (ITRS). The replacement of SiO_2 with a high-κ material allows for an increase in the physical thickness of the gate insulator, while maintaining a low equivalent oxide thickness and low direct tunneling current. Hf-based dielectric stands out in comparison to the other high-κ dielectrics and becomes the leading candidate to replace SiO_2. The identification of alternate gate dielectrics requires complete characterization. Especially, the electrical characterization of high-κ gate dielectric is crucial.

In this investigation, the MOS capacitors with various high-κ materials deposited by atomic layer chemical vapor deposition (ALCVD) are employed as test structures to study the electrical properties of high-κ materials in the low frequency region. ALCVD is a well-controlled surface saturating process using gas-solid interactions to deposit thin film, which is becoming the primary method for the deposition of gate dielectric in state-of-the-art silicon devices. Through conventional capacitance-voltage (C-V) and current-voltage (I-V) measurements, some important parameters, such as, dielectric constant, threshold voltage, oxide charge/interface states and leakage current density can be obtained. Since most material characterization is routinely performed only in the megahertz frequency range, there is limited information in literature on the performance

of high-κ dielectrics in the high frequency regime, i.e., radio frequency (RF) range. This investigation includes RF characterization of high-κ dielectrics to provide a comprehensive description. In RF characterization, the focus is placed on hafnium dioxide. The dielectric constant and dielectric loss up to 65 GHz has been successfully measured by the reflection coefficient (S_{11}) measured with a vector network analyzer. By creating a reliable equivalent circuit model, an optimization technique is applied to extract the intrinsic capacitance. The optimizer matches the measured and simulated data over entire frequency range. The error function is less than 0.1% at frequency of 65GHz, which is at least one order magnitude less than reported in literature. For our samples, the high-frequency characteristics are consistent with low-frequency characteristics measured with a LCR meter. This result demonstrates Hf-based high-κ dielectric can be the promising alternative for high speed device gate dielectric application.

CHAPTER 1: INTRODUCTION

The semiconductor industry has been driven by continuous scaling of Complementary Metal-Oxide-Silicon (CMOS) technology over the past three decades. The source of the success of the MOS transistor is the fact that a transistor can be scaled to increasingly smaller dimension, which enables the microelectronics industry to meet many technological requirements: high circuit density, fast switching speed and low standby power. For microprocessor application, transistor delay times have been reduced by more than 30% per technology generation resulting in a doubling of microprocessor performance every two years [Moore's law]. The 2003 edition of International Technology Roadmap for Semiconductors (ITRS) [1] projects continued rapid scaling in the physical gate length and other transistor dimensions for leading-edge logic chips as described in Table 1.1.

The traditional Si-based CMOS scaling includes gate length, gate dielectric thickness, source/drain extension and junction depth. Among them, the key element is the gate dielectric that has been employed for decades to separate the gate from the silicon channel: silicon dioxide (SiO_2). Gate dielectric thickness should be linearly scaled with electric gate length to maintain the same amount of gate control over the channel. Figure 1.1 shows the physical thickness trend of SiO_2 for the various logic generations [2]. Since the gate leakage current exponentially increases with the decreasing of the physical thickness of gate dielectric, the traditional SiO_2 gate dielectric has reached the fundamental leakage limit, due to tunneling. A new material has to be explored to replace the SiO_2.

It is not accidental for SiO_2 to be selected as gate dielectric in all previous generations. The use of amorphous, thermally grown SiO_2 as gate dielectric offers many advantages, which include thermal stability on silicon substrate, high quality Si-SiO_2 interface as well as easy integration in CMOS processing. In addition, the hard breakdown field of 10 MV/cm and low midgap interface state densities on the order of

$10^{10}/cm^2$ can be normally realized in modern CMOS devices. All of these superior electrical properties in SiO_2 present a significant challenge for any alternate gate dielectric candidate.

Table 1.1: MPU (Microprocessor Unit) Product Generations

Year of Production	2003	2004	2005	2006	2007	2008
Technology Node		90			65	
DRAM ½ Pitch (nm)	100	90	80	70	65	57
MPU Printed Gate Length (nm)	65	53	45	40	35	32
MPU Physical Gate Length (nm)	45	37	32	28	25	22
Year of Production	2009	2010	2012	2013	2015	2016
Technology Node		45		32		22
DRAM ½ Pitch (nm)	50	45	35	32	25	22
MPU Printed Gate Length (nm)	28	25	20	18	14	13
MPU Physical Gate Length (nm)	20	18	14	13	10	9

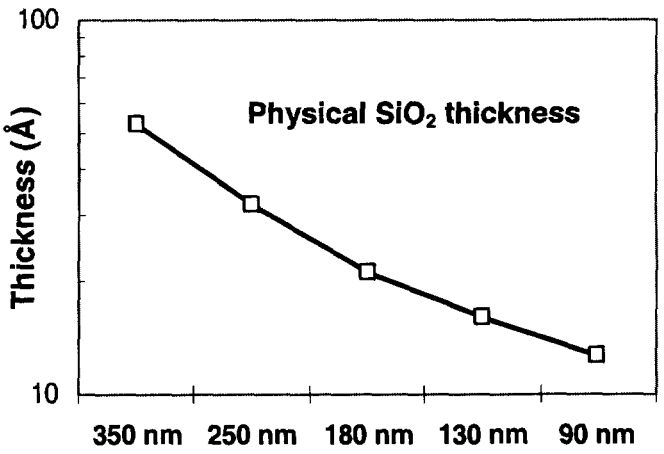


Figure 1.1: Scaling of physical thickness of SiO_2 gate oxide across technology generations.

1.1 Model-based transistor scaling and performance

Continued scaling has extensively been used to enhance device and circuit performance in modern CMOS technology. This enhanced circuit performance includes faster switching speed, lower power dissipation, and high circuit density. A common element employed to examine the switching time is a CMOS inverter [3], as shown in Fig 1.2. The switching time is limited by both the fall time required to discharge the load capacitance by the n-FET drive current and the rise time required to charge the load capacitance by the p-FET drive current. The switching time can be expressed by

$$\tau = \frac{C_{Load} \times V_{DD}}{I_{dsat}} \tag{1.1}$$

where C_{Load} is the load capacitance, V_{DD} is supply voltage and I_{dsat} is the saturation drive current. If the V_{DD} is kept unchanged, it is evident that the maximum drive current I_{dsat} is desired to reduce the switching time. The saturation drive current can be approximated as

$$I_{dsat} = \frac{W}{2L}\mu C_{ox}(V_G - V_T)^2, \qquad V_G - V_T \le V_D \tag{1.2}$$

where W is channel width, L channel length, μ the channel mobility, C_{ox} gate capacitance density, V_G gate voltage, V_D drain voltage, and V_T the threshold voltage. Therefore, an increased in gate capacitance or reduction of gate length results in an increase of saturation drive current I_{dsat}.

For the gate capacitance, consider a simple model of parallel plate capacitor.

$$C = \frac{\kappa \varepsilon_0 A}{t_{ox}} \tag{1.3}$$

where κ is the gate dielectric constant (also referred to as the relative permittivity), ε_0 the permittivity of vacuum, A the area of the capacitor, t_{ox} the thickness of gate dielectric. In

order to get high gate capacitance, the gate dielectric with high κ value or thin gate dielectric thickness should be used.

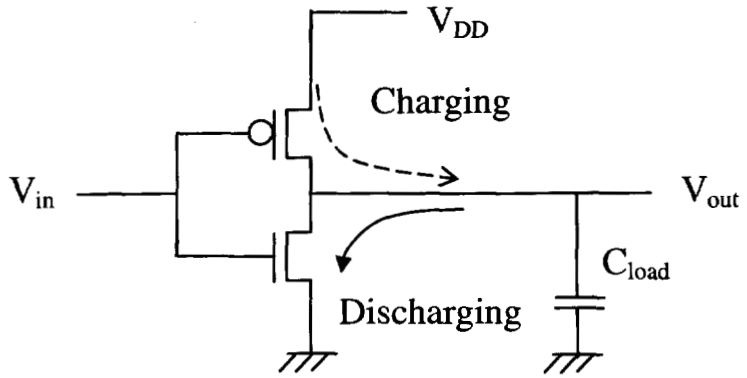


Figure 1.2: Illustrations of charging and discharging the load capacitance C_{Load}

1.2 Scaling limit of current gate dielectric

The scaling of MOSFET was first proposed by Bob Dennard [4] of IBM in 1972. Thereafter, the scaling has been successfully implemented in Si-based microelectronics industry and become the guideline to design and develop the devices for future technology generations. The initial scaling concept was based on maintaining a constant electric field while reducing the dimensions of the fundamental active device in the circuit: the field effect transistor. The dimensions include the channel length L, channel width W, source/drain junction depth x_j and the gate dielectric thickness t_{ox}. Due to the non-scalability of threshold voltage V_T, the constant voltage (supply voltage) scaling was adopted in modern CMOS products. Table 1.2 presents the above two scaling laws.

Gate dielectric thickness is linearly scaled with electric gate length to maintain the same amount of gate control over the channel. From the history of Intel's process technology, the gate dielectric thickness has been shrinking along with the gate length (L) by [5]

$$t_{ox} = L / 45 \qquad (1.4)$$

With L approaching 53 nm in Intel's 90 nm process and t_{ox} is just 12 Å, representing only five atomic layers of SiO_2. Once the gate dielectric thickness continues to be scaled below 8 Å, SiO_2 is too thin to be a good insulator as a gate dielectric. In the study by Muller et al. [6,7], a minimum of 8 Å of SiO_2 is required to obtain bulk properties. Such thin SiO_2 may result in severe problem in logic devices. The leakage current through SiO_2 layer increases exponentially as the gate dielectric thickness decreases. This leakage conduction leads the transistor to stray from its ideal "on" and "off" state and causes logic failure in the end.

Table 1.2: Constant Field Scaling vs Constant Voltage Scaling [8]

Parameter		Expression	Scaling Law	
			Constant E	Constant V
Dimension		L, W, t_{ox}, x_j	$1/\lambda$	
Voltage		V_{DD}, V_T	$1/\lambda$	**1**
Electric Field		E	**1**	λ
Doping Density		N_B	λ	λ^2
Circuit	Capacitance	$C_G = A \cdot \varepsilon / t_{ox}$	$1/\lambda$	
	Current	I_D	$1/\lambda$	λ
	Gate Delay Time	$t_{pd} = C_G \cdot V_{DD} / I_D$	$1/\lambda$	$1/\lambda^2$
	Power Dissipation	$I_D \cdot V_{DD}$	$1/\lambda^2$	$1/\lambda$
Interconnection	Line Resistance	$R_L = \rho \cdot l / A_L$	λ	
	Time Constant	$R_L \cdot C_L$	1	
	Current Density	I_D / A_L	λ	λ^3

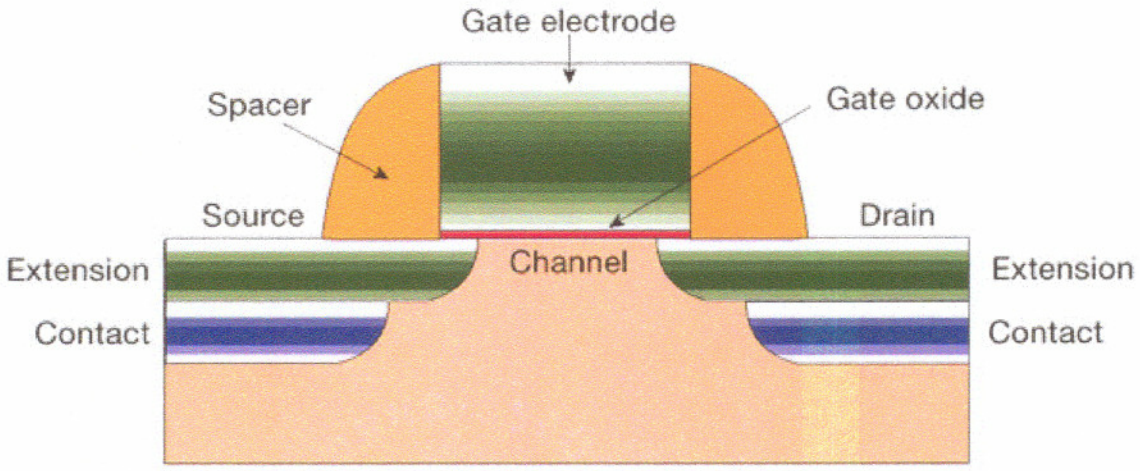
Ultrathin SiO_2 also gives rise to other concerns. On one hand, a film as thin as 8 Å should be uniform enough over the whole wafer. On the other hand, a very thin film is more likely to have more pin-hole defects. As reported by DeGrave et al. [9], the buildup of the defects within the SiO_2 layer degrades the oxide breakdown property and

eventually causes the reliability problem. When the thickness of SiO_2 is in sub-20 Å regime, high boron concentration in heavily doped polysilicon gate electrode will easily diffuse through the thin SiO_2 layer upon thermal annealing and disturb the doping concentration in channel region, which causes a shift in threshold voltage. It was reported that boron penetration could be relieved by nitrogen incorporation into oxide layer.

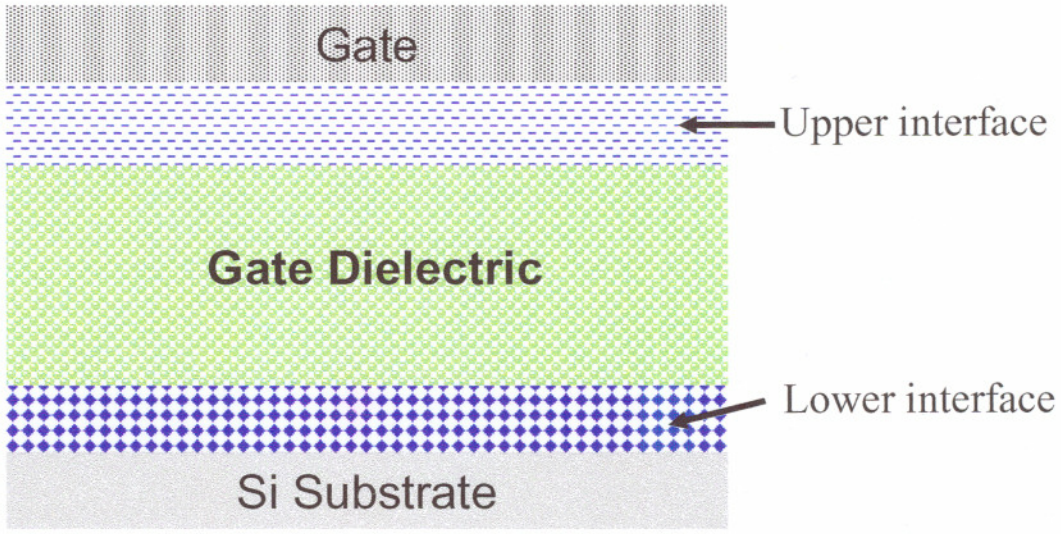
The above discussion clearly implies that high gate leakage current and pinhole density in ultrathin SiO_2 layer may preclude its use as gate dielectric in CMOS below 65 nm technology node. New materials have to be introduced into CMOS integrated circuit technology as potential replacements for SiO_2 and make it possible to be continually scaled to the next generation of transistors to meet increasing performance goals. In keeping with this trend, Intel recently announced that high-κ gate dielectric combined with the metal gate electrodes would be applied in its 45 nm process node to reduce the gate leakage current at least 100 times [10].

1.3 Ideal MOS structure

The building block of CPU is the MOSFET, whose structure is shown in Fig 1.3. The gate oxide separates gate electrode from the conduction channel in silicon substrate. Although aluminum was initially used as gate electrode, it was replaced by polycrystalline silicon in modern CMOS technology due to the advantage of the self-aligned polysilicon gate process. Polysilicon can be highly doped (different dopants for NMOS or PMOS) to increase the conductivity.



(a)

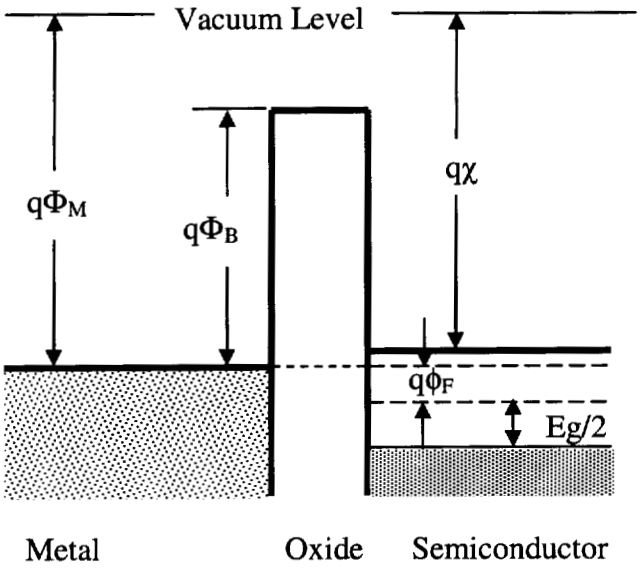


(b)

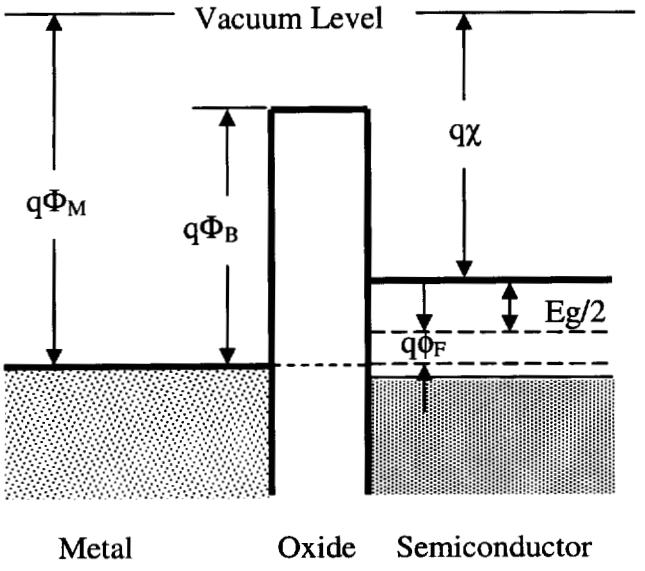
Figure 1.3: Schematic illustration of MOSFET structure. (a) Cross-section of a MOSFET (b) MOS gate stack structure.

Since the gate oxide is the middle layer of the gate sandwich structure, the interface with either gate electrode or silicon substrate are particularly important for device performance. The upper interface can be engineered to block Boron outdiffusion from P^+ gate electrode. The lower interface must be engineered to reduce interface trap densities and minimize carrier scattering (maximize carrier mobility) to enhance device performance. These two interfaces also contribute to the gate capacitance if their thicknesses are comparable to the thickness of gate dielectric.

The energy band diagram of an ideal MOS is illustrated in Fig 1.4. For ideal MOS, there are no charges within the oxide as well as on its two interfaces. When there is no gate voltage applied, ideally, the work function difference $q\Phi_{MS}$ between the metal gate and the semiconductor is zero.



a.) n type



b.) p type

Figure 1.4: Energy band diagram of an ideal MOS capacitor at no gate bias

$$q\Phi_{MS} = q\Phi_M - q(\chi + E_g/2q - \phi_F) = 0, \qquad \text{n-type} \qquad (1.5)$$

$$q\Phi_{MS} = q\Phi_M - q(\chi + E_g/2q + \phi_F) = 0, \qquad \text{p-type} \qquad (1.6)$$

where $q\Phi_M$ is the work function of the metal, χ the semiconductor electron affinity, E_g the energy bandgap, ϕ_F potential difference between Fermi level E_F and the intrinsic Fermi level E_i, Φ_B the potential barrier between the metal and the gate dielectric. Since the Fermi energy is flat across the dielectric, voltage of the band is called flat band voltage (V_{FB}). This voltage is usually not zero due to the trapped charges in the oxide. In the SiO_2-Si system, there are four types of defect charges classified with respect to their location, as displayed in fig 1.5.

a.) Mobile ionic charge Q_m. This is caused primarily by ionic impurities, such as Na^+, K^+ and H^+, which are mobile within the oxide.

b.) Oxide trapped charge Q_{ot}. This charge distributed in the oxide may be positive or negative. Trapping may result from the radiation, hot-carrier injection and Fowler-Nordheim tunneling.

c.) Fixed charge Q_f. It is a positive charge located in the oxide layer less than 2 nm from the SiO_2-Si interface, due to structure defects. This charge is related to the oxide deposition process and can be minimized by low-temperature hydrogen or forming gas anneal. There is no electrical communication with the channel in silicon

d.) Interface trapped charge Q_{it}. This is positive or negative charge, which is located at the SiO_2-Si interface. It is caused by the oxidation process (dangling bond). Interface trapped charge can be charged or discharged and electrically communicates with underlying channel in silicon. It may be neutralized by the low-temperature hydrogen or forming gas anneal.

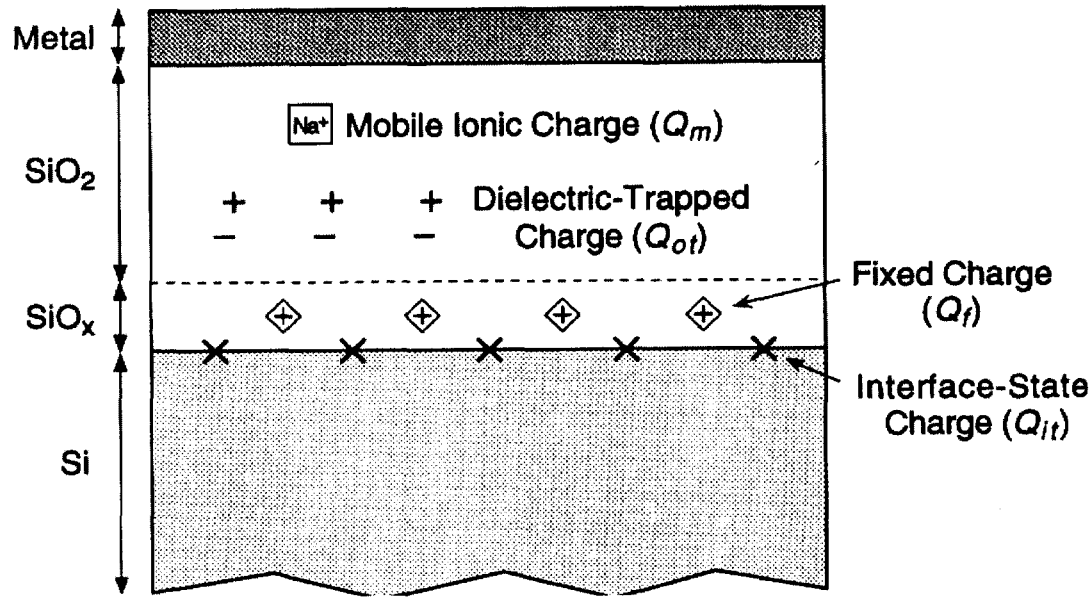


Figure 1.5: Four types of defect charges associated with thermally grown SiO_2. [11]

1.4 Summary

Continued scaling of CMOS devices is demanding alternate gate dielectric to replace SiO_2. Any new materials need perspective characterization before they are introduced into the present CMOS process. In chapter 2, the identification of suitable alternate gate dielectrics is discussed first. In chapter 3, the theoretical background on dielectric polarization mechanisms is reviewed, which is the basic principles to explain the electrical behavior of dielectric materials. DC and high-frequency characterizations of high-κ gate dielectrics are explored in chapter 4 and 5, respectively. At last, chapter 6 presents two undesirable effects of high-κ gate dielectrics: mobility reduction and dielectric relaxation.

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CHAPTER 2: ALTERNATE HIGH-κ GATE DIELECTRICS

To reduce the gate leakage current and improve gate capacitance, it will be necessary to introduce a high-κ gate dielectric to the CMOS process for 65 nm technology node and beyond as a replacement for SiO_2. Due to the superior properties of SiO_2, it is a grand challenge to find a suitable high-κ gate dielectric. There are a number of issues that must be simulatiously addressed: (1) The thermodynamic stability in contact with silicon, (2) High dielectric constant and band offsets for carrier transport, (3) High quality interface, (4) Gate electrode compatibility, (5) Process integration, and (6) Reliability.

2.1 Thermodynamic stability in contact with silicon

At a first glance, there are a lot of dielectrics with $\kappa > 3.9$. However, most dielectrics are not thermodynamically stable in direct contact with silicon. There is a thin layer formed at the interface between the gate oxide and Si substrate, which degrades the effect of high-κ dielectric. In the study of G.B. Alers et al.[1], the formation of a thin SiO_2 layer was observed at the Ta_2O_5/Si interface, as shown in Fig 2.1. The reaction between Si and Ta_2O_5 is [2]:

$$\frac{13}{2}Si + Ta_2O_5 \xrightarrow{\Delta G^{o}_{1000K}=-41.3332\,KJ/mol} 2TaSi_2 + \frac{5}{2}SiO_2 \qquad (2.1)$$

where ΔG^{o}_{1000K} is the standard Gibbs free energy difference between the products and reactants at 1000 K. The negative Gibbs free energy means the reaction is favorable at 1000K. Similar interface layers were confirmed in $SrTiO_3$ [3], Al_2O_3 [4] and ZrO_2 [5].

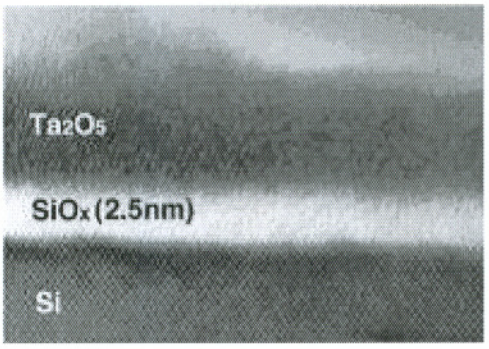

Figure 2.1: SEM image showing the formation of interface layer between Ta_2O_5 layer and silicon substrate.

The existence of an interface layer between silicon and these dielectrics eliminates them as alternate gate dielectrics unless a buffer layer is added in between. Consequently, the thermodynamic analysis is initially employed to eliminate unsuitable dielectrics from consideration and identify the best candidates for detailed study. The thermodynamic stability of binary oxides and nitrides of elements in the periodic table was comprehensively assessed by Darrell G. Schlom et al. [6-7]. Fig 2.2 shows that there are fewer nitrides than oxides that are thermodynamically stable in contact with Si. In addition, some nitrides are conductors. Of the binary nitrides that are stable (experimentally demonstrated) and potentially stable (insufficient thermodynamic data for calculation), and that are insulators, have dielectric constants that range from $\kappa = 5$ to $\kappa = 9$. In contrast to the binary nitrides, all of the remaining binary oxides are insulators with dielectric constants in the range from $\kappa = 4$ to $\kappa = 24$. Besides the consideration of thermodynamic stability on Si, some materials are piezoelectric or pyroelectric (potential piezoelectric), which are not desirable for gate dielectric application, for example, BeO, AlN, Si_3N_4, and Ge_3N_4. Therefore, the binary oxides appear more promising than nitrides as alternate gate dielectric materials.

It is also noticeable that there are some ternary oxides which are thermodynamically stable and could have high dielectric constants, such as $LaAlO_3$. They are usually comprised of silicon-compatible binary oxide constituents and have superior property than that of binary oxides. Due to insufficient thermodynamic data to evaluate these ternary oxides, further experiment demonstration will be necessary.

1 IA												13 IIIA	14 IVA	15 VA	16 VIA	17 VIIA	18 VIIIA
1 H 1.008	2 IIA																2 He 4.003
3 *Li* 6.941	4 **Be** 9.012											5 B 10.81	6 C 12.01	7 N 14.01	8 O 16	9 F 19	10 Ne 20.18
11 Na 22.99	12 **Mg** 24.31	3 IIIB	4 IVB	5 VB	6 VIB	7 VIIB	8	9	10	11 IB	12 IIB	13 **Al** 26.98	14 **Si** 28.09	15 P 30.97	16 S 32.07	17 Cl 35.45	18 Ar 39.95
19 K 39.1	20 **Ca** 40.08	21 *Sc* 44.96	22 Ti 47.88	23 V 50.94	24 Cr 52	25 Mn 54.94	26 Fe 55.85	27 Co 58.47	28 Ni 58.69	29 Cu 63.55	30 Zn 65.39	31 Ga 69.72	32 Ge 72.59	33 As 74.92	34 Se 78.96	35 Br 79.9	36 Kr 83.8
37 Rb 85.47	38 **Sr** 87.62	39 **Y** 88.91	40 **Zr** 91.22	41 Nb 92.91	42 Mo 95.94	43 Tc -98	44 Ru 101.1	45 Rh 102.9	46 Pd 106.4	47 Ag 107.9	48 Cd 112.4	49 In 114.8	50 Sn 118.7	51 Sb 121.8	52 Te 127.6	53 I 126.9	54 Xe 131.3
55 Cs 132.9	56 Ba 137.3	*	72 **Hf** 178.5	73 Ta 180.9	74 W 183.9	75 Re 186.2	76 Os 190.2	77 Ir 190.2	78 Pt 195.1	79 Au 197	80 Hg 200.5	81 Tl 204.4	82 Pb 207.2	83 Bi 209	84 Po -210	85 At -210	86 Rn -222
87 Fr -223	88 Ra -226	**	104 Rf -257	105 Db -260	106 Sg -263	107 Bh -262	108 Hs -265	109 Mt -266									

*	57 **La** 138.9	58 **Ce** 140.1	59 **Pr** 140.9	60 **Nd** 144.2	61 Pm -147	62 *Sm* 150.4	63 *Eu* 152	64 **Gd** 157.3	65 *Tb* 158.9	66 *Dy* 162.5	67 *Ho* 164.9	68 *Er* 167.3	69 *Tm* 168.9	70 *Yb* 173	71 *Lu* 175
**	89 Ac~ -227	90 Th 232	91 Pa -231	92 U -238	93 Np -237	94 Pu -242	95 Am -243	96 Cm -247	97 Bk -247	98 Cf -249	99 Es -254	100 Fm -253	101 Md -256	102 No -254	103 Lr -257

Thermodynamicically unstable with silicon at 1000K
Experimentally demonstrated
Insufficient thermodynamic data to complete calculation

(a) Metal oxide (M_xO_y) may be thermodynamically stable in contact with silicon at 1000K.

1 IA																	18 VIIIA
1 H 1.008	2 IIA											13 IIIA	14 IVA	15 VA	16 VIA	17 VIIA	2 He 4.003
3 Li 6.941	4 *Be* 9.012											5 **B** 10.81	6 C 12.01	7 N 14.01	8 O 16	9 F 19	10 Ne 20.18
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19 K 39.1	20 Ca 40.08	21 **Sc** 44.96	22 **Ti** 47.88	23 V 50.94	24 Cr 52	25 Mn 54.94	26 Fe 55.85	27 Co 58.47	28 Ni 58.69	29 Cu 63.55	30 Zn 65.39	31 Ga 69.72	32 *Ge* 72.59	33 As 74.92	34 Se 78.96	35 Br 79.9	36 Kr 83.8
37 Rb 85.47	38 Sr 87.62	39 Y 88.91	40 **Zr** 91.22	41 Nb 92.91	42 Mo 95.94	43 Tc -98	44 Ru 101.1	45 Rh 102.9	46 Pd 106.4	47 Ag 107.9	48 Cd 112.4	49 In 114.8	50 Sn 118.7	51 Sb 121.8	52 Te 127.6	53 I 126.9	54 Xe 131.3
55 Cs 132.9	56 Ba 137.3	*	72 **Hf** 178.5	73 Ta 180.9	74 **W** 183.9	75 Re 186.2	76 Os 190.2	77 Ir 190.2	78 Pt 195.1	79 Au 197	80 Hg 200.5	81 Tl 204.4	82 Pb 207.2	83 Bi 209	84 Po -210	85 At -210	86 Rn -222
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**	89 Ac~ -227	90 Th 232	91 Pa -231	92 U -238	93 Np -237	94 Pu -242	95 Am -243	96 Cm -247	97 Bk -247	98 Cf -249	99 Es -254	100 Fm -253	101 Md -256	102 No -254	103 Lr -257

Thermodynamicically unstable with silicon at 1000K
Experimentally demonstrated
Insufficient thermodynamic data to complete calculation

(b) Metal nitride (M_xN_y) may be thermodynamically stable in contact with silicon at 1000K.

Figure 2.2: Summary of Si-compatible metal binary oxides and nitrides. The shaded elements are thermodynamically unstable in contact with Si under conventional CMOS processing conditions.

2.2 High dielectric constant κ and band offsets for carrier transport

The gate structure can affect the effective gate dielectric constant. Fig 2.3 schematically displays two gate structures: single layer and stacked gate dielectrics. In case A, there is one single high-κ dielectric layer and thickness $t_{high\text{-}\kappa}$. Here one term t_{eq} is introduced to represent the equivalent oxide thickness (EOT) of SiO_2 that could be required to achieve the same capacitance density as SiO_2. t_{eq} can be represented by

$$t_{eq} = \frac{K_{SiO_2}}{K_{high-\kappa}} t_{high-\kappa} \tag{2.2}$$

In case B, the upper layer is high-κ layer, the lower layer is an interface layer (usually SiO_2). Thus, the total capacitance of the stack dielectric is given by

$$\frac{1}{C_{tot}} = \frac{1}{C_1} + \frac{1}{C_2} \tag{2.3}$$

where C_1 and C_2 are the capacitances of the upper and lower layer, respectively. The equivalent oxide thickness of the stack dielectric is simplified to

$$t_{eq} = \frac{K_{SiO_2}}{K_{high-\kappa}} t_{high-\kappa} + t_{SiO_2} \tag{2.4}$$

It is clear from equation 2.4 that the minimum achievable equivalent oxide thickness is limited by that of the SiO_2 layer. The existence of low-κ layer will reduce the total capacitance of gate stack capacitance. Therefore, the low-κ layer dominates the overall capacitance and sets a limit on the minimum achievable t_{eq}. The main benefit of intentionally or unintentionally using SiO_2 as the lower layer of gate stack is that the unparalleled quality of the SiO_2-Si interface is helpful to maintain a high channel carrier mobility.

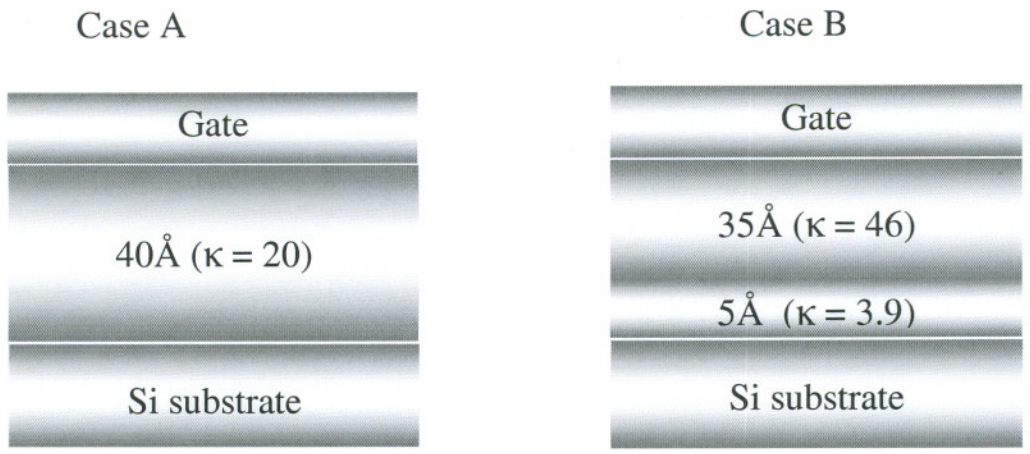

Figure 2.3: Schematic illustration of gate structures. Case A is a single-layer dielectric, and case B is stacked gate dielectric with an interfacial layer SiO_2

The example in Fig 2.3 is also used to illustrate the effect of gate stack structure on equivalent oxide thickness. To get t_{eq} = 8 Å, thickness of the dielectric with $\kappa = 20$ can be 40 Å by calculation from equation 2.2. In case B, if the thickness of interfacial layer SiO_2 is 5 Å, the dielectric with $\kappa = 46$ (from equation 2.4) has to be used to get the same t_{eq} without changing the total gate thickness. It means that a higher dielectric constant material has to be used in the gate stack structure compared to the single gate dielectric. In addition, the quality of dielectric-dielectric interface needs serious consideration.

Although the thicker gate oxide with the high dielectric constant may prevent the direct tunneling across the gate dielectric, the conduction can still occur by the excitation of electrons or holes to the oxide. As shown in Fig 1.4, for an electron transferring from Si substrate to the gate, it is governed by the conduction band (CB) offset $\Delta E_C = q[\chi-(\Phi_M - \Phi_B)]$. For an electron transferring from gate to Si substrate, it is governed by the energy barrier Φ_B between gate electrode and oxide. In order to get the low leakage current, the oxide's valence and conduction bands with respect to Si and gate electrode must be both high. It will likely preclude using the high κ oxides with band offsets less than 1 eV in

gate dielectric application. The band offsets can be determined by photoemission spectroscopy [8] or deep-level transient spectroscopy [9]. Due to availability of a few experimental measurements on band offset, some calculated band offsets with respect to Si were reported by John Robertson et al [10]. The calculated barrier heights of oxides are given in Table 2.1 and shown schematically in Fig 2.4. The experimental band offsets of SiO_2 and Si_3N_4 on Si are included for completeness [11]. Some values agree well with the experimental values [12-14]. The oxides of La, Y, Hf, Zr, and Al have conduction band offsets of >1 eV. In the absence of the value of band offset, the energy bandgap can be used as a reference to predict the relevant barrier height. A large bandgap generally implies a large band offset. The energy bandgap stipulated by ITRS [15] is at least 4 eV, and preferably > 5 eV for new technology nodes.

Table 2.1: Comparison of potential high-κ candidates.

Material	κ	Band gap E_g (eV)	ΔEc (eV) to Si	E_{BD} (MV/cm)
SiO_2	3.9	8.9	3.2	15
Si_3N_4	5-7	5.1	2	10-11
Al_2O_3	9-11	8.7	2.8	10
Y_2O_3	15	5.6	2.3	5
La_2O_3	30	4.3	2.3	--
Ta_2O_5	26	4.5	1-1.5	4
TiO_2	80-100	3.5	1.2	0.5
HfO_2	22-25	5.7	1.5	15
ZrO_2	22-25	7.8	1.4	15

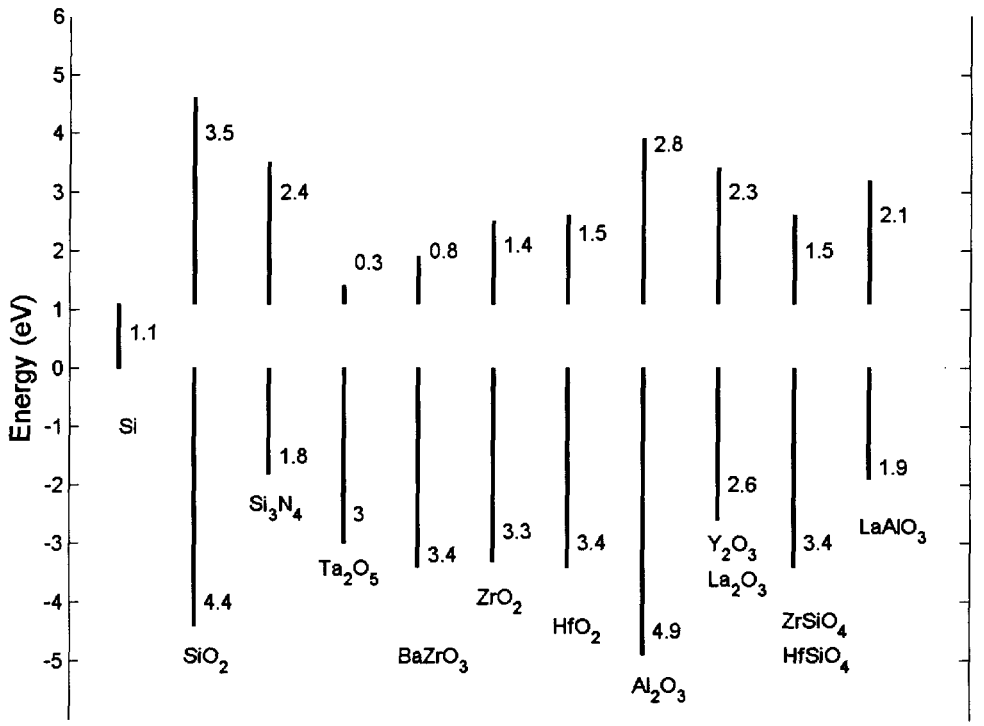

Figure 2.4: Calculated band offsets of oxides on Si.

From the fig 2.4, it is obvious that band offsets for most transition metal oxides are quite asymmetric. The barrier heights of the electrons are much less than that of the holes. Therefore, the electron travel is the major cause of the leakage. Some methods of increasing the conduction band offsets are discussed by John Robertson [16]. It is notable that the dielectric constant and band gap of a given material usually exhibit an inverse relationship as shown in Fig 2.5. The selection of high-κ gate dielectric has to be a trade-off between dielectric constant and band gap.

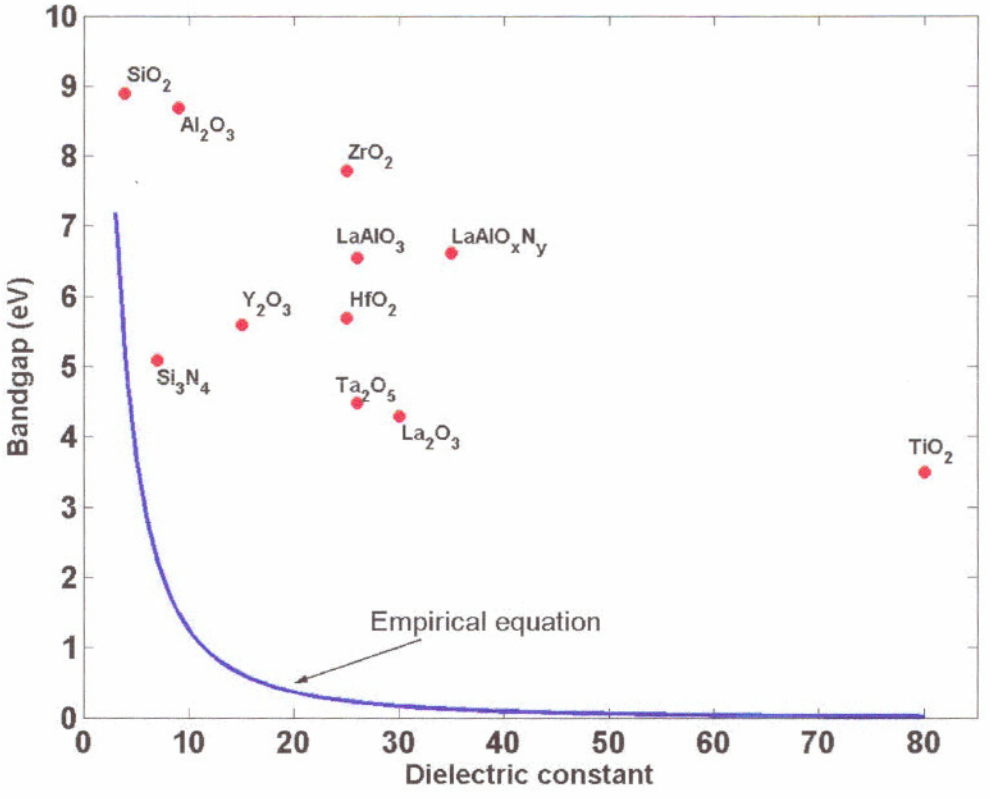

Figure 2.5: Plot of dielectric constant κ versus optical bandgap E_g for oxides. Empirical equation proposed by J. A. Duffy shows that dielectric constant varies roughly inversely with bandgap.

2.3 High quality interface

As schematically illustrated in Fig1.3, the gate dielectric has two interfaces. For the lower Si-dielectric interface, it has a very strong influence on the MOS channel mobility and drive current of CMOS devices. For the upper metal-dielectric interface, it has a great effect on the capacitance equivalent thickness (CET) as well as impurities (such as oxygen or boron) penetration through gate dielectric. These two interfaces should be smooth enough to reduce the charge scattering [17]. Compared to SiO_2, the high-κ materials tend to produce unfavorable bonding condition with Si and lead to

formation of a high defect density near the Si-dielectric interface, resulting in poor electric properties. The classic SiO_2 gate dielectric has a high quality interface with the Si channel, i.e. low interface state density (~ 10^{10} states/cm^2) and flatband shift. There is no high-κ dielectric with similar interface quality as SiO_2 on silicon. It was reported that ZrO_2 and HfO_2 had high oxygen diffusivity [18]. Oxygen penetrates the thin gate dielectric and forms an undesired SiO_2 thin layer at the Si-dielectric interface. Some post deposition anneal processes in oxygen-rich ambient may also expedite the oxygen diffusion through gate dielectric and result in SiO_x-containing interface. The uncontrolled amount of SiO_2 formation at the interface will severely compromise the capacitance gain from the high-κ layers in the gate stack system. Hence, an understanding and control of interfacial oxide growth has become critical to high-κ as gate dielectric application. It has also been found that the Al-containing interfacial layer exhibits extreme charge-related issues resulting in unacceptable performance in both threshold voltage control and channel carrier mobility.

The silicate reaction may occur for any metal-Si bonding condition. Silicate formation at the Si-dielectric interface will also lead to poor leakage current and electron carrier mobility. When polycrystalline silicon is used for gate electrode, the oxidation or silicate reactions discussed above may take place at the metal-dielectric interface. This interfacial layer, however, does increase EOT. Steps are taken to passivate the upper interface and reduce the boron penetration in some cases. Quevedo-Lopez et al. reported that the incorporation of N could prevent the formation of an interfacial layer and improved Si surface quality [19-20].

The work by W. Tsai et al. [21] proposed that heterogeneous island growth of high-κ materials was observed on H-terminated Si, whereas uniform high-κ film growth on OH-terminated Si. Thus, the surface clean and subsequent surface conditioning prior to high-κ deposition is critical for the Si-high-κ interface as it directly influences the growth morphology of the high-κ film.

Based on the above description, the ideal gate dielectric stack system may turn out to have a Si-O bonding structure at the channel interface. This several-monolayer-

interface could serve as a replacement for the high quality SiO_2 interface and preserve the high value of dielectric constant in the whole gate stack system.

2.4 Gate electrode compatibility

In gate stack engineering, not only the high-κ gate dielectric is considered as a replacement of the standard silicon dioxide gate dielectric, but also gate materials have to be incorporated to replace the polysilicon (poly-Si) electrode. Poly-Si gate can be tuned by different types of dopant implantation to create the desired threshold voltage V_T for both NMOS and PMOS. As silicon CMOS devices are scaled below 100 nm gate length node, poly-Si gate presents many restricting factors, such as, poly-Si gate depletion, high gate resistance, and boron penetration into the channel region etc. In contrast, metal gates are very desirable for eliminating poly-Si dopant depletion effects and sheet resistance constraints. Naturally, new gate materials have to meet several requirements, for example, thermal stability of the gate itself, proper work function with both NMOS and PMOS channels, material compatibility and integration with the CMOS process flow. Extensive work has been done on various materials and material combinations [22-25] in order to find a suitable metal gate to fulfill the desired properties.

Gate electrodes can be implemented with a single midgap metal or dual metal gates that are close to band edges of Si. The energy band diagrams associated with those two approaches are schematically displayed on Fig 2.6. Midgap gates (e.g., TiN, W) are inadequate for advanced Si-based CMOS devices due to large threshold voltage V_T and severe short-channel effects at the sub-100 nm technology node [26]. Additionally, the work function of TiN depends not only on the deposition method [27], but also on the annealing condition [28]. The classic device simulations by Indranil De [29] suggests that gate Fermi level should be 0.2 eV below (above) the conduction (valence) band edge of silicon for NMOS (PMOS) devices. In other words, the metal gate has to have a work function close to 4 eV and 5 eV for NMOS and PMOS, respectively. It is observed that

the metal work functions on high-κ dielectrics may differ appreciably from their values on SiO_2 or in a vacuum [30].

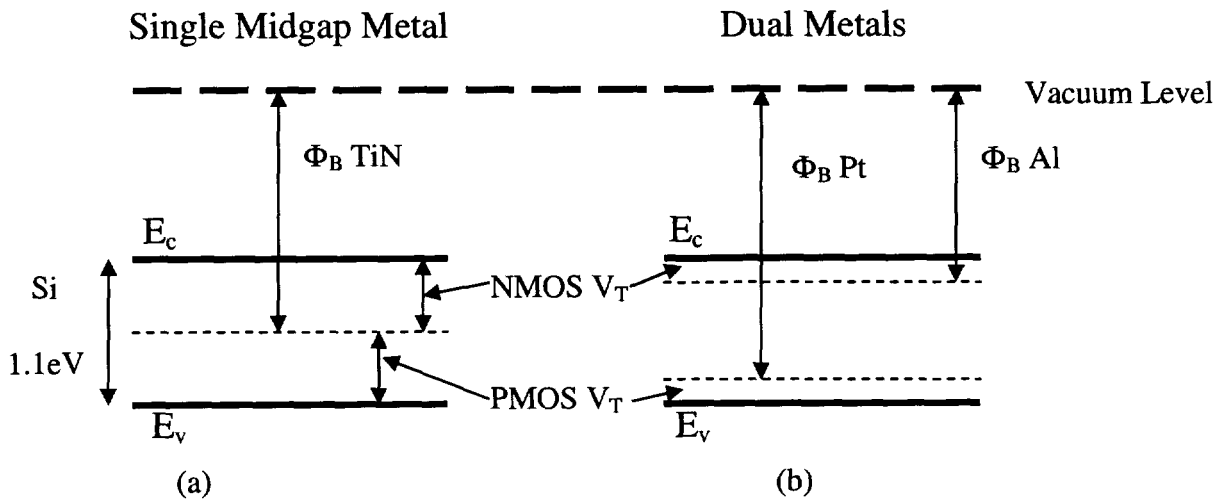

Figure 2.6: Energy diagrams of threshold voltages for NMOS and PMOS devices using (a)midgap metal gates and (b) dual metal gates

The thermal stability issue does exist at the metal-dielectric interface. Metal-dielectric interfaces have been investigated using approaches similar to those employed for the Si-dielectric interface. Fillot et al. [31] evaluated the thermal stability of metal on HfO_2 gate dielectric by thermodynamic calculation and X-ray reflectometry with the reflectometry results correlated with atomic force microscopy (AFM) and transmission electron microscopy (TEM) observations. This study showed that platinum, palladium and nickel were highly stable on HfO_2 gate dielectric. Whereas, the aluminium, niobium and titanium presented a critical stability issue on HfO_2 by forming interfacial layer and diffused interface. Besides the elemental metals, some conducting metal oxides are also attracting more attention, for example, IrO_2 and RuO_2. H. Zhong et al. [32-34] have reported thermal stability of RuO_2 up to 800 °C, low resistivity of 65 μΩ•cm, and a measured work function of 5.1 eV for PMOS. They further showed that use of binary

Ru-Ta alloys offered workfunction-tuning opportunities that could provide both NMOS and PMOS compatible work functions [35].

2.5 Process integration

For the alternate gate dielectric, it is important to ensure that the deposition process for the dielectric is fully compatible with current CMOS processing, cost and throughput. At the same time, there can be no deleterious impact upon transistor performance, such as, channel mobility, threshold voltage and lifetime. In general, the high-κ integration issues include deposition techniques, film microstructure, chemical stability under the process conditions [36], and high-κ film removal quandary.

2.5.1 Deposition techniques

The present SiO_2 gate dielectric is thermally grown in a furnace or rapid-thermal-processing reactor. With the alternate gate dielectric, an appropriate deposition method needs to be chosen to get the desired properties. The line-of-sight physical vapor deposition (PVD) approaches are first ruled out due to potential radiation or ion-induced damage to the dielectrics. The possible choice may be chemical vapor deposition (CVD) in one of its variations, such as metalorganic CVD (MOCVD), atomic layer CVD (ALCVD), rapid thermal CVD. These techniques offer a number of benefits, such as good uniformity and thickness control, reasonable wafer throughput, and compatibility with 300 nm wafer processing. ALCVD method appears more promising because of its well-controlled surface saturating process and precise control of the dielectric composition at atomic level. For the more complex metal oxide dielectrics, with potentially higher κ-values, which are not easily accessible by ALCVD at the present

time, molecular beam epitaxy (MBE) could be an alternative technique. However, MBE could also be limited by its poor throughput in the manufacturing environment.

As discussed before, the surface preparation prior to high-κ deposition is critical in gate stack fabrication. W. Tsai et al [37-38] studied three types of Si surface termination prior to high-κ deposition to evaluate the effects on the morphology and electrical characteristics of high-κ dielectrics. Poor nucleation characteristic was also observed on H-terminated Si by M. Copel [39], whereas there was no problem on OH-terminated Si.

2.5.2 Film microstructure

There are three microstructures for gate dielectrics: amorphous, polycrystalline and epitaxial. The conventional SiO_2 gate dielectric remains in amorphous state at high temperatures. Unlike SiO_2, very few high-κ dielectrics have the resistance to crystallization displayed by SiO_2. Most high-κ dielectrics undergo phase transformation from amorphous to polycrystalline at relatively low temperatures. For example, HfO_2 has a crystallization temperature ~ 650 °C. The application of polycrystalline gate dielectric is probably limited by interfacial roughness and defects associated with grain boundaries. Interfacial roughness may reduce carrier mobility through charge scattering [40]. It is also well-known that the grain boundaries serve as high leakage paths. In contrast, amorphous structure may exhibit isotropic electric properties without suffering from grain boundaries. Therefore, amorphous film structure appears to be an ideal one for gate dielectrics application. This is one virtue of SiO_2. Epitaxial single crystal dielectrics have also been considered by virtue of avoiding grain boundaries and providing a good interface. However, the MBE approach is limited by its low throughput. The further research on epitaxial dielectrics is required.

2.5.3 Chemical stability under the process conditions

The gate dielectric is formed at the early stages of a CMOS process. The primary concern in regard to the chemical stability of gate dielectric on silicon is the subsequent thermal processing conditions that the dielectric stack must tolerate after deposition. One step from a typical CMOS process flow is the rapid thermal anneal used to activate the dopant in source and drain regions. A typical anneal temperature is around 1000 °C. The gate dielectric must not undergo deleterious reactions with silicon under the anneal conditions. The amorphous structure must not crystallize. Any diffusion of the metal element into the silicon channel or gate electrode (i.e. polysilicon gate) is undesirable, as it could severely damage the interface and reduce the charge carrier mobility by scattering.

2.5.4 High-κ film removal quandary

Most high-k materials are resistant to the chemistries used for SiO_2 gate dielectric. It is a grand challenge to find the chemistries and processes that remove high-κ films without gate, source or drain damage. For hafnium-based materials, high temperatures are needed to etch the $Hf_xSi_yO_z$, and HfO_2 films still do not etch well. Some people are considering use of a combination of dry plasma etch followed by a wet etch. Others are thinking about damascene-type gate to avoid depositing high-κ materials directly over the source/drain area.

2.6 Reliability

The introduction of high-κ dielectric favors reduction of the gate leakage current. However, there are reliability issues that need to be addressed, such as, charge trapping [41], threshold/flatband voltage shift with respect to SiO_2 dielectric [42], and dielectric breakdown property. The high-κ dielectrics, unlike SiO_2, exhibit significant charge trapping. Both electron and hole trapping have been observed in high-κ materials, i.e. ZrO_2 and TiO_2, [43]. Understanding charge trapping is one of the most important issues for successful optimization of high-κ dielectrics. Charge trapping can be reduced with process optimization.

Flatband voltage shift can be compensated by interface engineering. Whereas V_T shift is believed to be related to charges in the high-κ layer. Charge trapping also causes V_T to shift with time under a gate bias. The work of S. Zafar et al. [44] reported charge trapping characteristics of both Al_2O_3 and HfO_2 dielectrics. The threshold voltage shift was attributed to the trapping of charges in the existing traps without the creation of new traps. Similar results were obtained by L. Pantisano et al. [45], who showed that V_T instability in stacked high-κ dielectrics was caused by charging/discharging of HfO_2 film defects, independent of the HfO_2 thickness. S. Ramanathan et al. [46] also found that charge trapping did depend on deposition method of gate electrode, likely due to exposure of the high-κ dielectric to ambient prior to gate electrode deposition. The V_T shift problem is more severe with hafnium oxide than with hafnium silicon oxynitrides or hafnium silicate dielectrics, according to a study at IMEC (Leuven, Belgium).

In addition, one should point out that most high-κ dielectrics show lower breakdown electric field with respect to conventional SiO_2 dielectric.

In summary, the introduction of high-κ gate dielectric gives rise to new challenges on reliability: fixed charge elimination, suppression of charge trapping, mobility improvement, and interfacial layer reduction.

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CHAPTER 3: DIELECTRIC POLARIZATION

The dielectric materials have the property that their electrons, ions, or molecules become polarized under the influence of an external electric field. The dielectric constant is a material property. Some dielectric materials show low κ, whereas others show high κ. To understand the dielectric property, it is necessary to explore the polarization mechanism. In addition, ac dielectric constant is generally different from static case. The frequency dependence of dielectric constant will be discussed at the end of this chapter.

3.1 Polarization mechanism

The relative displacement of the positive and negative charges in matter is called dielectric polarization. Permanent polarization may exist in some materials even in the absence of an applied external electric field, for example, in ferroelectrics. However, most dielectric materials display polarization in an external electric field. Under the electric field, any separation between negative and positive charges of equal magnitude Q may lead to electric dipole moment P, which is defined by equation

$$P = Qa \tag{3.1}$$

where a is a displacement vector from the negative to the positive charge. This induced dipole moment is termed polarization. The electric dipole moment in a dielectric from its atomic and molecular structure may be caused from interfacial, dipolar, ionic or electronic polarization. The sum of the four polarization mechanisms contribute to the dielectric constant of the dielectric material.

3.1.1 Interfacial polarization

Interfacial polarization arises from the accumulation of charges at the interface. When mobile charges moves to one of the electrodes by external applied field, interfacial polarization occurs because of the existence of the dipole moment between mobile charges at the interface and immobile counterpart in the bulk, as explained in fig 3.1. The mobile charges can be mobile ions, trapping of electron or hole.

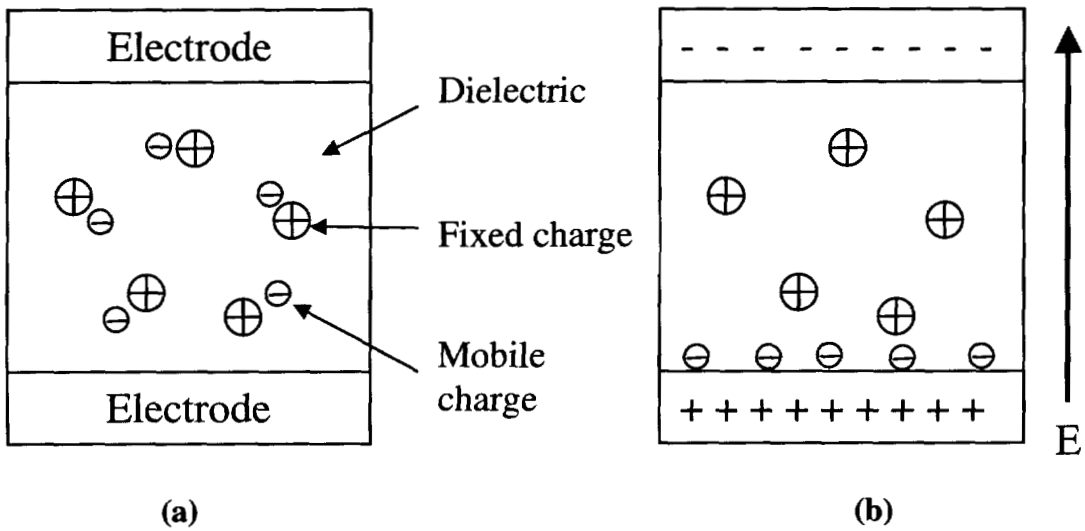


Figure 3.1: Interfacial polarization (a) In the absence of a field, there is no net separation between mobile negative charges and fixed positive charges in the dielectric (b) In the presence of a field, mobile negative charges move toward the positive electrode. There is a net separation between mobile charges and fixed charges in the dielectric.

3.1.2 Dipolar polarization

For molecules with permanent dipole moments, for example, HCl, the molecules are randomly oriented at thermal equilibrium in the absence of an electric field. Once external electric field is applied, the dipoles are forced to align themselves in the direction of the field so as to form the polarization. The molecules, however, may move around randomly and collide with each other under the influence of thermal vibrations. Thermal vibration can disturb the dipole alignments, but there always exist a net average dipole moment along the field, which displays a net polarization. This contribution to the dielectric constant is called as dipolar polarization, as shown in fig 3.2.

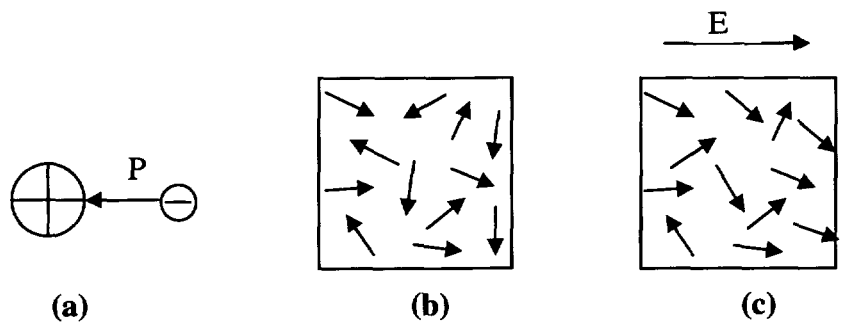


Figure 3.2: Dipolar polarization (a) One molecule with permanent dipole moment (b) In the absence of a field, dipole moments are randomly located without net dipolar moment (c) In the presence of a field, dipoles experience forces along the direction of the field, showing a net dipole moment.

3.1.3 Ionic polarization

For the materials with ionic crystals, such as NaCl, ions are located at well-defined crystal lattice sites. In the absence of electric field, there is no net polarization because positive dipole moment is equal to negative dipole moment, as schematically

displayed in fig 3.3. When an electric field is applied, the negative ions shift along the direction of the field and positive ions shift in an opposite direction. The net average dipole moment is produced by the displacement of the charges. This polarization has strong dependence of the electric field.

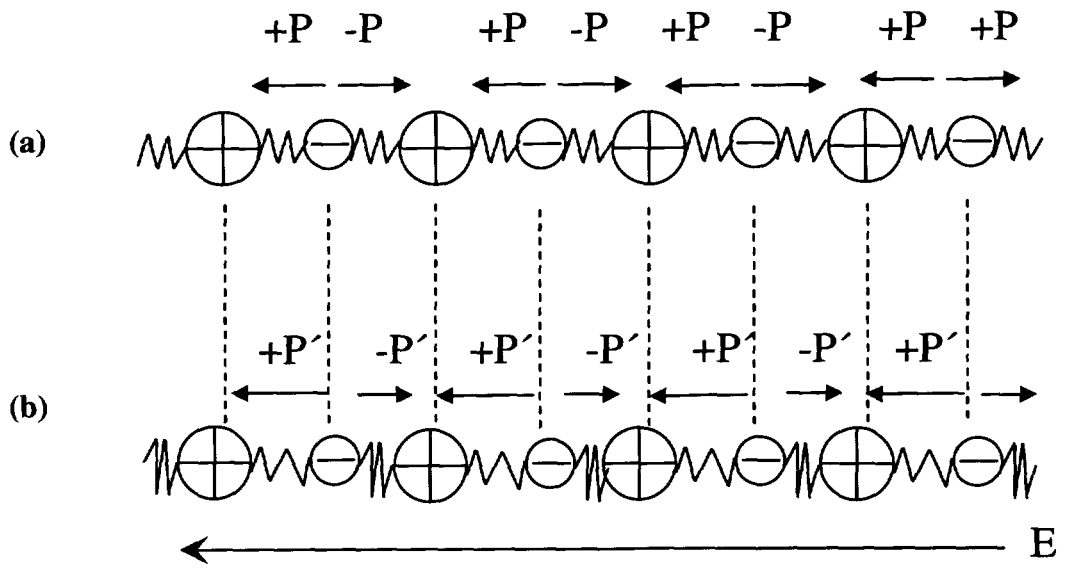


Figure 3.3: Ionic polarization (a) In the absence of electric field E, there is no net dipole moment (b) In the presence of an electric field E, there is net dipole moment.

3.1.4. Electronic polarization

The electronic charge is distributed in a spherically symmetrical manner around the nucleus so as to show no net polarization. If an electric field is applied to an atom, the positively charged nucleus tends to move in the direction of the electric field, while the electrons move in the opposite direction. In each atom, a slight displacement is created as depicted in fig 3.4. The amount of shift depends on the nature of the atomic forces and the electric field. The sum of the polarization of each atom contributes for the dielectric constant.

For covalent materials, the electrons are shared with neighboring atoms in covalent bonds, such as in Si atoms. These valence electrons are loosely tied to the ionic cores. Under the presence of an electric field, the distribution of the negative charges is readily shifted with respect to the positive charges associated with the ionic cores so as to exhibit polarization. This displacement of electrons in covalent bonds gives rise to electronic polarization, which is the main contribution to the large dielectric constants of covalent dielectrics.

(a) (b)

Figure 3.4: Electronic polarization (a) An initially unpolarized atom (b) A polarization of the atom develops.

3.2 Frequency dependence and dielectric loss

3.2.1 Frequency dependence of dielectric constant

The above discussed the dielectric polarization under an applied electric field. This electric field can be either dc or ac condition. The polarization under ac condition leads to an ac dielectric constant, which is of cause strongly frequency dependent. In dipolar polarization, if the field changes too fast, the dipoles can not follow the field so remain randomly oriented. Therefore, dipolar polarization has no contribution at high

frequency. Similarly, mobile charges can not respond to the field in interfacial polarization. Both ionic and electronic polarizations simultaneously contribute to the dielectric properties over a range of frequencies. In the infrared range, the inertial effects of the ionic displacements prevent the ions from responding fast enough. Ions are unable to contribute to the polarization at such high frequencies. Then, the dielectric properties become a function of just the electronic polarization.

3.2.2 Dielectric loss

In general, the dielectric constant can be written by the complex form as

$$\varepsilon_r = \varepsilon_r^{'}(\omega) - j\varepsilon_r^{''}(\omega) \tag{3.2}$$

where $\varepsilon_r^{'}$ is the real part and $\varepsilon_r^{''}$ is the imaginary part, both being frequency dependent. The real part determines the capacitance of a capacitor with this dielectric medium. The imaginary part determines the energy loss in the dielectric medium as a result of the polarization mechanisms. Consider a capacitor with the paralleled plates. The admittance Y can be represented as

$$Y = \frac{j\omega A\varepsilon_o\varepsilon_r(\omega)}{t} = \frac{j\omega A\varepsilon_o[\varepsilon_r^{'}(\omega) - j\varepsilon_r^{''}(\omega)]}{t}$$

$$= \frac{j\omega A\varepsilon_o\varepsilon_r^{'}(\omega)}{t} + \frac{\omega A\varepsilon_o\varepsilon_r^{''}(\omega)}{t} = j\omega C + G_p \tag{3.3}$$

where

$$C = \frac{A\varepsilon_o\varepsilon_r^{'}(\omega)}{t}$$

and

$$G_p = \frac{1}{R_p} = \frac{\omega A \varepsilon_o \varepsilon_r^{''}(\omega)}{t}$$

According to equation (3.3), the capacitor can be represented by a parallel circuit of an ideal capacitor C and a resistance of R_p as schematically displayed in fig 3.5.

Dielectric loss is the electrical energy lost in the polarization process under the influence of the applied ac field. The energy is absorbed from the ac voltage and converted to heat during the polarization of the molecules. Energy loss is determined by $\varepsilon_r^{''}$. Therefore, it is desired for $\varepsilon_r^{''}$ to be as small as possible for a given dielectric medium. The term loss tangent is defined by equation 3.4. It is evident that loss tangent is also frequency dependent.

$$\tan\delta = \frac{\varepsilon_r^{''}}{\varepsilon_r^{'}} = \frac{G_p}{\omega C} \tag{3.4}$$

The total polarization is the sum of the contributions from interfacial, dipolar, ionic and electronic polarizability. The dipolar polarizability arises from molecules with a permanent electric dipole moment that can change orientation in an applied electric field. The ionic contribution comes from the displacement of a charged ion with respect to other ions. The electronic contribution arises from the displacement of the electron distribution relative to a nucleus. Dielectric constant actually has a complex form as expressed by equation 3.2. The real part $\varepsilon_r^{'}$ determines the capacitance of capacitor, while the imaginary part $\varepsilon_r^{''}$ determines the dielectric loss. Both $\varepsilon_r^{'}$ and $\varepsilon_r^{''}$ are frequency dependent as shown in fig 3.6. $\varepsilon_r^{'}$ will be reduced as the frequency increases. The characterization of $\varepsilon_r^{'}$ and $\varepsilon_r^{''}$ will be presented in chapter 5.

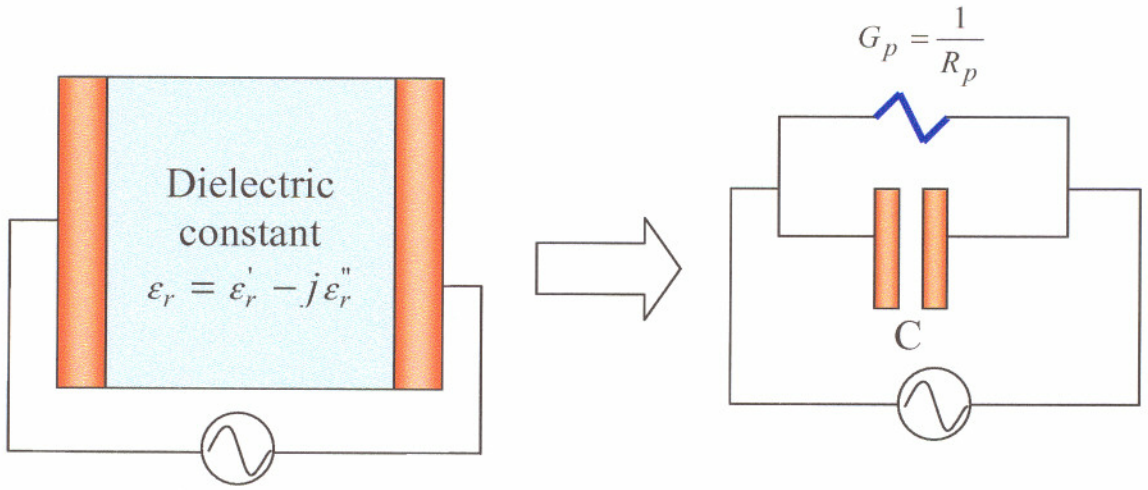


Figure 3.5: Capacitor behavior (a) AC signal applied on a capacitor (b) A capacitor can be represented with a lossless capacitor C in parallel with a conductance G_p.

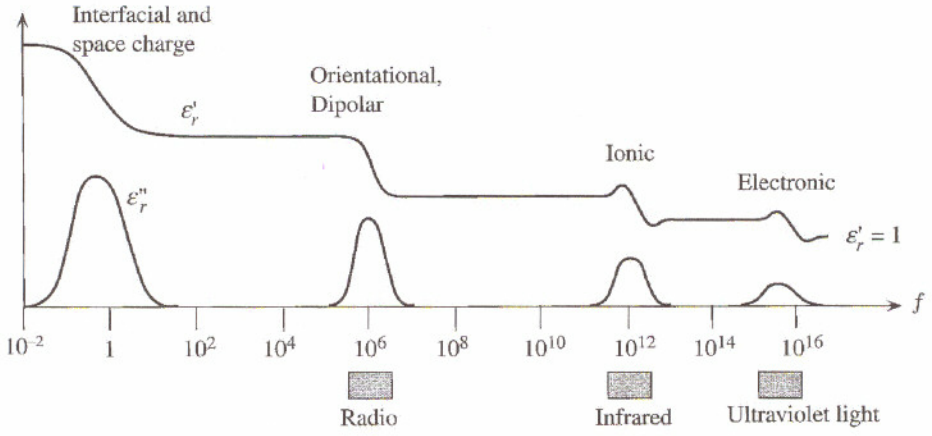


Figure 3.6: The frequency dependence of the real and imaginary parts of the dielectric constant under the several contributions to the polarizability.

CHAPTER 4: CHARACTERIZATION OF HIGH-κ MOS CAPACITORS

Many electrical measurements are developed to investigate fundamental device parameters for CMOS process technology, such as gate dielectric thickness, flatband voltage V_{FB}, interface trap density, etc [1]. The Metal-Oxide-Semiconductor Capacitor (MOS-C) is used extensively as a test structure to investigate the electrical properties of MOS devices and to monitor integrated-circuit fabrication process because it is simple to fabricate and well-established interpretation of the results. The most commonly used tools for studying MOS-C are the capacitance voltage (C-V) and current voltage (I-V) measurements. This chapter will develop the theory behind these measurements and discuss the measurement limitations for ultra-thin gate dielectric, followed by the electric characterization of MOS-C with high-κ dielectric.

4.1 Capacitance voltage analysis

A lot of information about an MOS device and the oxide-semiconductor interface can be obtained from C-V characterization of the device. The capacitance is measured by superimposing a small-amplitude ac signal on an applied dc gate voltage. The ac signal is necessary for capacitance measurement, while the dc voltage determines the bias condition. The measured capacitance is a function of the applied dc gate voltage. The ideal C-V characteristics of a p-type MOS-C are shown in fig 4.1, assuming that there is no charge trapped in the oxide and at the oxide-semiconductor interface. Since the C-V characteristics of n-type MOS-C are just a mirror of those of p-type, only p-type MOS-C is used for discussion.

It is evident that there are three regimes: accumulation, depletion and inversion. When a negative bias is applied to the gate, the majority carriers (holes) in the substrate are attracted toward the gate and accumulate at the oxide-substrate interface. The oxide

thickness can be extracted from the oxide capacitance in the strong accumulation region, where the capacitance is essentially constant. As the gate voltage moves toward positive values, the holes are repelled away from the oxide-substrate interface and form a depletion layer under the oxide until the maximum depth of the depletion layer is obtained. As a result, the measured capacitance is regarded as the sum of the oxide capacitance and the depletion capacitance in series. As the gate voltage increases beyond the threshold voltage, the minority carriers from thermal generation of electron-hole pairs drift to the oxide-substrate interface and form an inversion layer. For high frequency C-V measurement (HF-CV), the measured inversion-region capacitance at the maximum depletion depth is keeping constant minimum capacitance. While at the low frequency C-V measurement, the minority carriers from thermal generation get enough time to respond the ac voltage. The measured capacitance is just the oxide capacitance. Therefore, the inversion capacitance is frequency dependent. Typically, the high frequency characteristics of the MOS capacitor are measured.

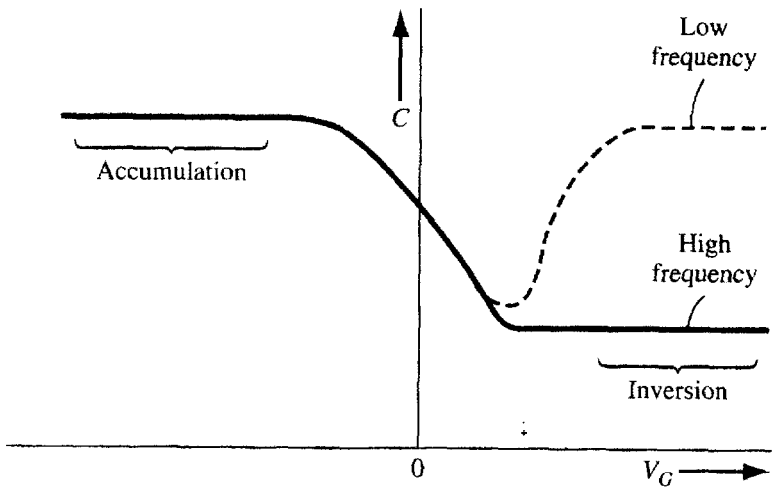


Figure 4.1: Typical low-frequency and high frequency capacitance versus gate voltage of an MOS capacitor with a p-type substrate.

4.1.1 Key requirements for successful C-V measurements

Besides compensating for stray capacitance from the cables and switch matrix, the measurement sequence and other parameters setting are critical to the success of C-V measurement. The most important C-V measurement requirement is to record data only under equilibrium conditions. The fully charged conditions are generally regarded as the equilibrium condition. There are two key parameters affecting the precision of measurement: hold time and delay time. After initially applying a voltage to a MOS-C, it is necessary to provide an adequate hold time before recording the capacitance. After each step of the gate voltage, an adequate delay time is allowed before recording the capacitance.

If the C-V sweep starts in the inversion region, an MOS-C is first driven into deep depletion after the voltage is initially applied on the gate. Then, if the starting voltage is maintained for a hold time, the HF-CV capacitance climbs and ultimately stabilizes at the minimum capacitance C_{min} at equilibrium. If the hold time is too short, the MOS-C can not adequately recover from deep depletion. The measured capacitance is a little lower than C_{min} at the equilibrium. Once the MOS-C has reached equilibrium after applying the initial bias, an inversion to accumulation measurement can be swept with relatively small delay times since the minority carriers recombine relatively quickly as the gate bias is reduced. However, if the delay time is too short (sweep is too fast), minority carriers do not have enough time to complete recombination. The measured capacitances are a little higher than equilibrium values in the inversion region as a result of nonequilibrium condition, which is illustrated as dash line in fig 4.2 [1]. When the measurement is swept from accumulation to inversion, if the delay time is too short (the sweep is too fast), there is not enough time for MOS-C to generate minority carriers to form inversion layer. Deep depletion occurs and the measured capacitances are lower than the equilibrium values, which is displayed as dotted line in fig 4.2. For high lifetime material, there is a tendency for HF-CV measurement to enter into deep depletion by sweeping the MOS-C

from accumulation to inversion. Therefore, the sweep direction from inversion to accumulation is preferred.

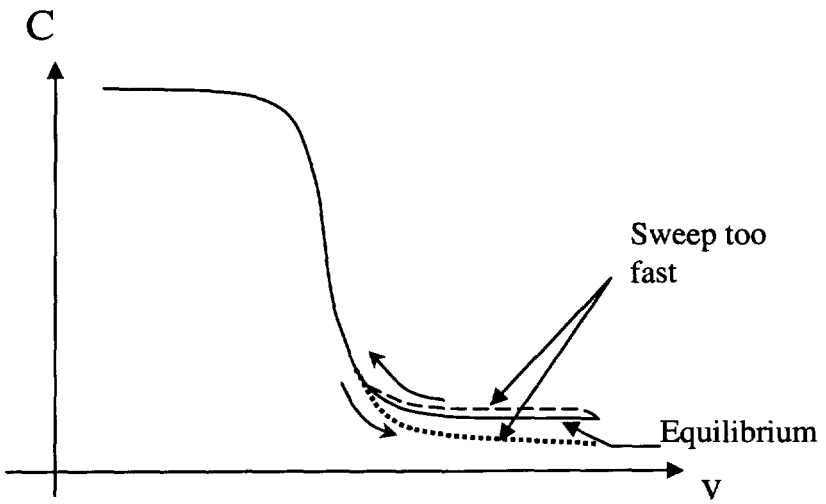


Figure 4.2: Effect of sweep rate and direction on the MOS-C HF-CV measurement.

4.1.2 Limitations of C-V measurement for ultra-thin dielectrics

When the dielectric thickness is reduced to below 15 Å, the capacitor becomes very lossy due to high leakage current. The C-V measurement may show roll-off effects in both the inversion and accumulation regions [2], as shown in fig 4.3. The effect of gate leakage in capacitance measurement can be represented by the dissipation factor (D). D can be expressed by

$$D = \frac{G_p}{\omega \bullet C_p} \tag{4.1}$$

where G_p and C_p are the measured conductance and capacitance respectively, which are as defined in equation 3.3. For an ideal capacitor without any parasitic, the value of D is zero. If tunneling conductance G_p is large due to high leakage current, then the dissipation factor D will be very large. Therefore, it is not unusually to see high D values

in capacitance measurement with ultra-thin gate dielectric. The roll-off effect in C-V curve may occur by virtue of high D. Since D is inversely proportional to frequency, a low frequency C-V measurement is not suitable for high leakage dielectric MOS-C. The approximate instrumentation error for LCR meters is given by equation 4.2 [3].A high measurement frequency is preferred for MOS device with ultra-thin gate dielectric.

$$\text{error } (\%) = 0.1\sqrt{1+(\frac{G_p}{\omega C_p})^2} \tag{4.2}$$

Besides the frequency, some non-optimized setups [4] may also cause high D and result in roll-offs in C-V measurement, for example, cabling calibration, shield connections, probe station setup, etc. The overall cable length in the system must be kept as close as possible to the calibration length of the LCR meter. If the cabling calibration length is shorter than the physical length, C-V curve rolls up. If the calibration length is longer than the physical length, the curve rolls off. The chuck can also couple into measurement and become obvious when D is high. To successfully perform C-V measurement, the above limitation factors should be carefully taken into consideration.

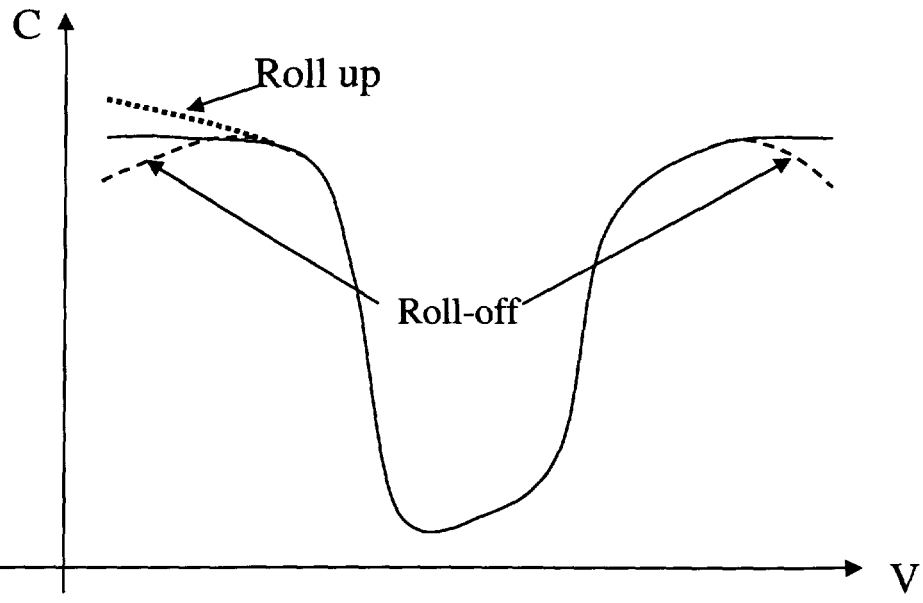


Figure 4.3: The capacitance attenuation in both accumulation and inversion regions in p-type MOS-C C-V measurement. Solid line indicates measurement under equilibrium, while dashed line denotes roll-off.

4.2 Experimental

For this investigation, the substrates are generally 5×5 cm^2 p-type silicon wafers. The silicon surface pretreatment was an organic clean followed by a 10% HF dip prior to loading into the deposition system. Some high-κ dielectrics, such as Al_2O_3, ZrO_2, HfO_2, or the laminate of above high-κ dielectric combination were deposited using the self-limiting growth process of ALD [5-6]. This method enables precise control of the film composition and thickness since the growth proceeds one monolayer at a time on an atomic scale.

The ALD reactor is made by the Finnish company Microchemistry Ltd [7]. After high-κ deposition, the wafers received a rapid thermal annealed (RTP) at 850 °C for 60 seconds in N_2, which had been shown to reduce the interface-state density. Circular geometry MOS capacitors were defined using a shadow mask. A 1000 Å layer of

platinum was then electron-beam evaporated by CHA system at Sharp Labs. This process formed a grid of circular MOS capacitors. After capacitor definition, the wafers experienced a forming gas anneal in N_2 / H_2 at 450 °C for 30 minutes.

The optical thickness of high-κ dielectrics were measured with an ellipsometer by Sentech Industruments GmbH, SE 800 series. C-V measurements were made using HP4284A precision LCR meter. The signal frequency was 1 MHz. To avoid nonlinear effects, a signal oscillation level of 25 mV was used. Measurements were made in parallel mode as illustrated in fig 3.5. Current-voltage (I-V) measurements were made using HP4156A precision semiconductor parameter analyzer.

4.3 The parameters extracted from C-V measurements

C-V measurements are a fundamental characterization technique for MOS devices. A large number of device parameters can be extracted from C-V curve. These parameters include oxide thickness, flatband voltage (V_{FB}), bulk doping concentration, and interface trap charge density etc. In this chapter, focus will be on the extraction of oxide thickness and flatband voltage.

4.3.1 Extracting the oxide thickness

4.3.1.1 From oxide capacitance (C_{ox}) at accumulation region

It is fairly simple to extract the oxide thickness for a relatively thick oxide (i.e. > 50 Å) film. In the strong accumulation region, C_{ox} acts like a parallel-plate capacitor, and the oxide thickness can be calculated from C_{ox} by equation 1.3. As the oxide thickness is reduced, the direct tunneling leakage current increases exponentially [8]. As a result, the

quasistatic capacitance measurements become difficult. A high frequency measurement has to be applied to overcome the leakage problem.

For low leakage device, the shunt resistance is very large so that the MOS capacitance can be obtained from a single measurement by ignoring the shunt resistance and determining the capacitance using the series circuit model in fig 4.4 (a). For ultra-thin oxides (i.e. < 20 Å) with large leakage currents, C-V measurement is modeled as parallel equivalent circuit as shown in fig 4.4 (b) [1]. This model neglects the series resistance. The actual equivalent circuit should be represented by fig 4.4 (c). At high frequency, the series resistance becomes dominant since the impedance of the capacitor is very low. Both the series and shunt parasitic resistance have to be taken into account in C-V measurement. Fig 4.5 shows the frequency-dependent capacitance with the optical oxide thickness of 1.7 nm by using parallel circuit model. This discrepancy of C_{ox} at accumulation region makes it difficult to extract oxide thickness.

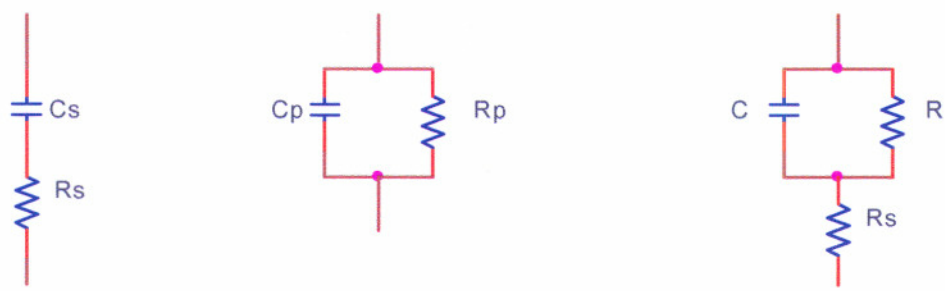


Figure 4.4: Small-signal equivalent circuit models of MOS capacitor: (a) series circuit model for low-leakage devices, (b) parallel circuit model for low series resistance devices, and (c) actual circuit environment.

4.3.1.2 From dual frequency C-V measurements

There are three elements in actual circuit environment. However, only two parameters (capacitance C_p and conductance G_p) can be determined from a single C-V measurement. To extract the true capacitance C in fig 4.4 (c), it is necessary to make two C-V measurements with two different frequencies. Equating the imaginary parts of the measured impedance (in fig 4.4 (a)) and the true impedance (in fig 4.4 (c)), one obtains

$$\frac{1+\omega^2 C^2 R^2}{CR^2} = \omega^2 C_p (1+D^2) \tag{4.3}$$

Measuring the capacitance C_p and dissipation factor D at two different frequencies, one can get

$$C = \frac{f_1^2 Cp_1^2 (1+D_1^2) - f_2^2 Cp_2^2 (1+D_2^2)}{f_1^2 - f_2^2} \tag{4.4}$$

where C_{p1} and D_1 refer to the values measured at the frequency f_1, and C_{p2} and D_2 refer to the values measured at the frequency f_2. With similar treatment of the real parts of the impedance, one can also obtain the shunt resistance R and series resistance Rs.

$$R = \frac{1}{\sqrt{\omega^2 C_p C(1+D^2) - \omega^2 C^2}} \tag{4.5}$$

and

$$R_s = \frac{D}{\omega C_p (1+D^2)} - \frac{R}{1+\omega^2 C^2 R^2} \tag{4.6}$$

Dual frequency C-V measurement may eliminate the frequency-dependent roll-off effect and get the corrected C_{ox} at accumulation region. Furthermore, accurate oxide thickness can be extracted from corrected C_{ox}. This corrected frequency-independent capacitance is shown in fig 4.6, which is using both data (50 kHz and 100 KHz) and data (100 KHz and 1MHz).

4.3.1.3 Quantum mechanic consideration

When the oxide thickness is scaled below 20 Å, the classic MOS-C models described above may not accurately reflect the capacitance of the MOS-C. Additional factors, such as quantum mechanical (QM) [9-11] confinement effects near the silicon surface, have to be considered. In general, the QM effects cause a reduced maximum capacitance resulting in an increase in the EOT. J.R. Hauser et al. [12] developed a NCSU CVC program, which includes quantum mechanical effects into the theoretical C-V model. Oxide thickness is estimated by fitting the C-V experiment data to a theoretical model using a nonlinear least squares technique, where oxide thickness, flatband voltage, and substrate doping density are used as the fitting parameters [13]. This program is applied to characterize the high frequency C-V curves for our MOS capacitors.

4.3.2 Extracting the flatband voltage

One way to determine the V_{FB} experimentally is to plot $1/(C_{hf})^2$ versus V_G, which. was proposed by R. J. Hillard et al. [14]. In the plot of the second derivative of the $1/(C_{hf})^2$ with respect to V_G versus V_G, the first peak location coincides with V_{FB}, as shown in fig 4.7. Due to the limited resolution of each measurement point, errors are introduced that limits precise determination of the V_{FB}. To accurately determine the V_{FB}, one can perform a parabolic fit to the measured data around the location of peak in

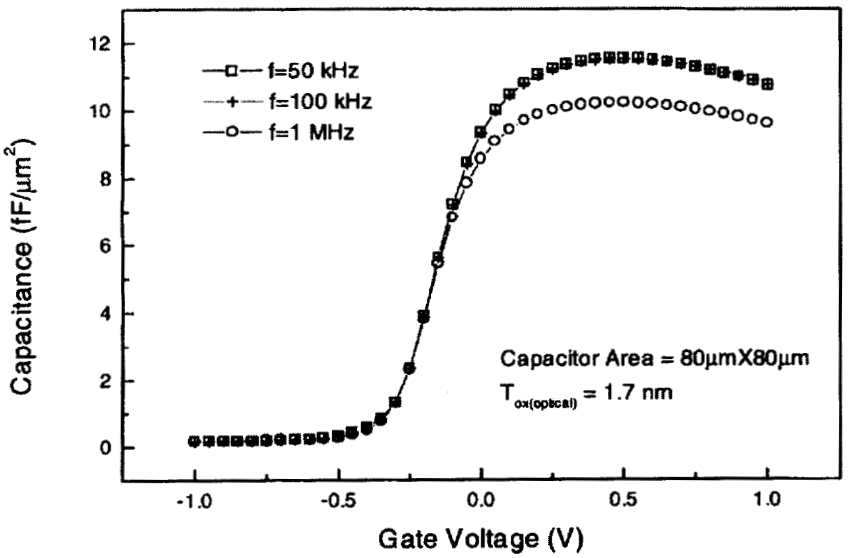


Figure 4.5: The measured frequency-dependent n-type MOS capacitance in strong accumulation region using the parallel circuit model.

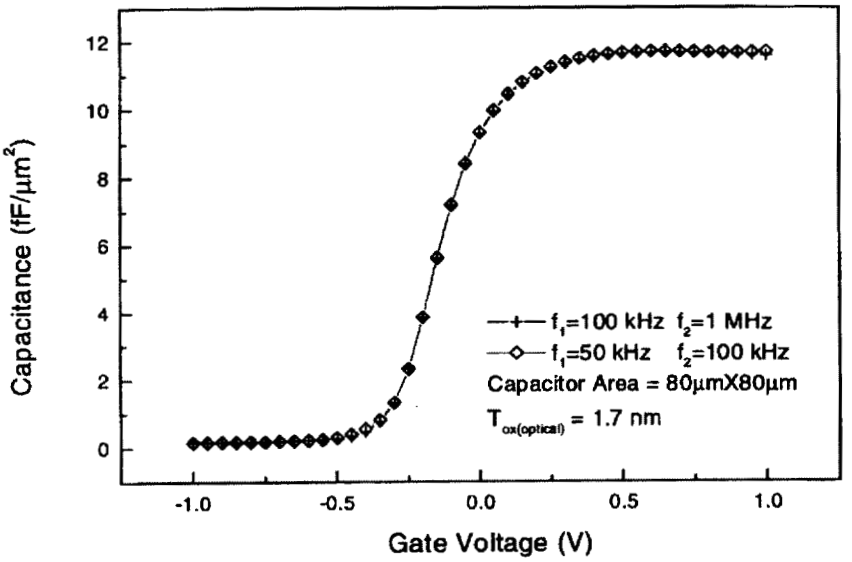


Figure 4.6: The true HF-CV curve obtained by combining the raw data from 100 kHz and 1 MHz (cross) and 50 kHz and 100 KHz (diamond).

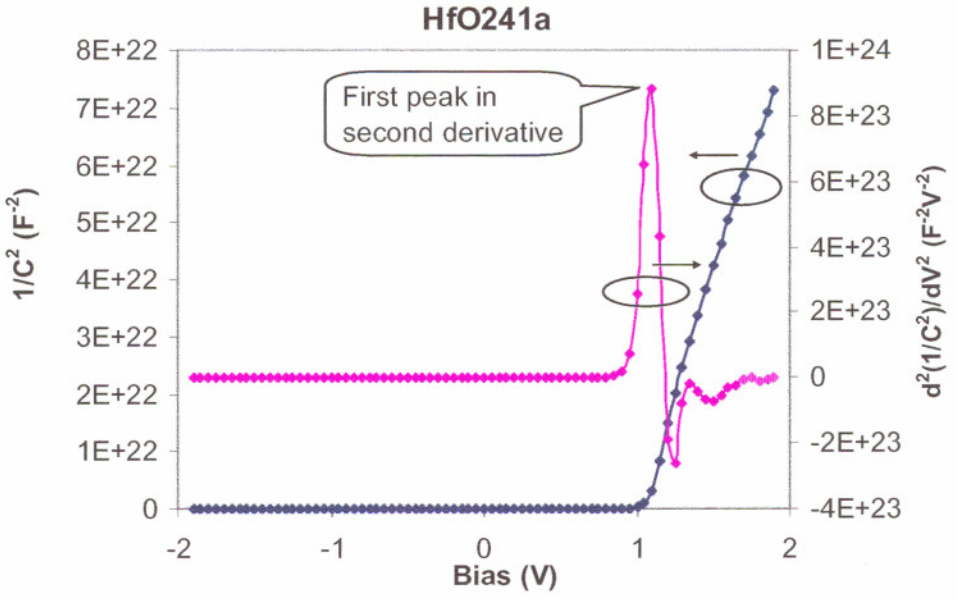


Figure 4.7: Plot of $1/C^2$ and $d^2(1/C^2)/dV^2$ versus gate voltage V_G on a MOS-C with an EOT 24 Å. Flatband voltage V_{FB} determined by the first peak in the second derivative.

second derivative. For interface trap density D_{it} in the 10^9 $cm^{-2}eV^{-1}$ and 10^{10} $cm^{-2}eV^{-1}$ range, the effect of interface trap on V_{FB} measurements can be neglected for MOS-C. For our MOS-C samples, D_{it} is in the 10^{11} $cm^{-2}eV^{-1}$ and 10^{12} $cm^{-2}eV^{-1}$ range. In the following data analysis, NCSU CVC program is still applied to extract the flatband voltage.

4.3.3 Oxide charges

Once the flatband voltage is determined, the effective oxide charges Q_{EFF} can be given by [15]:

$$Q_{EFF} = (\Phi_{MS} - V_{FB})\, C_{ox} \tag{4.7}$$

and

$$Q_{EFF} = Q_f + Q_m + Q_{ot} \tag{4.8}$$

where Φ_{MS} is work-function difference, Q_f the fixed oxide charge density, Q_m mobile oxide charge density, and Q_{ot} oxide trapped charge density. Oxide charges can make the C-V curve shift. Fig 4.8 shows that the entire C-V curve is shifted along the voltage axis with respect to the ideal C-V curve when one ignores the oxide charge. The shape of the C-V curve is unaltered and parallel to the ideal C-V curve. C-V curve is shifted to more towards the negative bias values for both p-type and n-type substrates for positive oxide charge. Similarly, shift is more towards positive bias values for negative oxide charge. Therefore, the polarity of oxide charge can be determined if oxide charge is the sole cause of the shift.

From $1/C^2$ versus V_G curve, the substrate doping density can be determined, which is used to calculate the Fermi potential ϕ_F. Substituting ϕ_F into equation 1.5 or 1.6, the V_{FB} of ideal C-V curve can be obtained. For example, if the gate material is platinum, provided that the doping density of p-type substrate is 10^{16} cm^{-3}, then the work function difference is 0.734 V in a vacuum, which is the same as V_{FB} for ideal C-V curve.

One source of oxide trapped charge is electrons or holes injected from the substrate or from the gate, respectively. These oxide trapped charges may give rise to the flatband voltage shift ΔV_{FB} during the bias sweeping between from inversion to accumulation and vice versa. The ΔV_{FB} can be expressed by [16]

$$Q_{ot} = -\Delta V_{FB} C_{ox} \tag{4.9}$$

Equation 4.9 is also used to check whether a measured ΔV_{FB} is due to charge injection into the oxide or due to mobile charge in the oxide, which is illustrated in fig 4.9. The positive flatband voltage shift can occur if electrons are injected from the substrate, whereas negative flatband voltage shift can occur if holes are injected from the gate, or positive mobile charges in the oxide.

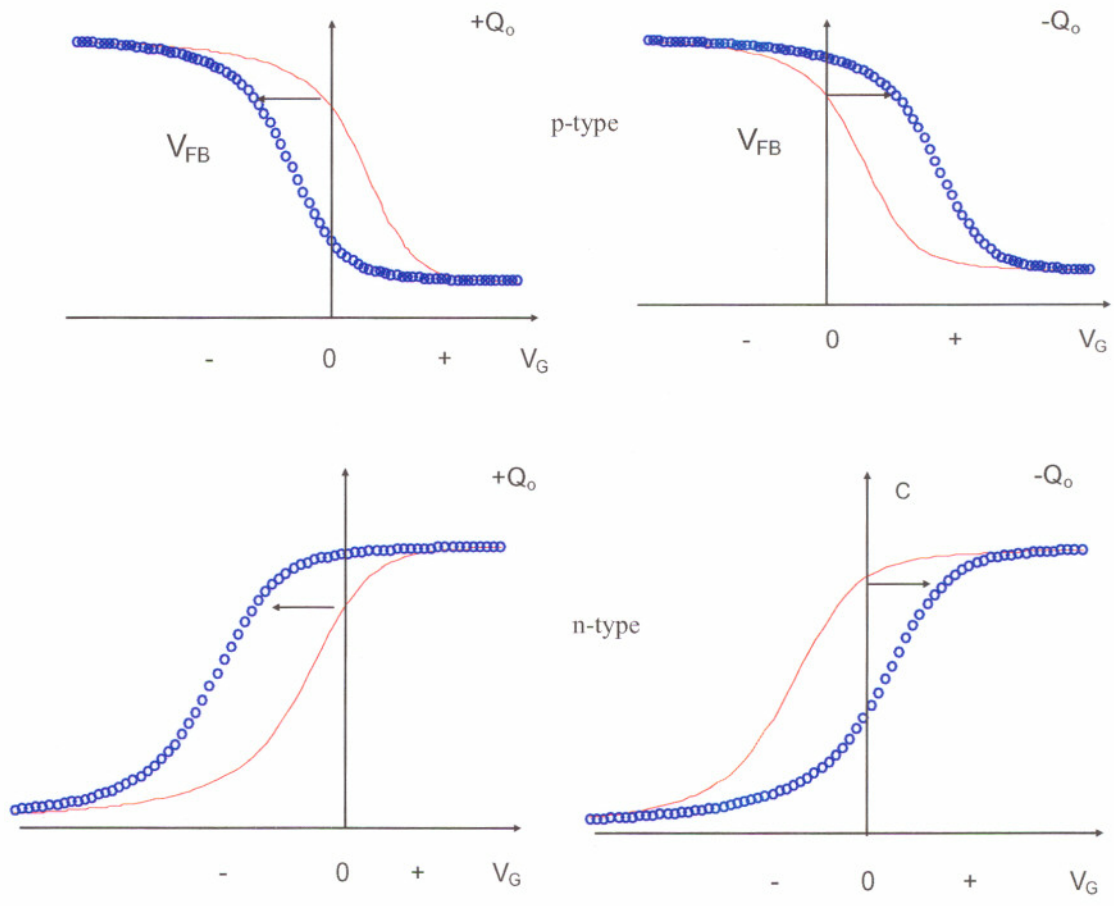
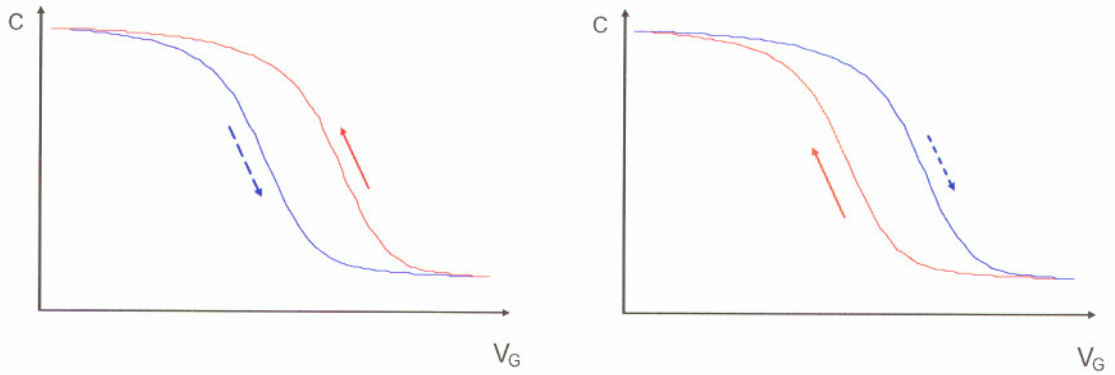


Figure 4.8: The effect of oxide charge on high-frequency C-V curve. Solid line represents ideal C-V curve, the circle represents experimental points. Positive oxide charge makes C-V curve left shift with respect to voltage axis for both n-type and p-type substrates. Negative oxide charge makes C-V curve right shift.



(a) (b)

Figure 4.9: Effect of charge injection and mobile charge on high frequency C-V curve. Negative charges injected from the substrate results in positive flatband voltage shift in (a). Positive charges injected from gate or positive mobile ions give rise to negative flatband voltage shift in (b).

4.3.4 Interface trap charge

The feature that distinguishes interface trap charge from oxide charge is that interface trap charge varies with gate bias, whereas oxide charge is independent of gate bias. Although the interface trap charges do not follow the ac gate voltage in HF-CV measurements, they do follow very slow changes in gate bias. They have no contribution to capacitance in HF-CV curve, but interface trap occupancy varies with gate bias so as to cause the HF-CV curve to stretch out along the gate bias axis because interface trap occupancy must be changed in addition to changing depletion layer charge. This stretch-out is illustrated in fig 4.10. The ideal C-V curve is calculated without interface traps. Unlike the oxide fixed charge and work function differences, interface traps produce a distortion in the shape of the C-V curve.

Fig 4.10 shows that the interface trap levels are uniformly distributed in the Si bandgap. If the interface trap energy level distributes with a pronounced structure, for example, interface trap level density increases abruptly somewhere in the Si bandgap, capacitance will change much more slowly with gate bias (flatten out) as the abrupt

increase in interface trap density is swept past the Fermi level at the silicon surface by the gate bias, which is illustrate in fig 4.11. Interface trap density can be determined from high-low frequency C-V measurements [17].

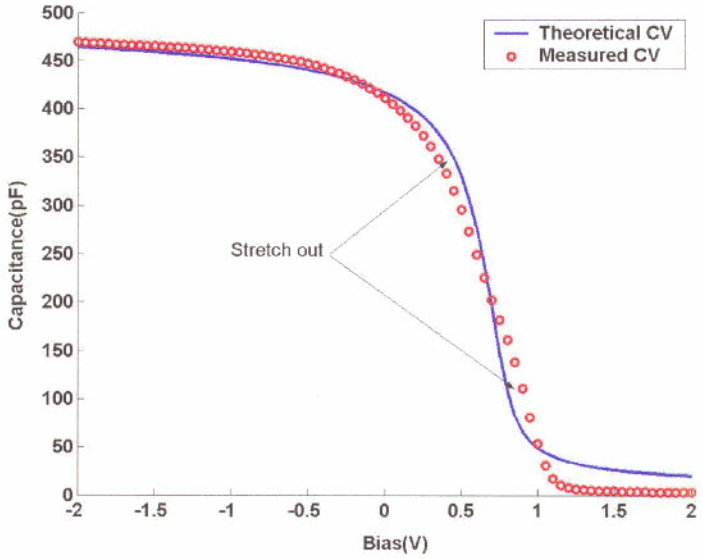


Figure 4.10: The comparison of theoretical and experimental high frequency C-V curves of MOS-C for sample HfO241a with EOT of 24 Å. The theoretical curve is calculated for a device without interface trap charge. Stretch-out in measured C-V curve indicates large interface states density and interface states level is uniformly distributed in Si bandgap.

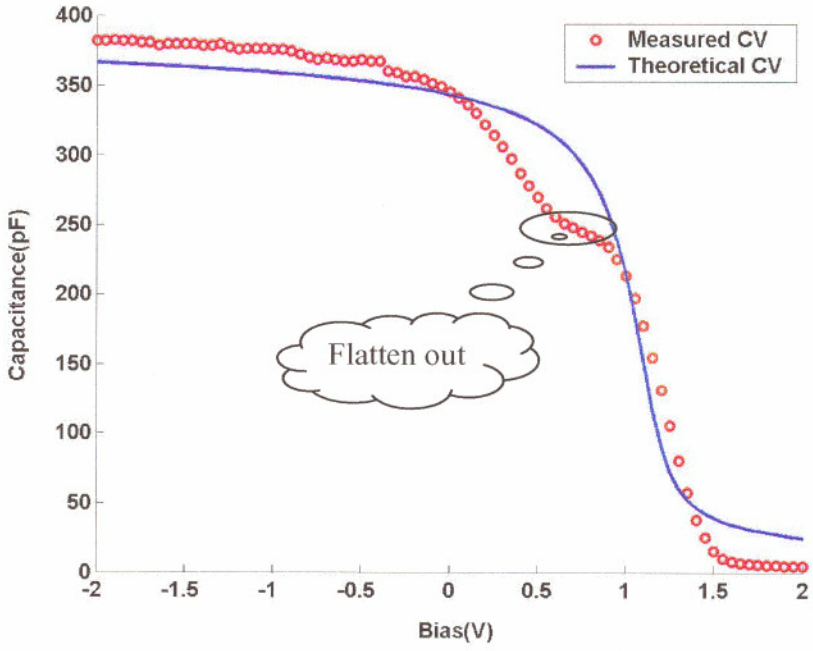


Figure 4.11: The flattening-out is observed in high frequency C-V curve of MOS-C for sample HfO253-10 with EOT of 28.7 Å due to non-uniform distribution of the interface trap energy level.

4.4 Results and analysis

4.4.1 From C-V measurements

The well-behaved C-V curves are obtained for HfO_2/ZrO_2 stacks with EOT of 18 Å, as shown in fig 4.12. No roll-off was observed in the accumulation regions of HF-CV curves for all MOS-Cs with high-κ and SiO_2 dielectrics. This demonstrates that the leakage current through these thin dielectrics are relatively low. The whole HF-CV curves are fitted to extract MOS-C parameters. The accuracy and precision of the gate area determines how closely the calculated C-V curve will fit the measured C-V curve.

The physical oxide thickness from ellipsometer, extracted EOT, V_{FB}, ΔV_{FB} and κ are listed in table 4.1. The physical oxide thickness was measured at five positions per wafer.

The highest dielectric constant value of 29 was achieved for HfO_2/ZrO_2 stack dielectric. For most of high-κ dielectrics, the values of κ are below 18, which are lower than what were expected. It may be explained by two reasons: (1) the κ of ultra-thin

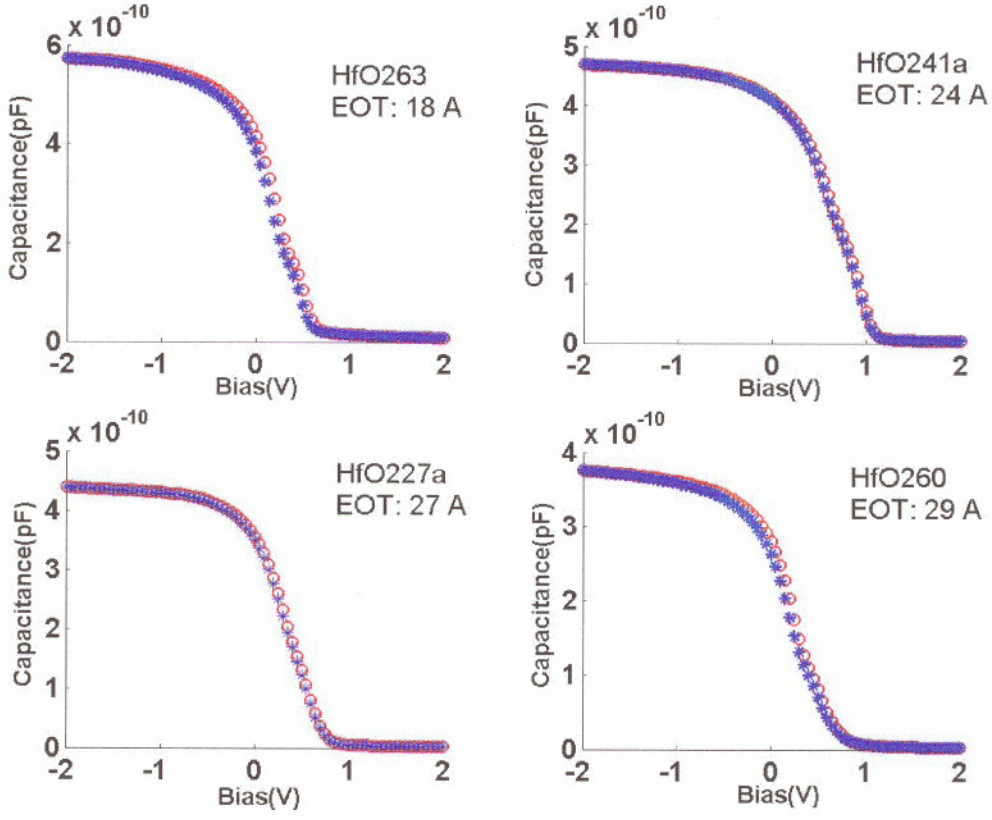


Figure 4.12: Well-behaved high frequency C-V curves for MOS-Cs of high-κ dielectrics with EOT less than 30 Å. The red circle data are measured from inversion to accumulation. The blue star data are measured from accumulation to inversion. The C-V curves show very small hysteresis.

Table 4.1: Extracted parameters by using NCSU CVC program

Wafer ID	Anneal	Physical Thickness(Å)	$V_{FB}1$(V)	$V_{FB}2$(V)	ΔV_{FB} (V)	EOT (Å)	κ
HfO247a	✓	152	0.51372	0.47828	0.035441	70.176	8.447
HfO247b		235	0.56003	0.46348	0.096554	74.732	12.264
HfO241a	✓	39	0.76173	0.73250	0.029230	24.1	6.311
HfO241b		58	0.33080	0.31850	0.012300	38.41	5.889
SiO30a	✓	636	5.89260	5.82500	0.067600	533.865	4.646
SiO30b		698	5.42170	5.37031	0.051390	599.46	4.541
SiO34a	✓	333	3.08150	2.94080	0.140700	268.375	4.839
SiO34b		361	1.34753	1.38871	-0.041184	252.056	5.586
SiO32b		687	2.04170	2.06810	-0.026400	467.19	5.735
SiO29b		2219	8.34338	8.15810	0.185280	1189.065	7.278
HfO241b		✧	0.70313	0.59320	0.109930	105.321	✱
HfO231	✓	✧	-0.59510	-0.68860	0.093500	308.5	✱
HfO230a	✓	✧	0.46632	0.48388	-0.017560	164.3036	✱
HfO230b		✧	0.55626	0.54903	0.007230	202.412	✱
HfO228a	✓	✧	0.43440	0.42578	0.008625	28.41159	✱
HfO228b		✧	0.28137	0.26386	0.017510	76.88365	✱
HfO227a	✓	✧	0.09917	-0.03900	0.138172	27.2	✱
HfO227b		✧	0.09817	0.09225	0.005920	26.98418	✱
HfO259a	✓	1105	-0.05394	0.40698	-0.460920	230.283	18.714
HfO259b	✓	1097	0.11228	1.41410	-1.301820	288.2277	14.843
HfO253-6	✓	29	0.78269	0.78012	0.002560	23.68	4.776
HfO253-10		56	1.13070	1.13269	-0.001985	28.7	7.610
HfO254-6	✓	28	1.71000	1.69640	0.013600	22.66	4.819
HfO254-10		42	0.57681	0.54197	0.034840	24.25	6.755
HfO260	✓	54	0.34826	0.29707	0.051190	29	7.262
HfO261	✓	139	0.75325	0.67863	0.074615	30.44745	**17.804**
HfO262	✓	30	-0.53057	-0.51990	-0.010670	**4.0443**	**28.930**
HfO263	✓	60	0.34265	0.28458	0.058070	**18**	13.000
SiO37	✓	74	0.94330	0.92590	0.017400	66	4.373
SiO38	✓	44	0.60936	0.59550	0.013860	43.5	3.945
SiO40	✓	63	1.30200	1.30420	-0.002200	65.5	3.751

Note: $V_{FB}1$ is the flatband voltage at the sweep from + to – bias. $V_{FB}2$ is from – to + bias.

✧: No optical physical thickness available.

✱: No κ value due to absence of physical thickness

dielectrics cannot maintain the same dielectric property as their bulk material. (2) the presence of an interfacial SiO_x layer could explain the lower κ values. By plotting the

dielectrics cannot maintain the same dielectric property as their bulk material. (2) the presence of an interfacial SiO_x layer could explain the lower κ values. By plotting the EOT versus physical thickness of the high-κ layer, the interfacial layer thickness and the dielectric constant can be estimated. In our case, due to a limited number of samples, it is not capable of plotting the EOT versus physical thickness. The actual structural composition and exact thickness of the interfacial layer is still unknown. A high resolution TEM is preferred for characterization of the interfacial layer.

The net fixed charged density in the high-κ dielectric can be estimated by equation 4.7 using the extracted MOS-C parameters. The hysteresis of the C-V curves sweeping from different directions are less than 50 mV for high-κ MOS capacitors with EOT less than 30 Å. It is noticed that most of ΔV_{FB} are positive, which result from negative charges injected into high-κ layers. Post metallization anneal (PMA) is necessary to reduce the traps near the high-κ/Si interface since it introduces hydrogen in the wafer. These hydrogen atoms are able to form silicon-hydrogen bonds and reduce the number of traps present in the dielectric. Due to one batch of samples with wrong PMA process showing serious hysteresis problem, it is believed that the optimized dielectric deposition process and PMA can alleviate hysteresis effect.

Interface engineering is critical for the application of high-κ gate dielectric. It is believed that interface trap charge density in high-κ layer is higher than that in conventional SiO_2 gate oxide. The stretch out caused by interface trap charge is observed for some samples with EOT from 23 to 29 Å as shown in fig 4.13. The change of interface trap occupancy may give rise to the change of the effective fixed oxide charges, which directly cause the hysteresis in HF-CV curve. The substrate clean process prior to high-κ deposition, gate dielectric stacks structure as well as the optimization of high-κ layer deposition have strong effects on the magnitude of interface trap charge density. Due to different process of high-κ layer, sample HfO263 with EOT 18 Å in fig 4.12 shows negligible stretch out of HF-CV curve comparing to those samples with similar EOT in fig 4.13.

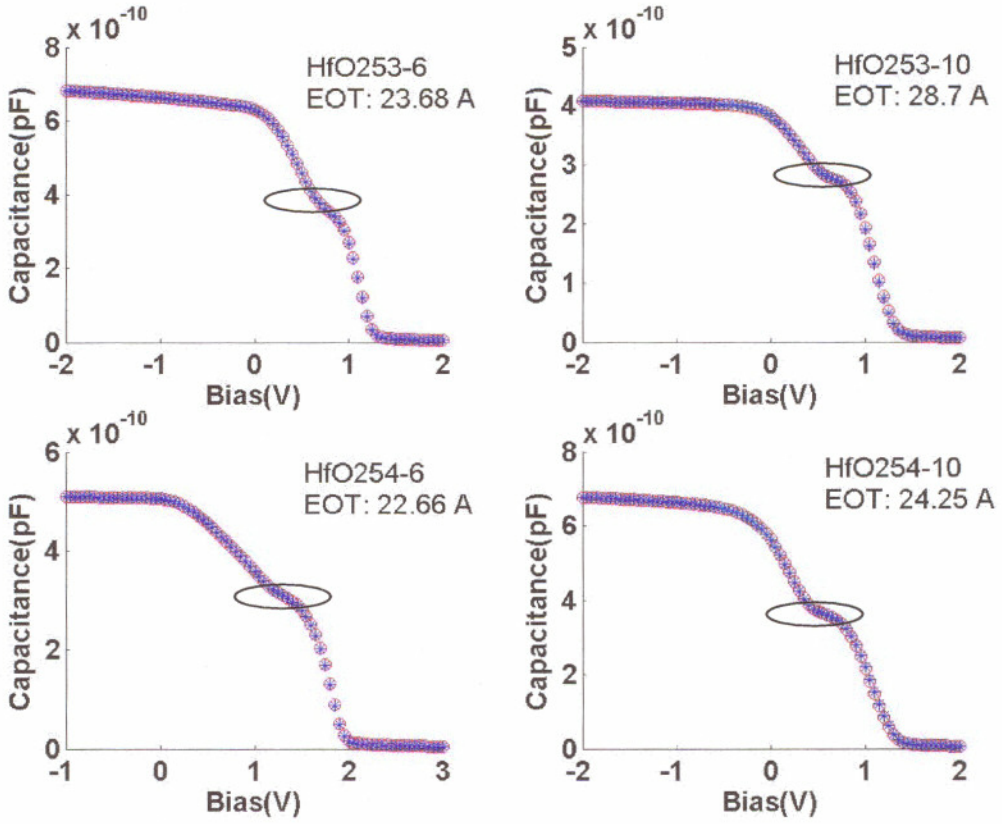


Figure 4.13: The interface trap charge gives rise to stretch out of high frequency C-V curves for MOS capacitors with high-κ dielectrics with EOT from 23 to 29 Å.

4.4.2 I-V measurements

The leakage current over a large thickness variation were measured. Fig 4.14 shows the current density versus gate bias for all high-κ capacitors. The I-V measurements are very reproducible, which is examined by SiO_2 samples SiO40 and SiO37 with EOT of 65.5 and 66 Å, respectively, as shown in fig 4.15. Sample HfO262 (EOT = 4 Å) and HfO263 (EOT = 18 Å) display very low leakage current with respect to thermally grown SiO_2 [18] with similar equivalent oxide thickness shown in fig 4.16.

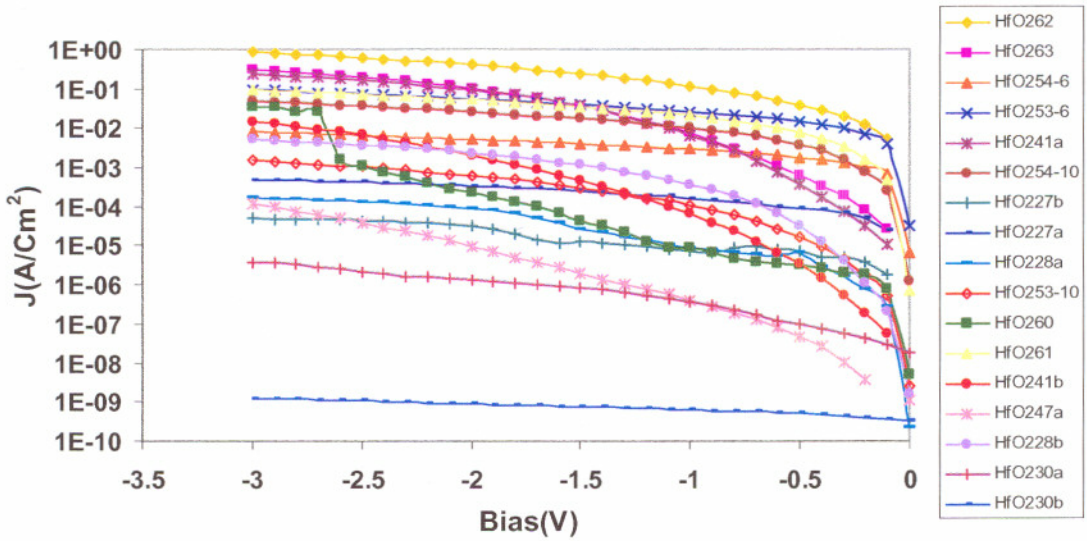


Figure 4.14: Leakage characteristics of MOS capacitors for high-κ dielectrics with EOT from 4 to 202 Å.

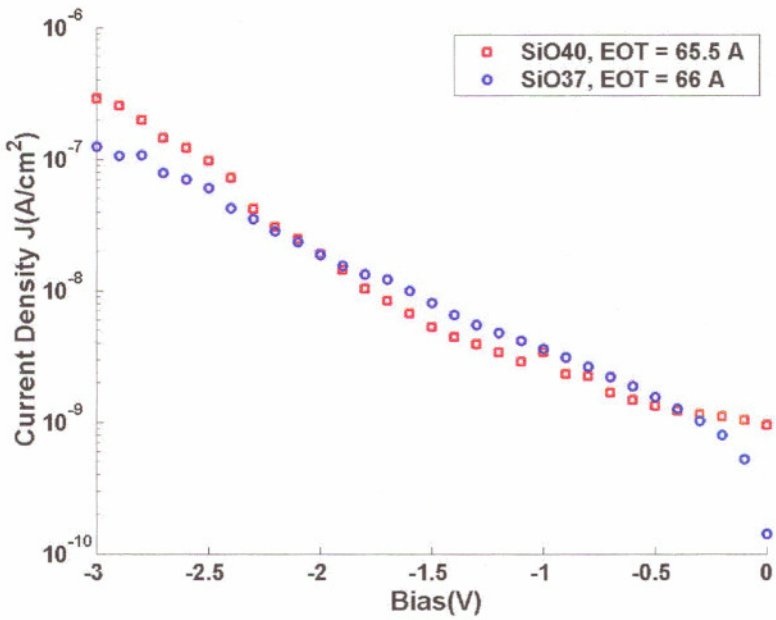


Figure 4.15: Current-voltage measurements are reproducible for different samples with similar EOT.

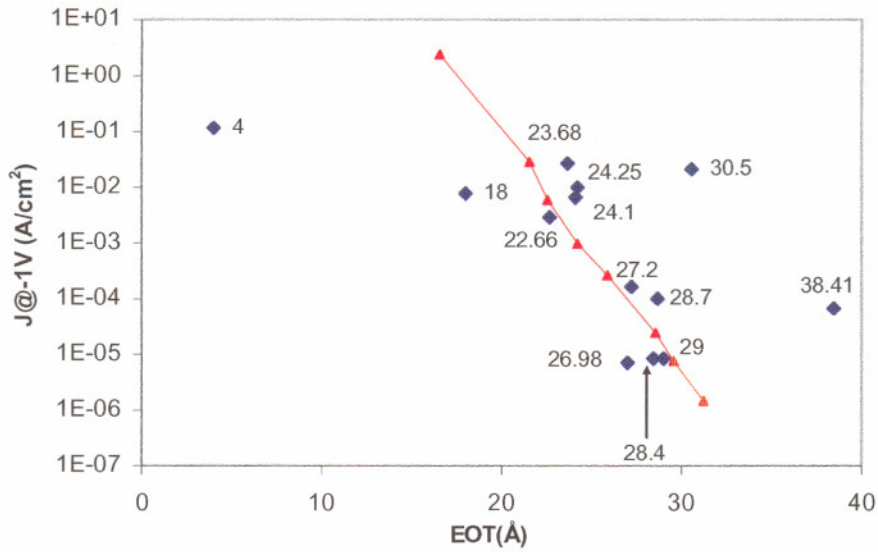


Figure 4.16: Plot of leakage current density versus EOT for high-κ capacitors at gate voltage -1 V. The diamond represents the capacitor with high-κ dielectrics. The triangle represents the thermally grown SiO_2.

There are several conduction mechanisms to contribute to the current-voltage characteristic of MOS capacitors for example, Schottky emission, Poole-Frenkel (P-F) emission, Fowler-Norheim (F-N) tunneling, directly tunneling as well as space charge limited current, etc. The real I-V characteristic usually represents simultaneous contributions of several of these mechanisms. However, only one typically limits the current, making it the dominant current mechanism over a given bias range. The conduction mechanism may also be affected by defects and trapping states in insulator.

When the oxide thickness is less than 3 nm, direct tunneling dominates the carrier transport. Samples HfO253-6 and HfO254-6 had physical oxide thickness of 29 Å and 28 Å, respectively, and had high interface trapped charges that were confirmed by HF-CV measurements shown in fig 4.13. The logarithm of the current depends linearly on the square root of the gate voltage from moderate to high electric field, which is illustrated in fig 4.17. Therefore, the conduction mechanism is represented by Schottky emission.

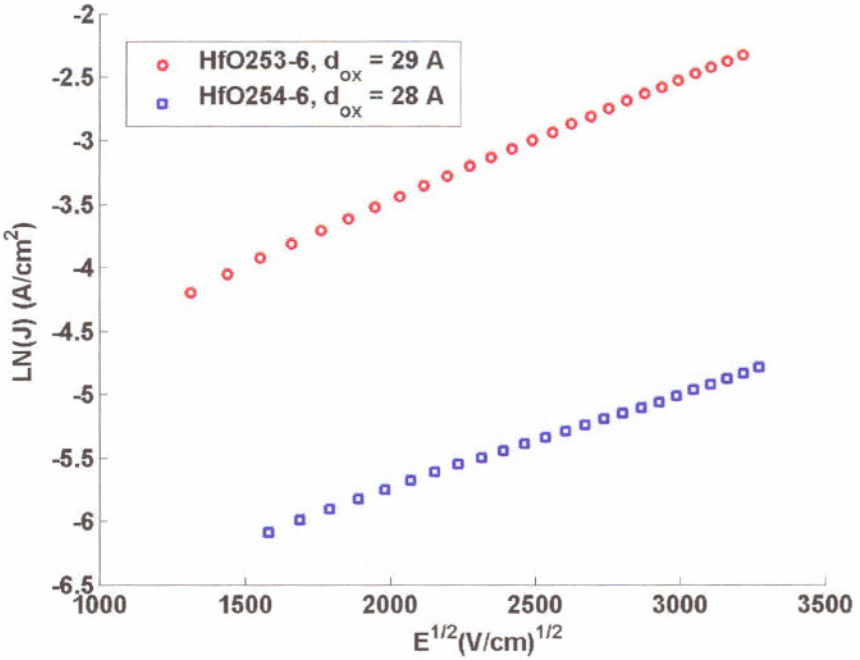


Figure 4.17: Ln(J) vs $E^{1/2}$ characteristics of high-κ capacitors. The linear relationship indicates Schottky conduction mechanism [19].

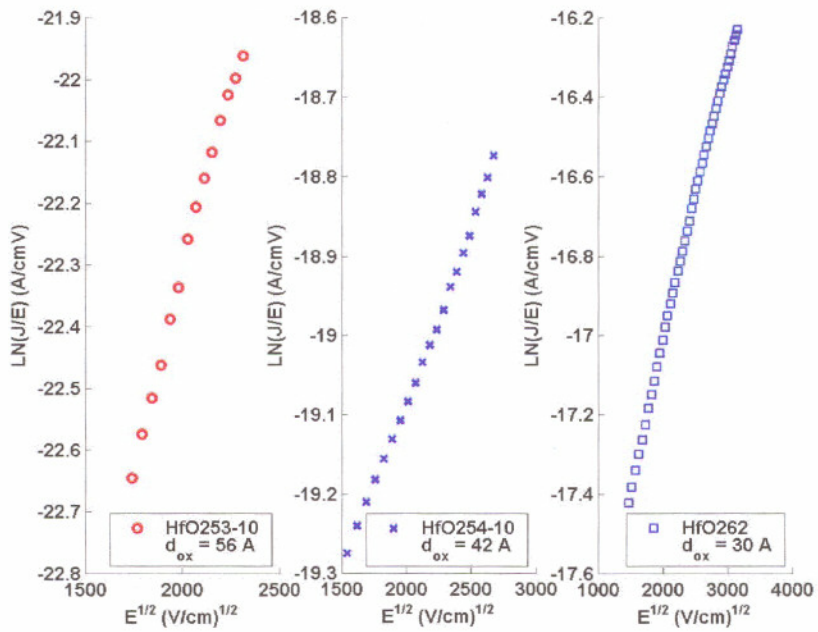


Figure 4.18: Plot of ln(J/E) vs $E^{1/2}$ for high-κ film with high density of interface trapped charge. The straight line indicates Poole-Frenkel conduction mechanism.

For the moderately thick films from 3 nm to 6 nm, the thickness of high-κ layer is large enough to start suppressing the direct tunneling [20]. The existence of a large density of interface trapped charge and oxide defects may make Poole-Frenkel emission the dominant leakage mechanism. The detailed characterization of P-F emission for traps in CVD silicon nitride had been discussed by Frenkel [21]. To check for this current mechanism, experimental I-V characteristics are typically plotted as ln(J/E) as a function of the square root of the electric field $E^{1/2}$ in the insulator. On this scale, the P-F conduction is observed as a straight-line as shown in fig 4.18. The confirmation of a large density of interface traps in these high-κ layers is presented in fig 4.13.

For thick high-κ layers without large amount of interface trap levels, Fowler-Nordheim tunneling is identified as a dominant current mechanism. As a proof, the F-N plots of $\ln(J/E^2)$ versus 1/E are examined to show linear relationship, which are shown in fig 4.19.

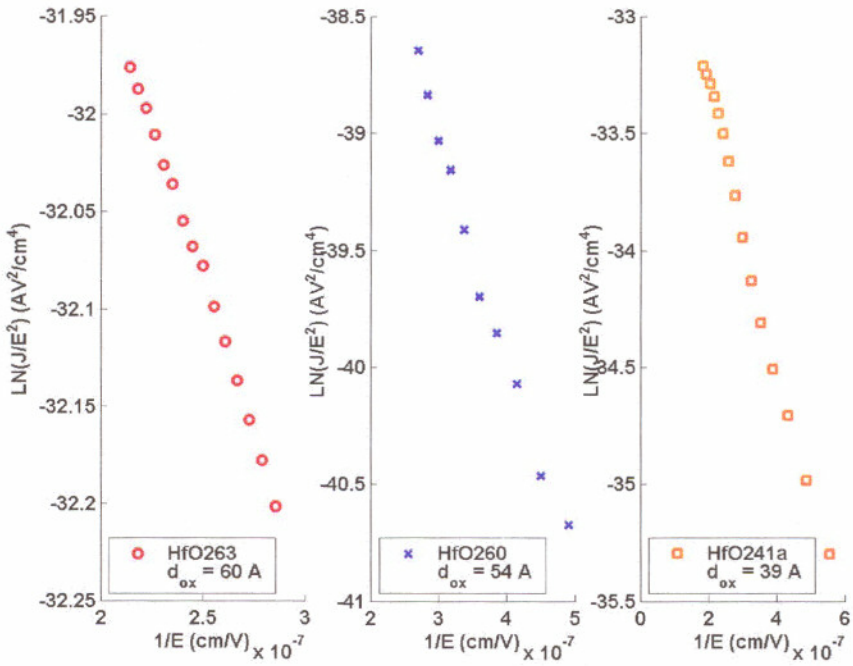


Figure 4.19: Plot of $\ln(J/E^2)$ vs 1/E for thick high-κ film without high density of interface trapped charge. The straight line indicates Fowler-Nordheim conduction mechanism.

4.5 Conclusion

In this chapter, I-V and C-V characteristics of ALCVD grown HfO_2, ZrO_2 and Al_2O_3 dielectric thin films prepared at various deposition conditions were investigated. The experimental HF-CV data fitted to the theoretical model to extract the EOT by including quantum mechanical effects. Error in capacitor area showed up in the extracted EOT. Dielectric constant as high as 28 and EOT of 4 Å has been achieved in sample HfO262 with HfO_2/ZrO_2 stacks. The reason why dielectric constants in ultrathin high-κ films are lower than those in bulk materials is believed to be due to the existence of interfacial layer. Neglect of interface capacitance in evaluating κ by capacitance measurements gives low values of κ. The low hysteresis (10 mV) in HF-CV curves is observed in sample HfO262, indicating low oxide charge in the insulator. For most of other high-κ MOS capacitors, the hysteresis is usually within 50 mV. The degradation in hysteresis is observed with non-optimal PMA, indicating optimized PMA is necessary to improve the electrical properties of the deposited films. The well-behaved high frequency C-V curves are obtained except for stretch-out in some samples due to existence of interface trapped charge in the insulators. The conduction through high-κ layer has also been investigated. In thin films with thickness less than 3 nm, the conduction mechanism is likely a combination of direct tunneling and defect-assisted tunneling. When significant interface trapped charge is present, Schottky emission is regarded as the primary conduction mechanism. In moderately thick high-κ dielectrics, Pooler-Frenkel emission dominates the carrier transport in films with high interface trap charge. In thick layers, Fowler-Nordheim tunneling is the major conduction mechanism. The very low leakage current is also observed in sample HfO262 at current density of 0.02 A/cm^2 and on electric filed of 1MV/cm.

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CHAPTER 5: HIGH FREQUENCY CHARACTERIZATION OF HIGH-κ MIM CAPACITORS

In charter 4, the electrical properties of high-κ dielectric were characterized at frequencies up to 1MHz. However, it is very important to investigate the dielectric response of a high-κ layer at high frequency, for example, radio frequency (RF) range. High-κ dielectrics in high frequencies do not show the same dielectric constants as those at low frequencies. In chapter 3, it was demonstrated that dielectric constant is frequency-dependent. The influence of the frequency on the dielectric constant is becoming increasingly important as CMOS are pushed upward in frequency into the 1-10 GHz region and beyond. The dielectric constant will decrease as the operating frequency increases. Therefore, the question arises: how about the performance of high-κ dielectric in the microwave region? The shift in capacitance with different operating frequencies is known as dispersion. The presence of dielectric dispersion can cause the distortion of the signals and the loss of capacitive characteristics needed for application. Dielectric dispersion is caused by the frequency dependence of the polarization mechanisms. When an ac electric field is applied to a dielectric material, each polarization mechanism can contribute to the net polarization up to a limited frequency. Beyond this frequency range, the given polarization mechanism is wiped out. In the current chapter, we describe the electrical characterization of the amorphous hafnium dioxide films over a broad range of frequency from 100 MHz to 65 GHz, which range covers RF regime and enters into microwave frequencies. HfO_2 film has been characterized electrically for frequency up to 65 GHz using MIM structure.

5.1 Introduction

Dielectric constant can be obtained from capacitance measured by C-V analysis. Current available LCR meters are incapable of measuring the capacitance accurately over microwave range. The microwave capacitance of a device under test (DUT) can be derived from the scattering parameters, which are measured by vector network analyzer (VNA). Fig 5.1 shows the schematic of a two-port network for s-parameter measurement [1]. The component of the impedance Z of DUT can be calculated from reflection coefficient S_{11}. S_{11} can be expressed by

$$S_{11} = \frac{Z_1 - Z_0}{Z_1 + Z_0} \tag{5.1}$$

where Z_0 is the characteristic impedance of the measurement system (usually is 50 Ω), and Z_1 is the input impedance at port 1. This relationship between reflection coefficient and impedance is the basis of the Smith chart transmission-line calculation. Consequently, S_{11} can be plotted on Smith chart.

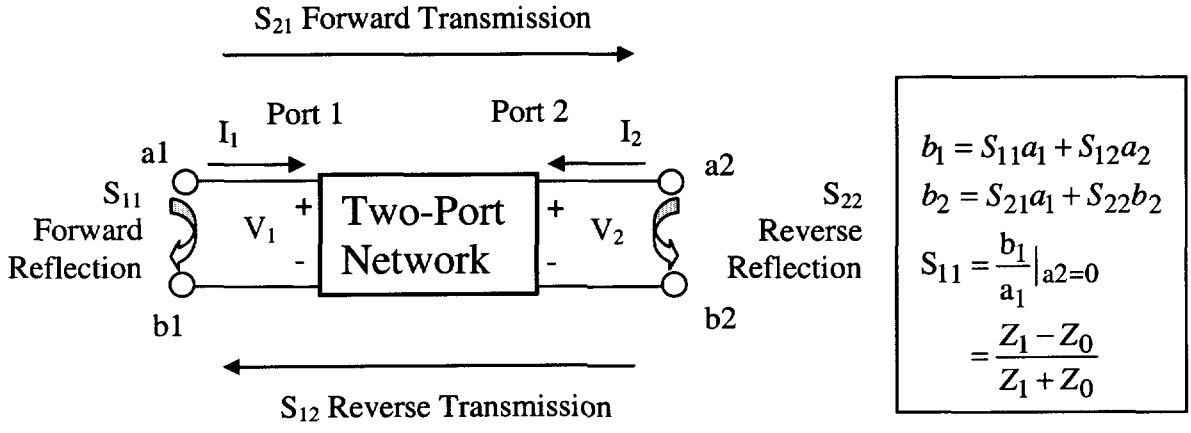


Figure 5.1: Schematic of a two-port network.

To correct the imperfections of the measurement system, calibrations down to the probe tips are required to make accurate on-wafer measurements. The de-embedding technique is applied to eliminate not only the non-ideal nature of cables and probes, but also the internal characteristics of the VNA itself. The calibration of VNA is performed by rather complex procedures, such as, Short-Open-Load-Through (SOLT), load-Refection-Match (LRM) or Through-Reflection-Load (TRL) [2, 3]. It is important to note that the specific electrical behaviors of the standards depend on the contact pattern and probe pitch used. In this work, one port network is used to measure S_{11} parameter. Short-Open-Load (SOL) is employed for standard calibration of one-port network, as shown in fig 5.2. Three contacts for the coplanar probe are one signal contact in the center pad and the others are ground contacts with a 125 μm pitch, which is called Ground-Signal-Ground (GSG) configuration, as shown in fig 5.3. Since GSG pattern has higher performance than the Ground-Signal (GS/SG), GSG is adopted as the contact pattern in this work.

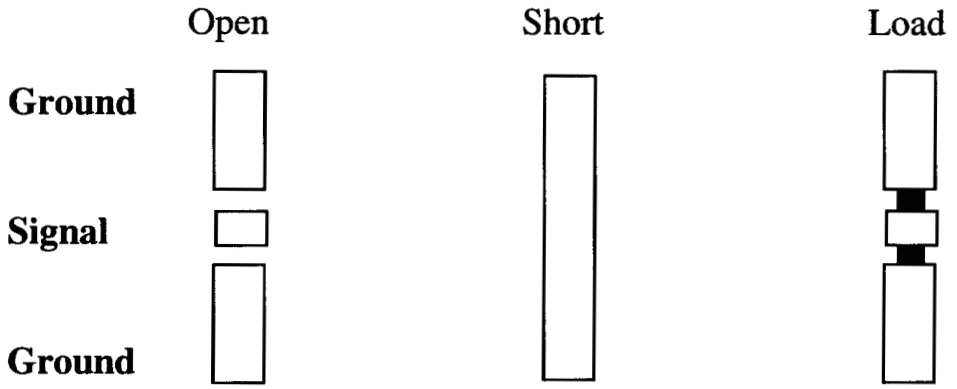


Figure 5.2: Standard calibration SOL of one-port network. Load circuit standard is implemented by terminating with 50 Ω load resistor.

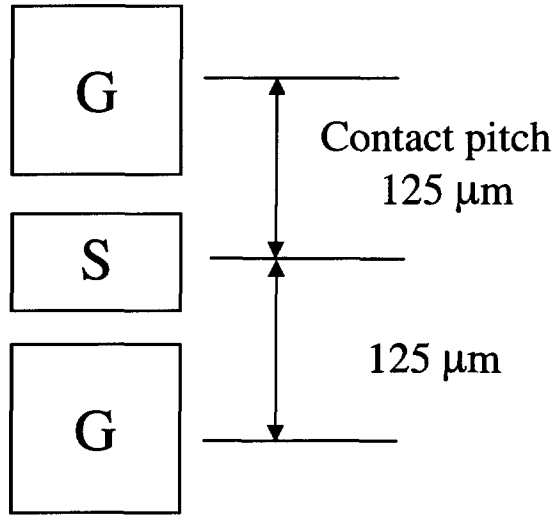


Figure 5.3: GSG pad pattern for one-port network measurement employed in this work.

5.2 Experimental

5.2.1 Test structure: Metal-Insulator-Metal (MIM)

A test structure is designed to investigate the dielectric constant and loss tangent of amorphous hafnium dioxide film at frequencies up to 65 GHz. The test component is parallel-plate MIM capacitor as shown in fig 5.4. The test structure consists of a matrix of MIMs with different width and length. This matrix was designed to study the effect of the shape and size of capacitor on MIM capacitance. One can get more information, such as, the relationship between capacitance and capacitor area, and the effect of area-to-perimeter ratio of the capacitor on the capacitance. The physical dimensions of the capacitors are listed in table 5-1.

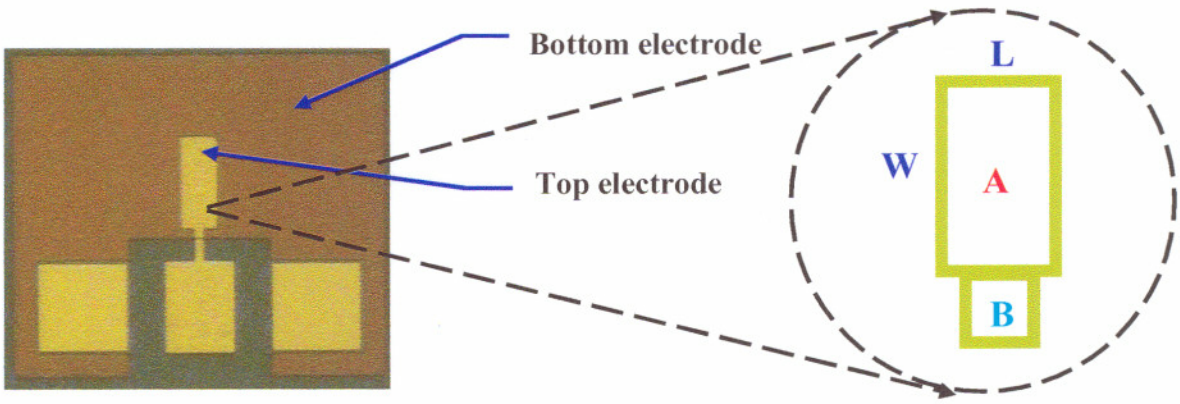
The TiN bottom electrode was first deposited on 6-inch silicon wafers. Then, a 40 Å amorphous HfO_2 layer was deposited by atomic layer deposition [4,5] processed at Genus [6]. HfO_2 layers were patterned by the standard photolithographic process. Finally,

TiN layer was deposited, patterned, and etched to produce the top electrode. Since TiN is a very hard material, an aluminum top layer was added to improve the probe contact.

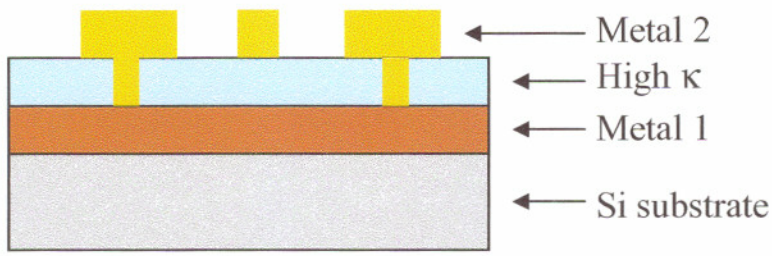
5.2.2 Electrical measurement

One-port vector network analysis is useful for extracting induction, capacitance and impedance as a function of frequency. To characterize the microwave performance of high-κ dielectric, TiN/HfO_2/TiN MIM capacitors were employed to measure S_{11} parameters by using GSG coplanar probes with Agilent E8361A PNA series network analyzer at frequencies from 100MHz to 65GHz. There were three wafers with different precursors for HfO_2 deposition and their wafer ID were 2366, 2364 and 2285, respectively.

The low frequency measurement under zero bias at 1MHz was performed using a HP4275A multi-frequency LCR meter. One probe was placed on the signal pad of GSG configuration, the other probe on one of the ground pads connected by via holes. The dielectric constants measured under zero bias at 1 MHz were used as reference for comparing values over the RF range.



(a) Top view



(b) Cross section

Figure 5.4: Layout of MIM capacitor using 40Å HfO_2. MIM consists of a variable area A and a fixed area B (10 ×10 μm^2)

Table 5.1: Width and length of area A (all units in μm)

W \ L	10	20	40
0	0 × 10	0 × 20	0 × 40
10	10 × 10	10 × 20	10 × 40
20	20 × 10	20 × 20	21 × 40
30	30 × 10	30 × 30	30 × 40
40	40 × 10	40 × 20	40 × 40
50	50 × 10	50 × 20	50 × 40
100	100 × 10	100 × 20	100 × 40

5.2.3 Modeling and optimization

The model of a capacitor has been discussed in chapter 3. MIM can be represented by an ideal capacitor C and a shunt conductance G in parallel. Shunt conductance G governs the resistance of leakage current in the dielectric medium. In other words, the lower the value of conductance G, the lower leakage current. It means the power dissipated in the dielectric medium is small. Since the two interfaces between the electrodes and dielectric layer are very thin, they can be treated as a series resistor, which includes the contribution of the connecting cables. The series inductance L also has to be taken into account for the parasitic inductance in the two electrodes for microwave application. L can be separated into L_1 and L_2, which correspond to the inductance of top and bottom electrode respectively. In our case, due to the same material for MIM electrodes, it can be simplified to one inductance L, whose magnitude is the sum of L_1 and L_2. This simplified RLCG model shown in fig 5.5 is sufficient to describe the MIM.

An optimization technique is applied to extract the intrinsic capacitance. Agilent Advance Design System (ADS) is used to simulate and optimize the above equivalent circuit. The schematic of optimization circuit is illustrated in fig 5.6 in detail. The optimization component controls the simulation by receiving the data and testing the data until the goals are reached. The optimizers are differentiated by their search methods and error function formulations. The search method determines how the optimizer arrives at new parameter values, while the error function measures the difference between simulated and measured S parameter. In our case, the differences between the measured and modeled S-parameters are minimized. The least-squares error function is calculated by evaluating the error for each specified goal at each frequency point individually, then squaring the magnitudes of those errors. The smaller the value of the error function, the more closely the responses coincide. In this optimization, the real and imaginary parts of the modeled S_{11} will be adjusted to match the measured value. It is noted that the optimizer tries to match the measured S_{11} over the entire simulated frequency range.

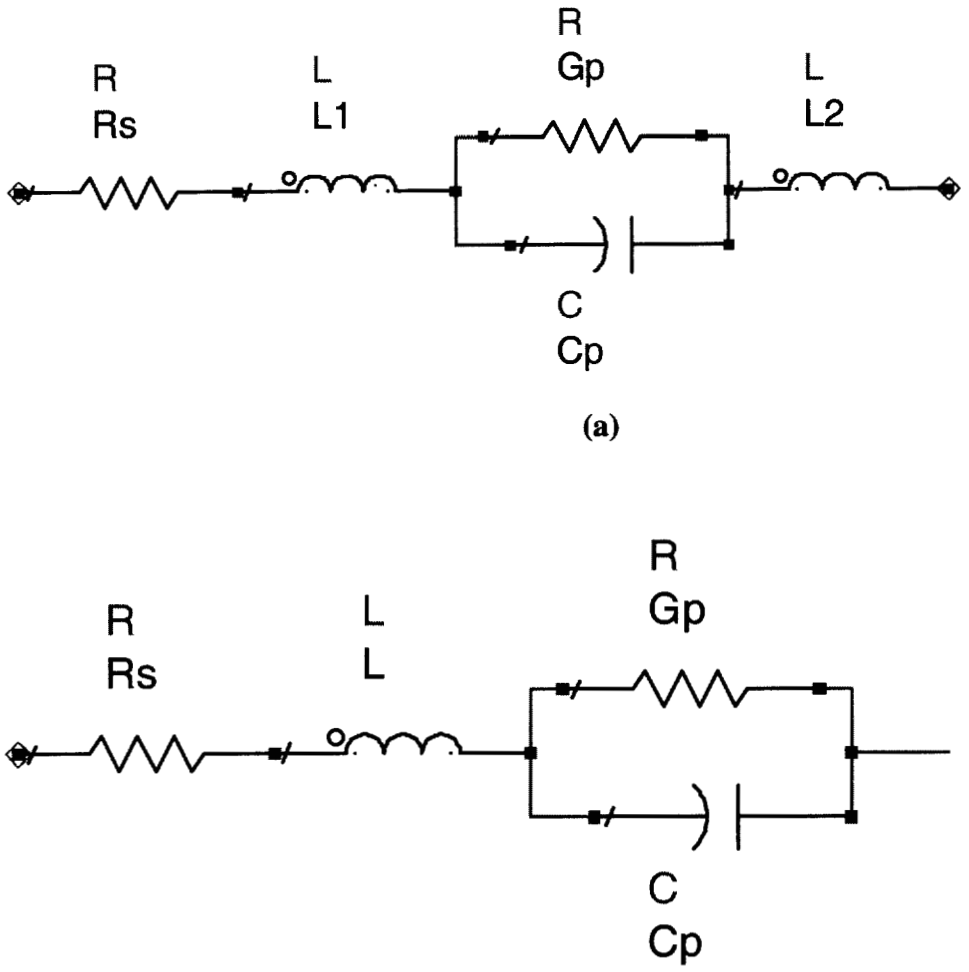


Figure 5.5: Equivalent circuit model for MIM capacitor. (a) Practical circuit model. L_1 and L_2 represent the inductance of top and bottom electrode respectively. (b) Simplified RLCG model, where L is the sum of L_1 and L_2.

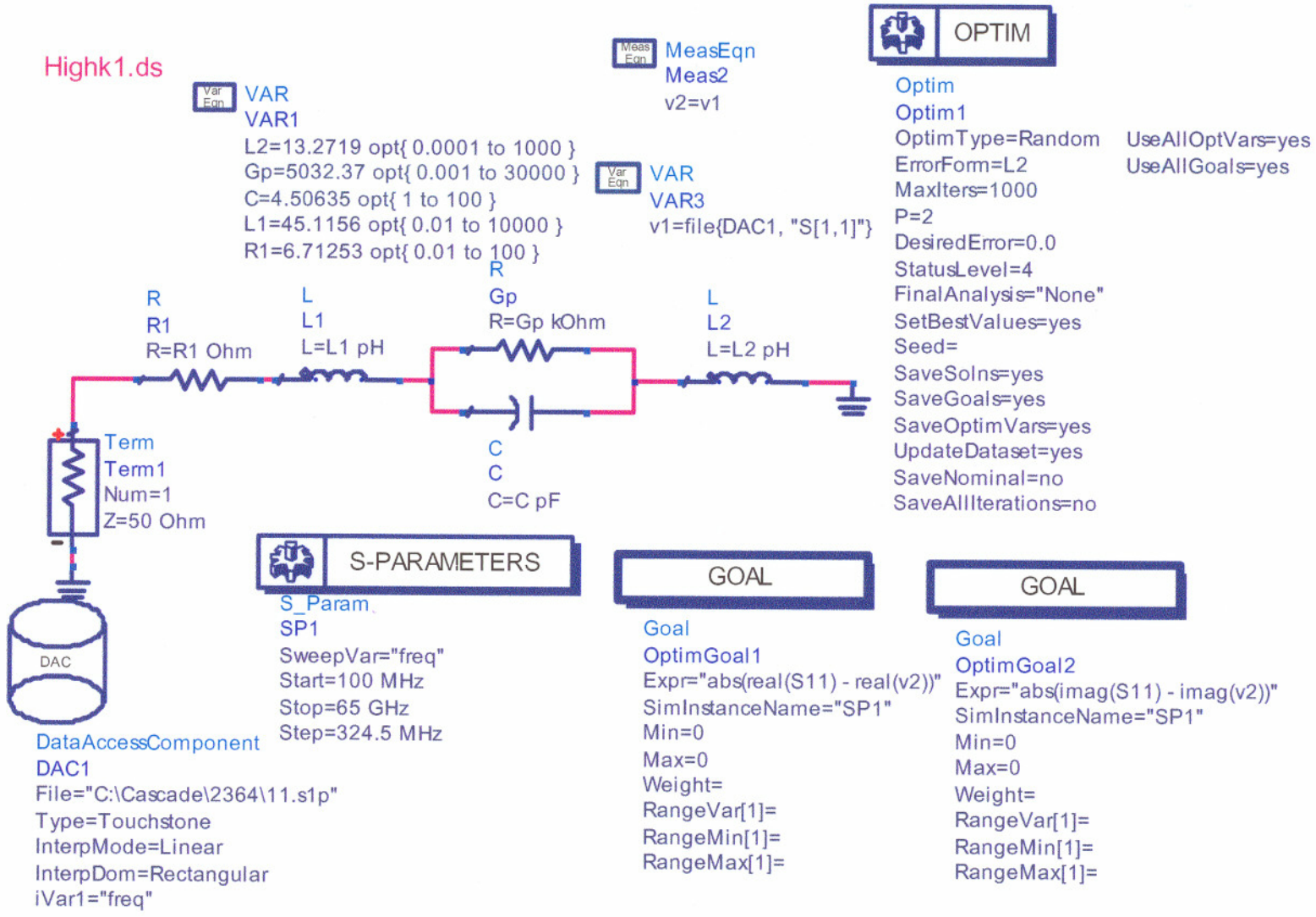


Figure 5.6: Schematic of equivalent circuit for optimization

5.3 Results and discussion

The equivalent circuit model as indicated in Fig 5.5 is established to extract the capacitance at microwave regime. Any parasitic component embedded in MIM capacitor may lead to above model failure on optimization. For example, fig 5.7 shows the optimization results for wafer 6889 with RLCG model at the frequency up to 20 GHz. The measured S_{11} parameter (represented by v2 dataset, red curve) is displayed by Smith chart in fig 5.7a. It is obvious that the sole capacitor should not be illustrated by curve v2 because of the existence of a piece of flat line in the Smith chart. The Smith chart has circles of constant resistance and arcs of constant reactance. Fig 5.7 shows that the resistance reduces as the frequency increases. Not only are the magnitude and phase of S_{11} parameter mismatched between simulated and measured values, but also the real and imaginary parts of S_{11} parameter. This suggests that RLCG model in fig 5.5 cannot represent the device under test. The modification of equivalent circuit model by adding one transmission line, as shown in fig 5.8, makes the simulated and measured S_{11} match each other. The optimization results for modified equivalent circuit model in fig 5.9 show great improvement on S-parameter match.

The above optimization procedure indicates that DUTs in wafer 6889 are not exactly the same as the originally designed MIM capacitors. The transmission line is expected to embed into the device since the transmission line has the property of negative impedance at some frequencies. Therefore, the analysis of dielectric properties of a high-κ film is only meaningful when both dielectric constant and loss tangent are extracted from the equivalent circuit model, which makes the simulated and measured S-parameter match well.

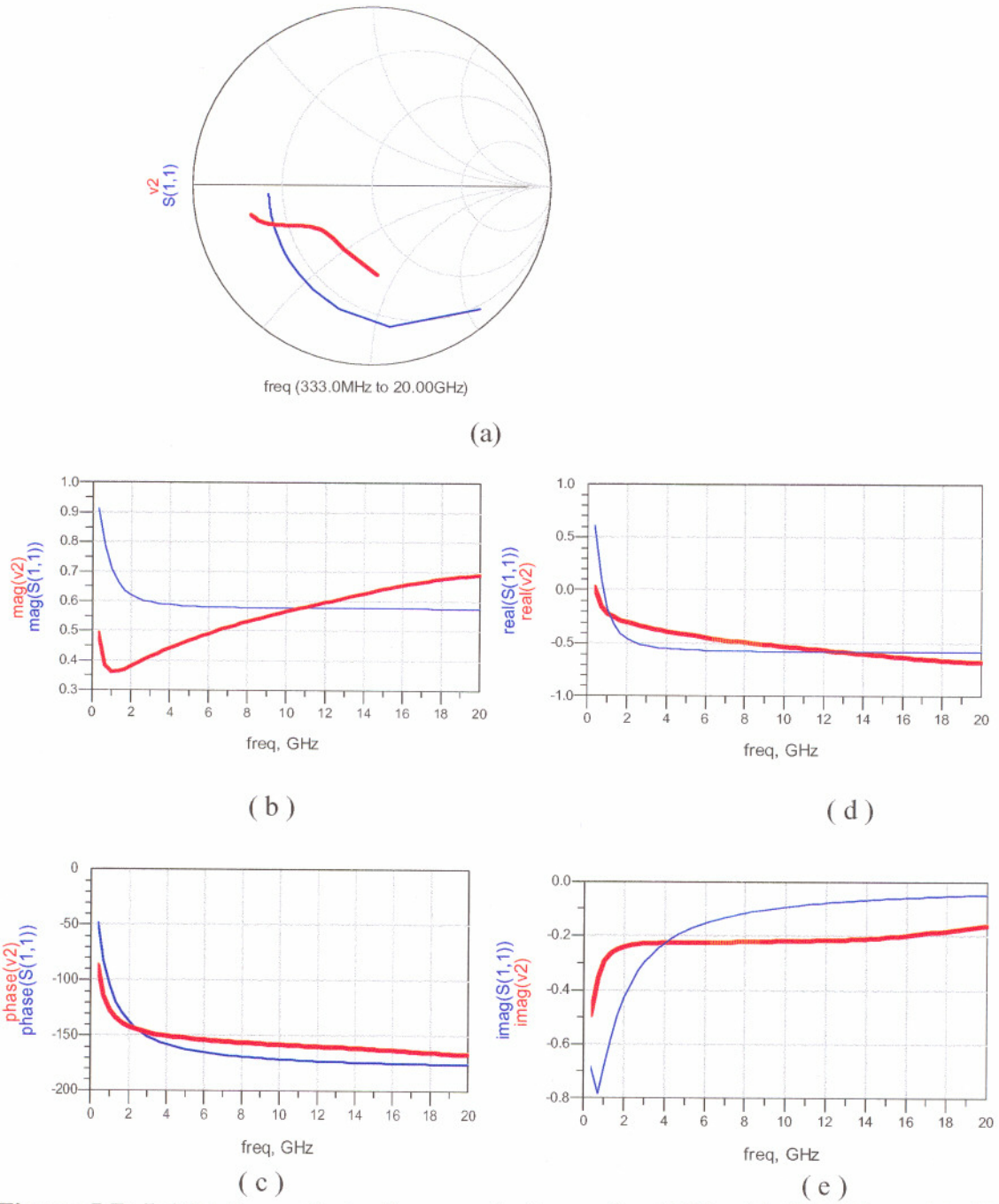


Figure 5.7: Initial S_{11} optimization results for wafer 6889 with RLCG model. The red curve represents dataset v2 of the measured S_{11} parameter. The blue one is the simulated S_{11} parameter. (a) Smith chart (b) Magnitude (c) Phase (d) Real part (e) Imaginary part.

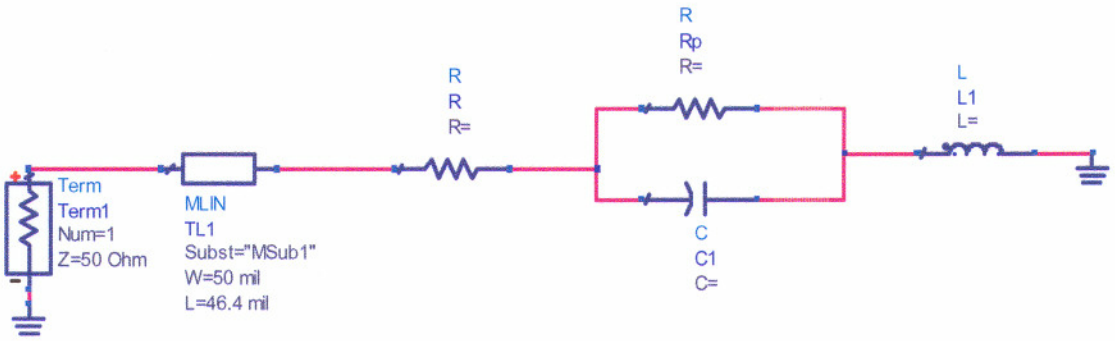


Figure 5.8: Modified model for wafer 6889 by adding one transmission line.

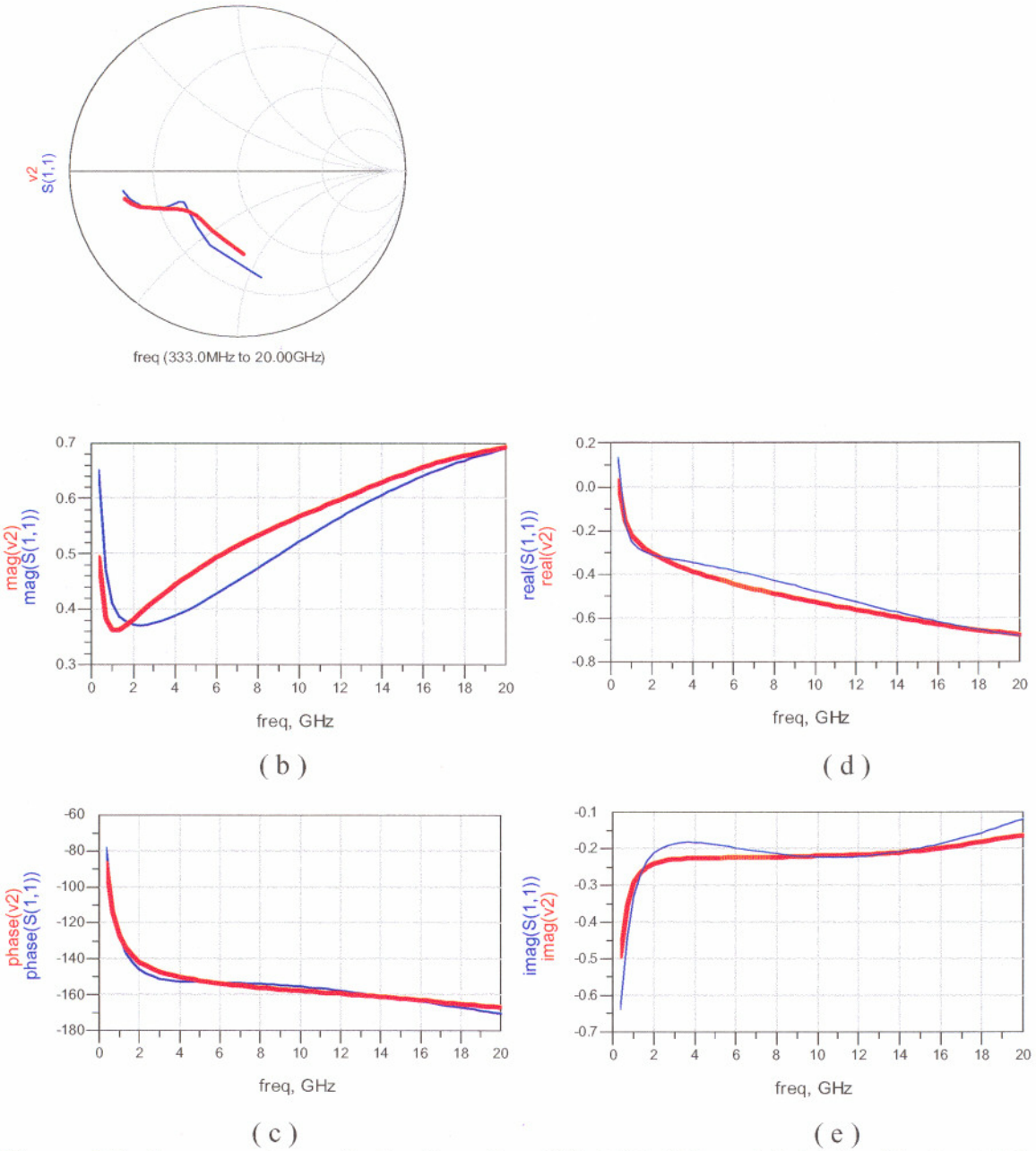


Figure 5.9: S-parameter optimization of modified RLCG model. (a) Smith chart (b) Magnitude (c) Phase (d) Real part (e) Imaginary part.

5.3.1 Dielectric constant and loss tangent

A good match between simulated and measured S-parameters over all frequency range is achieved for devices on all three wafers. This suggests that the equivalent circuit model is valid and reliable for parameter extraction of capacitance C and conductance G. The dielectric constant and loss tangent can be calculated by equation 3.3 and 3.4, respectively. The important thing to notice is that the extracted C and G represent the dielectric properties of the dielectric medium, which are different from the measured C_m and G_m in HF/LF C-V measurement due to three elements model for actual capacitor.

Fig 5.10 shows the optimization results of wafer 2364. Error function is even less than 0.1% at frequency of 65GHz to ensure the precision of the parameters extraction, which is much less than that reported in literature. It is desirable to keep the capacitance constant over the frequency range as wide as possible. The distribution of dielectric constant and loss tangent are displayed in fig 5.11 and fig 5.12. High dielectric constants, 20.59, 21.86 and 21.06 were achieved for MIM capacitors of area 100 μm^2 at 65 GHz on wafer 2366, 2285 and 2364, respectively. While measured under dc condition with zero bias, the dielectric constants were 21.08, 22.50 and 22.71 for the corresponding wafers when interface capacitances are ignored in evaluating κ. High capacitance densities ranging from 45.56 to 48.36 $fF/\mu m^2$ were obtained at 65GHz. The high capacitance densities are resulting not only from thin physical thickness of dielectric films, but also from high dielectric constants. The dielectric constant is less dependent on frequency and remains almost constant throughout the whole frequency range up to 65GHz. The capacitance reduction is limited within 2% indicating the excellent performance in microwave applications. This is of great importance for gate dielectric in CMOS technology in microwave applications. Also, the loss tangent is below 0.001 over almost the whole frequency range.

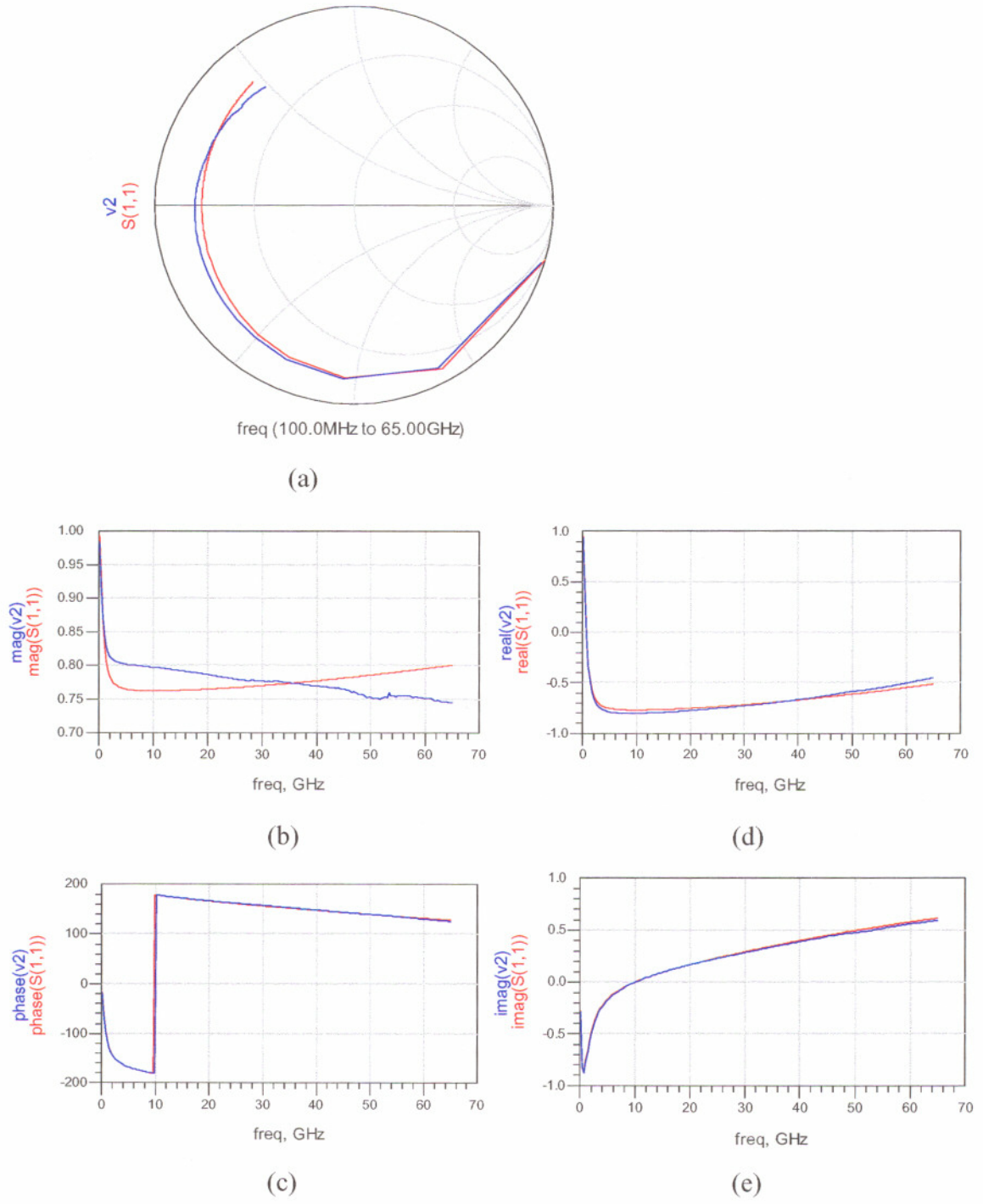


Figure 5.10: A good match between simulated and measured S-parameter for 40 Å HfO_2 MIM in wafer 2364. (a) Smith chart (b) Magnitude (c) Phase (d) Real part (e) Imaginary part.

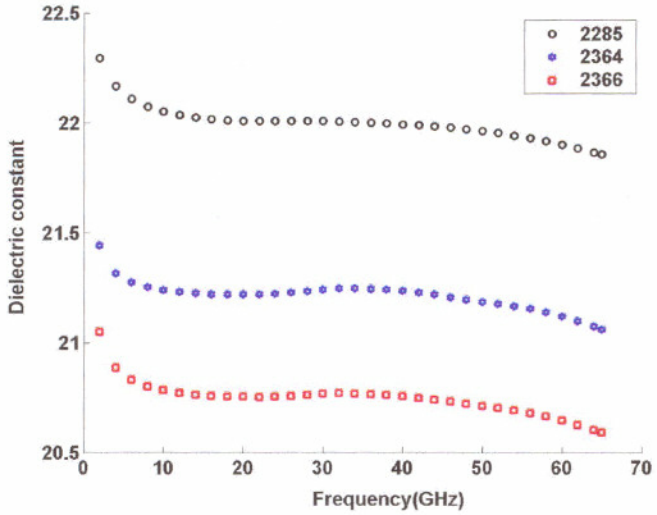


Figure 5.11: The frequency-insensitive dielectric constants were achieved in 40 Å HfO_2 MIM capacitors.

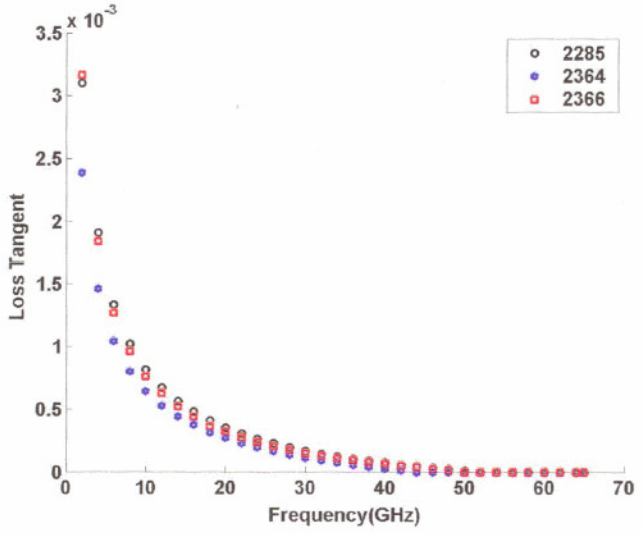


Figure 5.12: Plot of loss tangent as a function of frequency.

5.3.2 Capacitance variation and breakdown electric field

Besides the high value of capacitance density and permittivity of gate dielectric, additional parameters of importance to precision CMOS design are the sensitivity of capacitors to area and area-to-perimeter ratio. The linear relationship between capacitance and capacitor area is required for CMOS design. As shown in fig 5.13, the excellent linear relationship exists in HfO_2 MIM capacitors over the entire frequency range. Table 5-2 also shows that the area-to-perimeter ratio of the capacitors does not have an impact on the capacitance.

In addition, it is necessary to study the variation of capacitance per unit of capacitor length or width over a wide frequency range. There are different sets of length and width used to pattern the MIM capacitors. For example, for the device of 10um length, we designed the widths of 10 μm, 20 μm, 30 μm 40 μm and 50 μm, respectively. These devices are used to explore the capacitance variation based on the effect of different width. The distribution of capacitance changing with length or width at different frequencies is displayed in Fig 5.14. It is obvious that frequency-dependent capacitance reduction per unit of length or width is very small. The maximum difference is 0.005pF/μm for width and 0.009pF/μm for length. This characteristic of frequency-independent and size-insensitive dielectric film is the fundamental guarantee of the MOS device working on microwave regime.

For gate dielectric application, it is also important to characterize its breakdown electric field. The breakdown field for HfO_2 film is 7.7 MV/cm, which is a little lower than that of thermal silicon dioxide. Fig 5.15 shows the distribution of breakdown field at different capacitor area. Fig 5.16 gives the characteristic of leakage current density for wafer 2366. This leakage current density is a little higher than reported in literature [7].

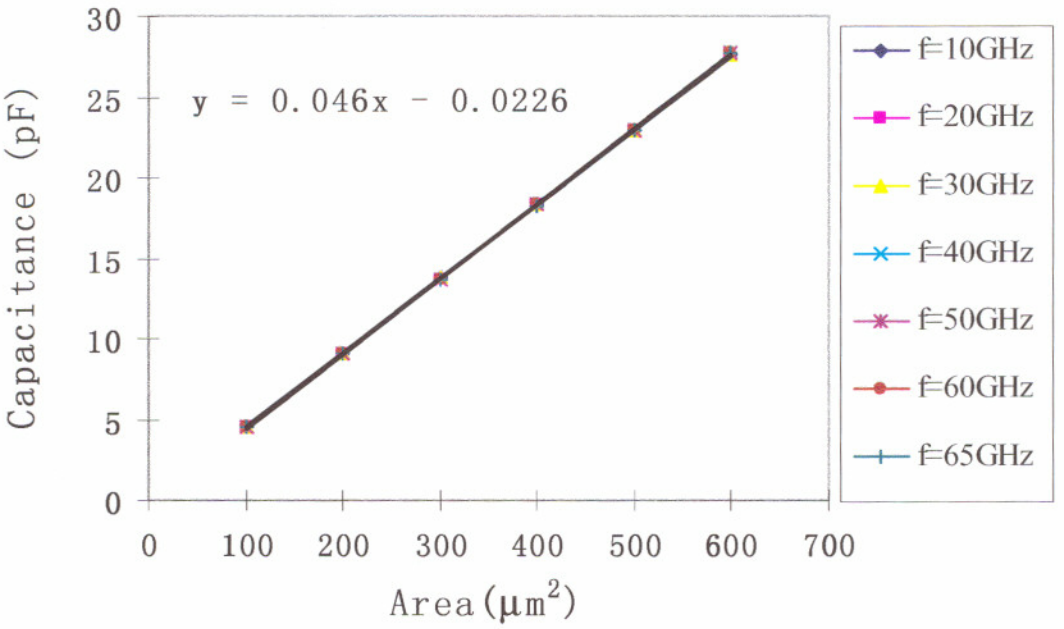
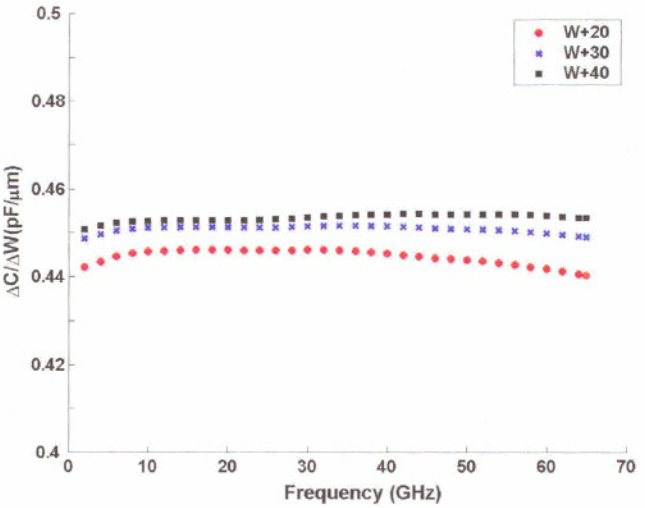


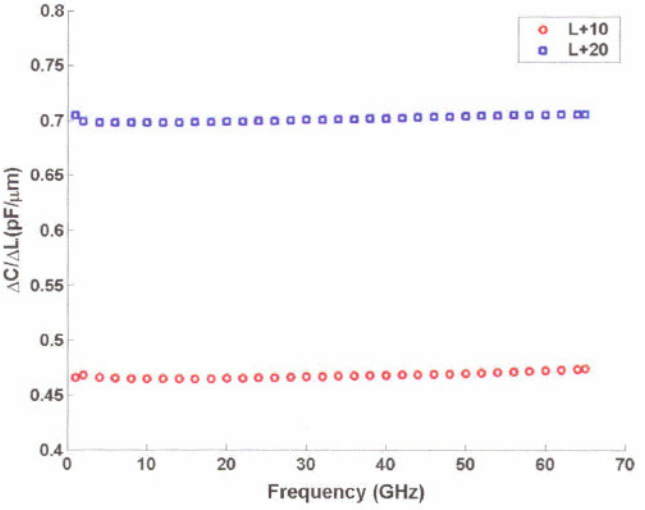
Figure 5.13: The plot of capacitance versus capacitor area shows linear relationship all over the frequency range in 40 Å HfO_2 MIM capacitors.

Table 5.2: The effect of area-to-perimeter ratio on capacitance

Cell ID	Area (μm^2)	C (pF)
11	100	4.520
21	100	4.539
31	100	4.560
13	300	13.625
22	300	13.624
15	500	22.716
23	500	22.703
32	500	22.778
25	900	40.666
33	900	40.799
17	1100	50.113
26	1100	49.582
27	2100	94.901
36	2100	94.337



(a) Width effect on MIM capacitance



(b) Length effect on MIM capacitance

Figure 5.14: Effect of the size of dielectric film on MIM capacitance

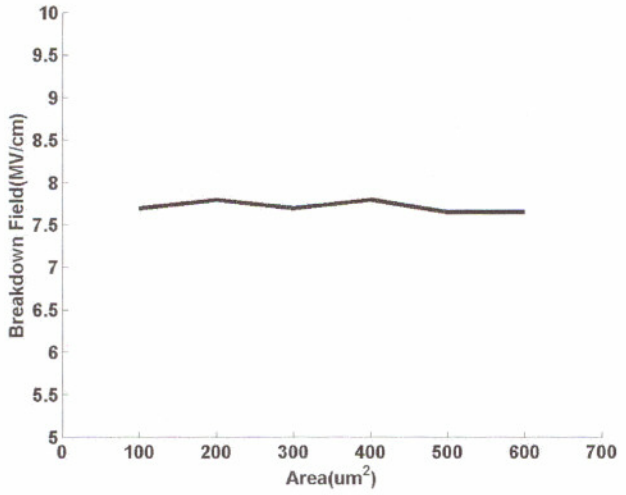


Figure 5.15: The distribution of breakdown electric field in wafer 2366.

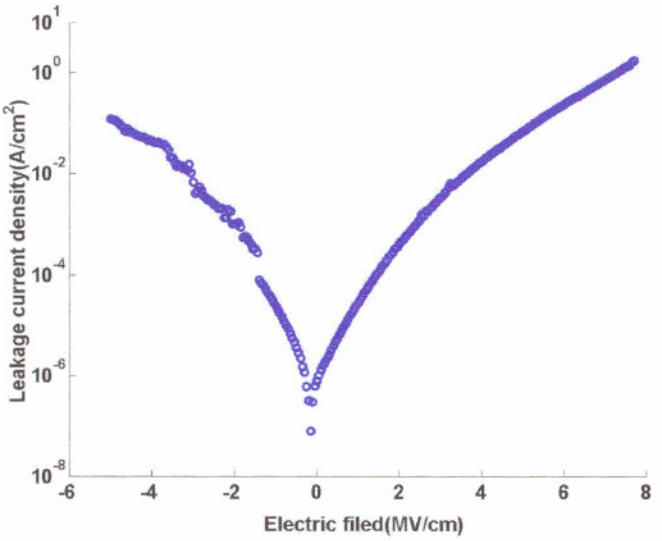


Figure 5.16: J-E curve with a positive dc bias applied at the top electrode for MIM capacitor in wafer 2366.

5.4 Conclusion

High performance MIM capacitors with HfO_2 dielectric film prepared by atomic layer deposition have been demonstrated and successfully characterized over the frequency range of 100MHz to 65GHz. An optimization technique is applied to extract the intrinsic capacitance. An excellent match between simulated and measured S-parameter in the optimization exists over all the frequency range up to 65 GHz. The equivalent circuit model is proved to be valid and reliable to extract the parasitic parameters in microwave regime. We achieved high capacitance densities of 46 $fF/\mu m^2$ and dielectric constant of 21 at 65GHz. The good dielectric quality has been supported by the considerably low dispersion and loss tangent. Non-dispersive behavior of MIM is also essential for precision analog circuit design [8]. In addition, both the linear relationship between capacitance and capacitor area and low sensitivity of capacitors to area-to-perimeter ratio suggest that HfO_2 is a promising gate dielectric alternative to SiO_2.

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CHAPTER 6: FUTURE WORK

The low-frequency and high-frequency responses of the high-κ dielectrics have been investigated in this dissertation. However, all of above characterization are based on MOS capacitors and MIM capacitors. There is still a long way to go for completely characterizing high-κ material for logic applications. Some problems arising from applying high-κ material in CMOS technology have not been explored yet. The switch to high-κ material may be the most significant change in future generations. The next phase of work has to be focused on the characterization of MOSFETs with high-κ gate insulator.

The shift to high-κ gate dielectric may solve the gate leakage issue resulting from the scaling of gate oxide thickness, it can, however, lead to new undesired effects that do not exist in thermal SiO_2 gate insulator. Two major problems that have been reported are: (1) channel mobility degradation (2) dielectric relaxation in high-κ materials.

6.1 Mobility degradation

It has been reported that high-κ/poly-Si transistors exhibit severe channel mobility degradation [1-2]. Furthermore, there have been a series of problems setting the proper threshold voltage due to Fermi-level pinning [3], especially for P-MOSFET. The various physical scattering mechanisms are attributed to channel electron mobility in the high-κ materials. Robert Chau [4] recently reported that the surface phonon scattering was the primary cause of electron mobility degradation in the HfO_2 dielectric. This phonon scattering goes away when a gate is made from a specific metal material. The metal-gate electrode material can also provide desirable work functions for both n-channel and p-channel MOSFETs. Therefore, it is necessary to check the channel mobility for high-κ/metal-gate MOSFET. The effective electron mobilities can be measured as a function of temperature and transverse electric field (E_{eff}), as shown in fig 6.1. For MOSFET characteristics, the family of I_d-V_{ds} and the subthreshold I_d-V_{gs} characteristics of n-

channel and p-channel MOSFET's are shown in fig 6.2. The subthreshold slopes of the long-channel high-κ transistors may also suggest the amount of interface traps present [5].

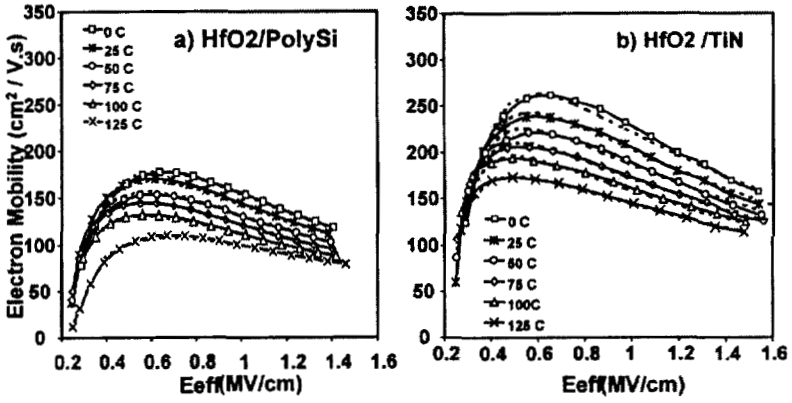

Figure 6.1: Measured and modeled data as a function of temperature and E_{eff} for (a) HfO_2/poly-Si and (b) HfO_2/TiN gate stacks.

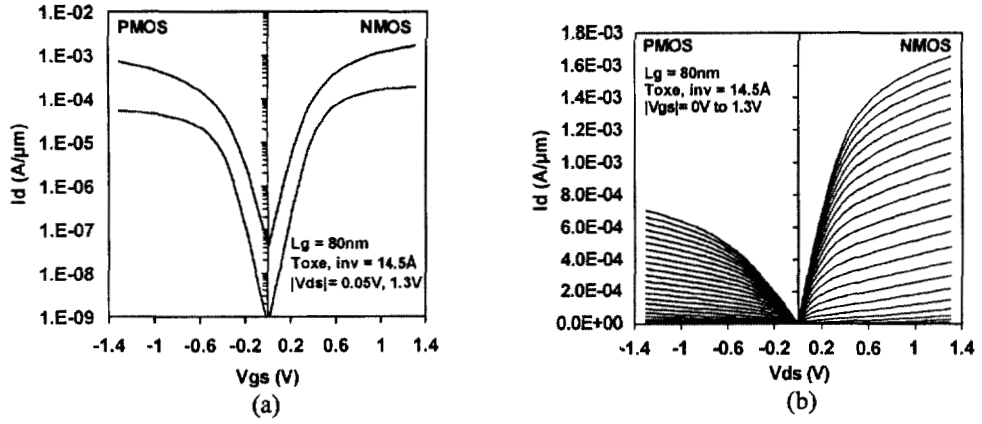

Figure 6.2: MOSFET characterization (a) Subthreshold I-V curves for PMOS and NMOS with high-κ/metal-gate (b) Family of curves for PMOS and NMOS with high-κ/metal-gate.

6.2 Dielectric relaxation

Dielectric relaxation (DR) is not a new concept. When the electric field is removed, the polarization is reduced gradually due to dipole's random interactions with the other molecules through molecular collisions, lattice vibrations. DR represents this sluggishness of the dipole response to the applied field. Reisinger's first discussion of DR on high-κ materials in IEDM at 2001 attracted more attention [6]. Reisinger suggested that a residual polarization effect in high-κ dielectric was much larger than that in SiO_2. This may cause serious device integration problem since DR causes threshold voltage shift over time. Two years later at IEDM, the Stanford group [7] explained DR phenomenon by the model of electron tunneling through a double well potential in amorphous materials. They suggested the material couldn't be made perfect to avoid this effect. However, an IMEC researcher commented that DR could be suppressed after his group put in an interface layer.

DR was regarded as the property of the material and found to follow a power law dependence known as the Curie-von Schweidler law [8]. The relaxation effect was observed more in the film annealed or deposited at higher temperatures in the study of Lingwal [9]. In the microwave region, the dielectric characteristics are most often dominated by slowly varying dielectric relaxation. The equivalent circuit was often employed to describe DR, as shown in fig 6.3 [10]. The new study of IMEC [11] confirmed that electron trapping and de-trapping in the high-κ dielectric stacks caused the dielectric relaxation current. They investigated the thickness dependence, gate voltage polarity dependence and temperature dependence of the relaxation currents in high-κ dielectric stacks and concluded that the traps located near the SiO_2/high-κ interface was the root cause of dielectric relaxation currents. Meanwhile, this study, one more time, emphasizes the importance of the interface between high-κ dielectric and silicon substrate on the successful application of high-κ material on CMOS logic technologies.

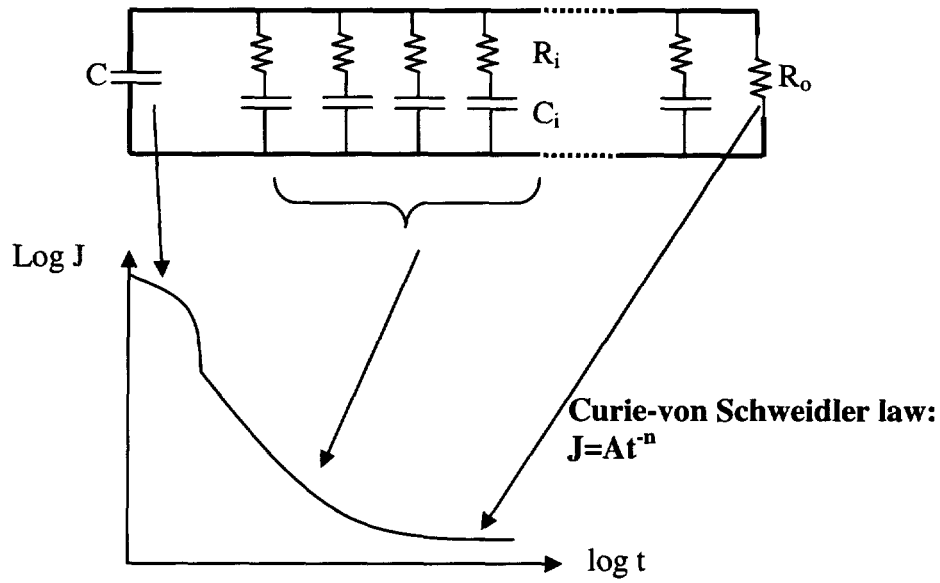

Figure 6.3: The equivalent circuit explaining dielectric relaxation. C is intrinsic film capacitance which immediately responds to the change of an applied voltage. R_o is DC resistance. Each pair of R_iC_i represents dielectric relaxations with relaxation time R_iC_i.

6.3 High frequency measurement on MOSFETs

High frequency characterization can be carried out on MOSFETs by two-port RF measurement. The equivalent circuit model of MOSFET is shown in Fig 6.4. With the similar optimization technology discussed at chapter 5, the parameters of MOSFET are extracted like MIM capacitor. This measurement methodology can also be applied to plot C-V curve at microwave range. At each frequency sweep, the intrinsic gate capacitance can be extracted. If a given bias is applied at each frequency sweep, one set of gate capacitance and gate bias is obtained. By applying a series of different gate bias, a series of gate capacitances and gate bias are acquired to plot the C-V curve.

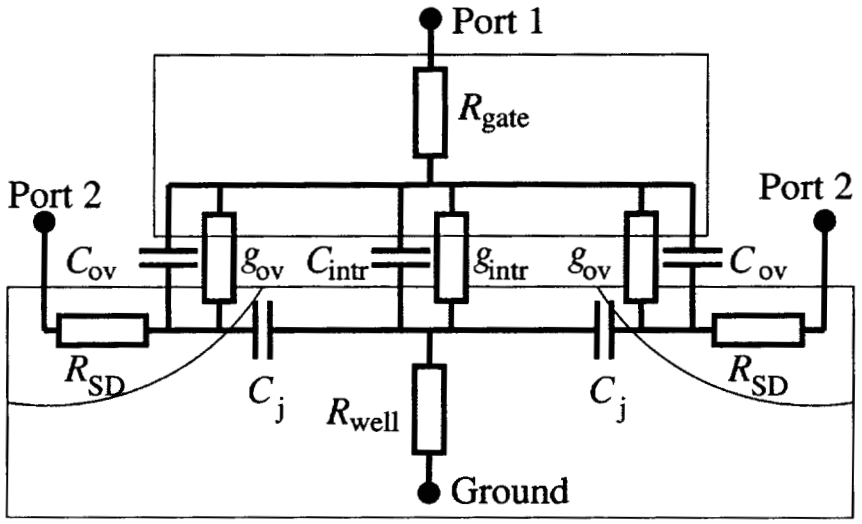

Figure 6.4: An equivalent circuit model of MOSFET in accumulation.

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BIOGRAPHICAL SKETCH

Weiming He was born in Shanghai, China. He earned a Bachelor degree in Material Science from Shanghai Jiao Tong University in 1991. He then worked as process engineer in semiconductor industry until he had chance to continue his graduate study in United States in 1998. Weiming earned Master degree in Materials Science from Auburn University in 2000. He got employment in Oregon and worked as device engineer in Fujitsu Microelectronic Inc. This position resumes his interest in component research. Weiming joined Ph.D. program at the Oregon Graduate Institute of Science and Technology in the Spring of 2002 where he pursued a doctoral degree in Electrical Engineering until he graduated in 2004. During the time in Oregon, he got two daughters: Amanda and Estelle.