The Sputtered Au/Pt/Ti Thin Film Stack for GaAs Metallization: Microstructure, Stress, and Surface Roughness

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The dissertation "The Sputtered Au/Pt/Ti Thin Film Stack for GaAs Metallization: Microstructure, Stress, and Surface Roughness" by Zhenkun Ren has been examined and approved by the following Examination Committee:

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Dedication

In memory of my grandmothers Rugui Zhang and Taohua Wang

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Abstract

The Sputtered Au/Pt/Ti Thin Film Stack for GaAs Metallization: Microstructure, Stress, and Surface Roughness

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Au/Pt/Ti multilevel film is the most widely used metallization scheme in GaAs ICs. The traditional way to deposit Au/Pt/Ti films is evaporation, which suffers from low throughput, low yield and high level of contamination. Recently, sputtering has been adopted as another choice of deposition method and has been demonstrated to be superior in yield and throughput compared to evaporation. This research studies the properties of the sputtered Au/Pt/Ti film including microstructure, surface morphology and residual stress and also their effects on the metallization's performance and reliability.

FIB produced TEM cross-sections have been extensively employed to examine the microstructure of the sputtered Au films. It was showed that the grain size, defect density varies significantly as the film growth proceeds due to the cumulative effect of energetic particle bombardment. The residual stress of the sputtered Au film at a series of thicknesses was measured by substrate curvature method and the stress dependency on film thickness is associated with the microstructure evolution.

The thermal-mechanical behavior of the individual Au, Pt, Ti films as well as the multifilm structures including Pt/Ti and Au/Pt/Ti were studied by thermal cycling the films/SiO_2/Si wafers inside Tencor FLX2320. The stress relaxation mechanisms of Au film were studied by quenching the specimens at specific temperatures during thermal cycling and subsequently producing cross-sections for TEM observation. It is found that

thermally assisted dislocation glide, coupled grain boundary diffusion and surface diffusion dominants the relaxation process. Grain growth has minor contribution to the relaxation process.

The mechanisms of nanoscale hillock formation in silicon nitride passivated sputtered Au/Pt/Ti film is the emphasis of this research. The hillock topography and cross-section were characterized by AFM and TEM respectively. It is proposed that the hillocks are formed by the localized deformation and delamination of silicon nitride film under compression, which includes the stress imposed by the relaxation of the underlying Au film as well as the thermal mismatch stress introduced upon cooling. The primary factors affecting the hillock formation include the surface roughness of the as-deposited metal film, and the adhesion between metal and dielectric film.

1 Introduction

Au/Pt/Ti multilevel metallization scheme has been widely used in GaAs circuitry as the gate metal for MESFET, interconnects, and also electrical contacts for passive devices such as MIM capacitors. Generally this thin film stack is deposited in a large batch-style dome system based on evaporation, which lacks automation and involves lots of manual wafer handling. Although adequate for small volume production, evaporation is certainly not a good choice for large volume production due to several major drawbacks including high level of particulate contamination, low yield and low throughput. Another common technique that has been used to deposit metal films for integrated circuits is sputtering, which is generally performed in the single-wafer processing system that employs a load-lock systems and cassette-to-cassette cluster tools. This process configuration is completely automated hence the deposition is carried out in a rather small and well-controlled chamber. Over the years, sputtering has been well developed and has become a successful metallization deposition technique for the Si industry. However, it cannot be directly transferred to GaAs circuits because this process suffers from lack of directionality, which is required by the specific lift-off patterning technique utilized by GaAs circuits processing. Recently, by optimizing several process parameters, sputtering has been successfully introduced as an alternative metallization method for GaAs ICs and has been demonstrated to be superior in yield and throughput compared to the traditional evaporation.

The microstructure, mechanical properties, and electrical properties of the sputtered metal films are different from those of the evaporated ones and these differences have significant influences on device performance and reliability. One

purpose of this study is to examine the material properties of the sputtered metal film, especially properties of Au film, and then associate them with the sputtering mechanism.

It is not surprising that new problems always emerge with the advance of technology. One problem we have encountered in the new sputtering process is the nano-hillock formation in the silicon nitride passivated Au/Pt/Ti films. The hillock formation imposes a reliability problem specifically in MIM (Metal-Insulator-Metal) capacitor application because the dielectric could be penetrated during the formation of the hillock if these hillocks are materials coming out from the underlying metal film. Another possibility is that the hillocks only exist in the dielectric layer. Even so the hillock formation still modifies the dielectric morphology which affects its electrical properties. Therefore another objective of this study is to understand the hillock formation mechanism. The fabrication of MIM capacitor consists of three steps: 1. Sputtering the bottom Au/Pt/Ti film stack. 2. Depositing an ultra-thin silicon nitride dielectric by PECVD (Plasma Enhanced Chemical Vapor Deposition) at elevated temperature. 3. Sputtering the top Au/Pt/Ti film stack. AFM (Atomic Force Microscope) examination of the metal and dielectric surface shows that the initial bottom Au film has a relatively flat surface with uniform roughness across the examination area, while after step two hillocks are present on the dielectric film. In comparison, hillock formation never occurred when evaporation was used to deposit the metal films. The electrical testing shows that the breakdown voltage of capacitor with sputtered contacts are degraded compared to those with evaporated ones.

Hillocks were frequently observed in Si metallizasions. Over the years, it has been extensively studied because this is a major yield and reliability-limiting factor. The most common hillocks are annealing hillocks, which generally formed in metal films during the cyclic heating and cooling. These thermally induced hillocks have been reported in several metal films such as Al, lead, and Au. It is believed that the annealing hillocks are generated as a result of the relaxation of compressive stress within the metal film, which is caused by the thermal expansion coefficient mismatch between film and substrate. The formation of hillocks relieves the strain energy of the film, thereby reducing the compressive stress. The hillocks stated here are different from the annealing hillocks in the following aspects: 1. The previously reported hillocks usually are very

huge (a few micron in height), while the hillocks we found are in nanoscale (about 70Å in height). However, with the continued down scaling of the dielectric thickness, these tiny hillocks could also cause potential reliability problems. 2. The annealing hillocks are formed in metal film on semiconductor substrate without the top dielectric film. While in this case, the presence of silicon nitride is a key factor that induces the hillocks. Based on the current hillock formation theories, it is suspected that the formation of the hillocks is related to the stress relaxation within the metal and dielectric film. Further investigation is carried out to gain insight into the hillock formation mechanism.

This thesis contains eight chapters including this introduction. Chapter 2 briefly describes GaAs materials properties and the basic device operation principles for schottky contact and MESFET (Metal Semiconductor Field Effect Transistor). Chapter 3 discusses several important issues regarding GaAs circuit metallization. These include the common GaAs metallization systems, metallization design consideration, and metal deposition techniques including evaporation and sputtering, and also the metallization reliability.

The experimental procedures employed in this thesis are described in chapter 4. These include Au/Pt/Ti film deposition, Transmission Electron Microscopy (TEM), Atomic Force Microscopy (AFM), stress measurement and electrical parameters testing.

Chapter 5 discusses several important material properties of the as-sputtered Au/Pt/Ti film including microstructure, intrinsic stress, resistivity and their correlations.

In chapter 6, the stress relaxation mechanism of sputtered Au/Pt/Ti film during thermal cycling is studied. TEM technique is used to examine the microstructural evolution of the Au film during thermal cycling.

Chapter 7 deals with the hillock formation problem in the passivated sputtered Au/Pt/Ti film. In this chapter, the hillock formation mechanism is explored by examining the microsturctural and interface features of a FIB produced TEM cross-section at a hillock site. The hillock formation dependence on the bottom Au thickness is presented. Finally, the effect of hillock on the MIM capacitors electrical performance is treated. This chapter also compares the evaporated and sputtered Au/Pt/Ti film from several aspects such as microstructure, stress, and hillock formation tendency.

Summary and conclusions of this thesis are presented in chapter 8.

2 GaAs Devices

Si and GaAs are the most important semiconductors for high-speed devices in modern electronic applications. Si was developed much earlier than GaAs and has become the most popular and widely used semiconductor due to its capability of fabricating dense and fast microcircuits at relatively low manufacturing cost. However, GaAs has higher electron mobility and effective carrier velocities, which make it very competitive with Si in high-speed discrete devices and integrated circuits such as microwave, optoelectronic, and some digital applications. In this chapter, we will first describe the crystal structure and electrical properties of GaAs, and then discuss the physics of the Schottky contact and MESFET due to their close relationship to this research.

2.1 Material Properties of GaAs

GaAs is our most familiar III-V compound semiconductor. It has the zincblende lattice which can be represented by two interpenetrating fcc lattices. As shown in Fig. 2.1, the fcc lattices of Ga and As has been shifted relative to each other by a quarter length along the body diagonal. This zincblende structure can also be regarded as one fcc unit cell with two basis atoms at each lattice point, one is Ga another is As.

The chemical bonds between Ga and As atoms are covalent bonds rather than ionic. Five of the outer shell electrons are contributed by Ga and three by As. The bonding of GaAs is illustrated in Fig. 2.2. At absolute zero, there are no free electrons available for current conduction. When temperature increases, some electrons, which possess enough thermal energy to be excited from the covalent bond, become free and

can contribute to current conduction. Each liberated electron leaves behind an electron vacancy or empty energy state which is referred to as a hole. A nearby electron can hop into this hole and generate another hole which is available to be filled by another electron. The flow of holes is another description of current flow except the fact that it is in the opposite direction of electron movement. From the nature of hole generation, it is straightforward that both the electron and hole concentrations at 0 K should be equal to the semiconductor's intrinsic concentration.

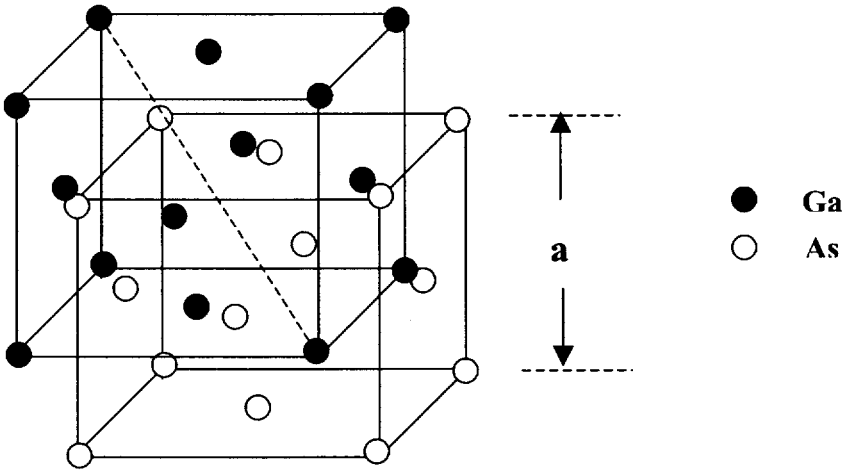

Figure 2.1 GaAs zincblende lattice structure

(W. Liu, Fundamentals of III-V Devices: HBTs, MESFETs, and HFETs/HEMTs, Wiley-Interscience, 1999, p. 6, reprinted by permission of publisher.)

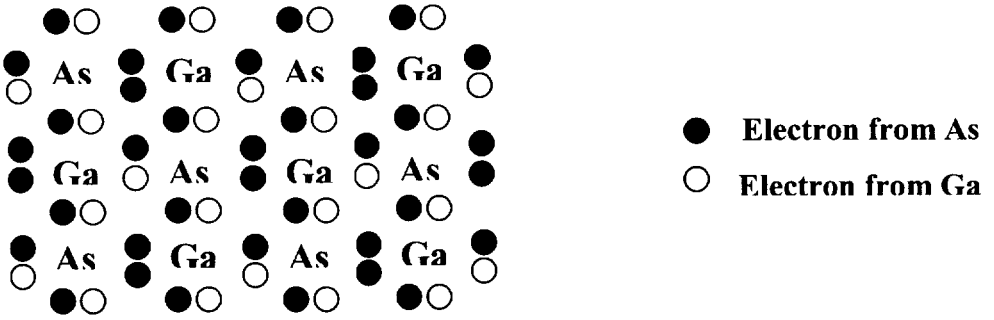

Figure 2.2 Schematic diagram showing the atomic bonding in GaAs

(W. Liu, Fundamentals of III-V Devices: HBTs, MESFETs, and HFETs/HEMTs, Wiley-Interscience, 1999, p.9, reprinted by permission of publisher.)

Only a small fraction of electrons can be thermally excited from valence band to conduction band at room temperature. To have a better control of the semiconductor's conductivity, substitutional impurities are incorporated into the pure semiconductor to vary the mobile carrier concentrations. For instance, Si (four outer shell electrons) is the most frequently used dopant for GaAs devices. If a Ga atom is replaced by a Si atom, an additional free electron will be generated and wander about the crystal to contribute to electrical conduction. This will make Si doped GaAs an n-type semiconductor. If instead an As site is occupied by a Si atom, a lack of one electron in the bond with the adjacent Ga will make the material p-type. Therefore, Si can behave as a donor or acceptor with a change in the lattice site occupied. As illustrated above, the conductive property of a semiconductor can be modified greatly by controlling the dopant type and doping levels.

Unlike Si, GaAs is a direct band gap semiconductor, which means its valence band maxima and conduction band minima corresponds to the same wave vector. Because of the direct gap nature, photons can be absorbed or emitted by GaAs depending on whether it is a carrier generation or recombination process. This special characteristic makes GaAs a very useful material in optoelectronic applications.

The most important beneficial feature of GaAs that makes it a preferable choice in high-speed device application is its high electron mobility. A useful estimation for μ_n in low-doped GaAs was proposed by Blakemore [1]:

$$\mu_n = 8000\left(\frac{300}{T}\right)^{2.3} \frac{cm^2}{V-s} \qquad (2.1)$$

and the drift velocity of electrons can be represented by equation 2.2:

$$\upsilon_d = \mu_n E \qquad (2.2)$$

where E is the applied external electric field. At room temperature, μ is roughly 8000 cm^2/V-s in lightly doped GaAs, which is much higher compared to the electron mobility of 1417 cm^2/V-s in a low-doped Si with Arsenic impurities [2].

Another advantage of GaAs over Si is its semi-insulating nature, which can provide low interconnection capacitances in IC circuits.

2.2 Schottky Contact

Most of the electronic devices are connected by means of metal-semiconductor contacts. Basically, two types of contacts have been studied with great interest by lots of researchers: ohmic contacts (low resistance) and schottky (rectifying) contacts. These are also the major contacts used for active devices.

The series resistance of an ohmic contact at the metal-semiconductor interface is very small and can be neglected during the device operation. The low resistance property makes it a crucial component in many GaAs devices such as MESFET, LED, lasers, and solar cells. However, since this research concerns itself with Au/Pt/Ti multilevel metallization system which is primarily used for schottky contact in MESFET devices, this section will concentrate on the operation of a schottky contact.

Schottky contact was first presented by Schottky in 1938 [3]. When a metal and a semiconductor are brought into intimate contact, a barrier to electron and hole flow is formed. If the barrier is not narrow enough to permit the occurrence of direct field emission (tunneling), a schottky barrier has been built. A band diagram of a schottky barrier is shown in Fig. 2.3. To draw a clear picture of the schottky model, it is necessary to restate several important definitions here. The vacuum or free-electron energy E_0 represents the energy level an electron would have if it were just free of the influence of the given material and with a zero kinetic energy. The work function of a metal Φ_m is the energy needed to move an electron from the Fermi level (E_f) of the metal to the vacuum level. Similarly, incase of semiconductor, this energy difference between E_0 and E_f is referred to as the semiconductor work function Φ_s. Instead of being a constant, Φ_s is a function of the semiconductor doping concentration since E_f varies with the doping level. Another important quantity that does not depend on doping is the electron affinity χ_s, which is defined as the energy difference of an electron between vacuum level and the lower edge of the conduction band.

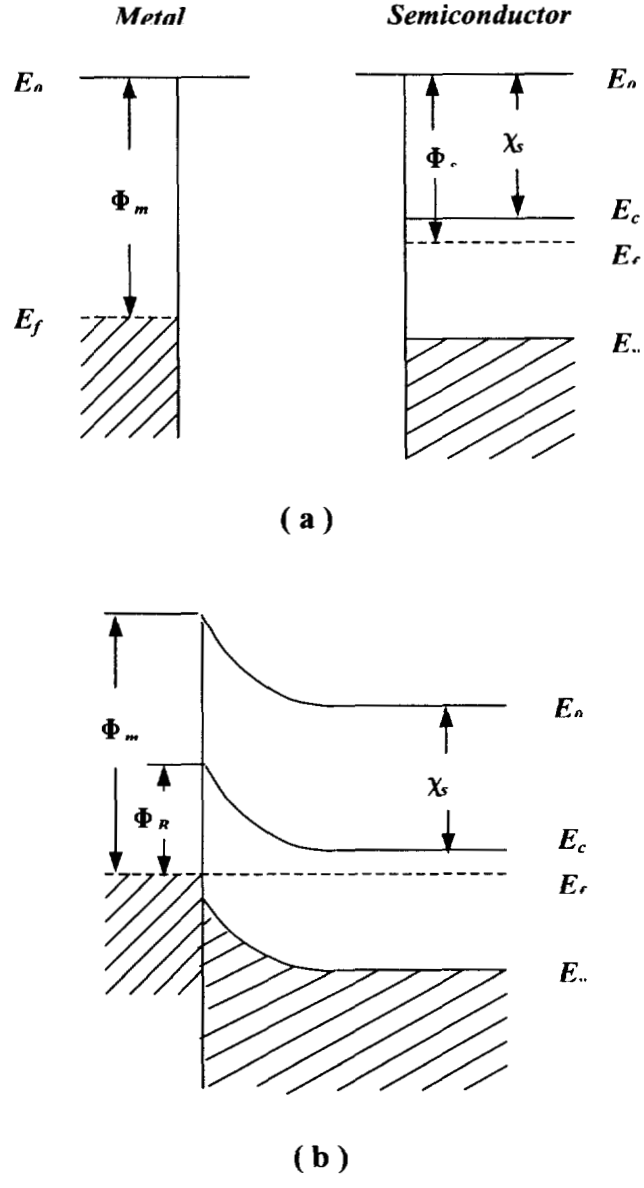

Figure 2.3 Band structure of Schottky contact to n-type semiconductor with $\Phi_m > \Phi_s$. (a) band diagram for metal and semiconductor separated from each other. (b) idealized equilibrium band diagram for a Schottky contact.

If we consider a certain metal and semiconductor in Fig. 2.3(a), it is obvious that in this case, $\Phi_m > \Phi_s$, which means that the average energy of electron in the semiconductor is higher than that in the metal. At thermal equilibrium, the disparity of

electron energy will cause the transfer of electron from the semiconductor into the metal until the Fermi level on both side coincides. An intrinsic electric field established by the positive ions left in the semiconductor and electrons flowing into the metal will prevent the further electron transfer. The resulting band structure near the contact region is shown in Fig. 2.3(b). It is evident from the band structure that the barrier height Φ_B under thermal equilibrium can be represented by:

$$\phi_B = \phi_m - \phi_s \qquad (2.3)$$

When an external electric field is applied across the contact, this barrier can be either reduced or increased depending on whether the additional field is forward or reverse bias. Additional current starts flowing cross the contact due to the disturbance of the thermal equilibrium condition. The current-voltage characteristics predicted by the thermionic model are given by [4]:

$$J = J_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \qquad (2.4)$$

where J_0 is the saturation current and n is the ideality factor.

From equation 2.3, barrier height Φ_B should be proportional to the metal work function. However, schottky diodes formed on many of the III-V compound semiconductor do not show this behavior. Strong dependence of barrier height on metal work function is observed predominately in ionic semiconductors. In many covalent semiconductors Φ_B is less sensitive to Φ_m or virtually independent of Φ_m [5]. This is thought to be due to the "Fermi level pinning" at the semiconductor surface. Lots of investigation has been done in this field and selected researcher's explanation will be presented here. In 1947 Bardeen [6] proposed that if the localized surface states exist at the metal-semiconductor interface in sufficient numbers (greater than 10^{13} cm^{-2}), the barrier height would be insensitive to the metal work function. He characterized the continuously distributed surface states by a neutral level Φ_0, and found that $\Phi_B = E_g - \Phi_0$, which is referred to as Bardeen limit. Tamm [7] and Shockley [8] have shown that these surface states could be intrinsic to the semiconductor surface. However, other studies showed that there are no detectable intrinsic surface states in the band gap of well-cleaved GaAs [9,10]. Spicer et al [11,12,13] proposed the unified model, in which surface states are associated with native defects (acceptor or donor). In single defect

model, Grant et al [14] suggested that the surface states are associated with a single defect near or at GaAs surface. Quite different from the above opinions, Brillson [15] argues that the metal/semiconductor interfaces are not atomically abrupt, but contain reacted interfacial regions or interdiffused regions which govern the schottky barrier behavior. Woodall and Freeouf [16] extended Brillson's model and pointed out that the fermi level position at the interface is not controlled by surface states density but rather is related to the work functions of microclusters of one or more interface phases.

The previous discussion shows that the understanding of the metal-semiconductor interfacial phenomena is fundamental to schottky barrier operation. Due to the "Fermi-level pining", the majority of metals used in integrated circuits produce schottky barrier with only a small spread in barrier height [17]. Consequently, the choice of metal for schottky barrier hinges on other reliability considerations such as metal-semiconductor interdiffusion, high temperature stability and electromigration.

2.3 MESFET

GaAs does not have a high quality native oxide that can be easily grown just like Si does. Recently, extensive study has been carried out trying to find an optimum oxide for GaAs, but most of the oxides end up with high density of surface states, which make it difficult to fabricate GaAs MOSFET (Metal Oxide Semiconductor Field Effect Transistor). Alternatively, schottky barrier MESFET (Metal Semiconductor Field Effect Transistor) became a successful device example that has been practically used in GaAs circuits.

A typical MESFET structure is given in Fig. 2.4. As shown in Fig. 2.4, MESFET is a three terminal devices with a schottky barrier positioned between two ohmic contacts. The GaAs below the contact metal is usually n-type doped and is the major current conducting layer, which we call channel. Below the channel is a semi-insulating buffer layer whose main function is to prevent the leakage current flowing between channel and substrate. The metal contact of the schottky barrier which is called gate can modulate the amount of depletion width into the channel region, allowing more current to flow when depletion is small and vice versa. The two ohmic contacts beside

gate are referred to as source and drain respectively. Their negligible resistances make them suitable to source and collect the current flowing in the channel.

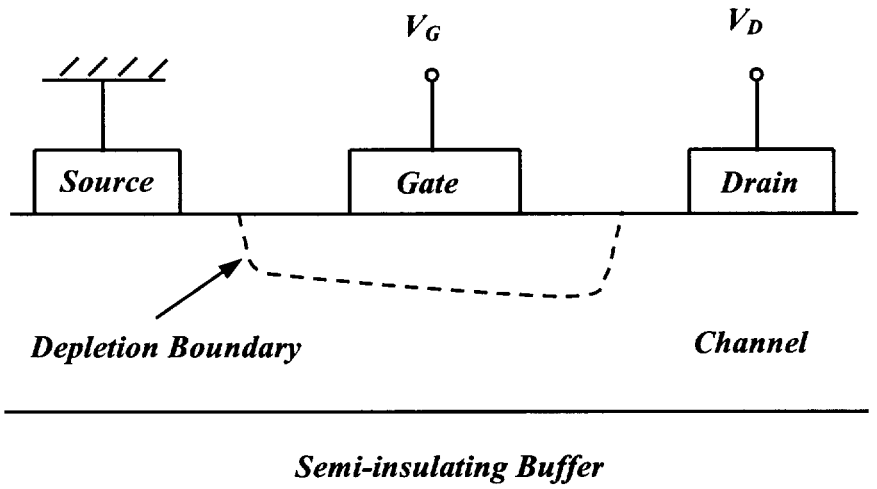

Figure 2.4 Cross section of a GaAs MESFET structure.

If the thickness of the channel layer is smaller than the zero bias depletion width, the channel is cut off and there is no current flowing between source and drain. Positive gate-source voltage V_{GS} can be applied to reduce the depletion width and form a conductive channel. This kind of MESFET is normally off and is annotated as enhancement-mode MESFET (E-MESFET). Conversely, if the channel layer is thicker than the depletion width, then the device is normally on and negative V_{GS} must be applied to turn off the device. This device is annotated as depletion-mode MESFET (D-MESFET). Typical I_{DS}-V_{GS} characteristics of E-MESFET and D-MESFET are shown in Fig. 2.5. The source-drain current I_{DS} can be controlled by varying the gate-source voltage V_{GS} and drain-source voltage V_{DS} in a similar way MOSFET does. I_{DS}-V_{DS} relationship of a MESFET is given in Fig. 2.6. The *I-V* characteristics of a MESFET can be approximated by the following equation [18]:

Linear region: $$I_{DS} = \beta\left(2\left[V_{GS} - V_T\right] - V_{DS}\right)V_{DS}\left(1 + \lambda V_{DS}\right) \quad (2.5)$$

Saturation region: $$I_{DS} = \beta\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right) \quad (2.6)$$

Where V_T is the threshold voltage and β, λ are constants dependent upon the MESFET properties. The constant β is proportional to (μ_n W/L), here μ_n is the electron mobility, W and L are gate width and length respectively. The constant λ measures the output conductance g_0 which is defined as δI_{DS} / δV_{DS}. From equation 2.5 and 2.6, higher operation speed can be achieved in GaAs IC compared to Si IC due to a bigger μ_n in GaAs.

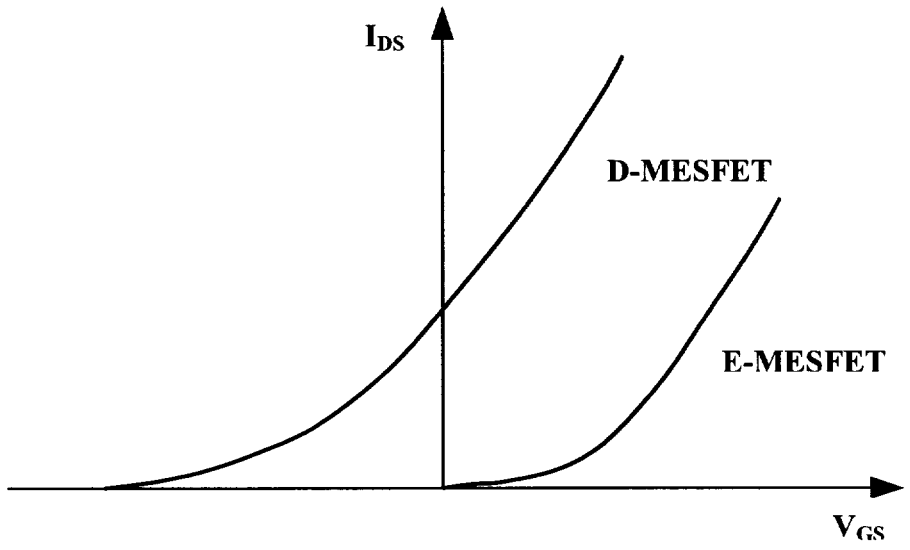

Figure 2.5 I_{DS}-V_{GS} **characteristics of E-MESFET and D-MESFET.**

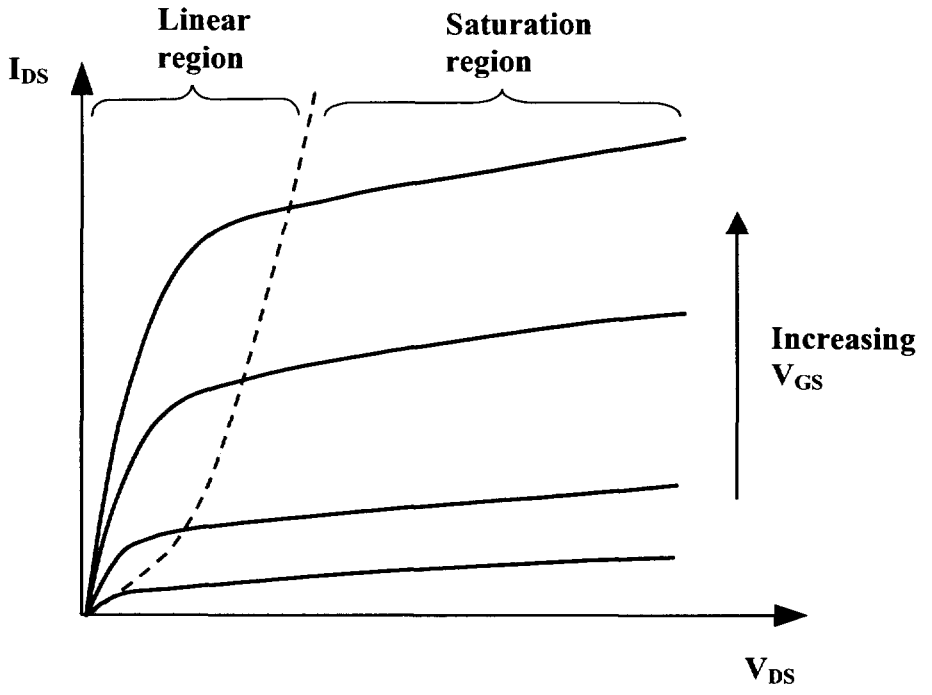

Figure 2.6 I_{DS}-V_{DS} **characteristics of a GaAs MESFET.**

MESFET is a very fundamental and critical device in GaAs IC and can be used in both analog and digital applications. The metallization for MESFET can be categorized as two blocks according to their different metallization requirements: ohmic contact metallization (negligible resistance) and schottky contact metallization (rectifying). Metallization for schottky contact using sputtered Au/Pt/Ti thin films is one of our major interests in this research.

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3 Metallization for GaAs Devices and Circuits

As the microelectronic technology progressed to twenty first century, the dimensions of semiconductor devices have been dramatically reduced from micron to sub-micron scale. The demands for electronic materials properties, process methods, circuit pattern definition, process integrity, packaging, yield and reliability issues have been tremendously increased and will continue to increase in order to further miniaturize the microchip and boost its speed. As a key component to integrated circuits, metallization not only provides interconnects between millions, even billions of devices, but also allows them to communicate with the outside world. The proper operation of the integrated circuits as expected by the IC designer greatly depends on the performance and reliability of the circuit metallization. More and more problems in metallization has arisen due to the continuous shrinking of the device dimension, such as stress, adhesion, interdiffusion, electromigration, and so on. The continued miniaturization of the semiconductor devices inevitably requires both the improvement of the current technology and development of new metallization schemes. In this chapter, we will first give a brief introduction to the GaAs metallization systems and discuss the specific metallization design considerations for different systems respectively. The metallization fabrication technology will be summarized. Finally and most importantly, we will deal with yield and reliability issues that are also the hearts of volume production. The application of Au/Pt/Ti thin film metallization scheme in GaAs IC will be highlighted through this chapter since it is the focus of this research.

3.1 GaAs Metallization Systems and Design Considerations

In integrated circuits, almost 50% of the chip area is covered by interconnects and contacts. Any defects such as short or open circuits can cause the failure of the whole circuit. So, the primary consideration during the metallization design is to provide the desired device electrical properties and precise connection between these devices.

GaAs does not have a stable native oxide just like Si does; hence, MESFET became the most predominant device used in production volume GaAs ICs. As illustrated in section 2.3, the source and drain of a MESFET are formed by ohmic contacts and the gate is formed by a schottky barrier. Therefore, the GaAs metallization system can be classified as three major components: (1) ohmic contacts, (2) schottky contacts, (3) interconnects and vias. Although the electrical property requirements for these components are quite different, they all follow some general design guidelines [1][2]:

(1) Produce the correct electrical behavior.

(2) Good adherence to GaAs surface and dielectrics.

(3) Lithography process compatibility for selective etchability and/or liftoff replication.

(4) Reasonable matching of thermal expansion coefficients with GaAs and dielectrics.

(5) Good resistance to metallurgical reactions, oxidations, and corrosion.

(6) Reasonable ductility to allow wire bonding.

In addition, the ohmic and schottky contacts should exhibit the following attributes:

(1) Excellent contact stability during normal device operation.

(2) Stable, low ohmic contact resistance.

(3) Stable schottky barrier height.

(4) Reliable operation at higher ($\geq$125°C T_j) temperatures.

And finally the metals used as first-level, via-fill, and second-level interconnects should have three properties:

(1) Compatibility with the contact metallization.

(2) High conductivity and low via contact resistance.

(3) Good resistance to electromigration.

We will emphasize schottky contact and interconnect metallization in the following text and give a brief discussion on ohmic contact metallization for the sake of completeness.

1. Ohmic Contact:

The fundamental nature of an ohmic contact is its negligible resistance, which can be easily achieved in Si by doping the semiconductor near the contact region at least 10^{19} donors/cm^3 [3]. However, this technique cannot be applied to GaAs due to several practical difficulties. First of all, the doping level of the layer immediately beneath the metallization should be at least $5x10^{19}$ donors/cm^3 in order to achieve field emission in GaAs [4]. While in reality, the maximum obtainable donor concentrations for conventional epitaxial growth techniques such as LPE (liquid phase epitaxy), VPE (vapor phase epitaxy), MOCVD (metal-organic chemical vapor deposition), and MBE (molecular beam epitaxy) is generally limited to below $2x10^{19}$ donors/cm^3. This limit is caused by the lower donor binding energy, solid solubility of the impurity atoms in GaAs and also by the absence of an effective diffusion technology. It has been reported that donor level as high as $5x10^{19}$ donors/cm^3 can be obtained by using MBE technology [5]. Even though in cases of high concentration of impurity, the key problem is how to make these impurity atoms electrically active. Conventional annealing for activating an implant is generally limited to doping levels up to about $(2\text{-}5)x10^{18}$ donors/cm^3 [6]. Pulsed annealing by either laser or electron beams can result in higher doping levels, $(2\text{-}4)x10^{19}$ donors/cm^3, but complication of processing and the high defect density levels give rise to poor electron mobility, which severely restricted these techniques application in IC fabrication [7].

Conventional ohmic contacts technology fall into two categories: sintered and alloyed. In the sintered contact scheme, the metal-GaAs interaction occurs in solid phase, whereas in alloyed scheme this reaction takes place in liquid phase. The basic idea of both technologies is to deposit a metal containing dopant impurities onto GaAs. Then the contact is annealed and a heavily doped thin layer of GaAs is believed to form immediately beneath the metallization as a result of the metal-GaAs interaction. Sintered contacts based on Ge/Pd, Ge/Ni, Ge/Ta, Ge/Mo, Au-Ge, and Au-Ge/Ag/Au were tried out at various times, with often poor and diverse results on contact resistivity, surface

texture, and reliability [8]. Alloyed ohmic contacts have been extensively studied and are generally employed by present GaAs IC technology.

Alloyed ohmic contacts were developed to overcome the donor doping concentration limitations discussed earlier. Over the years, several alloyed metallization schemes have been investigated and notable metals and alloys were Sn, Au-Sn, Au-In, Au-In-Ge, and Au-Ge [3]. Among them, Au-Ge eutectic system has been proved to be the only one that works well as an ohmic contact to GaAs and so far, most contacts presently in use are based on this metallization scheme. In principle, this contact is formed in the following way: The Au-Ge is deposited onto GaAs and the complete structure is heated above the Au-Ge eutectic temperature (~ 356°C). The Au-Ge metallization melts and a portion of GaAs dissolves in the melt. Upon cooling, the GaAs regrows epitaxially from the melt at the melt/GaAs interface. This regrown GaAs layer incorporates a high concentration of Ge, making it heavily doped n-type, hence forming a 'tunneling' type contact. Usually enough excess metal remains on top of the regrown layer to facilitate metallic contact to other devices. To achieve low resistance in this contact, Ge must be exclusively on Ga lattice sites and provide active carriers in excess of $2x10^{19}$ donors/cm^3 [9]. One possible explanation about the contact formation mechanism is that Au acts as a selective gettering agent for Ga atom, as Ga diffuses out of the GaAs, the lattice site of Ga is replaced by Ge instead of by Au. The contact resistance can be reduced by using optimized quantity of Au:Ge in proper proportions [10]. Even though this technique sounds easy in theory, problems still exist in real fabrication. The contact tends to ball up and becomes non-uniform both laterally and in depth [11]. Improvements have been made by adding Ni [11], Pt [3], or In [12] to the Au-Ge metallization, either in the eutectic mixture or as a separate layer. In actual practice, The Au-Ge is almost always used in conjunction with a Ni overlay metal for improved adherence and uniform wetting during the alloying cycle. The specific contact resistivity is found to depend upon alloying time and temperature and also upon the heating and cooling rates. Since Arsenic is more volatile component in GaAs, a short alloy cycle time is usually necessary to prevent excessive As loss from the GaAs surface [13]. In general, the optimum alloy time and temperature must be determined experimentally. In addition, "surface cleaning" of the GaAs to reduce oxide before Au-Ge deposition is another critical consideration

because the lowest possible contact resistance is obtained in those regions where the crystalline order of the contacted GaAs surface has been well maintained or where a crystalline solid-phase formation has grown at the metal-semiconductor interface [14].

The biggest problems for alloyed ohmic contacts are reproducibility and stability. It is a relatively crude method and the degree of alloy penetration and contact uniformity are fairly uncontrollable. The non-uniform interface makes it difficult for contacting thin layers, and the lateral non-uniformities do not aid small contact geometries. These problems in addition with the reliability issues certainly restrict its future application since the current trend in IC industry is to minimize the device size to achieve high operation frequency.

2. Schottky Contact

The schottky barrier is one of the most important structures in GaAs ICs. When choosing a metal for schottky contact, the primary consideration is the capability of performing the required electrical function. Here, the key parameters of concern for a high quality schottky contact are the barrier height Φ_B and ideality factor n, which govern the rectifying behavior of the contact. However, as we discussed earlier, the barrier height produced by various metal on GaAs is fixed around 0.8V due to the Fermi level pining at metal-semiconductor interface, the choice of schottky metal thus relies more on the practical fabrication and reliability issues such as adherence, etchability, interdiffusion resistance, compatibility with interconnect system, and barrier stability consistent with the IC operating environment. The optimum metal should be able to produce the required barrier height and meanwhile balance all the other stability requirements.

Initially, individual metals were studied and applied to form single-layer schottky contact to GaAs. From the point of view of rectification, electrical resistivity, resistance to chemical attack, wire bonding and thermal conductivity, gold would be a very attractive and nearly ideal candidate due to its superior properties. However, problems emerge when devices have to operate at elevated temperatures. At 250°C, Au started to diffuse into GaAs while Ga diffuses to the surface through the Au layer to form Ga_2O_3 [15]. This interdiffusion becomes more severe when temperature increases and Au forms precipitates and dislocations in GaAs which quickly degrades the device

performance. In addition, the barrier height decreases almost 50% at about 400°C. The interface diffusion, barrier instability, plus the poor adherence of Au at high temperature led researchers towards other potential schottky barrier metals.

Another material that exhibits good resistance to chemical attack is Pt. But interdiffusion and compound formation begin to occur at a relatively low temperature range of 250-300°C [16]. Pd and Ni have the similar thermal stability as Pt. Refractory metals such as Mo and W exhibit inert interface behavior with GaAs at high temperature. While in this case the poor adhesion has been observed due to the thermal expansion coefficient mismatch between the metal and the GaAs [17]. The induced thermal stress always tends to peel off the metals from substrate. Three metals with good stable thermal properties on GaAs are Al, Ti, and Tantalum, although unfortunately all suffer the problem of surface oxidation. Al is most commonly used as a single layer schottky barrier in spite of the oxidation problem. However the interdiffusion of Al/GaAs exists at relatively low temperatures (125°C). Despite the low temperature interdiffusion, the contact is still considered inert since the reaction is not large-scale when compared to Au/GaAs. The outdiffusion of Ga constitutes a major failure mechanism in small signal FETs characterized by gate shorts or high leakages [14]. Furthermore, the lower resistance to electromigration of Al dramatically limits its application in GaAs ICs.

In summary, it is very difficult to find the optimum metal that satisfies all the metallization criteria for GaAs ICs. Consequently, this drives the development of mutilayer metallization scheme in which several metal layers are combined to create the ideal schottky contact.

Over the years, several mutilayer metallization schemes have been studied and among them, Ti/Pt/Au has been proved to be successful and has become the most commonly used schottky barrier metals for GaAs digital ICs and MMICs. It was constructed as a result of the following considerations. As the first layer, Ti adheres well and forms a thermally stable schottky barrier in contact to GaAs up to 350°C [18]. However, Ti has a relatively high resistivity and suffers the surface oxidation problem. Hence it is used in conjunction with a thick Au layer to increase the conductivity and resistance to electromigration. As we discussed earlier in single-layer metallization, Au/GaAs interface is very unstable at elevated temperature and a barrier layer must be

placed between Au and GaAs to avoid the interdiffusion to occur. Ti alone is not adequate to isolate Au from GaAs. In practice, this is accomplished by using a barrier metal such as Pt or Pd (Pt is most often used) above the Ti layer. The optimization of the thickness of individual components of this trilevel system must take into considerations of several factors. First of all, the thickness of the Pt layer is determined based on the criteria that it must prevent Au from reaching GaAs. In commercial GaAs ICs this thickness is usually in a range of 200-1000Å. The exact thickness of Pt also depends on the thickness of Ti layer since Ti also isolates Au and GaAs except its major task as the schottky barrier metal and adhesion layer. Another thing we should be aware of is that Pt can react with GaAs at relatively low temperature. Therefore, Ti layer should be thick enough to stop Pt reaching GaAs surface. The thickness of Ti layer is determined through reliability studies and it is found that a 400-800Å Ti layer can provide an adequate barrier to Pt.

Several other multiplayer metallization schemes have been investigated besides the most commonly used Ti/Pt/Au contact. A good summary of these contacts can be found in ref. [19].

Another important category of GaAs schottky contacts is the high-temperature schottky barriers, which has been developed with the utilization of self-aligned gate (SAG) technique. The motivation of using SAG is to reduce source and drain series resistances by implanting a heavily doped n^+ regions adjacent to the FET gate. Generally, a post-implantation anneal at 800-850°C is required to activate the n^+ dopants and repair the crystalline structure damage induced by implantation. In SAG technique, gate has been used as a mask during the implantation. Therefore, the schottky barrier metallization used for SAG technique must remain stable during anneal process, which means it should at least stand a temperature of 800°C.

Refractory metals such as Ta, Mo, and W were tried first but little success has been achieved due to the thermal stress associated adhesion problem. Yokoyama et al. have conducted the most extensive work in developing a GaAs FET SAG process [20]. Initially, TiW (10:90 wt.%) was thought to be the most promising metallization scheme. While the experiment results indicated that both Ga and As reacted with Ti at 750°C and a lowering in barrier height and increase in ideality factor were observed. This drove the

development of new metallization approaches using refractory silicides and nitrides [21]. Refractory metals such as Ta, Mo, and W form intermetallic compounds with Si with very stable metallic bonds. The thermal stability experiment results showed that the barrier heights and ideality factors were very stable in the case of Ta-Si_x, Mo-Si_x, and TiW- Si_x after anneal at 850°C for 1hrs [20]. It has also been reported that WN film is a very prospective candidate for the SAG technique because of its stability and the higher barrier height and lower resistivity compared to the silicide systems [22].

3. Interconnects and Vias

The interconnect system of GaAs ICs can be divided into three levels: first level interconnects, second level interconnects, and vias which unite the first and second metal systems at appropriate crossovers. Since they all have their own special electrical and reliability requirements, we will treat them separately here.

The essential criteria of being the first level metal is high electrical conductivity, good adhesion, and compatibility to ohmic and schottky barrier contacts. Au, Al, Ag, and Cu are the only candidates with adequate electrical conductivity that can be considered for interconnects application. Unfortunately, Ag is highly reactive and certainly cannot be used in GaAs; Cu is a fast diffusion atom in GaAs thus Cu and its alloys are not used for GaAs devices. Al, the favorite interconnect choice for Si has also been excluded because of the formation of high resistance intermetallic between Al and Au (required for ohmic contact on GaAs). Hence, Au becomes the best metal available for the first level interconnects. However, as we discussed previously in schottky barrier metallization, Au has poor adhesion and diffuses into GaAs at elevated temperatures, hence Ti and Pt layers are required to serve as the glue layer and diffusion barrier respectively. Besides providing the first level interconnects, Ti/Pt/Au also plays a role both as the MESFET gate metal contact and the overlay of ohmic contact. The purpose of adding an additional metal layer on ohmic contact is to increase the conductivity. In MMICs, the first level metal may also be used as the electrodes of capacitors and transmission line elements.

Vias are those contact windows opened through the interlayer dielectrics and later filled with metals to link the first and second level interconnect. The choice of via metal is based on high electrical conductivity, compatibility to the first level metal and

resistance to corrosion and electromigration. A Ti/Au layer is normally used for via metal in typical IC process.

The requirements for the second level metal are similar to that of the vias. In addition to high conductivity and great resistance to electromigration at high current densities, Au is also a ductile metal capable of wire bonding. Hence, Au is generally chosen as a second level metal with a Ti layer beneath it as the adhesion layer. This provides an ideal all Au metal system, free from intermetallics.

From above discussion, it is obvious that Ti/Pt/Au multilevel metal scheme plays an important role in GaAs metallization. It has been used as gate metal for MESFET, first level interconnects, and electrodes for MIM capacitors. Thus the microstructure, electrical properties of each metal component and the interaction between these metals have great impact on GaAs ICs' performance and reliability.

3.2 Metal Deposition Techniques: Evaporation vs. Sputtering

Unlike Si technology which has a long development history and has established a relatively mature process methodology, III-V compound semiconductor industries only emerged recently and are still striving to reach the Si-like high volume production and yield in order to meet the rising demands of the telecommunication market. Although many of the Si processing techniques can be adapted to GaAs fab, the unique material properties of GaAs still make the transfer of Si fabrication techinques impossible for GaAs. Some justification, modification is needed to make the current idea work in this new area.

Normally, GaAs IC metals are deposited by one of the following three methods: (1) Evaporation (2) Sputtering (3) Plating. The choice of the deposition technique is greatly based on the film characteristics, compatibility with the patterning method, yield, reliability, and sometimes also the cost. The primary consideration when choosing a deposition technique for GaAs application is to try to achieve the minimum sidewall coverage in the mask openings due to the utilization of liftoff as the replication method. It is well known that as a noble metal, Au is incapable of being dry etched like other metals. Instead, liftoff turns out to be a very effective way for Au patterning in GaAs. The liftoff

process sequence is illustrated in Fig. 3.1. In liftoff, a photoresist pattern protects portions of the wafer surface during deposition of a metal layer. The areas without photoresist allow metal adhesion to the wafer surface. When the photoresist pattern is stripped away using a solvent, the metal adhering to the resist is lifted off leaving behind the completed metallization layer [23]. It is very important to obtain vertical or overhanging resist edge profiles to ensure a discontinuity in the metal coverage between the resist and wafer surfaces. Furthermore, liftoff won't be successful if metal deposition has good sidewall coverage, which is preferred in some other cases. Hence, in GaAs, the deposition equipment is always designed in a way to allow the vertical impingement of metal atoms on wafer surface. In addition to minimum sidewall coverage, film uniformity is also another critical issue that needs to be considered. Excellent film uniformity is required for best device performance. Another important factor that cannot be neglected is the metal deposition temperature which should be controlled carefully to avoid the damage of photoresist caused by excessive heating.

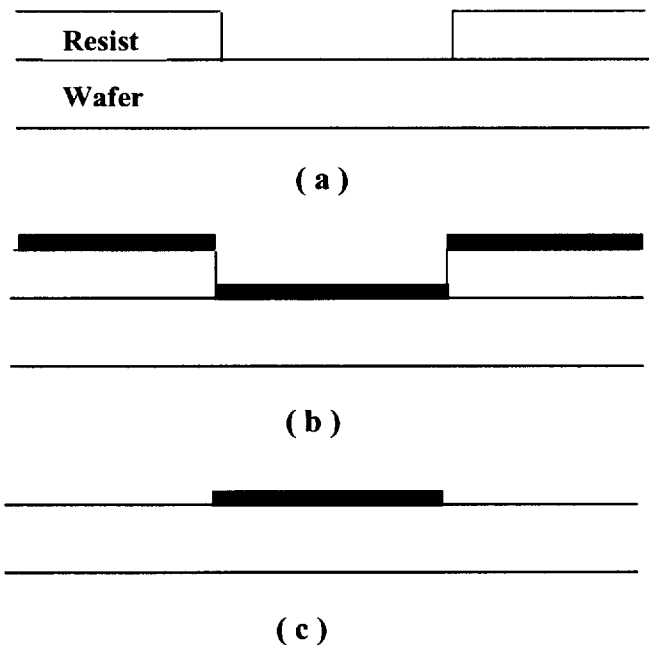

Figure 3.1 Liftoff process sequence. (a) Resist patterning. (b) Metal deposition. (c) Strip resist, unwanted metal is removed.

Evaporation:

Ohmic, schottky contacts and the first level interconnected are generally deposited by evaporation. During evaporation, thermal energy is imparted to atoms in liquid or solid source such that their temperature is raised to the point where they either efficiently evaporate or sublime and subsequently transfer themselves onto a substrate located a distance away from the source. Various techniques can be applied to heat the source and the most widely used method in current microelectronic industry is electron-beam heating. The disadvantages of the conventional resistively heated sources include contamination by crucibles, heaters, and support materials and the limitation of relatively low input power levels. Conversely, e-beam evaporation eliminates all these disadvantages and can deposit pure films at appreciable rates which is essential in microelectronic fabrication [24]. When designing an evaporator system for GaAs metallization, minimum sidewall coverage required by the liftoff process should always be considered first. This criterion can be met by choosing the appropriate deposition geometry inside the evaporator. The deposition geometry consists of several aspects: source and substrate geometry, source characteristics and the orientation and placement of substrate relative to the source. For better liftoff results, the wafers must be fixed to allow vertical impingement by evaporated atoms. In addition, this geometry also determines the film thickness uniformity, which is of equal importance when considering device performance. Ref. [24] gives detailed discussion of various geometries and their effects on film uniformity and conformal coverage. In III-V industry, metal evaporation is usually performed in a dome-shaped batch system which can provide minimum sidewall coverage. A mask is generally inserted in front the dome to overcome the film uniformity problem.

While suited to small volume lines, evaporation is not effective for high volume, high yielding production [25]. In the isotropic evaporation process, most mechanical components are also coated with significant quantities of metal. Many of these components are located closer to the target than wafers and receive much heavier deposition. Since batch is not equipped with load lock system, these heavy coatings are exposed to atmospheric gases on a routine basis while loading wafers. Higher stress is generated in these coatings due to oxidation and adsorption of gases and therefore more

particulate will be generated due to flaking off of the coatings. This significantly reduces the production yield. Besides the high level of contamination, extensive manual wafer handling is involved in batch process. High labor content, low automation and low throughput for larger wafer sizes cannot meet the ever-increasing demands of today's telecommunication market. These principle disadvantages of evaporation drive the development of sputtering as an alternative metallization technique for GaAs application.

Sputtering:

Sputtering is a well-established deposition technique with sophisticated and automated equipment available for metallization. It is presently the method of choice for most VLSI applications. Detailed coverage of sputtering processes and mechanisms can be found in Ref. [26]. There are various forms of sputtering systems, among them, DC sputtering is the simplest and its basic process is depicted in Fig. 3.2. Inside the chamber, the target or cathode, which is the metal to be deposited, is connected to the negative terminal of the DC power supply and the substrate or the anode, is grounded or biased. After evacuation the chamber, an inert gas, normally argon, is introduced and the gas pressures usually range from a few to a hundred millitorr. With typically several kilovolts applied to the cathode, the electrons leave the target and travel toward the anode until they strike and ionize one or more inert gas atoms in their path. The positive ions generated through electron-gas collision will be accelerated back to the target. They strike the target surface and some of them with sufficient energy will eject neutral target atoms which will travel in a random way and eventually deposit on the growing film. Besides DC sputtering, there are other variations of sputtering such as AC, magnetron, alloy, reactive sputtering and so on.

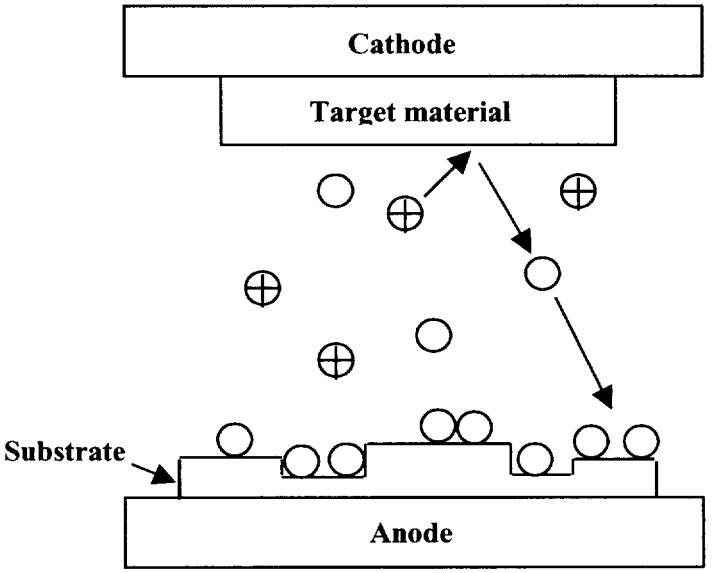

Figure 3.2 DC sputtering process

Unlike the batch evaporator, the newly developed sputtering system can be equipped with cassette-to-cassette cluster tools to improve the labor efficiency. A load-lock system is added to maintain higher vacuum level so that the deposition can take place in a relatively small, well-controlled chamber hence the contamination level has been significantly reduced [27]. In addition, less thermal stress is induced since the deposition is carried out at lower temperature. All these advantages of sputtering over evaporation make it a very attractive metallization alternative for high volume, high yield, low cost production. But sputtering suffers from a lack of directionality, which is required by the lift-off technique. To solve this problem and allow metal lift-off using sputtering, J. O'sullivan et al [28] did extensive modeling and experimental work. They investigated various sputtering parameters: wafer to target spacing, the sputtering pressure, the degree of ionization and the resist profile. Their results shown that by utilizing a two layer resist profile incorporating an overhang structure combined with a long working distance sputtering system, non-conformal, high base coverage can be achieved for successful metal lift-off. Some III-V companies has already replaced the evaporation with the highly automated sputtering system and proved that sputtering is very a capable metallization method for high volume, high yield and low cost production.

The properties of metal film produced by evaporation and sputtering are very different due to the different deposition mechanisms. This study investigates the properties of the newly developed sputtered Au/Pt/Ti film including microstructure, residual stress, surface morphology, and resistivity. Some of these properties are also compared with that of the evaporated film.

3.3 Metallization Reliability

The metallization system always plays a major role in the yield and reliability of integrated circuits. The factors that contribute to poor yield and reliability due to metallization problems were summarized by Sabnis in Ref. [29]. A detailed discussion of reliability and degradation issues of GaAs devices can be found in Ref. [30].

It has already been demonstrated in GaAs fab that large volume, high yield production can be achieved by using all-sputtering process. This was attributed to the dramatic reduction of the intralevel or interlevel metal shorts or opens. Evaporators and their associated tooling typically contributed high particle counts plus a high density of metal "splashes" that could introduce potential shorts or opens in circuits. By employing the sputtered Au/Pt/Ti metallization scheme, metallizaiton defect level was significantly reduced and higher yield was achieved [27]. It is very important for us to understand the dominant failure mechanism of any newly emerging technology, predict its lifetime, and eventually solve the problem to meet the ever-increasing lifetime expectation. One possible reliability problem that has been encountered so far in the sputtered Au/Pt/Ti films is hillock formation in MIM application, where Au/Pt/Ti film stack serves as the electrodes. Hillocks were observed after depositing a PECVD silicon nitride dielectric layer on the bottom Au/Pt/Ti metal stack. Consequently, the electrical properties of the capacitor with sputtered contacts were degraded compared to those with evaporated contacts. This was also the focus of this work.

Hillock formation, which consists of the numerous outgrowths of materials on the surface, is considered detrimental to the integrated circuits especially when it happens in metal contacts and conductors. The presence of these metal protrusions can cause cracking or penetration of the dielectrics, which give rise to interlevel conductor shorts or

breakdown of capacitors. The earlier discovery of hillock formation was during the cyclic heating and cooling of Al film used for Si metallization [31]. Since then, thermal induced hillocks were also reported in other metal films such as and gold [32], lead [31][33], tin [34], copper [35], silver [36], as well as $TiSi_2$. In addition to annealing, hillocks can also be induced by lack of adhesion and local delamination at the film-substrate interface, electromigration in metal conductors, and thin film growth at crystallographic direction of <100> as opposed to <111> [37].

Being one of the major yield and reliability-limiting factor, hillocks have been extensively studied over the years. It is generally believed that the annealing hillock formation is due to the relaxation of compressive stress, which could be either the extrinsic thermal stress caused by the thermal expansion coefficient mismatch between film and substrate, or the intrinsic stress generated during film growth. The formation of hillocks relieves the strain energy of the film because they are composed of material that has diffused from the bulk of the film, thereby reducing the compressive stress. However, a complete understanding of hillock nucleation, growth kinetics and dynamics has not been accomplished. This information is actually quite important because if we have a thorough understanding about this phenomenon, then certain methods could be found correspondingly to predict, or suppress hillock formation. Therefore, further experimental and theoretical work is needed to formulate a model to explain hillock formation.

Many models have been proposed to explain the hillock formation mechanism. A brief description of several selected researchers' works is provided here to give a general picture of this field. Fredric Ericson et. al. [38] studied the annealing hillock formation in evaporated Al films of various thicknesses by in-situ SEM heating and cross-sectional TEM observation. To verify the hillock formation dependency on stress, they performed a cantilever microbeam bending experiment, where a stress gradient was introduced in the film prior to heating, and found that the stress state and magnitude strongly influenced the hillock size and density. Their TEM investigation of hillocks provided support for the growth mechanism generally proposed in the literature: hillock growth occurs at elevated temperature and under compressive film stresses by migration of material along grain boundaries, presumably at triple pipes, up to the surface where it is deposited in a growing hillock. Initially, the hillocks are separated from the original

film surface by a grain boundary-like interface. During prolonged annealing, grain growth of adjacent grains will progress into the hillocks until they become integrated in the crystalline film. Chaudhari [39] has theoretically investigated hillock formation and suggested that it occurs by a diffusional creep mechanism. Creep either by lattice diffusion according to the model proposed by Nabarro [40] and Herring [41], or by the grain boundary diffusion process proposed by Coble [42] is the means of relaxing film stresses. It has also been pointed that in a stressed film complete relaxation cannot take place entirely via grain boundary diffusion, since that alone would leave the inside of the grains under stress [43] [44]. In addition to grain boundary and lattice diffusion, dislocation motion either being glide-controlled or climb-controlled can also contribute to the relaxation of stresses in thin films. H. L. Caswell [45] observed these motions through the formation of visible slip lines at the surface. Another important relaxation mechanism worth noting is the surface and interface diffusions. Unlike bulk materials, in multilayer thin film structures, there will be an interface between film and substrate on one side, and a free surface or an interface between the film and a second layer on the other. These two interfaces are particularly important when there is an equi-biaxial stress in the plane of the film, as would generally be the case for isotropic films under a thermal-expansion mismatch stress. As illustrated in Fig. 3.3, under this condition, all the grain boundaries are under an identical normal stress and Coble and Nabarro-Herring creep, as they are formulated for bulk materials, cannot occur. Instead, diffusion of atoms can only take place between the bulk of the film to the free surface, and to the substrate-film or film-film interface, either by diffusion through the lattice or along the grain boundaries. Atoms at the surface of the film will be redistributed either by surface diffusion or by evaporation and condensation. Since the redistribution acts in series with the process of diffusion to the surface, the slowest process will be rate-limiting. As a result, grain boundary grooves will develop under tensile stress, or hillocks will form under compressive stress.

As we can see from the above discussions, stress relaxation in thin films can proceed along different pathways. Hillock formation, being the result of compressive stress relaxation, must take place through certain relaxation mechanisms. It is unlikely that this process can be completed only by one relaxation mechanism. Several

mechanisms could be involved and operate simultaneously. The goal is to understand the dominant operating mechanism that relaxes the strain fastest in a certain regime. Frost and Ashby had a detailed discussion about the various relaxation mechanisms and their strain rate equations in ref. [46]. Only the most frequently observed relaxation mechanisms in thin films, including dislocation glide, dislocation climb, and diffusional creep [47], will be briefly discussed in the following text:

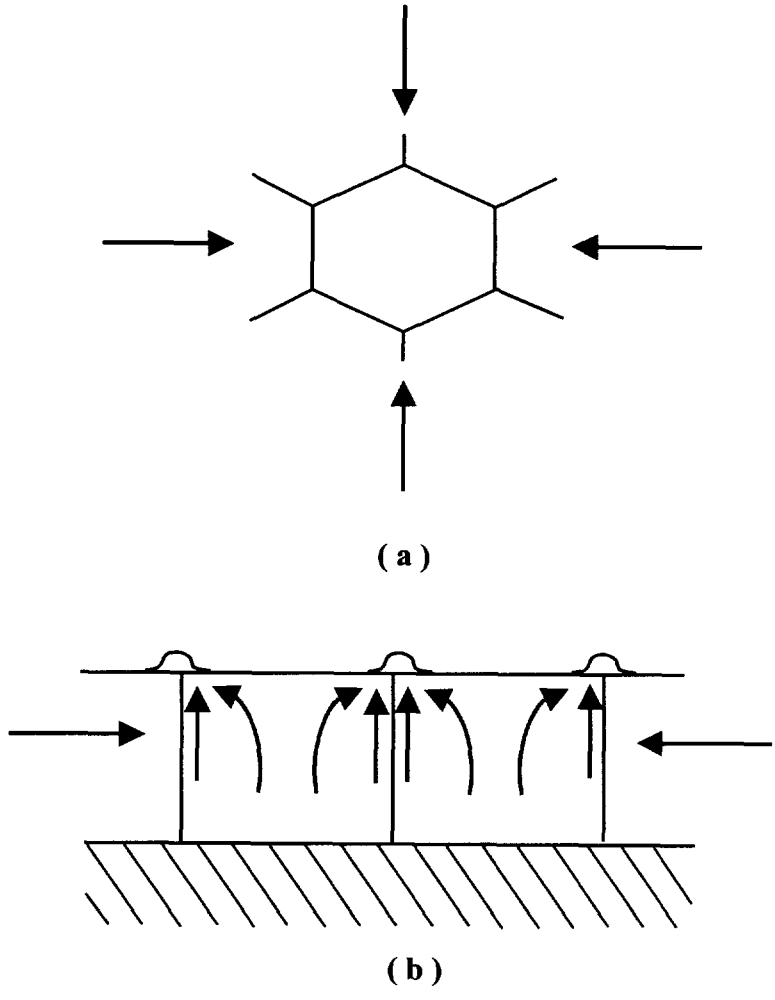

Figure 3.3 Schematic illustrations of the possible paths along which atoms can diffuse to relax stress in an equibiaxially stressed film. (a) Euqibiaxial compressive stress, (b) Atoms diffusion paths.

*1. **Dislocation Glide***: Dislocation motion is impeded by the presence of obstacles such as impurity atoms, precipitates, and other dislocations. In thin films, additional obstacles to dislocation motion such as the native oxide, the substrate and grain boundaries are present. An empirical law for the dislocation glide strain rate $\dot{\varepsilon}_1$ as a function of stress and temperature is

$$\dot{\varepsilon}_1 = \dot{\varepsilon}_0(\sigma/\sigma_0)\exp(-\Delta G/kT)$$

where σ_0 is the flow stress at absolute zero temperature, ΔG is the free energy required to overcome obstacles, $\dot{\varepsilon}_0$ is the pre-exponential factor, and kT has the usual meaning.

*2. **Dislocation Climb:*** When the temperature is raised sufficiently, rather than impeded by obstacles, dislocations can circumvent them by climbing vertically and then gliding. This sequence can be repeated at new obstacles. The resultant strain rate of the climb-controlled creep is given by

$$\text{at } T > 0.3T_m, \quad \dot{\varepsilon}_2 = A_2 \frac{\mu b}{kT} D_b \left(\frac{\sigma}{\mu}\right)^5,$$

$$\text{at } T > 0.6T_m, \quad \dot{\varepsilon}_3 = A_3 \frac{\mu b}{kT} D_L \left(\frac{\sigma}{\mu}\right)^7,$$

here, μ is the shear modulus, D_b and D_L are the thermally activatd grain-boundary and lattice diffusion coefficients respectively, and A_2 and A_3 are constants.

*3. **Diffusional Creep:*** Viscous creep in polycrystalline films can occur by diffusion of atoms within grains (Nabarro-Herring creep) or by atomic transport along grain boundaries (Coble creep). The respective strain rates are given by

$$\dot{\varepsilon}_4 = A_4 \frac{\mu}{kT} \frac{\Omega}{ld} D_L \left(\frac{\sigma}{\mu}\right),$$

$$\dot{\varepsilon}_5 = A_5 \frac{\mu}{kT} \frac{\Omega \delta D_b}{ld^2} \left(\frac{\sigma}{\mu} \right),$$

where $\dot{\varepsilon}_4$ is the strain relaxation rate by lattice diffusion, $\dot{\varepsilon}_5$ is the strain rate by grain boundary diffusion, A_4 and A_5 are constants, Ω is the atomic volume and δ is the grain boundary width.

A very useful way to predict the dominant relaxation mechanism in certain regime is to construct a deformation mechanism maps, which was first developed for bulk materials [46], and then extended to thin films by Murakami et al. [48]. Fig. 3.4

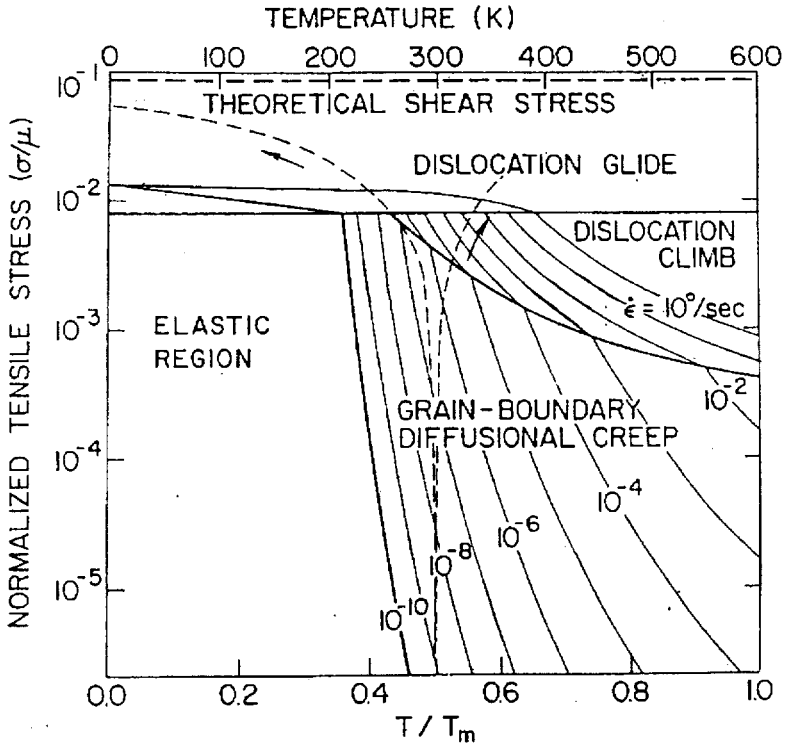

Figure 3.4 A calculated deformation mechanism map for a Pb thin film with h = 0.5μm and g = 0.25μm.

(Reprinted from Thin Solid Films, **55**, M. Murakami, "Thermal strain in Lead thin films II. Strain relaxation mechanisms," pp.101-111, 1978, with permission from Elsevier.)

gives a calculated deformation mechanism map for a 0.5-μm thick Pb thin film. In constructing the deformation mechanism map, the process exhibiting the largest strain relaxation rate is calculated at each point in the field of the normalized stress-temperature space. The field boundaries are determined by equating pairs of rate equations for the dominant mechanisms and solving for the resulting stress dependence on temperature.

So far, all the discussions are concerned with the manner in which the annealing hillocks form. The following text will deal with some other matters such as hillock size, density, distribution and their dependency on stress, time and temperature. Chang and Vook [49] investigated the hillock growth in Al-Cu films during isothermal annealing after their initial nucleation and formation, and found that the initial density of hillocks decreases and their average size increases in a manner that resembles the Ostwald ripening process [50] [51]. They assume that the decrease in hillock density is thermally activated with an activation energy E. It is also assumed that a similar thermal activation governs the increase in hillock size at a given temperature. The basic equations they proposed are as follows:

$$N = N_0 \cdot exp(-m_1 t)$$

$$D = D_0 \cdot exp(m_2 t)$$

where N is the hillock density, D the hillock diameter, t the time, and m the temperature-dependent rate. The rate m is assumed to be given by:

$$m = m_0 \cdot exp(-E / kT)$$

Their experiment data obtained from SEM insitu observations of hillock growth fitted well into these equations and the calculated activation energies were proved to be very helpful in identifying the different diffusion mechanism at various temperatures. The annealing hillocks in sputtered Au thin film were observed by W. B. Pennebaker [32]. He created a model that is able to relate the sign and magnitude of the stress with hillock size and density based on the following assumptions: the hillocks are formed by recrystallization driven by thermal stress. During annealing, the stress is initially compressive and slowly decays to zero as the hillocks grow. The hillock formation is the primary stress relief mechanism. His model is described by the following equation:

$$D_M = (\sigma_0 S / \beta N)^{1/4}$$

Where D_M is hillock lateral dimension, σ_0 is the initial compressive stress inside the film, S is film thickness, N is number of hillocks per unit area, β is coefficient defined by the film elasticity parameters.

In general, hillocks develop under compression in films that adhere well to their substrates. In the absence of such good adhesion, relatively frequently film under compression will locally lift off from their substrate or underlying film. These local delaminations have a similar appearance to that of the annealing hillocks although the formation mechanism is completely different. Adhesion is a very important subject in thin film structure and it is certainly the first attribute a film must possess before any of its other properties can be manifested or exploited. Adhesion between film and substrate can be affected by several factors including film stress, substrate morphology, bonding forces, chemical interactions and so on. In this work, the hillocks were induced during the PECVD Si_3N_4 deposition process, rather than during the deposition of Au/Pt/Ti films, or the annealing of the as-sputtered films. Hence, besides stress relaxation of metal films at elevated temperature, adhesion is another critical factor that needs to be considered while discussing the hillock formation mechanism in this particular case.

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4 Experiment Procedures

4.1 Deposition of Thin Films

Au/Pt/Ti Deposition:

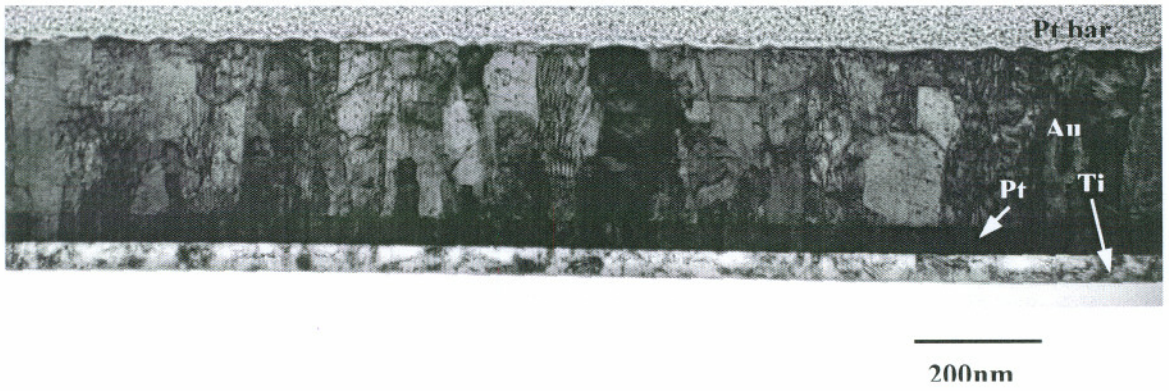

Figure 4.1 TEM cross section image of Au/Pt/Ti thin film stack used in this thesis.

The structure of Au/Pt/Ti thin film stack examined in this thesis is shown in Fig. 4.1. In this study, 500Å of Ti and 500Å of Pt were used while the Au film thicknesses varied for the purpose of examining the effects of thickness on film properties. Au, Pt, Ti thin films are all deposited by using single wafer PVD cluster tools designed specifically for lift-off applications. The integration of pre-metallization cleaning and sputter deposition is realized by employing four connected process modules, one for plasma etch cleaning and the remaining three for Ti, Pt, Au deposition respectively. Wafers were cleaned in-situ first by sputter etch, then automatically transferred under vacuum to next

sputter deposition module. Cold electrostatic chucks (ESC) were applied inside each deposition chamber to keep the temperature below 80°C. The deposition rates for these metals are: R_{Ti} = 10.42 Å /sec, R_{Pt} = 14.71 Å /sec, R_{Au} = 30.30 Å /sec.

Au/Pt/Ti films are deposited onto GaAs substrates for making real devices, blanket Au/Pt/Ti films were sputtered onto Si wafers in this study considering that the GaAs wafers are relatively expensive and multiple wafers were needed for the planed experiments. A thin layer of SiO_2 was deposited on top of the Si substrate to prevent the interdiffusion and reaction between metal films and the substrate. Since the thermal expansion coefficients of GaAs and Si are pretty close, using Si wafers instead has negligible effects on the stress measurement. The interaction between metal films and the substrate is also not a concern because of the presence of the SiO_2 layer.

PECVD Si_3N_4 Deposition:

One important application of Au/Pt/Ti metallization is acting as the contacts for Metal-Insulator-Metal (MIM) capacitors. A typical MIM capacitor structure is shown in Fig. 4.2. In this study, Plasma Enhanced Chemical Vapor Deposition (PECVD) process was used to deposit Si_3N_4 as the MIM capacitor's dielectric layer. The deposition took place in four identical modules configured with the same temperature, plasma, and reactive gas supply. Within each module, the platform was preheated to 350°C and wafer was held on it for 10sec before deposition in order to stabilize temperature. When deposition was completed, wafer was transferred to the next module and the same deposition procedure was repeated. This multi-module process features higher throughput and excellent film quality. Finally, wafer was cooled down to room temperature in air for 30sec.

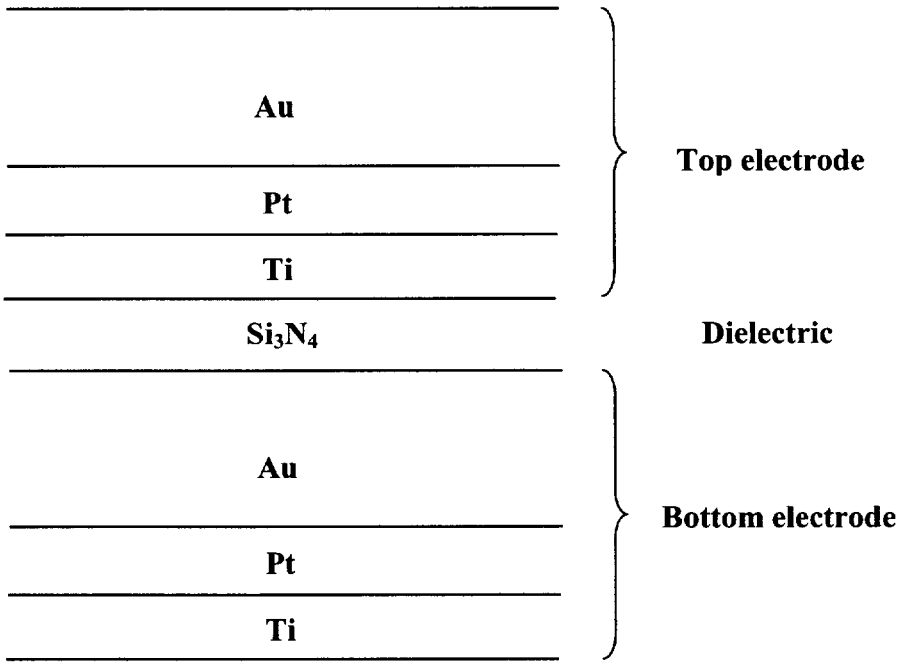

Figure 4.2 MIM capacitor structure

4.2 Transmission Electron Microscopy

As a parallel electron beam travels through and interacts with a TEM specimen, they are either scattered by a variety of processes or they may remain unaffected. The result is that a nonuniform distribution of electrons, which contains the structural and chemical information about the specimen, emerges from the exit surface of the specimen. Transmission Electron Microscope (TEM) constructed with sets of electromagnetic lenses, restricting apertures, and electron detectors utilizes the information carried by the forward-scattered electrons and can display this nonuniform distribution in the forms of specimen images or diffraction patterns.

4.2.1 TEM Specimen Preparation

TEM analysis requires that the region of interest must be electron transparent and represent the materials' real structure. This means that certain tools and techniques must be used to remove most of the bulk material within a small area in the center, leaving only an extremely thin section for TEM observation. There are many ways to produce a TEM specimen, the method of choice will depend on the information needed, material, availability of equipment, and skills. In general, we can divide the specimen in two groups: planar and cross-section. For semiconductor devices which have multiple layers and interfaces, cross-sectional specimens perpendicular to the substrate allows precise examination of device structure and interface morphologies. In this research, Focused Ion Beam (FIB) produced cross-sectional TEM specimens were used to study the interface structure of the metal layers and microstructural features within each layer. In addition, a planar specimen was produced by Gatan precision ion polishing system (PIPS) to examine the Au film quality and grain distribution.

Cross-sectional TEM Preparation:

First, the bulk sample was coated with 500Å Au-Pd thin film in Hummer II sputter coater to increase specimen conductivity and also prevent damage to specimen surface during manual polishing and FIB imaging. Then the site to be analyzed was identified and cut into a small piece with a diamond saw. In general, a 1mm x 2mm section was preferred because it can perfectly fit into our 3mm TEM specimen holder. Since GaAs is very brittle, the cutting speed was adjusted to the medium level to prevent the specimen from breaking.

The next step is to use the Gatan disc grinder to pre-thin the cut section to a thickness of 100μm or less. Efforts were made to make the sample as thin as possible since it can tremendously reduce the FIB milling time. The sample was attached on a metal stub with low melting point Crystalbond wax. The maximum temperature of the specimen mounting hot plate used to melt the wax is roughly 100°C, therefore, specimen was slightly heated at this step. The metal stub was inserted into the disc grinder and

manually ground on 3M imperial lapping film discs until a reasonable thin specimen was achieved.

After manual polishing, the specimen was cleaned in acetone and attached to a half molybdenum washer as shown in Fig. 4.3. The choice of glue depended on the temperature at which the TEM analysis was carried out. For ordinary room temperature analytical TEM, super glue cured by pressure was used. But this kind of glue is not suitable for in-situ heating TEM analysis because it cannot stands temperature higher than 200°C. Instead, heat curing G-1 epoxy endurable up to 400°C was used for high temperature in-situ analysis.

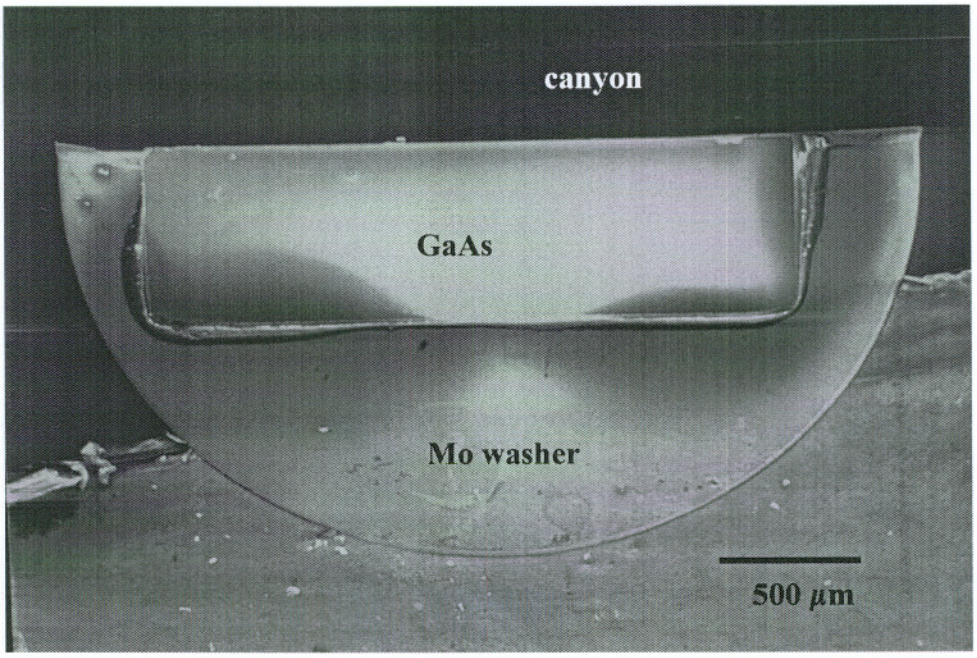

Figure 4.3 SEM image of a TEM specimen attached to a half washer

Finally, FEI 610 FIB workstation was used to create an electron transparent thin foil at the desired location on the specimen. The metallized surface of the sample was positioned perpendicular to the Ga Beam direction. To avoid the beam damage to the

interested area, a 20μm x 1μm x 1μm platinum-bar was deposited in-situ prior FIB milling by Ion Beam Enhanced Chemical Vapor Deposition at the location of the final thin foil. Then 15-25 μm wide and 4-5 μm deep canyons were cut at both sides of the platinum-bar, leaving an electron transparent thin section in the middle ready for TEM analysis. Fig. 4.4 shows a SEM picture of the finished FIB produced TEM cross-sectional specimen.

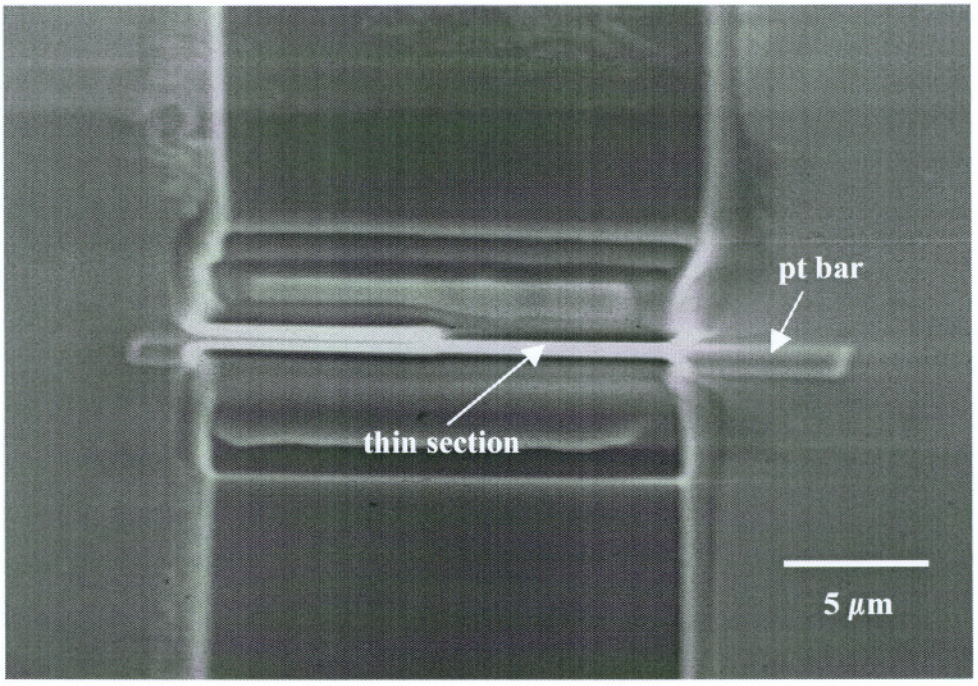

Figure 4.4 SEM image of a finished FIB produced TEM cross-sectional specimen

Planar TEM Preparation:

A 1mm x 2mm small section was cut from a wafer with blanket metallization using diamond saw. The sample was attached to a Mo washer with super glue by positioning the metalization surface towards the washer so that a portion of the top Au

layer can be exposed from the 1mm center hole on the washer. The specimen was then polished at the backside to a thickness of 10μm using Gatan disc grinder. The final ion milling was carried out in Gatan PIPS at a milling angle of 5° and beam energy of 5keV.

4.2.2 TEM Microstructure Observation

JEOL 2000FX TEM/STEM operating at 200keV accelerating voltage was employed throughout this study. Bright Field (BF) images were taken to examine the microstructural features of the metallizaiton including grain size, dislocation density and interface morphology.

This microscope was equipped with a Quantum EDS X-ray detector capable of detecting nitrogen and elements with higher atomic numbers than nitrogen. EDS X-ray qualitative analysis performed in the STEM mode was carried out in each metal layer and their interfaces to investigate the interdiffusion between these metal layers.

Microdiffractions were performed in several consecutive Au grains to identify the grain orientations. Diffraction patterns simulated by Desktop Microscopist software were compared with the experimental data to determine the grain orientation.

In-situ TEM experiments were carried out at Lawrence Berkeley National Laboratory.

4.3 Atomic Force Microscope Characterization

In this work, the Au/Pt/Ti metallization being studied has a very smooth surface with a nanoscale roughness. The hillocks, which are about 7nm high and are the primary interest of this research, are relatively "tiny" compared to micron-scaled Al hillocks. Therefore, most of the traditional Scanning Electron Microscope (SEM) imaging with a resolution of 3-4nm is not capable to resolve such fine surface topography. The recently developed Atomic Force Microscope (AFM), which can measure sub-angstrom surface roughness on ultrasmooth surfaces, turned out to be a perfect choice for this study.

Tapping mode AFM was performed on a Veeco Dimension 3100 to examine the surface morphology of these metal films. The probes used for this study was Nanosensors

NCH-16 silicon cantilever. In tapping mode AFM, a tip attached to an oscillating cantilever is scanned across the sample surface under the drive of a piezoelectric scanner. The tip lightly "taps" on the sample surface and contacts the surface at the bottom of its swing. The vertical positions of the scanner at each point in order to maintain the set point oscillation amplitude are stored to form the topographic image of the sample surface.

A variety of analysis functions are available on this machine. Generally, we used section and roughness analysis to study the film roughness and hillock geometry.

Since the nanoscale hillocks are not observable by optical microscope or SEM, locating and marking a hillock, which is the first step of making a TEM hillock cross-section, becomes quite complicated. Fortunately, AFM has adequate resolution to reveal these tiny hillocks and makes the locating much easier. The detailed hillock locating procedure is described below: First, a hydrocarbon cross marker was randomly deposited in SEM by performing an EDX line scan. Several spot markers were also made by performing EDX spot scan for the purpose of easy identification. Next, the specimen was scanned by AFM and the image of hillocks with the initial reference markers was generated. Referring to this image, a certain hillock was chosen and another line marker was precisely deposited on the selected hillock in SEM. Finally, specimen was scanned in AFM again to verify the placement of markers. An AFM image of a located hillock is shown in Fig. 4.5.

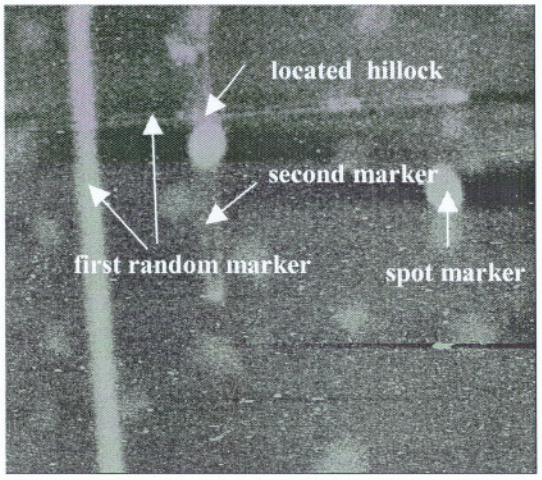

Figure 4.5 AFM image showing the SEM markers and the located hillock

4.4 Thin Film Stress Measurement

4.4.1 Stoney Formula

The formulas which have been used in virtually all experimental determinations of film stress are variants of an equation first given by Stoney in 1909 [1], which is given by equation 4.1 [2]:

$$\sigma = \frac{Eh^2}{(1-\nu)6Rt} \qquad (4.1)$$

where

$\frac{E}{(1-\nu)}$ is the biaxial elastic modulus of the substrate

h is the substrate thickness

t is the film thickness

R is the substrate radius of curvature

σ is the average film stress

The detailed derivation of stoney formula can be found in Ref. [3]. Fig. 4.6 gives a schematic drawing of an originally flat substrate being deformed to radius R by the deposition of a thin film. The film is under tension in Fig. 4.6(b) and compression in Fig. 4.6(c). In most cases, substrate wafers often have a nonconstant curvature and are sometimes deformed into a potato-chip shape. Nevertheless, the average stress in subsequently deposited films usually can be determined with good precision by subtracting curvature data of the initial bare substrate from that obtained after coating it, both scanned over identical paths. Therefore, the effective radius can be determined by the following equation:

$$\frac{1}{R} = \frac{1}{R_2} - \frac{1}{R_1} \qquad (4.2)$$

$$R = \frac{1}{\frac{1}{R_2} - \frac{1}{R_1}} = \frac{(R_1 R_2)}{R_1 - R_2} \qquad (4.3)$$

where

R_1 is the radius of the initial bare substrate

R_2 is the radius of the wafer after the film deposition

R is the effective radius used in stony formula to calculate film stress

In case of multi-layer films, the curvatures are additive and the total curvature is just the sum of the individual film contributions. Stoney's formula then yields:

$$\frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_n} = \frac{6(1-\nu)(\sigma_1 t_1 + \sigma_2 t_2 + \cdots + \sigma_n t_n)}{Eh^2} \qquad (4.4)$$

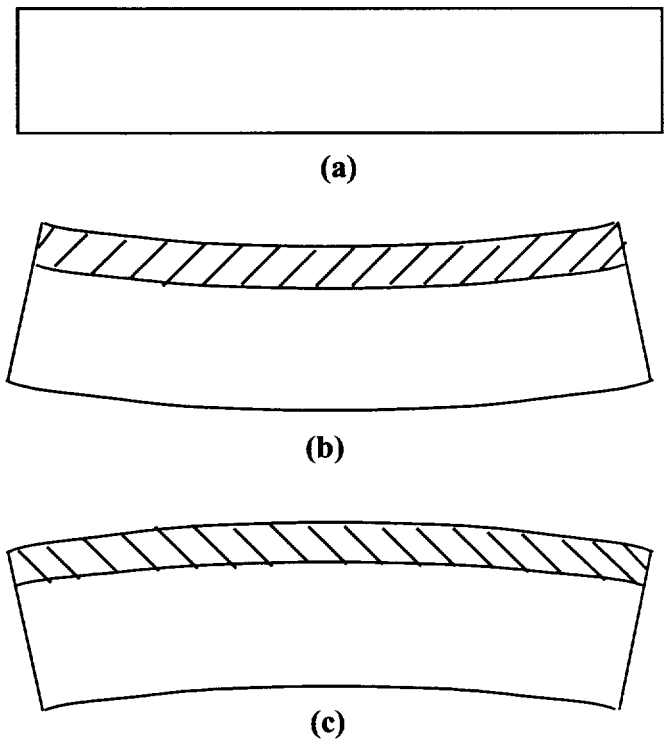

Figure 4.6 (a) flat substrate, and substrate deformed by films under (b) tensile stress and (c) compressive stress

4.4.2 Stress Measurement

The residual stress measurement and in-situ annealing stress evolution of the sputtered metal films were carried out in Tencor FLX-2320, which measures the changes in the radius of curvature of a substrate caused by deposition of a thin film and automatically converts to stress. To calculate the film stress, the substrate radius must be measured before and after film deposition. Since wafers often have a nonconstant curvature, the average radius is obtained by measuring R as a function of position X and performing a linear regression. The materials constants used to calculate film stress are listed in Table 4.1:

Table 4.1 Materials constants used to calculate film stress

Wafer	Biaxial elastic modulus ($x10^{11}$Pa)	Substrate thickness (μm)	Wafer diameter (150mm)
GaAs (100)	1.239	675	150
Si (100)	1.805	675	150

A hot plate is equipped with Tencor FLX-2320 to measure the film stress on a wafer as a function of temperature after film deposition. The thermal stress induced in sputtered metal films due to the thermal expansion mismatch and the stress relaxation at elevated temperatures were evaluated by annealing the as-sputtered wafers in air from room temperature to 450°C at a ramping rate of 10°C/min. The hot plate temperature was then cooled down to room temperature at –10°C/min.

4.5 Electrical Performance Measurement

As discussed in previous sections, the major application of Au/Pt/Ti metal stack is to serve as the first level interconnects, MESFET gates, and electrodes for MIM capacitors. For all these application, low resistivity and smooth surface topography are preferred in order to achieve best conductivity and to improve yield and reliability. Hence, the electrical property measurements were focused on the resistivity measurement

of as-sputtered metal films and the breakdown voltage and leakage current measurement of MIM capacitors with various bottom electrode roughness.

4.5.1 Resistivity Measurement

The resistivity measurement of the sputtered Au/Pt/Ti thin film stack was carried out on Signatone four point probing system, using as-deposited 6 inch wafers as the specimens. This 4-point probe consists of four equally spaced tips with finite radius. A high impedance current source is used to supply current through the outer two probes; a voltmeter measures the voltage across the inner two probes to determine the sample resistivity. Since very little contact and spreading resistance is associated with the voltage probes, fairly accurate sheet resistance can be obtained and then used to calculate the resistivity. For a semi-infinite thin sheet wafer, the sheet resistance and resistivity can be represented by Equation 4.5 and Equation 4.6 respectively:

$$R_s = \frac{\pi}{\ln 2}\left(\frac{V}{I}\right) \qquad (4.5)$$

where

V is the voltage across the inner two probes

I is the supply current flowing in the outer two probes

Consequently,

$$\rho = R_s t = \frac{\pi t}{\ln 2}\left(\frac{V}{I}\right) \qquad (4.6)$$

where t is the film thickness

4.5.2 Leakage Current and Breakdown Voltage Measurement

A SEM image of the MIM capacitor structure used for breakdown voltage and leakage current testing is shown in Fig. 4.7. HP 4145A semiconductor parameter analyzer connected with a Micromanipulator 8860 wafer probe station was used to perform these measurements.

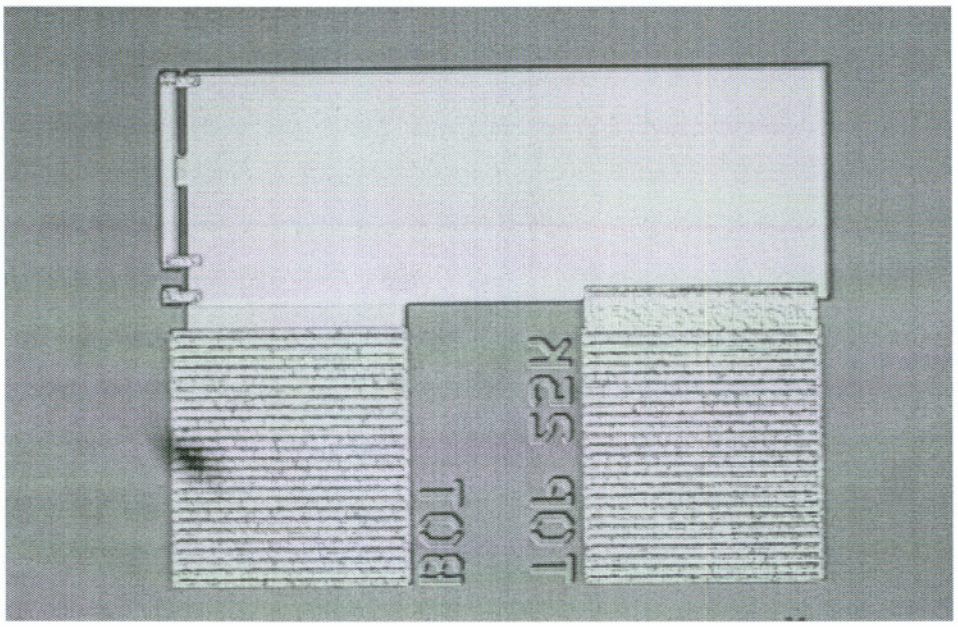

Figure 4.7 SEM image of the MIM capacitor structure used for breakdown voltage and leakage current measurement

During the experiment, the capacitor's top electrode was ramped from 0V to 100V, while the bottom electrode was grounded. The leakage currents at each data point were stored and then plotted vs. the applied voltage as shown in Fig. 4.8. For this application, we defined the breakdown voltage as the voltage corresponding to a 20 milliamp leakage current. One thing should be noted is that since the maximum compliance current allowed on HP 4145A in this voltage range is 20 milliampere, the current will remain constant after reaching this threshold, even though the actual leakage current flowing in the capacitor could be higher. Nevertheless, this does not affect our measurement because a 20 milliamp leakage current is big enough to consider that the capacitor is in breakdown. For better sampling, measurements were performed on each wafer at three specific dies and the averages were taken to be treated as the final leakage current and breakdown voltage.

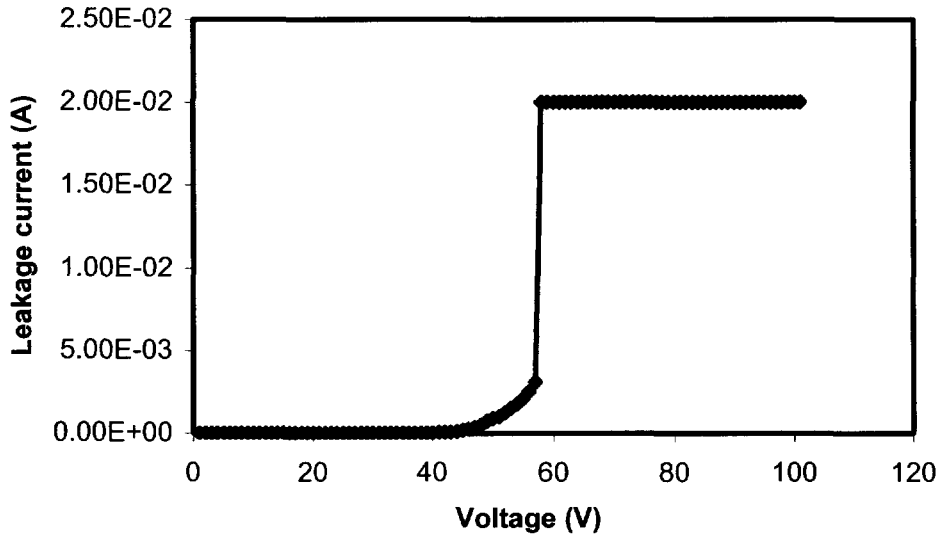

Figure 4.8 Typical leakage current vs. voltage graph in reliability test

In reliability analysis, the samples were first heat stressed at 280°C for 72 hrs and 168 hrs respectively, then the same routines were carried out to perform electrical measurements and data analysis as described previously.

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5 Properties of the As-sputtered Au/Pt/Ti Film: Microstructure, Residual Stress, and Resistivity

This chapter discusses several important material properties of the as-sputtered Au/Pt/Ti film including microstructure, intrinsic stress, resistivity and their correlations. The reasons these properties were chosen to be studied are two fold: 1. Generally, these properties significantly affect thin metallic film's application and performance as metallization for microelectronics. 2. These properties have a strong dependence on deposition method and parameters. With sputtering replacing evaporation and becoming a promising method to deposit Au/Pt/Ti film stack, it is necessary to reveal the property modifications introduced by sputtering and the correspondent effects on film electrical performance.

5.1 Residual stress of the sputtered Au, Pt and Ti film

The residual stress of a 0.05μm sputtered Ti film was found to be compressive with magnitude of 18Mpa. Only the stress at this thickness was examined because the thickness of Ti film does not vary much when used as glue layer. For similar reason, the residual stress of sputtered Pt film was measured only at thickness of 0.05μm. The measurement showed that a fairly large compressive stress of 840 MPa exists in Pt film.

The residual stress of sputtered Au film was tested at thicknesses ranging from 0.02μm to 0.6μm. These specimens were sputtered using exactly the same process parameters. The resultant stress is plotted as a function of film thickness in Fig. 5.1. This curve exhibits two distinct regions with increasing of film thickness: 1. Tensile stress appears initially. Then it quickly descends to a non-stress state at about 0.2μm. 2. Beyond

0.2μm, stress becomes compressive and it builds up very slowly with further thickness increase.

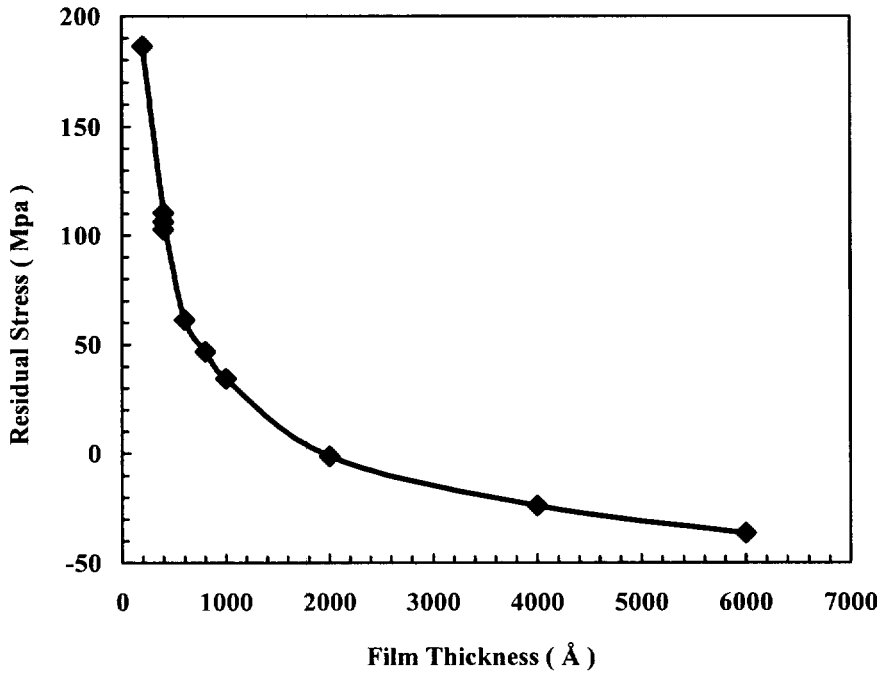

Figure 5.1 Effect of film thickness on residual stress in as-sputtered Au film.

The thickness-dependent stress has been observed in other sputtered metallic films. Hoffman and Thornton did the most intensive investigation about the effects of process parameters on internal stress of sputtered films [1][2][3][4]. They studied a variety of metallic elements including Titanium, nickel, molybdenum, tantalum, and Chromium. Specifically, the thickness dependence of stress they have discovered dramatically depends on the working pressure [5][6][7][8]. At low vacuum pressure, the internal stress is compressive, whereas at high pressure, tensile stress develops. Despite the stress state, the internal stress always increases with film thickness at a constant pressure, which is in agreement with our experimental results. However, the transition of stress state from tensile to compressive was not observed. They call the increased stress with thickness as incremental stress, but did not explain why stress varies with thickness.

The thickness dependence of stress observed in sputtered tungsten film [9] is very similar to Fig. 5.1. The film first experiences tension, then the stress quickly changes to high compression and remains constant for thicknesses up to 0.2 μm. The transition of stress was explained by a phase transformation from β–W to α–W in the substrate adjacent part of the film. In sputtered carbon films, the stress was found to be compressive and it decreases as the film thickness increases, which was attributed to the compressive stress relaxation by voids formation in the thicker films [10]. The study of sputtered molybdenum and tantalum films showed that the compressive stress relaxation with the increasing of thickness is due to the film microstructure evolution including grain growth and phase transformation [11]. In summary, the thickness dependence of stress varies sensitively with the metallic elements and deposition parameters, no generalization can be made to anticipate this effect. But it is believed that there is a direct link between the film morphology evolution and the stress development. The film's intrinsic stress is the cumulative result of chemical and microstructural defects incorporated during the film condensation process. In this study, the microstructural effect is suspected to be the cause of stress dependence on thickness. The correlation between film microstructure and intrinsic stress will be explained in details in the next section.

5.2 The Correlation between the microstructure and residual stress of the sputtered Au film

Physical vapor deposited film exhibits a spectrum of microstructures depending on the process conditions, with the fundamental factors being the kinetic and thermal energy supplied to the growing film. Generally, thin film structure can be categorized into four zones. Three different structure zones (Z1, Z2, and Z3) were initially identified in an evaporative deposition study [12], and a forth "transitional" zone (ZT) between Z1 and Z2 was identified in sputter deposition [13]. The formation of the structure zones dramatically depends on bombarding energy and the homologous temperature, which is the ratio of the substrate temperature to the melting point of the film and is denoted by T_s/T_m. The homologous temperature is one important factor that determines the adatom mobility hence it controls the film microstructure evolution. Z1 occurs at T_s/T_m so low (<

0.2) that adatom surface diffusion is negligible. The films are usually low density, voided, and consist of columns typically tens of nanometer in diameter separated by voids a few nanometers across. The columns have poor crystallinity (many defects) or are amorphous. Films with this zone structure are generally in a state of tensile stress. Z2 occurs at $T_s/T_m > 0.3$ or so, high enough that surface diffusion is becoming significant. It consists of columns having tight grain boundaries between them and having a characteristic diameter which increases with T_s/T_m. Crystalline columns have a lower density of defects than in Z1. Z3 occurs at $T_s/T_m > 0.5$ or so, high enough so that considerable bulk annealing of the film is taking place during deposition. Z3 is characterized by more isotropic or equiaxed crystallite shapes. ZT contains defected columns similar to those of Z1, but the voids are absent. ZT is usually expected for energy-enhanced processes. The residual stress with ZT varies depending on the bombarding energy.

It is noteworthy that the transition of these growth modes is not always abrupt with temperatures. Sometimes, the film growth mode changes from one zone to another during growth producing a deposit with a microstructure that changes through the film thickness.

In this study, a TEM cross-section technique was employed to examine the microstructrual variation of the sputtered Au film at a range of thicknesses. Fig. 5.2 shows the microstructure of a 0.05μm Au film and a 0.4μm Au film respectively. Apparently, both films are continuous polycrystalline film with columnar grain structure that is very typical for sputtered film. With the deposition temperature kept below 80°C, Z1 or ZT structure is expected in the sputtered Au film. The TEM images clearly show that the porous, voids rich Z1 structure was not observed, instead, a dense, ZT structure was obtained in both films due to the energetic particle bombardment. The distinctions between these two films are also obvious: 1. The grain size of the 0.05μm film is about 0.03μm, much smaller than that of 0.4μm film which is about 0.24μm. 2. The defect density, particularly interstitial clusters and dislocations, are much higher in the 0.4μm film than that of the 0.05μm film. The microstructural variations with thickness are considered to mainly determine the internal stress evolution as the film grows.

100 nm

(a)

400 nm

(b)

50 nm

(c)

Figure 5.2 TEM cross-sections show the microstructural variation of sputtered Au film at different thicknesses. (a) low magnification image of a 0.05μm film. (b) low magnification image of a 0.4 μm film. (c) high magnification image of a 0.05μm film showing grains with low defects density.

It needs to be pointed out that there was no intentional heating during film deposition, thermal stress was generated in these films due to the heat introduced by the particle bombardment. However, it was neglected here since the thermal stress components exist in each specimen therefore it does not contribute to the transition of stress from tensile to compressive. Atomic scale vacancies which are invisible in the TEM image probably exist, and could be one of the sources that contribute to the tensile stress generation. However, this should only be a minor factor because the vacancies tend to be annihilated at internal or external surfaces or recombine with interstitials due to the energetic particle bombardment. It is suggested that the grain boundary relaxation is the dominant mechanism during the sputtering process that causes the tensile stress generation in the thinner film. The grain boundary relaxation model was initially proposed by Hoffman [14] and is the most generally used model to explain the tensile stress creation. At the initial stage of film growth, only isolated islands with certain crystallographic orientations form, which is referred to as Volmer-Weber growth mode. Since the film at this stage is discontinuous, it certainly cannot sustain any internal stress. As the film growth progresses, these islands eventually coalescence with each other so that the interatomic attractive forces can act across the gaps between these continuous islands, or grains, and will cause an elastic deformation (relaxation) of the grain walls. The grain boundary deformation is balanced by the intragrain tensile forces imposed by the constraint exerted by the adhesive forces of film to the substrate. According to this model, the maximum tensile stress corresponds to the completion of the coalescence of the islands, and the stress is anticipated to be inversely proportional to the grain size. Within the first 0.1μm film thickness, the reduction of the tensile stress as the growth of the film can be explained by the gradual increase of grain size caused by recrystallization. This is very straightforward since with more grain boundary being eliminated, less attractive forces will be acting on the film. Grain growth can continuously contribute to the tensile stress relaxation as long as the grain size is not saturated and keeps increasing with film thickness. However, this process cannot induce compressive stress in the film. The appearance of compression in films beyond 0.2μm must occur under another mechanism.

Possible explanations for the generation of compressive stress as the films become thicker are Ar gas incorporation and ion peening. X-ray analysis of the TEM thin foil didn't reveal any Ar presence in the Au layer. However, there might be a tiny amount of Ar that was not detected because the Ar composition is below the detection limit. But the Ar incorporation cannot explain the compressive stress increase with film thickness unless the Ar content increases with thickness too, which tends to be unlikely. The ion peening mechanism proposed by D'Heurle [15] is a more plausible explanation, and is also supported by the TEM observation. The most significant feature observed from the TEM image of the 0.6μm film is the dense, "forest-like" dislocations and numerous dark spots. In comparison, only a few dislocations were observed in the 0.05μm film. These dislocations and dark spots are direct results of the continuous particle impingement on the growing film. During the deposition, the film atoms are displaced from their equilibrium positions through a series of primary and recoil collisions producing a volumetric distortion, which is frozen at low temperature because of insufficient mobility. Also, a large amount of interstitials is generated through bombardment and later will agglomerate to form interstitial clusters, or dislocations and dislocation loops by further interstitial capture. It is these interstitial clusters and dislocations that give rise to the compressive stress. The creation of these interstial defects is an accumulative process. The stress builds up when more such defects are created and more volumetric distortion are introduced, which explains the stress increase as film grows thicker and thicker.

It needs to be pointed out that the processes that contribute to the internal stress including vacancy and interstitial generation, dislocation loop growth, and grain growth proceed simultaneously, so that the resultant stress will be the sum of all these processes.

5.3 The Effect of Thickness on Resistivity of the as-sputtered Au/Pt/Ti Films

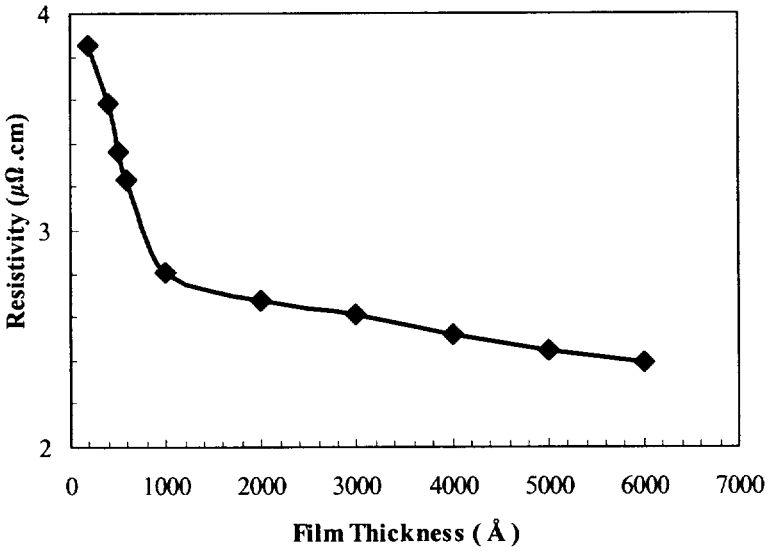

Figure 5.3 The effect of thickness on resistivity of as-sputtered Au film.

The resisitivities of sputtered Au were evaluated at various thicknesses and plotted vs. film thickness in Fig. 5.3. For a continuous thin film in microelectronic applications the resisitivity is a function of several parameters: temperature, purity, film thickness, crystallinity, defect structure, and applied field. The total resistivity is the sum of all the individual contributions of these factors. Fig. 5.3 shows film thickness dependence of resistivity and it is obvious that the resisitivity decreases with the increase of film thickness, which is expected because the scattering of the electrons from the interfaces of the film dominates all the scattering collisions when the thickness of the film approaches the mean free path (MFP) of the conduction electrons. In addition, the grain dimension increase during film growth as a result of the recrystallization also contributes to the drop of the resistivity. Although more defects including point defects and

dislocations were created as the film becomes thicker due to the continuous particle bombardment, and will result in an increase in resistivity, this clearly is not a dominant factor in Fig.5.3. However, defect density and its orientations play a more important role when films are annealed at elevated temperatures. The measurement shows that after being annealing at 350°C for 5 minutes, the resistivity of a 0.1μm film drops from 2.81$\mu\Omega$-cm to 2.498$\mu\Omega$.cm, and the resistivity of a 0.6μm film drops from 2.388$\mu\Omega$-cm to 2.013$\mu\Omega$-cm, which means a maximum of 15% reduction in resistivity by annealing. This has been attributed to the reduced defect density and the re-orientation of the dislocations. TEM cross-sections demonstrate that in the as-sputtered film most dislocations are perpendicular or inclined to the substrate, while after annealing, they are aligned parallel to the substrate. Schröder [16] has pointed out that the resistance of a dislocation is maximized when the dislocation line axis is perpendicular to the direction of current flow and is minimized when the current flows parallel to the axis. Therefore, post-deposition heat treatment is beneficial in lowering film resistance.

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6 Stress Relaxation Mechanisms of Sputtered Au/Pt/Ti Thin Films during Thermal Cycling

Thin metal films constrained by a rigid substrate are usually subject to thermal stresses during temperature cycling owing to the mismatch of thermal expansion coefficient between film and substrate. In integrated circuits, devices with thin metal films usually experience temperature excursions during the subsequent processing steps or service conditions. When the stress exceeds the elastic limit, films deform plastically and the ongoing relaxation process alters the film's electrical and mechanical properties. These alterations usually end up deteriorating microelectronics' performance and reliability. Understanding the relaxation mechanisms is essential to control the effects of stress on film properties. Recently, a substantial amount of research has been carried out in this field due to its growing importance. Particularly, there have been interests in Al [1] [2] and Cu [3] [4] [5] films because of their extensive usage as the metallizations for Si circuits. This chapter deals with the stress issues in sputtered Au film on Si substrate with an oxide layer in between during thermal cycling. The particular reason that motivates the interest in this field is that the relaxation of the metal films during PECVD Si_3N_4 deposition causes a series of reliability problem. One example is the hillock formation in MIM capacitors that will be discussed in next chapter. Solving the problem greatly relies on the understanding of the relaxation mechanisms.

6.1 Stress-Temperature Behavior of Sputtered Au/Pt/Ti Thin Films

The stress-temperature behavior of a sputtered Au/Pt/Ti film on SiO_2/Si substrate is shown in Fig. 6.1. When analyzing the stress curve, two points need to be

noted: 1. All the wafers used for stress measurement have a thin oxide layer on top to prevent the metal from diffusing into the substrate. The reported values of thermal expansion coefficient of Si and SiO_2 are 2.49×10^{-6} $°C^{-1}$ [6] and 0.5×10^{-6} $°C^{-1}$ ~ 4.1×10^{-6} $°C^{-1}$ [7] respectively, negligible thermal stress will be generated by adding a thin oxide layer. Thus, the stress-temperature curve is mainly determined by the thermal mechanical behavior of the metal films. 2. The measured stress only represents the average stress within the film stack. Whereas the stresses are different within each metal film and even vary along the thickness in each metal layer. Since Au/Pt/Ti films are always used together and experience same temperature excursions, understanding the stress behavior of the composite film structure is necessary.

Initially, since Au, Pt, and Ti all have much larger thermal expansion coefficient than the substrate, compressive stress built up and increased linearly with temperature due to the negligible relaxation rate. The slope of the curve in this regime is simply the product of difference in thermal expansion coefficients and the biaxial elastic modulus of the film. As temperature and stress increased, the relaxation rate eventually become comparable with the loading rate, leading to the maximum compressive stress around 100°C, which is the transition point where the rate of plastic relaxation exceeds the applied loading rate [8]. The relaxation rate kept increasing up to 300°C, resulting in a dramatic decrease of film stress. However, the relaxation rate was slowed down during the rest of the heating cycle, and a constant stress around 40Mpa is maintained within the film. On the cooling cycle, the stress become tensile and no obvious yielding was observed.

The stress-temperature curve of the second cycle had a completely different shape than that of the first one. Both the heating and cooling curve were straight lines with the slope close equal to that of the initial heating portion. Obviously, thermal strain is accommodated elastically in the second cycle. The curve shape difference indicates that the relaxation in the first cycle was accompanied by irreversible microstructural change.

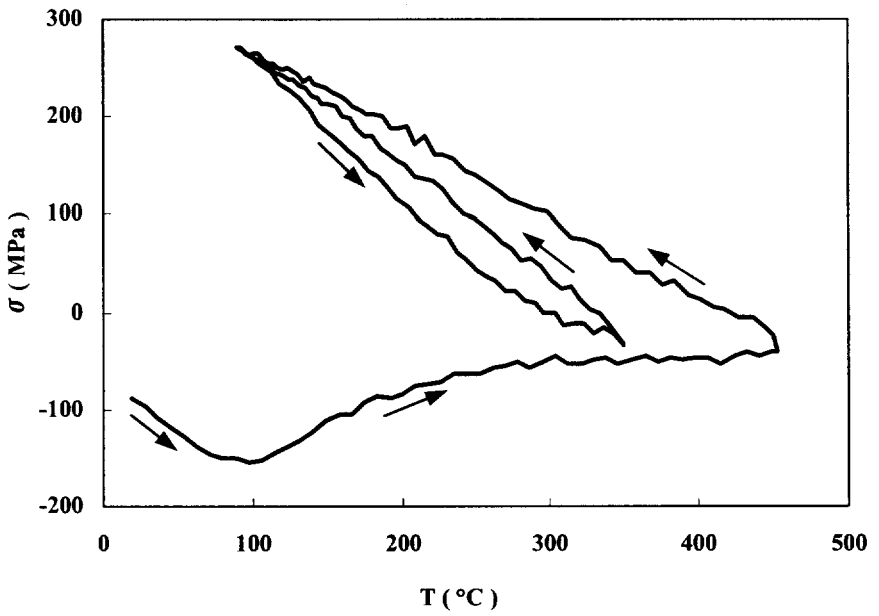


Figure 6.1 Stress-temperature behavior of Au(6000Å)/Pt(500Å)/Ti(500Å)/SiO_2/Si system during thermal cycling. The temperature ramping rate is 10°C/min.

The effects of film thickness and loading rate on stress-temperature behavior of sputtered Au/Pt/Ti films were also examined. As shown in Fig. 6.2, all these curves possessed the same features as illustrated in Fig. 6.1. Except for the residual stress, film thickness did not influence the stress development and relaxation process. The variation of temperature ramping rate affected the curve by changing the position of the maximum compressive stress point. A higher ramping rate led to a higher maximum compressive stress and the corresponding temperature was also higher. This can be easily explained by the competition between relaxation rate and loading rate. A higher temperature ramping rate means a higher loading rate, the relaxation rate cannot keep up with the loading rate, therefore more stress will be accumulated before these two rates became comparable.

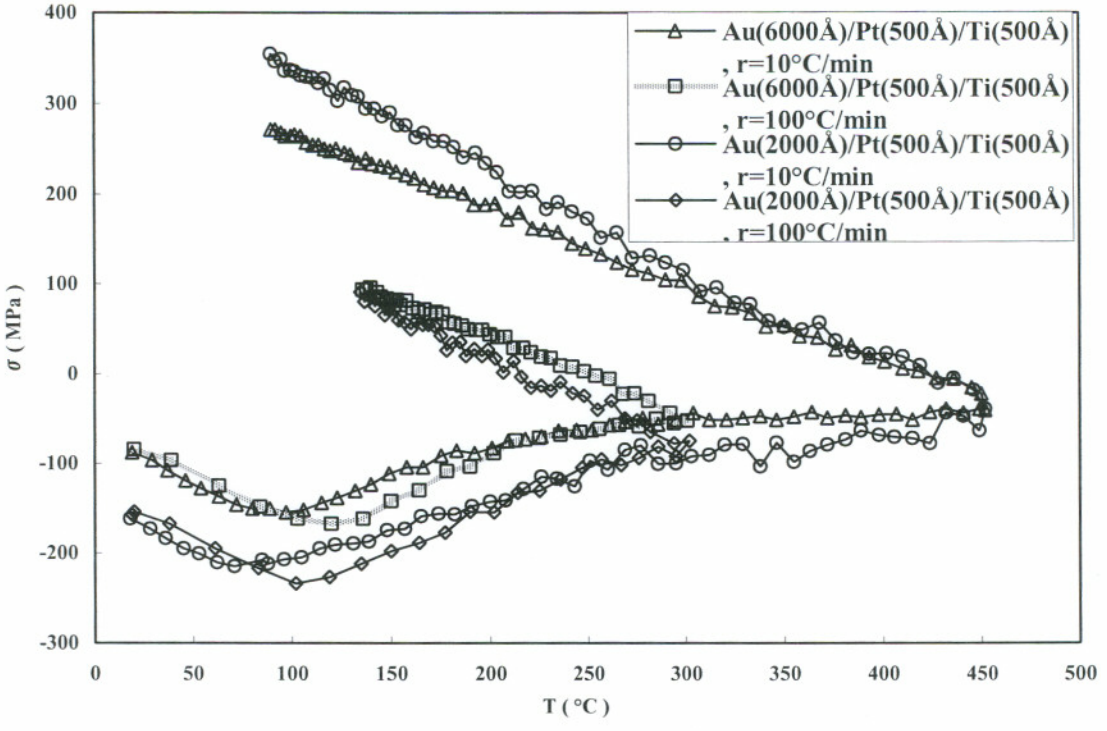


Figure 6.2 Effects of Au film thickness and temperature ramping rate on stress-temperature behavior of Au/Pt/Ti/SiO_2/Si system. Wafers with various Au film thicknesses were thermal cycled at temperature ramping rates of 10°C/min and 100°C/min respectively. The employed Au thicknesses were 6000Å and 2000Å, while the thicknesses of Pt and Ti were always 500Å.

As pointed out before, the stress obtained using substrate curvature method for a multilayer thin film stack is merely the average stress within the film. To further understanding the stress-temperature behavior of each metal film, single metal film are individually deposited on the substrate and their stress-temperature behaviors are shown in Figures 6.3, 6.4 and 6.5 respectively.

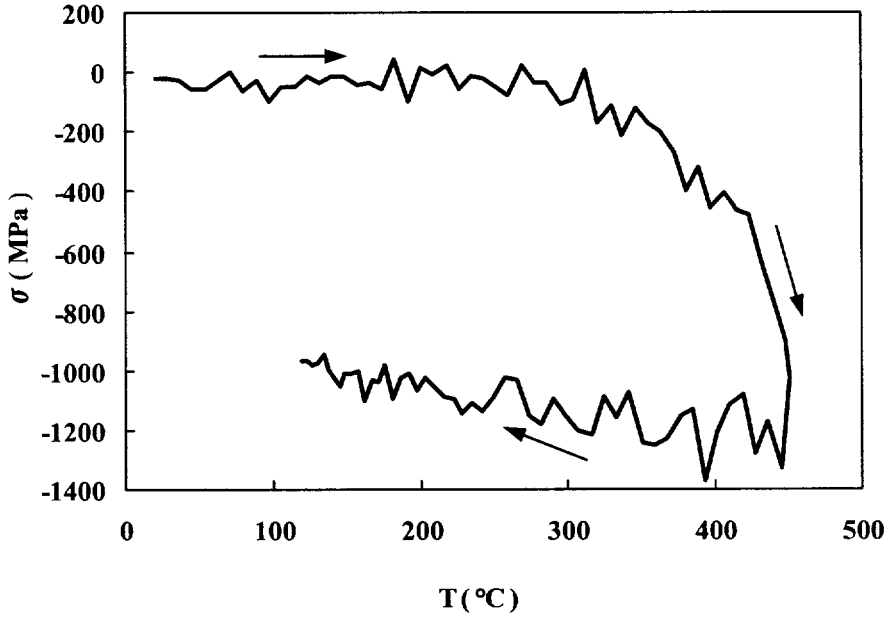


Figure 6.3 Stress-temperature behavior of Ti(500Å)/SiO_2/Si system during thermal cycling. The temperature ramping rate is 10°C/min.

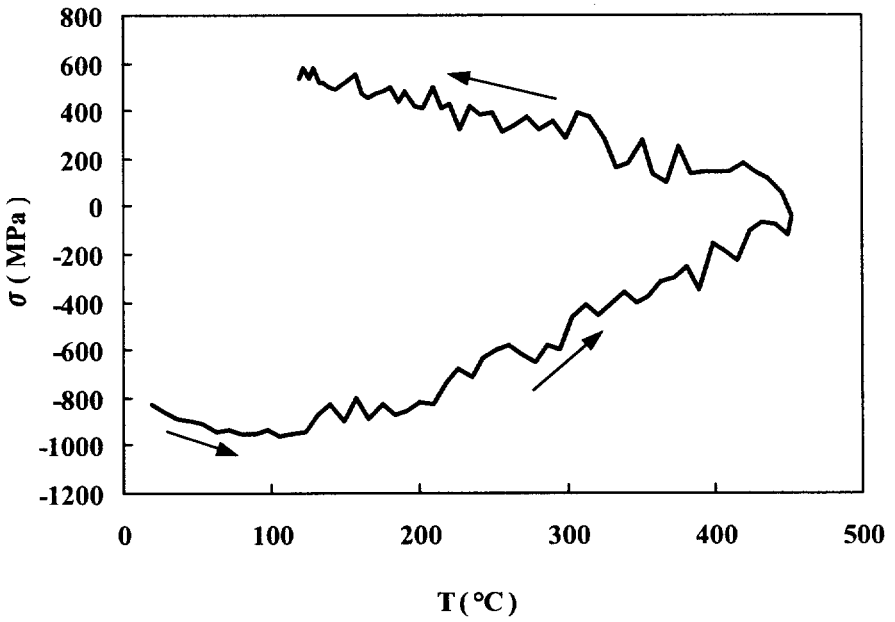


Figure 6.4 Stress-temperature behavior of Pt(500Å)/SiO_2/Si system during thermal cycling. The temperature ramping rate is 10°C/min.

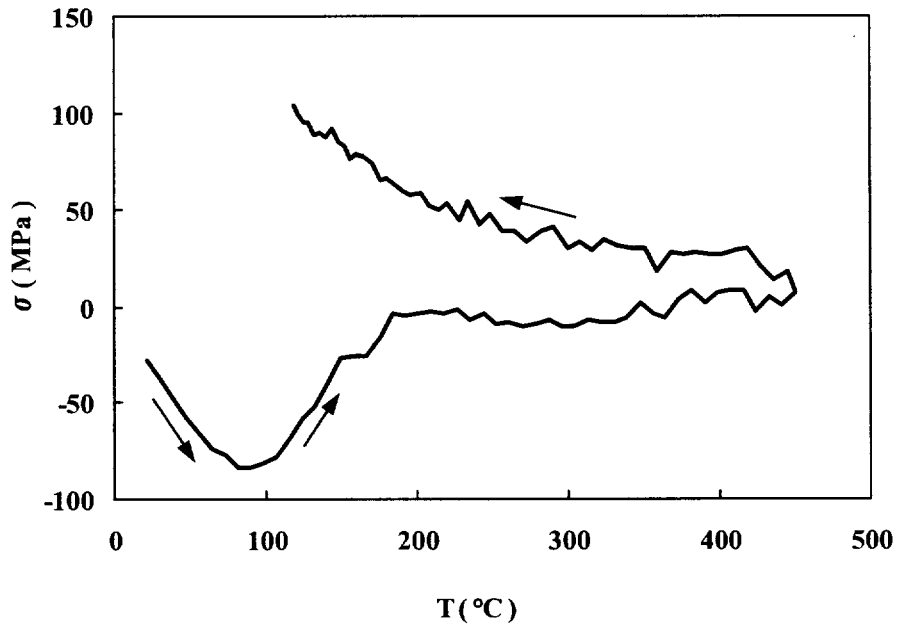


Figure 6.5 Stress-temperature behavior of Au(6000Å)/SiO_2/Si system during thermal cycling. The temperature ramping rate is 10°C/min.

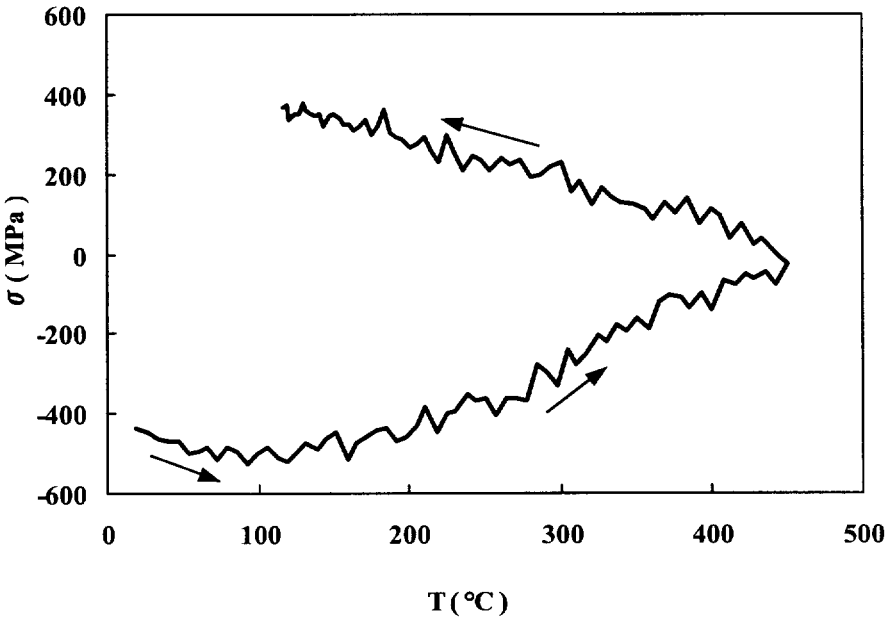


Figure 6.6 Stress-temperature behavior of Pt(500Å)/Ti(500Å)/SiO_2/Si system during thermal cycling. The temperature ramping rate is 10°C/min.

The stress-temperature curve of $Ti/SiO_2/Si$ system Fig. 6.3 cannot be explained by the normal stress development and relaxation process. The metal surface became rutile or purple in color after thermal cycling. Since the thermal cycling was carried out in an air ambient, it was suspected that the oxidation of the Ti layer had occurred because the color change observed here was in agreement with the oxidation reaction of Ti on SiO_2 reported by Sreenivas in ref [9].

The stress-temperature curve of the $Pt/SiO_2/Si$ system in Fig. 6.4 showed that the maximum compressive stress took place around 100°C and the stress kept decreasing through the whole heating cycle. No obvious reaction and diffusion of Pt were observed. In the cooling cycle, tensile stress was generated and increased linearly with the decrease of the temperature.

The oxidation reaction of the Ti film is not a concern when used a Pt layer is deposited above the Ti layer without breaking the vacuum, mainly because the Pt layer isolates the Ti from O_2, and the amount of O_2 diffusing through the Pt layer is very limited. Fig. 6.6 shows the stress-temperature curve of $Pt/Ti/SiO_2/Si$ system, which looks very similar to that of the $Pt/SiO_2/Si$ system. No color change was observed after thermal cycling.

In Fig. 6.5, the maximum compressive stress of a 6000Å sputtered Au film occurres around 90°C. Beyond that point, the compressive stress quickly drops to zero around 190°C and remains nearly zero during the rest of the heating cycle. The stress development in the cooling cycle can be divided into two stages: 1. Slow increase of tensile stress between 250°C and 450°C. 2. Rapid tensile stress increase below 250°C. This is probably due to that certain high temperature relaxation mechanism is still operative when stress turns tensile. While the temperature is dropping, the relaxation will be slowed down and eventually cease to operate. The detailed relaxation mechanisms of sputtered Au film will be addressed in the next section.

Now the additive effects of multiple films can be considered. When a second film is deposited on top of the first, any moments and bending caused by the second film would cause the strain in the first film to change very slightly. To a very good approximation, the stress in a given film depends only on its misfit with the substrate. The other films present have essentially no effects on the stress in a particular film.

Consider n films of thicknesses t_1, t_2, $t_3 \cdots\cdots t_n$, each thin film deposited on a substrate imposes a separate bending moment M_1, M_2, $M_3 \cdots\cdots Mn$, which correspondingly produces a curvature K_1, K_2, $K_3 \cdots\cdots Kn$. Since the moments are additive, so are the curvatures. The addition of the curvatures yields equation 5.1:

$$K_{total} = \left(\frac{1-\nu}{E}\right)_s \frac{6}{t_s^{\,2}}\left(\sigma_1 t_1 + \sigma_2 t_2 + \cdots\cdots + \sigma_n t_n\right) \qquad (5.1)$$

since $K_{total} = 1 / R_{total}$, equation 5.1 can also be written as:

$$\sigma_1 t_1 + \sigma_2 t_2 + \cdots\cdots + \sigma_n t_n = \left(\frac{E}{1-\nu}\right)_s \frac{t_s^{\,2}}{6R_{total}} \qquad (5.2) \quad \text{or}$$

$$\sigma_1 t_1 + \sigma_2 t_2 + \cdots\cdots + \sigma_n t_n = \sigma_{average}\left(t_1 + t_2 + \cdots\cdots + t_n\right) \qquad (5.3)$$

where $\sigma_{average}$ is the average stress in mutilayer films. According to equation 5.3, the average stress in Au/Pt/Ti multifilm stack can be predicted by:

$$\sigma_{average} = \frac{\sigma_{Au} t_{Au} + \sigma_{Pt} t_{Pt} + \sigma_{Ti} t_{Ti}}{t_{Au} + t_{Pt} + t_{Ti}} \qquad (5.4)$$

the calculated stress-temperature curve of Au(6000Å)/Pt(500Å)/Ti(500Å) films is plotted in Fig.6.7, together with the experimental data for comparison. Comparing the predicted data with the experimental data, two discrepancies were observed: 1. The experimental stress curve shows that a constant compressive stress about 50Mpa was sustained between 250°C and 450°C in the heating cycle. However, this sluggish relaxation was not expected using the model above. 2. The real stress developed in the cooling cycle was higher than predicted. The first discrepancy implies that the relaxation rate was decreased at high temperature in the multifilm stack. Since the thermal cycling of a single layer of Au, Pt, and Ti on substrate did not reveal any difficulty of stress relaxation in the high temperature range, this cannot be explained unless a relaxation process was suppressed

when these films are used together. The relaxation of the Au film is not likely to be significantly affected because it is the top layer and the underlying Pt and Ti have little effect on it. But, the relaxation of Pt and Ti are going to be different considering that the free surfaces in the single film are replaced by metal/metal interfaces. The diffusion along surface or interface is very important in thin films because the grain boundary diffusion, a dominant stress relaxation mechanism at high temperature, cannot work in a thin film unless it is coupled with surface or interface diffusion [10]. However, the atom diffusivity at a metal/metal interface is much lower than that of a free surface, consequently, the relaxation by coupled surface and grain boundary diffusion will be significantly suppressed in the sandwiched films. From this point of view, the flattening of the stress-temperature curve at high temperature in Au/Pt/Ti multifilm stack is probably caused by the lacking of relaxation through of coupled surface and grain boundary diffusion in Pt and Ti films. The diffusivities at the metal/oxide interface and metal/metal interface may also play a minor role. The second discrepancy can be explained in the same way. In addition, the resistance to dislocation motion imposed by the metal/metal interface also inhibits the relaxation process.

In summary, Au, Pt, and Ti all contribute to the stress relaxation within Au/Pt/Ti/SiO_2/Si system in the low temperature range (<300°C), whereas at high temperatures (300-450°C) Au film dominates the relaxation process. In practice, the thickness of Au film employed is 5-10 times larger than that of Pt and Ti films. The performance and reliability of Au/Pt/Ti metallization scheme is mainly determined by the properties of the Au film. Therefore, only the stress relaxation mechanisms of sputtered Au film during thermal cycling will be discussed in detail in the next section.

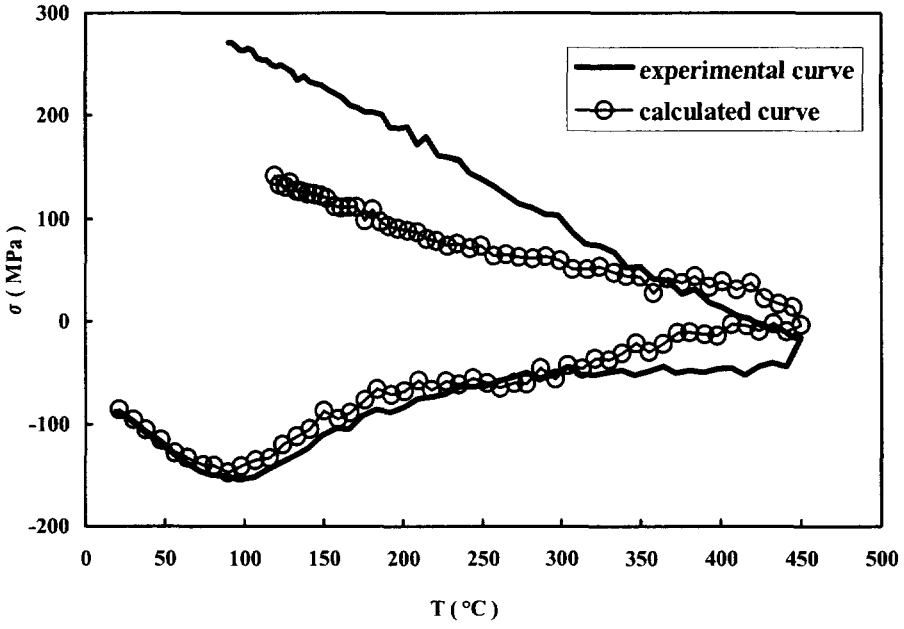


Figure 6.7 Comparison of calculated and experimental stress-temperature behavior of Au(6000Å)/Pt(500Å)/Ti(500Å)/SiO_2/Si system. The temperature ramping rate is 10°C/min.

6.2 TEM Study of Stress Relaxation Mechanisms of Sputtered Au Film during Thermal Cycling

So far, a considerable amount of effort has been made trying to control the film stress through modeling. A general approach is to obtain the thin film stress-temperature behavior using the substrate curvature method based on Stoney's formula, and then compare the modeling result with the experimental data. The comparison usually provides valuable information about the dominant relaxation mechanisms in various regimes. Most of the stress relaxation models are established based on Frost and Ashby [11] investigation on deformation mechanism of bulk metals. A summary of these deformation models was given in section 3.3. Since a thin film varies from bulk materials

in aspects such as film microstructure and mechanical constants, applying the models developed for bulk metals to thin film stacks require appropriate modifications. Thouless [12] have modified the diffusional creep equations to account for the fact that matter flows between the grain boundaries and the free surface rather than between neighboring grain boundaries. He proved that by entering the correct thin film parameters these modified models can be successfully used to simulate stress-temperature behavior of a thin Cu film. Generally, the discrepancies between simulation results and experimental data usually exist and it greatly relies on the accuracy of the model and the thin film parameters used during the simulation. The analysis becomes especially complicated because certain parameters sensitively depend on the film thickness and process conditions. In this Study, at specific temperatures during thermal cycling specimens were quenched and TEM cross-sections were produced to characterize the microstructural evolution of Au film during stress relaxation. The dominant relaxation mechanisms can be directly predicted from the microstructural evolution. The TEM cross-sections were produced by the following procedures: 2cm × 2cm sections cut from an as-deposited wafer were heated in differential scanning calorimetry (DSC) to desired temperatures at a ramping rate of 10°C/min. Ar ambient was used because of its good thermal conductivity. After reaching the desired temperature, the specimen was quenched immediately in order to freeze the microstructure at a certain temperature. The quenching was realized by pouring liquid nitrogen into a cap around the DSC cell. While cooling the Ar ambient, the specimen's temperature dropped rapidly and the cooling rate was measured to be approximately 100°C/min. Little microstructure change was expected during the cooling.

The stress-temperature behavior of a 3000Å Au film on the Si substrate with a thin oxide layer in between was shown in Fig.6.8. Initially, the relaxation rate is negligible and the stress increases linearly with temperature. The stress is compressive because Au has a much larger thermal expansion coefficient than the substrate. The maximum compressive stress around 80°C is the transition point at which the rate of plastic relaxation exceeds the applied loading rate. As the effect of relaxation become more obvious, the film stress decreases rapidly and dropped to nearly zero around 180°C. On the cooling cycle, the stress become tensile and no obvious yielding was observed up to 100°C.

This study focused on the stress relaxation mechanisms of the compressive stress in a sputtered Au film during the heating cycle. The TEM images of the microstructural evolution of Au film during thermal cycling were shown in Fig.6.9. Electron diffraction proved that the Au film is highly textured with (111) planes nearly parallel to substrate with a maximum 10° deviation. The as-sputtered film in Fig.5.9 (a) consists of columnar grains with a high density of dislocations and interstitial clusters as a result of the energetic ion bombardment. Compressive residual stress of 12.6MPa was found in the as-deposited condition and is most likely caused by the extra planes and atoms stuffed into the lattice during sputtering.

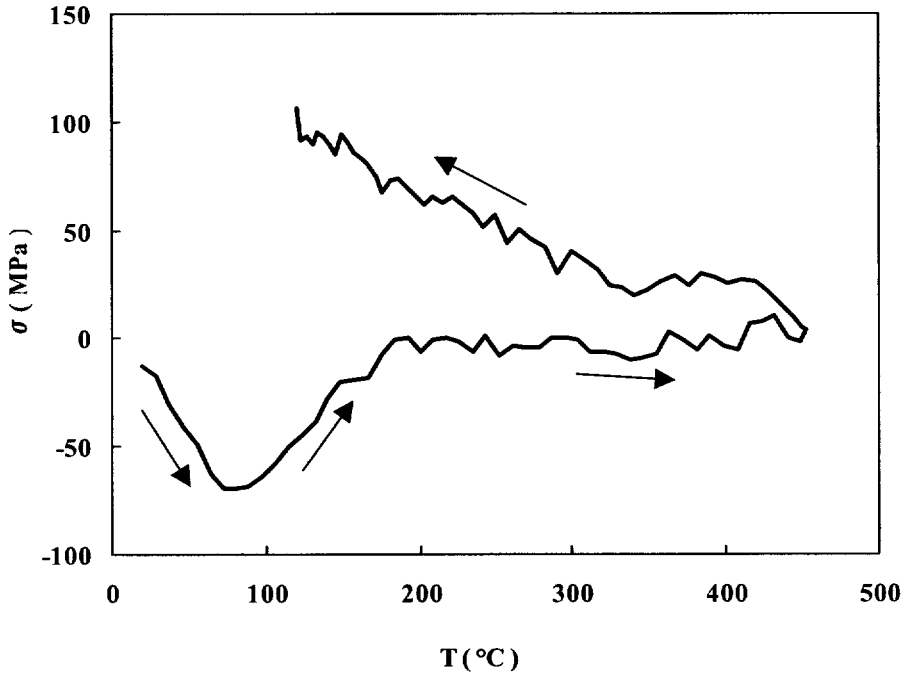
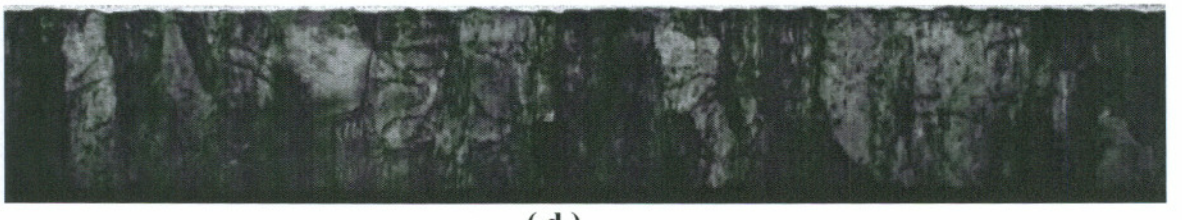


Figure 6.8 Stress-temperature behavior of Au(3000Å)/SiO_2/Si system during thermal cycling. The temperature ramping rate is 10°C/min. A thin layer of SiO_2 was deposited onto the substrate to prevent Au from diffusing into the Si.

(a)

(b)

(c)



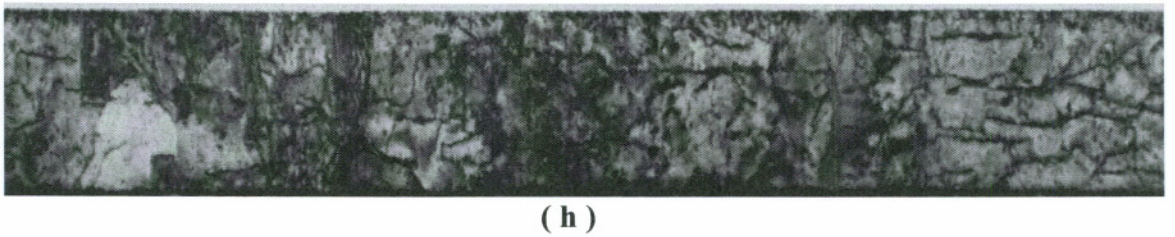
(d)

300 nm

(e)

(f)

(g)



(h)

300 nm

Figure 6.9 Microstructural evolution of sputtered Au film during thermal cycling. Each TEM cross-section corresponds to the microstructural condition of Au film at a certain temperature during thermal cycling. The temperatures are (a) room temperature, (b) 75°C, (c) 150°C, (d) 200°C, (e) 250°C, (f) 300°C, (g) 350°C, and (h) 400°C respectively.

The first salient feature on the stress-temperature curve is the rapid stress relaxation between 90°C and 180°C. Referring to TEM images in Fig. 6.9, little microstructure change can be detected up to 150°C, while an obvious decrease of dislocation density is observed at 200°C in Fig. 6.9(d). At this intermediate temperature range, relaxation by diffusional flow such as grain boundary diffusion and lattice diffusion is negligible because such processes require temperature higher than roughly $T_m/3$ of pure metal. The most likely mechanism responsible for relaxation in this regime is dislocation motion, which is probably dislocation glide since climb is generally activated at higher temperatures. For a fcc metal, gliding along the (111)<110> slip system is believed to control the relaxation process. When the resolved shear strength on the glide plane exceeds the minimum stress required to move the dislocations, the dislocations start to glide and contribute to the stress relaxation. As a result, the compressive stress rises only slowly and eventually passes through a maximum around 90°C on the stress curve. With continued increase of temperature, gliding becomes much easier owing to the thermal assistance, resulting in reduced flow stress. The decrease of stress after the maximum is interrupted at 150°C, where the stress remains almost constant for a short period and starts to decrease again at 166°C. This can be explained by the hindered dislocation glide at obstacles, mainly grain boundaries. Frost and Ashby have discussed the relaxation by dislocation glide in bulk metals in ref [11]. As they pointed out, the low temperature plasticity by dislocation glide is almost always obstacle-limited. The TEM cross-section in Fig. 6.9(a) shows that the obstacles in a sputtered Au film are mainly other dislocations, interstitial clusters, and grain boundaries. While the dislocations glide, they interact with other dislocations and interstitial clusters. The mean velocity of these dislocations determines the rate of transport of atoms to the grain boundaries and interfaces, resulting in the initial relaxation rate below 150°C. Neither recrystallization nor dramatic dislocation annihilation is observed below 150°C. Therefore, most of the mobile dislocations will eventually get piled up against the grain boundaries. Further relaxation becomes much more difficult, leading to the constant stress between 150°C and 166°C. A significant decrease of dislocation density is observed between 150°C and 200°C from Fig. 6.9(c) and Fig. 6.9(d), which can explain the restarted stress decreasing beyond 167°C from the following two points: 1. The

dislocations are very likely being absorbed at grain boundaries. With a large number of dislocations being annihilated at grain boundaries, the average dislocation spacing increases, which, according to Frost and Ashby's model, lower the Gibbs free energy for dislocation gliding. Besides the interaction of dislocations with grain boundaries, the dislocation-dislocation interaction also leads to dislocation annihilation. 2. Dislocation annihilation leads to the relaxation of the stress because the lattice distortions introduced by these dislocations are removed.

It is interesting to notice that most of the dislocations perpendicular or inclined to the substrate disappear at temperatures above 300°C. The remaining dislocations are close or nearly parallel to the substrate. Both perpendicular and parallel dislocations originally exist in the as-sputtered film. Since the resolved shear in the direction perpendicular to the substrate is zero in an equibiaxial stressed film, the parallel dislocations hardly glide under in-plane stress. Conversely, the perpendicular dislocations can glide easily on their glide plane until stopped by grain boundaries or other dislocations. When large number of perpendicular dislocations have been annihilated, the parallel dislocations become more visible. Therefore, gliding of these perpendicular dislocations dominates the relaxation process.

At temperatures above 180°C, the stress remains nearly zero, which means that the relaxation rate is so fast that any thermal stress developed within the film can be relieved immediately. This requires a relaxation rate equal or greater than the thermal strain rate. Dislocation glide is still operative in the high temperature range but becomes less important both due to the remaining low dislocation density and low stress level. Grain growth has been observed in TEM images, which is certainly a contributing relaxation mechanism because the film gets densified when the extra volumes possessed by the grain boundaries are eliminated. Other than grain growth, Grain boundary grooves on an Au surface was revealed by AFM scanning on samples that have been thermal cycled to 300°C and above. The grain boundary grooves and triple junctions are pointed out in Fig. 6.10. These grooves indicate that grain boundary diffusion also contributes to the relaxation process. The formation of grain boundary groove under stress-driven grain boundary diffusion is illustrated in Fig. 6.11. This process can be divided into two steps:
1. Under compressive stress, atoms are transported from the bulk film to the free surface

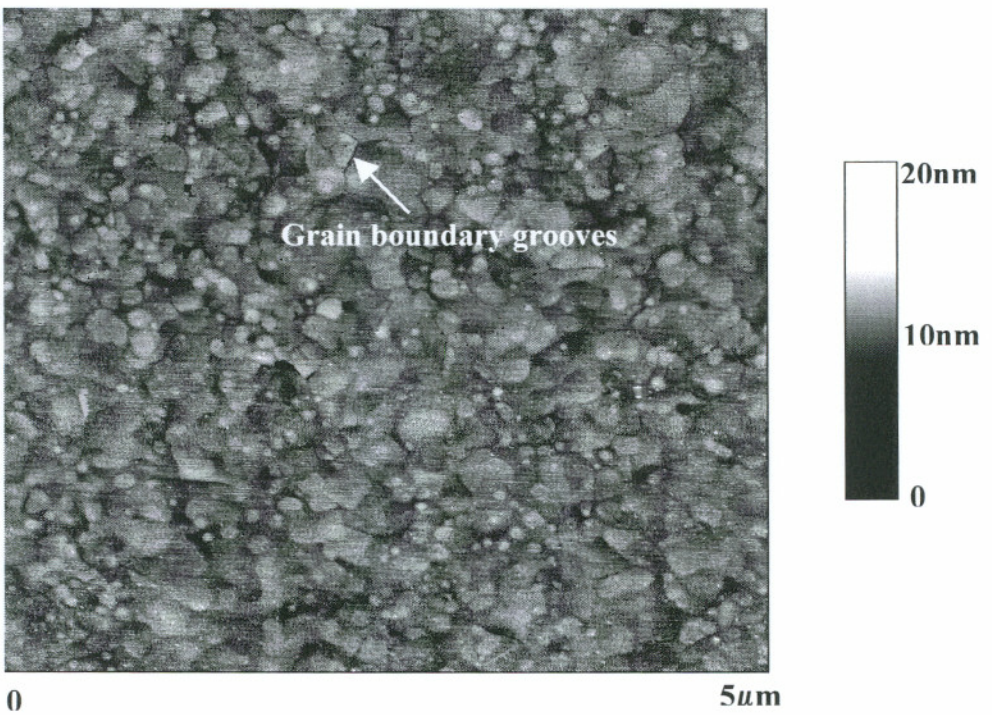


Figure 6.10 AFM image of Au surface that has been thermally cycled to 350°C, showing the presence of grain boundary grooves as a result of coupled grain boundary and surface diffusion in response to compressive stress.

through grain boundary diffusion. 2. Atoms at the film surface will be redistributed by surface diffusion. As pointed out by Thouless [10], Coble and Nabarro Herring creep, cannot operate if the stress-state is equi-biaxial and there is no difference in the chemical potential of neighboring grain boundaries. However, the stresses in unpassivated films may be relaxed by the diffusion of matter between the bulk of the film and the surface, either by diffusion through the lattice diffusion or along the grain boundaries. In this case, grain boundary diffusion plays a more important role than lattice diffusion. If the rate of surface diffusion cannot compete with that of grain boundary diffusion, hillocks will develop at film surface, as shown in Fig.6.11(a). In case of fast surface diffusion, atoms migrate along the surface so as to reduce a minimum surface free energy. The resultant grain boundary grooves are formed driven by the minimization of surface and grain boundary area.

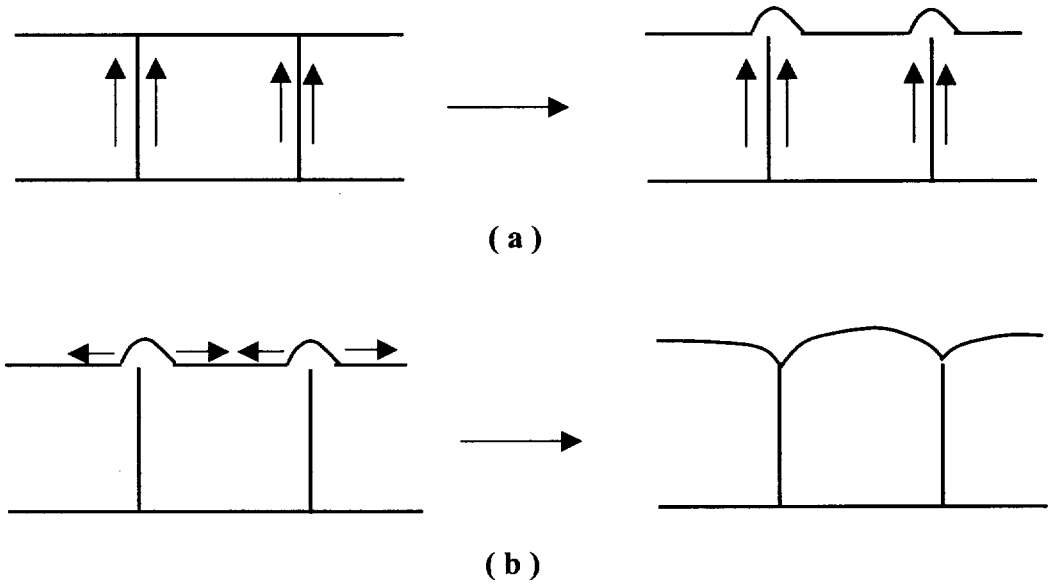


Figure 6.11 Formation of grain boundary grooves under compressive stress by coupled grain boundary and surface diffusion. (a) Atoms are transported from the bulk film to the free surface through grain boundary diffusion. (b) Atoms at the film surface are redistributed by surface diffusion.

To determine whether the coupled grain boundary and surface diffusion dominates the stress relaxation at temperatures greater than 180°C, we employ a model derived by Thouless [10] to calculate the strain relaxation rate induced by this mechanism. The strain relaxation rate by coupled surface and boundary diffusion can be estimated by equation 6.1

$$\dot{\varepsilon}_r = 3D_b\delta_b\Omega\frac{\sigma}{kTlh^2} \qquad (6.1)$$

where D_b is the grain boundary diffusion coefficient, δ_b is the boundary width, Ω is the atomic volume of the diffusing species, σ is the film stress, k is the Boltzmann's constant, T is the absolute temperature, l is the grain size, and h is the film thickness. The grain boundary diffusivity $D_b\delta_b$ can be calculated according to equation 6.2

$$\delta_b D_b = \delta_b D_0 \exp(-Q/RT) \quad (6.2)$$

where D_0 and Q are the pre-exponential factor and activation energy for boundary diffusion, and R is the gas constant. The relevant material parameters of Au and the calculated strain relaxation rate at various temperatures are given in Table 6.1. The thermal loading rate can be obtained from equation 6.3

$$\dot{\varepsilon}_l = (\alpha_{Au} - \alpha_{GaAs})\Delta T \qquad (6.3)$$

with thermal expansion coefficient being denoted as α. For a heating rate of 10°C/min, taking α_{Au} as 14.2×10^{-6} [6] and α_{Si} as 2.49×10^{-6} [6], the resultant loading rate is $1.95\times10^{-6}s^{-1}$. The relaxation rates in Table 6.1 are then compared with the loading rate. The comparison shows that grain boundary diffusion is negligible below 150°C. The relaxation rate by grain boundary diffusion becomes comparable to the loading rate at 200°C and finally exceeds it somewhere between 200°C and 250°C. Beyond this temperature, boundary diffusion alone is adequate to relieve the thermal stress developed in the film, which strongly supports that the grain boundary diffusion is the dominant relaxation mechanism.

Table 6.1 Calculation of strain relaxation rate by grain boundary diffusion

$\delta_b D_0 = 3.1 \times 10^{-16} m^3 s^{-1}$ [13]
$Q = 84.906\ kJ.mol^{-1}$ [13]
$\Omega = 1.695 \times 10^{-29} m^3$
$R = 8.31441$
$k = 1.38 \times 10^{-23} JK^{-1}$

T (°C)	σ (MPa)	l (10^{-9}m)	$D_b\delta_b$ (m^3s^{-1})	$\dot{\varepsilon}_r$ (s^{-1})
21	-12.6	160	2.55×10^{-31}	4.22×10^{-12}
74	-69.1	177	5.13×10^{-29}	2.36×10^{-9}
90	-68.5	177	1.88×10^{-28}	8.21×10^{-9}
150	-20.5	209	1.02×10^{-26}	9.68×10^{-8}
201	-5.9	230	1.36×10^{-25}	3.01×10^{-7}
253	-8	306	1.15×10^{-24}	2.34×10^{-6}
304	-1	306	6.38×10^{-24}	1.48×10^{-6}
355	-7.5	574	2.69×10^{-23}	2.29×10^{-5}
398	-3.2	767	7.62×10^{-23}	1.94×10^{-5}

In summary, the relaxation of the compressive stress at intermediate temperatures (70°C-200°C) is controlled by thermally assisted dislocation glide. The relaxation is hindered when dislocations pile up against grain boundaries around 150°C-167°C. Further relaxation is enabled when a significant amount of dislocations is absorbed at grain boundaries. At higher temperatures (>200°C), stress-driven grain boundary diffusion coupled with surface diffusion dominates the relaxation process. Grain growth has a minor contribution to the relaxation process.

6.3 In-situ TEM Study of Stress Relaxation Mechanism of Sputtered Au Film during Thermal Cycling

In section 6.2, the microstructure of Au film was only examined at selected temperatures due to the time-consuming TEM cross-section preparation procedure. The detailed information about microstructural evolution occurring between two selected temperatures is yet unknown. To gather this information, the in-situ heating TEM technique is employed to continuously observe the microstructural change during annealing. In this technique, a finished TEM cross-section is loaded into a specially designed TEM holder which runs a certain amount of current through the specimen so that the sample temperature can be ramped at the desired rate. Since the heating is insitu, the interested microscopic activities including dislocation motion, defects annihilation, grain growth, and recrystallization can be observed real-time.

The first insitu experiment failed because a catastrophic recrystallization occurred around 250°C before any obvious microstructural change was observed. After recrystallization the original polycrystalline Au film became a single crystal. The recystallization process originated from one end of the foil, propagated rapidly all the way to the other end. It is believed that diffusing of Au atoms under the stress gradient causes this recrystallization. In a FIB produced TEM specimen, due to the geometry effect the stresses within the supporting bulk film is much larger than that within the thin foil located at the center of the canyon. Therefore a stress gradient exists at the bulk-foil boundary. As a result, large amounts of atoms flow from the bulk film to the thin foil. Atom-atom collisions and energy transfers take place along the diffusion path, which increases the mobility of the Au atoms in the thin foil and allow them to eventually reside at new lattice sites with lowest energies. To eliminate the stress gradient, two deep cuts were made at the bulk-foil boundary to disconnect them from each other, leaving the foil only connected with the bulk specimen at the substrate. Thus the atoms diffusion is solely controlled by the stress within the foil.

With the thin foil isolated from the bulk film, the catastrophic recrystallization process did not happen in the second insitu experiment. However, the expected dislocation gliding, coupled surface and grain boundary diffusion and grain growth were

still not observed. Fig. 6.12 shows the still images made from the recorded videotape. The dense dislocations in the as-sputtered film did not move much during the heating, instead most of them gradually faded and eventually disappeared. In comparison, the TEM images of the quenched specimen shows that the dislocations within the bulk film glide inside grains and get annihilated either at grain boundary or by dislocation-dislocation interaction. The discrepancy of these two observations can be explained from the following points: 1. Due to the film geometry restriction, the stress within the bulk film is equi-biaxial while the stress within the TEM thin foil is uniaxial. Also, under identical temperature excursion, the thermal stress generated within the thin foil is much smaller than stress generated within the bulk film, and it is just not large enough for a dislocation to overcome the obstacles and glide to the grain boundaries. Relatively, it is easier for dislocations to climb a short distance to the foil surfaces considering the TEM specimens are only about 500Å-1000Å thick. The dislocations will fade away and eventually vanish as more parts of a dislocation have climbed to the foil surface. 2. In a cross-section TEM specimen, the film surface is covered by a platinum coating, hence surface diffusion is not available. Consequently, atoms at grain boundary will diffuse to the foil surfaces rather than to the film/coating interface.

In order to eliminate the thin foil geometry effect and make the insitu observation more accurately reflects the microstructural evolution in a bulk film, a thicker TEM specimen was utilized and insitu heated inside a 300kV TEM microscope at Lawrence Berkeley National Laboratory. However, no obvious dislocation glide was observed which is probably because that the specimen was still not thick enough to eliminate the thin foil effects. As shown in Fig. 6.13, the defect density started to drop around 250°C. At about 310°C, recrystallization occurred and new grains with nearly now defects were formed.

So far, the insitu studies of the stress relaxation mechanism are not quite successful due to the thin foil effects. Further efforts should be made trying to eliminate this effect.

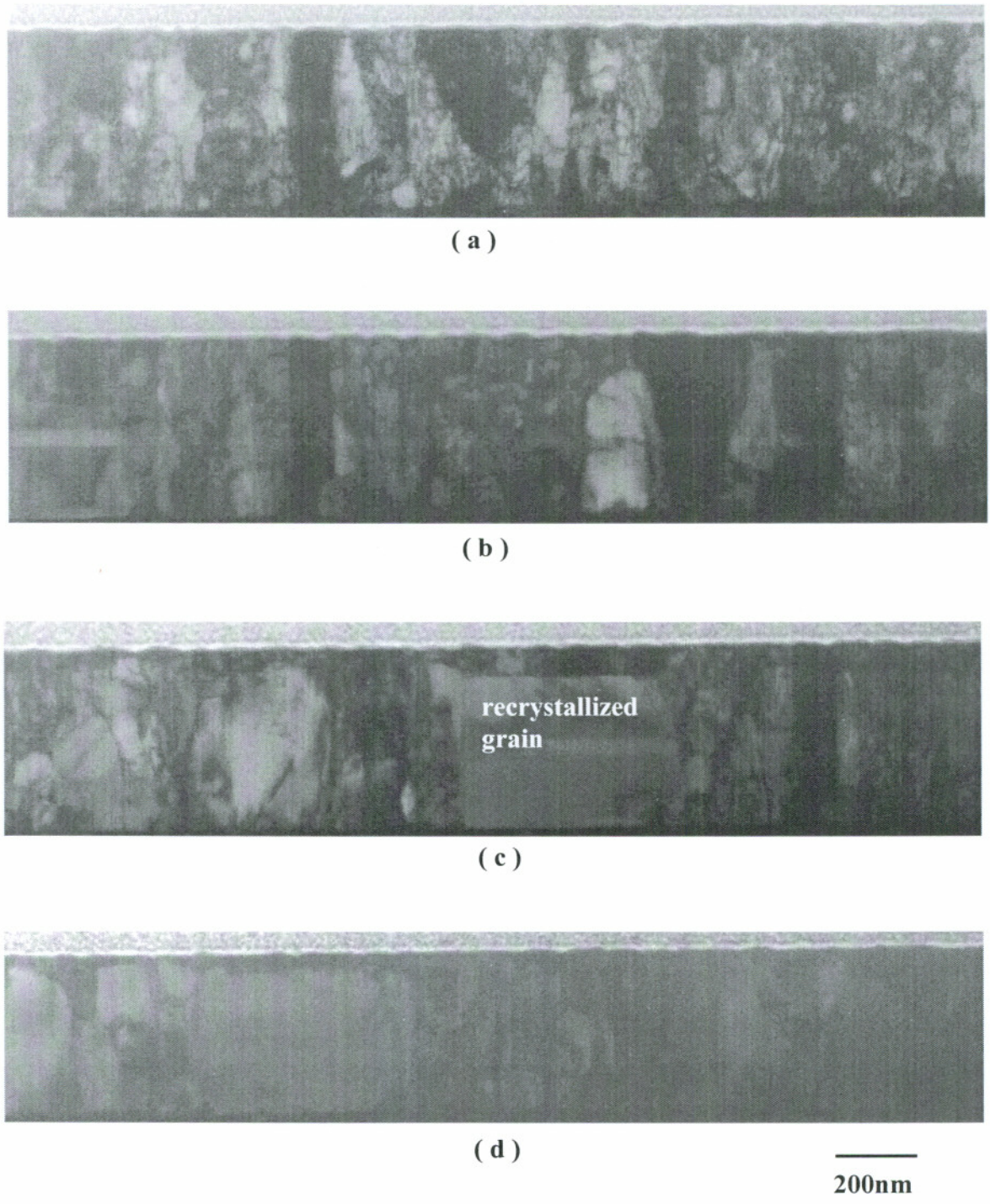


Figure 6.12 Video-captured TEM images show microstructural evolution of sputtered Au film during insitu TEM heating. Image (a) is in as-sputtered condition. Images (b)-(d) were captured at the following temperatures: (b) 200°C. (c) 310°C, (d) 415°C.

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7 Hillock Formation in Passivated Sputtered Au/Pt/Ti Thin Film Contact and its Effects on MIM Capacitor's Electrical Performance

Hillock formation in metallization has always been a great concern to process engineers considering its effect on device performance and reliability. In spite of all the advantages sputtering has brought to us, one problem we have encountered with this new technique was the hillock formation during PECVD process, in which a thin layer of Si_3N_4 was deposited onto the existing as-sputtered Au/Pt/Ti films to serve as device passivation or dielectric layer for MIM capacitors. Consequently, the electrical performance of the MIM capacitor was dramatically degraded. Even though hillocks have been extensively investigated by many researchers, most of the previous work dealt with the thermally induced hillocks in Si metallizations such as Al-Cu. According to our knowledge, hillock formation was rarely reported in GaAs metallization. In this chapter, we will explore the hillock formation mechanism and emphasize its effects on the electrical performance of MIM capacitors.

7.1 Comparison of Evaporated and Sputtered Films

Fig. 7.1 is the AFM image of the top Au layer in the as-sputtered Au/Pt/Ti metal stack. Hillocks are not observed in the as-sputtered film. A cross-sectional line was drawn on the top-view image and the vertical profile along this line is displayed in below. This two-dimensional profile shows that the Au film has a very smooth topography other than the presence of a uniform film roughness.

Hillocks are observed after depositing a dielectric layer on sputtered metal stack. Fig. 7.2 presents typical hillocks image generated by performing an AFM scanning on the dielectric surface. The cross section of the marked hillocks shows that the heights of these hillocks are in a range of 60-80Å and the diameters are about 2-3μm. Compared to those "gigantic" hillocks formed in other metal films, these nanoscale hillocks were extremely small in height, but not quite small enough to be ignored if we think about the dielectric thickness which has been scaled down to a few hundred angstroms in order to fabricate capacitors with small area and high capacitance. These hillocks not only affect the precision of the capacitance, moreover, they also raises reliability problem of possible dielectric penetration.

In comparison, hillock formation is not a concern for evaporated film. Fig. 7.3 and Fig.7.4 shows the AFM image of the evaporated Au film in as-deposited and passivated condition respectively. Neither of them shows the hillock presence. The microstructures of as-sputtered and as-evaporated Au/Pt/Ti are compared in Fig. 7.5. The as-sputtered Au film in Fig. 7.5(a) consists of columnar grains with high density of dislocations and interstitial clusters as a result of the energetic ion bombardment. On the contrary, the as-evaporated Au film has a much less defect density.

The residual stress measurement, which is given in Fig. 7.6, shows that compressive stress is introduced in metal film during sputtering and tensile stresses is introduced during evaporation. This result coincides with the theory that hillocks tend to form in metal film under compression as a result of stress relaxation. However, this is only a possible mechanism and no conclusions can be drew at this point, further characterization of surface topography evolution during the stress relaxation at high temperature is essential to verify its suitability in this case.

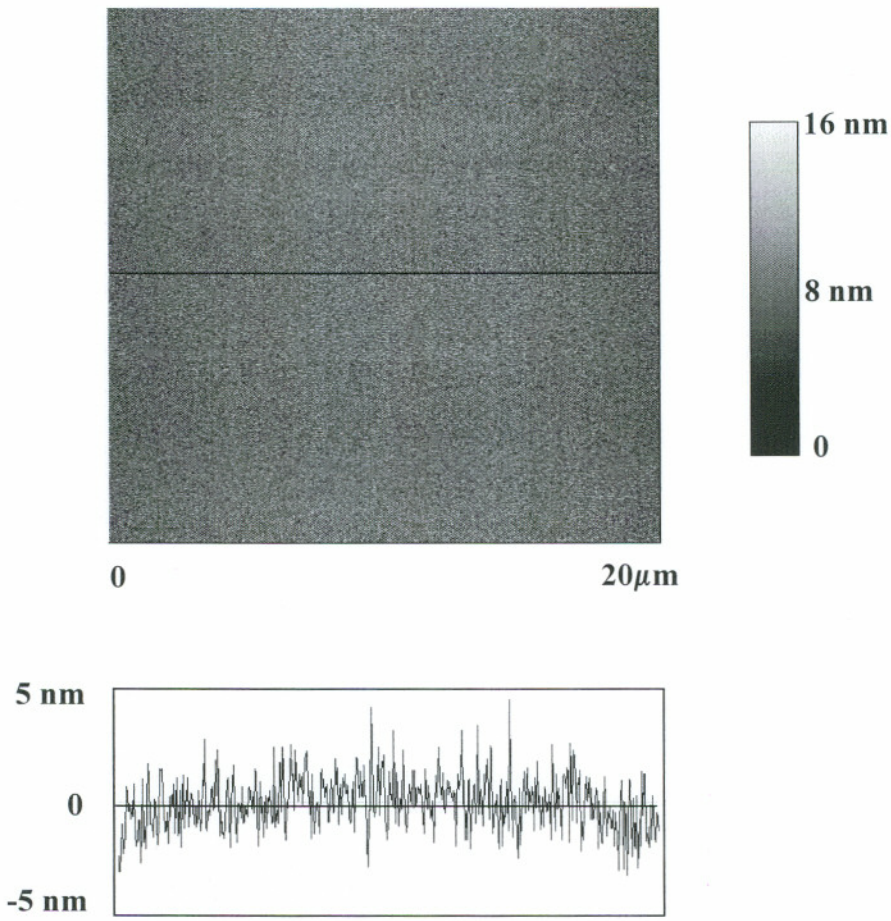


Figure 7.1 AFM topography and cross-sectional profile of the top Au layer in the as-sputtered Au/Pt/Ti films. Hillocks are not observed.

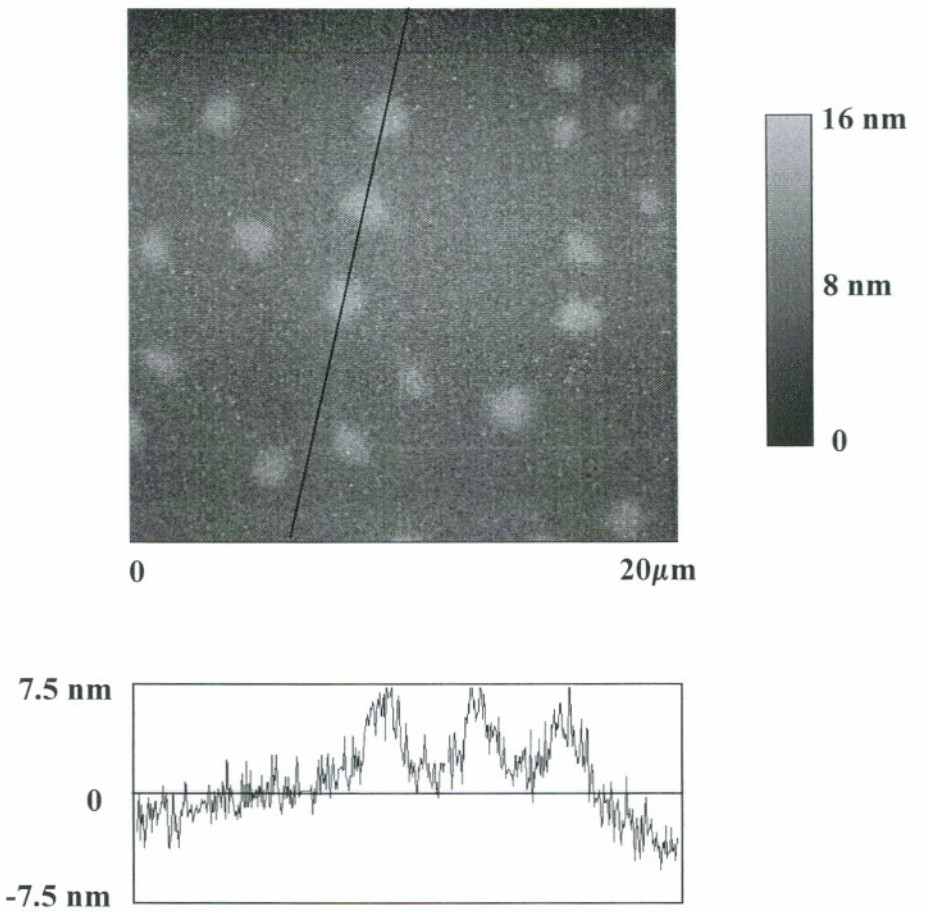


Figure 7.2 AFM topography and cross-sectional profile of the Si_3N_4 passivated sputtered Au/Pt/Ti films. Hillocks are observed.

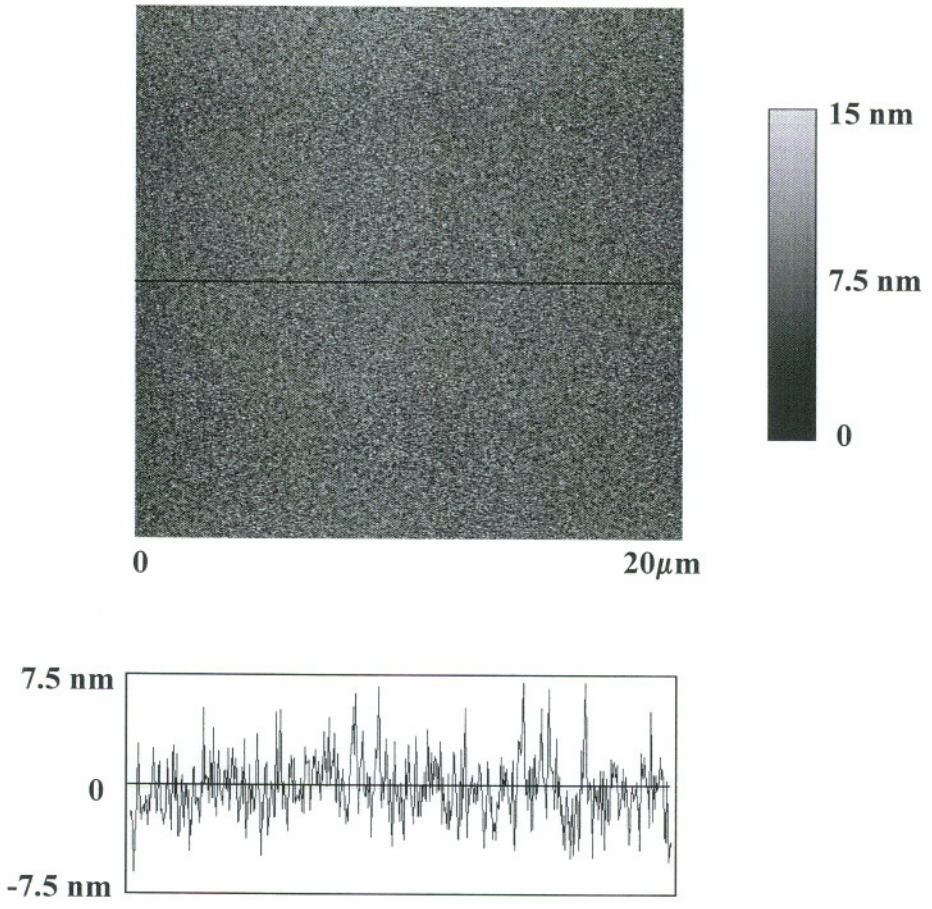


Figure 7.3 AFM topography and cross-sectional profile of the top Au layer in the as-evaporated Au/Pt/Ti films. No hillocks are found.

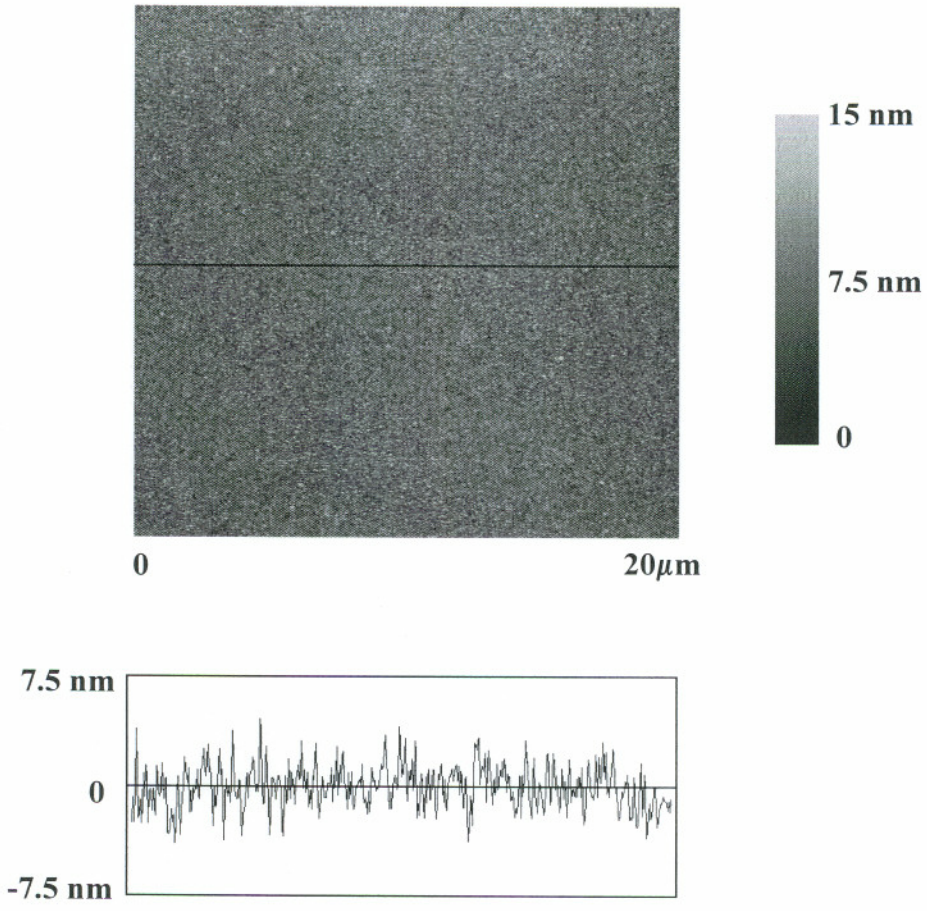
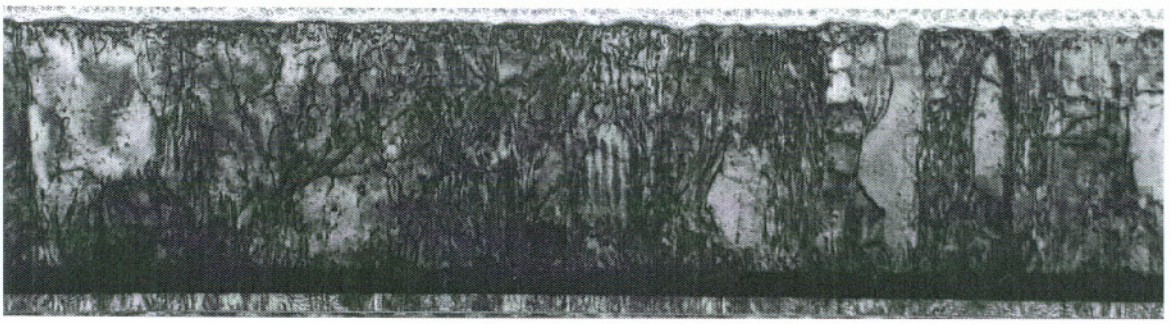
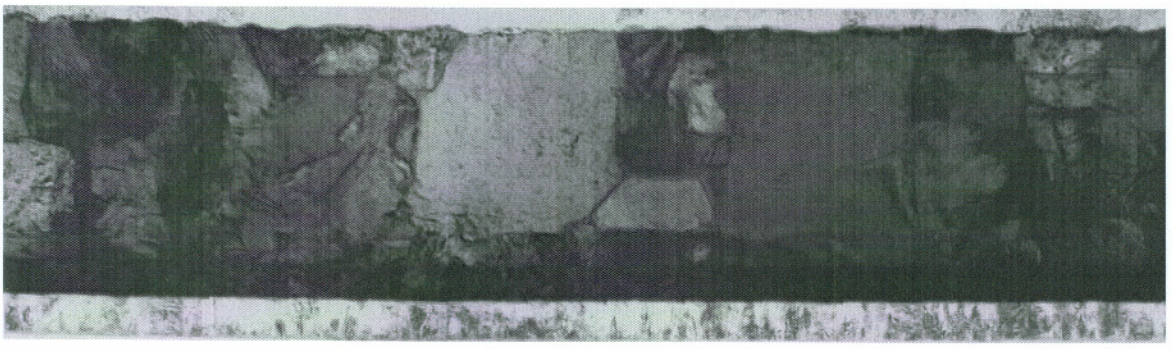


Figure 7.4 AFM topography and cross-sectional profile of the Si_3N_4 passivated evaporated Au/Pt/Ti films. Hillock presence is not observed.



150 nm

(a)



200 nm

(b)

Figure 7.5 Microstructure comparison of as-sputtered and as-evaporated Au film. (a) TEM cross-section of as-sputtered Au film. (b) TEM cross-section of as-evaporated Au film.

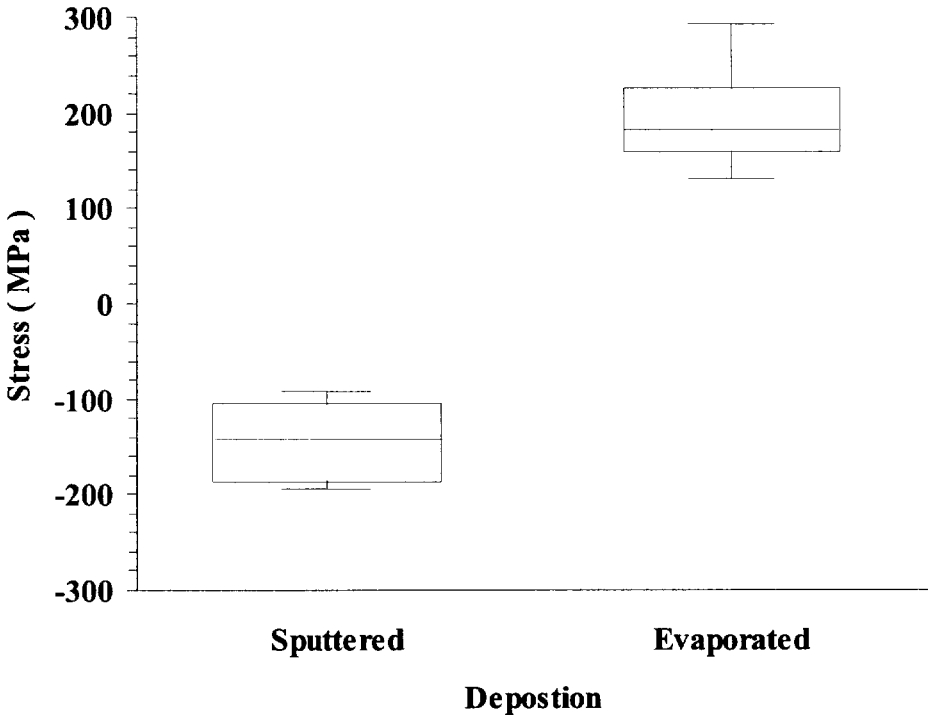


Figure 7.6 Comparison of residual stress within as-sputtered and as-evaporated Au films.

7.2 Hillock Formation Mechanism

The hillocks were initially observed on the dielectric surface. As stated in previous section, so far, most of the hillocks observed in metal films during temperature cycling are formed as a result of compressive stress relaxation. Since Au/Pt/Ti films experience temperature excursion during Si_3N_4 deposition, it is very possible that the compressive stress within the Au/Pt/Ti film induced by the thermal expansion coefficient match between metal and substrate is the driving force for hillock formation. To verify this possibility, the as-sputtered Au/Pt/Ti films were thermal cycled to a series of temperatures up to 400°C and subsequently scanned in AFM to check the hillock presence. The resultant Au topographies and cross-section profiles are presented in Fig. 7.7 and Fig. 7.8 respectively. However, hillocks are not found in these thermal cycled specimens. On the contrary, the Au film surface becomes flatter and flatter with the increase of temperature. Obviously, the hillocks observed in this study are not the general annealing hillocks in unpassivated metal films. Even though compressive stress relaxation within Au/Pt/Ti films does occur at elevated temperatures, the relaxation process does not cause the catastrophic material outgrowth from the metal film. Moreover, the presence of the Si_3N_4 dielectric layer seems to be necessary for the hillock formation.

To prove that the hillocks are not in metal films, the top layer of nitride passivation on a wafer with hillocks was etched away by hot H_3PO_4 solution and the exposed Au surface was examined by AFM. The resultant surface topography is shown in Fig. 7.9, the Au surface is very flat and no hillocks are present in Au/Pt/Ti film.

To gain insight into the hillock formation mechanism, a hillock was located and a TEM cross-section was made at the hillock site. The resultant TEM image is shown in Fig. 7.10. From the picture, the underlying Au film is not exactly conformal with the Si_3N_4 layer, thus the hillock image in Fig.7.2 only represents the topography of the dielectric film. Hillocks formed in metal films observed by other researchers often have features such as [1]: 1. A boundary exists between the hillock and the original surface. 2. The hillock is completely or partially integrated into the original film beneath it.

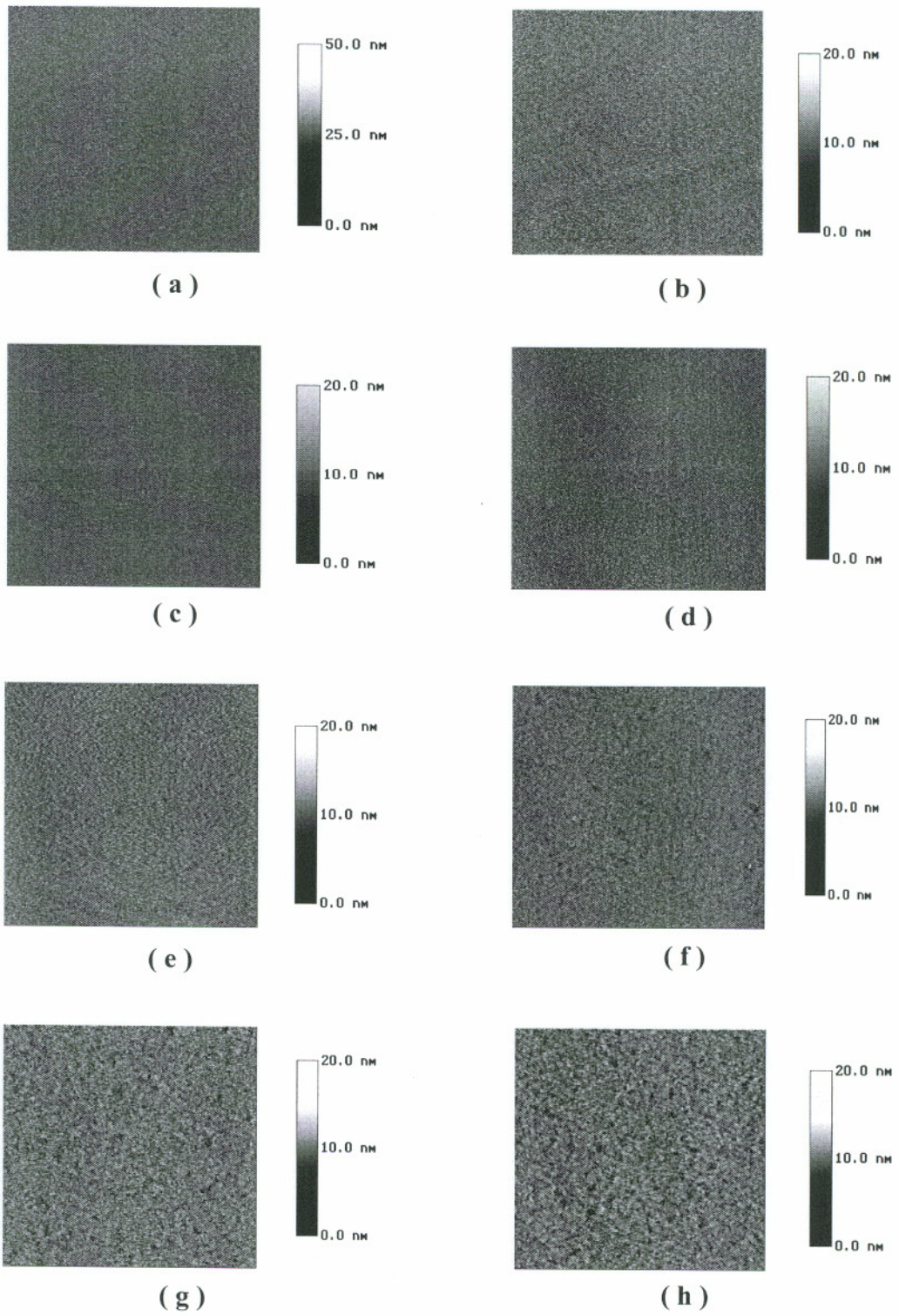


Figure 7.7 **(a) AFM topography of as-sputtered Au/Pt/Ti film surface. (b)-(h) AFM topographies of Au/Pt/Ti film surface after thermal cycling. The maximum temperatures are (a) 75°C, (b) 150°C, (c) 200°C, (d) 250°C, (e) 300°C, (f) 350°C, (h) 400°C respectively. The scan areas are $20\times20\mu$m.**

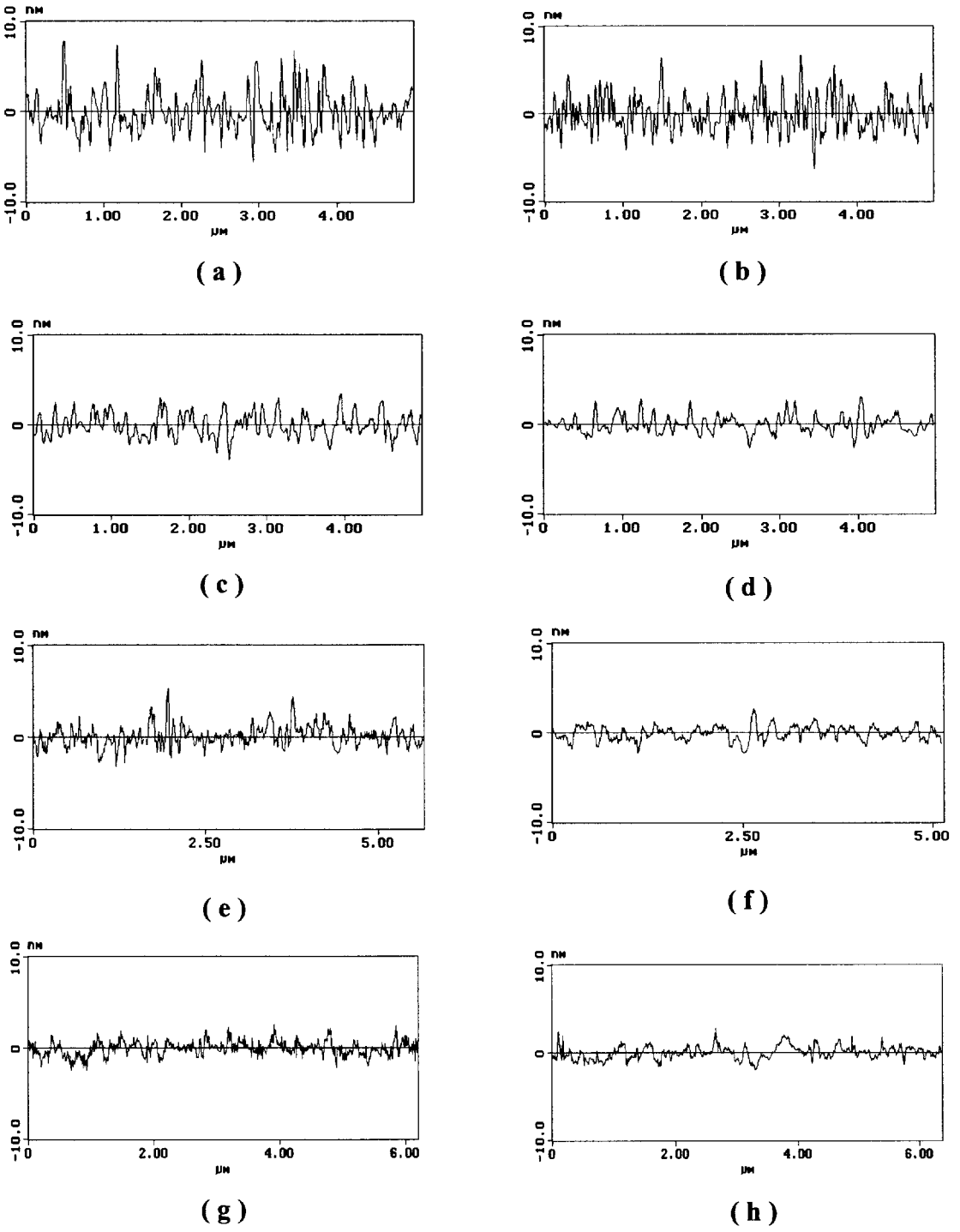


Figure 7.8 (a) AFM cross-section of as-sputtered Au/Pt/Ti film surface. (b)-(h) AFM cross-sections of Au/Pt/Ti film surface after thermal cycling. The maximum temperatures are (a) 75°C, (b) 150°C, (c) 200°C, (d) 250°C, (e) 300°C, (f) 350°C, (h) 400°C respectively.

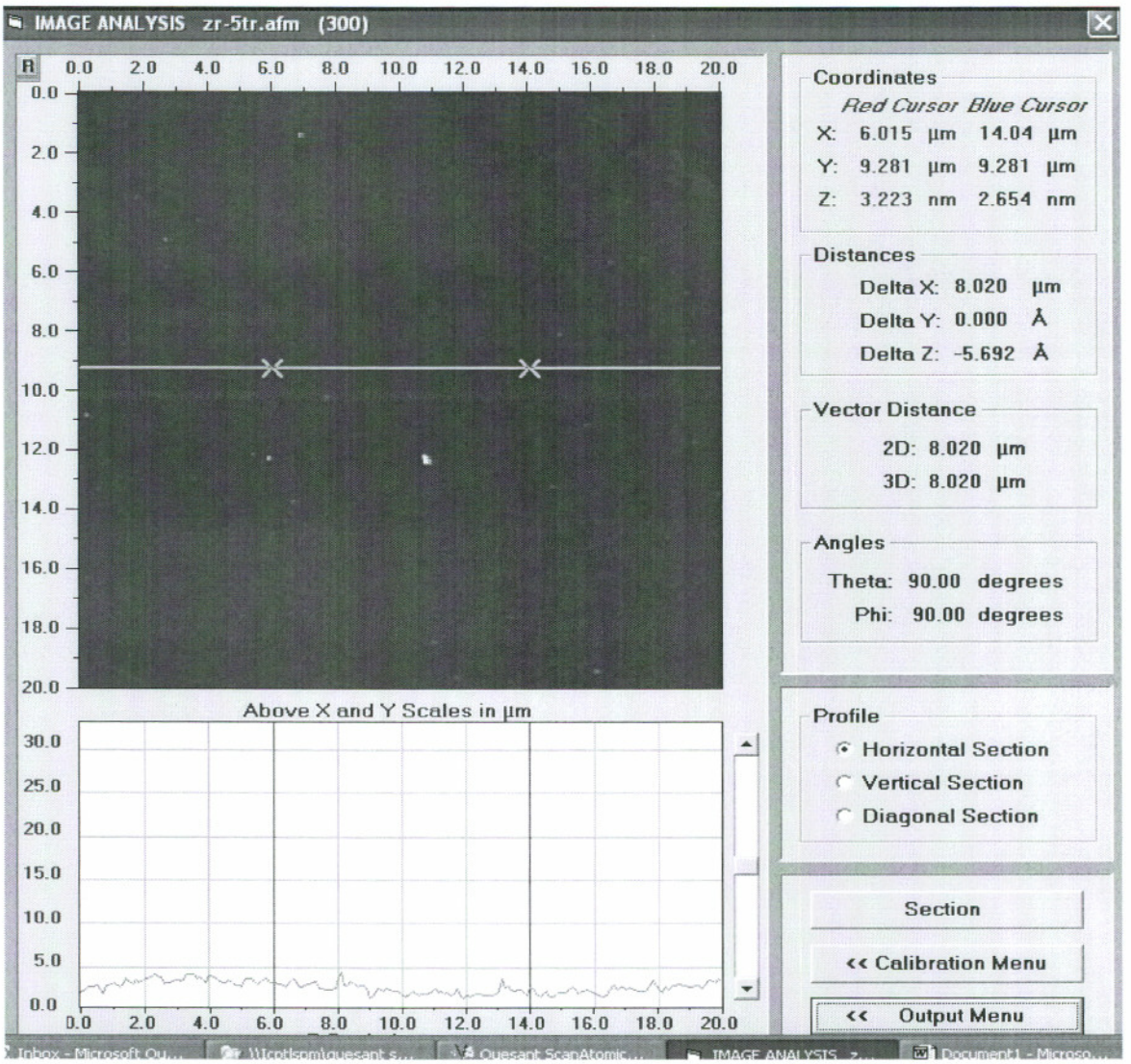


Figure 7.9 AFM image of the exposed Au surface after the top passivation nitride is removed by chemical etch. The vertical scale, lower graph, is in angstroms.

3. Hillock is formed by grain boundary sliding mechanism, in which some grains just slide out of the film. These typical TEM microstructure features of a hillock are not observed in Fig. 7.10. This agrees with the previous AFM examination result that hillocks are not found in the as-sputtered Au film during thermal cycling. The top dielectric film demonstrates a wavy structure with delaminations showing at several sites. The presence of delamination is usually an indicator of possible adhesion problem. The fact that passivation layers generally have limited adhesion to gold metallization [2], plus the wavy structure of the dielectric film, lead us to think that the hillocky topography is probably formed due to the buckling of the Si_3N_4 dielectric film under large compressive stress.

Recalling the PECVD dielectric deposition procedure, the stress within Si_3N_4 film is generated in two stages: 1. During the Si_3N_4 deposition and 2. During the post-deposition cooling process. In the first stage, there are two stress components need to be considered: the growth stress and stress introduced by the relaxation of the underlying Au/Pt/Ti film. No thermal stress supposed to be introduced because the wafers with sputtered metals were preheated for a short time before the deposition, hence no temperature excursion occurs at this stage. The growth stress is hard to measure because the PECVD deposition system does not have the insitu stress measurement capability. However, it can be estimated by film residual stress, which is measured by directly depositing Si_3N_4 onto the substrate and measuring the wafer curvature before and after deposition. The residual stress basically consists of two parts: the growth stress and the thermal mismatch stress induced during cooling. The measurement shows that Si_3N_4 film has a tensile residual stress of 3.5MPa, which is considered to be very small compared to other stress components and will be neglected in the following analysis. Other than the residual stress, a compressive stress component is exerted on the growing Si_3N_4 film due to the shrinkage of the Au/Pt/Ti film during the ongoing stress relaxation. One thing to be noted is that although the wafers are preheated, complete stress relaxation within the metal films is probably impossible since the preheating only takes a few seconds. Also, upon cooling stage, additional compressive stress is generated inside dielectric film due to the difference of thermal expansion coefficient between Au and Si_3N_4. When the

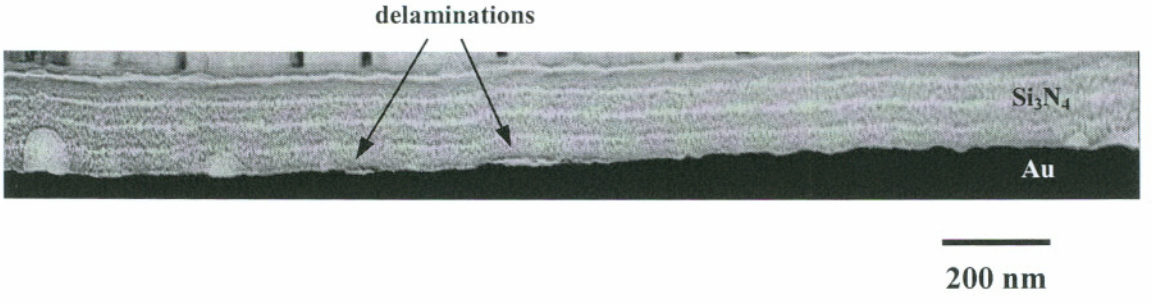


Figure 7.10 TEM cross-section of Si_3N_4 morphology at a hillock site. The underlying Au film is deposited by sputtering. The vertical direction has been extracted for illustration purpose.

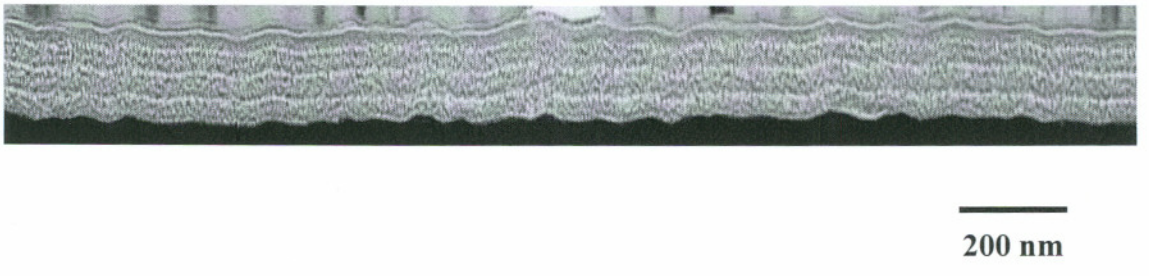


Figure 7.11 TEM cross-section of Si_3N_4 morphology without hillock presence. The underlying Au film is deposited by evaporation. The vertical direction has been extracted for illustration purpose.

compressive stress gets so large, the original flat dielectric film deforms into a wavy configuration. This deformation process strongly depends on the adhesion condition between Si_3N_4 and Au. An excellent bonding certainly increases the film stiffness thus makes it more stable under large compression. It also helps the stress distribute more uniformly in the film so the resultant deformation tends to be uniform too. Since Au has a poor adhesion to Si_3N_4, deformation of Si_3N_4 is relatively easy and delaminations are expected where the bonding is extremely poor. Practically, the stress has a non-uniform distribution due to the factors such as the anisotropy of the film properties and the uneven distribution of adhesion. Therefore some areas will deform more severely than others and produce a protruding a larger delamination and deformation where the stress is the highest.

In the beginning of this chapter, we compared the evaporated and sputtered Au film and found that compressive residual stress exists in the as-sputtered Au film while tensile stress exists in the as-evaporated Au film. We also mentioned that the hillock might be metal protruding from the film surface as a result of compressive residual stress relaxation within sputtered metal films. However, the above experimental results clearly show that the metal film does not have a hillocky topography. Instead, the hillocks are generated in Si_3N_4 under compression. The absence of hillock in passivated evaporated metal film certainly cannot be explained by the difference of residual stresses between sputtered and evaporated films because Si_3N_4 is always under compression no matter what kind of residual stress exists in the underlying metal film. Besides microstructural and residual stress, another significant difference between sputtered and evaporated film is the surface roughness. AFM cross-sections in Fig. 7.12 show that the roughness of the sputtered film, which has the hillock formation problem, is much smaller than that of the evaporated film with same thickness. It is well known that the adhesion strength primarily depends on the film mechanical properties and interfacial geometry. A rough surface provides more bonding area and mechanical anchoring hence enhances adhesion. Consequently, the stress within the Si_3N_4 tends to distribute more uniformly in case of evaporated film and the resultant deformation should be uniform too. The morphology of the Si_3N_4 film with evaporated metal film was examined by TEM cross-section in Fig. 7.11. Clearly, under the uniform deformation induced by the large roughness, the Si_3N_4

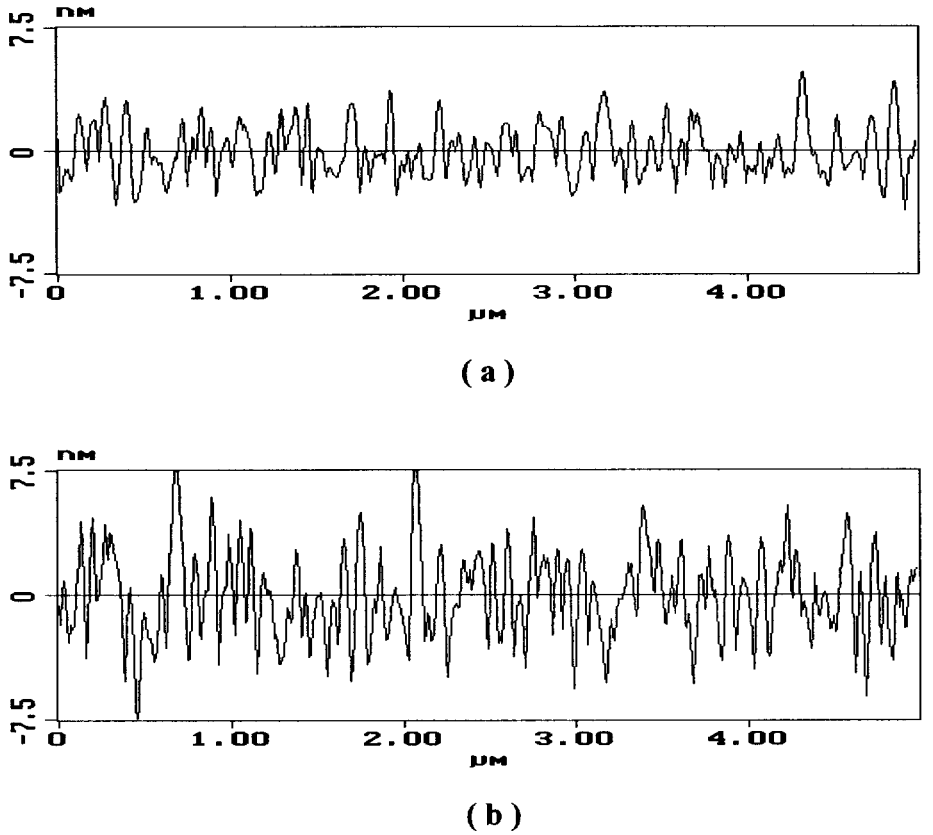


Figure 7.12 AFM cross-section profile of (a) As-sputtered Au film, and (b) As-evaporated Au film.

topography is much more conformal with the underlying Au surface and delamination is not observed. In comparison, despite the presence of hillocks, the Si_3N_4 in Fig. 7.10 is much flatter and delaminations are observed at several sites. This confirms that the roughness is the key factor that determines the hillock formation variation between sputtered and evaporated film. For a film with higher roughness, the mechanical locking and increased bonding area improve the adhesion of the film, hence suppress hillock formation.

The hillock formation dependency on Au film roughness can also be demonstrated by varying the sputtered Au thickness. Fig. 7.13 shows the AFM topographies and cross-sections of the Si_3N_4 passivated Au/Pt/Ti film with various Au film thickness. As illustrated, hillocks are not observed when the Au thickness is greater than 2000Å. Before the Si_3N_4 deposition, the as-sputtered films have been examined in AFM and the corresponding cross-sectional profiles are shown in Fig. 7.14. Obviously, the roughness of the as-sputtered Au film increases with the Au film thickness. Likewise, a thicker film that possesses larger surface roughness provides much stronger bonding between Au and Si_3N_4. Stress tends to distribute uniformly within Si_3N_4 film, as well as deformation, which gives less opportunity for hillock nucleation. In the case of a thinner Au film, relatively poor adhesion leads to intensified stress at certain areas and causes hillock to grow as a result of local severe dielectric deformation.

In summary, the hillock formation is a result of the nonuniform deformation of the Si_3N_4 under compression. It does not have a direct relationship with the switching of metal deposition from evaporation to sputtering. The primary factors affecting the hillock formation include metal film surface roughness, and the adhesion between metal and dielectric film.

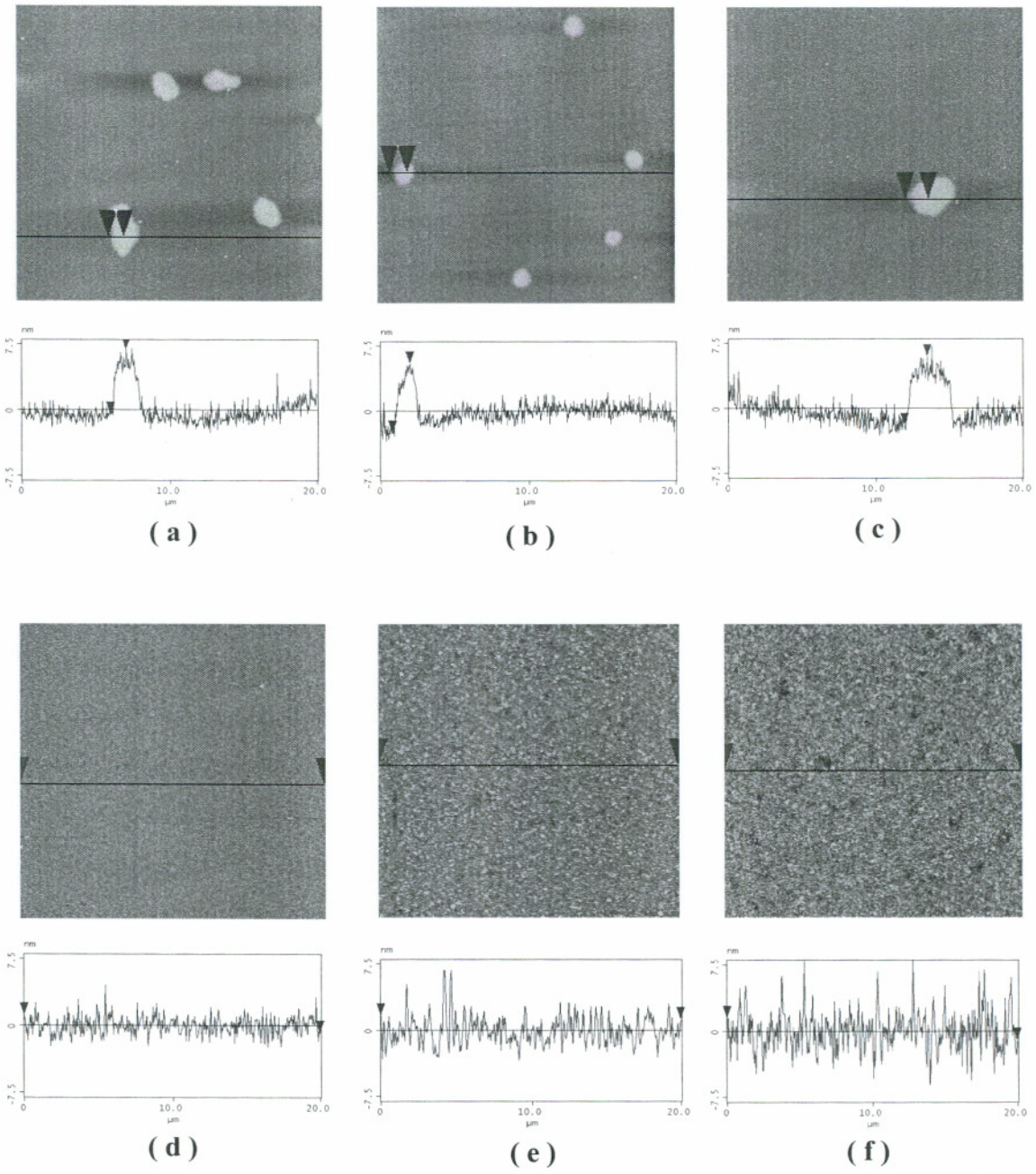


Figure 7.13 AFM topographies and cross-sections of the Si_3N_4 passivated sputtered Au/Pt/Ti film with various Au thickness, showing the hillock formation dependency on Au thickness. The Au film thicknesses are (a) 200Å, (b) 600Å, (c) 1000Å, (d) 2000Å, (e) 4000Å, (f) 6000Å, respectively

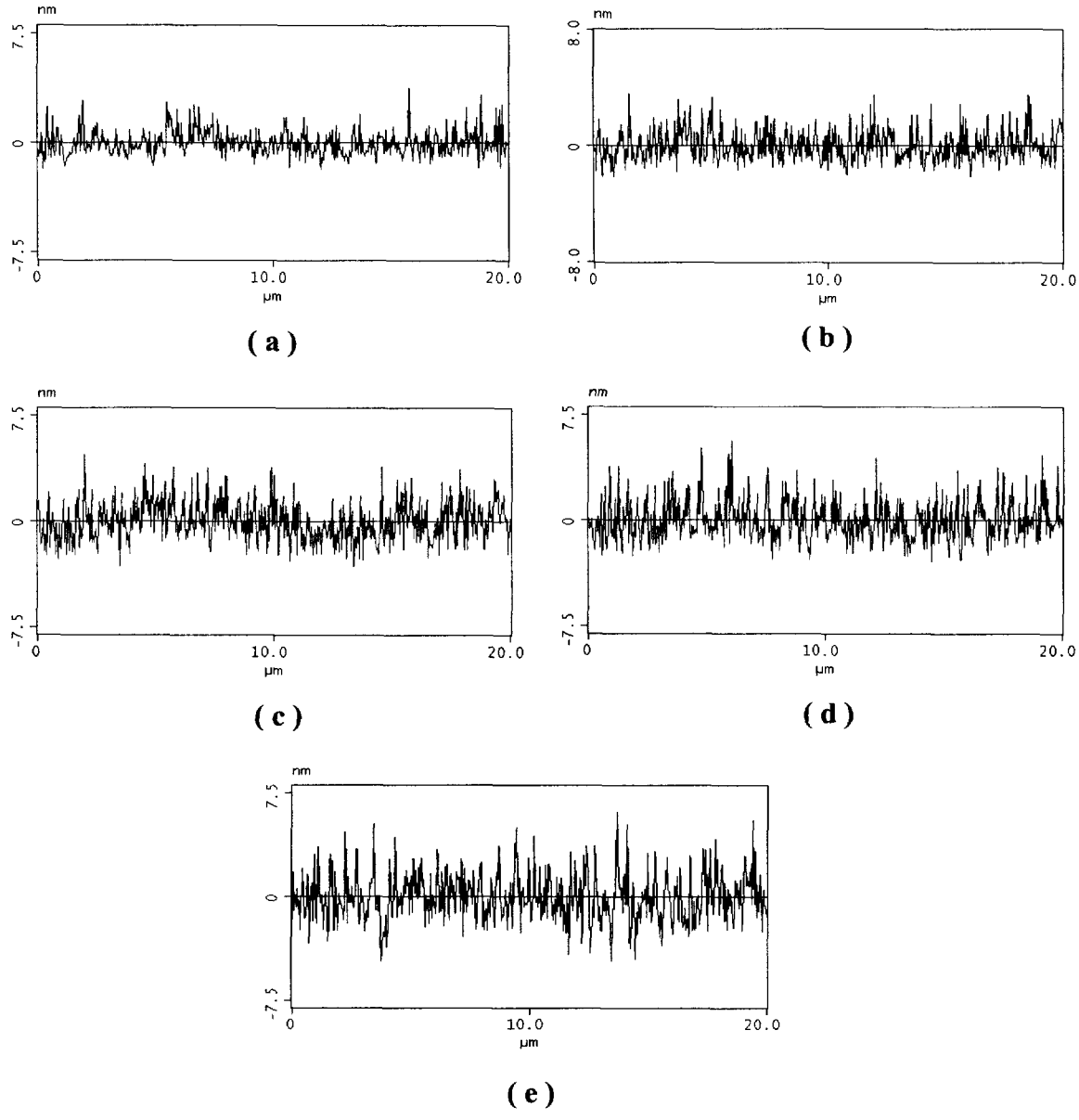


Figure 7.14 AFM cross-sections of as-sputtered Au/Pt/Ti film with various Au thickness, showing the surface roughness of Au film increases with Au thickness. The thicknesses of Au film are (a) 200Å, (b) 1000Å, (c) 2000Å, (d) 4000Å, (e) 6000Å, respectively.

7.3 The Effect of Hillock Formation on MIM Capacitor's Electrical Performance

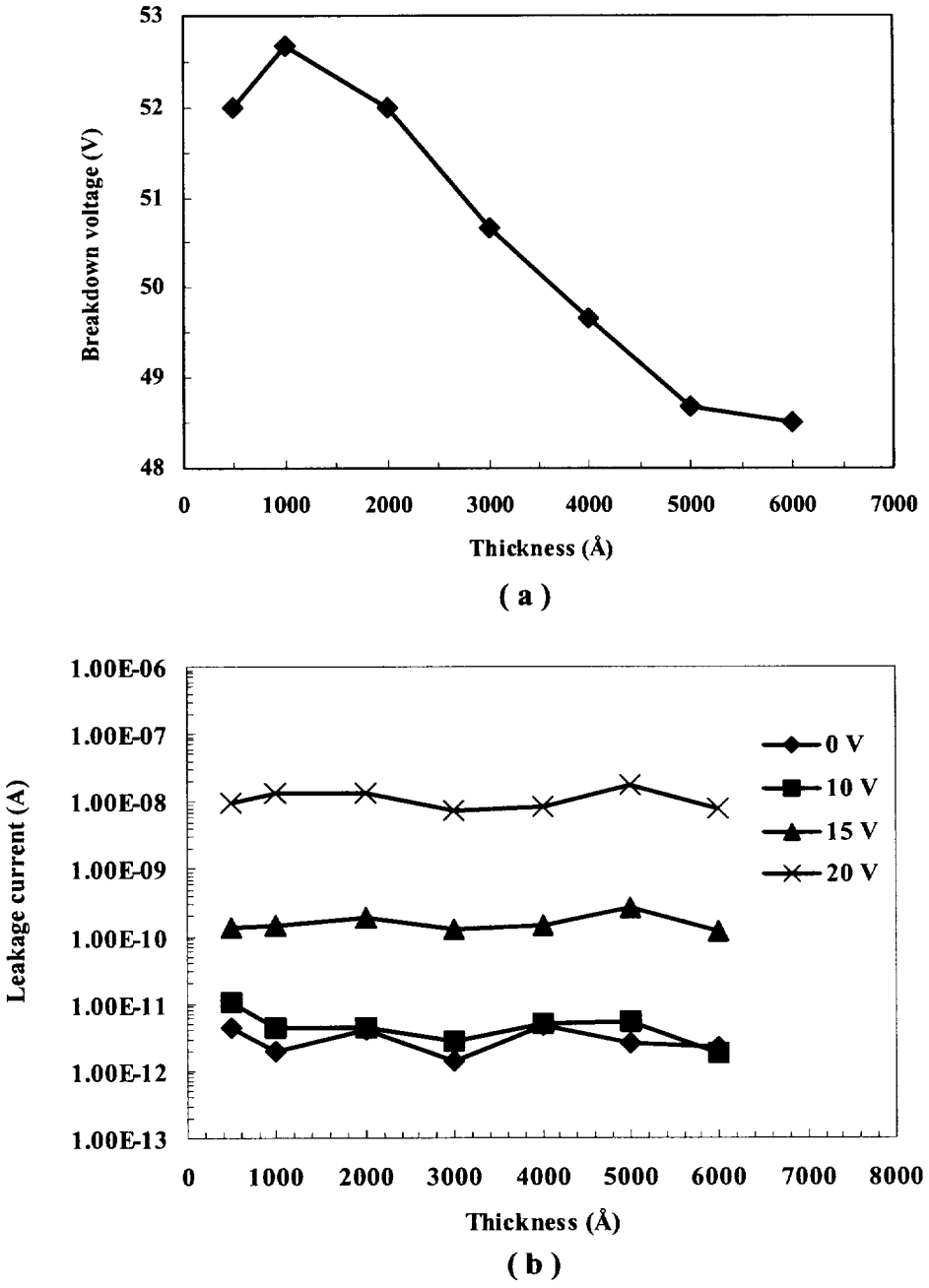
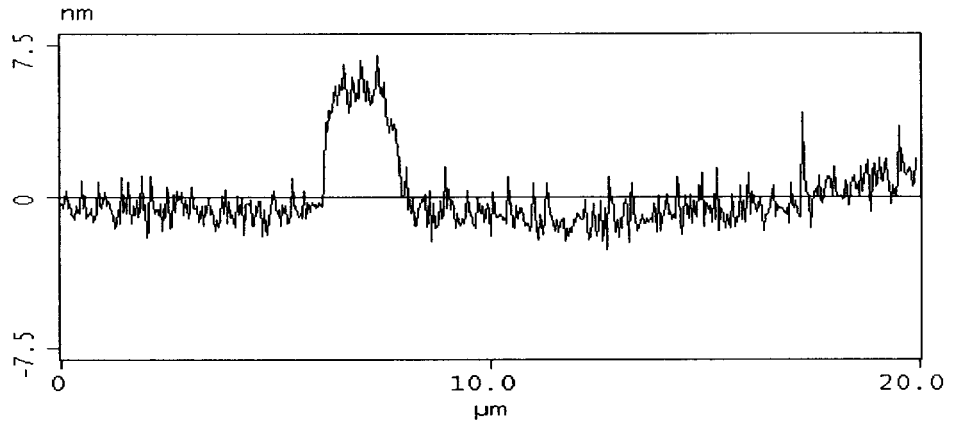


Figure 7.15 The effects of Au film thickness on MIM capacitor's electrical performance. (a) Breakdown voltage, (b) Leakage current.

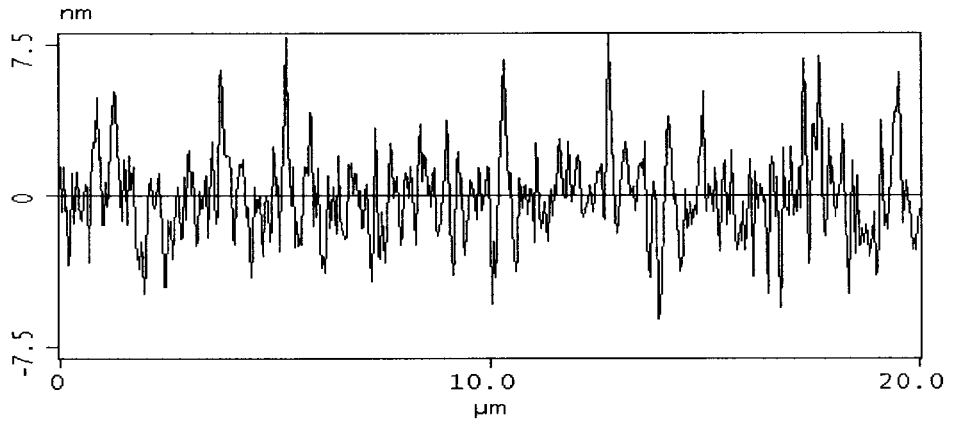
The electrical performance and reliability of the MIM capacitor greatly depends on the dielectric film structure and properties. Theoretically, a flat, conformal dielectric film without hillock formation is preferred because hillocks may produce local extremely high electric fields that lead to the dielectric breakdown at lower voltages than expected. From this point of view, a thicker metal film should be considered as the bottom electrode since it suppresses the hillock formation. On the other side, the thinner film also has its advantage considering that the roughness of a thinner Au film is much less than that of a thicker one. AFM roughness analysis shows that the measured RMS increases from 0.338nm to 1.784nm when Au film thickness increases from 200Å to 6000Å. It is hard to achieve a flat, conformal dielectric film when the underlying Au surface on which the dielectric will be deposited is very rough. Both the hillock and the Au roughness affect the MIM's performance and it is yet unknown which factor plays a more important role.

To evaluate the effect of hillock as well as the surface roughness on MIM capacitor's electrical property, a series of capacitors were fabricated with the bottom Au film thickness ranging from 200Å to 6000Å. The capacitor's breakdown voltage and leakage current were measured and plotted versus Au film thickness in Fig. 7.15. It shows that the breakdown voltage decreases up to 10% when the thickness increases from 200Å to 6000Å, while no obvious trend is observed for leakage currents. The decrease of the breakdown voltage with increase of thickness indicates that the Au roughness has a more critical effect on dielectric property. Fig. 7.16 compares the cross-section profiles of the Si_3N_4 films with the underlying Au thicknesses being 200Å and 6000Å respectively. With a thicker Au film in Fig. 7.16(a), the dielectric surface is composed of evenly distributed large and wide peaks with peak-valley distance about 60-80Å. Even though hillocks are absent in this case, the height of these large peaks is about same as that of the hillocks. Essentially, these large peaks can be considered as hillocks only with smaller lateral dimensions, thus they deteriorate the dielectric property the same way as the hillock does. Conversely, when a thinner Au film is used in Fig. 7.16(b), in spite of the presence of few hillocks at some area, the rest of the dielectric surface is very smooth. Overall, the dielectric film is much flatter and more conformal when a

thinner Au film is employed. Therefore, it is not very surprising that the breakdown voltage decreases with the increase of bottom Au thickness.



(a)



(b)

Figure 7.16 Comparison of the Si_3N_4 surface profiles with thin and thick Au films. (a) Au thickness is 200Å. (b) Au thickness is 6000Å.

References

[1] F. Ericson, N. Kristensen, and J-Å Schweitz, "Atransmission electron microscopy study of hillocks in thin aluminum films," J. Vac. Sci Technol. B, **9 (1),** 1991, pp.58-63.

[2] G.L. Schnable, R.B. Comizzoli, W. Kern, and L.K. White, "A survey of corrosion failure mechanisms in microelectronic devices," RCA Review, **40**, 1979, pp.416-445.

8 Summary and Conclusion

Thin film metallization always plays an important role in the development of microelectronic industry. In the past several decades, the advance of the integrated circuits greatly depended on the continuous improvement of metallization materials and processing methods. With the capability to fabricating extremely fast devices, the metallization has become a critical factor that limits the speed and reliability of the microelectronic chip, which still tends to be true in the future. This study investigates the materials properties of the newly developed sputtered Au/Pt/Ti thin film metallization scheme for GaAs integrated circuits. Generally Au/Pt/Ti film was deposited by the traditional evaporation, which is a process suitable for small volume production while cannot meet the demand of today's fast growing electronic market. Recently sputtering has been particularly designed to deposit low sidewall coverage Au/Pt/Ti film that suits the specific lift-off process used for GaAs IC patterning. The new process demonstrates a superior manufacturing yield and throughput compared to evaporation. The purpose of this thesis is two fold: 1. Characterize the evaporated and sputtered Au/Pt/Ti thin film including microstructure, stress and resistivity. 2. Study the hillock formation mechanisms in the silicon nitride passivated Au/Pt/Ti film and their correlations with microstructure and stress.

FIB produced TEM cross-sections have been extensively employed in this study to examine the microstructural features of the sputtered Au films. It was shown that the grain size, defect density varies significantly as the film growth proceeds. The early stage Au film consists of small and clear columnar grains with only a few dislocations. As the thickness increases, the density of dislocations and interstitial clusters increases dramatically as a result of the cumulative effect of energetic particle bombardment. In

addition, grain growth was also observed and probably occurs through the recystallization process, which is induced by the particle bombardment and its associated heat generation. The residual stress of the sputtered Au film was measured by substrate curvature method using Tencor FLX2320. The stress was found to transit from tensile to compressive as the film grows. This thickness dependence of stress was eventually attributed to the microstructure evolution. Grain boundary relaxation model proposed by Hoffman was applied to explain the initial tensile stress present in film below 2000Å. The gradual reduction of the tensile stress and the eventual transition to the compressive stress is a direct result of the energetic particles bombardment, which creates high number density of interstitial clusters and dislocations which cause compressive stress in the lattice. In addition to this main mechanism, grain growth also contributes to the tensile stress reduction. The resistivity of the sputtered Au was evaluated using a four-point probe at various film thicknesses. It was found that the resistivity decreases from 3.848$\mu\Omega$.cm to 2.388$\mu\Omega$.cm as the film thickness increases from 0.02μm to 0.6μm. 71% of the total reduction occurred when thickness is increased from 0.02μm to 0.1μm. Beyond 0.1um, the resistivity decreases gradually with the increase of film thickness. Such resistivity-thickness behavior is expected and mainly controlled by the electron scattering at film free surface and interface. For a film at a constant thickness, post-deposition annealing was found to be able to effectively lower the film resistivity up to 15%. This has been attributed to the reduced defect density and the re-orientation of the dislocations which scatter the conduction electrons. Most of the original dislocations are perpendicular or inclined to the substrate, while after anneal, they are aligned parallel to the substrate and has a much smaller resistance to the current flow.

The thermal-mechanical behavior of the individual Au, Pt, Ti films as well as their multilevel structures including Pt/Ti and Au/Pt/Ti were studied by thermal cycling the film/SiO_2/Si wafers inside Tencor FLX2320 and simultaneously measuring the film stress. By comparing the resultant stress-temperature curves, it is found that the stress relaxation of the Au/Pt/Ti composite structure at low temperature range (<300°C) is governed by the relaxation of all three metal films (Au, Pt, Ti), whereas the relaxation at high temperature (300-450°C) is dominated by the relaxation of Au film due to the lacking of coupled surface and grain boundary diffusion in Pt and Ti film. Only the

relaxation mechanisms of Au film were investigated since Au is the major contact metal and always plays an important role in the relaxation of the Au/Pt/Ti multilevel scheme. Small sections cut from a wafer deposited with blanket Au film were heated in DSC and quenched at specific temperatures (75°C, 150°C, 200°C, 250°C, 300°C, 350°C, 400°C). TEM cross-sections were then produced to examine the microstructures of Au film at elevated temperatures. The observations show that the relaxation of the compressive stress at intermediate temperatures (70°C-200°C) is controlled by thermally assisted dislocation glide. The relaxation is hindered when dislocations pile up against grain boundaries around 150°C-167°C. Further relaxation is enabled when a significant number of dislocations are absorbed at grain boundaries. At higher temperatures (>200°C), stress-driven grain boundary diffusion coupled with surface diffusion dominates the relaxation process. Grain growth has a minor contribution to the relaxation process. Insitu TEM thermal experiment was carried out to observe the microstructural evolution in real time. However, because the stress within the thin TEM foil is much smaller than that within the bulk film, the dislocation motion and the grain growth that are observed in the quenched specimen were not observed in the insitu heating. In future studies, a planar specimen can be used instead of a cross-section specimen to perform the insitu TEM heating since the planar specimen has inplane biaxial stress which is closer to the stress conditions within the bulk film. It is critical during ion milling specimen preparation that a cooling stage should be used, otherwise the heat generated during the milling will anneal out large numbers of defects that originally exist in the as-deposited film.

The mechanisms of nanoscale hillock formation in silicon nitride passivated sputtered Au/Pt/Ti film is the emphasis of this research since the hillocks significantly affect the MIM capacitor's electrical performance. The surface morphology and cross-section of films with and without hillock were characterized using AFM and TEM respectively. The top passivation nitride was removed by chemical etch and exposed metal surface was examined by AFM. The results show that the underlying Au surface is very flat and no hillocks are present. This indicates that hillocks are not metal protrusions and the hillocky topography is contributed by the top nitride film. TEM cross-sections show that under compression the silicon nitride film is deformed into a wavy structure with and without hillocks. The dielectric film is more conformal with the underlying Au

film in specimens in which hillocks do not exist. However, disregarding the presence of the hillock, the dielectric film of the hillocky specimen is less wavy than the specimen without hillocks, which also agrees with the AFM observation. Delaminations between silicon nitride and Au were observed at several locations in the hillock cross-section. Based on these observations, it is proposed that the hillock forms as the silicon nitride is locally deformed by compressive stress, which includes the stress imposed by the relaxation of the underlying Au film at elevated temperatures and the thermal mismatch stress introduced upon cooling. The primary factors affecting the hillock formation include the as-deposited metal film surface roughness, and the adhesion condition between metal and dielectric.

The Au film thickness dependence of the hillock formation is explained by the film surface roughness variation. The surface roughness of the as-sputtered Au film increases with the film thickness, therefore the surface of a thinner film is significantly flatter than that of a thicker film, which will leads to a relatively poor interface adhesion between silicon nitride and the thinner Au film. Consequently, when subjected to a large compressive stress, the deformation of the dielectric will not be uniform because of the weak bonding force at interface. Instead it is more easily to be peeled off at certain locations to relieve the majority of the stress, while leaving the rest area almost unaffected. This explains that in a passivated thinner Au film, although hillocks are present, the general roughness of the silicon nitride remains very small. In comparison, for a thicker Au film with a much rougher surface, the silicon nitride only becomes much wavier under compression due to the uniform deformation.

It is obviously that the thickness of the Au film is a very important parameter since it not only determines the contact resistance, but also affects the interface structure and the dielectric morphology. Its effect on dielectric performance has been evaluated by testing the MIM capacitor's leakage current and breakdown voltage. The measurements show that the breakdown voltage decreases with increasing Au thickness, while no strong dependence of leakage current on thickness is observed. The trend of the breakdown voltage is not very surprising because overall the dielectric film is much flatter and more conformal when a thinner Au film is employed, hence the chances of breakdown is reduced.

This study gives a detailed investigation focusing on the properties of the sputtered Au/Pt/Ti thin film deposited at one set of processing parameters. More study should be carried out in the future to explore the effect of sputtering parameters on film properties. Such deposition parameters should include ion bombardment energy, gas pressure, target to substrate distance, substrate bias, substrate temperature and so on. The process should be eventually optimized to achieve high directionality(to facilitate liftoff), minimum film resistance, lower residual stress and smooth surface.

Developing low temperature PECVD (Plasma Enhanced Chemical Vapor Deposition) is another very promising project since this will eliminate a lot of problems associated with thermal effects, such as thermal stress development, stress relaxation, and degradation of film properties at high temperature. It is especially beneficial to this study since the dielectric quality will be dramatically improved without the deformation of the dielectric under temperature-induced stress.

Vita

The author, Zhenkun Ren, was born in Taiyuan, Shanxi Province, China, in April 1976. She enrolled in Beijing University of Aeronautics and Astronautics in 1995 and received her B.S. degree in Materials Science & Engineering in 1999. Then she came to US and enrolled in graduate school at Washington University. After studied in Materials Science for one year, she transferred to Oregon Graduate Institute of Science & Technology in 2000 and received a M.S. degree in Electrical Engineering in June 2001. She continued her Ph.D. study at OGI School of Science & Engineering at Oregon Health & Science University (OGI merged with OHSU in 2001) and received her Ph.D. degree in Electrical Engineering in October 2004. Her research focuses on thin film metallization for GaAs ICs.