Optimization and Temperature Dependence of Current Gain in Polysilicon-Emitter-Contacted Bipolar Transistors

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To My Husband

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Table of Contents

List of Tables and Figures

ABSTRACT

Optimization and Temperature Dependence of Current Gain
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Presented herein are the results of an experimental and theoretical investigation of the factors influencing the current gain of a polysilicon-emitter-contacted bipolar transistor (PEC transistor). Specifically, the temperature behavior of gain and its optimization are comprehensively discussed. The results show that the PEC transistor exhibits a stronger temperature dependence, when compared with conventional transistors. This is attributed to the diffusion length of minority carriers (holes) in the polysilicon. The current gain, hfe for a common emitter configuration at low frequencies has been extensively modeled. The analysis reveals that the mobility and the recombination lifetime of the minority carriers in the polysilicon are the key parameters for optimizing hfe in PEC transistors.

Electrical measurements were carried out on PEC transistors, with no intentional oxide layer between the polysilicon contact and the monosilicon emitter, over a temperature range from 25°C to 165°C.

This data was analyzed by assuming that the increase in current gain is due only to the decelerated transport of the minority carriers in the polysilicon contact. With this assumption a two region model is used to derive a general equation for hfe, from which the temperature dependence and the properties for optimizing current gain were examined.

It is shown that the increased temperature dependence in PEC transistors over conventional transistors can be accounted for by the temperature dependence of the hole diffusion length in the n+ polysilicon. Examination of the polysilicon dependent term of hfe uncovered the minority carrier, mobility and recombination lifetime as the parameters responsible for enhanced current gain.

CHAPTER 1

Introduction

Since the invention of the silicon bipolar junction transistor (BJT) in 1948 it has dominated the Integrated Circuit (IC) market. The metal-oxide-semiconductor field-effect transistor (MOSFET) began to take a share of that market with the advent of the silicon planar process and the technology to produce a well behaved silicon-dioxide silicon interface. The MOSFET is now the most important device for very-large-scale integrated (VLSI) circuits such as microprocessors and semiconductor memories. This is because it is especially adaptable to high density and low power consumption.

However, the BJT has continued to be used in applications where high gains are necessary and for high speed applications. Since the early 1970's, bipolar technology has shown steady progress toward the realization of VLSI. Dramatic improvements in packing density and performance have been achieved primarily through evolutionary and in some cases revolutionary changes in lithographic systems and generic process techniques. One of these revolutionary changes was the replacement of the usual metal contact to the heavily doped emitter with a doped polycrystalline silicon.

The use of the polysilicon-emitter-contacts results in several improvements; higher dc current gain, higher densities (because of reduction in collector-base overlap area), self aligned gates, better emitter-base breakdown characteristics, and faster switching speeds.

This thesis is focused on an experimental and theoretical study of some of the properties of the polysilicon-emitter-contacted bipolar transistor. Specifically, the temperature dependence and the optimization of the current gain are systematically examined and characterized.

CHAPTER 2

Previous Work

2.1. Device Type

A number of different techniques can be employed to fabricate a polysilicon-emitter-contacted bipolar transistor (PEC transistor) [1-4]. Naturally, the fabrication processing determines the characteristics of the device. The most significant process steps are the surface treatment given to the wafer prior to the polysilicon deposit, the dopant concentration of the polysilicon (the polysilicon may be doped when deposited or subsequently doped by diffusion or ion implantation), and the annealing time and temperature.

Recent transmission electron microscopy (TEM) studies reveal that these different processing steps produce a different interfacial layer between the polysilicon contact and the monosilicon emitter [3-5]. It was found that if the wafer had an RCA clean prior to the polysilicon deposit, a surface layer of oxide approximately 15 angstroms thick was formed [4]. This oxide layer was not broken up by normal pre or post annealing. If the wafer was given a dip in buffered hydrofluoric acid (HF) prior to the polysilicon deposit, a thin layer of oxide approximately

4 angstroms thick forms, which breaks up easily at annealing temperatures of 900 °C. Thus, the PEC transistors can be separated into two types of devices. Those with an oxide layer between the polysilicon contact and the monosilicon emitter and those with no interfacial layer. Normally a device fabricated using an RCA clean has an oxide layer, unless annealing temperatures greater than 1000 °C are used. Those fabricated using an HF treatment have a broken up oxide layer which, electrically speaking, means no interfacial layer. The HF treatment can produce a device with a thin continuous oxide layer [3], but this is the exception, not the rule. The transistors measured in this work can be classified as having no oxide layer. Therefore aside from some brief comments, the main content of this paper will be focused on transistors with no oxide layer.

2.2. Experimental

Various different properties of the PEC transistors have been reported in a number of papers, but only a few have data on current gain vs temperature. Graul et al. in 1976 [6], Graaf et al. in 1979 [7], and Van Halen et al. in 1985 [8] have all published temperature data for transistors with a thin oxide layer between the monosilicon and polysilicon. These devices have a different temperature dependence than those with no oxide layer [9].

Ning et al. [1] in 1980 reported on the temperature dependence in devices with no oxide layer. Later, beginning in 1981, Soerwirdjo and Ashburn [9-11] published a series of papers with data for both types of devices. The experimental data show that, for a transistor with no oxide layer, that the current gain increases with the temperature. The exact values of the gain are difficult to compare because these papers record the measurements on a low resolution exponential graph. Nevertheless, the data appears to have the same temperature relationship. It should be noted that Ning et al. deposited a doped polysilicon and Ashburn and Soerwirdjo implanted the polysilicon after it was deposited. The difference in these devices lies in the presence of a peak in the arsenic concentration at the polysilicon-monosilicon interface, due to gettering during drive-in for the implanted device. Ning's measurements have a lower overall gain than those used by Ashburn and Soerwirdjo. Both show a stronger temperature dependence for the PEC transistor than for the conventional transistor, which agrees with measurements made in this work.

2.3. Theory

Current gain improvements for the PEC transistor over conventional transistors by a factor from 3 to 30 have been reported by several authors [1, 4, 10, 12]. Various models have been proposed to explain this

increase. In all models the gain increase is attributed to the reduction of the base current while the collector current remains constant. The base current consists mainly of minority carriers injected into the emitter from the base region. Two major theories have emerged to explain the slowdown in the minority carrier, viz. tunneling through an interfacial oxide layer (tunnel emitter model) [7] and decelerated transport in heavily doped polysilicon region (two-region model) [1]. The two region model can explain an improvement in gain by a factor of 3. The much larger gain improvements are attributed to tunneling and explained by the tunnel emitter model.

Yu et al. [2] describes the transport of the minority carriers through the polysilicon region by a box analysis. The first box is the grain. By applying the diffusion equation the current at the end of each grain is expressed as a continuous function of the excess minority carrier concentrations in the grain. The second box is the grain boundary where the current is expressed as a linear function of the carrier concentration with the slope defined as qD_{gb}/δ. Here D_{gb} is the diffusion constant of amorphous silicon and δ is the grain boundary width. At this point Yu rewrites these equations in terms of the surface recombination velocity for each layer and combines them using a tridiagonal system of 2N-1 linear equations. By doing this he obtains an equation that defines an

effective recombination velocity to characterize the effect of the polysilicon layer on the behavior of the injected minority carriers in the emitter. Unfortunately, by doing this the temperature dependent terms are absorbed into the fictitious velocity and can no longer be isolated.

Ning et al. [1] uses a simplified box analysis by making the polysilicon layer a black box with an average mobility, diffusion constant, and diffusion length. These average values are the result of the changes in these parameters as the minority carrier moves through the grains and the grain boundaries. This two region model assumes that the base current can be attributed entirely to the diffusion of holes across the emitter and the polysilicon contact which must be a continuous function of the minority carrier concentration. The theoretical analysis of the experimental data quoted in section 2.2 use this model. From this model the small increase in the temperature coefficient of the gain compared to a conventional transistor is accounted for by the temperature dependence of the diffusion length [10]. Ashburn et al. [9] later added a second temperature dependent term, namely the minority carrier mobility of polysilicon. Experimental measurements of the temperature dependence of the minority carrier mobility of polysilicon shows no temperature dependence [13].

These authors [1,9,10] begin with a standard temperature dependent equation for conventional devices [6,14-16].

$$hfe = constant\ \exp(-\Delta E/kT) \tag{2.1}$$

This equation assumes the exponential behavior of the temperature dependence, theoretically masking out any other temperature terms which are then absorbed into the constant [14]. If that assumption were valid, the diffusion length term which has only a square root of temperature dependence would also be masked out, making theoretically the temperature dependence for both the conventional transistor and the PEC transistor identical.

CHAPTER 3

Present Work

3.1. Fabrication and Device

The samples measured in this experiment were fabricated on a 40-100 ohm cm, 3 inch p-(111) silicon wafer. The base region was implanted with 40 keV $25As^+$ with a dose of 4 x $10^{15}cm^{-3}$ to form the initial emitter region. Polysilicon was deposited, after cleaning and a dip in hydrofluoric (HF) acid. The polysilicon was implanted with 150 keV $75As^+$ with a dose of 2 x $10^{15}cm^{-3}$ and annealed at 900°C for 30 minutes. A more detailed description of the fabrication of this device has been published elsewhere [17].

TABLE 3.1

Device Parameters	
w_E	1400Å
w_B	1800Å
w_{poly}	2500Å
A_E	$.5\ x\ 4\mu m^2$
N_D(emitter surface)	$10^{20}cm^{-3}$
N_A(base)	$3x10^{17}cm^{-3}$

The resulting polysilicon-monosilicon interface is a layer of discontinuous oxide with fingers of monosilicon growing into the polysilicon region [3,4]. The doping profile should show a small increase in the arsenic concentration at this interface [3]. The device parameters are listed in Table 3.1.

3.2. Experimental Results

Current Gain vs Temperature measurements were made over a temperature range from 25°C to 165°C at 20°C intervals. At each temperature base current, collector current, and hfe were recorded as V_{be} was varied from 0.2 V to 1.2 V in increments of 0.05 V. Plots of V_{be} vs I_C and I_B were made to show that current gain remained constant over at least three decades of current for each transistor[18,19]. Figure 3.1 is an example of the curves obtained. The relationship between temperature and current gain is shown in figure 3.2. A npn transistor with no polysilicon layer is normally assumed to have an exponential temperature dependence as discussed. The exponent is proportional to the bandgap narrowing of the heavily doped emitter (ΔE). If this data were to fit a similar equation ΔE, the bandgap difference, must be very small.

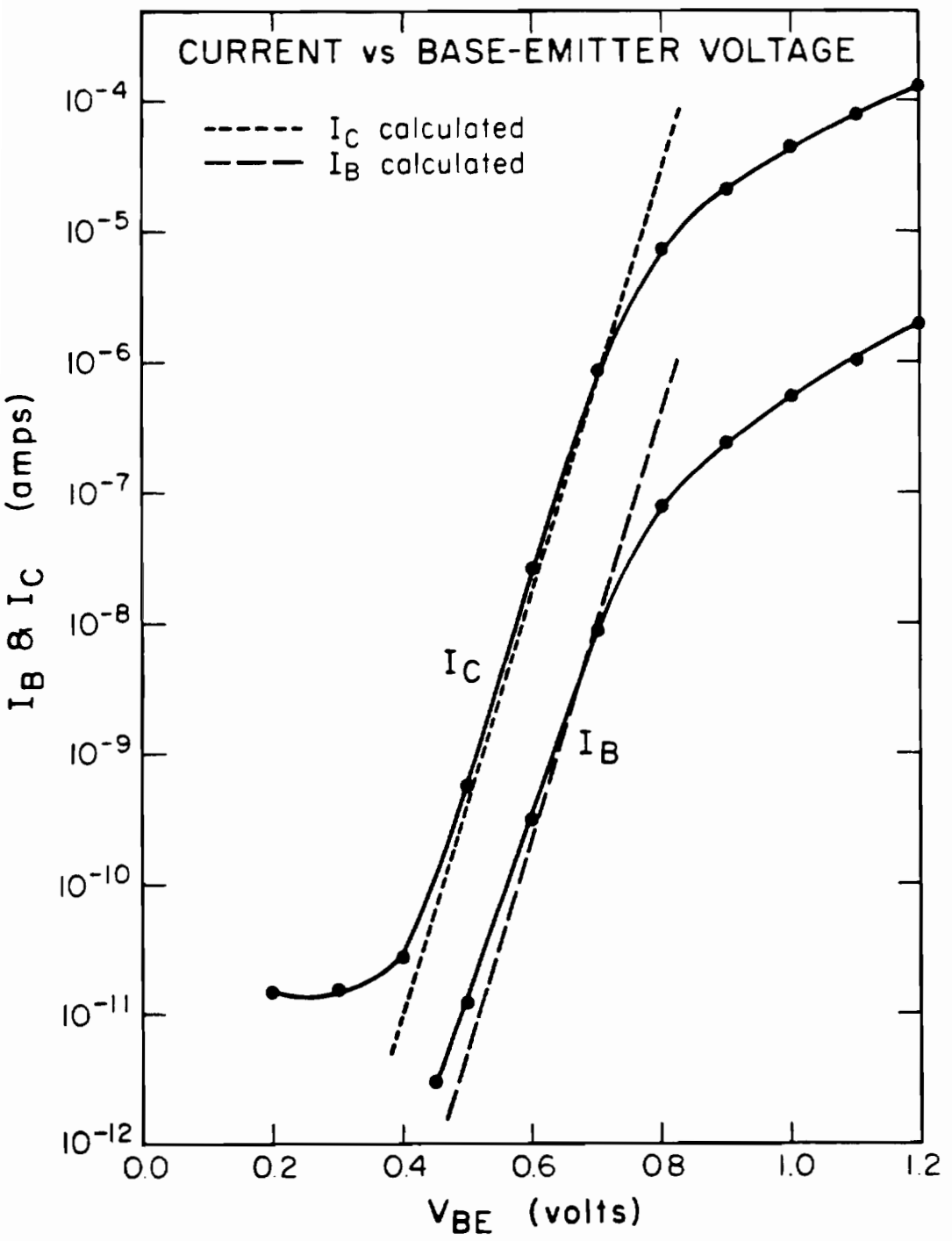

Figure 3.1. Current-voltage characteristics for polysilicon-emitter-contacted bipolar transistors.

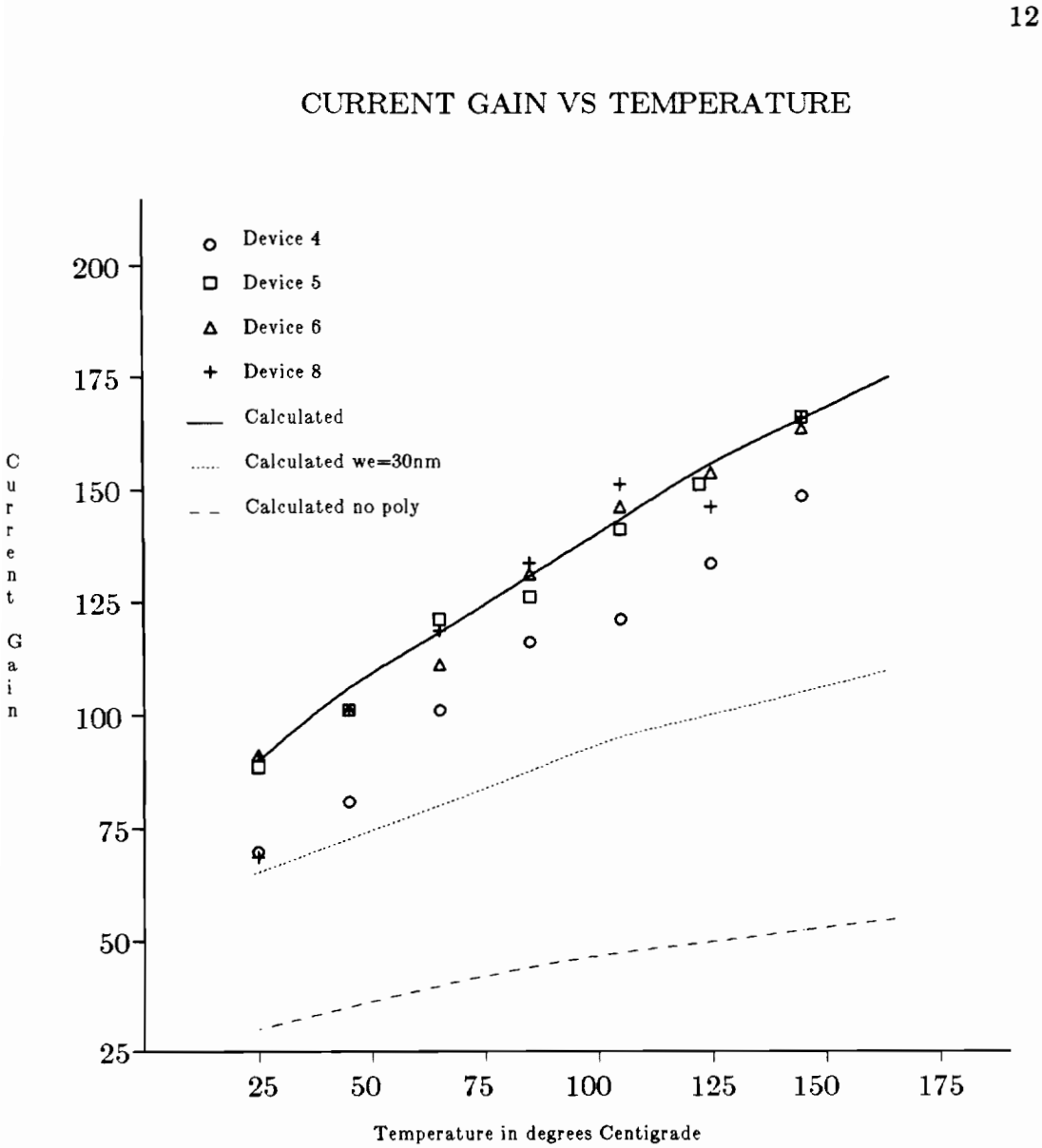

Figure 3.2. Temperature dependence of current gain for PEC transistors.

3.3. Theory

Consider a npn transistor under the active bias condition. The transistor is an effective current amplifier. The corresponding current flow diagram is sketched in figure 3.3 [20]. The current gain is defined

as:

$$hfe = \frac{I_C}{I_B} \tag{3.1}$$

Consider figure 3.3. The reverse saturation current (3) is significant only if V_{cb} is large. For normal operation under active bias, V_{cb} is small and the saturation current can be neglected. For a well designed transistor, with a base width less than one tenth the diffusion length, the base recombination current (1) can also be neglected. Using these assumptions the collector current (I_C) is made up of only the electrons injected

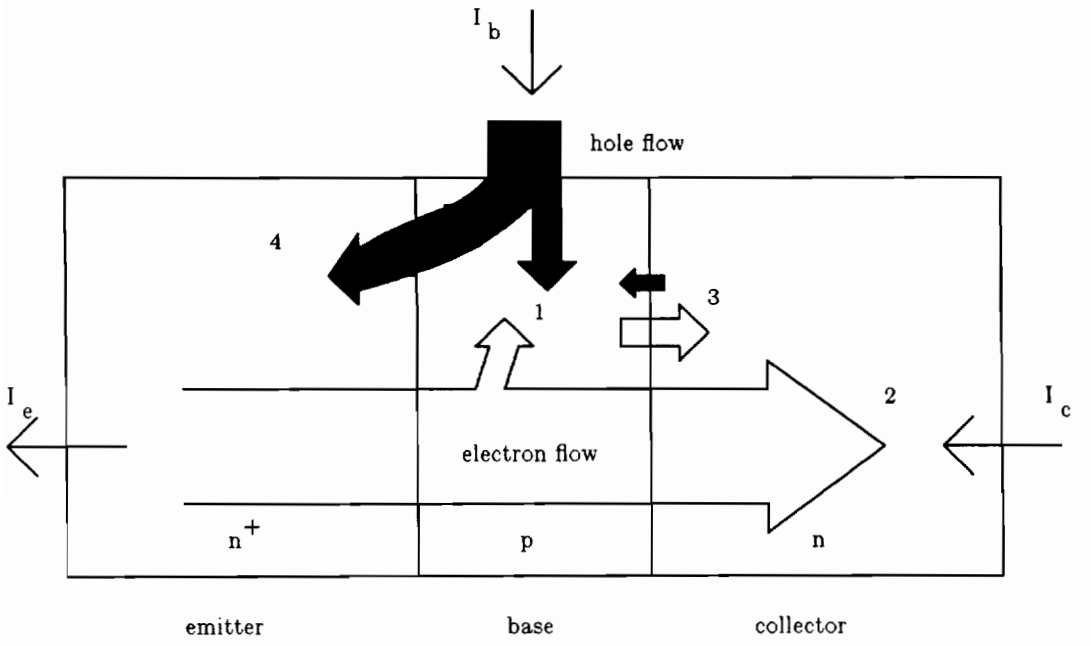

Figure 3.3. The electron and hole flow of an active biased NPN transistor.

into the base from the emitter ($I_{nB}\exp(qV_{be}/kT)$), since none are lost in the base region or at the base collector interface. The base current (I_B) is made up of the holes injected into the emitter from the base terminal (4) ($I_{pE}\exp(qV_{be}/kT)$). The current gain is [15],

$$hfe = \frac{I_{nB}}{I_{pE}} \tag{3.2}$$

These two currents (I_{nB} and I_{pE}) are both diffusion currents. I_{nB} is the electron diffusion current in the base. I_{pE} is the hole diffusion current in the emitter.

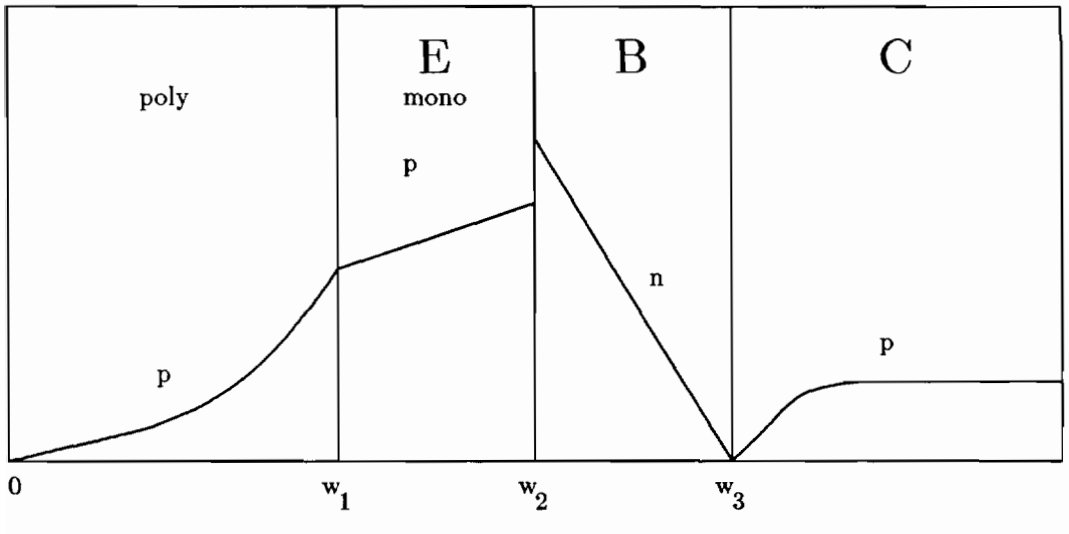

Figure 3.4. The minority carrier distribution of an active biased polysilicon-emitter-contacted NPN transistor.

For a simple two-region model similar to Ning et al. [1] the minority carrier distribution under active bias is shown in Figure 3.4. It is important to note that this model shows no boundary layer and can only be applied to devices that have a broken up oxide layer at the monosilicon-polysilicon interface as described earlier. It is probably not a good model for those devices with balled up oxide at the interface. The following equations are derived in detail in appendix A and notations can also be found there. Solving the diffusion equation for J_{nB} [21], the current density, with the boundary conditions $n = n_{oB}$ *at* $x = w_2$, and $n = 0$ *at* $x = w_3$,

$$J_{nB}(w_2) = \frac{-qD_{nB}}{L_{nB}} n_{oB} \coth\frac{w_B}{L_{nB}} \tag{3.3}$$

with, $w_B = w_3 - w_2$ denoting the base width. Similarly, upon solving the diffusion equation for J_{pE} with boundary conditions $p = 0$ *at* $x = 0$, $p = p(w_1)$ *at* $x = w_1$, $p = p_{oE}$ *at* $x = w_2$, and eliminating $p(w_1)$ by using the boundary condition that the hole current is continuous at $x = w_1$, one finds

$$J_{pE}(w_2) = \frac{qD_{p2}}{L_{p2}} p_{oE} \left[\frac{\frac{D_{p2}}{L_{p2}} \operatorname{csch}^2\frac{w_E}{L_{p2}}}{\frac{D_{p2}}{L_{p2}} \coth\frac{w_E}{L_{p2}} + \frac{D_{p1}}{L_{p1}} \coth\frac{w_1}{L_{p1}}} - \coth\frac{w_E}{L_{p2}} \right] \tag{3.4}$$

Here, $w_E = w_2 - w_1$ is the emitter width. Using equations 3.3 and 3.4 with the conditions $w_B \ll L_{nB}$ and $w_e < L_{p2}$ the current gain is given to a good approximation by [1, 9, 10],

$$hfe \approx \left[\frac{n_{oB}}{p_{oE}}\right]\left[\frac{D_{nB}}{D_{p2}}\right]\left[\frac{w_E}{w_B} + \frac{D_{p2}L_{p1}}{w_B D_{p1}} \tanh \frac{w_1}{L_{p1}}\right] \qquad (3.5)$$

If $w_1 \longrightarrow 0$, which is the case for an npn transistor with no polysilicon layer, the current gain is reduced to [14, 16, 22, 23],

$$hfe(no\ poly) \approx \left[\frac{n_{oB}}{p_{oE}}\right]\left[\frac{D_{nB}}{D_{p2}}\right]\left[\frac{w_E}{w_B}\right] \qquad (3.6)$$

This equation can also be obtained by following the same procedures detailed above using the boundary conditions $p = 0$ at $x = w_1$ and $p = p_{oE}$ at $x = w_E$, where $w_1 = 0$ [24-26].

The temperature dependence can be analyzed by doing a term by term inspection of equations 3.5 and 3.6.

a) n_{oB}/p_{oE} is the minority carrier concentration ratio at the base emitter junction. Under moderately doped conditions this would simply be N_D/N_A, but since the emitter is heavily doped bandgap narrowing occurs in the emitter. When the emitter is heavily doped the bandgap E_g is reduced by ΔE due to the numerous dislocations and lattice deformations. This change in the bandgap causes a change in the value and

temperature dependence of the equilibrium carrier concentration (n_i). Therefore,

$$n_{oB} = \frac{(n_{iB})^2}{N_A} = \frac{AT^3 \exp \frac{(-E_g)}{kT}}{N_A} \tag{3.7}$$

and [26]

$$p_{oE} = \frac{(n_{iE})^2}{N_D} = \frac{AT^3 \exp \frac{-(E_g - \Delta E)}{kT}}{N_D} \tag{3.8}$$

This introduces an exponential temperature dependence,

$$\frac{n_{oB}}{p_{oE}} = \frac{N_D}{N_A} \exp\left[\frac{-\Delta E}{kT}\right] \tag{3.9}$$

The minority carrier concentration of the emitter at the base-emitter junction (p_{oE}) is difficult to determine. The doping profile of a npn transistor shows N_D decreasing rapidly at this junction. This concentration and the corresponding ΔE were used as a fitting parameter. To calculate this ratio the values $N_A = 3 \times 10^{17}$ cm^{-3}, $N_D = 4 \times 10^{19}$ cm^{-3}, and $\Delta E = .089$ eV were used. With a surface concentration of 10^{20} cm^{-3} the choice of the value 4×10^{19} cm^{-3} is reasonable for the concentration at the base-emitter junction. Many studies have been carried out to calculate and measure ΔE in silicon but definite values of

ΔE are still not available; $\Delta E = .089$ eV is not an unreasonable value for this doping level and is in the range of values reported in the literature [10, 14, 15].

b) D_{nB}/D_{p2} is the ratio of the diffusion constant of the base region to the diffusion constant of the monosilicon emitter region. It is convenient to examine the diffusion constant ratio through the Einstein's relationship,

$$\frac{D_{nB}}{D_{p2}} = \frac{\mu_{nB}\ kT/q}{\mu_{p2} kT/q} = \frac{\mu_{nB}}{\mu_{p2}} \tag{3.10}$$

The mobility is limited by two mechanisms, ie. lattice and impurity scattering. The lattice scattering is strongly temperature dependent due to thermal vibration ($\mu = CT^{-3/2}$) [27], while impurity scattering is dependent only on the number of scattering centers and thus temperature independent. For doping levels greater than 10^{19} cm^{-3}, like in the emitter, impurity scattering dominates [20, 28] and the mobility is essentially a constant with respect to temperature [29-31]. For the base where the doping level is much smaller, lattice scattering dominates. The temperature dependence for the diffusion ratio can thus be expressed as,

$$\frac{\mu_{nB}}{\mu_{p2}} = \frac{CT^{-3/2}}{\mu_{p2}} \tag{3.11}$$

Here μ_{p2} is the mobility of the minority carrier in the single crystalline layer of the emitter and $CT^{-3/2}$ is the mobility of the minority carrier in the base. From Eq. 1.2.10 in Muller and Kamins [28] μ_{nB} at 300°K can be calculated to be 484 cm^2/Vs. Equating this value to $CT^{-3/2}$, C is determined to be 2.51 x 10^6 $cm^2/VsK^{3/2}$. The hole mobility can be calculated using the empirically derived expression given by Caughey et al., resulting in $\mu_{p2} = 49$ cm^2/Vs [32].

c) w_E/w_B or $w_E/w_B + (D_{p2}L_{p1}/D_{p1}w_{p1})\tanh(w_1/L_{p1})$ in the absence or presence of the polylayer. The emitter width (w_E) and base width (w_B) are temperature independent within normal operating temperatures. These widths are determined almost exclusively by the impurity profile. It can be shown for temperatures above 100°K that 100% of the impurities become ionized [14]. For a transistor with no polysilicon layer this term is temperature independent.

The diffusion constant for the monosilicon emitter region (D_{p2}) and for the polysilicon emitter contact region (D_{p1}) has a T dependence according to the Einstein's relationship as discussed previously,

$$D_{p2} = \mu_{p2}kT/q \tag{3.13}$$

$$D_{p1} = \mu_{p1}kT/q \tag{3.14}$$

Both μ_{p2} and μ_{p1} are temperature independent. The non-temperature

dependence of μ_{p1} (the mobility of the holes in the polysilicon) is supported by reported data [13].

The minority carrier diffusion length in the polysilicon layer (L_{p1}) follows the 1/2 power law on temperature,

$$L_{p1} = \sqrt{\mu_{p1} \tau_A kT/q} \tag{3.15}$$

The Auger recombination lifetime (τ_A) is temperature independent at temperatures less than 400°K [33]. From equations 3.13-15 the temperature dependence of this last term for a transistor with a polysilicon contact, with the additional condition $w_1 \gg L_{p1}$, can be expressed as,

$$\frac{w_E}{w_B} + \frac{\mu_{p2}}{w_B}\left[\frac{\tau_A kT}{\mu_{p1} q}\right]^{1/2} \tag{3.16}$$

This shows a npn transistor with a polysilicon layer has only a $\sqrt{T}$ term difference when compared to a transistor without a polysilicon layer. The values needed to calculate this last term, not previously given, are $\mu_{p1} = 9.6$ cm^2/Vs [34] and $\tau_A = 100$ ps [2,35]. Using these values $L_{p1} \approx 0.5 \times 10^{-5}$ cm which is in agreement with the values reported in the literature [1,10,35].

Upon inserting all the temperature dependent terms into equation 3.5, one can write,

$$hfe \approx \frac{N_D}{N_A} \exp\left[\frac{-\Delta E}{kT}\right]\left[\frac{CT^{-3/2}}{\mu_{p2}}\right]\left[\frac{w_E}{w_B} + \frac{\mu_{p2}}{w_B}\left[\frac{\tau_A kT}{\mu_{p1} q}\right]^{1/2}\right] \quad (3.17)$$

The values used in equation 3.17 to fit the measured temperature dependence of hfe are listed in table 3.2. Figure 3.2 shows the calculated curves for both a transistor with and without polysilicon, and the experimental data. As can be seen, good correlation between the experimental data and theory seems to exist. This graph also shows the predicted factor of 3 current gain improvement over conventional transistors.

TABLE 3.2

Calculation Values		
Parameter	Value	Reference
N_D(base-emitter junction)	4 x 10^{19}cm^{-3}	[9]
N_A(base)	3 x 10^{17}cm^{-3}	
E_g	1.124 eV	[28]
ΔE	.089 eV	[15, 36, 37]
C (lattice scattering const)	2.51 x 10^{6}cm^{-3}	
A (minor carrier conc const)	4.64 x 10^{31}cm^{-6}	
μ_{nB} @300K	484cm^2/Vs	[28]
μ_{p1} (polysilicon)	9.6cm^2/Vs	[34]
μ_{p2} (monosilicon)	49cm^2/Vs	[32]
w_1 (polysilicon)	2500Å	
w_E	1400Å	
w_B	1800Å	
τ_A (polysilicon)	100ps	[2, 35]
τ_B (base)	18us	[38]

To verify that these values reflect the actual device, I_C and I_B were also calculated using the following equations,

$$I_C = AJ_{nB} exp(V_{BE}/kT) \tag{3.18}$$

and

$$I_B = AJ_{pE} exp(V_{BE}/kT) \tag{3.19}$$

The results are shown in figure 3.1, and is seen to be in good agreement with experimental data.

This theory can be compared with Ning's measurements for thick and thin polysilicon with the use of equation 3.5. Calculations were carried out using this equation with $w_1 = 30$ nm and $w_1 = 300$ nm. The results for the case of $w_1 = 30$ nm are shown in figure 3.2. The theoretical results for the 300 nm device were so close to the 250 nm device data already graphed that they were not included. Further calculations of I_B were made for the different widths. I_B for the thinner polysilicon was found to be larger as Ning predicted, but the temperature dependence of I_B remained basically the same for both thicknesses.

Note that the third term of equation 3.5,

$$F(w_1) = \frac{w_E}{w_B}\left[1 + \frac{D_{p2}L_{p1}}{D_{p1}w_E}\tanh\frac{w_1}{L_{p1}}\right] \tag{3.21}$$

uncovers the parameters responsible for the enhanced current gain in

PEC transistors. Figure 3.5 illustrates the behavior of this term as a function of the polysilicon width (w_1), with $w_E/w_B = 1$ and several different values of the hole, recombination lifetime (τ_A) and mobility (μ_{p1}) in the polysilicon. It is interesting to note that figure 3.5 specifically points to the fact that improvements greater than a factor of 3 can actually be achieved in the PEC transistor with no oxide layer under the polysilicon contact.

Looking at this term as a gain factor for the PEC transistor with $w_1 > L_{p1}$, it can be expressed as,

$$\frac{w_E}{w_B} + \frac{D_{p2}L_{p1}}{D_{p1}w_B} \tag{3.22}$$

which is equivalent to,

$$\frac{w_E}{w_B} + \frac{\mu_{p2}}{w_B}\left[\frac{\tau_A kT}{\mu_{p1}q}\right]^{1/2} \tag{3.23}$$

This shows the three parameters effecting current gain are the ratio of the emitter width to base width (w_E/w_B), τ_A, and μ_{p1}.

At first glance it would seem that by making $w_E \gg w_B$ the gain would be increased significantly and overshadow the second term. However, unlimited increase of w_E results in increased series resistance and increased RC time constant. Also, equation 3.5 is not valid for $w_E > L_{p2}$

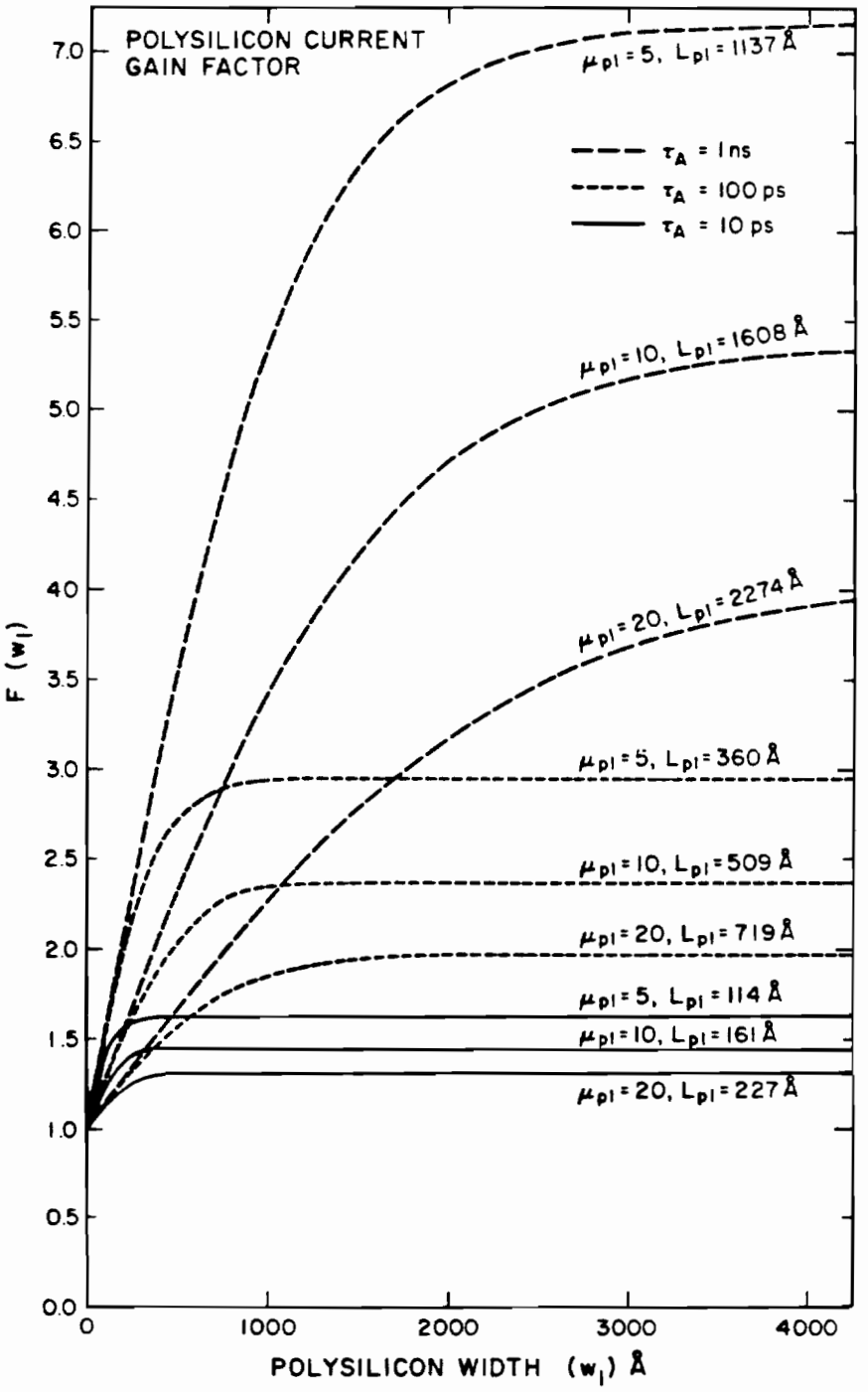

Figure 3.5. Polysilicon term as a function of w_1 with variables τ_A and μ_{p1}.

(note equation 3.4 for this condition, csch $w_E/L_{p2} \rightarrow 0$ and the equation becomes the same as it would be for a conventional transistor). This leaves τ_A and μ_{p1} as the two viable parameters for optimizing hfe.

It is easy to see from figure 3.5 that as τ_A increases or μ_{p1} decreases the current gain will increase. The minority carrier, lifetime (τ_A) and mobility (μ_{p1}) in the polysilicon are determined in a complex manner by the doping level, the grain size, grain boundary density, ect. These values can be altered by modifying some of the processing steps such as deposition, the annealing time and temperature. Further studies are required to investigate these effects.

CHAPTER 4

Conclusion

In this thesis the polysilicon-emitter-contacted bipolar junction transistors (PEC transistors) were characterized both theoretically and experimentally. An emphasis was focused on examining the temperature dependence of the current gain (hfe). Some of the highlights of the work are summarized as follows.

1) The current gain of PEC transistors are shown to be more temperature sensitive than in conventional devices.

2) This temperature data was satisfactorily quantified, by using the two region model and pertinent inherent electronic properties of polysilicon thin films.

3) The enhanced temperature dependence of the current gain is to be primarily attributed to the temperature dependence of minority carrier diffusion length of the polysilicon.

4) The expression for current gain derived in this thesis is general enough to provide a few guide lines for optimized hfe. Specifically it is shown that a higher hfe could result with smaller minority carrier mobility in polysilicon and larger minority carrier lifetimes therein.

5) Smaller mobilities are normally associated with fine grain polysilicon films, while larger lifetimes could be achieved with grain boundry hydrogenation.

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APPENDIX A

NOTATION

hfe	Current Gain using h-parameters for a common emitter configuration
I_{pE}	Hole Diffusion Current in the Emitter
I_{nB}	Electron Diffusion Current in the Base
p_{oE}	Emitter Hole Concentration at the Base-Emitter Junction
n_{oB}	Base Electron Concentration at the Base-Emitter Junction
D_{p1}	Hole Diffusion Constant in the Polysilicon Contact
D_{p2}	Hole Diffusion Constant in the Monosilicon Emitter
D_{nB}	Electron Diffusion Constant in the Base
w_1	Polysilicon Contact Width
w_E	Monosilicon Emitter Width
w_B	Base Width
L_{p1}	Minority Carrier Diffusion Length in the Polysilicon
L_{p2}	Minority Carrier Diffusion Length in the Emitter
L_{nB}	Minority Carrier Diffusion Length in the Base
N_D	Minority Carrier Concentration in the Emitter
N_A	Minority Carrier Concentration in the Base

C	Lattice Scattering Constant
τ_A	Recombination Lifetime of Holes in the Polysilicon
τ_B	Recombination Lifetime of Electrons in the Base
μ_{p1}	Hole Mobility in the Polysilicon
μ_{p2}	Hole Mobility in the Emitter
μ_{nB}	Electron Mobility in the Base
ΔE	Bandgap Narrowing in the Heavily Doped Emitter
n_{iE}	Equilibrium Carrier Concentration in the Emitter
n_{iB}	Equilibrium Carrier Concentration in the Base

Detailed Derivation of Current Gain

General Equations

The current gain is the ratio of two diffusion currents,

$$hfe = \frac{J_{nB}}{J_{pE}} \tag{A.1}$$

The diffusion currents are defined as,

$$J_{pE} = -qD_p \frac{d}{dx} p(x) \tag{A.2}$$

and

$$J_{nB} = qD_n \frac{d}{dx} n(x) \tag{A.3}$$

To proceed further an expression for the excess minority carries across the base and the emitter must be given. One starts with the continuity equation for holes

$$\frac{\partial p(x,t)}{\partial t} = D_p \frac{\partial^2 p}{\partial x^2} - \mu_p E(x) \frac{\partial p}{\partial x} - \frac{p}{\tau_p} \tag{A.4}$$

For steady state conditions ($\partial p / \partial t = 0$) and negligible drift ($\mu_p E(x) \frac{\partial p}{\partial x} \rightarrow 0$) results in the diffusion equation,

$$D_p \frac{\partial^2 p}{\partial x^2} = \frac{p}{\tau_p} \tag{A.5}$$

The general solution to this equation with $L_p = \sqrt{D_p \tau_p}$ is,

$$p = A\exp(x/L_p) + B\exp(-x/L_p) \tag{A.6}$$

Current in the Polysilicon Contact Region

Solving equation A.6, for the polysilicon contact region (see figure 3.4), using the boundary conditions at x = 0, p = 0 and at x = w_1, p = $p(w_1)$.

Since at x = 0, p = 0 then A = -B therefore,

$$p(x) = A\left[e^{x/L_{p1}} - e^{-x/L_{p1}}\right] \tag{A.7}$$

At x = w_1, p = p(w_1) then,

$$p(w_1) = A\left[e^{w_1/L_{p1}} - e^{-w_1/L_{p1}}\right] \tag{A.8}$$

Solving equation A.8 for A and substituting into equation A.7,

$$p(x<w_1) = p(w_1)\left[\frac{e^{x/L_{p1}} - e^{-x/L_{p1}}}{e^{w_1/L_{p1}} - e^{-w_1/L_{p1}}}\right] \tag{A.9}$$

Taking the derivative of equation A.9 and inserting into A.2,

$$J_{pE}(x<w_1) = \frac{-qD_{p1}}{L_{p1}}\, p(w_1)\left[\frac{e^{x/L_{p1}} + e^{-x/L_{p1}}}{e^{w_1/L_{p1}} - e^{-w_1/L_{p1}}}\right] \tag{A.10}$$

therefore,

$$J_{pE}(0) = \frac{-qD_{p1}}{L_{p1}}\, p(w_1)\, \mathrm{csch}\, \frac{w_1}{L_{p1}} \tag{A.11}$$

and

$$J_{pE}(w_1) = \frac{-qD_{p1}}{L_{p1}}\, p(w_1)\, \coth\, \frac{w_1}{L_{p1}} \tag{A.12}$$

Current in the Emitter Region

Solving equation A.6, for the emitter region, using the boundary conditions at x = w_1, p = $p(w_1)$ and at x = w_2, p = p_{oE}.

At x = w_1 A.6 is,

$$p(w_1) = Aexp(w_1/L_{p2}) + Bexp(-w_1/L_{p2}) \tag{A.13}$$

At x = w_2 A.6 is,

$$p_{oE} = Aexp(w_2/L_{p2}) + Bexp(-w_2/L_{p2}) \tag{A.14}$$

Solving for A for both A.13 and A.14,

$$A = p(w_1)exp(-w_1/L_{p2}) - Bexp(-2w_1/L_{p2}) \tag{A.15}$$

and

$$A = p_{oE}exp(-w_2/L_{p2}) - Bexp(-2w_2/L_{p2})$$

Equating and solving for B,

$$B = \frac{-p_{oE}\,exp\,(w_1/L_{p2}) + p\,(w_1)exp\,(w_2/L_{p2})}{exp\,((-w_1+w_2)/L_{p2}) - \exp((w_1-w_2)/L_{p2})} \qquad (A.16)$$

Substituting B into equation A.15, A is equal to,

$$A = \frac{p(w_1)e^{(-2w_1+w_2)/L_{p2}} - p(w_1)e^{-w_2/L_{p2}} + p_{oE}e^{-w_1/L_{p2}} - p(w_1)e^{(-2w_1+w_2)/L_{p2}}}{e^{(-w_1+w_2)/L_{p2}} - e^{(w_1-w_2)/L_{p2}}} \qquad (A.17)$$

Subtracting out the first and fourth term in the numerator of equation A.17, and then substituting the value of A and B above into equation A.6, the value of p the minority carriers in the emitter region can be expressed as,

$$p(x) = \frac{\left[p_{oE}e^{-w_1/L_{p2}} - p(w_1)e^{-w_2/L_{p2}}\right]e^{x/L_{p2}} + \left[-p_{oE}e^{w_1/L_{p2}} + p(w_1)e^{w_2/L_{p2}}\right]e^{-x/L_{p2}}}{e^{(-w_1+w_2)/L_{p2}} - e^{(w_1-w_2)/L_{p2}}} \qquad (A.18)$$

Taking the derivative of equation A.18 and inserting into A.2,

$$J_{pE}(w_1<x<w_2) = \frac{qD_{p2}}{L_{p2}} \frac{p(w_1)\left[e^{(x-w_2)/L_{p2}} + e^{(w_2-x)/L_{p2}}\right] - p_{oE}\left[e^{(x-w_1)/L_{p2}} + e^{(w_1-x)/L_{p2}}\right]}{e^{(-w_1+w_2)/L_{p2}} - e^{(w_1-w_2)/L_{p2}}} \qquad (A.19)$$

Therefore,

$$J_{pE}(w_1) = \frac{qD_{p2}}{L_{p2}} \left[p(w_1)\coth\frac{w_2-w_1}{L_{p2}} - p_{oE}\,\mathrm{csch}\frac{w_2-w_1}{L_{p2}}\right] \qquad (A.20)$$

and

$$J_{pE}(w_2) = \frac{qD_{p2}}{L_{p2}} \left[p(w_1) \operatorname{csch} \frac{w_2 - w_1}{L_{p2}} - p_{oE} \coth \frac{w_2 - w_1}{L_{p2}} \right] \quad \text{(A.21)}$$

Emitter Current at the Base/Emitter Junction

The current is continuous at the polysilicon contact and monosilicon emitter junction therefore equation A.12 is equal to A.20. Equating these and solving for $p(w_1)$ gives,

$$p(w_1) = \frac{p_{oE} \dfrac{D_{p2}}{L_{p2}} \operatorname{csch} \dfrac{w_E}{L_{p2}}}{\dfrac{D_{p2}}{L_{p2}} \coth \dfrac{w_E}{L_{p2}} + \dfrac{D_{p1}}{L_{p1}} \coth \dfrac{w_1}{L_{p1}}} \quad \text{(A.22)}$$

Here $w_E = w_2 - w_1$. Inserting this value into equation A.21 the current at the Base/Emitter junction is,

$$J_{pE}(w_2) = \frac{qD_{p2}}{L_{p2}} p_{oE} \left[\frac{\dfrac{D_{p2}}{L_{p2}} \operatorname{csch}^2 \dfrac{w_E}{L_{p2}}}{\dfrac{D_{p2}}{L_{p2}} \coth \dfrac{w_E}{L_{p2}} + \dfrac{D_{p1}}{L_{p1}} \coth \dfrac{w_1}{L_{p1}}} - \coth \frac{w_E}{L_{p2}} \right] \quad \text{(A. 23)}$$

For the condition $w_E < L_{p2}$ then $\operatorname{csch}(w_E/L_{p2}) \rightarrow L_{p2}/w_E$ and $\coth(w_E/L_{p2}) \rightarrow L_{p2}/w_E$ therefore,

$$J_{pE}(w_2) \approx qD_{p2}\, p_{oE} \left[\frac{\dfrac{-D_{p1}}{L_{p1}} \coth\dfrac{w_1}{L_{p1}}}{\dfrac{D_{p2}}{w_E} + \dfrac{D_{p1}}{L_{p1}} \coth\dfrac{w_1}{L_{p1}}} \right] \tag{A.24}$$

Current in the Base Region

The diffusion equation A.5 can be written for electrons also,

$$D_n \frac{\partial^2 n}{\partial x^2} = \frac{n}{\tau_n} \tag{A.25}$$

The general solution to this equation with $L_n = \sqrt{D_n \tau_n}$ is,

$$n = A\exp(x/L_n) + B\exp(-x/L_n) \tag{A.26}$$

Solving this equation, for the base region (see figure 3.4), using the boundary conditions at x = w_2, n = n_{oB} and at x = w_3, n = 0.

Since at x = w_2, n = n_{oB} then,

$$n_{oB} = Ae^{w_2/L_{nB}} + Be^{-w_2/L_{nB}} \tag{A.27}$$

And at x = w_3, n = 0 then,

$$0 = Ae^{w_3/L_{nB}} + Be^{-w_3/L_{nB}} \tag{A.28}$$

Solving for A and equating A.27 and A.28,

$$A = -Be^{-2w_3/L_{nB}} = n_{oB}e^{-w_2/L_{nB}} - Be^{-2w_2/L_{nB}} \tag{A.29}$$

Solving for B,

$$B = \frac{n_{oB} e^{w_3/L_{nB}}}{e^{(w_3-w_2)/L_{nB}} - e^{(-w_3+w_2)/L_{nB}}} \tag{A.30}$$

Substituting B into equation A.29, A is equal to,

$$A = \frac{-n_{oB} e^{-w_3/L_{nB}}}{e^{(w_3-w_2)/L_{nB}} - e^{(-w_3+w_2)/L_{nB}}} \tag{A.31}$$

Substituting the value of A and B above into equation A.26, the value of n the minority carriers in the base region can be expressed as,

$$n(x) = -n_{oB}\left[\frac{e^{(-w_3+x)/L_{nB}} - e^{(w_3-x)/L_{nB}}}{e^{(w_3-w_2)/L_{nB}} - e^{(-w_3+w_2)/L_{nB}}}\right] \tag{A.32}$$

Taking the derivative of equation A.32 and inserting into A.3,

$$J_{nB}(x) = \frac{-qD_{nB}}{L_{nB}} n_{oB}\left[\frac{e^{(-w_3+x)/L_{nB}} + e^{(w_3-x)/L_{nB}}}{e^{w_B/L_{nB}} - e^{-w_B/L_{nB}}}\right] \tag{A.33}$$

here $w_B = w_3 - w_2$. Therefore at the base/emitter junction the base current is,

$$J_{nB}(w_2) = \frac{-qD_{nB}}{L_{nB}} n_{oB} \coth \frac{w_B}{L_{nB}} \tag{A.34}$$

For the condition $w_B \ll L_{nB}$ then $\coth(w_B/L_{nB}) \rightarrow L_{nB}/w_B$ and,

$$J_{nB}(w_2) \approx \frac{-qD_{nB}}{w_B} n_{oB} \tag{A.35}$$

Current Gain

Now substituting equation A.35 and A.24 into equation A.1 gives,

$$hfe \approx \left[\frac{n_{oB}}{p_{oE}}\right]\left[\frac{D_{nB}}{D_{p2}}\right]\left[\frac{w_E}{w_B} + \frac{D_{p2}L_{p1}}{D_{p1}w_B}\tanh\frac{w_1}{L_{p1}}\right] \qquad \text{(A.36)}$$

VITA

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