SOI MOS Devices
for Active Matrix
Electroluminescent Displays

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To

my parents and sister

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A	Area of a pn junction
A_G	Area under the gate
C_{ox}	Gate oxide capacitance per unit area
C_d	Depletion capacitance per unit area
C_{it}	Capacitance per unit area due to the interface charge
C_L	Load capacitance
D	Carrier diffusivity
d_{epi}	Epi layer thickness
D_{it}	Interface trap density
D_{nB}	Electron diffusion coefficient in the base
D_{hE}	Hole diffusion coefficient in the emitter
E	Electric field
E_c	Critical electric field for breakdown voltage
E_g	Bandgap
f_p	Frequency of operation
g_m	Transconductance
HF	Hydrofluoric acid
I_B	Base current
I_C	Collector current
I_{CP}	Charge pumping current
I_D	Drain Current
I_{Dsat}	Saturation current

I_{rev}	Leakage current across a reverse biased junction
I_{sub}	Substrate current
k	Boltzmann constant
L	Channel length, drift region length
L_{eff}	Effective channel length
L_b	Base width
L_n	Minority carrier diffusion length (electron)
M	Avalanche multiplication factor
N_A, N_a	Acceptor concentration
N_B	Base doping concentration
N_E	Emitter doping concentration
N_{epi}	epi layer dopant concentration
n_i	Intrinsic carrier concentration
N_t	Interface trap density
Q_{ox}	Interface charge density
R_{ch}	Channel resistance
R_{drift}	Drift region resistance
R_{on}	On-resistance
R_{sp}	Specific on-resistance
S	Sub-threshold swing
Si	Silicon
SiO_2	Silicon Oxide
Si_3N_4	Silicon Nitride
T	Temperature
t_{box}	Buried oxide thickness

t_{si}, t_{soi}	SOI film thickness
V_A	Pulse amplitude for charge pumping
V_{bG}	Back gate voltage
V_{BR}	Breakdown voltage
V_{FB}	Flat-band voltage of a MOS capacitor
V_D	Drain voltage
V_{DD}	Power supply or drive voltage
V_{DS}	Drain to source voltage
V_{fG}	Front gate voltage
V_{GS}	Gate to source voltage
V_{th}	Threshold voltage
W	Device width
x_{dmax}	Maximum depletion width
Z	Device width
W_B	Base width
W_E	Emitter width
α_n	Electron ionization coefficient
α_p	Hole ionization coefficient
β	Gain of a bipolar transistor
γ	Emitter injection efficiency
ΔE_g	Difference in bandgap
ΔE_V	Valence band offset between Si and SiGe
$\Delta\phi_s$	Energy range scanned within the bandgap
ε	Permittivity
μ	Mobility

μ_{FE}	Field effect mobility
ρ	Resistivity
σ_n	Electron capture cross-section
τ	Generation lifetime, Device lifetime for hot carrier stress
τ_n	Minority carrier lifetime (electron)
$\tau_{dynamic}$	device lifetime obtained from the dynamic stress of a device
$\tau_{dcstress}$	device lifetime obtained from the DC stress of a device
φ_F	Substrate surface potential
ϕ_s	Metal-semiconductor workfunction difference
ψ	Electric potential

List of Acronyms

AMEL	Active Matrix Electroluminescent
AMLCD	Active Matrix Liquid Crystal Display
BC	Back Channel
BESOI	Bonded and Etched Back Silicon on Insulator
BOX	Buried Oxide
BPSG	Borophosphosilicate Glass
CMOS	Complimentary Metal Oxide Semiconductor
CRT	Cathode Ray Tube
CVD	Chemical Vapor Deposition
DRAM	Dynamic Random Access Memory
DSD	Dielectric Semiconductor Dielectric
EL	Electroluminescent
ELO	Epitaxial Lateral Overgrowth
FC	Front Channel
FD	Fully Depleted
FIPOS	Full Isolation by Porous Silicon
HMD	Helmet Mounted Display
HVIC	High Voltage Integrated Circuit
IC	Integrated Circuit
ILD	Inter-Level Dielectric
ISE	Isolated Silicon Epitaxy
ITO	Indium Tin Oxide
LATID	Large Angle Tilt Implanted Drain
LDD	Lightly Doped Drain

LDMOS	Lateral Double Diffused Metal Oxide Semiconductor
LOCOS	Local Oxidation of Silicon
LPCVD	Low Pressure Chemical Vapor Deposition
LSPE	Lateral Solid Phase Epitaxy
LTO	Low Temperature Oxide
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-channel Metal Oxide Semiconductor
PACE	Plasma Assisted Chemical Etching
PD	Partially Depleted
PMOS	P-Channel Metal Oxide Semiconductor
RESURF	Reduces Surface Field
SCE	Short Channel Effects
SIMOX	Separation by Implanted Oxygen
SOI	Silicon on Insulator
TFT	Thin Film Transistor
TFSOI	Thin Film Silicon on Insulator
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration
XTEM	Cross-sectional Transmission Electron Microscope
ZMR	Zone Melting Recrystallization

ABSTRACT

SOI MOS Devices for Active Matrix Electroluminescent Displays

Shafqat Ahmed
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Silicon-on-insulator (SOI) technology offers higher speed, lower power consumption, and reduced process complexity as compared to their bulk counterparts. SOI substrates are used in high resolution active matrix electroluminescent (AMEL) displays mainly due to the simple but effective isolation techniques provided by the SOI technology. In this thesis, SOI MOS devices and their specific applications in AMEL displays were investigated.

First, important material parameters such as mobility, minority carrier lifetime, and generation lifetime were determined to investigate the crystalline quality of different types SOI substrates. The high mobility and lifetime values extracted from the experimental results indicate a viable SOI wafer manufacturing technology. Special attention was paid to the design of high voltage lateral double diffused metal oxide semiconductor (LDMOS) transistors used in the AMEL pixel arrays. A two-dimensional simulator was used to model the SOI LDMOS structure and design rules were developed for optimization of the breakdown voltage performance. The design rules were then verified by experimental results from fabricated devices and near ideal breakdown voltage performance of a short drift region LDMOS transistor was demonstrated. The investigation of short drift region devices has led to the successful scaling of the current AMEL

pixel technology.

High temperature operation of SOI devices was investigated in detail. It was found that low leakage currents due to the reduced junction area in SOI devices enable them to operate at high temperatures. Comparison of I_{off}/I_{on} ratio at elevated temperatures suggests that dielectrically isolated SOI devices are more suitable for high temperature operations as compared to traditional junction isolated bulk Si transistors. Hot carrier effects, an important reliability hazard for short channel devices, were also studied and it was shown that power-law relationships developed for characterization and lifetime estimation of bulk devices can be extended to partially depleted SOI devices.

Low breakdown voltage of NMOS transistors has been a long known problem in the SOI technology. A possible solution may involve the use of SiGe in the source-drain regions, which lowers the gain of the parasitic bipolar transistor inherent to the SOI NMOS design. The valence band off-set between Si and SiGe leads to an improvement in the breakdown voltage. A two dimensional device simulator was used to demonstrate the feasibility of this concept.

Chapter 1

Introduction

1.1 Silicon-on-insulator Technology

Silicon-on-insulator (SOI) technology offers unique advantages as compared to the traditional bulk silicon technology. SOI devices are not only considered an almost essential extension of low voltage bulk CMOS scaling, but they are also finding wide range of applications in the high voltage arena [1-5]. The availability of high quality SOI substrates has spurred enormous amount of research and technology development. In this dissertation, both low voltage CMOS and high-voltage lateral double-diffused MOS (LDMOS) devices fabricated on SOI substrates and their applications in active matrix electroluminescent (AMEL) displays are investigated. Before exploring the advantages and issues regarding the use of SOI substrates in AMEL technology, potential benefits of SOI in today's semiconductor technology is first reviewed.

One of the major benefits of SOI substrates is the simple dielectric isolation of active circuit components. Junction isolation, wells and trenches are used in the traditional bulk CMOS technologies in order to prevent latch-up, which occurs due to inherent parasitic bipolar transistors present in an inverter layout. These practices increase the die area, resulting in higher cost and reduced yield. Memory chips fabricated on conventional Si substrates are also susceptible to alpha particles, which generates charge in the bulk material and introduces "soft error" in the stored data. However, circuits fabricated on SOI substrates offer excellent latch-up immunity and radiation hardness due to the

complete isolation provided by the buried oxide (BOX) layer.

Devices fabricated on SOI substrates have less parasitic capacitances and improved short channel effects. The absence of bottom junctions under the source-drain implant in typical thin film SOI devices not only significantly reduces the parasitic capacitance, but also decreases the leakage current. The reduced capacitance offers two fold benefit to high speed ULSI circuits. Researchers often use CV/I figure of merit to compare different technologies, where C, V, and I refer to the load capacitance, power supply voltage (V_{DD}), and saturation current (I_{Dsat}), respectively [6]. A smaller CV/I number translates into a faster circuit operation due to reduced capacitance and higher drive current. As the ratio of the storage capacitance versus the parasitic capacitance decreases, the DRAM cells can be designed with lower storage capacitance, enhancing the access time of the circuit [7]. An SOI CMOS process is not only faster than a comparable bulk technology, but also has reduced process complexity or the number of required mask steps, which is a consequence of simpler and more effective isolation techniques. According to one published report, an SOI process can reduce the die size by as much as 30% [5]. A reduction in die size is beneficial for economic reasons as well as shorter interconnect lengths for faster circuit operation.

Packing density of transistors is driven upward for two primary reasons: (1) the ability to fabricate more complex chips without a significant increase in the die size, and (2) faster circuit speed. As a result, the on-chip power consumption has become one of the major issues in today's VLSI technology. The dynamic power dissipation of a given chip can be approximated by using the simple expression [8]:

$$P_d = C_L V_{DD}^2 f_p \tag{1.1}$$

where C_L, V_{DD}, and f_p refer to the total load capacitance, power supply voltage, and frequency of operation. From eqtn. 1.1, it is evident that an SOI based IC technology will have less dynamic power dissipation at a given frequency and power supply voltage.

According to a recently published article, SOI circuits may have only two-third the capacitance of a comparable bulk technology, making SOI ICs more power efficient [6]. Static power dissipation, which is directly proportional to the leakage current, is also reduced.

Every year chip vendors introduce both memory and microprocessor chips that are faster and are more complex than their predecessors. In order to achieve this, the number of transistors per chip is increased, forcing the device engineers to scale the size of the individual transistors in an attempt to reduce the die size and also obtain higher speed. As the device dimensions are scaled, the substrate doping concentration increases and junctions become shallower in order to battle punch-through and short channel effects such as threshold voltage roll-off, caused by charge sharing between gate and the source-drain depletion regions. The lateral and vertical scaling of the MOS transistors cause higher electric fields within the device. High lateral electric field near the channel-drain interface causes hot carrier effects in sub-micron devices. The hot carriers, mostly electrons, causes damage to the thin gate oxide and are responsible for trap generation at the oxide interface near the drain junction. As a result, channel mobility is degraded and an increase in the drain series resistance is also observed. These device degradations manifest themselves in the form of an increase in threshold voltage, and reduction of transconductance (g_m) and the drive current. Hot carrier effect has become a major reliability problem for sub-micron devices and one of the primary causes of reduction of power supply voltage or the drive voltage (V_{DD}) in the cutting edge micro-processors. However, fully depleted SOI devices offer improved hot electron resistant capabilities due to a reduction of the lateral electric field at the channel-drain interface [9]. A reduction in the parasitic capacitance enables the chip designer to lower the power supply voltage without sacrificing speed, further enhancing the inherent hot carrier resistance of the fully depleted devices.

Figure 1-1 and 1-2 schematically illustrates some of the inherent advantages of a low voltage SOI CMOS technology - higher speed, lower power consumption, reduced process complexity, and enhanced reliability.

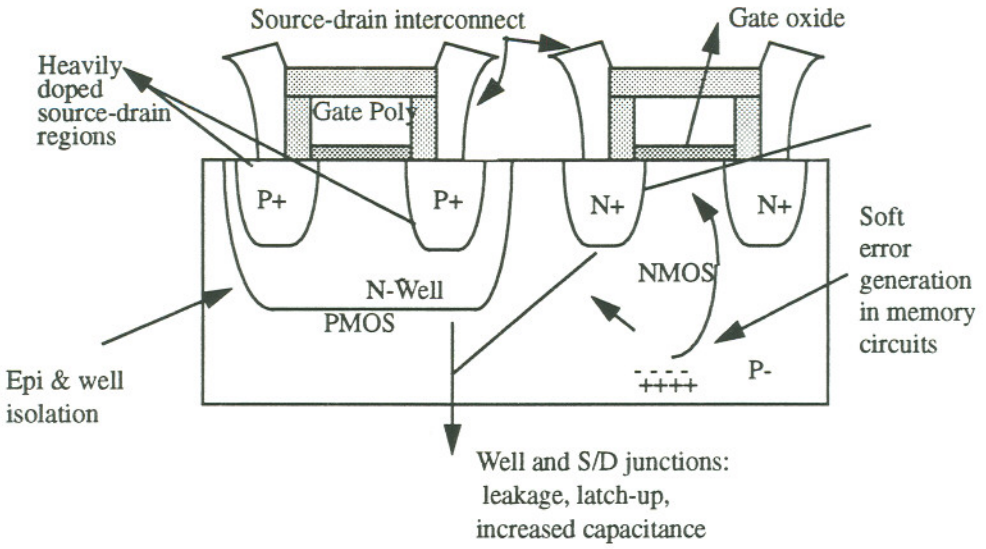

Figure 1-1: Cross-sectional view of traditional bulk CMOS devices.

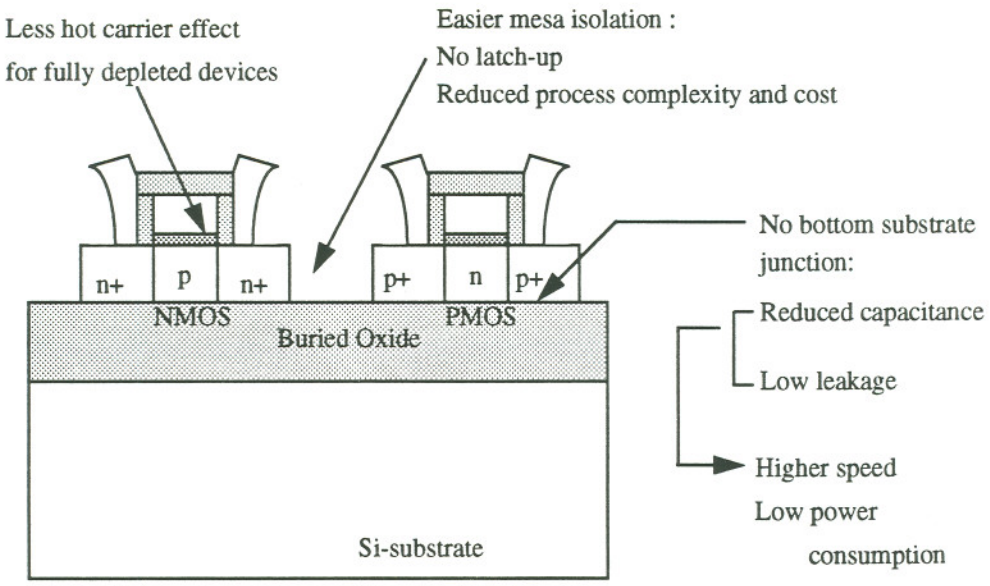

Figure 1-2: Cross-sectional view of SOI based CMOS devices.

Although most of the current research focuses on low-voltage, high-speed applications of SOI devices, high voltage integrated circuits (HVIC) also benefit immensely from the unique advantages offered by the SOI technology [4]. Use of ultra-thin SOI layers may allow the realization of ideal breakdown voltage performances for HVIC technology [10]. There is a great demand for power ICs which combine both high voltage components and CMOS logic devices without sacrificing significant amount of chip area. One of the biggest concerns in the bulk power technology has been the electrical isolation of high voltage components, which can be easily achieved in thin film SOI technologies by the use of mesa isolation techniques, as seen in Fig. 1-2. Mesa isolation involves fabricating individual devices on Si islands or mesas, completely dielectrically separated by the buried oxide underneath and field oxides grown on the edges or sidewalls of the islands. Applications in home appliances, automotive industry, and space electronics may be especially attractive. Due to reduced junction areas, SOI devices also offer low leakage currents at elevated temperatures. Therefore, SOI-based HVICs can fill a true void in today's IC market.

The rest of this chapter is devoted towards why and how SOI based technologies are currently applied to manufacture very high resolution helmet mounted displays (HMDs). The device and circuit design issues for active matrix electroluminescent (AMEL) displays on SOI substrates for helmet mounted operations are addressed. Finally, a brief overview of this thesis is also included.

1.2 Application of SOI substrates in flat panel display technology

In today's high paced world, where information is a priced commodity, displays are the focus of intense research and development activity because of their ability to interface with the user. Although traditional cathode ray tubes (CRTs) are still cheaper and arguably have the best quality pictures, they are heavy, power hungry, and occupy large

amount of space and therefore, not suitable for portable applications. For medical surgeons, technicians, assembly line workers, and users of virtual reality interfaces there is a need for high resolution displays which are light, power efficient, and easily interfaceable with computers or other embedded microprocessors. Military personnel in a battle field or in an armored vehicle, fighter pilots maneuvering at high speeds may also use see-through displays which will enable them to access vital information without having to look at a conventional monitor away from their line of sight. These displays are commonly referred to as helmet mounted displays (HMDs). SOI technology is presently being used for the fabrication of both active matrix liquid crystal displays (AMLCD) and active matrix electroluminescent (AMEL) displays for helmet mounted applications. While AMLCDs are more power efficient and currently offer full color capability, AMEL displays are more rugged and offer wider viewing angles for direct view applications [11-13]. Full color AMEL displays are currently in development.

Active matrix addressing scheme offers faster response time, and reduced cross-talk among pixels as compared to the passive matrix approach. In an active matrix design, each pixel contains one or more transistors, which act(s) as highly non-linear on-off switch. Until recently, all the research efforts towards active matrix displays used amorphous silicon or poly-silicon thin film transistors (TFTs). However, these transistors suffer from low speed, high leakage current, and uniformity variations from pixel to pixel, which makes them unattractive for fast and high resolution HMDs. Since large area substrates are not essential for HMDs, SOI substrate is a natural choice for these displays.

Dr. Peter Brody and his coworkers at Westinghouse Research Laboratories are the pioneers in AMEL displays [14]. Their work also included fabrication of thin film transistors (TFTs) for active matrix liquid crystal displays. Brody *et al.* reported a functioning 6x6-inch 20-lpi (lines per inch) AMEL display with good brightness and contrast ratio in 1975 [14]. CdSe thin film transistors were used for active area devices. Although the pixel pitch was greater than 1000 μm, their efforts were significant in the early days of

technology development. The pixel circuit configuration of their AMEL display was very similar to that used in today's high resolution AMEL display systems. The research group at Westinghouse also made notable contributions to active matrix liquid crystal displays. They demonstrated successful operation of TFTs for AMLCD applications. The TFTs were fabricated on a wide variety of substrate materials [15].

Although several other research teams have also made significant contribution to the AMEL technology, none of these efforts culminated into a commercial product - mainly due to issues regarding reliability and the isolation of the low and the high voltage devices [16-17]. The requirement for a small area high voltage transistor was also a significant obstacle for the early researchers. Although the feasibility of AMEL displays were demonstrated 20 years ago, commercially available displays are yet to become a reality.

An electroluminescent device consists of light emitting phosphor layer(s), which is usually ZnS or SrS, sandwiched between two layers of insulator. The phosphor layer is doped with activators, such as Mn or rare earth atoms. The device is then placed between two conducting layers and an alternating voltage is applied between the two conducting plates. When the electric field within the device reaches high enough values due to the applied voltage, the electrons residing at one of the insulator/phosphor interface states are accelerated. Electrons with high kinetic energy impact excite the activators. These activators, also known as the luminescent centers, return to their original stable states upon de-excitation, thereby emitting light at certain wavelengths depending on the allowed electronic states of the activator atoms. It should be noted that the voltage required to "turn on" an EL device is usually higher than 120 V.

All the AMEL pixel circuitry are based on the two-transistor cell concept, where a low voltage transistor is used to store the digital data at the hold node which in turn controls the high-voltage transistor [11]. The hold node is connected to a storage capacitor and also to the LDMOS gate. The high voltage lateral double diffused MOS

(LDMOS) transistor is placed in series with the EL material and thus decides whether a particular pixel is "on" or "off." This LDMOS structure is discussed in detail in section 3.1.1 of this thesis. Figure 1-3 shows the circuit schematic of an AMEL pixel. Each pixel is addressed by a data and a select line. High speed peripheral CMOS devices are also integrated in the same die for fast addressing of individual pixels, geared towards video applications with 64-bit temporal gray scale [11].

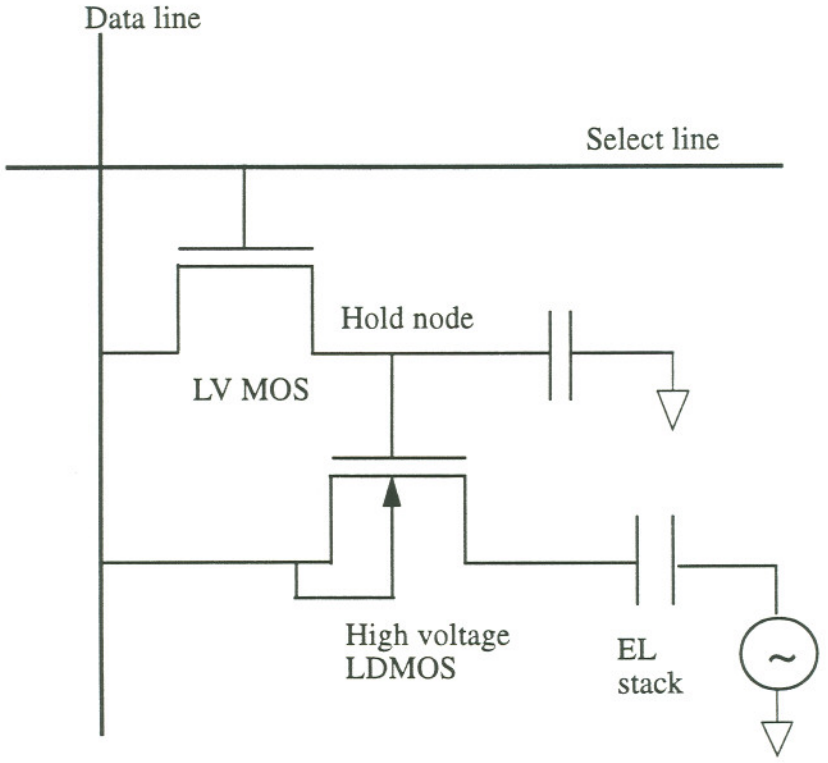

Figure 1-3: The single pixel circuit for AMEL display

As mentioned in the previous paragraph, the pixel is either on or off depending on the blocking voltage of the high voltage transistor. The pixel period is divided into two sub-periods: Load and Illuminate [13]. In the load cycle, high-voltage AC is off and a

logic '1' or '0' is written at the hold node using appropriate select and data pulses. The select line is pulled high such that the access transistor is on and then the hold node is either charged ('1') or discharged ('0') through the access transistor. After the information is loaded into the hold node of the pixel, both select and data lines are grounded and high voltage AC is applied during the Illuminate cycle. If a logic '1' is written at the hold node, which is also connected to the LDMOS gate, the LDMOS operates in the linear regime and essentially creates a low voltage path to ground. As a result, the applied AC voltage is dropped across the EL material, causing light emission. On the other hand, if the pixel is off, the drain of the LDMOS transistor is held at the breakdown voltage and the voltage drop across EL is not sufficient to cause light emission. Usually, EL devices are driven at 40 volts (also known as the modulation voltage) above the threshold voltage of the device. It has been demonstrated that in the off-state if the high voltage device blocks at least 80 volts or twice the modulation voltage of the EL material, good contrast between the on- and off-pixels can be obtained, as shown in Fig. 1-4. A detailed explanation of this subject matter can be found in reference 11.

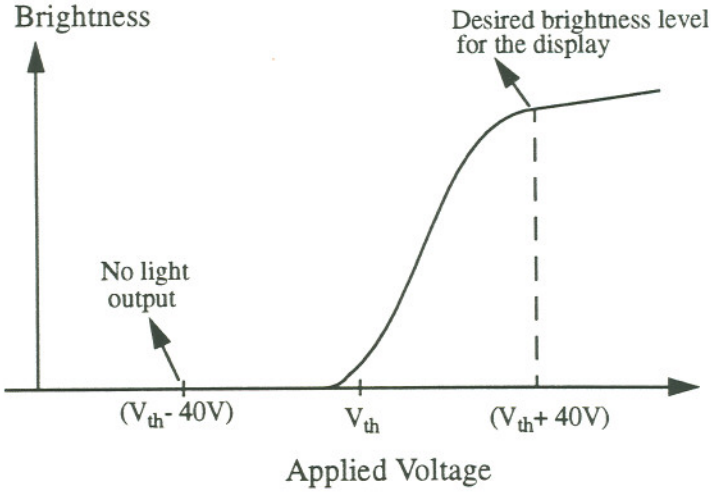

Figure 1-4: Good contrast is achieved by blocking the modulation voltage

The challenge in manufacturing AMEL displays lies in the design of high voltage devices that can be placed within the small dimensions of the pixel. One of the primary goals of this thesis is to design and experimentally demonstrate the feasibility of high voltage short drift region LDMOS transistors. The isolation of low- and high-voltage components of the pixel circuitry is also equally important as the application of high voltage pulses can cause significant amount of capacitive coupling among the circuit components in the active area of the AMEL display. Careful layout of the pixel is crucial to avoid such effects. It should be noted that the ease of isolation in the active area circuitry is probably the single most important reason behind the choice of expensive SOI substrates.

The successful operation of 1280x1024 AMEL pixel arrays with 24 μm pitch has already been demonstrated [11-13]. In this dissertation, the focus is on the design and fabrication of devices for high resolution AMEL displays with pixel dimensions as small as 12x12 μm^2. The motivation for the reduction in the pixel geometry was the enhancement of the resolution of the current AMEL technology.

1.3 Dissertation Overview

This thesis has been organized into six chapters including this introduction. Chapter 2 contains a review of the present state of the SOI technology and describes the substrates used in this investigation. A short discussion regarding the pros and cons of partially and fully depleted SOI substrates is also included. Electrical measurements conducted on devices fabricated on different SOI substrates to obtain important material parameters such as mobility, interface states density, minority carrier lifetime, and generation lifetime are presented. Such parameters are important for device design considerations. For example, minority carrier lifetime plays a significant role in determination of bipolar gain and mobility is directly proportional to the amount of drive current a device

can supply to charge a capacitive load. Chapter 3 is devoted to the design issues regarding high voltage devices on SOI substrates and their specific applications in AMEL displays. Experimental results are also presented including the near ideal breakdown voltage performance from a short drift region lateral double diffused MOS structure. Design trade-offs and short drift region DMOS design is discussed in detail. Chapter 4 details the high temperature behavior of the low voltage CMOS and high voltage DMOS devices. Threshold voltage, mobility and leakage current as functions of temperature are analyzed and compared with the results predicted by simple analytical expressions used to describe MOS devices. Hot electron damage, an important reliability hazard for short channel MOS devices, is discussed in chapter 5. Using accelerated test methods, physical mechanisms for device degradations are identified and device lifetimes for partially depleted (PD) SOI structures are obtained. Using charge pumping method the hot carrier damage is quantified in terms of generated interface state density. In chapter 6, conclusions are drawn and suggestions for future research on this interesting topic are discussed.

Although some portions of this dissertation specifically deal with issues and problems related to the AMEL displays, a significant portion of this work is geared towards partially depleted SOI substrates and devices.

Chapter 2

SOI Substrates

2.1 SOI Manufacturing Techniques

The advantages of fabricating semiconductor devices on top of an insulating film have been well known. In fact, Lilienfeld filed a patent application in 1926 for a "method and apparatus" for solid-state amplifier, which may be considered the first transistor ever patented [18]. Lilienfeld's amplifier was made of "non-single crystal semiconductor film deposited on an insulating substrate." However, the revolution in the electronics industry was caused by the development of the single crystal silicon (Si) growth and processing technology. Ironically, as the bulk Si technology reaches its limit, there is a renewed effort to create high quality single crystal films on top of insulating substrates for a variety of potential benefits for both low- and high-voltage ICs. Although researchers have employed a plethora of techniques for obtaining SOI substrates, it was only recently that high quality SOI wafers have been commercially available.

There are many ways to produce a single crystal Si film on top of an insulator. The most obvious choice involves epitaxial growth of single crystal Si on a lattice matched crystalline insulator. Sapphire, Cubic-Zirconia, Spinel are some of the crystalline insulators that have been used for this application. However, silicon-on-sapphire (SOS) is the only mature technology with limited applications in radiation hard devices for military and space explorations [19].

Researchers have developed technologies which employ (re)crystallization of

poly- or amorphous-Si films. All these methods involve crystallization of deposited poly or amorphous Si by melting the film with a high energy laser or electron beam. In the zone melting recrystallization (ZMR) technique, a strip heater is used to obtain lateral growth of a single crystal film [20]. A modified and improved version of the ZMR technique is commonly known as ISE or Isolated Silicon Epitaxy. Homoepitaxial techniques such as epitaxial lateral overgrowth (ELO) and lateral solid phase epitaxy (LSPE) have also been reported [21-22]. Interesting process techniques such as Full Isolation by Porous Silicon (FIPOS) takes advantage of very high oxidation rates of porous Si films as compared to a layer of bulk Si [23]. Porous Si film is created by the electrochemical dissolution of p-type Si in HF acid solution. An n-type layer, which will form the SOI island, is protected from the HF by a deposited Si_3N_4 mask.

The two most promising SOI technologies, however, avoid any form of epitaxial growth. The technology considered most promising for the low voltage USLI applications uses oxygen implantation into a standard bulk Si wafer to create a layer of insulating silicon oxide (SiO_2) film; hence, the name SIMOX or Separation by IMplanted OXygen [24]. For thick (> 0.5 μm) buried SiO_2 layers, BESOI (Bonded and etched-back SOI) substrates are considered to be the most promising material for commercial applications, specially in the "smart-power" IC market.

In this chapter, three commercially available SOI wafer manufacturing techniques (SIMOX, BESOI, and ZMR) are reviewed, along with the relative advantages and disadvantages of each technology. In the second part of this chapter, important electrical characteristics of devices fabricated on some of these substrates are measured. From the measured data important material parameters such as the minority carrier lifetime and mobility have been extracted. Interface trap densities at the back and front interfaces have been compared for both ISE and SIMOX substrates. It should be noted that the traps present at the oxide interfaces play an important role in determination of the threshold voltage of a MOS device. Large number of defects in the interfaces may also severely

reduce carrier lifetime and mobility, affecting the current driving capability of the device.

2.1.1 SIMOX

The acronym SIMOX was first coined by Izumi *et al.* at NTT, Japan [24]. The processing steps involve a high dose implantation of oxygen at a prescribed depth below the Si surface, followed by a high-temperature thermal anneal cycle, as shown in Fig. 2-1. Since two oxygen atoms are needed for every Si atom for a continuous SiO_2 layer, the minimum dose required for creating a continuous buried oxide layer can easily be calculated by using the following equation:

$$\text{Implant Dose} = 2\ (t_{box})\ (\text{Atomic conc. of Si}) \qquad (2.1)$$

where t_{box} refers to the buried oxide thickness. According to the above mentioned equation, the ideal dose should be $1x10^{18}$ cm^{-2} for a buried oxide thickness of 0.1 μm. Unfortunately, higher doses are required in order to obtain a flat topped implantation profile instead of a typical skewed gaussian type distribution. The implantation must also be performed at an elevated temperature (500-600° C) to maintain the crystalline quality of the top Si film. On the other hand, if the implantation temperature is higher than 700° C, SiO_2 precipitates may form near the Si-SiO_2 interface.

It has been determined that $1.4x10^{18}$ cm^{-2} is the critical dose for formation of a continuous buried SiO_2 layer at 200 keV beam energy. This dose requirement (~$1.4x10^{18}$ cm^{-2}) is also known as the "critical dose" [3]. Presently, most commercial manufacturers use a 150-200 keV beam with a total dose of 1-$2x10^{18}$ cm^{-2}. For many years the high dose requirement was the principal obstacle for producing high quality buried oxide layers. Conventional implanters used in the semiconductor industry for channel or source-drain implants will have very low throughput for such high doses. High-current implanters,

with beam currents higher than 200 mA, had to be developed to meet the requirements for such a demanding task [25].

Post-implant thermal treatment must be preformed for two primary reasons. The thermal treatment anneals out the crystalline damage to the top Si film. Secondly, during the thermal cycle, the oxygen atoms still present in the Si film are diffused and incorporated into the buried oxide layer. Thus a monocrystalline Si film is formed over a buried oxide layer. Post-implant anneals are usually performed at temperatures higher than 1300° C. Researchers at AT&T have performed annealing at 1405° C to obtain precipitate-free SOI substrates with smooth oxide interfaces and carrier mobilities very close to bulk-Si [26]. A special high intensity halogen lamp system was used to keep the backside of the wafer at 1412° C, the melting point of Si.

The quality of SOI layer has been improved further by adopting a multiple implant scheme. The defect density of the SOI layer decreases significantly if the implant dose is kept below the value of the critical dose. Therefore, in the multiple implant scheme the "implant and anneal" cycle is repeated several times. While each implant step receives a lower dose than the critical dose, the total dose eventually exceeds the critical dose for a continuous oxide layer formation. As a result of lower dose and multiple annealing cycles, the dislocation density in the Si film decreases significantly and the Si islands in the buried oxide disappears. Multiple implant also helps to obtain a sharper Si-SiO_2 interface.

For low voltage, deep sub-micron ($L_{eff} < 0.25\ \mu m$), high speed CMOS applications ultra-thin SOI layers with thin buried oxide (t_{si}~400-600Å, t_{box}~500-2000Å) are required. For such applications, a low energy and low dose multiple implant procedure has been developed. Low dose implants are not only cheaper, but also reduce contamination in the SOI film since the concentrations of carbon and other heavy metal contaminants are proportional to the implant dose. With the availability of implanters capable of producing beam currents higher than 200 mA, it is expected that the price of an eight inch

wafer will become comparable to a similar sized prime quality bulk wafer with an epi film, often used in twin-well high density CMOS applications. However, the number of defects in the form of pinholes in the buried oxide and dislocations in the SOI film due to silicon precipitates at Si/SiO_2 interface still remains a concern for chip manufacturers interested in using SIMOX wafers for commercial ICs [27].

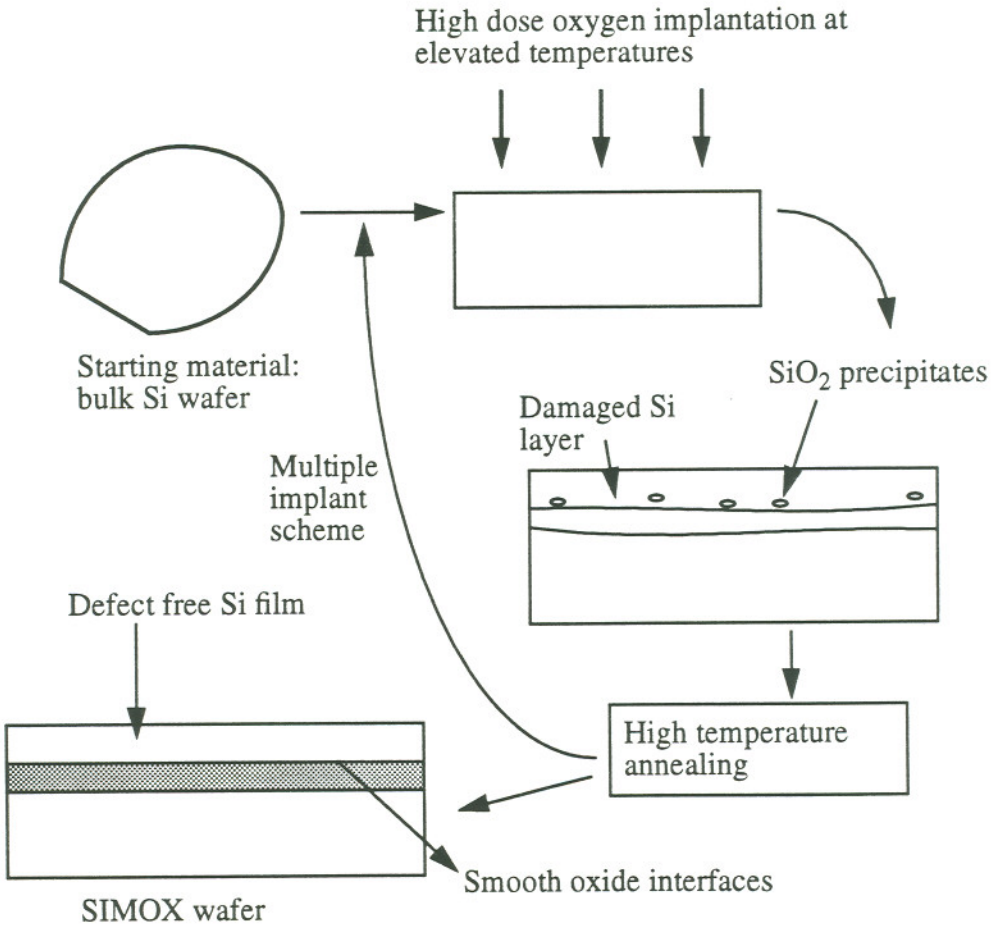

Figure 2-1: Manufacturing of SIMOX Substrates

2.1.2 ZMR

In the ZMR process, a deposited amorphous or poly-Si film on SiO_2 is (re)crystallized using the same technique used in the float zone method for high quality bulk-Si wafer production. The method was pioneered by the Lincoln Laboratory at MIT in the mid-1970s. An improved version of this technique was commercialized in the late eighties and is now known as Isolated Silicon Epitaxy (ISE) [27].

The process starts with the wet oxidation of a single crystal bulk-Si wafer. The pin-hole free thermal oxide is usually 1 μm or thicker, depending on the particular device applications [20]. The oxide is then removed from the perimeter of the wafer and an amorphous or poly-Si film is deposited using low pressure chemical vapor deposition (LPCVD). The whole stack is then capped with low temperature oxide (LTO) followed by a Si_3N_4 deposition. The wafer is placed on a substrate holder which is heated up to 1200° C in an inert atmosphere. A graphite strip heater is then used to crystallize the top Si layer. The heater, placed 40 to 80 mils above the surface, is heated up to 2200° C. The Si at the edge of the wafer acts as a seed for the epi-layer growth. The poly at the edge of the wafer is in contact with the underlying silicon substrate and as the poly melts a substrate seeded growth occurs. As the strip heater moves across the wafer, the lateral growth continues with the same orientation as the original substrate, as shown in Fig. 2-2.

Finally, the capping layers above the recrystallized single crystal film is removed. These layers not only protect the wafer from possible carbon and other metal contaminants, but also act as a barrier to thickness variations and prevents the molten silicon from beading up. Some of the important parameters for recrystallization include the distance between the wafer and the heater, the scan speed, and the deposited poly thickness. A slow scan speed combined with a thick (>0.5 μm) poly layer give the best results. On the other hand, a thin poly with a fast scan speed results in poor crystalline quality [27].

Thickness variations across the wafer affects threshold voltage and subthreshold slope, two important device parameters. Unfortunately, two types of thickness fluctua-

tions are commonly observed in commercial ZMR wafers [3]. Even with a capping layer, limited amount of mass transport in the scan direction causes the SOI layer to be thinner at the side where recrystallization starts as compared to the other end.

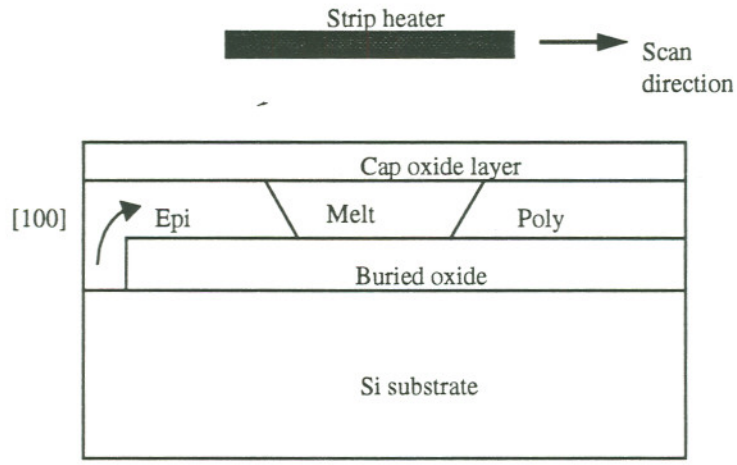

Figure 2-2: SOI film formation - the lateral movement of the melt front

(after Zavracky *et al.*, [27])

Another ZMR drawback is the short range waviness, caused by the finite stiffness of the capping layer. This phenomenon is the result of a meniscus formation at the surface of the liquid silicon [3]. The surface tension equilibrium along the cap layer, solid and liquid Si is also responsible. This short range waviness, shown in Fig. 2-3, can be associated with sub-grain boundaries in the form of dislocations in the SOI film. The periodic, parabolic shaped wave patterns usually have 20 nm of peak to peak thickness variation, limiting possible applications of ZMR wafers only to thick film devices (> 0.3 μm) for high voltage operations.

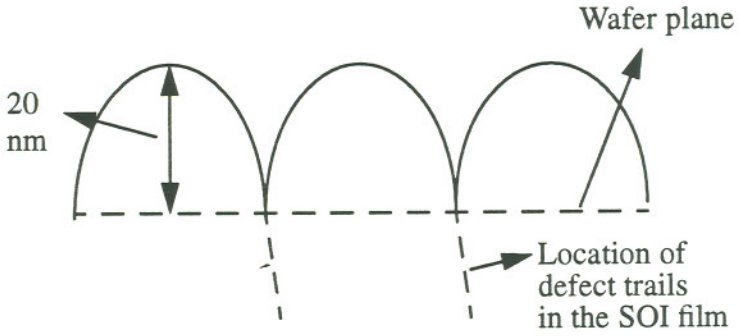

Figure 2-3: Short range waviness seen in ZMR wafers

(after Colinge, Silicon-on-Insulator Technology: Materials to VLSI, [3])

2.1.3 BESOI

Conceptually, BESOI manufacturing technique is the simplest among the ones discussed so far. Two oxidized wafers are "bonded" together with or without externally applied forces. The top piece, also known as the seed wafer, is then etched back to obtain a thin SOI film. However, a proper understanding of the bonding mechanisms and defect removal in the bonded SOI films are still the focus of intense research and development in laboratories around the world. This technique can also be applied to bond different semiconductor materials on the same wafer without resorting to heteroepitaxial growth.

Bonding technology started with the use of external forces, which can be applied in the form of high temperature, pressure and high voltage electrical pulses. In 1985 Lasky *et al.* pioneered the technique of room temperature bonding followed by a high temperature thermal anneal [28]. A recently published article reviewed the rules vital to a successful bonding, originally described by Lord Rayleigh and still applicable to modern wafer bonding technology [29]. The four main points are summarized in the next paragraph.

The presence of particles on the bonding surfaces may have severe detrimental

effects on the process. The temperature of the bonding pieces must be kept as close as possible. Thinner pieces have better bonding strength since they can adapt more easily to each other's shape. The distance (10-15Å) between two pieces of silica bonded at room temperature does not change if additional stress or pressure is applied.

The basic bonding process comprises of four process steps [30]:

1. Wafer preparation: This step usually involves formation of an etch stop or polish stop in the seed wafer, and the deposition or growth of insulating layers on one or both wafers.
2. Bonding: At this point, the seed wafer (the top piece) and the handle wafer (the bottom piece) are actually joined together at room temperature.
3. Thermal annealing is performed to strengthen the bond between the wafers.
4. In order to achieve the desired SOI film thickness, the seed wafer is lapped, etched and/ or polished.

Figure 2-4 illustrates the major process steps involved in the wafer bonding process.

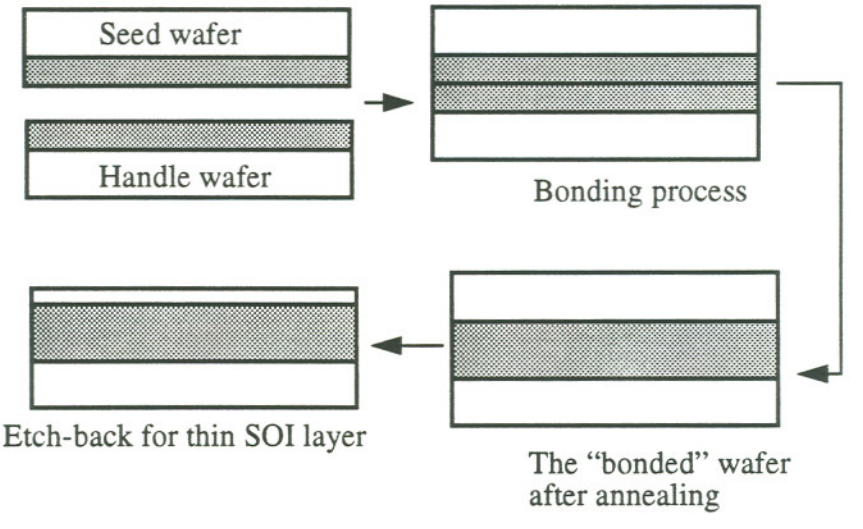

Figure 2-4: Bonding wafer manufacturing: the basic process steps

When two oxidized Si wafers are placed against each other, the bonding occurs due to the attraction between the hydroxyl groups (OH^-) adsorbed on the two surfaces. This attraction may cause spontaneous formation of hydrogen bonds between the wafers. However, if the wafers are dried after oxidation, the bonding may not take place. Once the wafers are bonded at room temperature, a thermal anneal cycle is performed to strengthen the bond. The bonding kinetics show three different phases which is a function of the annealing temperature. The first phase, observed at low temperatures (up to 300° C), is dominated by the hydrogen bonds. In the second phase, a Si-O-Si bond is formed and this phase may extend up to 1000-1100° C. At the intermediate temperatures, elastic wafer deformation is observed and thermal vibration of molecules increases. At higher ambient temperatures, a viscous or plastic flow of SiO_2 completes the final bonding of the seed and the handle wafer.

Once the bonds between the seed and the handle wafer has been established, the bonded wafer must be further processed in order to obtain a thin SOI layer for device processing. The selective wafer thinning process involves a built-in polish or etch-stop in the seed wafer. Double etch-stop technique has been able to produce ultra-thin SOI wafers with 100±10 nm Si film thickness. A relatively new process, called plasma-assisted chemical etch (PACE) was developed by researchers at Hughes and is currently used in commercial wafer production [31]. A high pressure plasma is used to etch the Si film at high etch rates with thickness variations less than 10 nm across the Si wafer. *In situ* thickness measurement data is used to control the etch process. Usually a boron doped p^+ layer is used as an etch stop. However, B contamination remains a major problem for some of the BESOI wafer manufacturers.

There are two types of voids generally observed in BESOI wafers. Intrinsic voids are caused either by the outgassing of surface contaminants (mainly hydrocarbons) or the water vapor formation by the Si-OH+OH-Si -> H_2O+Si-O-Si reaction. Both these mech-

anisms occur around 200° C. Fortunately, these intrinsic voids disappear at higher annealing temperatures. The extrinsic voids are mostly due to particles trapped between the bonded surfaces. A 1μm diameter particle can generate a void as large as several millimeters in diameter. The extrinsic voids are usually immune to annealing, necessitating the use of ultra-pure chemicals and water in an ultra-clean processing environment.

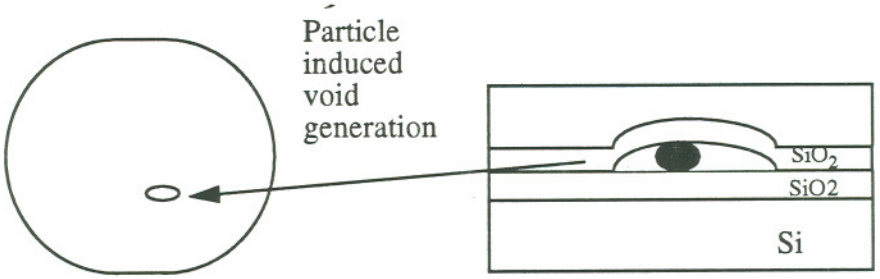

Figure 2-5: Creation of voids in the SOI film

(after Colinge, Silicon-on-Insulator Technology: Materials to VLSI [3])

For power device applications, thicker buried oxide layers are necessary (> 2 μm) to obtain the optimum breakdown voltage performance. However, it is difficult to create a thick buried oxide layer using SIMOX technique. Although SIMOX remains a material of choice for low power, high-speed, deep sub-micron technologies, BESOI and ZMR wafers are the more likely choices for high voltage, "smart-power" IC applications.

2.2 Fully Depleted (FD) vs. Partially Depleted (PD) SOI Substrates

A review of SOI technology will not be complete without discussing the merits and demerits of the fully and partially depleted substrates, which is a hotly debated topic among SOI technology experts. Although most experts agree that devices fabricated on fully depleted substrates show superior performance, issues regarding manufacturability

are forcing some chip makers to take a second look at the partially depleted substrates.

In a fully depleted device, the SOI film thickness must be less than x_{dmax}, the maximum depletion width for a MOS structure. The maximum depletion width can be calculated by using the following expression [32]:

$$x_{dmax} = \sqrt{\frac{4 \cdot \varepsilon_{Si} \cdot \Phi_F}{q \cdot N_a}} \tag{2.2}$$

where N_a is the substrate or channel doping, ε_{Si} is the permittivity of Si, and Φ_F is the substrate Fermi potential expressed by $\frac{kT}{q}\ln\frac{N_a}{n_i}$, where n_i is the intrinsic carrier concentration. SOI wafers with film thicknesses higher than x_{dmax} are known as the partially depleted substrates.

The biggest advantage of fully depleted MOS devices is the absence of the floating body, which causes the kink effect in the IV characteristics and lowers the forward bias breakdown voltage of the device. In a partially depleted NMOS device, high drain bias causes impact ionization at the channel-drain junction due to the high electric field in the region. The holes, due to the positive biases at the drain and the gate of the device, move to the body-source junction. Unlike a similar bulk device, these holes cannot move to the substrate contact due to the buried oxide layer and raise the potential of the body (channel) of the device. Fig. 2-6 illustrates the events that lead to the "kink" effect in partially depleted SOI MOS devices.

Eventually, the reverse biased body-source junction becomes forward biased due to the accumulation of holes in the body of the transistor, causing additional electron injection from the source. This additional carrier flow shows up as a kink in the I_{DS}-V_{DS} curve, as shown in Fig. 2-7. The "kink" is difficult to model using a SPICE-type circuit simulator due to the complex nature of this phenomenon. For analog applications, this

effect also causes a reduction in the device gain. Although a body contact can be used to eliminate the floating body related kink effect in partially depleted devices, it is not an attractive option due to the additional area requirements for the body contact. However, for digital applications, additional drive current may be beneficial as long as the effect can be properly modeled.

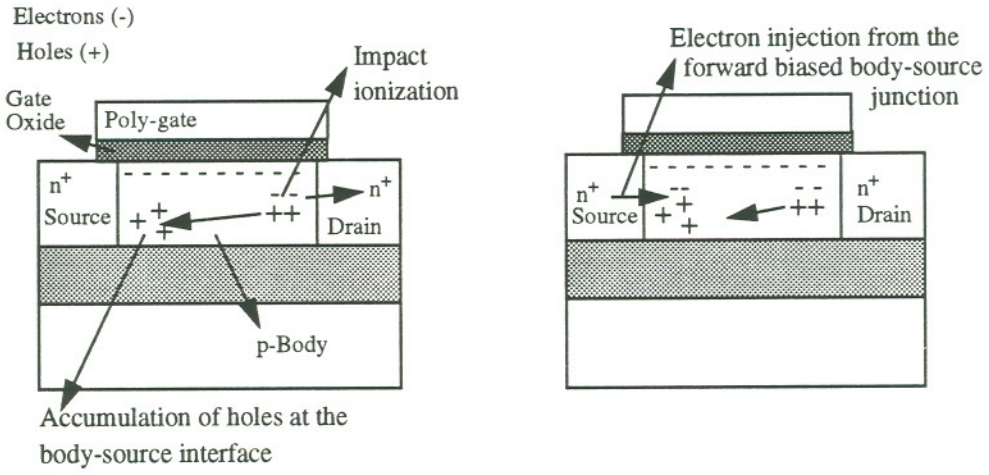

Figure 2-6: Phenomenological model of the "Kink" effect in PD SOI Devices

In a fully depleted device, the influence of the gate bias over the channel potential is greatly enhanced [33]. Thus fully depleted devices show less short channel effects (SCE) such as V_{th} roll-off. Near-ideal subthreshold swings (S) have been obtained in such thin film devices. As the SOI film gets thinner, subthreshold swing S approaches 60 mV/ decade, which is the ideal value for MOS devices. Thinner SOI films also provide better punchthrough protection, negating the need for higher substrate doping. High substrate doping leads to mobility reduction and higher electric fields within the device.

The decrease in the vertical electric field also leads to mobility enhancement.

Researchers at Toshiba have extracted a mobility of 900 cm^2/Vs from a fully depleted SOI (t_{soi}~350Å) device as compared to 650 cm^2/Vs, obtained from an identical bulk counterpart [33].

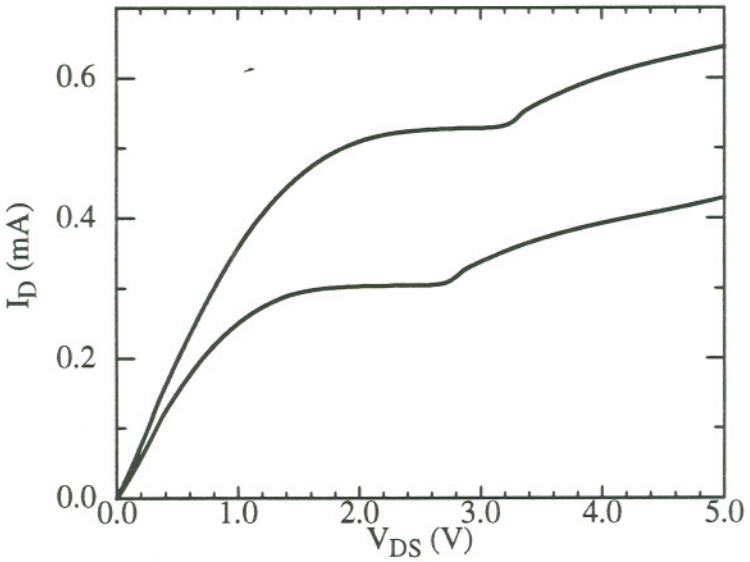

Figure 2-7: "Kink" effect observed in an SOI NMOS device (W/L=10/3 μm)

The absence of the kink effect in a fully depleted device can be attributed to two effects. Firstly, the reduction of the electric field near the channel-drain junction causes less impact ionization and hole generation in the channel. Secondly, the hole potential barrier at the channel-source junction is significantly smaller. Thus, the holes can easily be transported into the source and recombine without causing any electron injection into the body.

Shahidi *et al.*, however, point out that the reduction in threshold voltage roll-off in submicron fully depleted devices is caused by the shallower junction depths and not inherent to the fully depleted structures [34]. A bulk device, with similar ultra-shallow

junctions (< 500 Å), will have better SCE. They also mention that the reduction in the floating body effect is very sensitive to the film thickness and a 5-10 nm variation in the film thickness brings back the floating body effect. The floating body effect manifests itself in the form of device leakage that cannot be turned off.

The SOI film thickness must be well below x_{dmax} in order to reduce the V_{th} sensitivity to the SOI film thickness. Unfortunately, this results in unacceptably low V_{th} for the device. A higher substrate doping, which will increase the threshold voltage, will cause the device to operate in the partially depleted mode and is not an acceptable solution to the problem at hand. Based on these issues mentioned above, the researchers at IBM prefer partially depleted thin SOI devices [34]. They argue that if the film thickness is around 0.1 μm, it is possible to create highly retrograde non-uniform channel doping and V_{th} sensitivity to film thickness can be eliminated. The kink effect may not be suitable for analog applications but the excess current generated by the floating body may turn out to be advantageous for digital applications. The "kink" can also be reduced by the use of a lightly doped drain (LDD) structure, which reduces the electric field near the drain-channel interface. This comes at the expense of increased source-drain series resistance of the MOS device.

SOI technology is still evolving and one cannot say for sure which of the two, fully or partially depleted substrates, will be the material of choice for future generation devices with channel lengths as short as 0.1 μm. The quality of the SOI wafers, in terms of uniformity of the film thickness and defect density, will play a major role in settling such matters of interest.

2.3 Electrical Properties of SOI Substrates

In this section, some important material parameters are extracted from the electrical characteristics of MOS devices fabricated on various types of SOI substrates [35-

36]. The extracted parameters include field-effect mobility, minority carrier lifetime, generation lifetime, subthreshold slope, and interface trap density. These extracted parameters are compared to bulk values and previously published values for various SOI substrates. The objective of this exercise is to obtain a general picture of today's SOI technology.

2.3.1 Mobility

Mobility is a material parameter that indicates how strongly the motion of a carrier (electron or hole) is influenced by the applied electric field [32]. In a bulk semiconductor, mobility is a strong function of temperature and dopant concentrations which determine the scattering rates during carrier transport. For MOS devices, mobility is also affected by surface scattering as the conduction takes place only in the thin inverted channel region underneath the gate oxide. The vertical electric field is also responsible for mobility degradation at high gate voltages. The field effect mobility (μ_{FE}) can be extracted from the I_D-V_{GS} curve using the following equation:

$$\mu_{FE} = \frac{\partial I_D}{\partial V_{GS}}\left(\frac{L}{W}\right) \cdot \frac{1}{C_{OX}} \cdot \frac{1}{V_{DS}} \tag{2.3}$$

where I_D refers to the drain current and V_{GS} is the gate-to-source voltage. C_{ox} is the gate oxide capacitance per unit area and V_{DS} refers to the small applied drain to source bias. Field effect mobility, extracted from a MOS I_D-V_{GS} curve, is usually smaller than the bulk mobility mainly due to surface scattering effects.

The surface mobility μ_o can be expressed as a function of the interface trap density [37]:

$$\mu_o \sim \frac{1}{(1+\alpha_1 D_{it})} \tag{2.4}$$

where D_{it} is the interface defect density and α_1 is an empirically determined constant ($\sim 0.2 \times 10^{-11}$ $cm^2 eV^{-1}$). Although the mobility values extracted from MOS current-voltage characteristics are lower than the ideal mobility, mobility extraction is routinely carried out in parametric testing of devices as it can reveal process and material related interface defects.

Electron mobilities for the back (at the buried oxide interface) and the front (at the gate oxide interface) channel were extracted from NMOS transistors fabricated on commercially available ISE and SIMOX wafers. The measured μ_{FE} values are presented in Table 2.1. It should be noted that the mobility values are slightly lower than previously published results due to somewhat higher channel doping concentrations of the measured devices [38].

Table 2-1: Front Channel (FC) and Back Channel (BC) Electron Mobility

Material type	FC mobility (cm^2/Vs)	BC mobility (cm^2/Vs)
ISE	558	566
SIMOX	584	595
SIMOX [38]	630	350
NMOS-Bulk [35]	610	-

Excellent cross-sectional transmission electron microscope (XTEM) photographs of buried oxide interfaces have been published, indicating that the back oxide interface is

comparable to that of high quality gate oxide on an atomic scale [38]. However, back channel mobility values have always been worse than that of the front channel [38-39]. Our results from the devices fabricated on commercial SIMOX and ISE wafers are significant in that respect as they indicate the recent progress made in the wafer manufacturing technology.

The mobility values in Table 2-1 are strong indications of a mature SOI wafer manufacturing technology. It is interesting to note that the front and the back gate mobilities are very close, indicating a buried oxide interface without any major defects. During the fabrication of the test chip an anneal cycle was used to drive-in the implanted impurities in the transistor body. Therefore, It is possible that the back channel has a lower doping concentration as compared to that of the front channel, leading to an improvement in the back channel mobility values.

2.3.2 Subthreshold Slope

Subthreshold slope may be used to understand more about the Si-SiO_2 interface quality. The subthreshold slope indicates how fast an MOS device can be turned on from the off state. Device physicists often use S or the subthreshold swing, which is the inverse of the slope, as a figure of merit for high speed MOS transistors. For a partially depleted device, S can be theoretically calculated from the following expression [37]:

$$S = \left(\frac{d}{dV_G} log_{10} I_D\right)^{-1} = (2.3)\left(\frac{kT}{q} \cdot \frac{C_{ox} + C_d + C_{it}}{C_{ox}}\right) \qquad (2.5)$$

where C_{ox}, C_d, and C_{it} refer to the capacitances per unit area due to the gate oxide, depletion under the gate, and the interface traps, respectively. The interface trap capacitance C_{it} is simply qD_{it}, where D_{it} is the number of interface traps per unit area per unit energy.

In this section, the subthreshold swing S at both the front and back channel has been experimentally determined. For this experiment, we used an edgeless device in order to eliminate the effect any edge parasitic may cause. Fig. 2-8 and 2-9 show the subthreshold characteristics of both edge and edgeless devices. The 'bump' in the edge device is the result of the lower 'turn-on' or threshold voltage of the parasitic device. However, in the moderate and strong inversion regime, the current from the parasitic is significantly lower than the actual device since the parasitic device width is significantly smaller than the drawn channel width.

Fig. 2-10 shows the layout of both types of device structures and the exact location of the parasitic "edge" device. The lower threshold of the edge devices can be caused by several factors. Boron depletion near the sidewalls during the field oxide growth is primarily responsible for this phenomenon. Additionally, charge sharing between the parasitic and the actual device may result in a lower V_{th}. Difference in the number of interface trap density at the "gate" of the parasitic device, due to a different crystalline orientation of Si at the sidewall Si-SiO_2 interface, may also contribute to a lower threshold voltage. The use of an edgeless device in this experiment makes it convenient to extract the subthreshold swing S of the 'actual' device.

Both the ISE and the SIMOX wafers were subjected to the same process conditions. Therefore, the value of the depletion capacitance can be considered to be the same with the number of interface states determining the difference in the values stated in the table. The capacitance values in Table 2-1 are indicative of a small number of interface states.

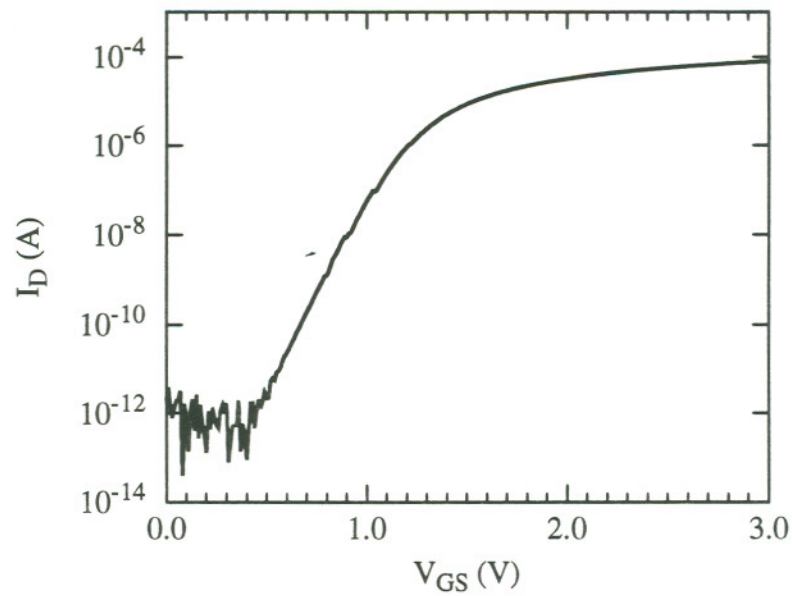

Figure 2-8: Subthreshold slope of an edgeless device (L=2 μm) on SIMOX.

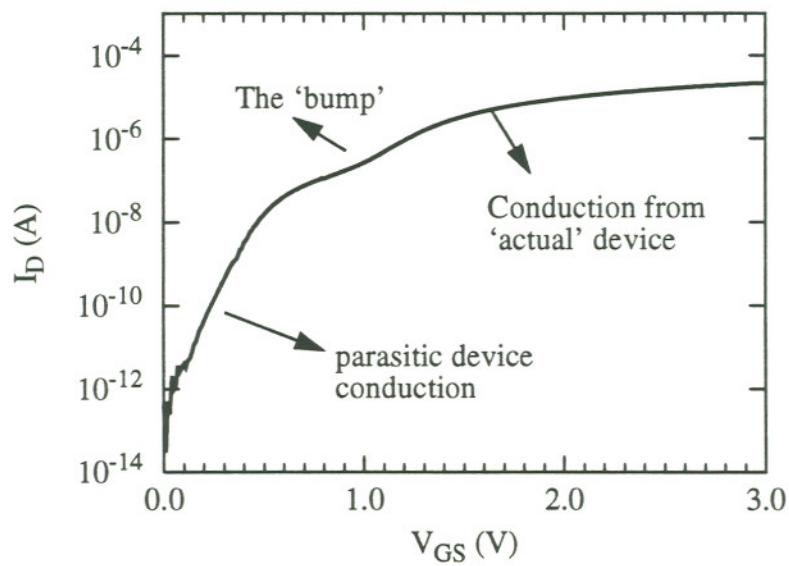

Figure 2-9: Subthreshold slope of an edge device (L=3 μm) on SIMOX

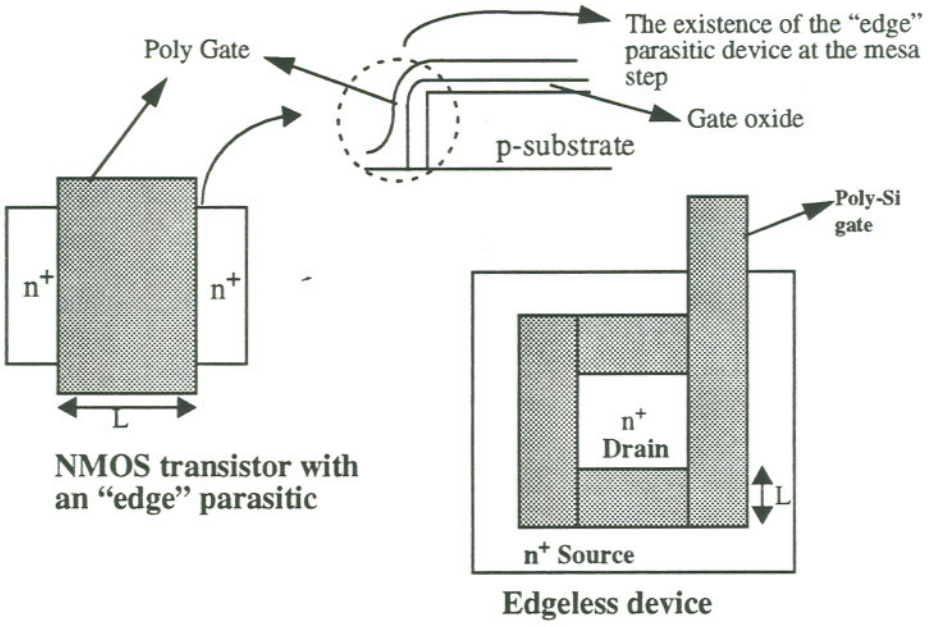

Figure 2-10: Layout and cross-sectional view of "edge" and edgeless devices

Table 2-2: Depletion and Interface State Capacitance

(From Subthreshold Swing Measurements)

Material type	C_d+C_{it} Front Channel ($10^{-7}F/cm^2$)	C_d+C_{it} Back Channel ($10^{-7}F/cm^2$)
ISE	0.787	1.97
SIMOX	1.37	2.39

A closer look at the numbers reveals that the back oxide has more interface states as opposed to the front gate oxide, as has been observed by other researchers [38]. However, capacitance due to the back interface is not significantly higher than that of the front oxide. Since the number of interface traps is directly proportional to C_{it}, the numbers suggest a back interface without any significant major defects. A charge pumping experiment, described in Chapter 5 of this thesis, can be performed to directly obtain the number of interface traps. However, a contact to the body of the SOI device is essential. Unfortunately, an edgeless device with a body contact was not available in the test chip used in this investigation.

2.3.3 Minority Carrier Lifetime

Minority carrier lifetime τ_n or τ_p is an important material parameter that strongly affects bipolar device characteristics and is inversely proportional to the bulk traps that can act as recombination centers. For example, the minority carrier lifetime (electron life-time) in a p-type semiconductor material may be expressed as [40]:

$$\tau_n = \frac{1}{\sigma_n v_{th} N_t} \tag{2.6}$$

where σ_n is the electron capture cross-section, v_{th} is the thermal velocity, and N_t is the trap density. Low minority carrier lifetime has been a problem area in SOI technologies due to high defect densities.

For this aspect of our investigation, short channel (L_{eff}=1.7, 2.7 μm) NMOS devices with a body contact was used to determine the minority carrier lifetime in commercially available ISE material. The source, body, and the drain contact are biased as the collector, base, and the emitter of a bipolar transistor. The gate of the MOS device is kept at a small negative bias to avoid any MOS turn-on. Using this configuration, we

obtained the Gummel plot and then plotted h_{FE} or beta as a function of the collector current, as shown in Fig. 2-11 and 2-12. In Fig. 2-12, collector current vs. beta for a 2.7 μm L_{eff} device is also included to illustrate the relationship between the gain and the base width of a bipolar transistor.

The beta or small signal gain of a bipolar transistor can be expressed by the following equation [41]:

$$\beta = 2 \cdot \left(\frac{L_n}{L_B} \right)^2 - 1 \qquad (2.7)$$

where L_n is the minority carrier diffusion length and L_B is the base width (in this case the effective channel length of the device). Equation 2.7 is valid when $\beta >> 1$ and emitter efficiency γ is close to 1. Since the source-drain doping concentration is about three orders of magnitude higher than channel doping, the criterion for $\gamma \sim 1$ is satisfied. The electron diffusion length is calculated by knowing that $L_n = \sqrt{D_n \tau_n}$, where D_n and τ_n are the diffusion coefficient and the minority carrier lifetime, respectively. Using Einstein's relationship and extracting the mobility value (530 cm^2/Vs) from the MOS device measurements, D_n and consequently τ_n were calculated.

Using eqtn. 2.7 and the relationship between L_n and τ_n, the minority carrier life-time for electrons in the ISE material was found to be 687 ns (L_{eff}=1.7 μm), which is an impressive number compared to the last published value in this type of SOI substrate (70ns, 1989) [41]. Our results show the improvements in the SOI material technology in the last six years and confirms the view that thin film silicon-in-insulator (TFSOI) BiCMOS technology may play an important role in the realization of Si-based high-speed, low-power communication chips [2].

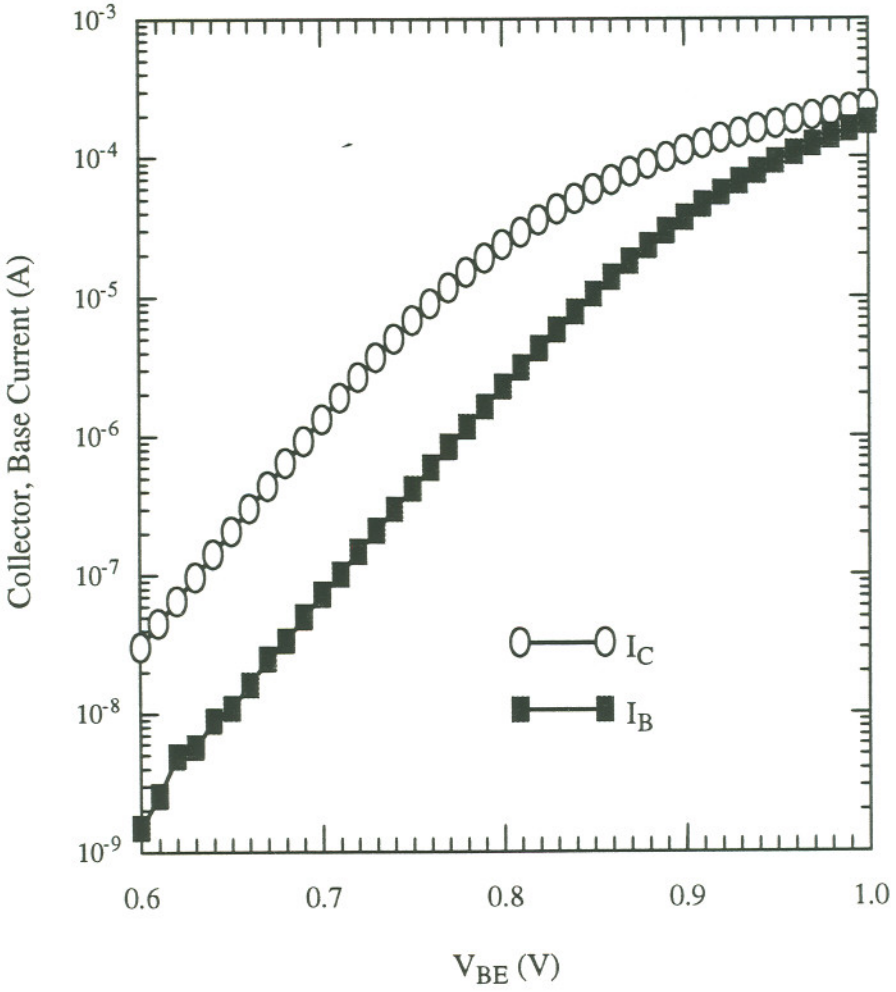

Figure 2-11: The Gummel plot (Base width=1.7 μm)

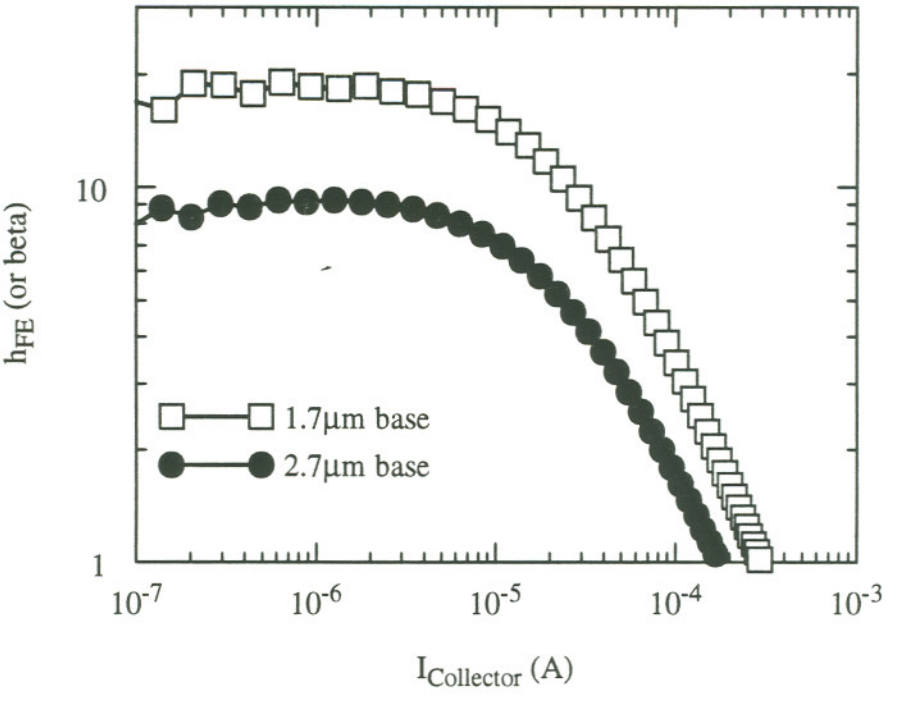

Figure 2-12: Extraction of small signal gain or beta (I_C/I_B)

2.3.4 Generation Lifetime Measurements

Generation lifetime is often used as a figure of merit for SOI material characterization as it points towards the crystalline quality of the Si film. Leakage current in a pn junction, bipolar gain, and the refresh time in a DRAM chip are some of device parameters that are strongly affected by the generation lifetime of carriers [37].

The dual gate nature of MOS transistors fabricated on SOI substrates may be used to measure the generation lifetime within the body of the transistor. This technique, first described by Barth and Angell [42], uses a transient deep depletion effect. The experimental setup for this measurement is shown in Fig. 2-13.

The basic arrangement of our measurement involves biasing the backgate into

inversion at a small drain voltage and establish a steady state current flow in the back channel. The front gate is biased into accumulation. Then the front gate is pulsed into stronger accumulation, resulting in a drop in drain current at the back channel. The transient recovery of the drain current is measured to extract the generation lifetime for the given SOI material.

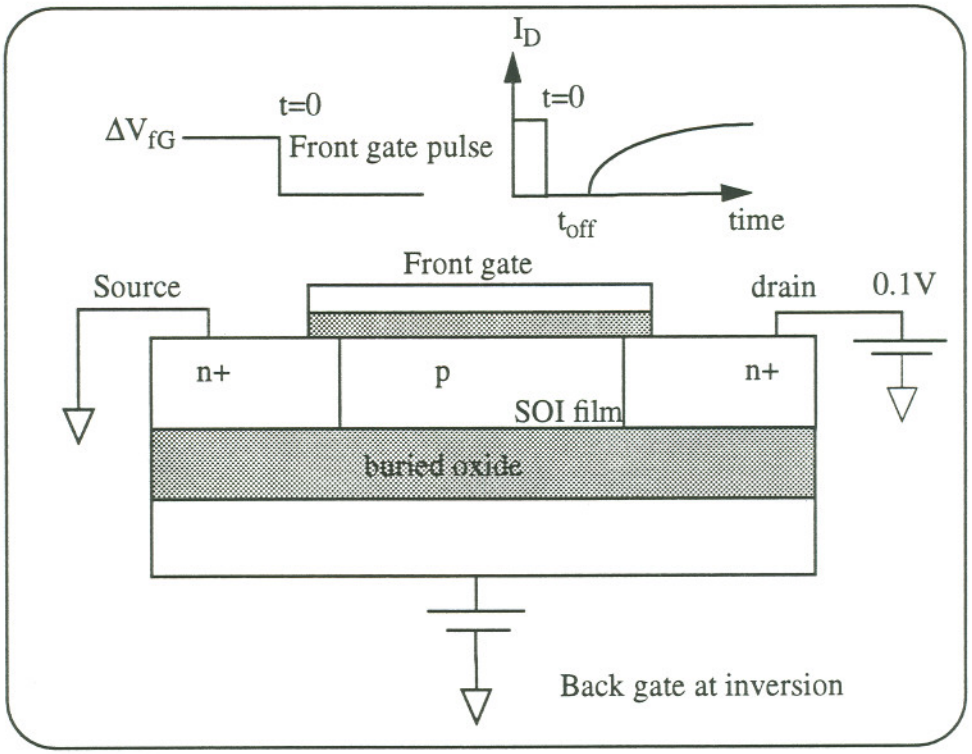

Figure 2-13: Experimental set-up for generation lifetime measurement

Before the application of the pulse at the front gate, an inversion layer exists at the back gate and an accumulation layer is present at the front gate interface. When the negative voltage pulse is applied to the front gate, the front channel surface potential and the body potential decreases. The holes necessary to form the stronger accumulation region

under the front gate causes deep depletion in the neutral film. However, in order to maintain the charge conservation at the back gate, the total inversion charge in the back channel decreases with the available hole population. As a result, a sudden drop in the drain current is observed. In absence of hole injection from the n^+ source-drain, the drain current reestablishes itself only through the thermal generation process. It should be mentioned that the experiment is performed in a dark ambient to prevent any photo-generation and a small drain bias is used to avoid carrier generation through impact ionization.

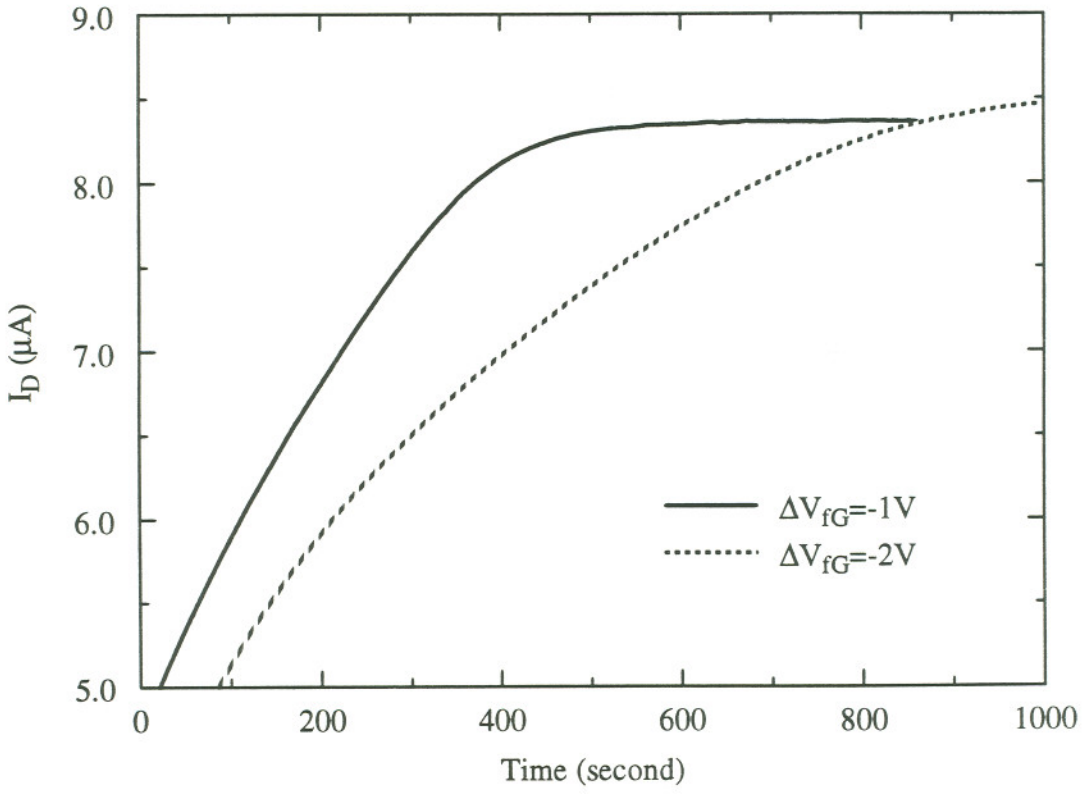

Figure 2-14: Current transients in lifetime measurement experiment (SIMOX)

The Fig. 2-14 shows the transient drain current for two different front gate pulse amplitudes with a contant back gate bias of 30V. Since the holes are generated only

through the thermal generation process, it may take minutes to establish a steady state current flow in the previously inverted back channel. In the second case, the channel current actually disappears due to the lack of sufficient inversion charge near the back channel.

The equation for calculating generation lifetime in an enhancement mode SOI device has been be derived knowing that the generated majority carriers (in this case holes) affect both the front gate accumulation charge and the back gate depletion charge. A continuity equation for the majority carriers in the transistor body can be written [43]:

$$\frac{dQ_D}{dt} + \frac{dQ_a}{dt} = qn_i\left(\frac{W - W_\infty}{\tau}\right) + qn_i s \tag{2.8}$$

where Q_D and Q_a are the back and the front gate depletion and accumulation charge, respectively. W and W_∞ refer to the time dependent and steady state depletion width in the transistor body. Effective generation lifetime is expressed as τ and s is the effective surface generation velocity. The first term on the right hand side of eqtn. 2.8 refers to the generated holes in the depletion region while the second term accounts for the surface generation. After using the proper expressions for the accumulation and the depletion charge, one can arrive at the following expression [43]:

$$\frac{-N_A C_{of}}{2n_i\varepsilon_s}\frac{d}{dt}\left[K(I_\infty - I_D) + \frac{\varepsilon_s}{C_{of}} + \sqrt{\frac{4\varepsilon_s\phi_F}{qN_A}}\right]^2 = \frac{K(I_\infty - I_D)}{\tau} + s \tag{2.9}$$

where $K^{-1}=qN_A\mu(Z/L)V_D$. I_∞ and I_D refers to the steady state and the transient drain current. Z and L are the channel width and length of the MOS transistor, respectively. N_A is the channel doping, ϕ_F is the back channel potential, and C_{of} is the front gate oxide

capacitance per unit area.

The calculation of generation lifetime τ does not require an explicit solution of eqtn. 2.9. If the left hand side of the equation is plotted against the right hand side, a straight line results if device operation only in the linear region is considered. The inverse of the slope of the straight line is the generation lifetime τ. During this experiment, the drain is biased at 0.1V to ensure operation in the linear region.

The generation lifetime obtained from a SIMOX NMOS transistor is ~ 81 μs. The plot used to determine to the lifetime is shown in Fig. 2-15.

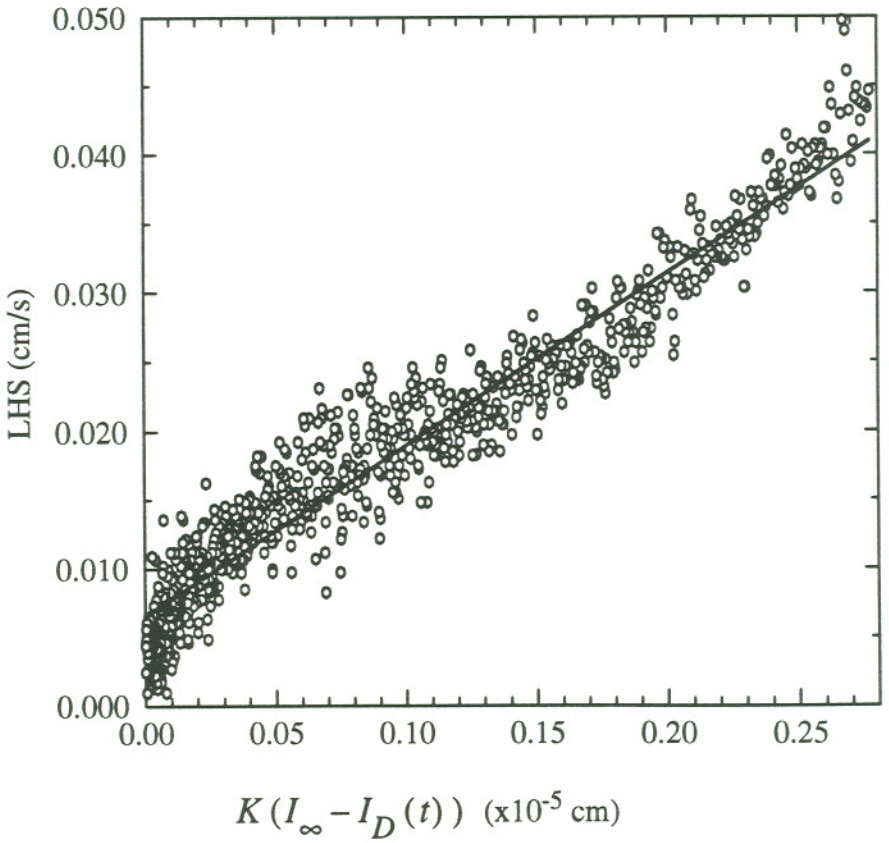

Figure 2-15: 'Zerbst' type plot for the extraction of generation lifetime

(For the current transient shown in Fig. 2-14, ΔV_{fG}=-2V)

A similar device fabricated on an ISE substrate yielded a lifetime of ~11 μs. According to our results, the SIMOX substrates have fewer defects in the SOI film as compared to that of the ISE wafers.

The surface generation velocity s, the y-intercept in the Fig. 2-15, is 0.007cm/sec. This small value can be attributed to the fact that the front interface is accumulated and the back interface is inverted. Both events screen the interface states and reduce the surface generation velocity. This is also indicative of the fact that bulk generation is the dominant mechanism in this experiment as compared to the generation of carriers at the oxide interfaces.

In Fig. 2-16, results from a similar experiment are plotted. In this case, different back gate biases were used to observe the variation of the generation lifetime as a function of the film thickness. However, in both cases it takes about the same time for the current to reach the steady state value. The deep depletion width in the SOI film is varied by changing the back gate bias. The results, therefore, suggest that the generation lifetime is not a strong function of the SOI film depth [43].

The lifetime values obtained in these experiments are high enough for commercial IC applications. The values reported in the literature are in the range of 0.1-130 μs. These results, obtained from commercial wafers, compare well with the best results published to date.

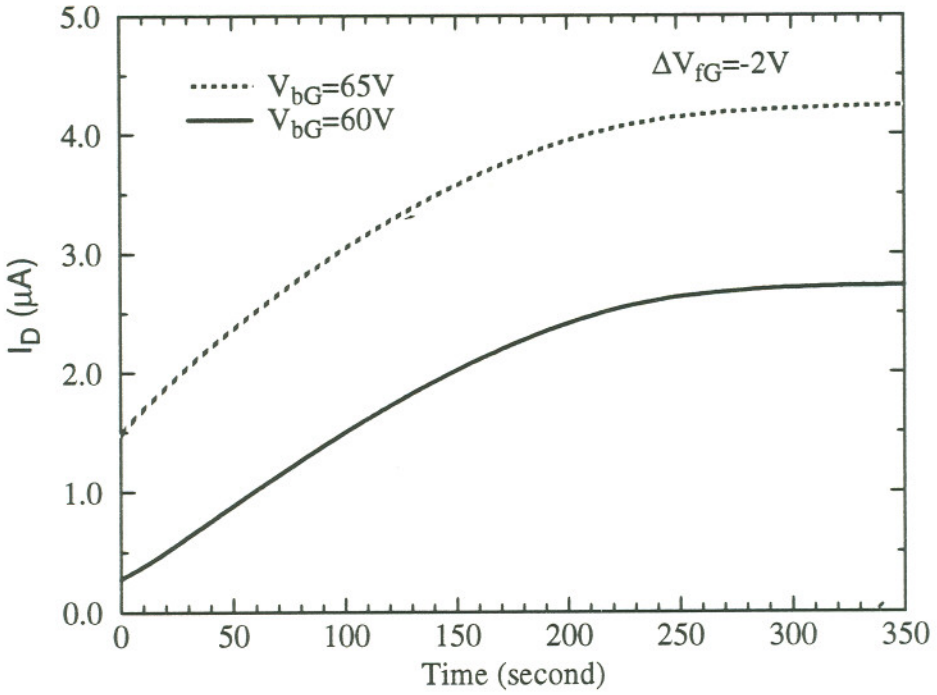

Figure 2-16: Variation of the back gate bias (ISE)

Chapter 3
High Voltage LDMOS Design on SOI Substrates

3.1 High Voltage Devices on SOI

The market and demand for high voltage devices that can be integrated with standard low-voltage CMOS logic or control circuitry are growing at a steady pace. The advent of "smart power" technology will make the electronics used in the home appliances to aircrafts, more compact, cheaper and efficient as high voltage integrated circuits (HVIC) replace discrete devices and IC components. The availability of thin film, high quality SOI substrates offer device and process engineers an attractive alternative to traditional bulk Si design. The principal advantage of SOI design is the superior dielectric isolation of the high voltage devices as compared to the traditional junction isolation technique. A significant decrease in junction area is also a highly desirable feature for high temperature operations.

Over the years, many different device structures have been proposed and fabricated for high voltage applications. However, the structure most suited for HVIC design on SOI substrates is the lateral double-diffused metal oxide semiconductor (LDMOS) transistor [4]. In this chapter, a set of general design rules are developed for SOI LDMOS design. The optimization of the geometric aspects of the design and the doping concentrations are analyzed. A two dimensional device simulator is used to model and optimize the breakdown voltage performance of the SOI LDMOS structures. In the latter part of this chapter, issues relevant to the specific application of LDMOS structures in AMEL pixel

array (Fig. 1-3,Chapter 1) are discussed. Special attention has been paid to short drift region LDMOS device fabrication with near ideal breakdown voltage performance. The design concepts, developed from the 2D simulations, are experimentally verified by the fabrication and characterization of test structures on SOI substrates.

3.1.1 LDMOS Structure - Bulk versus SOI

A schematic cross section of a bulk LDMOS structure is shown in Fig. 3-1. Usually such devices are fabricated on an n^- epi-layer grown on a p^- substrate. Conventional LDMOS structures have thick epi-layers in contrast to a RESURF structure, which is discussed in the next section.

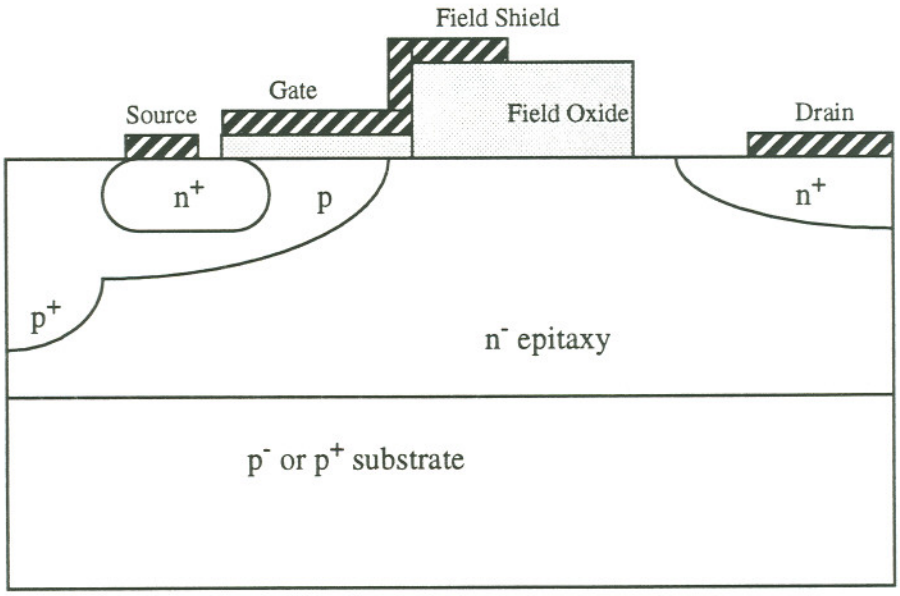

Figure 3-1: A schematic cross-section of a bulk-Si LDMOS structure (not to scale)

The threshold voltage of such high voltage devices are usually higher than CMOS logic devices and the channel is doped heavily as compared to the neighboring drift region, which consists of a n^-epi region between the channel and the n^+ drain contact. As a result, punchthrough is not an usual breakdown mode in these devices as the junction depletion does not extend much into the channel. The field plate, also know as the field shield plate, is essentially an extension of the gate electrode and improves the breakdown voltage performance of the pn^- junction by extending the depletion layer curvature [44]. The field shield thus reduces the electric field at the junction under the gate electrode and enhances the breakdown voltage of the structure. The field oxide thickness must be carefully chosen to insure the optimum performance of the device. The field oxide is usually grown by the LOCOS process using a nitride mask for the unoxidized areas. Careful monitoring of the oxide growth is essential as the oxide is grown in the active area of the device and may create defects near the channel/drift region interface. Problems related to defect induced leakage current will be addressed later in the chapter. An extensive analytical treatment of the breakdown voltage analysis of bulk LDMOS devices can be found in reference 45.

An SOI LDMOS structure, shown in Fig. 3-2, looks very similar to its bulk counterpart. A buried oxide layer is present between the substrate and the top Si film. The oxide layer plays a very important role in supporting the electric field and uniform distribution of the potential contours. The principal advantage is the easy isolation of SOI devices and reduced process complexity. For devices fabricated on thin Si films mesa isolation is a very effective technique. For thicker films, poly-Si filled trenches become a necessity. In this work, the focus is on the thin film devices since mesa isolation is the least complex among the available isolation techniques and also works well when the higher packing density of transistors is considered.

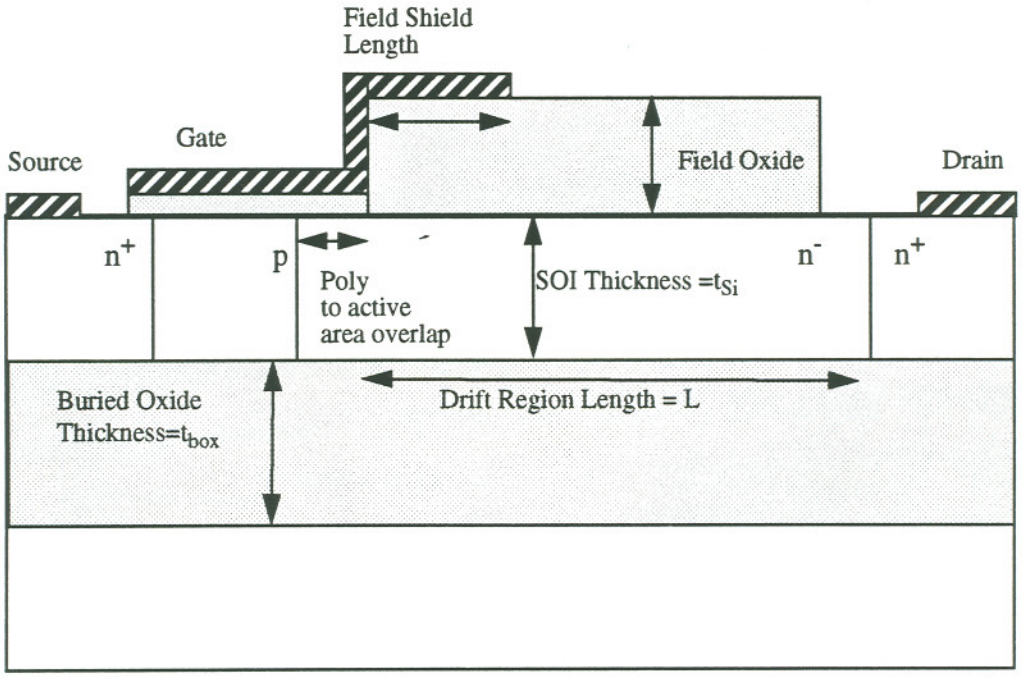

Figure 3-2: A schematic cross-section of an SOI LDMOS structure (not to scale)

3.2 Breakdown Voltage Optimization

The breakdown voltage of a high voltage transistor refers to the off-state drain voltage that the device can sustain without any significant amount of current flow. This off-state breakdown voltage is also the drain to source voltage drop when the device is operating in the breakdown mode. The voltage is usually dropped across a reverse biased pn junction [44]. The high electric field, across the depletion layer of the reverse biased junction, accelerates the carriers that are generated within the depletion region or transported by the diffusion mechanism. At high applied voltages, the carriers attain high velocities such that upon collision with the lattice they generate electron-hole pairs. This process of pair creation is aptly named impact ionization. The generated electrons and

holes can also cause impact ionization if they achieve high enough velocities from the collision process or through the acceleration due to the high electric field. Thus the event becomes a multiplicative phenomenon where each incoming carrier can initiate the creation of a large number of electrons and holes (avalanche breakdown).

3.2.1 Ionization Integrals

In order to quantify the rate of impact ionization under a certain applied bias, impact ionization coefficients for both electrons and holes have been defined. The impact ionization coefficient for an electron is defined as the number of electron-hole pairs generated by an incoming electron traversing through one cm of depletion layer. The electron ionization coefficient α_n, under an electric field of value E V/cm, can be expressed by the following equation [44]:

$$\alpha_n = a_n e^{-\frac{b_n}{E}}. \tag{3.1}$$

where $a_n = 7\text{x}10^5$ /cm and $b_n = 1.23\text{x}10^6$ V/cm. A similar equation for the hole ionization coefficient α_p can be defined, with $a_p = 1.6\text{x}10^6$ /cm and $b_p = 2\text{x}10^6$ V/cm. These values have been determined empirically and are used in the 2D device simulations, results of which will be presented in the latter part of this chapter.

Thus the average number of ionizing collisions encountered by a carrier traversing through a depletion region of width W can be expressed by the following expression, also known as the ionization integral:

$$I = \int_0^W \alpha(E)\, dx. \tag{3.2}$$

Avalanche breakdown occurs when the value of this integral approaches unity. For an extensive treatment of this material the reader is referred to reference 40.

3.2.2 2D Device Simulator for BV Calculation

In order to model and optimize the breakdown voltage performance of the LDMOS structures, the two dimensional device simulator Medici has been used extensively [46]. The simulator solves Poisson's equation and Current Continuity equations for a user defined geometrical structure and corresponding doping concentrations.

First, a device structure similar to the one shown in Fig. 3-2 is defined and a mesh of node points are generated. Then an incremental bias is applied at the drain electrode of the device. The values of the ionization integrals are computed at every node point for each bias voltage. The drain bias at which the value of any one of the ionization integrals equals or exceeds unity is defined as the breakdown voltage. The two dimensional potential contours and electric field profiles, generated by the simulator, provide important insight regarding the breakdown mechanism of a device.

3.3 RESURF Principle

The concept of the REduced SURface Field (RESURF) was first introduced by Apples and Vaes in 1979 [47]. They described a structure which consists of an n^- epitaxial layer grown on a p^- substrate and is laterally bounded by a p^+ region, as shown in Fig. 3-3. Fig. 3-1 can be regarded as a variation of this structure when only the p-channel, n^--epi and a p^- substrate are considered.

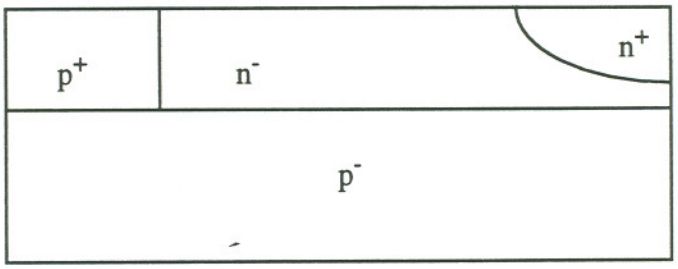

Figure 3-3: A generic lateral, high voltage device structure (RESURF principle)

A generic RESURF structure consists of two diodes: one horizontal p^-n junction and a vertical p^+n^- junction. The breakdown voltage of the horizontal junction is significantly higher than the vertical one, due to the low doping concentrations of the substrate and the epi-layer. In case of a thick epi-layer, the depletion takes place near the surface and does not extend to the horizontal junction. Therefore, the breakdown voltage is essentially determined by the vertical p^+n^- junction.

If a thin epi-layer is used, the depletion region due to the applied drain bias extends to the substrate-epi horizontal junction. As a result, both p^+n^- and p^-n^- depletion regions interact and the depletion stretches further along the surface, increasing the breakdown voltage of the structure. Therefore, in thin epi-layer structures, it is possible to spread out the depletion region and avoid potential crowding, resulting in reduced electric field at the surface area. A successful application of the RESURF principle depends on the epi-layer doping. The total charge in the epi-layer must be under strict control in order to optimize the breakdown voltage performance of the structure. If the doping is too high, a narrow surface depletion takes place. Thus a highly doped thin epi-layer becomes equivalent to a thicker one and does not exhibit the advantages offered by an optimized RESURF structure. On the other hand, too low an epi-layer doping concentration is also not beneficial;

the depletion reaches the n^+ contact at relatively low drain voltages and gives rise to high electric fields at the other end of the structure. Using 2D numerical simulations, Apples and Vaes showed that the delicate balance between the epi-layer thickness d_{epi} and the doping concentration N_{epi} conform to the following expression [47]:

$$d_{epi} \cdot N_{epi} \approx 10^{12} \frac{atoms}{cm^2} \tag{3.3}$$

At this value, a balance is reached between a fast depletion due to the low doping concentration and a narrow surface depletion caused by a heavily doped epi-layer. The RESURF principle is used extensively in thin-epi bulk LDMOS design.

3.3.1 Anomalous Breakdown of SOI LDMOS structures

It is expected that an LDMOS structure with a longer drift length will exhibit a higher breakdown voltage as compared to that of a short drift region device. However, an anomalous reverse biased breakdown of SOI LDMOS structures was observed in a set of fabricated test structures. In this section, the objective is to understand an anomalous breakdown mode in these structures with the help of the RESURF principle. The LDMOS structures were fabricated on an ISE wafer with the SOI film and buried oxide thicknesses of 0.35 and 1 μm, respectively. All the LDMOS structures are identical except for the drift region length, which varies from 10μm to 35 μm. Table 3-1 shows the measured breakdown voltage of the fabricated structures.

As seen in Table 3-1, the drift region length does not have a significant effect on the breakdown voltage performance of these structures. This phenomenon has been analyzed by the use of 2D simulations. An understanding of the RESURF principle as it applies to the SOI LDMOS structure is necessary to explain this anomalous breakdown mode of the fabricated LDMOS transistors.

Table 3-1: Drift Region Length and Breakdown Voltage of Fabricated Devices

Drift Region Length (μ m)	Measured Breakdown Voltage (V)
10	83
15	85
20	84
25	98
30	81
35	86

A structure with a 10 um drift region and similar doping concentrations used in the fabrication of the test structures was simulated using Medici. Using the ionization integral criterion mentioned in the previous section, the breakdown voltage was calculated to be 90 V, a value reasonably close to the measured values in Table 3-1. The potential contours within the device with drain biased at the breakdown voltage is plotted in Fig. 3-4.

The potential crowding near the p^+n junction gives rise to high electric fields near the Si-SiO_2 interface. The resultant electric field along the Si-SiO_2 interface is also plotted in Fig. 3-5. The peak electric field occurs under the gate edge and causes the reverse biased breakdown of the device.

A magnified photograph of an LDMOS transistor is seen in Fig. 3-6. Due to the asymmetric nature of the device structure, the drain, gate, and the source terminals are clearly recognizable. The presence of the drift region between the gate poly and one of the external contacts indicates the drain end of the device.

If a current limiting circuit element is not present during the reverse bias character-

ization of MOS transistors, catastrophic breakdown may permanently damage the device. Under high magnification the physical damage may be visible. The device, shown in Fig. 3-6, was photographed again after a catastrophic breakdown near the gate edge. The physical damage at the channel-drift interface is clearly visible in Fig. 3-7 and provides experimental verification of a high electric field peak near the gate edge.

The most important piece of information in Fig. 3-4 is that the depletion region is only 6 μm long, measured from the channel-drift region interface. This result indicates that an above optimum doping concentration has been used in the drift region of these devices. Therefore, all the fabricated structures with drift region length exceeding 6 μm have similar breakdown voltage performances. Longer drift length does not translate into further depletion and subsequently higher breakdown voltages.

In the next section, the drift region doping of the SOI LDMOS transistor along with other geometric parameters will be optimized. While we studied the effect of one particular device parameter, optimized value for other parameters were used.

The plotted potential contours:

10V to 90V with 10V interval

Undepleted region: does not support any Electric field

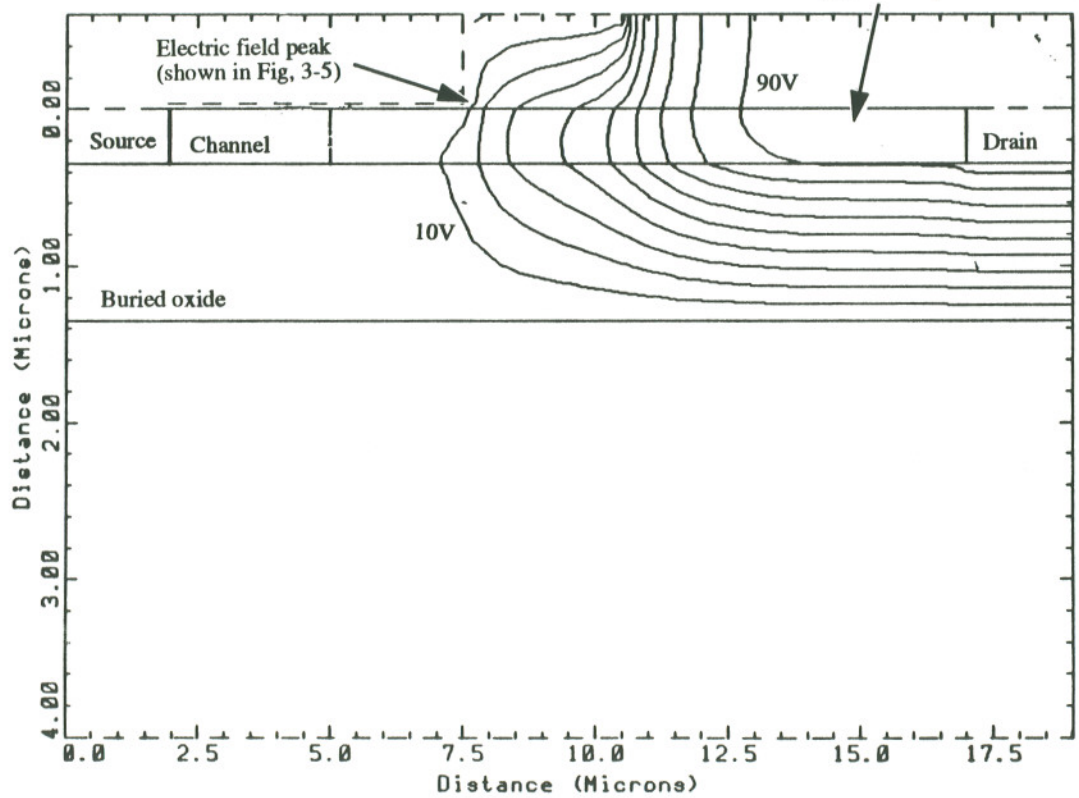

Figure 3-4: Potential contour distributions at the breakdown voltage (90V)

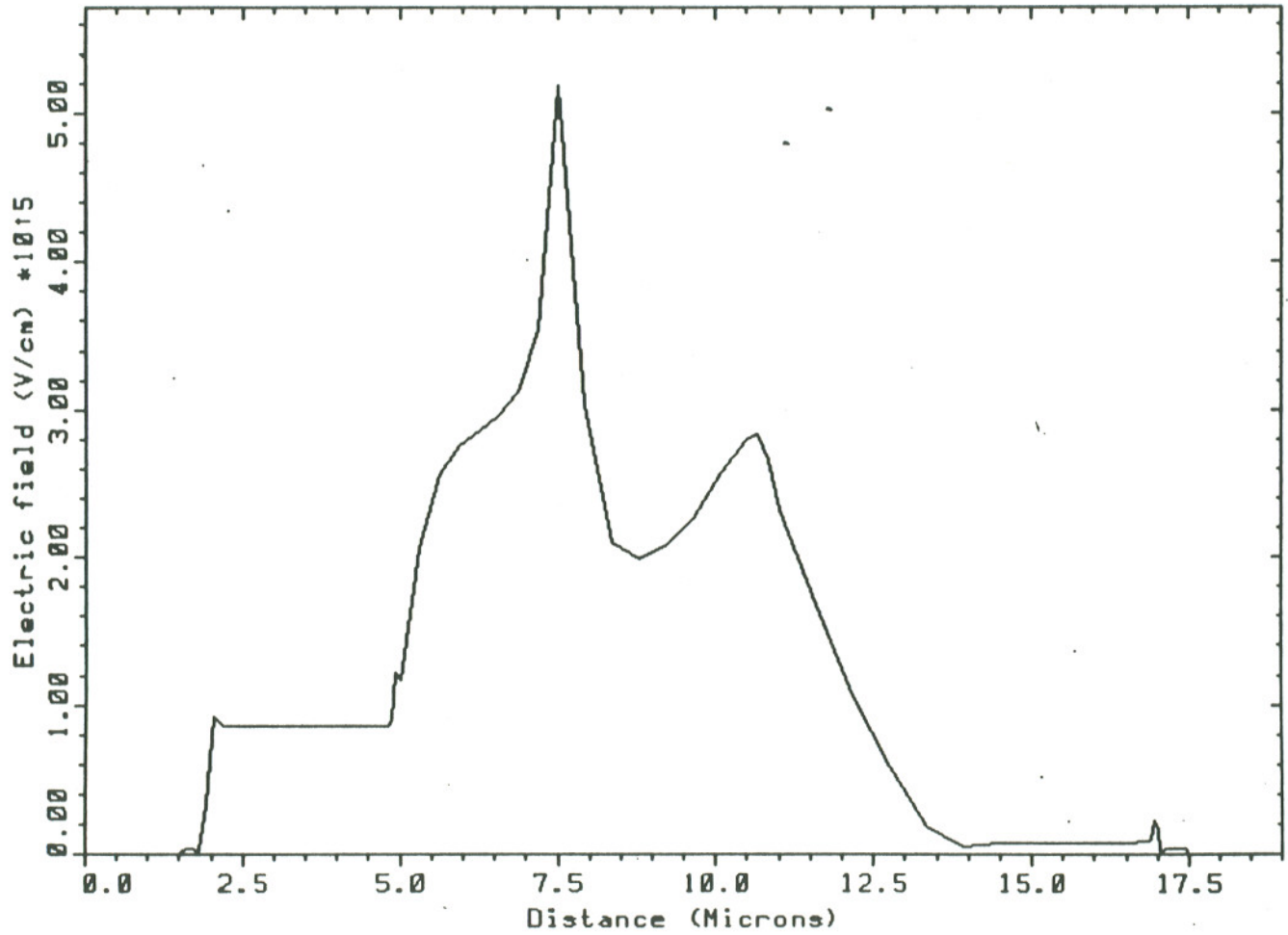

Figure 3-5: Electric field at the Si-SiO_2 interface

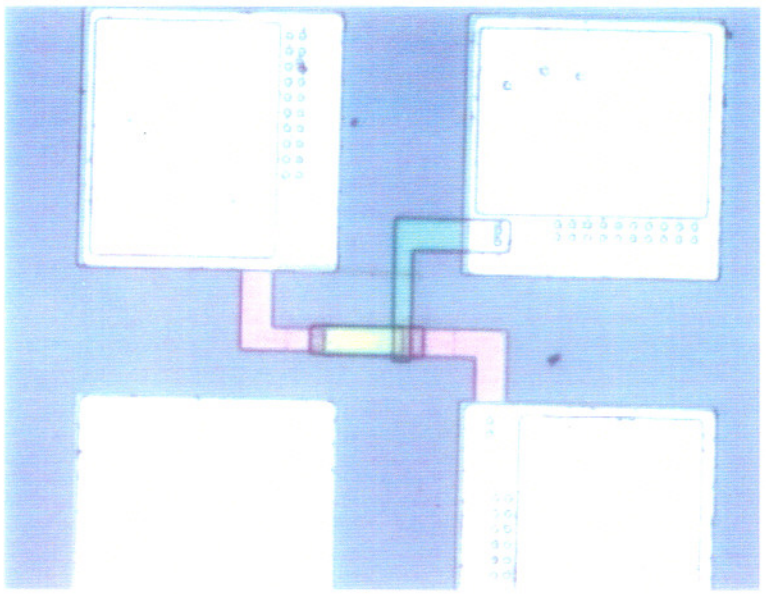

Figure 3-6: LDMOS transistor (L=30 μm, before catastrophic breakdown)

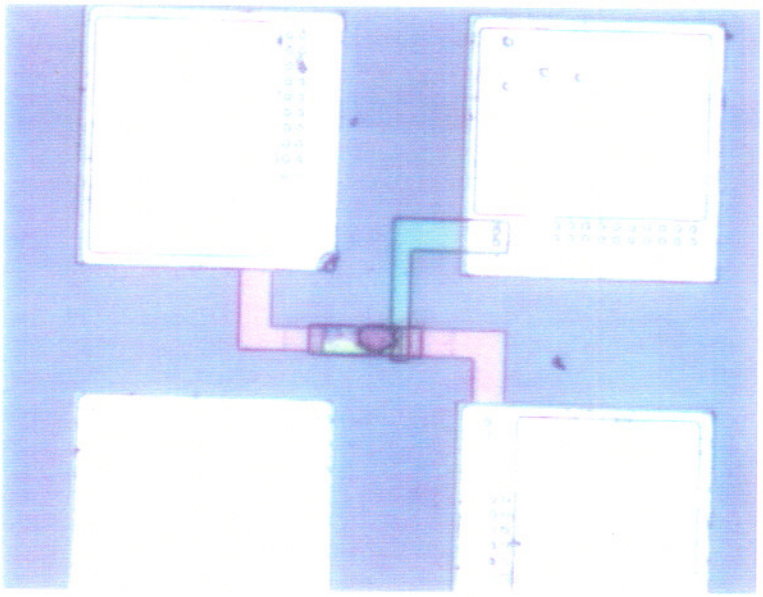

Figure 3-7: LDMOS transistor (after catastrophic breakdown)

3.4 Optimization of Device Parameters

The experimental results in the last chapter indicate a saturation in the breakdown voltage performance as a function of the drift region length of the LDMOS transistors, caused by nonoptimized drift region doping concentration. Before optimizing the device parameters, a knowledge of the ideal breakdown voltage of such an SOI LDMOS structure may be beneficial for a general understanding of this phenomenon. Merchant *et al.* have published extensively on the ideal reverse bias breakdown voltage (BV) of SOI structures [10, 48]. For a thin SOI layer and a thick buried oxide, the breakdown ionization path is either a horizontal path along the top or the bottom Si surface or a vertical path at the right edge of the depletion near the drift-drain interface. The underlying assumption is that in the ideal case the electric field under the gate electrode is small and the depletion reaches the drain contact region to give the maximum breakdown voltage performance. Then the ionization integral can be written as:

$$I[\psi(x)] = \int_0^L \alpha(\psi')\,dx \tag{3.4}$$

where $\psi(x)$ is the electrostatic potential along the top surface of the depletion in the drift region, $\alpha(\psi')$ is the ionization rate (defined in eqtn. 3-1), and $\psi' = \frac{d\psi}{dx}$ is the magnitude of the lateral electric field. For an optimized device with an ideal breakdown characteristics, the value of the integral must be as small as possible. The condition (also known as the Euler-Lagrange eqtn.), which minimizes I for a fixed drift length L and applied bias V, implies that $\psi \propto x$. Therefore, the lateral electric field must be uniform across the drift region for optimum breakdown voltage performance. At the breakdown voltage, the value of the integral reaches 1. Therefore, the critical electric field E_c can written as [10]:

$$E_c = \frac{b_n}{\ln(a_n L)}. \tag{3.5}$$

After integrating both sides of equation 3-5, the ideal breakdown voltage of an SOI LDMOS transistor can be written as [10]:

$$V_{BR} = \frac{b_n L}{\ln (a_n L)}. \tag{3.6}$$

For further analysis of the breakdown voltage phenomenon in SOI LDMOS transistors, the reader is referred to references 10 and 48.

The deviation from the ideal breakdown voltage, expressed in the above equation, can be caused by several factors. The effect of a nonoptimized drift doping has already been demonstrated. The inherent assumption in the formulation of eqtn. 3.6 is that the breakdown is caused by a horizontal ionization path in the drift region. However, due to a thick SOI film or in the presence of a thin buried oxide layer, a saturation in the breakdown voltage is often observed due to the presence of a vertical ionization path. The longer the drift length, the thicker buried oxide layer and thinner SOI film are needed to achieve the ideal breakdown voltage.

Although the ideal breakdown voltage for a given drift length can be computed using the eqtn. 3.6, 2D numerical simulations are essential for the selection of optimum buried oxide thickness, drift region doping and other important device parameters.

3.4.1 RESURF Principle and Optimization of Drift Region Doping

The RESURF principle can be applied to SOI LDMOS structures. The depletion in the epi-film is replaced by the depletion in the SOI layer. Keeping in mind the relationship between the epi-layer and the optimum doping concentration for the drift region, an SOI equivalent of eqtn. 3-3 can be written in the following fashion:

$$t_{Si} \cdot N_{drift} \sim 10^{12} \frac{atom}{cm^2} \tag{3.7}$$

where t_{si} is the SOI film thickness and N_{drift} is the optimum drift doping concentration.

In order to verify the effectiveness of eqtn. 3-7, an SOI LDMOS structure with a 10 μm drift region was simulated. The objective was to optimize the drift region doping concentration for the simulated structure. During the simulations the SOI film thickness was assumed to be 0.35 μm. The buried oxide thicknesses used for the simulations are the standard oxide thicknesses in commercial SIMOX (0.35μm), ISE (1μm), and Bonded (2μm) wafers. For each buried oxide thickness, the drift region doping had to be independently optimized. Breakdown voltage as a function of drift region doping is plotted in Fig. 3-8. There are several very important pieces of information in Fig. 3-8. Firstly, the breakdown voltage decreases sharply on the right hand side of the optimized dose. Therefore, the process should be designed such that the drift region doping is always on the left hand side of the peak breakdown voltage. This becomes more important in SOI LDMOS design as the SOI film thickness may vary as much as 20 nm in present wafer manufacturing technologies. For a fixed drift implant dose, depending on the SOI film thickness, the thickness nonuniformity can cause severe breakdown voltage variations across the wafer.

Secondly, unlike bulk, the thickness of the buried oxide plays an important role in determining the optimum charge in the drift region and eqtn. 3.7 must be used with caution. The optimum dose for the drift region doping decreases with an increasing buried oxide thickness and 2D simulations become a necessity. The optimum doping concentration can easily be calculated by knowing the optimum dose and the film thickness of the SOI layer.

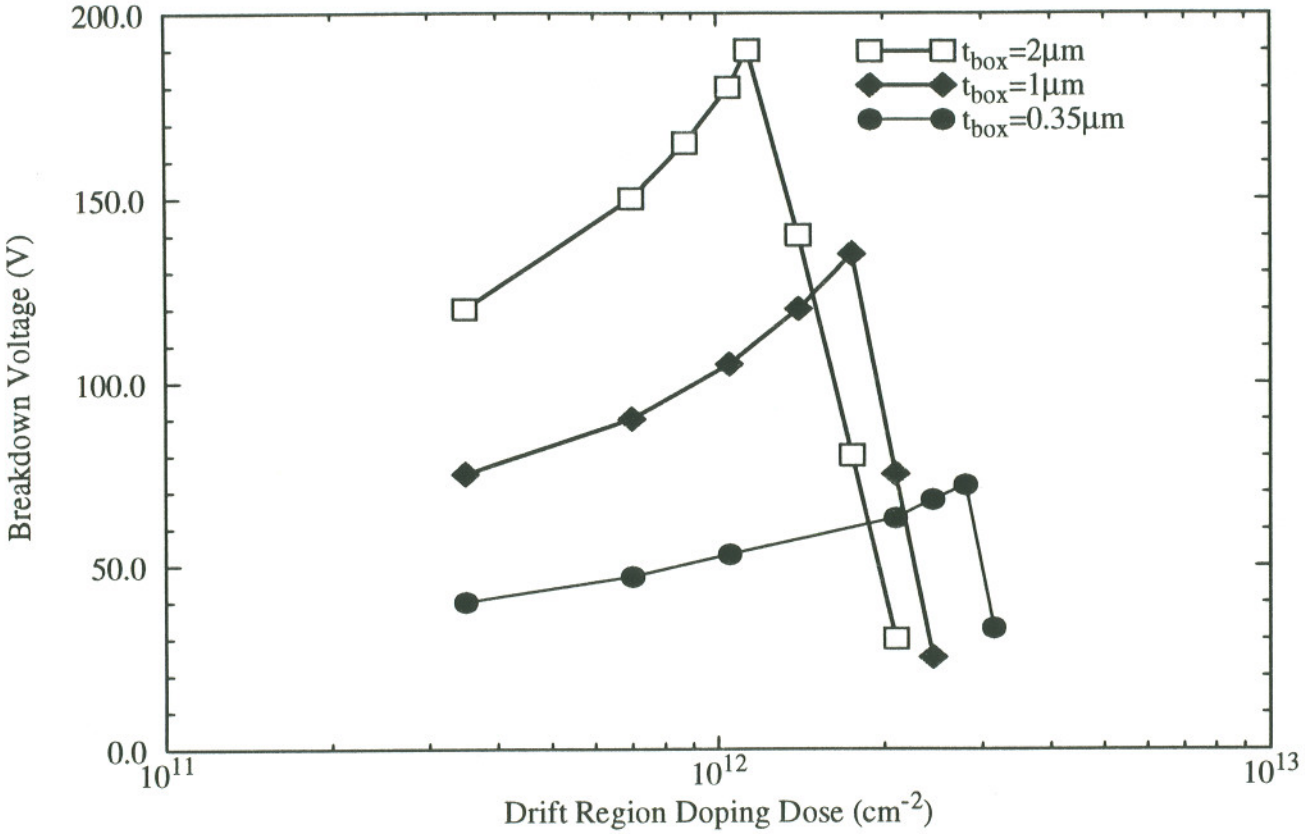

Figure 3-8: Breakdown voltage versus drift region doping dose (L=10μm)

3.4.2 Buried Oxide Thickness

Thick buried oxide layers are necessary to achieve the ideal breakdown voltage predicted by equation 3.6. The breakdown voltage of SOI LDMOS structures tend to saturate as a function of drift region length if the buried oxide is too thin. The fabricated LDMOS structures on SIMOX wafers with buried oxide thickness of 0.35 μm demonstrate a saturation in the breakdown voltage at ~65V. This event corresponds well with the 2D simulations which predicted a saturation value of 70V.

A thicker buried oxide and a corresponding lowering of the drift region doping translates into more uniform spreading of the potential contours. Since the electric field $E \propto \frac{d\Psi}{dx}$, uniform spreading of the potential contours results in low electric fields under a high drain bias. Thus with a lower doping concentration, longer depletion width and higher breakdown voltage can be realized. The longer the drift length, the thicker the buried oxide needs to be in order to obtain the ideal breakdown voltage predicted by eqtn. 3.6. For example, for a drift region length of 50 μm, a buried oxide thickness of 4.4 μm may be needed [10].

3.4.3 Field Shield Plate and Field Oxide Thickness

It is known that the electric field at the surface of a planar diffused junction is higher than that of an ideal parallel plane junction. The phenomenon is caused by the depletion region edge curvature effects in a diffused junction. However, a careful modification of the surface potential can be realized by controlling the depletion layer curvature. This objective is accomplished by the use of a metal (conductive) shield plate, placed at the edge of the junction. In the case of an LDMOS, a gate extension over a field oxide is typically used to achieve this goal (see Fig. 3-2).

The length of the field shield plate and the field oxide thickness are two important

parameters in this respect. The field shield plate has to be long enough such that potential crowding does not take place near the channel-drift junction. Furthermore, the field oxide must be sufficiently thick as not to give rise to a high electric field at the edge of the field plate.

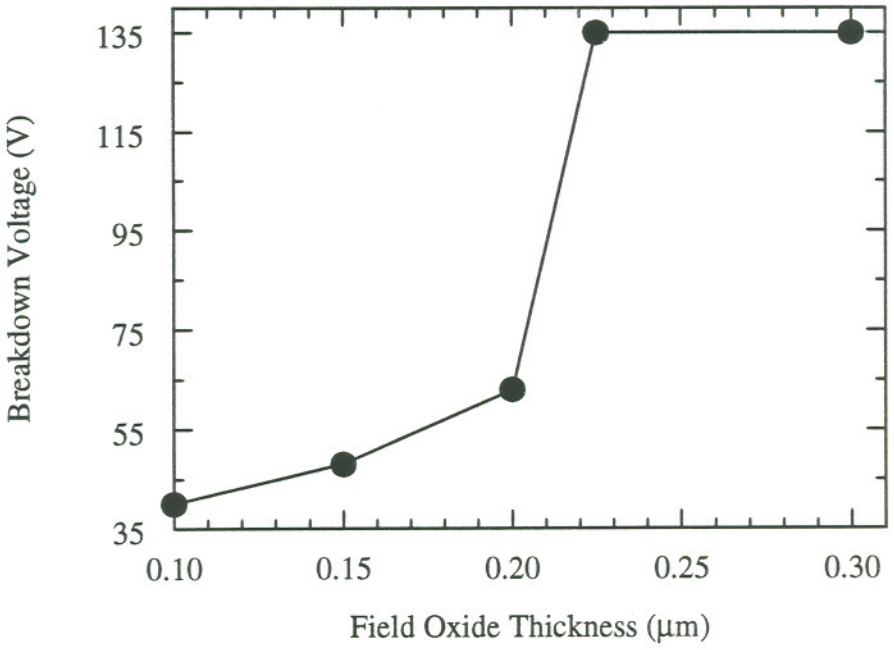

Figure 3-9: Breakdown voltage as a function of field oxide thickness

Field oxide thickness and field shield length have been optimized independently. In both cases, an optimum drift region doping has been used for the simulations. In Fig. 3-9, the breakdown voltage is plotted as a function of the field oxide thickness. A saturation in the breakdown voltage is observed for field oxide thicknesses greater than ~0.25 μ m. Further optimization will require a thicker buried oxide (> 1μm).

Similar type of behavior is observed in Fig. 3-10 where the breakdown voltage is plotted as a function of the length of the field shield plate. It has also been found that

without an optimized doping concentration in the drift region, the requirement for the minimum field shield length to achieve a saturation in breakdown voltage becomes more stringent.

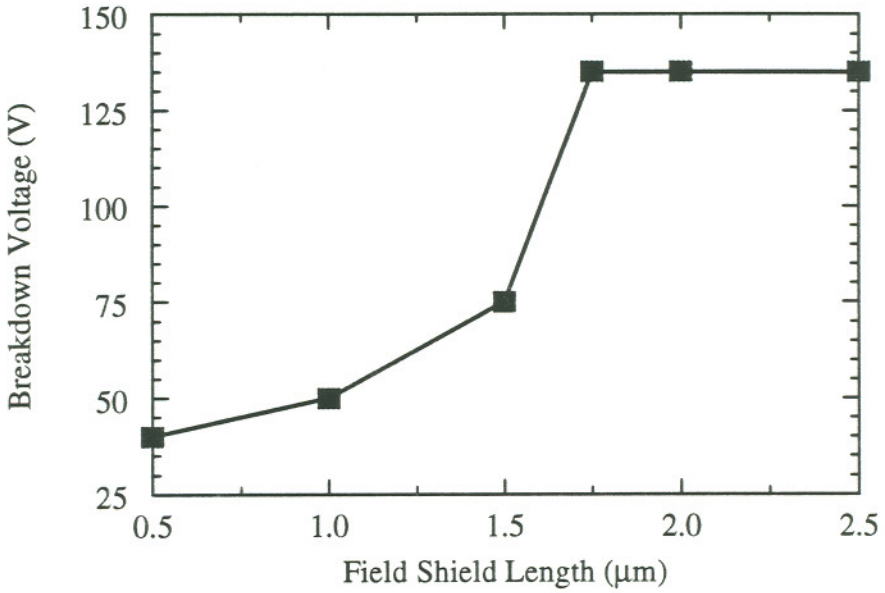

Figure 3-10: Breakdown voltage as a function of the field shield plate

3.4.4 Poly-to-Active Area Overlap

Poly-to-active area overlap refers to the gate (poly-crystalline Si) overlap of the active drift region, as shown in Fig. 3-2. It is an important design parameter in bulk LDMOS design and not enough overlap can lead to premature breakdown. However, Medici simulations show that in SOI LDMOS devices poly-to-active area overlap does not affect the breakdown voltage performance of the transistor. However, due to process variations some poly-to-active area overlap is necessary to ensure inversion along the full length of the channel.

If the potential contours in a bulk device, seen in Fig. 3-11, are compared to the

ones in an SOI transistor, plotted in Fig. 3-4, the difference becomes clear. In a bulk device, the potential contours extend under the channel and insufficient overlap may cause high electric fields under the channel edge, which is not the case in the SOI structure.

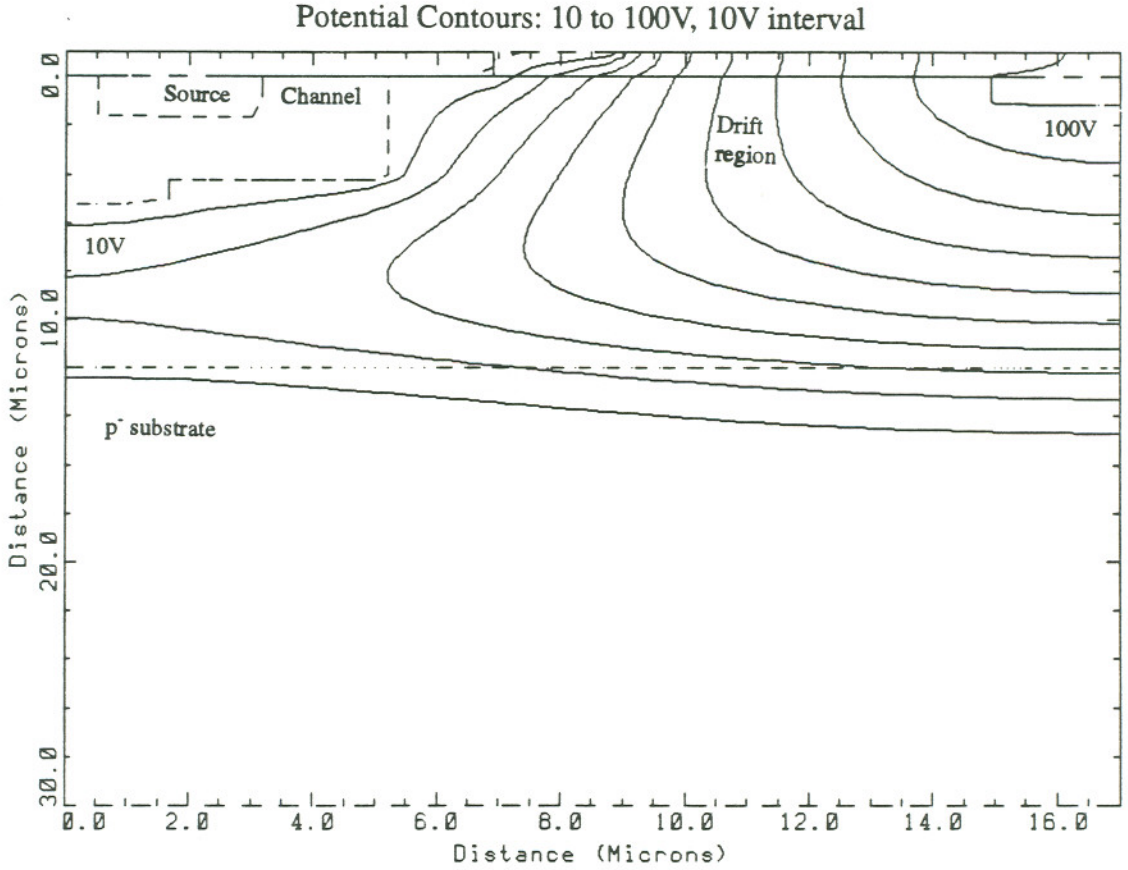

Figure 3-11: Potential contour distributions in a bulk LDMOS transistor

Based on these simulations, identical SOI LDMOS structures except for different poly-to-active area overlaps were fabricated. The measured reverse biased characteristics from two such devices are shown in Fig. 3-12. Both the structures have similar break-down voltages as suggested by the simulations. However, high amount of leakage current is observed with the 1μm overlap structure. The actual overlap in the fabricated devices

are shorter than the overlap defined by the lithography. The DMOS channel implant is performed before the field oxidation step, which defines the "physical" poly-to-active area overlap. Boron out-diffusion during the field oxide growth may increase the channel length, which will result in a shorter overlap. During the LOCOS growth, the edge of the field oxide also extends underneath the nitride mask. Therefore, it can be surmised that the high leakage current in the otherwise identical 1μm overlap device is caused by the LOCOS related defects positioned too close to the channel/drift region pn junction.

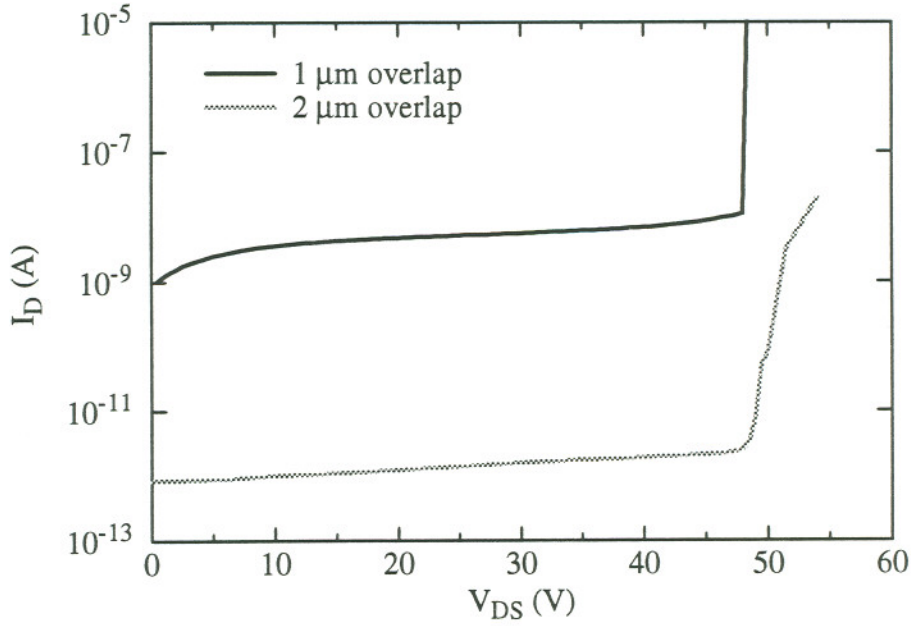

Figure 3-12: Leakage currents and breakdown characteristics in fabricated devices

(V_{GS}=0V, the wafer substrate was also grounded)

Stress and defect generation at the LOCOS edges has been a concern for the IC industry. LOCOS related leakage problems has specifically been reported in dynamic random access memory (DRAM) production, which leads the industry in packing density of transistors [50]. The defects are usually in the form of shallow pits, dislocation loops,

and stacking faults. A recent study suggests that the defect generation is caused by the maximized tensile stress at the LOCOS edges. It should be mentioned that in standard CMOS technology the LOCOS oxide is placed in between two transistors for isolation purposes. However, in LDMOS transistors the field oxide is part of the active device area and defects due to the oxide growth may have more serious consequences, as seen in Fig. 3-12. Therefore, a poly-to-active area overlap of 2 μm is recommended for leakage current considerations.

3.5 Application of LDMOS Devices for AMEL Displays

In an AMEL pixel, the drain of the LDMOS transistor is connected to the EL stack consisting of a semiconductor layer sandwiched between two layers of insulating dielectric material (see the circuit schematic in chapter 1). This extension from the drain acts as the bottom electrode for the electroluminescent devices. Figure 3-13 shows the cross-sectional view of the EL electrode as seen in the pixel cross-section.

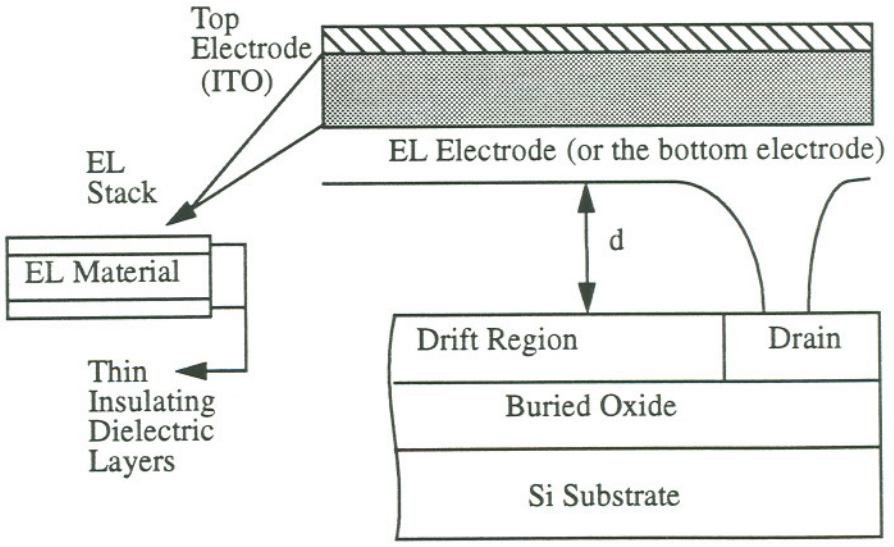

Figure 3-13: A cross-sectional view of the EL electrode and the LDMOS drain.

The presence of the EL electrode changes the potential contours and electric field profiles within the device in presence of a reverse bias on the drain. The potential contours in such a structure is plotted in Fig. 3-14. A revision of the generalized LDMOS design rules, developed earlier in this chapter, becomes necessary. In this section, some of the earlier simulations for LDMOS optimization are repeated with the presence of an EL electrode over the length of the device.

It has been found that although the basic design rules remain the same, longer field shield lengths and thicker field oxide thicknesses are necessary to obtain the optimum breakdown voltage performance for a given structure when the EL electrode is present. For example, for a discrete device the breakdown voltage as a function of field oxide thickness saturates at ~ 0.25 μm, as seen in Fig. 3-9; however, with the presence of an EL electrode, a 0.6 μm thick field oxide is required to observe any such saturation characteristics when the breakdown voltage is plotted against the field oxide thickness.

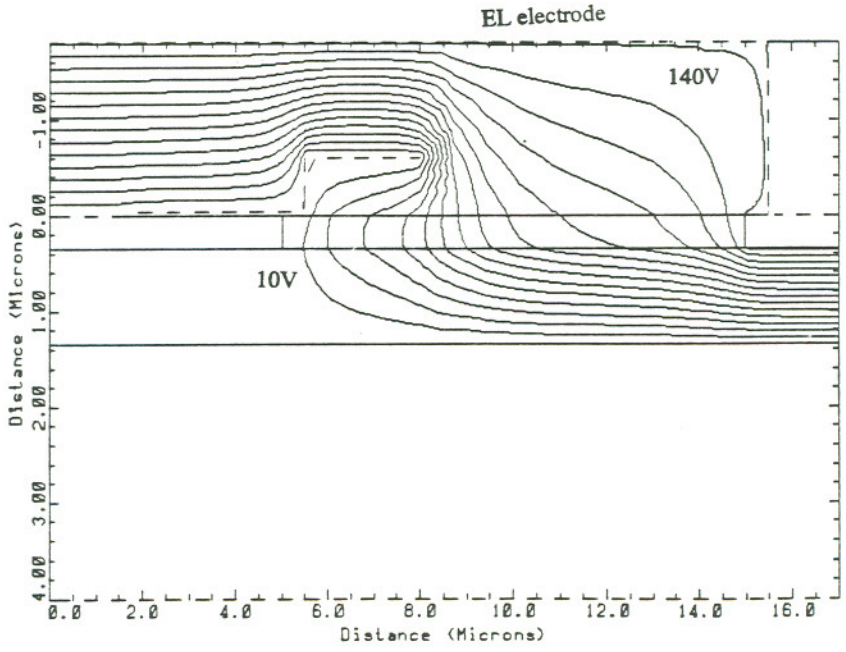

Figure 3-14: The potential contour distribution in presence of the EL contact

Previously, in the AMEL pixel circuit, a series of floating "shield plates" were included over the drift region. These floating shield plates were placed between the drift region and the EL electrode. The purpose of the shield plates was to increase the break-down voltage performance of the device by providing isolation from the high voltage EL electrode. However, 2D simulations showed that with the presence of a thick oxide layer 'd', discrete device breakdown performance can be achieved even when no such shield plates are present over the drift region. Fig. 3-15 illustrates how the breakdown of an LDMOS device placed in an AMEL pixel circuit configuration approaches the breakdown of a discrete transistor as a function of 'd', the inter-level dielectric (ILD) thickness between the field oxide and the EL electrode.

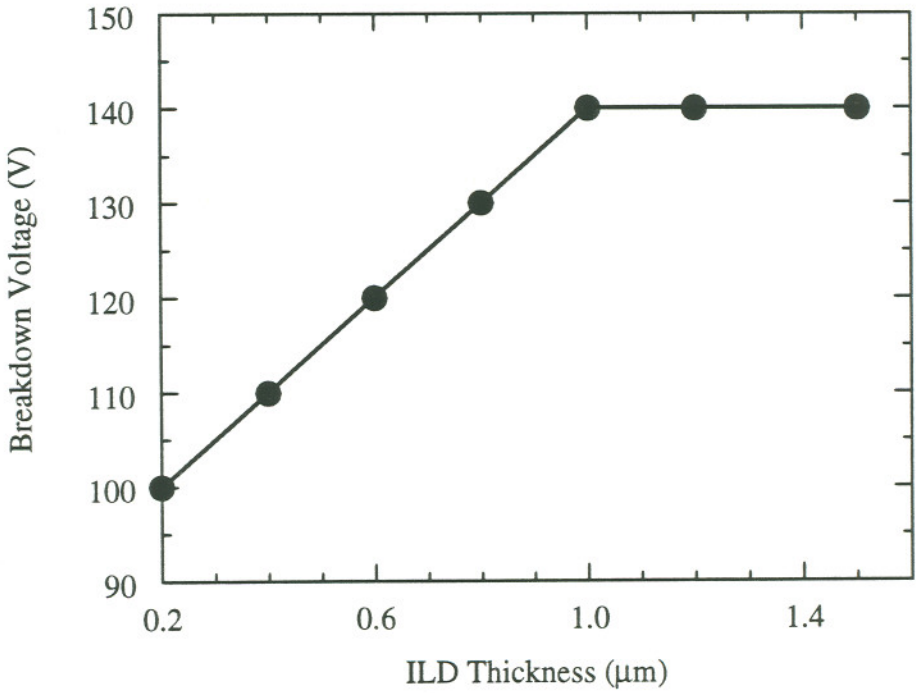

Figure 3-15: Breakdown voltage as a function of the ILD thickness 'd'

The breakdown voltage performance, as a function of the drift region doping, behaves in a similar fashion even with the presence of an EL electrode. Therefore, it can be concluded that with a set of more stringent design rules regarding field shield length and field oxide thickness, an LDMOS transistor can be placed in an AMEL pixel without any degradation in the discrete device breakdown voltage performance.

AMEL arrays fabricated without any "floating shield plates" and a thick ILD layer between the high voltage transistor and the EL electrode demonstrate excellent on-off behavior, which verifies the simulation results presented in this section.

3.6 Short Drift Region LDMOS Design for HVIC Technology

In this section, using 2D simulations and the design rules developed earlier in the chapter, it is shown that a 50V high-voltage IC technology can be developed using LDMOS structures with drift regions as short as 2 μm. Experimental results are then presented to demonstrate this concept, followed by detailed characterization of both the on- and off-state characteristics of the fabricated device.

The RESURF test devices were fabricated on ISE substrates with 1 μm buried oxide and 0.35 μm SOI film [35-36]. The mesa isolated devices were fabricated using ion implantation to form the drift, channel and the source-drain regions. The channel implant was performed to set the threshold voltage to about 1.8V. Both the gate and the field oxide were grown thermally in separate oxidation steps and n^+ poly Si is used as the gate and the field shield. Sputtered TiW was used for the source-drain contacts. The same metal layer was used as contact pads for electrical characterization. An HP 4156A parameter analyzer and a Micromanipulator probe station were used to characterize both on- and off-state characteristics of the fabricated transistors.

In Fig. 3-16 the breakdown characteristics of a 2 μm drift region LDMOS transistor is shown. The sharp reverse biased breakdown at ~50V is typical of electrical

breakdown caused by impact ionization. The ideal breakdown voltage of a 2 μm drift region device using eqtn. 3.6 was calculated to be 49 V, which is in excellent agreement with the experimental result. Although a 1μm thick buried oxide was used for this device, Medici simulations have shown that for a drift region length of 2 μm, much thinner buried oxide can be used to obtain ideal breakdown voltage performance. In fact, a standard buried oxide thickness of 0.35 μm used in commercially available SIMOX wafers will be sufficient to produce similar breakdown voltage performance.

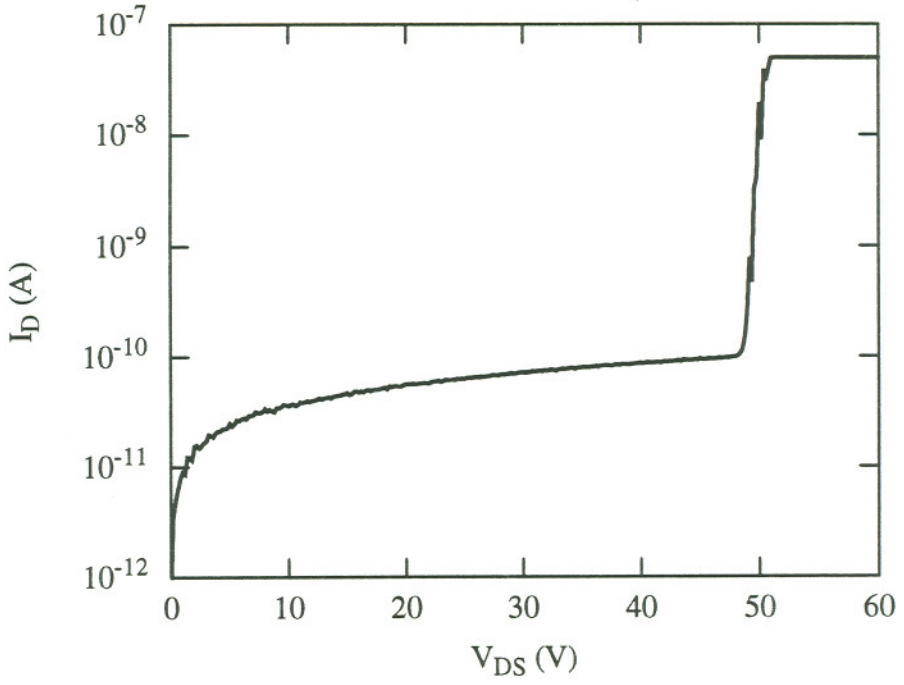

Figure 3-16: Reverse biased breakdown for the 2 μm drift LDMOS (W=10 μm)
(V_{GS}=0V, the wafer substrate was also grounded)

This device showed good subthreshold characteristics and the subthreshold swing S was measured to be 110 mV/decade. Figure 3-17 shows the subthreshold behavior of

the device. The subthreshold swing S can be further improved by thinning the gate oxide or lowering the substrate doping. The requirement for the high threshold voltage for the device increases the subthreshold swing. The device also has less than 1pA of leakage current per micron device width, as seen in Fig. 3-17.

The family of curves for the 2μm drift region LDMOS transistor is shown in Fig. 3-18. The drain current does not follow the simple square law relationship normally applied to describe the saturation current in long channel MOS devices due to mobility degradation at high gate biases.

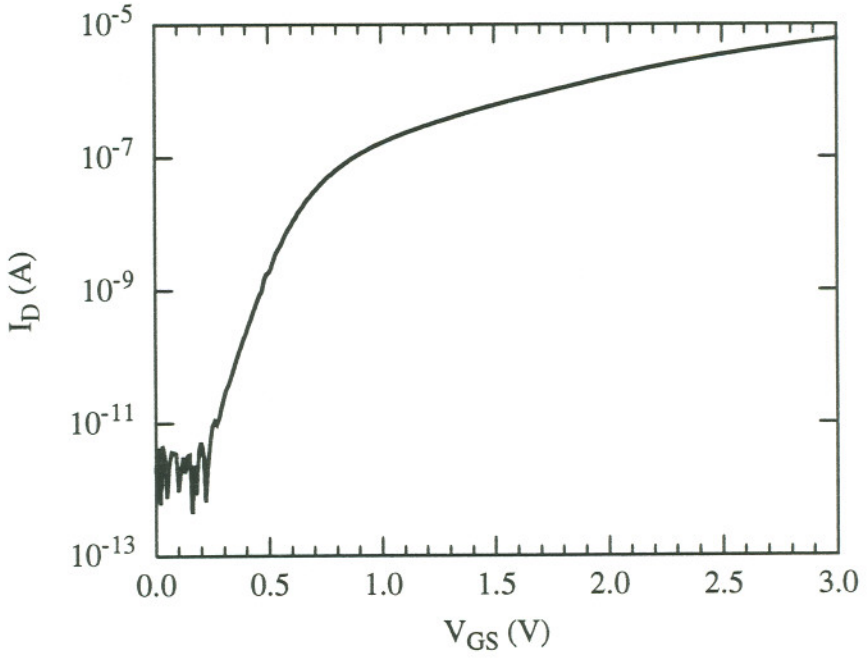

Figure 3-17: Drain Current as a function of the Gate Voltage (V_{DS}=0.1V)

Typical IV characteristics for the linear region is shown in Fig. 3-19. The linear region IV curves were also used to extract the on-resistance of the device. The specific on-resistance R_{sp}, defined as the product of the on-resistance and the area occupied

between the source and drain contact, was experimentally determined to be $2.91 m\Omega cm^2$ at a gate voltage of 15V. This value for the specific on-resistance is somewhat large as compared to the best available in the literature (IEDM 94, Texas Instruments, Ref. 51). The TI paper described an n-channel bulk LDMOS technology where a breakdown voltage of 47V and $R_{sp}=0.67 m\Omega cm^2$ were reported.

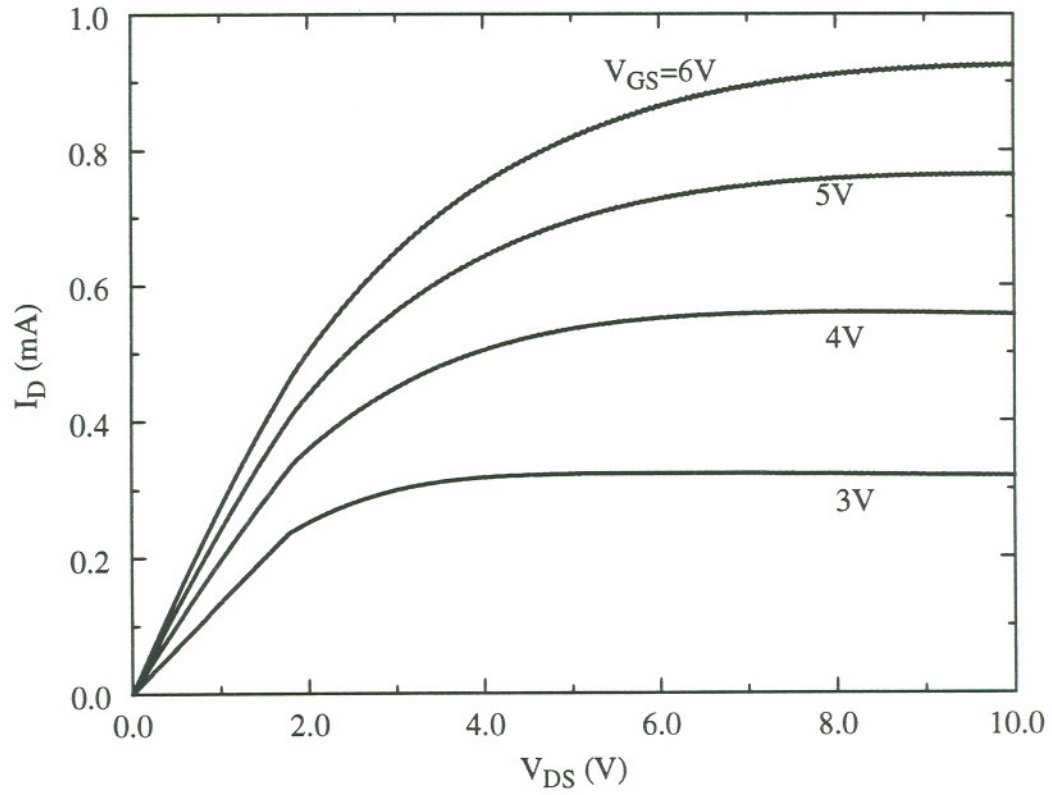

Figure 3-18: Family of curves for the 2 μm drift device

There is much room for improvement in the SOI LDMOS process used to fabricate the devices described in this thesis. The on-resistance of the LDMOS transistor consists of a channel and a drift region component. The channel contribution to the R_{sp} can be

reduced to 30-40% of its present value by the use of a sub-micron channel. A reduced channel doping will enhance the mobility. However, a thicker gate oxide may be needed to keep the threshold voltage at the present value. The TiW contact pads used in this test chip also contribute to higher resistance values as compared to the standard low-resistance aluminum pads and interconnects.

As pointed out the described LDMOS device was fabricated on an ISE wafer with 1 μm buried oxide thickness. For a SIMOX substrate with a 0.35 μm buried oxide, higher doping can be used without any penalty in the breakdown voltage. This increase in the drift region doping should lead to a significant reduction (~50%) in the drift region contribution to the on-resistance of the device.

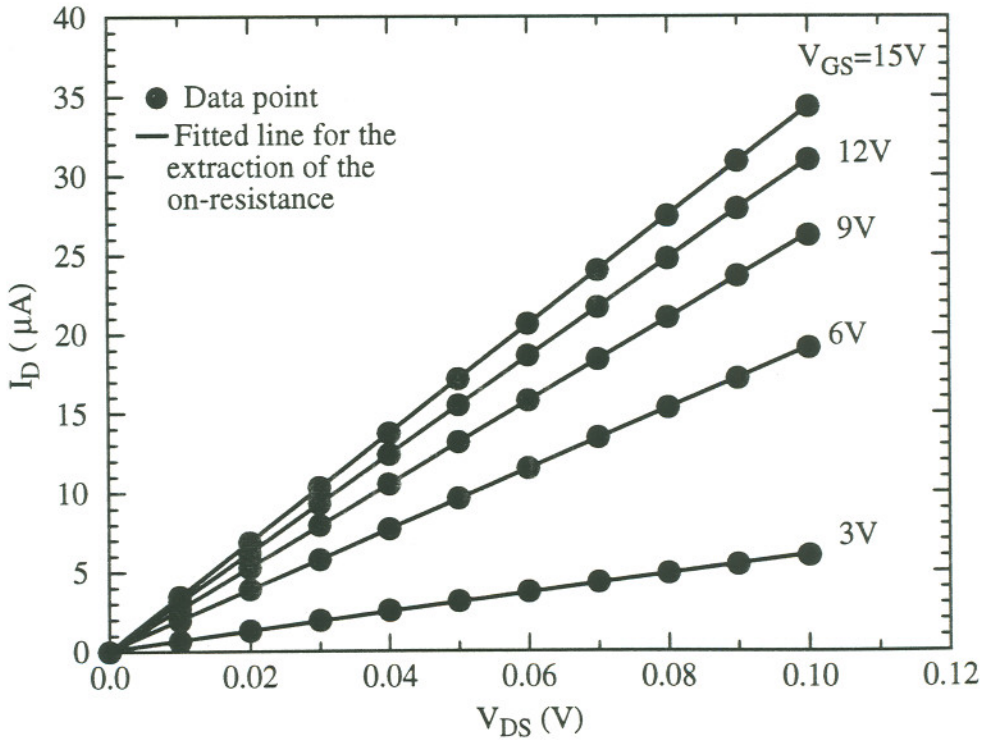

Figure 3-19: IV characteristics in the linear region

Finally, it is suspected that a "thin film effect" is responsible for the higher than expected drift resistance. During the oxide growth ~44% of the original SOI thickness is consumed and the actual thickness of the silicon film underneath the grown field oxide is ~0.18-0.2 μm. In such thin films, mean free path of the electron is shortened due to increased surface scattering from both the top and the bottom oxide interfaces. As a result, a reduction in the bulk mobility is observed resulting in an increase in the resistivity of the film. Therefore, a thicker film (>0.5 μm) is recommended for low on-resistance, short drift region high voltage LDMOS transistor fabrication.

Chapter 4
High Temperature Effects in SOI Devices

4.1 High Temperature Effects on SOI Devices

Some of the applications of smart power ICs require high temperature operations. For example, electronic components used in hostile environments, automotive and aircraft controls may need to operate at temperatures higher than standard 125°C requirement. Although some high temperature behavior of low voltage CMOS devices and ICs have been described in the literature [52-54], experimental data verifying the intrinsic advantages of high voltage SOI LDMOS design has not been available.

Thin film devices fabricated on SOI substrates are inherently suitable for high temperature operations. In a typical CMOS SOI device, the bottom junctions under the source and drain are replaced by the buried oxide layer. The significant decrease in the junction area reduces the leakage current at higher temperatures. In a traditional junction isolated bulk LDMOS device, the junction leakage currents at high temperatures become comparable to the on-current of the device. In this chapter, high temperature operation of both CMOS and high voltage LDMOS structures on SOI substrates are studied. We specifically look at the variation of important device parameters such as threshold voltage, on-current, on-resistance, and mobility as function of temperature. Leakage current, the primary limiting factor for the high temperature operation of IC components, is studied in detail. Standard analytic models, commonly used to describe MOS device behavior, have been used to explain the experimental data.

Both the NMOS and the LDMOS devices used in this study have been fabricated on ISE substrates with a 300Å gate oxide. The NMOS device (W/L=10/3 μm) had the standard lightly doped drain (LDD) structure and a threshold voltage of 1.25V at room temperature. A general description of the LDMOS device can be found in Chapter 3. The high voltage LDMOS transistor had a drift length of 10 μm. For electrical characterization we used a micromanipulator probe station, heat chuck and an HP 4156A parameter analyzer. The temperature of the heat chuck was maintained to within ±1°C of the set value. The measurements were performed in the dark in a standard Faraday box environment to shield the device under test from any electrical or optical noise. The temperature range considered for the NMOS device was 20 to 300°C and for the LDMOS device was 20 to 200°C.

4.2 On-State Device Behavior at Elevated Temperatures

4.2.1 Threshold Voltage

The threshold voltage of a MOS transistor can be expressed by the following expression [32]:

$$V_{th}(T) = \phi_{ms} + 2\phi_f + \frac{\sqrt{2\varepsilon q N_a (2\phi_f)}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \tag{4.1}$$

where ϕ_{ms} is the difference in the metal-substrate work function, ϕ_f is the substrate Fermi potential, N_a is the acceptor concentration in the channel, and Q_{ox} refers to the effective fixed charges per unit area at the oxide interface. The only temperature dependent terms on the right hand side of the equation is ϕ_f, which can be written as [32]:

$$\phi_f = \frac{kT}{q}\ln\left(\frac{N_a}{n_i(T)}\right) \tag{4.2}$$

where n_i is the intrinsic carrier population and is a strong function of the temperature and the bandgap. The intrinsic carrier concentration can be expressed as [32]:

$$n_i(T) = 3.87x10^{16}T^{\frac{3}{2}}e^{\frac{-E_g}{2kT}} \text{ cm}^{-3}. \tag{4.3}$$

For the temperature range under consideration, the change in the bandgap is too small to have any appreciable effect in the device electrical parameters and will be neglected.

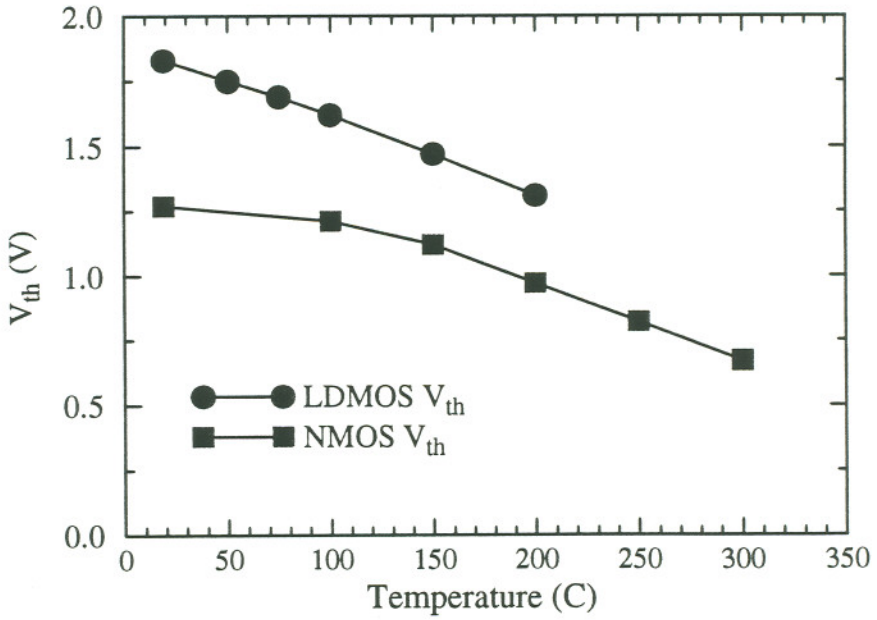

Figure 4-1: V_{th} as a function of temperature

The threshold voltage variation of both the NMOS and the LDMOS transistors, shown in Fig. 4-1, is due to the increase in the intrinsic carrier concentration in the channel

region. The threshold voltage variation of ~-3mV/°C is observed in the NMOS device. For the LDMOS device the variation is ~-2.9mV/°C.

4.2.2 Channel Mobility

The NMOS and LDMOS channel mobilities were extracted by differentiating the I_D-V_{GS} characteristics obtained at a small drain bias (0.1V) and using the following expression:

$$\frac{\partial I_D}{\partial V_{GS}} = \mu_{eff}(T) \cdot \frac{W}{L} \cdot C_{ox} = g_m \tag{4.4}$$

where g_m is the transconductance of the device and the other terms have their usual meaning. The maximum transconductance was used to obtain the mobility values at a given temperature. The extracted mobility values are plotted as a function of temperature in Fig. 4-2 (NMOS).

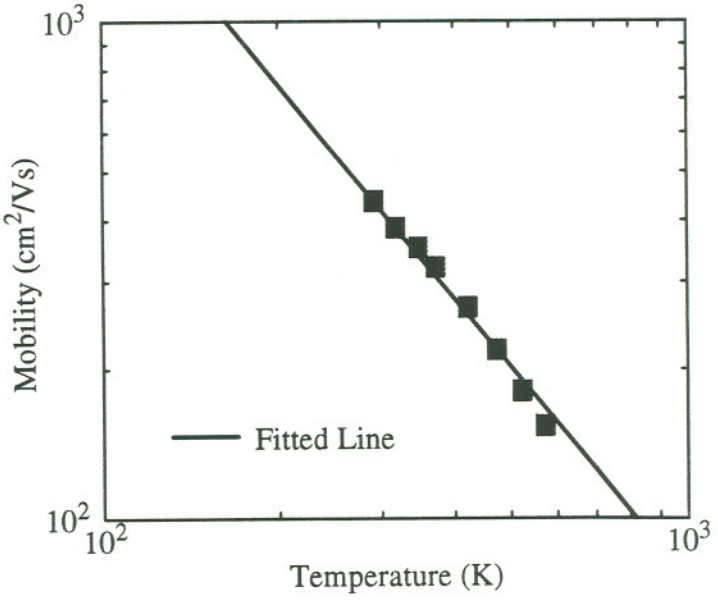

Figure 4-2: Mobility as a function of temperature (NMOS)

For the LDMOS transistor, the extracted transconductance values were first normalized to the room temperature value since it was not possible to extract the effective channel length and the corresponding mobility values. Since the geometric parameters of the device do not change as a function of temperature, the normalized transconductance values plotted in Fig. 4-3 can also be considered as the normalized mobility for the LDMOS transistor.

The temperature dependence of mobility is usually modeled as [53-54]:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{4.5}$$

where m~1.5 for CMOS devices. The mobility decreases as more acoustic phonon scattering takes place at higher temperatures [37]. The fitted lines in both Figures 4-2 and 4-3 have m~1.43. The $T^{1.43}$ temperature dependence for the LDMOS device is surprising since m=2.5 has been reported for a bulk LDMOS structure due to higher doping concentrations in the LDMOS channel region. However, in this work the channel and the drift region effects could not be separated.

In order to study the effects of temperature on the channel and the drift (or bulk) mobility independently, a special test structure is needed. In this test structure, the DMOS channel is self-aligned to the source and drain n^+ regions, and the drift region is eliminated. The device essentially looks like a simple NMOS structure with a heavily doped DMOS channel doping [54]. Since the device uses an identical gate processing and channel doping as the actual LDMOS transistor, the electrical characteristics will emulate the LDMOS channel. Unfortunately, this type of test structure was not available in the test chip used in this work.

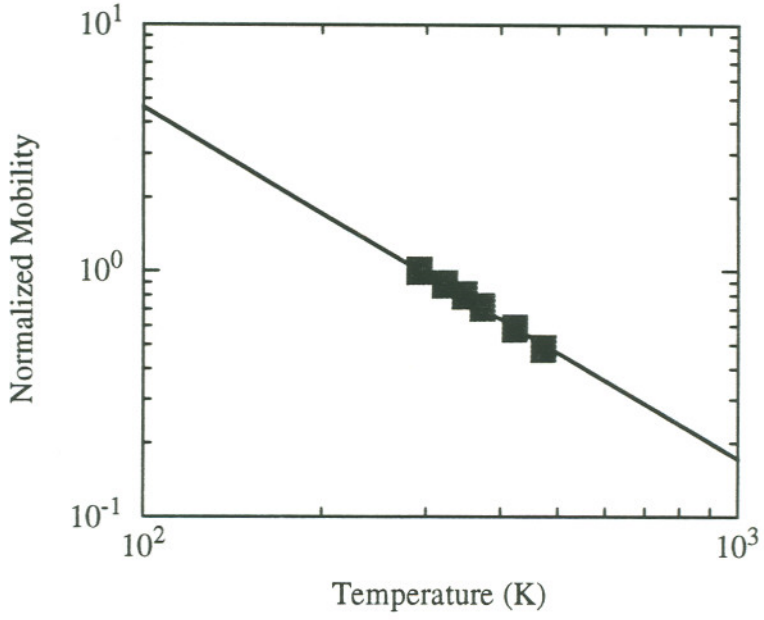

Figure 4-3: Mobility as a function of temperature (LDMOS)

4.2.3 On-state Resistance

The on-resistance of a MOS device can be expressed by the following expression [54]:

$$R_{on} = R_{ch} = \frac{L}{W\mu_{eff}(T)\, C_{ox}\,(V_{GS} - V_{th}(T))}. \tag{4.6}$$

For a fixed value of gate voltage the on-resistance is governed by two competing mechanisms. The reduction in channel mobility causes an increase in the on-resistance. On the other hand, the lowering of the threshold voltage at higher temperatures tend to lessen the value of the on-resistance for a fixed gate voltage. However, for large gate to source voltages the mobility term dominates and the channel resistance increases as a function of temperature. In Fig. 4-4, the measured on-resistance values have been plotted and a simple linear fit was found to be sufficient to describe the behavior at elevated tempera-

tures. The slope of the fitted line was found to be ~12Ω/°C.

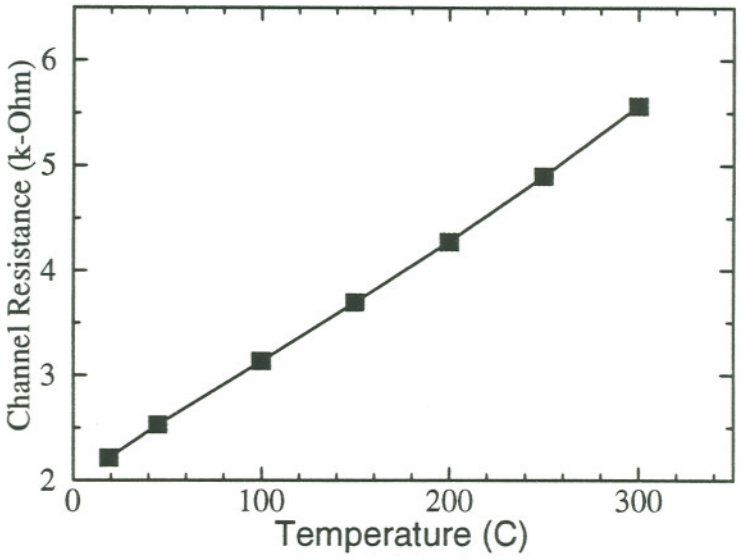

Figure 4-4: R_{on} as a function of temperature (NMOS)

For the LDMOS transistor, the on-resistance is comprised of both the channel and the drift region component.

$$R_{on} = R_{ch} + R_{drift} \tag{4.7}$$

While the channel component can still be expressed by eqtn. 4-6, the drift component is described by the following expression [55]:

$$R_{drift} = \frac{\rho}{\pi W}\left[\ln\left(\frac{L - r_1}{r_1}\right) + \ln\left(\frac{L - r_2}{r_2}\right)\right] \tag{4.8}$$

where ρ is the resistivity and L is the effective length of the drift region, r_1 is the effective radius of the current source at the channel end and r_2 is the effective radius of the current

sink at the drift- drain interface. Since the bulk resistivity showed a positive temperature coefficient, we expected the drift region resistance to increase as a a function of temperature. Figure 4-5 shows the increase in the total on-resistance of the measured LDMOS structure.

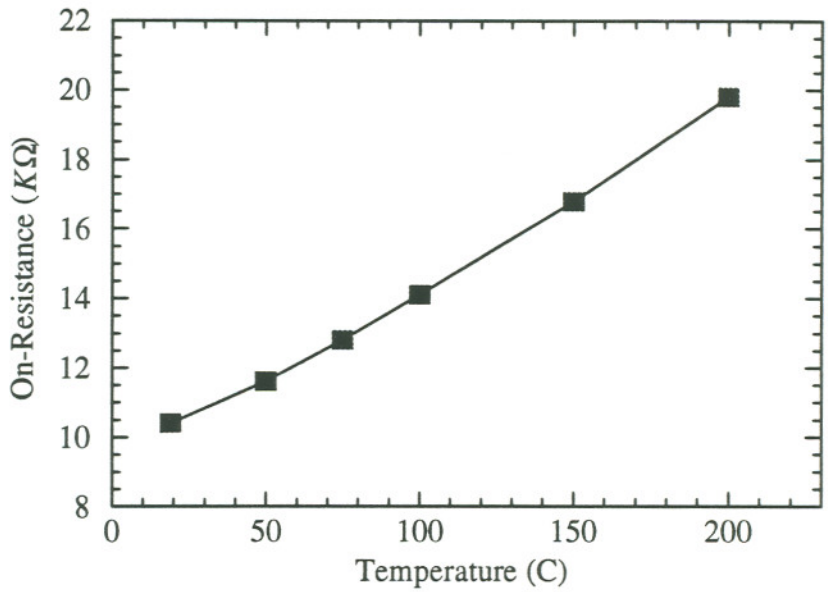

Figure 4-5: R_{on} as a function of temperature (DMOS)

For long drift length devices (> 40μm), thick buried oxide layers (>4μm) are necessary to obtain the optimum breakdown voltage [10]. However, the optimum drift region doping must be lowered with increasing buried oxide thickness. In a lightly doped drift region, the intrinsic carrier concentration may equal the n-type dopant concentration at an ambient temperature below 300°C. In such a case, the drift region resistance may actually decrease for further increase in the temperature.

4.2.4 Saturation Current

The saturation current of a long channel MOSFET can be expressed in the following fashion [32]:

$$I_{Dsat} = \frac{\mu_{eff} C_{ox} W}{2L} (V_{GS} - V_{th})^2 . \tag{4.9}$$

As mentioned in chapter 3, the IV characteristics do not quite follow this simple square law relationship at high gate voltages. Mobility and the threshold voltage are the two temperature dependent terms on the right hand side of this equation. At high gate voltages, the mobility degradation is the dominating factor as compared to the decrease in the threshold voltage. As a result, a reduction in saturation current is observed as the operating temperature is increased. This effect is shown in Fig. 4-6 where the NMOS IV characteristics measured at different ambient temperatures have been plotted. Similar effects have been observed in the saturation characteristics of the LDMOS transistor.

The most interesting effect observed in Fig. 4-6 is the absence of the "kink" effect at higher operating temperatures. There are two possible explanations for this disappearance. First, the holes generated by the impact ionization recombine with the thermally generated minority carriers (electrons) in the transistor body. As a result, there are not enough holes available to raise the potential of the transistor body. The source-body junction remains reverse biased and the kink effect disappears.

The other explanation involves the shorter mean free path of electrons at elevated temperatures. Shorter mean free path reduces the impact ionization rate, which causes fewer hole generation. Since no significant change in the breakdown voltage is observed at high temperatures, it can be concluded that the change in the impact ionization rate is not significant and the recombination process in the transistor body is the dominating factor in the disappearance of this parasitic bipolar effect.

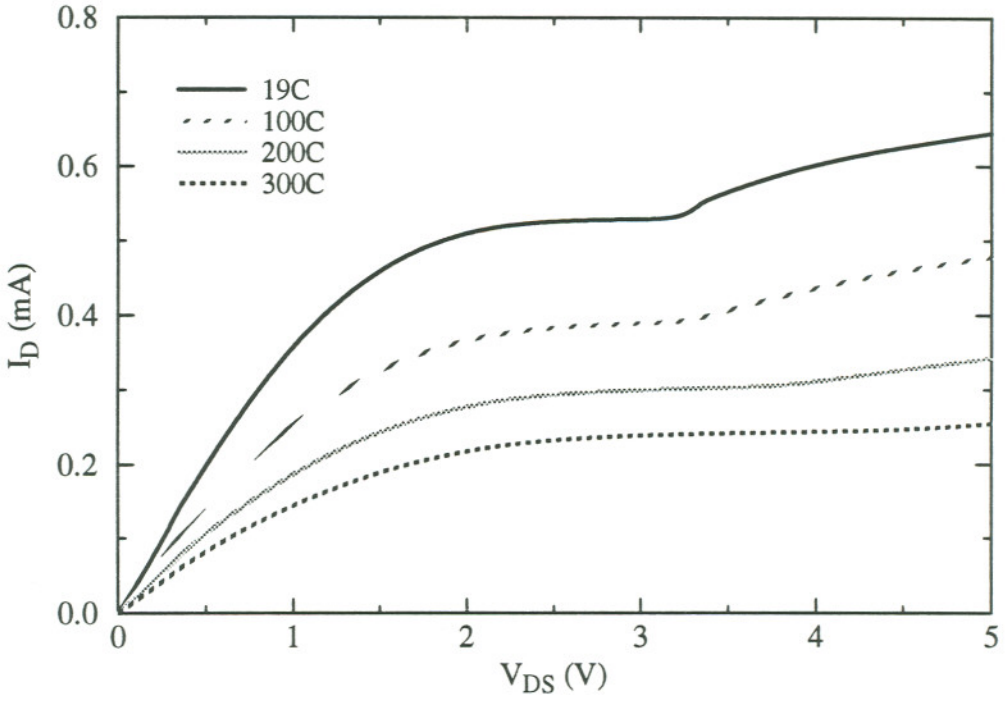

Figure 4-6: Disappearance of the kink effect (V_{GS}=5V)

4.3 Off-State Device Behavior at Elevated Temperatures

Breakdown voltage and the leakage current are the two off-state parameters that are of interest. It has been reported that the reverse biased breakdown voltage shows a very small positive temperature coefficient [54]. In the measurements performed as part of this work, no significant change in the breakdown voltage characteristics at high temperatures were observed. The severe increase in leakage current, however, is the most pressing issue for high temperature operation of devices and circuit components and is discussed in detail.

The leakage current across a reverse biased pn junction can be expressed by the following eqtn. [40]:

$$I_{rev} = qA\sqrt{\left(\frac{D}{\tau}\right)}\frac{n_i^2}{N} + \frac{qAn_iW}{\tau} \tag{4.10}$$

where A is the junction area, τ is the generation lifetime, and W is the width of the depletion region. The first term on the right hand side of the equation represents the diffusion component from generation in the neutral region and the second term refers to the depletion region generation component of the leakage current.

As seen in eqtn. 4.10, the generation component increases as $e^{-\frac{E_g}{2kT}}$ and the diffusion component increases as $e^{-\frac{E_g}{kT}}$ as a function of temperature. The measured behavior is seen in Fig. 4-7. The generation component is the dominating mechanism for temperatures lower than 150°C while the diffusion component dominates at higher temperatures. At lower temperatures the value of the leakage current is quite small (in the pico-ampere range) and therefore less accurate. The drawn line with $E_g/2$ slope does not fit well due to the "noisy" data in the very low current regime. In the high temperature regime, the total leakage current is dominated by the diffusion component and the drawn line with slope E_g fits nicely with the measured data points.

In Fig. 4-8, the subthreshold characteristics of the NMOS device have been plotted for three different temperatures. Although the off-current at zero volt gate bias is about 300 times smaller than the on-current at 3.5V gate bias at 300°C, the severe increase in the subthreshold slope caused by the high leakage current degrades the device performance.

For the LDMOS structure, the leakage current at 200°C was only 50 pA and the ratio of the off-current (@V_{GS}=0V) versus on-current (@V_{GS}=3.5V) was ~1.4×10^{-5} A. In comparison, in a bulk LDMOS structure the reported value for I_{off}/I_{on} ratio at 200°C was

greater than $1x10^{-2}$ [54]. The impressive improvement in the leakage current characteristics results from the severe reduction in the junction area. In an SOI device, the effective junction area for leakage current involves the vertical junction between the channel and drift region as opposed to the bulk LDMOS transistor in which both the n-drift/p-body (or channel) junction and the n-epi/p-substrate junction contribute to the leakage current (see Figures 3-1 and 3-2 for comparison). In fact, the n-epi/p-substrate junction leakage dominates the high temperature off-state current conduction [54]. This junction is totally eliminated in an SOI LDMOS design which leads to significant improvement in the high temperature leakage characteristics.

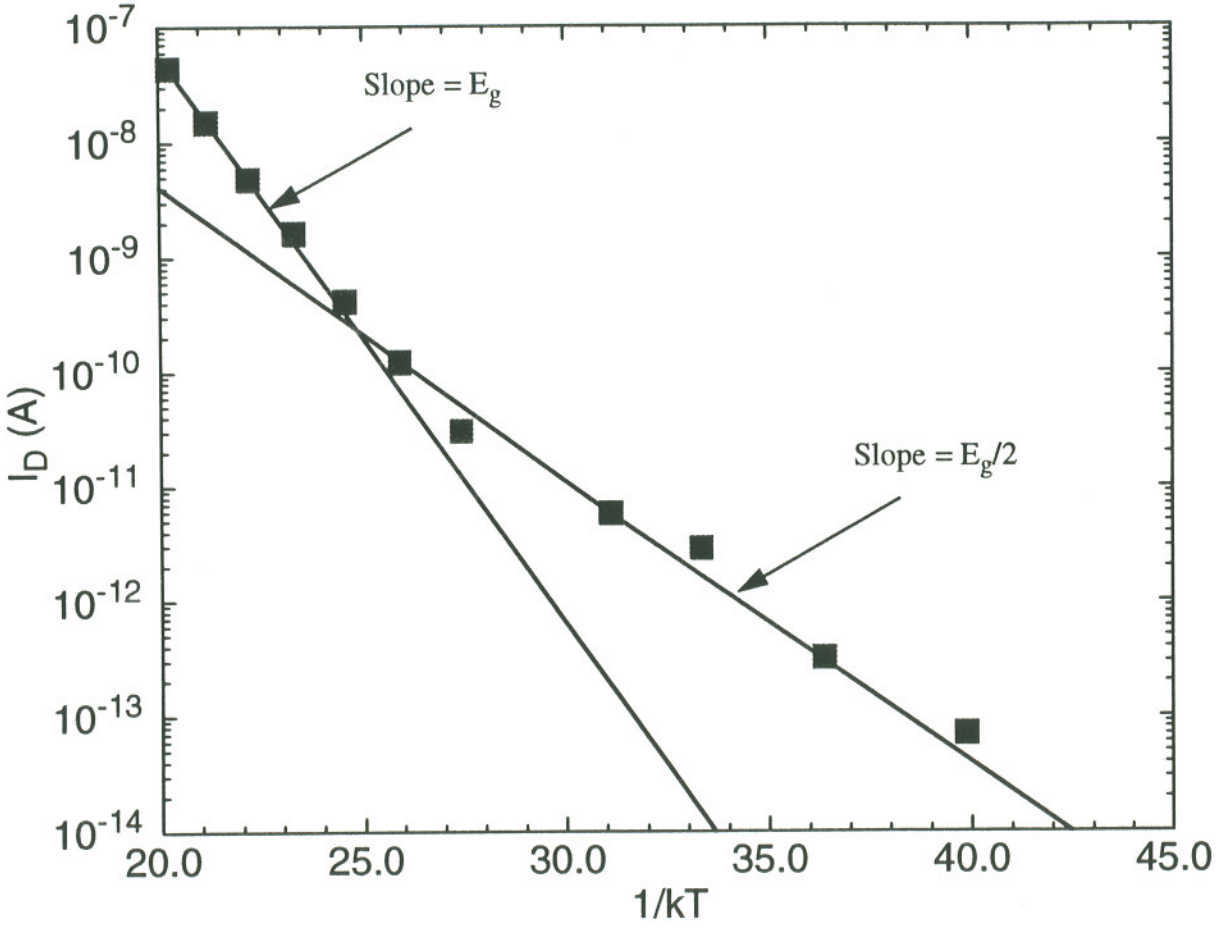

Figure 4-7: Leakage Current as a function of Temperature (NMOS)

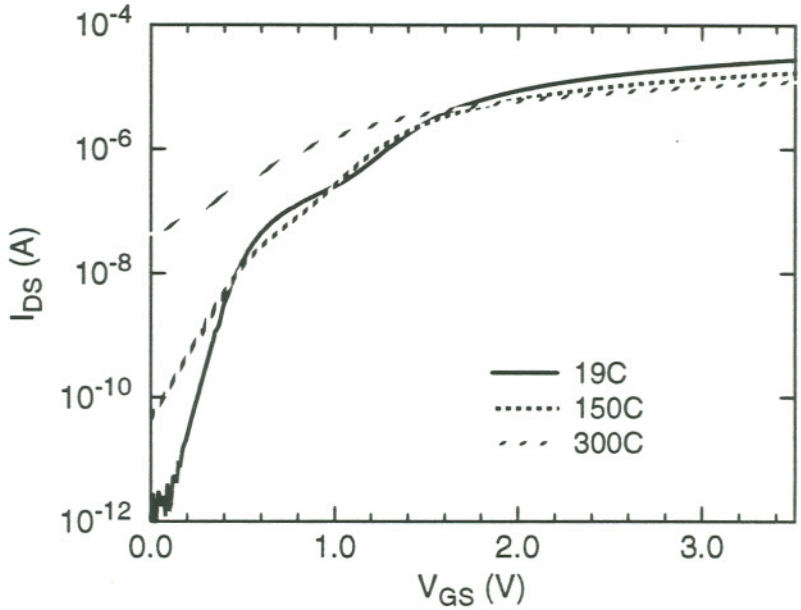

Figure 4-8: Subthreshold current as a function of temperature (NMOS)

The exponential increase in the leakage current poses a fundamental limitation on the maximum operating temperature of semiconductor devices [54]. The high leakage current prevents any reasonable turn-off of the device, causing high amount of static power dissipation. In this chapter, it is shown that high-voltage SOI devices demonstrate significantly lower leakage currents at elevated temperatures as compared to that of the bulk devices. Thus for high temperature operations dielectrically isolated SOI structures are superior to the bulk devices, which use traditional junction isolation.

Chapter 5
Hot Carrier Reliability for SOI Devices

5.1 Hot Carrier Reliability

The aggressive scaling of MOS devices has been at the center of intense research and development activities for the last thirty years. According to the historical trends, the minimum feature size of MOS structures in logic and memory ICs has been decreasing by a factor of two in every six years [56]. The goal is to increase the packing density and achieve higher circuit speed. The conventional scaling laws usually involve shrinking of device dimensions - reduction of junction depths, thinning of the gate oxide, and increase in the channel doping concentrations. Although the "constant field" scaling suggests a proportional reduction in the power supply voltage V_{DD}, it was only recently that the manufacturers have started to address this issue.

A decrease in V_{DD} translates into a reduction in the drive current and subsequent increase in the delay time of the circuit. As a result, chip designers are reluctant to scale the power supply voltage. However, in the recent years microprocessors and memory chips with reduced on-chip power supply voltages have been introduced for two primary reasons - hot electron reliability and power consumption.

MOS devices with channel lengths of 2 μm or smaller suffer from hot carrier damage - a long term reliability hazard due to the high electric fields in the device. This reliability hazard is particularly worrisome for deep sub-micron (<0.25μm) devices. NMOS devices (L_{eff}=0.15μm) showed evidence of hot carrier damage even when the

power supply voltages was scaled to 1.8V [57].

Hot carriers in a semiconductor material have significantly higher kinetic energy than the average carrier population. The kinetic energy of an accelerated electron can be expressed as $E-E_c = (3/2)\ kT_e > (3/2)\ kT$, where E is the energy of the electron, E_c is the energy level of the bottom of the conduction band and T_e is the effective temperature of the "hot" electron [58]. This effective temperature may be substantially higher than the ambient temperature. The electrons gain this additional kinetic energy as they accelerate under the high lateral electric field while traveling from the source to the drain.

The fraction of the electrons arriving at the channel-drain junction with sufficient kinetic energy to surmount the surface potential barrier at the $Si-SiO_2$ interface will get injected into the oxide. High energy electrons may also generate electron-hole pairs, which may cause additional damage to the oxide interface near the drain region of the device. The vertical electric field due to the applied gate bias may also supply the additional energy needed to surmount the interface barrier [58]. The peak electric field at the drain junction occurs near the $Si-SiO_2$ interface. High electric fields near the channel or the current path increases impact ionization and subsequent hot electron damage to the interface.

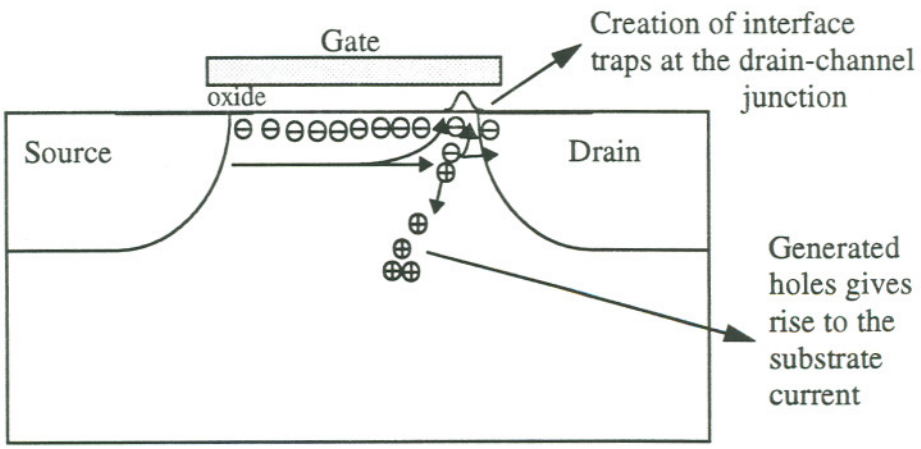

Figure 5-1: Impact ionization and hot carrier damage

The high electric field in a short channel NMOS device is caused by two primary reasons. First, if the channel is scaled without a reduction in the power supply voltage the electric field increases by the inverse of the same scaling factor. Higher channel doping, shallower junctions, and thinner gate oxides are used in sub-micron devices to battle short channel effects such as V_{th} roll-off, punchthrough, and degradation in the subthreshold characteristics. These measures also increase the electric field at the drain-channel interface. As a result, a high electric field peak arises at the drain-channel junction near the Si-SiO_2 interface. This lateral electric field that gives rise to the high energy electrons must be reduced to guarantee the long term reliability of the IC components.

The damage to the device or the oxide interface takes place in the form of interface traps and trapped charges. The trapped charges in the oxide cause a shift in the threshold voltage of the device by changing the flatband voltage of the MOS device. The generated interface traps cause mobility degradation in the channel.

It is recognized that the interface trap generation is the primary degradation mechanism in a hot electron damaged NMOS device. A bond-breaking model has been proposed to describe the creation of additional interface states [59]. According to this model, hot electrons break the silicon-hydrogen bond at the oxide interface. The Si-H bond at the interface are believed to be formed during the BPSG flow in steam, CVD of Si_3N_4, or the final post metal thermal anneal in forming gas (N_2+H_2) [60]. If the trivalent Si atom recombines with the hydrogen atom, no interface trap is generated. However, if the hydrogen atom diffuses away from the interface, a new interface trap is created.

The minimum kinetic energy needed for an electron to break such a Si-H bond can be calculated by adding the height of the potential barrier (~3.2 eV) and the bond strength (0.3eV). The potential barrier that a hole in the valence band must overcome at the oxide interface is significantly higher (4.5eV) than that seen by an electron in the conduction band. Holes also have smaller mean free path. Thus holes are significantly "cooler" than the electrons and are less effective in creating interface traps. As a result, the hot carrier

damage is primarily caused by the electrons in an NMOS device. Hot carrier (hole) effects even in sub-micron PMOS devices are not as significant as compared to the reliability problems faced by similar sized NMOS devices. However, it should be mentioned that while the probability of a hole injection is small, an injected hole may cause 2000 times more damage as compared to that of an electron [58].

In this chapter, it is shown that the degradation models developed for the characterization of hot electron stressed bulk MOS devices can be applied to partially depleted SOI devices as well. Due to the existence of an inherent parasitic bipolar device, the SOI NMOS devices demonstrate low breakdown voltages, which causes difficulty in conducting accelerated reliability testing at high drain biases. A solution to this problem is described. Before presenting our experimental results, hot electron resistant device structures are briefly reviewed.

5.1.1 The Lightly Doped Drain (LDD) Structures

As the devices are scaled into the sub-micron regime, several design and process changes have been implemented for hot electron reliability. They include the reduction of the power supply voltage, introduction of the lightly doped drain (LDD) structure, and modifications in the gate oxide processing conditions.

The LDD structure was first described by Ogura *et al.* in 1980 [61]. In this type of drain configuration, two separate implants are used to form the source-drain region. In a typical LDD process sequence, a shallow low dose drain implant is first performed (self-aligned to the deposited poly-gate). In the next step, a blanket spacer oxide deposition takes place. The etching of the spacer oxide creates the window for the heavy dose source-drain implant. The final resultant structure is shown in Fig. 5-2.

The principal advantage of the LDD structure is the reduction of the electric field peak at the channel-drain junction, the area where impact ionization rate is high and high

number of interface traps are created.

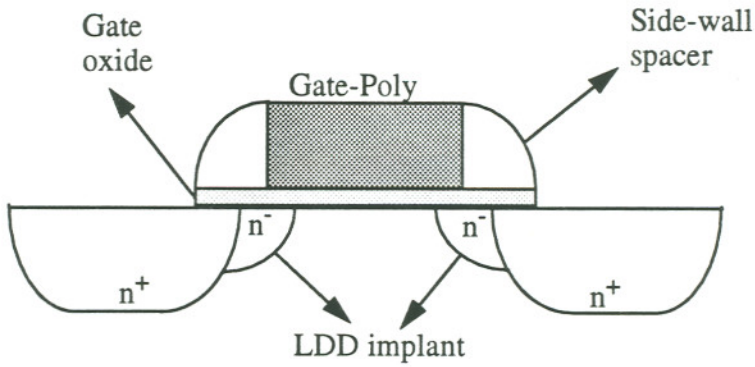

Figure 5-2: Schematic cross-section of an LDD Device

However, the advantage due to the reduced electric field in an LDD structure also causes increased series resistance due to lightly doped source-drain extensions. This addition in the series resistance causes a drop in the drain current. Therefore, the trade-offs regarding an LDD design must be considered during the design of the device. A higher LDD dose not only decreases the series resistance but also reduces the hot carrier robustness of a given structure. Many advanced source-drain doping structures have been implemented in the last ten years to battle the trade-offs regarding the LDD implants. For example, Large-angle-Tilt Implanted Drain or LATID structures take advantage of a tilt implant to create shallow n^- junctions [62]. The LATID process also offers higher throughput and more flexibility in the process design.

The other approach in fighting this reliability problem in sub-micron MOSFETs involve development of process technology to produce gate oxides with higher hot carrier resistance. This means the gate dielectric should have very low densities of interface traps, trapping centers, and fixed oxide charges. It has been found that the hydrogen atoms satisfying the dangling bonds at the interface have lower bond strength and make the device more prone to hot carrier damage. A reduction in the hydrogen and moisture

content of the oxide film has led to more reliable devices.

Another approach involves a modification of the chemical composition of the gate oxide [60]. Incorporation of nitrogen is performed by exposing the gate oxide to NH_3 at atmospheric pressure and high temperatures. Nitrogen incorporated in the gate oxide provide higher resistance to interface trap generation. Si-N bonds at the interface are known to have higher bond strength as compared to that of Si-H bond. N_2 content also increases the dielectric strength of the gate oxide.

5.2 Lifetime Prediction Using Accelerated Stressing

In order to characterize and quantify the hot electron damage, important device parameters such as threshold voltage (V_{th}), linear region transconductance (g_m), subthreshold swing (S), and drive current (I_D) are usually plotted as a function of the stress time. Most hot electron reliability studies involve applying DC stress voltages to the device for an extended period of time. The applied stress biases are usually higher than the normal operating voltages in order to accelerate the hot carrier damage and generate information about the long term reliability in a relatively short amount of time. Several drain voltages are usually chosen so that the damage under normal operating conditions can be extrapolated from the generated data.

Devices are often designed to provide at least ten years reliable operation [60]. The hot electron damage is often monitored by the substrate current, which provides important insight regarding the impact ionization rate at a given bias condition. The life-time of a device can be arbitrarily defined as the time required for 1 to 10% shift or degradation in a measured electrical parameter such as the threshold voltage or the drain current. In our experiments, the reduction in the linear current was monitored as a measure of the device degradation.

An example of finding the optimum stress point is provided in Fig. 5-3. First, the

drain is biased to 4.5V and the gate voltage is sweeped from 0 to 4.5V. The substrate current is measured as a function of the gate voltage. The gate voltage at which the substrate current reaches a peak value is the optimum stress point. For this bias, the maximum amount of impact ionization takes place and the hot electron damage to the interface is also at its highest for the given drain bias. At first the substrate current increases with gate bias as more electrons become available to cause impact ionization which gives rise to the hole current collected at the substrate contact. However, as the gate voltage increases even further, the electrons in the channel slows down due to the mobility degradation caused by the vertical electric field and the substrate current decreases with increasing gate voltage. As seen in Fig. 5-3, the optimum gate voltage is 2.7V for a drain bias of 4.5 V.

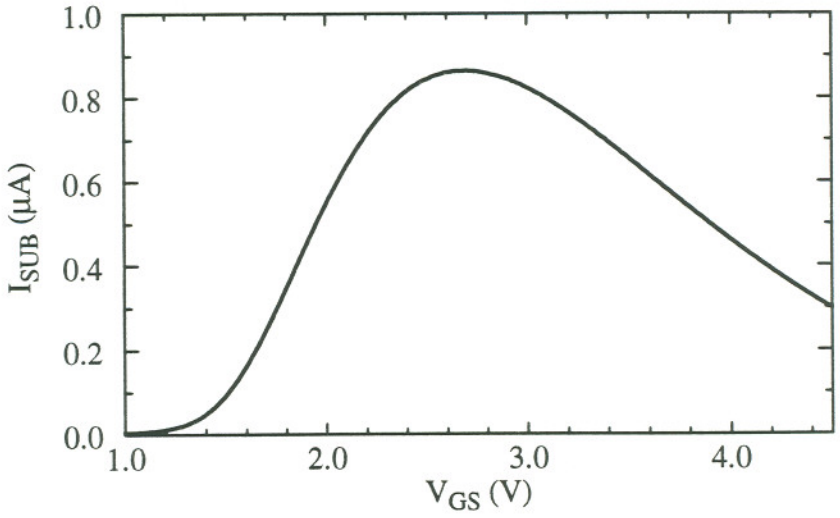

Figure 5-3: Determination of optimum stress point (L_{eff}=1.7 μm, V_{DS}=4.5V)

Based on empirical data, models have been developed to describe the device degradation as a function of stress time. It has been found that threshold voltage shift, linear current degradation and the increase in the subthreshold swing of a device follow a

simple power-law relationship. The following expressions are often used to fit the experimental data [59, 60, 63]:

$$\frac{\Delta I_D}{I_D} = At^m, \tag{5.1}$$

$$\frac{\tau I_D}{W} = B\left[\frac{I_{sub}}{I_D}\right]^n, \tag{5.2}$$

where ΔI_D is the linear current degradation, t is the stress time, τ is the device lifetime, and W is the width of the device. Also, 'A', 'm' and 'B', 'n' refer to fitting parameters for a given technology. There have been attempts to define universal values for m and n [59]. However, it is generally acknowledged that these parameters must be extracted from the experimental data for given technology. In equation 5.2, I_{sub} and I_D refer to the substrate and the drain current at a given stress voltage.

In this experiment, partially depleted LDD NMOS devices (L_{eff}=1.7μm) on ISE substrates with 300Å gate oxide were used. A special p^+ body contact, shown in Fig. 5.9, was provided such that substrate current could be monitored. Device stressing and characterization is performed by a HP 4156A parameter analyzer. The drain current degradation was monitored at regular intervals and is plotted in Fig. 5.4. Eqtn. 5.1 was used to fit the generated data and the value of 'm' was found to be 0.29. The values reported in the literature ranges from 0.1 to 0.8, depending on the technology (channel length, gate oxide, LDD formation, etc.) and the bias voltages used during the stress.

The shift in the threshold voltage and the linear region current can be seen in Fig. 5.5. A 9% decrease in the transconductance was observed after 2000 minutes of stressing. The device degradation was not severe as the chosen drain stress voltage (V_{DS}=4.5V) in this experiment is significantly lower than the bias that would typically be used (6-8V) for a comparable bulk device. Low breakdown voltage of PD SOI devices prevent stressing

at higher drain voltages.

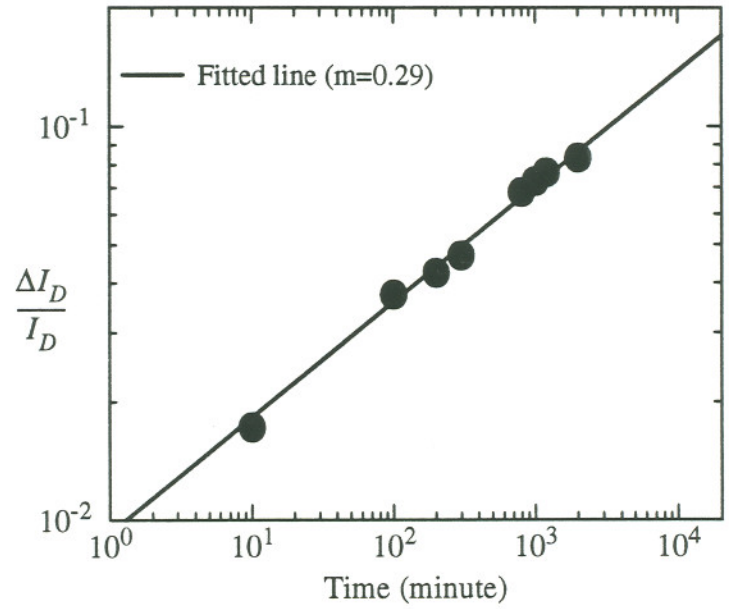

Figure 5-4: Linear current degradation (V_{DS}=4.5V, V_{GS}=2.7V)

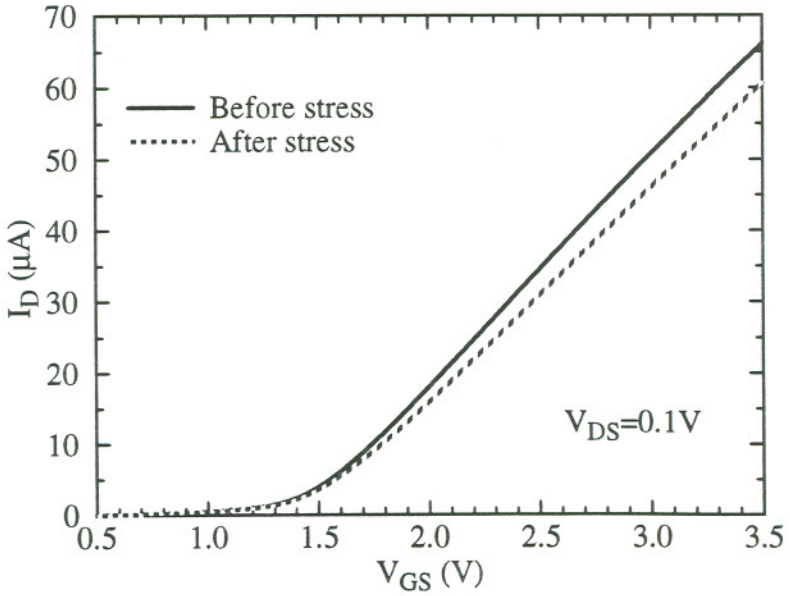

Figure 5-5: Change in V_{th} (total stress time = 2000 minutes)

Two more identical devices were also stressed at V_{DS}=4.25V, V_{GS}=2.45V and V_{DS}=4.0V, V_{GS}= 2.2V, respectively. The current degradation data for the other transistors were plotted and the power-law relationship given by eqtn. 5-1 was used to fit the data and obtain the 'm' values. Fig. 5-6 was plotted by measuring the ratio of the substrate current versus the drain current for each transistor at the respective stress voltages. Lifetime τ was arbitrarily defined as the stress time needed for 3% degradation in the linear current measured at V_{DS}=0.1V and V_{GS}=3.5V. The generated experimental data agrees well with the traditional bulk hot electron model (eqtn. 5.2) which predicts a power law relationship between the lifetime and the substrate current.

More data points at higher drain biases could not be generated because of the low forward bias breakdown voltage of the NMOS devices due to the inherent parasitic bipolar effect. Lowering drain voltages below 4V does not allow fast enough degradation useful for accelerated testing. A brief discussion on the parasitic bipolar effect and a possible solution to this problem is presented in section 5.4.

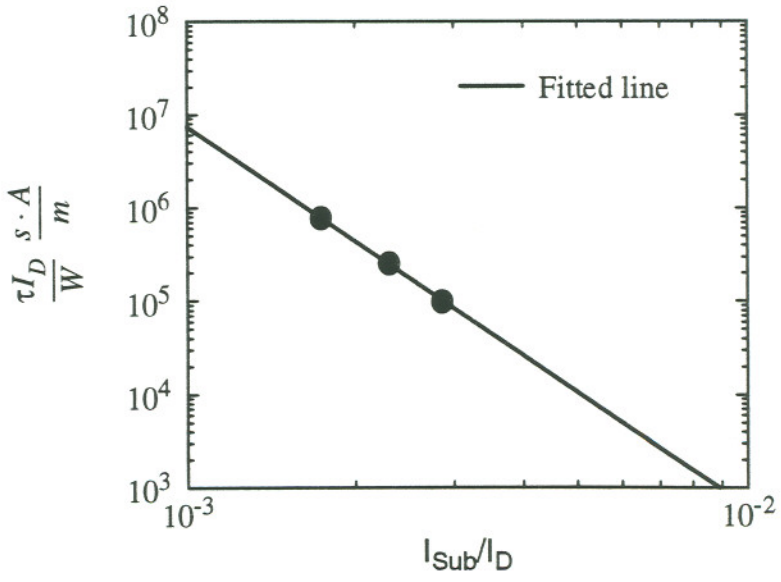

Figure 5-6: Lifetime prediction from the generated stress data

The drain current as a function V_{DS} has been plotted in Fig. 5-7. The linear region characteristics are severely affected as a result of the hot electron stress which increased the local flat band voltage and decreased the surface mobility of the device. However, current degradation in the saturation region has been affected to a lesser extent as the saturation current is almost independent of the physical properties of the region between the pinch-off point and the drain. Most of the interface damage due to the hot carriers are located in the pinched-off region near the drain-channel junction. As a result, the saturation current is less affected by the generated traps as compared to the current in the linear region. This phenomenon also indicates the strong localized nature of the damage.

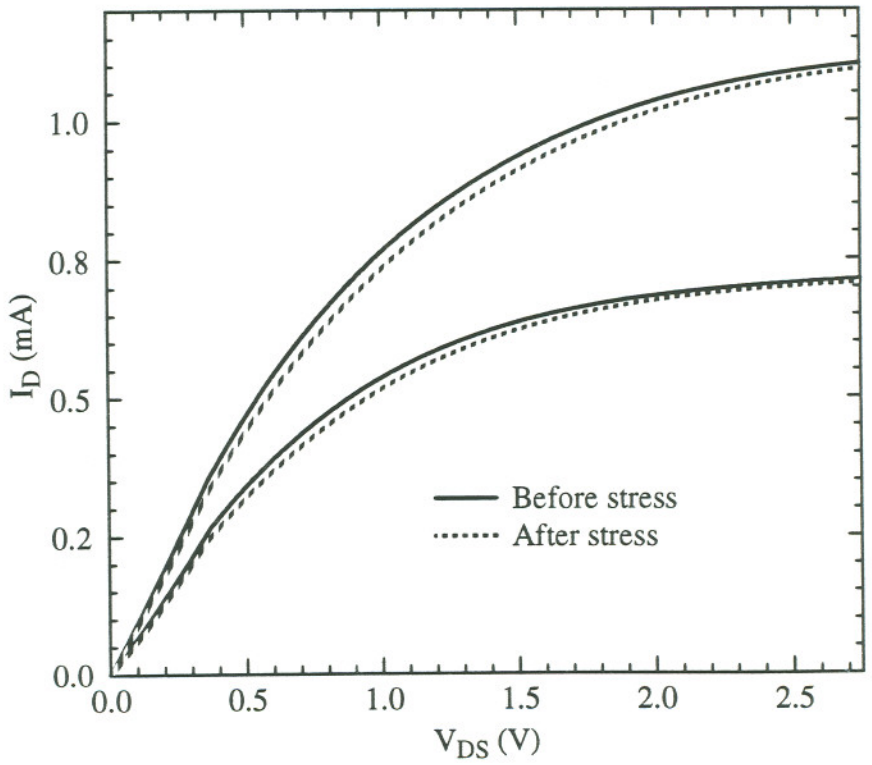

Figure 5-7: Current degradation: linear and saturation regions (V_{GS}= 4, 5V)

An AC lifetime can then be calculated knowing the lifetime obtained from the DC stress procedure. Pulsed measurements performed on CMOS inverters were used to develop the following correspondence between the static and dynamic lifetime [60]:

$$\tau_{dynamic} = \frac{\tau_{dcstress}}{duty\ cycle}. \tag{5.3}$$

A direct and elegant procedure to quantify the number of generated interface traps is commonly known as the charge pumping method [64]. A brief introduction to the charge pumping method and experimental results from stressed NMOS devices are presented in the next section.

5.3 Charge Pumping Experiment

Charge pumping method is a versatile technique to quantify the number of generated interface traps in a stressed MOS device. It is also possible to determine the spatial nature of the traps and their position in the bandgap [64].

In this technique, the gate of a MOS transistor is repetitively pulsed from an accumulation to a high inversion level. The source and drain electrodes are tied together to the ground and the body of the transistor is also connected to the ground through a picoammeter to measure the charge pumping current. The circuit schematic of such an experiment is shown in Fig. 5-8.

When the device goes into inversion, the minority carriers (in this case electrons) are provided by the source and the drain to form the channel. Some of these carriers are captured by the interface traps (states). As the gate pulse switched back to accumulation, the electrons in the inverted channel disappears. However, the captured electrons recombine with the majority carriers (holes) supplied by the body contact and a net charge pumping current is observed. The diodes between the source-drain n^+ regions and the

transistor body are reverse biased and do not contribute to the charge pumping current (I_{CP}). Thus I_{CP} is directly proportional to the number of captured minority carriers or the number of trap sites at the gate oxide interface.

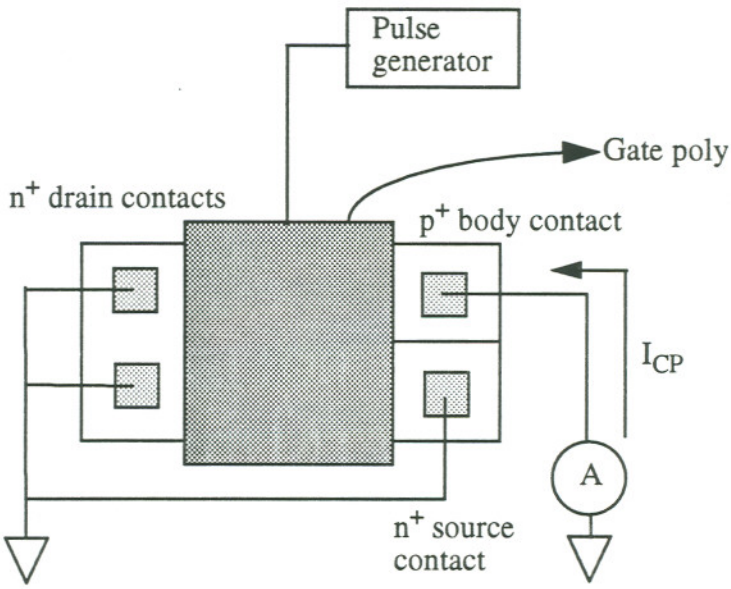

Figure 5-8: Set-up for the Charge-Pumping Experiment

A detailed analysis of the charge pumping phenomenon can be found in reference 64. For the sake of simplicity, we will briefly describe only the salient features of this experiment. In a typical procedure, the base level of the gate pulse is sweeped from a low accumulation to a high inversion level. The amplitude, frequency and the rise and fall times are kept constant. Figure 5-9 illustrates three distinct regions characterized by the presence or the absence of the charge pumping current as the pulse base voltage is sweeped.

In region I, the fast interface states are permanently filled with holes and channel formation never takes place. As a result, no charge pumping current is detected in this

regime. Similarly, in region III, the holes cannot reach the interface due to the inverted surface and no charge pumping current is observed. Only in region II, when the pulse base voltage is less than the flat band voltage and top level of the pulse is above the threshold voltage of the device, the majority carriers are able to recombine with the trapped minority carriers and a charge pumping current is observed.

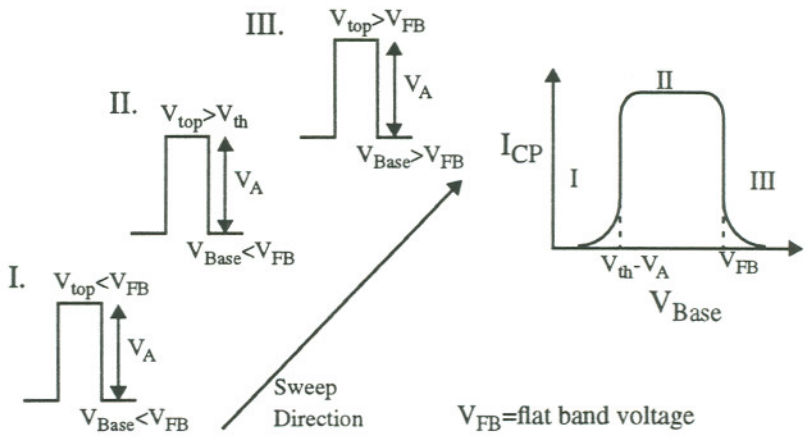

Figure 5-9: Charge pumping current as a function of the pulse base voltage

The maximum charge pumping current $I_{CP}(max)$ is related to the number of interface states by the following equation [64]:

$$I_{CP}(max) = D_{it} \cdot A_G \cdot f \cdot q \cdot (q \cdot \Delta\varphi_s) \tag{5.4}$$

where D_{it} is the average interface trap density (per unit area and energy), A_G is the area of the gate, f is the frequency of the gate pulse, and $\Delta\varphi_s$ is the energy range scanned within the bandgap.

In our experiment, the pulse amplitude and frequency was 6V and 500kHz, respec-

tively. The charge pumping currents, before and after stress (2000 minutes), have been plotted in Fig. 5-10.

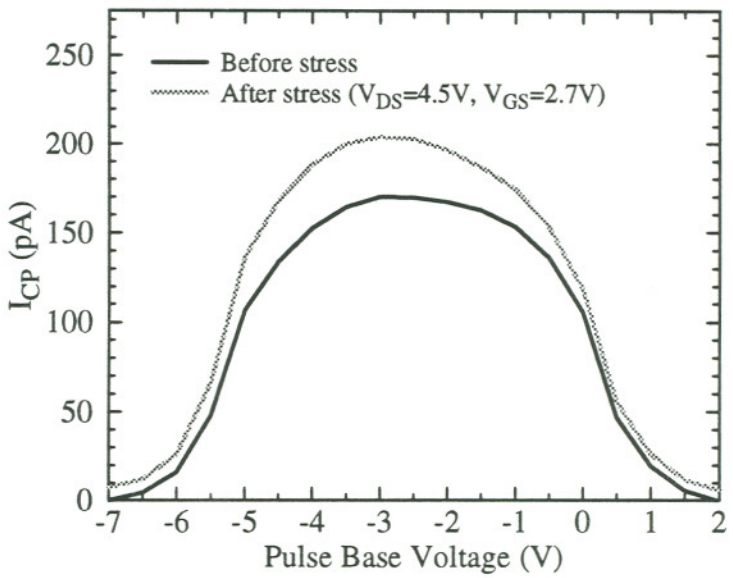

Figure 5-10: Charge-Pumping Current

The difference in the charge pumping current or ΔI_{CP} is proportional to the generated interface trap density during the hot electron stress. Therefore, the following equation can be written:

$$\Delta D_{it} = \frac{\Delta I_{CP}}{A_G \cdot f \cdot q \cdot (q \cdot \Delta\varphi_s)}, \tag{5.5}$$

where ΔD_{it} is the generated interface trap density. From our experimental data, the generated interface trap density is 3.4×10^9 cm^{-2} eV^{-1}. The extracted trap density is a relatively small number since the drain voltage used during the stress period was not high enough to cause a significant number of trap generation at the oxide interface.

5.4 Breakdown Voltage Improvement of PD SOI Devices

One of the principal obstacles in using partially depleted SOI devices for VLSI applications is the parasitic bipolar effect. The accumulation of holes not only causes the "kink" effect in I_D-V_{DS} characteristic, this effect is also responsible for low breakdown voltage of PD SOI NMOS transistors. The perceived use of thin film SOI transistors in the ULSI technology will be in the low power applications and the power supply voltage will be appropriately scaled to 2V or lower [34]. It is still desirable to obtain higher breakdown voltages for reliability considerations and burn-in experiments. We have seen in the earlier part of this chapter that the NMOS transistors could not be stressed at high drain voltages in order to generate data for the creation of a comprehensive hot carrier model in a short cycle time.

In this section, we propose the use of Silicon-Germanium (SiGe) in the source-drain regions of SOI NMOS transistors. This type of bandgap engineering will reduce the gain of the inherent parasitic bipolar (npn) transistor and thus improve the breakdown characteristics of the SOI NMOS devices. Very recently similar ideas have been proposed by researchers at Toshiba and Samsung [65-66].

It is well known that the current gain β of a bipolar transistor is related to the bandgap reduction ΔE_g between the base and the emitter by the following expression [40]:

$$\beta \equiv \frac{N_E D_{nB} W_E}{N_B D_{hE} W_B} \; e^{-\frac{\Delta E_g}{kT}} \tag{5.6}$$

where D_{nB} in the electron diffusion coefficient in the base, D_{hE} is the hole diffusion coefficient in the emitter, and W_E and W_B refers to the emitter and the base width, respectively. In the case of a PD SOI NMOS transistor, the body and the source can be considered as the base and the emitter. In order to reduce the parasitic bipolar gain,

several parameters such as the body and the source doping can be changed at the price of degrading the MOS performance. One of the other options is to reduce the impact ionization rate by decreasing the LDD doping. However, this option also provides diminishing return as the drive current of the transistor is a strong function of the source-drain series resistance.

The use of SiGe source-drain regions, however, may offer a solution without any such penalty. The conduction band off-set between Si and SiGe is negligible. Thus the current conduction in the channel is not affected. However, the valence band off-set makes it easier for the holes to surmount the body to source potential barrier. This "barrier lowering" effect is demonstrated in Fig. 5-11. As a result of this event, an improvement in the breakdown voltage is observed.

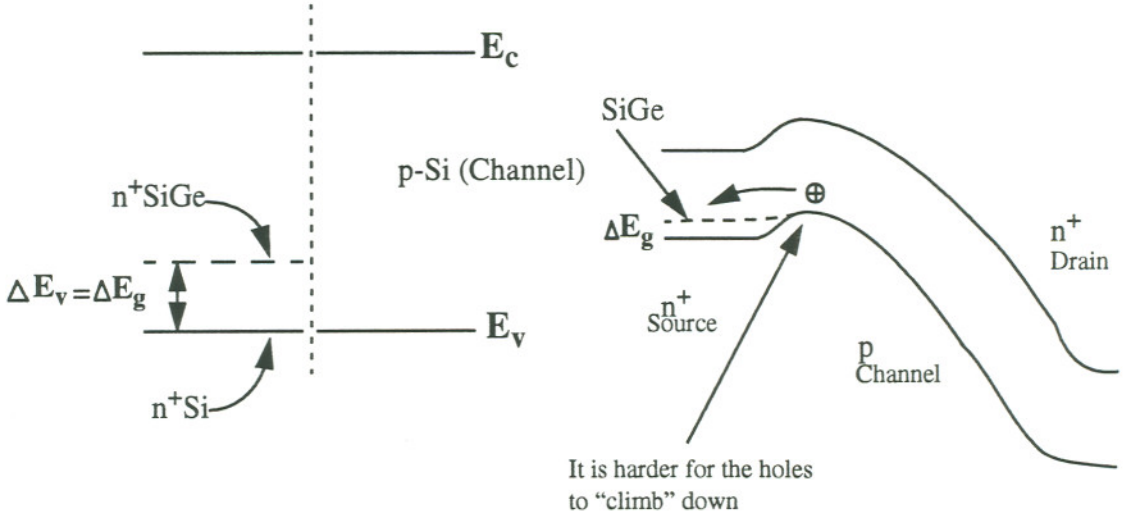

Figure 5-11: Band-diagram in presence of a positive drain bias

Sim *et al.* have proposed chemical vapor deposited growth of SiGe in the source-drain regions [66]. However, ion implantation is preferable as it reduces the process

complexity and can be incorporated in a standard CMOS process without any increase in the number of mask steps. A Ge implant self-aligned to the gate, before the spacer deposition, may be used to define the SiGe regions. Thus the same mask steps used for the LDD formation can be used to create Ge-implanted source-drain regions. Researchers have already demonstrated the formation of high quality Si-Ge layers by the use of ion implantation followed by a rapid thermal anneal [67]

The structure proposed in this work may offer an advantage that has been overlooked by other researchers. Ge has a higher workfunction than Si. If the poly-gate is implanted with Ge in the same process step, the flatband voltage of the MOS structure will increase as a result of the higher workfunction of SiGe poly-gate structure. This will allow the use of lower substrate doping for a given threshold voltage and add more flexibility to the design of sub-micron PD SOI devices.

Atlas, a two dimensional device simulator, was used to perform the 2D numerical calculations to demonstrate the feasibility of this concept. The bandgap model used for the simulation can be expressed as:

$$E_g(Si_{1-x}Ge_x)=E_g(Si)-(0.74)x \tag{5.7}$$

where x is the Ge content in the $Si_{1-x}Ge_x$ alloy. For the 2D simulations, x=0.2 was assumed and the valence band off-set was calculated to be 0.148eV. Identical SOI NMOS structures, with 0.5 μm channel lengths, were simulated. The results of the simulations (V_{GS}= 0V) are shown in Fig. 5-12. The impressive improvement in the breakdown voltage performance can be explained by looking at the following equations [37]:

$$I_B = (M-1)\,(I_{ch}+\beta I_B) = \frac{M-1}{1-\beta\,(M-1)} I_{ch}, \tag{5.8}$$

$$\text{and } I_D = M\,(I_{ch}+\beta I_B) = \frac{M}{1-\beta\,(M-1)} I_{ch}\ . \tag{5.9}$$

where I_{ch} is channel current, M is the multiplication factor, and I_B is the base current of the lateral bipolar transistor. The term βI_B refers to the collector current. The channel current is amplified by impact ionization and also by the bipolar action. When the value of $\beta(M-1)$ approaches one, the breakdown is observed. Since $\beta \propto e^{-\frac{\Delta E_g}{kT}}$, a ΔE_g (x=0.2) of ~0.148 eV corresponds to 1/300 reduction in the collector current and the breakdown voltage of the structure is significantly improved.

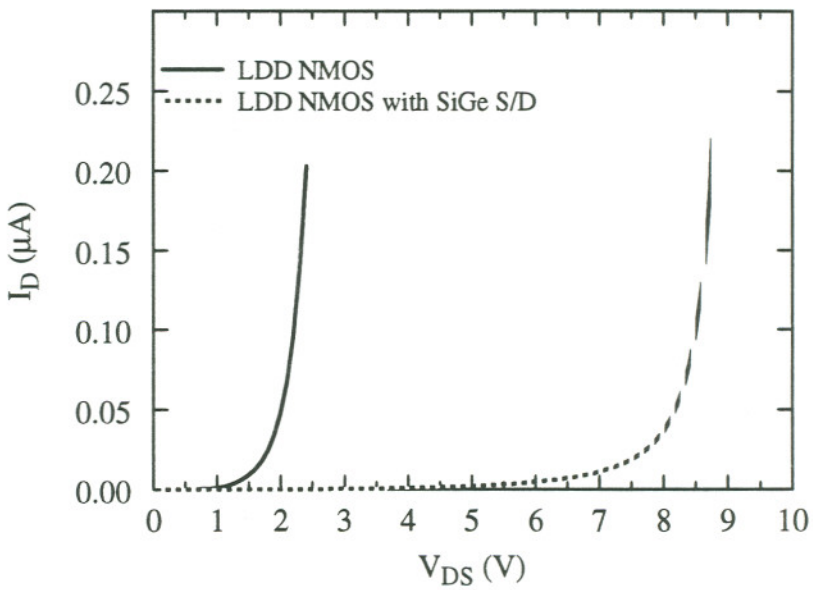

Figure 5-12: Breakdown voltage improvement with the use of SiGe source-drain

NMOS SOI transistors with SiGe source-drain regions can overcome the low breakdown voltage effect seen in the TFSOI technology. The process flow described in this work does not require any additional mask step. The high current implanters developed for SIMOX manufacturing may be used for high dose Ge implantation.

Chapter 6
Conclusions
and
Suggestions for Future Research

In this chapter, the results and discussions mentioned in the first five chapters of this thesis will be summarized. The important aspects of the experimental data regarding the status of present day SOI substrates, short drift region high voltage LDMOS design, and reliability issues with partially depleted MOS devices are reviewed. A photograph of an operational high resolution AMEL array with a 12 μm pixel pitch has also been included.

6.1 SOI Substrates for ULSI Technologies

It has been demonstrated that the commercially available SOI wafers have high front and back channel mobility values and low interface state densities. Reasonably high minority carrier and generation lifetimes were also extracted. These material parameters, extracted from fabricated devices, are important for ULSI device fabrication. For example, high lifetime values indicate that high performance bipolar or BiCMOS circuits or DRAM memory chips can be fabricated on commercially available wafers.

The generation lifetime, often used as a figure of merit for SOI substrates, was found to be 80 μs for SIMOX substrates, which ranks favorably when compared to the best reported in the literature (130μs, Ref. 43). The high values for both the front- and

back-channel mobility also indicate a mature SOI wafer manufacturing technology.

6.2 Short Drift Region High Voltage LDMOS Devices

Short drift region SOI LDMOS transistors can be incorporated with standard CMOS logic circuits for "smart power" IC applications. The use of SOI substrates allows easy isolation and higher packing density. In this thesis, a comprehensive design guideline for such devices has been presented. Medici, a two-dimensional device simulator, was used for the optimization of the device parameters. Potential contour and electric field profiles were plotted to obtain further insight into the breakdown mechanism of SOI LDMOS structures. The design rules were verified by the characterization of fabricated test structures. Experimental results from a short drift region LDMOS device with near ideal breakdown voltage performance has also been demonstrated.

6.3 Functional AMEL Arrays with 12 micron Pixel Pitch

AMEL displays with pixel dimensions of 12x12 μm^2 have been fabricated, reduced from the current design with the dimensions of 24x24 μm^2. These pixels have short drift region LDMOS transistors described in this thesis. A photograph of a functional pixel array is shown in Fig. 6-1.

This pixel scaling provides a basis for at least two fold increase in resolution over previous AMEL designs. The primary incentive for designing a scaled pixel is to develop a 2560x2048 HMD with a higher information content. The four fold increase in pixel density and the number of die per wafer for a given display format also allows significant cost reduction. The 2 μm drift region LDMOS structure, described in this thesis, will eventually allow the pixel pitch to be scaled down to 6 μm. This development is impor-

tant for economic considerations of color AMEL displays as four regular pixels are needed for a functional color pixel.

The success of the scaled design depended on the ability to fabricate a high voltage transistor in a 12x12 μm^2 pixel. The isolation of the low and the high voltage component of the pixel circuit is also of importance. The dielectric isolation provided by the use of SOI technology was essential for a successful design.

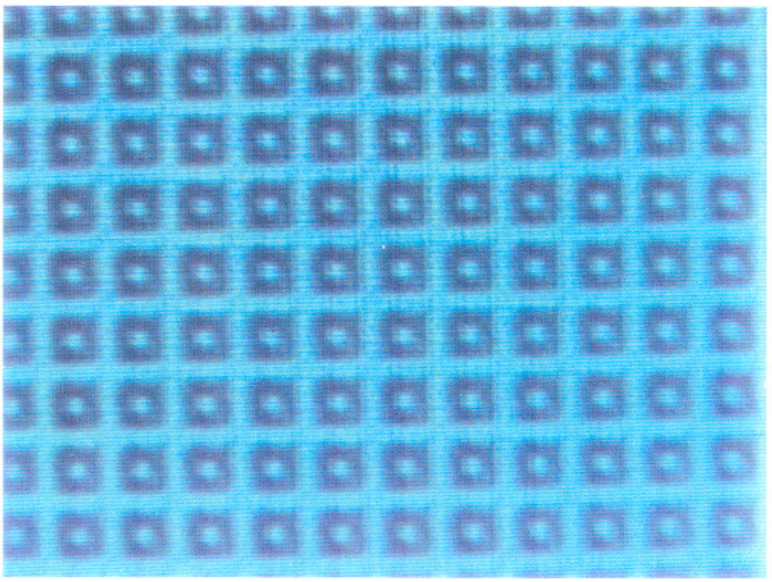

Figure 6-1: A functional AMEL pixel Array with 12 μm pitch

(Bright pixel in dark box)

This thesis provides important insights into the specific design of the LDMOS structures used in AMEL pixel arrays. Issues regarding the inter-level dielectric (ILD) thickness between the device and the EL contact have been investigated and successfully applied to the scaled pixel design.

6.4 Reliability and High Temperature Characteristics of SOI Devices

Hot electron effects in short channel PD SOI devices have been studied. Low breakdown voltage of the SOI NMOS transistors has been found to be an obstacle for generation of a comprehensive hot carrier model in a short cycle time. The use of SiGe in the source-drain regions to lower the gain of the parasitic bipolar may remedy the situation. The idea, independently developed by this author, has already been experimentally verified by other researchers.

Excellent high temperature behavior of SOI LDMOS transistors at elevated temperatures has been evidenced. Significant reduction in the junction area in SOI structures as compared to their bulk counterparts is the main reason behind the low I_{off}/I_{on} values at elevated temperatures.

6.5 Suggestions for Future Work

A comprehensive study of different types of defect densities in commercial SOI substrates and their effects on device and circuit performance is suggested. Statistical distribution of defect densities in commercial SOI wafer lots must also be studied. Although tremendous amount of device research and technology development is under way, major IC manufacturers are yet to announce any product development on SOI substrates. Such an investigation will generate important data regarding the feasibility of the use of SOI substrates for ULSI applications.

Although near ideal breakdown voltage performance was achieved in a fabricated LDMOS transistor, the on-resistance value for the device can be further improved by the use of a thinner buried oxide (which will allow higher drift doping), a thicker SOI film, and a sub-micron channel. LOCOS related defects has found to be causing significant leakage if sufficient distance (known as poly-to-active area overlap) between the channel and the field oxide edge is not present. However, poly-to-active area overlap does not

enhance the breakdown voltage performance but significantly increases the on-resistance in a short drift region device. Improvements in the LOCOS growth process is necessary for optimization of the on-resistance performance.

The number of die per wafer can be increased by a factor of sixteen if the pixel dimensions are scaled to 6x6 μm^2 from the current dimensions of 24x24 μm^2. Therefore, efforts should be made to scale the pixel pitch of the AMEL displays even further. Such aggressive scaling may be necessary for color AMEL HMDs, which will compete with similar low cost liquid crystal displays.

The advantage of an integrated SiGe-SOI technology should be pursued. The use of SiGe in SOI NMOS devices will improve the breakdown voltage performance. Similarly, Ge implanted into PMOS channels may improve the mobility and the current drive capability of p-channel devices. This will cause further reduction in die size as PMOS devices are currently sized 2-3 times larger than an NMOS device with similar current drive capabilities. The reduction in capacitance due to the use of SOI substrates and the improvement in the current driving capability of the SiGe PMOS device will allow a significant reduction in power supply voltage without compromising the speed of the circuit. An integrated SiGe-SOI technology may turn out to be the ideal candidate for the low power technology of the future.

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