N-CHANNEL BETA-SiC MOSFET

HER-SONG CHEN

B.S., National Taiwan Normal University, 1985

A thesis submitted to the faculty
of the Oregon Graduate Institute of Science & Technology
in partial fulfillment of the
requirements for the degree
Doctor of Philosophy
in
Electrical Engineering

April, 1993

This dissertation "n-Channel Beta-SiC MOSFET" by Her-Song Chen has been examined and approved by the following Examination Committee:

James D. Parsons
Associate Professor
Thesis Advisor

Thomas W. Sigmon
Professor

V.S. Rao Gudimetla
Assistant Professor

Leopoldo D. Yau
Director of Innovative Technology Modules, Intel Fellow
Intel Corporation

To My Parents

ACKNOWLEDGMENTS

There are so many people who helped me get through this part of my life. I would like to express my appreciation of my advisor, Prof. James D. Parsons, who had the vision to pioneer the work in beta-SiC epi-growth on titanium carbide, and who trained me to become a better scientist. Dr. Leopoldo D. Yau of Intel deserves my thanks because he spent a lot of time reading my thesis, and gave me the most valuable suggestions. I would also like to acknowledge the other members of my reading committee, Profs. Thomas W. Sigmon and V.S. Rao Gudimetla, for taking their time and providing me helpful comments.

I want to say thanks to Karen Oatis, Ajay Chaddha, Jin Wu, Gary Giust and SukRyong Hahn of the Parsons group for their help and discussion throughout this work. Also thanks to Jerry Boehme who gave the extensive help.

Most importantly, I also wish to express my great appreciation to my family for their enormous support and encouragement throughout these years. I owe them very much; without their support the task would have been next to impossible.

ABSTRACT

n-Channel Beta-SiC MOSFET

Her-Song Chen, Ph.D.

Supervising Professor: James D. Parsons

Beta silicon carbide (beta-SiC) is a promising semiconductor material. Its bandgap (2.2 eV), thermal conductivity (4.9 W/cm.°K), saturated drift velocity (2.5×10^7 m/sec) and many other characteristics are advantages for high temperature, high power and high frequency applications. Furthermore, its resistance to diffusion and its high breakdown electric field (2×10^6 V/m) present the possibility of high device densities. These advantages have long been recognized, but have not yet been utilized because of difficulties in single crystal beta-SiC synthesis.

In this thesis, the feasibility of developing n-channel inversion mode beta-SiC MOSFETs was studied and demonstrated. Epitaxial growth, materials processing and device processing procedures were developed, and employed to fabricate MOS capacitors and MOSFETs. The inversion characteristics of beta-SiC MOS capacitors were observed in dark for the first time. An in-situ doping technique was successfully incorporated into the fabrication of prototype recessed source/drain MOSFETs; we thus demonstrate that TiC_x is a suitable substrate for beta-SiC MOSFET structures.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION FOR WORK

Silicon (Si) has been the most important semiconductor material for the past 30 years. It has been fabricated into many kinds of devices, such as diodes, JFETs, MESFETs, MOSFETs and bipolar transistors. The metal oxide semiconductor field effect transistor (MOSFET) is one of the most useful devices for digital applications. The fundamental properties of Si are such that its performance limits for MOSFET applications are being approached.

In a MOS circuit, the delay of a single gate is dominated by the output rise and fall time. The rise and fall time is inversely proportional to the drift mobility and directly proportional to the dielectric constant (ε_{sem}) of a semiconductor[1]. High thermal conductivity is also important because MOSFET device generates heat that can cause failure when it operates at very high frequencies. A comparison of the mobility, dielectric constant and thermal conductivity of Si (silicon), GaAs (gallium arsenide), 6H alpha-SiC (6H alpha silicon carbide) and beta-SiC (beta silicon carbide) suggests that beta-SiC may be the optimum choice for the development of high frequency and high temperature MOSFETs (detailed in section 2.1).

The purpose of this thesis was to demonstrate the feasibility of beta-SiC MOSFET technology, and, in particular, to show inversion in beta-SiC MOS capacitors.

1.2 ORGANIZATION

This thesis contains six chapters.

In chapter 1, the motivation of this work and the organization of this thesis are presented.

Chapter 2 is an overview of the important properties of beta-SiC for electronic applications, especially for MOSFETs. It also gives a discussion of the synthesis approach for beta-SiC, including the apparatus.

Chapter 3 describes the processing techniques and their characterization results for the beta-SiC MOS capacitors and MOSFETs. Beta-SiC epi-growth procedure, reactive ion etching, oxidation and its relative calculation and modeling, TiC_X epi-growth and etching experiments, and contact metal deposition are discussed in this chapter.

Chapter 4 gives a detailed description of the structure and electrical characterization of beta-SiC MOS capacitors. Included in this chapter are the processing steps for beta-SiC MOS capacitors and related physical parameters obtained from these capacitors, studies of high frequency capacitance-voltage measurements, and modeling of beta-SiC MOS capacitors.

Chapter 5 discusses the structure and the electrical characterization of the beta-SiC MOSFETs. The processing steps of beta-SiC MOSFETs are also

discussed.

Chapter 6 contains a discussion of this work's contributions, and suggestions for future experiments.

CHAPTER 2

BETA-SIC PROPERTIES AND SYNTHESIS APPROACH

The important properties of beta-SiC for device applications and the synthesis approach employed are described in this chapter. Problems of titanium carbide (TiC_x) as a substrate for beta-SiC epi-growth are discussed in the end.

2.1 PROPERTIES OF BETA-SIC

The importance of SiC is well established. Each year, tons of SiC are produced in the world. This product is used for steel deoxidization, wear resistant parts, nuclear fuel cladding, protective coatings, heating elements, electrical resistors and varistors.

Silicon carbide has more than 170 polytypes and four crystal structures[40] (listed in table 2.1). Among these, beta-SiC is the preferable structure for device applications because of its attractive properties (table 2.2). At present, 6H alpha-SiC is more widely used than beta-SiC because its synthesis process is more mature.

Table 2.1 Crystal structures of SiC and their symbols.

Crystal	Symbol	Crystal Structure
Beta-SiC (ß-SiC)	3C-SiC	Cubic
Alpha-SiC (α-SiC) (170 polytypes)	*n*Hα-SiC	Hexagonal
	*n*Rα-SiC	Rhombohedral (Trigonal)
	*n*Tα-SiC	Tetragonal

note: *n* denotes a positive integer. Symbols with different *n* represent polytypes of the same SiC crystal structure.

Properties considered the most important that enhances the high frequency semiconductor applications are: 1) low dielectric constant, 2) high saturated drift velocity and 3) high carrier mobility. The dielectric constant is important because it is directly proportional to the amount of charge needed to set up electric-potential and, therefore, to the parasitic capacitance, which is directly proportional to the dielectric constant and is the fundamental speed limitation of a MOS device. The saturated drift velocity is important because it indicates the maximum speed at which a carrier can travel in a semiconductor. The mobility is important because it is a measurement of the ease with which charge can be made to flow. Therefore, the small dielectric constant (resulting in smaller parasitic capacitance), the high saturated drift velocity and the mobility (resulting in fast moving carriers) of beta-SiC suggest that its device is suitable for high frequency operation.

A semiconductor material suitable for high temperature applications should have a wide bandgap, a high thermal conductivity and form a good

diffusion barrier. A wide bandgap is important because they are less susceptible to thermal excitation of electrons by internal or external heating. Materials with high thermal conductivity are more suitable for high temperature operations because their devices are generally capable of dissipating more heat, and operate at lower temperatures. The diffusion barrier property is important because the movement of dopant impurities at high temperature results in the change of device structures and, therefore, device characteristics. Diffusion studies[23] on beta-SiC indicate that dopant diffusion in beta-SiC is extremely low even at temperatures approaching its dissociation temperature (partially because its high material density causes the dopant atoms less likely to move in the crystal). Therefore, the high thermal conductivity, the wide bandgap and the good diffusion barrier property of beta-SiC makes it attractive for high temperature operation. Moreover, the wide bandage property of beta-SiC suggests that its devices are able to handle higher current densities and operate at higher power level.

An insulator is an essential part of a MOS device. Therefore, a semiconductor suitable for MOSFET applications must have a suitable insulator. Gallium arsenide MOSFETs have yet to be developed because a stable insulator of GaAs compounds is not available. In contrast, the thermal oxide of beta-SiC has been proven to be quite similar to silicon dioxide, using the same oxidation process as that used for silicon[26,27,28].

Now that we discussed some of the most important properties of beta-SiC. The decision of using beta-SiC for high frequency, high power and high

temperature MOSFET applications is clear. The elimination of GaAs from consideration was discussed in the previous paragraph. Beta-SiC is more suitable than 6H alpha-SiC because beta-SiC has higher electron and hole mobilities although both of them have the potential to operate at high temperatures. Si is not desirable because the inter-diffusion of dopants in Si limits its devices operating at temperatures greater 200 °C.

Beta silicon-carbide properties discussed above indicate that it is suitable for all MOSFET applications. Other properties of beta-SiC, the difficulties of ion implantation and diffusion, suggest that the fabrication procedures of its MOSFET will be different from that of Si and that new processing techniques may be needed to fabricate beta-SiC MOSFETs. The diffusion process that is used in Si is not available for beta-SiC because beta-SiC is an excellent diffusion barrier.

The difficulty of ion implantation arises from the polytypes and from the high p-type dopant activation energy of beta-SiC. Semiconductor devices that are suitable for circuit applications must be of a single crystal and of a single polytype because grain boundaries and polytypism lead to variations in transport properties from device to device. Ion implantation has proven to be very successful for materials that do not exhibit polytypes[29]. However, ion implanted beta-SiC films form polytypes during the annealing process because of the high annealing temperatures (> 1600 °C) required to activate p-type dopants[30,31,32,33,34]. Although laser annealing is proposed to activate the Al or Ga dopants in beta-SiC[35], more research is needed in order to utilize this

technology.

The one crucial barrier to utilizing beta-SiC for MOSFET applications has been the unavailability of good quality single crystals. Due to the fact that beta-SiC does not melt but dissociates at 2830 °C under an Ar pressure of 35 atmospheres[36], commonly used methods of growing and purifying bulk single crystals, such as melt growth and zone refining, cannot be used for beta-SiC. Other methods of beta-SiC growth, such as sublimation[38] and melt growth[39], are plagued by problems of small crystal dimensions and/or polytypism. The other alternative to bulk beta-SiC crystal growth is by thin film growth, which is described in the next section.

Table 2.2 Comparison of important properties of ß-SiC, Si, GaAs and 6Hα-SiC for electronic applications.

Properties (300K)	Units	ß-SiC	Si	GaAs	6Hα-SiC	Reference
Bandgap energy (E_g)	eV	2.2	1.12	1.43	3.0	[1-4]
Hall Mobility						
Electrons	cm^2/V-sec	1000-4670	1500	9000	400-607	[14,16,21,22]
Holes	cm^2/V-sec	650	450	450	50	[14,23,24]
Dielectric Constant		9.7	11.9	12.8	>9.7	[29]
Saturated Drift Velocity	cm/sec	$2.5x10^7$	$1x10^7$	$2x10^7$	$2x10^7$	[14,20,25,26]
Breakdown Electric Field	V/cm	$2x10^6$	$3x10^5$	$4x10^5$	$2x10^6$	[14,27,30,31]
Minority Carrier Lifetime	millisec	?	2500	0.02	30	[28]
Thermal Conductivity	W/cm·°K	4.9	1.5	0.5	4.9	[32]
Dopant activation energy (E_a)						
n-type	meV	20	39	6	63	[14-17]
p-type	meV	160	45	26	210	[14,15,18,19]
Ionization Coefficient						
α_n	cm^{-1}	$7x10^5$	$4x10^5$	$2x10^5$	$7x10^5$	
α_n	cm^{-1}	$7x10^5$	$2x10^5$	$2x10^5$	$7x10^5$	
Density	g/cm^{-3}	3.21	2.32	5.65	2.32	

2.2 BETA-SIC SYNTHESIS APPROACH

Thin film growth of epitaxial SiC has been pursued by various methods, such as liquid phase growth[41], recrystallization[42] and vapor-phase epitaxy[43,44,45,46,47,48]. Vapor phase epitaxy (VPE) is the only technique which has been successfully employed to grow unpolytyped, single crystal beta-SiC. In this section the substrate selection for beta-SiC vapor-phase epitaxy and a short description of the growth apparatus are presented. The growth and characterization results are presented in chapter 3, where the necessary processing steps for beta-SiC MOS capacitors and MOSFETs are discussed.

2.2.1 Substrate selection

Choice of a substrate for epitaxial growth of beta-SiC is constrained by the following requirements: 1) the lattice parameter mismatch between the substrate and beta-SiC should be as small as possible; 2) the substrate and beta-SiC should have the same crystal structure 3) the expansion coefficient of the substrate should be greater than or equal to that of beta-SiC; 4) the substrate must be chemically stable at temperatures required for epitaxial growth of beta-SiC; 5) it must be possible to synthesize large crystals of the substrates; and 6) the substrate constituents must be electrically neutral in beta-SiC.

Lattice parameter matching of substrate and epi-layer is important because epitaxial growth is a process building a new crystal lattice through the influence of substrate atomic and molecular forces. Failure to match lattice parameters

results in independent nucleation growth of thin films, which causes elastic strains and other defects.

The substrate should have the same crystal structure as beta-SiC. A different crystal structure between layers and substrates permits epi-growth only on certain orientations of the substrate.

The substrate expansion coefficient should equal or exceed that of the epi-layer for two important reasons. First, the epi-layer will be compressionally loaded at room temperature, which reduces the chances of it forming micocracks and pinholes. Second, the surface morphology of thick (>1 um) epi-layers tends to be rough when the epi-layers are tensionally loaded.

Chemical stability of the substrate at epitaxial growth temperatures dictates that the substrate does not decompose or undergo phase transformations at or below the epitaxial growth temperature, and that it exhibits minimal surface reactivity with the chemical environment to which it is exposed to just prior to the start of epitaxial growth.

Vapor phase epitaxial growth of beta-SiC is presently persuaded on single crystal Si[47,49], 6H alpha-SiC[50] and TiC_x[46] substrates. The properties of these substrate materials for beta-SiC epitaxial growth are presented in table 2.3.

Silicon is presently the most widely used substrate for beta-SiC epitaxial growth. However, beta-SiC films grown on Si wafers contain a high density of misfit dislocations, stacking faults and antiphase domain boundaries (APDs); furthermore, elastic strains in the substrate/epi-layer interface region extend approximately 3 um into the beta-SiC film[60,61,62]. Epitaxial growth of beta-

SiC on disoriented Si substrates eliminates APDs; however, stacking faults, dislocations, and elastic strains still persist in the film regardless of the degree or direction of substrate disorientation. These defects are caused by the difference in the lattice parameters (~20%) and thermal expansion coefficients (~8% at 473 °K) between beta-SiC and Si.

Table 2.3 Important properties of beta-SiC, TiC_x, alpha-SiC and SiC for epitaxial growth.

property\material	beta-SiC	TiC_x	6H alpha-SiC	Si[52]
Crystal structure	Zincblend (cubic)[53]	Rocksalt (cubic)	hexagonal[53]	Diamond (cubic)
Lattice parameter(Å)	4.359[54]	4.328[55]	a= 3.081 c= 15.12[54]	5.431
Thermal expansion coefficient at 1000 °C (10^{-6}/°C)	5.8[56]	~7	5.12[57]	2.6
Melting temperature (°C)	2830±40 decomposes at 35ATM[58]	3120[55]	2830±40 decomposes at 35ATM[58]	1415
Thermal conductivity (W/cm.°K) at 300 K	4.9[59]	>2	4.9[59]	1.5

Beta-SiC epitaxially grown on 6H alpha-SiC substrates has a high density of double positioning boundaries[62] and stacking faults.[62] These defects are caused by simultaneous nucleation of the film in different sites rotated from each other by 60 degrees. Furthermore, beta-SiC can only grow on certain orientations

of alpha-SiC because the different crystal structures of beta-SiC and alpha-SiC.

The substrate material with a lattice parameter most closely matching that of beta-SiC and meeting all other constraints of beta-SiC epi-growth is TiC_x. The lattice parameter mismatch of TiC_x to that of beta-SiC is less than 0.7% (table 2.3). The higher thermal expansion coefficient of TiC_x causes preferred compressional loading of beta-SiC epilayers. There is no restriction imposed by TiC_x substrates on the growth orientation of beta-SiC because both have cubic crystal structures. The last of most important constraint met by TiC_x is that Ti and C are electrically inactive in beta-SiC. At the high temperatures required for epitaxial growth of beta-SiC (1200 °C to 1600 °C), some interdiffusion can be expected to occur, but without deleterious electrical effects. The advantages of using TiC_x for single crystal beta-SiC epi-growth are summarized in table 2.4.

Table 2.4 Advantages of using TiC for beta-SiC epi-growth.

TiC_x PROPERTIES	RESULTS
Cubic crystal structure	Beta-SiC epitaxial growth on all TiC_x orientations
Lattice parameter mismatch ~0.7%	Small elastic strains in the epi-layer/TiC interface
Small Thermal expansion coefficient mismatch to beta-SiC and beta-SiC epi-layer compressionally loaded	Beta-SiC epi-layer less likely to crack
Congruently melting	Large area single crystal TiC_x growth
Thermal conductivity > 2 W/cm°K at 300 °K	Suitable for high temperature application
High melting temperature ~ 3200 °C	No temperature limitation imposed on beta-SiC processing
Low work function (~3eV)	Ohmic contact to n-type beta-SiC

2.2.2 Beta-SiC epi-growth apparatus

1,2-disilylethane ($C_2H_{10}Si_2$) organometallic source was used as a single source of Si and C atoms for chemical vapor deposition of single crystal beta-SiC on TiC_x. $C_2H_{10}Si_2$ was selected because it contains an equal number of C and Si atoms and its decomposition characteristics suggest that C and Si can be obtained from it at approximately equal rates. We found that the equal number of C and Si decomposed from the $C_2H_{10}Si_2$ source during the growth makes the growth

condition more controllable and usually yields a better crystal quality. In the case of using C_2H_4 and SiH_4, very precise control of the Si and C atom ratio, which is very difficult for the existing mass flow controller technology, is necessary in order to obtain a good quality epi-layer. Therefore, $C_2H_{10}Si_2$ was used for both MOS capacitors and MOSFETs.

A schematic of the CVD system is shown in figure 2.1. The CVD system consists five major components, 1) reactor tube and heating coils, 2) gas delivery subsystem, 3) flow control subsystem, 4) exhaust subsystem and 5) leak check subsystem.

A specially designed inverted-vertical (IV) reactor tube[51] was used for the beta-SiC growth. The IV reactor assembly, shown in figure 2.2, includes a reactor tube and a reactor cap, both of which are made of fused quartz, a pyrolytic boron nitride (PBN) or fused quartz pedestal, a PBN mask, two PBN heat shields, and a graphite susceptor. RF heating coils surrounding the IV reactor are used to heat the substrate. The pedestal is a cup-shaped cylinder (shown in figure 2.3) and is coaxially supported within the reactor tube. The openings in the side wall, at the top of the pedestal, provide a flow path for by-product gases to reach the reactor exhaust. An enlarged view of the PBN pedestal base, PBN mask, substrate, susceptor and heat shield arrangement is shown in figure 2.4. The purpose of the graphite susceptor is to couple the RF generator coils and substrates. The heat shields are used to reduce heat loss, since the growth temperature of beta-SiC ~ 1290 °C, and without the heat shields, the RF generator would need to deliver more power to keep the substrate at the same temperature.

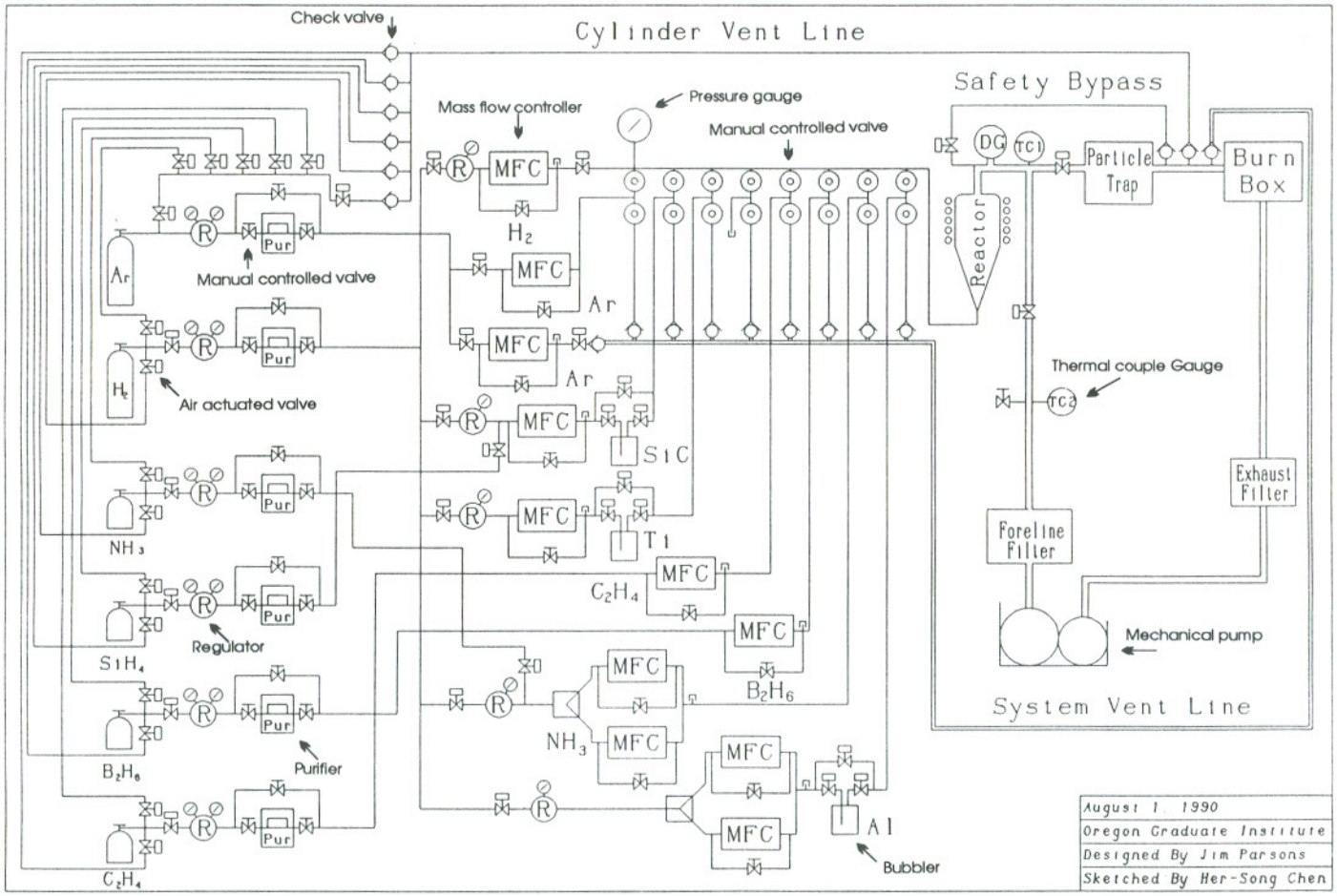


Figure 2.1 Beta-SiC chemical vapor deposition system used for beta-SiC epi-growth.

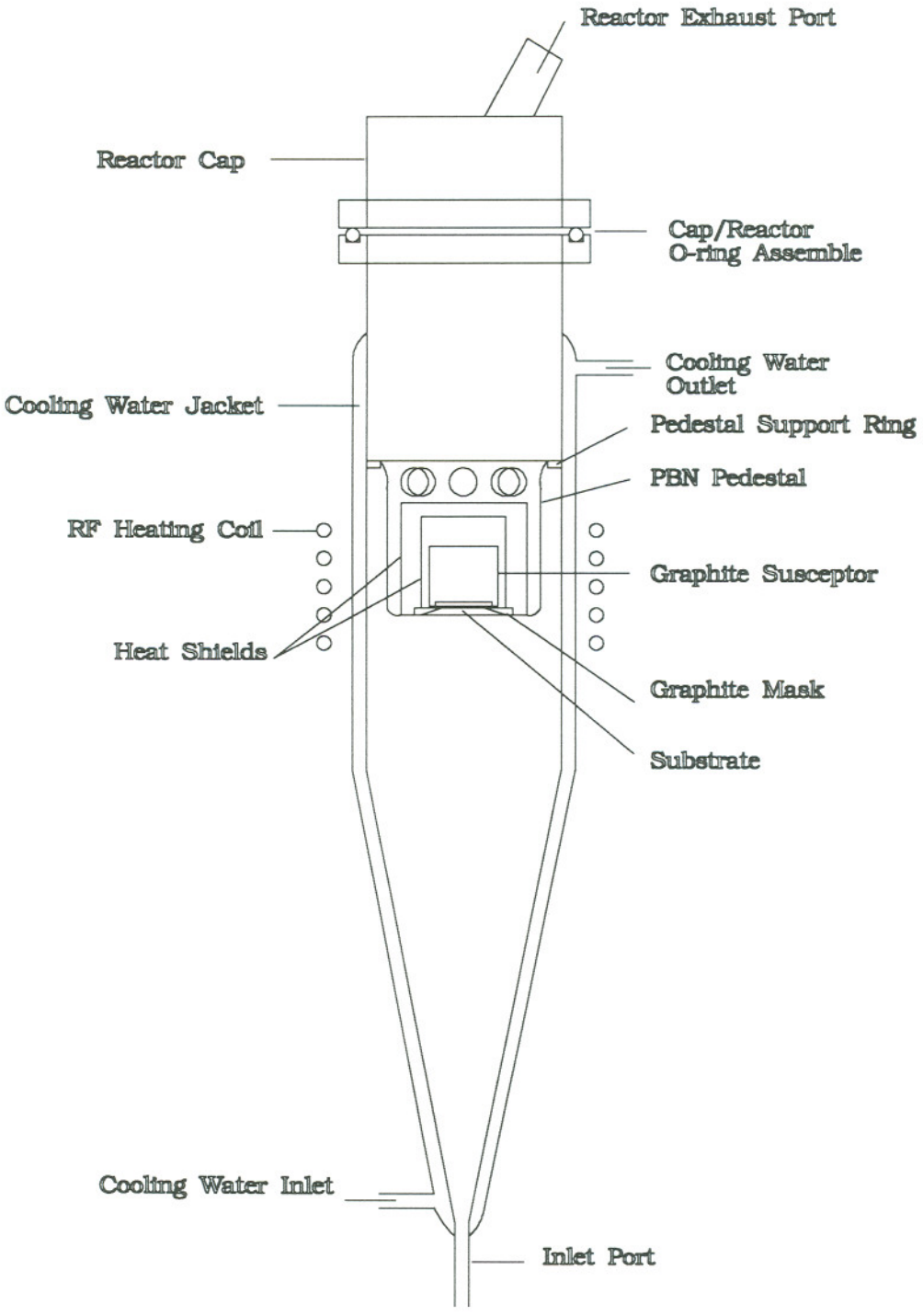


Figure 2.2 Cross-sectional drawing of the I-V reactor assembly, shown to scale.

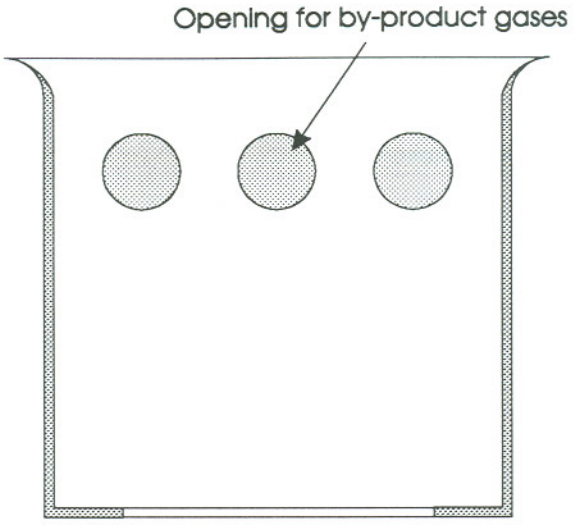


Figure 2.3 Cross-sectional view of PBN pedestal, shown to scale.

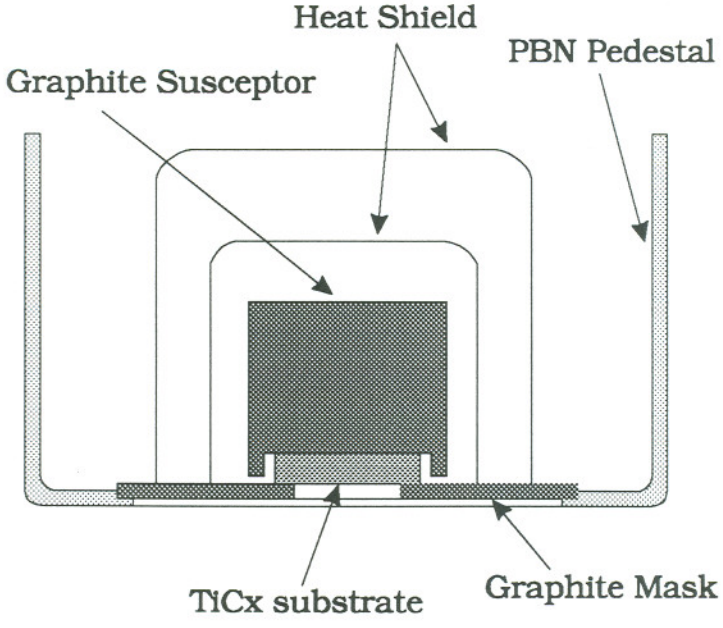


Figure 2.4 Enlarge view of the PBN pedestal base, PBN mask, substrate and susceptor arrangement, not shown to scale.

2.3 PROBLEMS OF TiC_X SUBSTRATES

Low defect TiC substrates are presently very difficult to obtain. The most usual defects in TiC_X substrates are grains and subgrains. A grain boundary is an interface between two different crystallographic orientations. It can be detected by grain boundary etching and subsequent inspection by an optical microscope, figure 2.5, if the change of orientation is on the order of 1°. The orientation change at subgrain boundaries is $\leq 0.1°$; it cannot be easily observed by an optical microscope or high contract SEM. However, subgrains can be easily observed by X-ray rocking curves.

Beta-SiC epilayers reproduce TiC_X substrates' defects, such as grain boundaries and subgrain boundaries. The grain boundaries of the beta-SiC layers can be avoided during the device processing because they can be observed with an optical microscope. In contrast, subgrains cannot be avoided because they cannot be seen under a microscope. Subgrains are not a fundamental property of TiC_X[63]. As with the other semiconductor material, the subgrain density of TiC_X will be reduced or even eliminated as more researchers become involved in improving the quality of TiC_X substrates.

The other problem of TiC_X is that it reacts with oxygen below 1000 °C, figure 2.6 and figure 2.7, to form titanium oxide (TiO_X), which has a very rough surface. This roughness makes subsequent processing procedures very difficult. One possible way to protect TiC_X from oxidation is to coat it with a material which does not react with oxygen. Alternatively, the beta-SiC substrate can be totally decoupled from the TiC_X substrate before the processing.

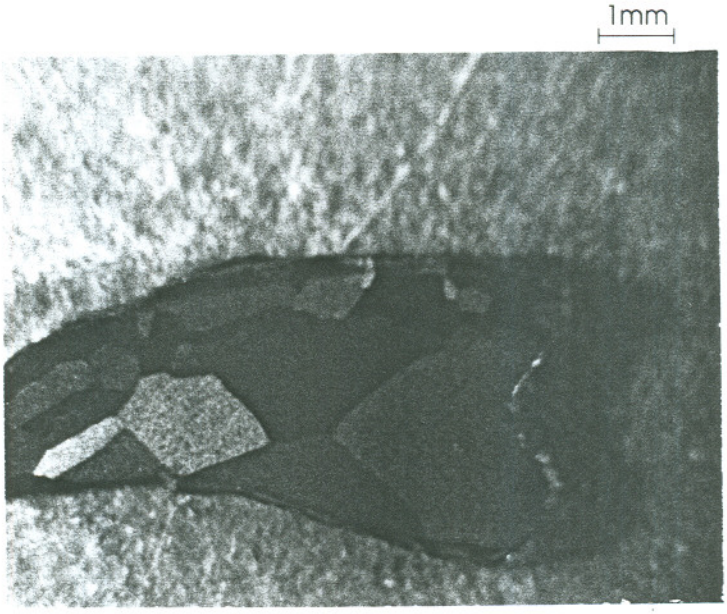


Figure 2.5 Micrograph of an unpolished TiC_x substrate. Grain boundaries can be seen.

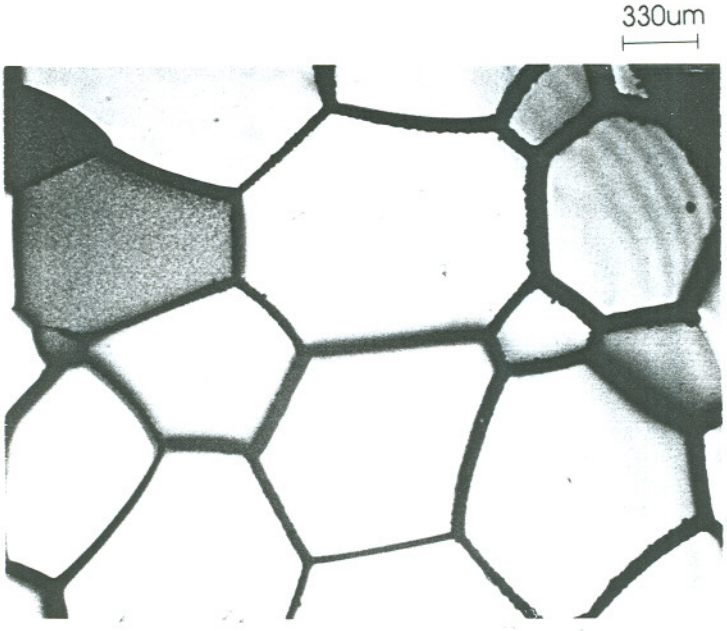


Figure 2.6 Nomarsky micrograph of a beta-SiC epi-layer on TiC_X substrate before oxidation. Grain boundaries can be easily seen.

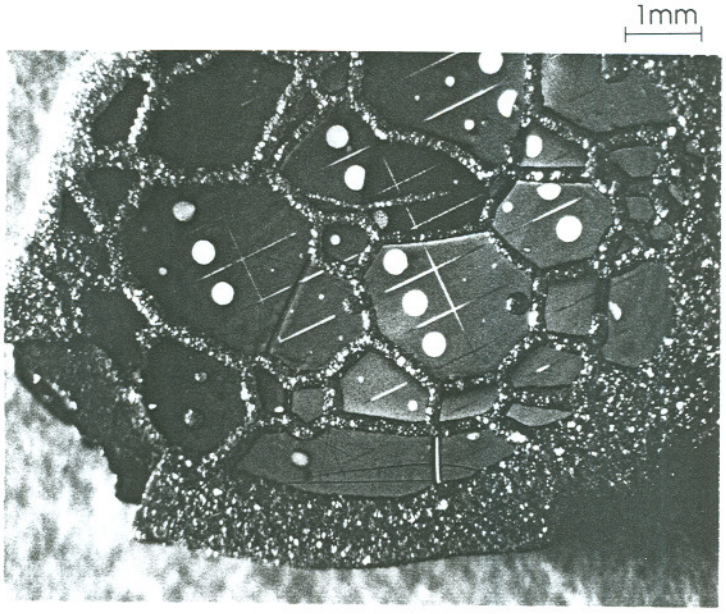


Figure 2.7 Micrograph of the same beta-SiC epi-layer as in figure 2.6 after oxidation. Grain boundaries, where beta-SiC didn't nucleate properly, shows very rough TiO_x surfaces. Note the circular dots are gate contact pads for MOS capacitors.

2.4 SUMMARY

In this chapter, we have discussed properties that make beta-SiC suitable for high temperature, high frequency and high power MOSFET applications. These properties are: high mobility, high breakdown field, wide bandgap, high thermal conductivity and good diffusion barrier property.

The synthesis approach of beta-SiC is also discussed. The decision of using TiC_x for beta-SiC epi-growth is because it contains properties suitable for the growth.

CHAPTER 3

PROCESSING AND CHARACTERIZATION

Processes developed and used for beta-SiC MOS capacitor and MOSFET fabrication are discussed in this chapter. The characterization results of these processes are also presented.

3.1 BETA-SIC EPI-GROWTH

3.1.1 Growth of beta-SiC

The TiC_x substrates were first cleaned in hot TCE, acetone and methanol (standard cleaning procedure), followed by etching in 4.8% HF for 2 min. and TiC etching solution, $HNO_3 : H_2SO_4 : H_20 = 5 : 4 : 1$, for 1 min. The 4.8% HF removed native oxide grown at room temperature, and the etching solution removed about 16 Å of TiC (see TiC etching in this chapter for details of TiC etching experiments). The freshly etched TiC_x gives a better epitaxial growth because strain in the TiC_x surface, from the polishing process, is removed. After etching, the sample substrates were loaded into the CVD reactor in Ar flow.

After leak checking the CVD growth system, the substrates were heated up to 1000 °C in 2.9 SLPM Ar (standard heat-up procedure), which (instead of

H_2) was used before 1000 °C to prevent the formation of Ti hydride. Since H_2 was used to carry organometallic sources, the same flow rate of H_2 was introduced, and Ar was bypassed at the same time. Samples were then heated up to 1600 °C for a 20 min. annealing in 11.3 sccm C_2H_4; this annealing procedure seemed to reduce the carbon deficiency in TiC_x ($X < 1$) substrates and gave a better epi-growth. After the annealing, the substrates were brought down to 1290 °C and ready for beta-SiC growth. 4 sccm of $C_2H_{10}Si_2 + H_2$ was subsequently introduced into the CVD system to start the epi-growth. Shut down procedure was in the reverse order without the 1600°C annealing. Al doped and B doped beta-SiC epitaxial growth were similar to the undoped beta-SiC growth except that ($(isoC_4H_9)_3Al$) for aluminum doped and B_2H_6 for boron doped beta-SiC were introduced along with $C_2H_{10}Si_2 + H_2$ during the beta-SiC epitaxial growth.

3.1.2 Growth characterization

3.1.2a Morphology and Crystallinity

The Nomarsky microscope and the scanning electron microscope (SEM) were used to observe the surface morphology of beta-SiC epi-layers and to document growth results. The surfaces of as-grown layers were usually rough. However, with 0.1 um diamond paste, samples were able to be polished smoothly. Surface roughness was independent of the growth time. Nomarsky micrographs of an as-grown beta-SiC layer and a polished layer are shown in

figure 3.1 and figure 3.2, respectively. The only visible defects after polish are pits, which were reproduced from the pits in the TiC_x substrate. An SEM micrograph of a polished layer is shown in figure 3.3. The single crystal nature of the grown beta-SiC layers was verified by electron channeling contrast pattern (ECCP), shown in figure 3.4.

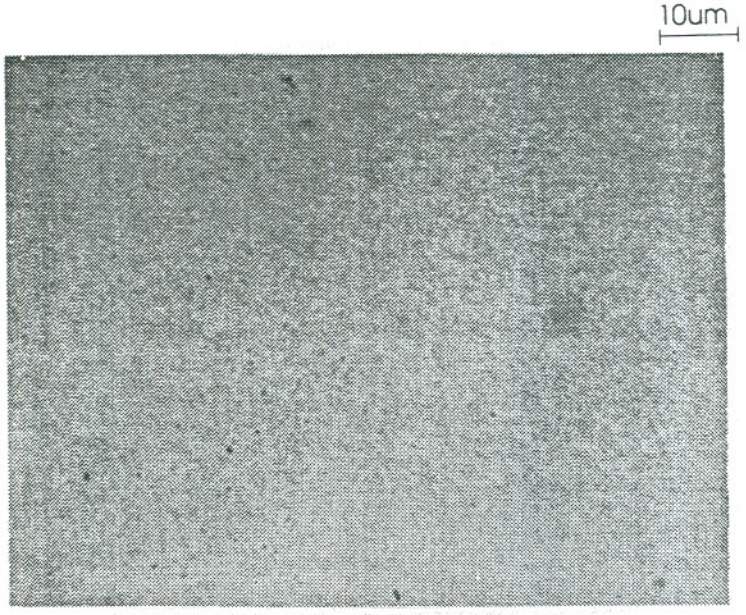


Figure 3.1 Nomarsky micrograph of an as-grown beta-SiC epi-layer.

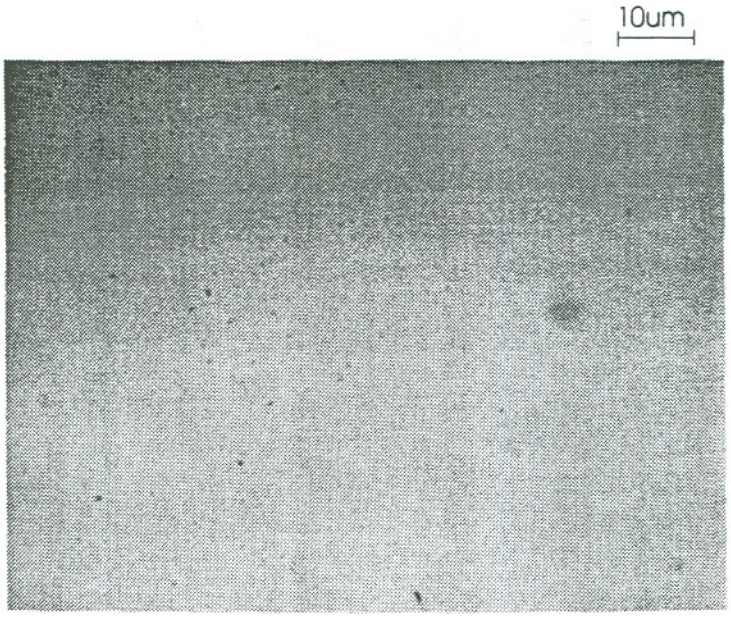


Figure 3.2 Nomarsky micrograph of the sample in figure 3.1 after 5 min. 0.1 um diamond paste polish.

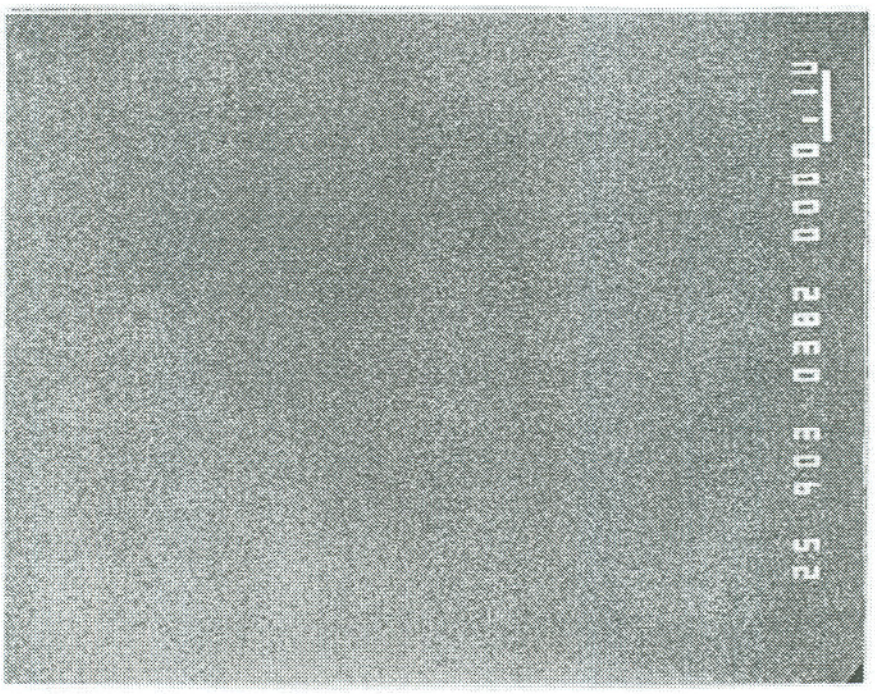


Figure 3.3 SEM micrograph of a polished beta-SiC epi-layer.

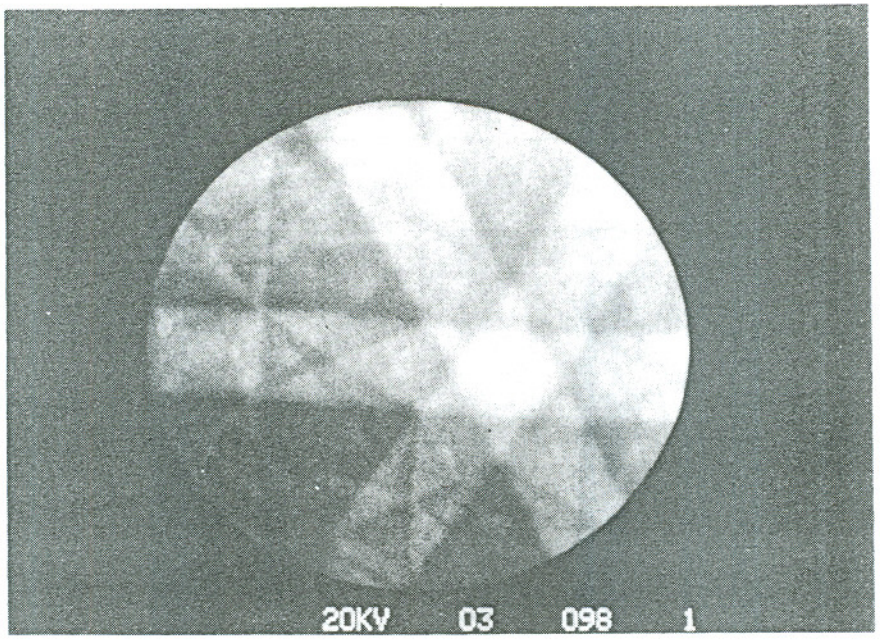


Figure 3.4 A typical micrograph of electron channeling pattern of <111> oriented, Al doped beta-SiC epi-layer.

3.1.2b Growth rate

The growth rate of beta-SiC was determined from SEM cross sections and from angle lapping, both of which are destructive methods. SEM method is destructive because samples are cleaved before being loaded into the SEM chamber. SEM results are shown in figure 3.5. Angle lapping was achieved by polishing sample's edge at 2.83° angle. Because of this lapping, the TiC thickness t was enlarged to t/sin(2.83) or 20.3 times, which can be easily measured. A typical angle lapping result is shown in figure 3.8. Both of these measurements gave about 5 um/hr growth rates.

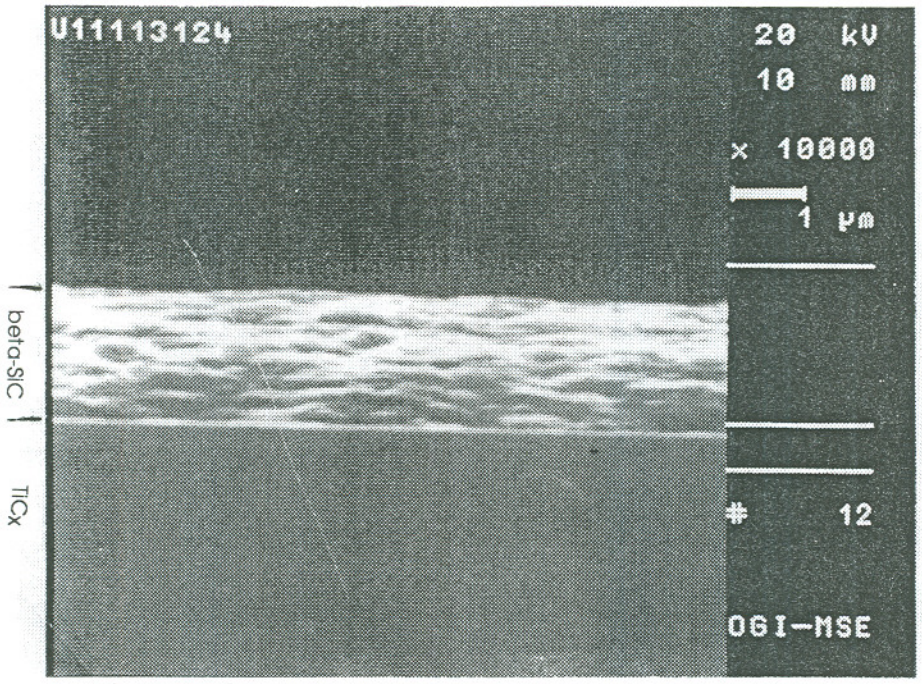


Figure 3.5 Side view of a beta-SiC epi-layer on TiC_x substrate by SEM. The 20 min. beta-SiC epi-growth resulted in a 1.6 um beta-SiC epi-layer.

A non-destructive method of estimating growth rate was by counting interference fringes after the CVD growth or any time during the growth, figure 3.6. Red and green fringes are usually easy to distinguish because the TiC_x substrate has a very reflective metal surface. The number of red fringes was between 35 and 40 per hour for our present growth condition. With the wavelength of red light (λ~ 6400 Å), refractive index of beta-SiC (n=2.48), number of red fringes (m) and a simple optical equation,

$$t = \frac{(m + \frac{1}{2})\lambda}{2n}, \qquad (3.1)$$

the growth rate of beta-SiC, t, was estimated between 4.8 and 5.2 um/hr. However, this is a very rough estimate because the sensitivity to light may be

different for different individuals.

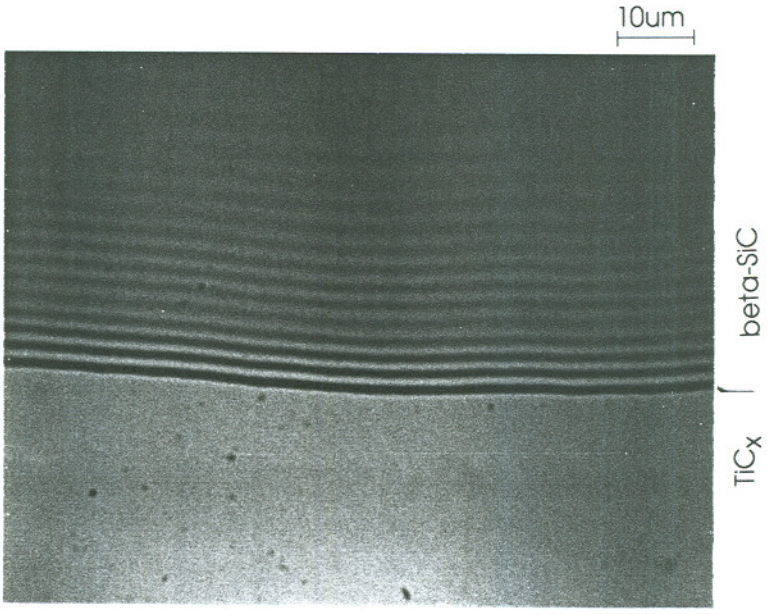


Figure 3.6 Top view of a beta-SiC epi-layer by a Nomarsky microscope. The interference fringes can be easily seen on the edge of the beta-SiC epi-layer because of the thinning edge.

3.2 Reactive Ion Etching of Beta-SiC

The reactive ion etching of beta-SiC was performed in a Plasmtrac 2406 reactive ion etching system. Sulfur hexafluoride (SF_6) was used as the reactant in the etching process, and Al, about 4000 Å thick deposited by vacuum evaporator, was used as a pattern masking material. All RIE etching of beta-SiC was performed using 80 mtorr SF_6 pressure and 150 watts of RF power. The etching rates of beta-SiC, TiC and Al, measured by a Sloan DEKTAK depth profiler, were 800 Å/min., 800 Å/min. and 17 Å/min., respectively.

3.3 TiC Epi-growth and Etching

Titanium carbide epi-layer was used in the beta-SiC MOSFETs as a "lift-off" layer for defining sources and drains. Therefore, the epi-growth procedure, growth characterization and wet chemical etching of TiC are described in the next few sections.

3.3.1 Growth of TiC

Titanium carbide was grown by CVD in the system used for beta-SiC. Samples, beta-SiC epi-layers on TiC_x, were first cleaned with our standard cleaning procedure, followed by a 2 min. 4.8% HF etching to remove native oxide. They were subsequently loaded into the CVD reactor. After the standard leak-check and heat-up procedure, 11.3 sccm ethylene (C_2H_4) was introduced into the CVD system to condition the sample surface at desired growth temperatures. 30 seconds later, titanium tetrachloride ($TiCl_4$) was introduced into the system, and the growth started.

3.3.2 Growth results and discussion

The growth rate and morphology of TiC epi-layers were used to judge the growth results. The morphology was determined by a Nomarsky microscope, and the growth rates of TiC epi-layers were measured by angle lapping. A typical angle lapping result is shown in figures 3.7 and 3.8.

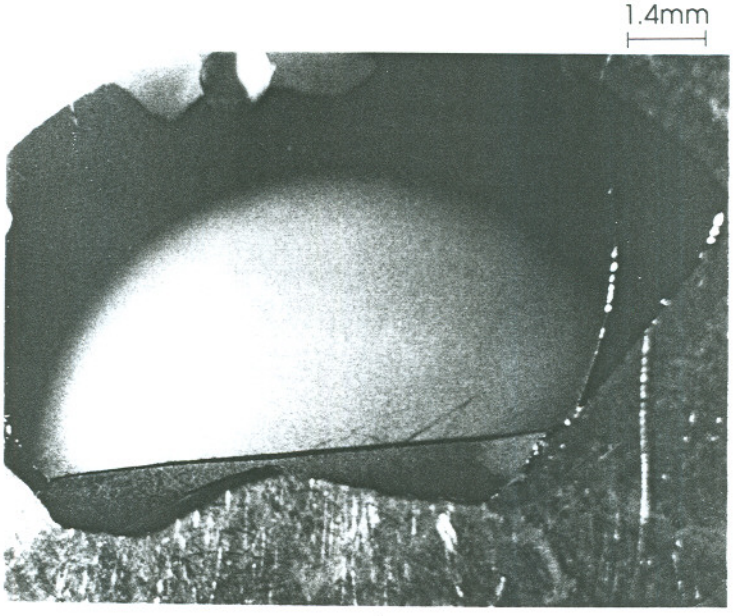


Figure 3.7 Top view of sample TiC11111007 after angle lapping. Note that the half-moon shape layer is the beta-SiC epi-layer, below which is the W shape TiC_x substrate.

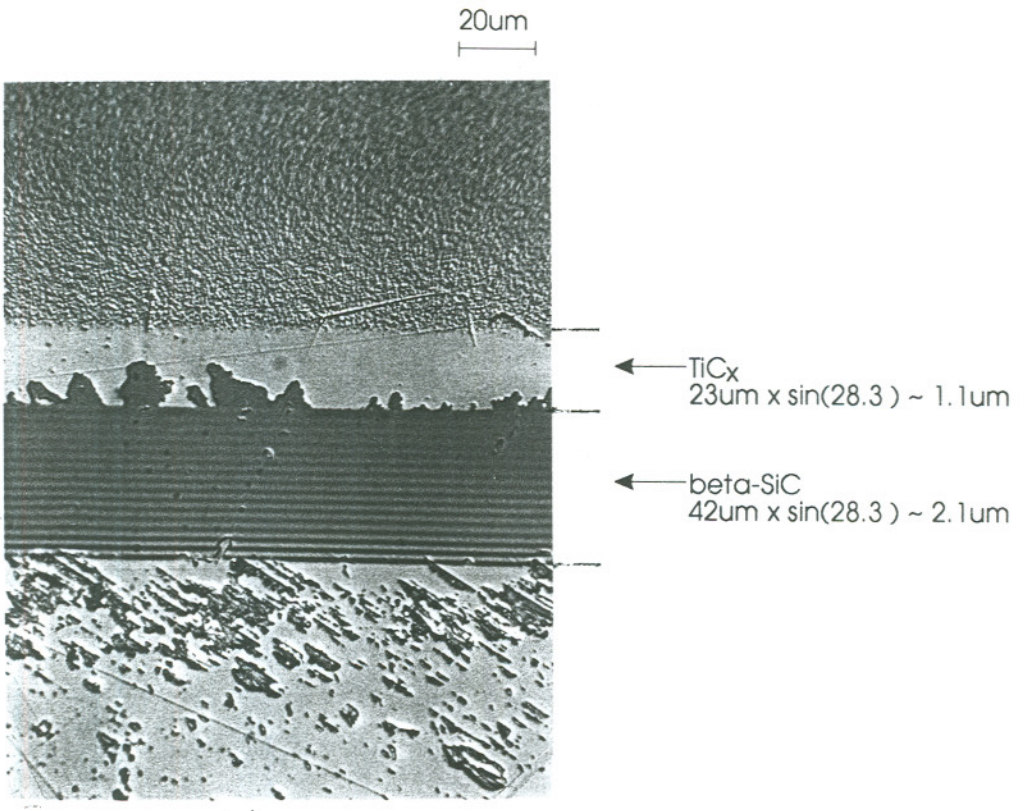


Figure 3.8 Enlarged view of the beta-SiC and TiC interface in figure 3.7. The TiC_x layer was grown for 30 min. Note that the bottom 1/3 of the micrograph is the TiC_x substrate, the top half of the micrograph is the TiC epi-layer, and beta-SiC is between the TiC_x substrate and the TiC epi-layer. Interference fringes are seen in the beta-SiC epi-layer because of its thinning edge. The thickness calculations of the TiC epi-layer and beta-SiC epi-layer are given in the right-hand side of the micrograph.

Several experiments were carried out to determine conditions suitable for TiC epitaxial growth. The results of these experiments are listed in Table 3.1.

Table 3.1 Results of TiC epi-growth.

Sample	Flow Rate (sccm)		Tg(C)	X(um/hr)	C/Ti	Morph.
	Q(TiCl4)	Q(C2H4)				
TiC002	0.85	0.5	1227	1.64	1.2	2
TiC003	0.85	1.0	1227	1.64	2.4	2
TiC004	0.85	0.25	1227	3.5	0.6	5
TiC005	0.85	0.43	1227	1.74	1.0	1
TiC006	0.85	0.5	1127	1.7	1.2	2
TiC007	0.85	1.0	1127	1.6	2.4	2
TiC008	0.85	1.0	1027	0.78	2.4	2
TiC009	0.85	1.0	1077	1.64	2.4	2
TiC010	0.85	0.43	1077	1.74	1.0	2
TiC011	0.85	0.43	1277	1.7	1.0	1
TiC012	0.85	0.43	1250	1.72	1.0	1

Tg=growth temperature. X=growth rate.
Morph.= morphology. C/Ti=carbon to titanium ratio

TiC002, TiC003, TiC004 and TiC005 were grown at the same Tg with different C/Ti ratios, 1.2, 2.4, 0.6 and 1.0, respectively. TiC004 had a very poor morphology; however, TiC002, TiC003 and TiC005 had about the same morphology and growth rate. This suggests that sufficient carbon atoms, C/Ti > 0.6, are needed to nucleate properly and that titanium atoms control the growth rate. TiC006 and TiC007 together with TiC009 and TiC010 confirm this conclusion.

TiC003, TiC007, TiC008 and TiC009 were grown at the same C/Ti ratio with different growth temperatures, 1227, 1127, 1027 and 1077 °C, respectively. TiC008 had very low growth rate, 0.78um/hr compared to 1.7um/hr for the other samples; on the other hand, TiC003, TiC007 and TiC009 have nearly identical

growth rates. This indicates that the growth temperature should be higher than 1027 °C in order to grow TiC efficiently. The highest temperature at which a TiC epi-layer can be grown may be higher than 1277 °C. However, we did not explore temperatures higher than 1277 °C. 1200 °C was used to grow TiC lift-off layers for defining the sources and drains of beta-SiC MOSFETs. The TiC epi-layer grown at 1200 °C, verified by electron channeling contrast patterns (ECCP), was single crystal.

3.3.3 Wet etching of TiC

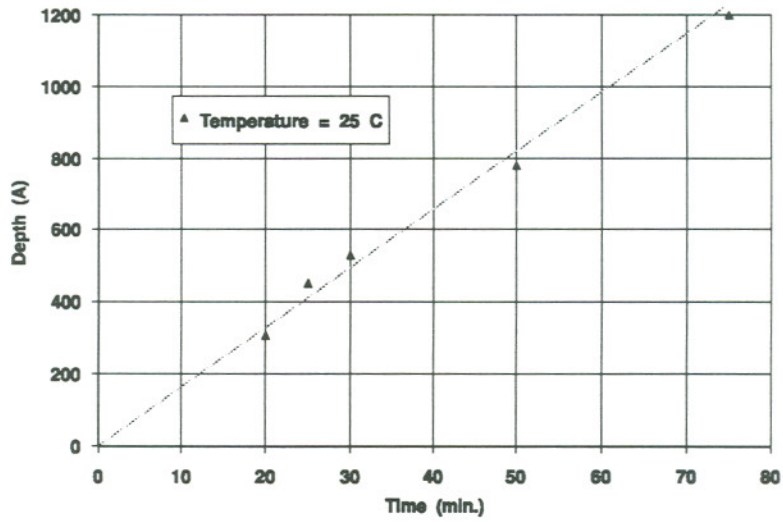


Figure 3.9 TiC etch depth versus time at 25 °C using TiC etching solution (H_2SO_4 : HNO_3 : H_2O = 1 : 5 : 4).

The etching rate of TiC_x in H_2SO_4:HNO_3:H_2O = 1:5:4 calibrated on existing bulk TiC_x substrates was found to be identical to that of TiC epi-layers.

The etching experiments were carried out by patterning TiC_X substrates with photoresist. They were subsequently etched with TiC etching solution at room temperature for various time periods, followed by measurement with Sloan DEKTAK II depth profiler. From the data in figure 3.9, the TiC etching rate is about 1000 Å/hr.

3.3.4 Summary of TiC epi-layer properties

The properties of TiC epi-layer are summarized in the following table.

Table 3.2 Summary of TiC epi-layer properties.

PROPERTY	RESULT
Advantages:	
low resistivity (~10 uΩ-cm)	The low resistivity of TiC makes TiC suitable for inter-connect for devices.
Easy to form	As described in the processing paragraph, TiC film can be grown at any temperature between 1077 and 1277°C. Hence, no precise control of temperature is needed.
Easy to etch for pattern generation	TiC is very easy to etch by TiC etching solution described the previous section. Best of all, this TiC etching solution does not attack beta-SiC epi-layers.
Good adhesion to beta-SiC	In order to test the adhesion of TiC dots to the beta-SiC substrate, 2.4um tungsten carbide probes were used to scribe these dots from several different directions. None of the TiC dots were peeled off.

Does not contaminate devices, wafers, or working apparatus	No evidence of contamination was observed during CVD growth or processing. In addition, TiC epi-layers can be completely removed from beta-SiC substrates by TiC etching solution without damaging the beta-SiC substrates.
Disadvantages:	
Not stable in oxidizing ambient	Both TiC_x substrates and epitaxial TiC films oxidize in an oxygen environment at a very low temperature, ~600 °C. Furthermore, the volume of TiC_x increases dramatically after oxidation, making later processing very difficult (figure 2.8).
Reacts with silicon oxide during high temperature CVD	The biggest drawback of TiC is that titanium reacts with silicon oxide (SiO_x) during the CVD process; worst of all, the oxide, which is used to passivate sample surfaces or as a dielectric material, is converted totally into a conducting layer. One possible way to avoid this problem is to use dielectric material other than oxide, such as nitride. However, further investigation is needed.

3.4 Gate Metal and n-Type Beta-SiC Contact Metal Deposition

Aluminum (Al) was used both as a gate and ohmic contact metal in the beta-SiC MOSFETs. However, when Al is exposed to air or higher temperature, it forms a thin oxide layer on the surface, which makes device probing very difficult. To avoid this problem, gold (Au), which does not form a protective oxide, was used to prevent Al oxidation. Therefore, to make gate electrodes or contact pads, aluminum, about 1000Å, was deposited on the samples in high vacuum (about $2x10^{-7}$ torr), followed by a 500 Å Au evaporation.

3.5 OXIDATION

The insulator is one of the most important components for a metal oxide semiconductor device. Nitride and oxide are two possible choices for the insulator in a metal-insulator-semiconductor (MIS) structure. Since the oxide was reported to have better properties[1], it was used as an insulator for both beta-SiC MOS capacitors and MOSFETs in this thesis. The developed oxidation procedure can be used for device passivation. Therefore, oxidation and its results are discussed in detail in the following sections.

3.5.1 Growth of oxide

In this oxidation study, thermal oxides were grown on undoped and Al doped beta-SiC epi-layers[2] for device applications. The beta-SiC epitaxial layers used in the study were grown on <111>7°→<0$\underline{1}$1> TiC_x substrates by CVD, and the grown layers were single crystal beta-SiC, which was verified by ECCP.

Because several groups have reported the thermal oxide of both alpha- and beta-SiC was silicon dioxide (SiO_2) and similar to the thermal oxide of Si[3,4], the beta-SiC oxidation procedure followed the Si oxidation procedure closely. Before oxidation, the samples were cleaned with hot TCE, acetone and methanol, and subsequently etched in 4.8% HF for 1 min. to remove native oxide. The samples were loaded into the oxidation system in 1990 sccm Ar, followed by increasing the furnace temperature to desired temperatures. When the oxidation started, 1600 sccm oxygen was introduced into the system through a bubbler,

which was filled with 70 °C water (H_2O), and the Ar was bypassed at the same time; the flow rate of H_2O vapor was calculated to be about 391 sccm at 70 °C. After the oxidation, the oxygen was bypassed, and Ar was introduced. The temperature of the furnace was subsequently reduced to 50 °C below the oxidation temperature, and the samples were annealed for 20 min. in Ar to remove oxidation-induced defects and fixed oxide charges. The samples were removed at 650 °C.

3.5.2 Results and discussion

The major purpose of the oxidation study was to determine its growth rate. Wet oxidations on undoped samples were performed at 1100 °C, 1150 °C and 1200 °C using undoped beta-SiC epi-layers for 1, 2, and 4 hours. Dry oxidations on undoped samples were carried out only at 1100 °C, 1150 °C and 1200 °C for 2 hours. Their results are shown in figures 3.10 and 3.11.

Auger electron spectroscopy (AES) was also used to determine the oxide properties. The AES results are used to develop a model for beta-SiC oxidation process, and experimental results are fitted into this model in the end of this section.

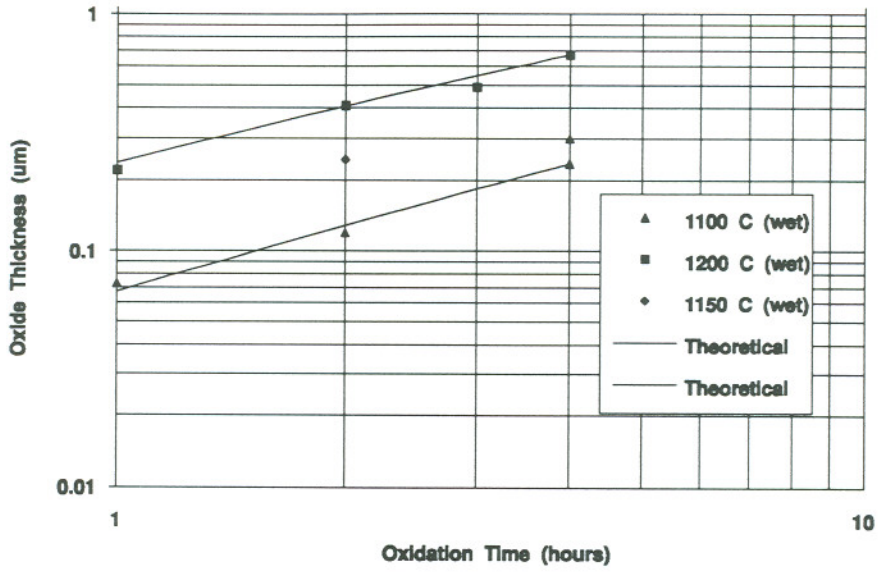


Figure 3.10 Oxidation thickness as a function of reaction time in a stream ambient (70 °C water) for beta-SiC epi-layer on <111>7°→<0$\bar{1}$1> TiC_x substrates at 1100, 1150 and 1200 °C.

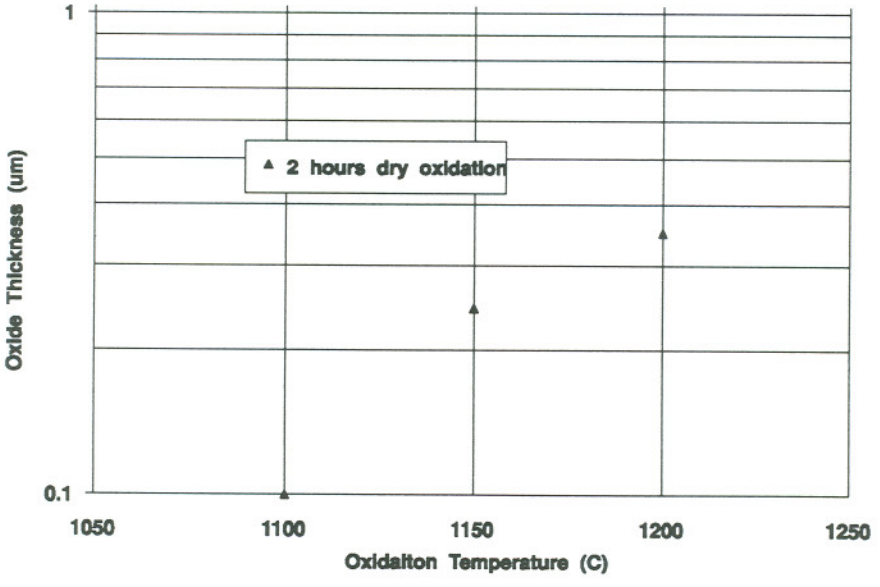


Figure 3.11 Oxide thickness as a function of temperature in dry oxygen for beta-SiC epi-layer on <111>7°→<0$\bar{1}$1> TiC_x substrates. The oxidation time was 2 hours for all three temperatures.

3.5.2a Oxide thickness

The oxide thickness was measured with a DEKTAK depth profiler. Before the depth profile measurement, the oxidized samples were patterned with photoresist, then etched by 6:1 buffered HF etching solution. The photolithography processing steps used were exactly the same as the procedures used for thermal oxides of Si. The oxide thicknesses were also determined by C-V measurements of the MOS capacitors, described in the next chapter.

The growth thickness of oxide on the Al doped samples, which were used for beta-SiC MOSFETs, was around 450 Å for the first hour at 1100 °C. This oxidation thickness is significantly lower than that of undoped beta-SiC, whose oxidation thickness for the first hour at 1100 °C was about 600 Å. One possible explanation of this decrease is that the aluminum may be incorporated into the silica during the oxide growth, thereby increasing the strength of the bond structure in silica. Because of the increasing bond strength between silicon and oxygen, the water enters the oxide less efficiently and diffuses through the oxide more slowly. As a result, the oxidation rate of Al-doped beta-SiC was lower. However, more studies are needed to verify this explanation.

3.5.2b Auger analysis

A Perkin-Elmer scanning Auger electron microscope was used for AES analysis. The primary electron beam used 5 KV of accelerating voltage and 0.117 uA current, and an Ar ion beam, 3 kV accelerating voltage and 0.5 mA current, was used to sputter the surface before AES analysis at different depths. The oxide

sputtering rate of this particular setup is 212 Å/min.

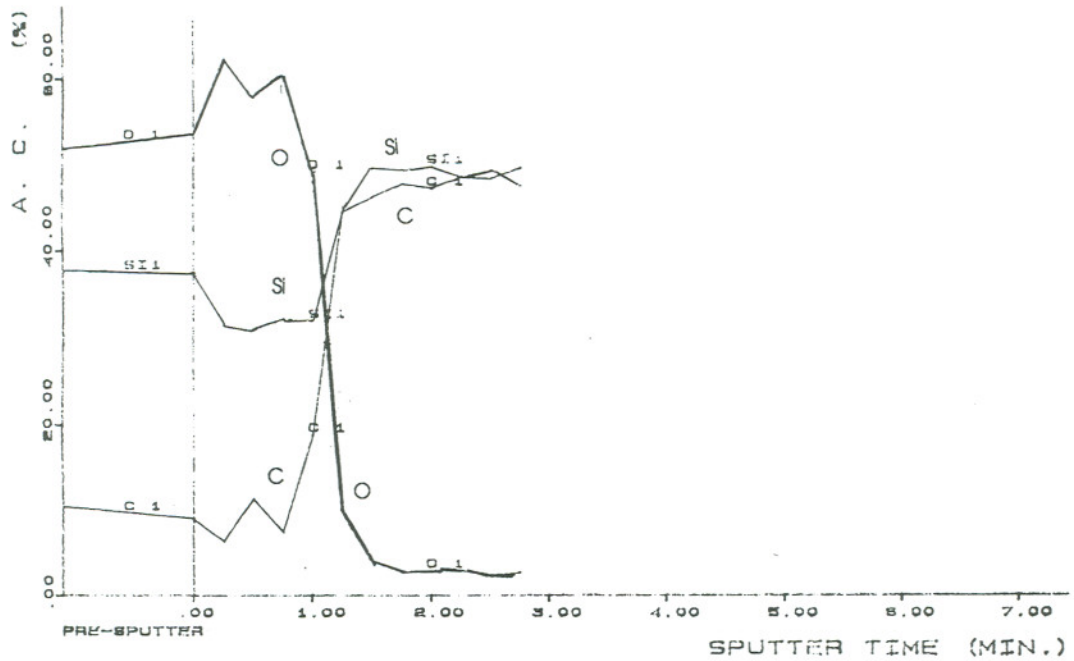


Figure 3.12 Auger depth profile of thermal oxide grown on beta-SiC epi-layer.

A typical AES profile of thermal oxide on undoped beta-SiC is shown in figure 3.12. The AES result shows that the oxide grown in wet oxidation is highly stoichiometric (Si/O ~ 0.5 to 0.54) and has less than 10 atomic percent carbon without the consideration of the carbon background noise and the matrix effect for C atoms in the oxide. With the consideration of background noise, the carbon percentage in the oxide is less than 5%; the matrix effect of carbon in oxide is beyond the scope of this dissertation. This result is lower than the 14% carbon in oxide reported by Chaudhry in 1987[1].

Other conclusions from the AES result are: The transition layer between

the oxide and beta-SiC was about 160 Å from the 212 Å/min. sputtering rate of oxide. No pile-up or depletion was observed in the interface region. The number of Si and C atoms was equal in the beta-SiC layer. The ratio of carbon peak-to-peak height in oxide and beta-SiC is 1:5, which implies that the C concentration is much lower in the oxide layer.

From a) the stoichiometric oxide, b) no pile-up of carbon in the interface and c) low carbon concentration in oxide, the oxidation process can be explained as follows: In the oxidation of beta-SiC, the O_2 diffuses to the SiO_2 - beta-SiC interface and reacts with SiC by breaking the Si-C bonds. The reaction produces C, CO, SiO_2 or CO_2. Since the diameter of CO_2 is 20% larger than the SiO_2 ring width[5], it is very unlikely that CO_2 can diffuse out of the oxide. Therefore, from observation b, either no reaction producing CO_2 occurs, or CO_2 decomposes into C or CO, both of which are more mobile than CO_2 and diffuse out. However, a small amount of the C atoms is left behind and remains in the oxide (from observation a and c). Using this beta-SiC oxidation model, modeling of oxidation in beta-SiC is discussed in the next section.

3.5.2c Modeling of oxidation in beta-SiC

Several factors must be considered for modeling oxidation in beta-SiC. These factors are:

a) transfer of the oxidizing species (O_2 or H_2O) from the gas to the outer layer of oxide.

b) transport of the oxidizing species across the oxide to the SiO_2 and beta-SiC interface.

c) reaction of the oxidizing species at the SiO_2 and beta-SiC interface.

d) transport of by-product gases (C and CO) from the SiO_2 and beta-SiC interface to the oxide surface.

e) existence of residual carbon in the oxide.

The out-diffusion of by-product gases has little effect on the oxidation process except in collisions among in-diffusing oxidizing species, out-diffusing by-product gases and remaining carbon atoms. This collision process can be modeled in the diffusivity of the oxidizing species. Since the effects of out-diffusing by-product gases are taken into account in the modeling of the in-diffusing species, the mathematical treatment of beta-SiC thermal oxidation process is exactly the same as that of Si[6]. Therefore, thermal oxidation of beta-SiC obeys the following relationship:

$$x_o^2 + Ax_o = B(t+\tau), \qquad (3.2)$$

which is based on the diffusion process through the oxide and the reaction at the interface. A , B and τ are constants which depend on oxidation conditions, and x_o is the oxide thickness. B is called the parabolic rate constant, and B/A is the linear rate constant.

From the model of oxidation, two predictions can be made: a) the energy

required to react H_2O with beta-SiC will be close to the energy required to break a Si-C bond, and b) the energy required to diffuse oxidizing species across oxide in beta-SiC will be higher than that in Si because the collision of in- and out-diffusing species makes the diffusion of oxidizing species less efficient than that in Si.

3.5.2d Fitting results into model

Parameters (A, B and τ) of wet oxidation on undoped beta-SiC are calculated for 1100 °C and 1200 °C wet oxidation by least squares method. However, it should be understood that only a minimum number of oxidation experiments were carried out because of the scarcity of TiC_x substrates. The calculated results may have more than 10% of uncertainty.

The constant τ was found to be very close to zero for both 1100 °C (τ=-0.016) and 1200 C (τ=0.017), which is the same as that reported for wet thermal oxidation of Si. Using A, B and τ values, theoretical curves of oxidation thickness versus oxidation time at two different temperatures are shown in figure 3.10.

Rewriting equation 3.2, it can be expressed in another form:

$$\frac{x_o}{A/2} = (1 + \frac{t+\tau}{A^2/4B})^{1/2} - 1 \ . \qquad (3.3)$$

In other words, equation 3.2 can be expressed by the normalized thickness

$x_o/(A/2)$ and the normalized oxidation time $(t+\tau)/(A^2/4B)$ for both temperatures. The normalized results were calculated for all data in figure 3.10. The theoretical curve after normalization was also calculated based on A, B and τ of 1100 °C oxidation data. The normalized oxidation thickness versus normalized oxidation time is shown in figure 3.13 for both experimental and theoretical results. The good agreement between these results confirms that thermal oxidation of beta-SiC followed equation 3.2.

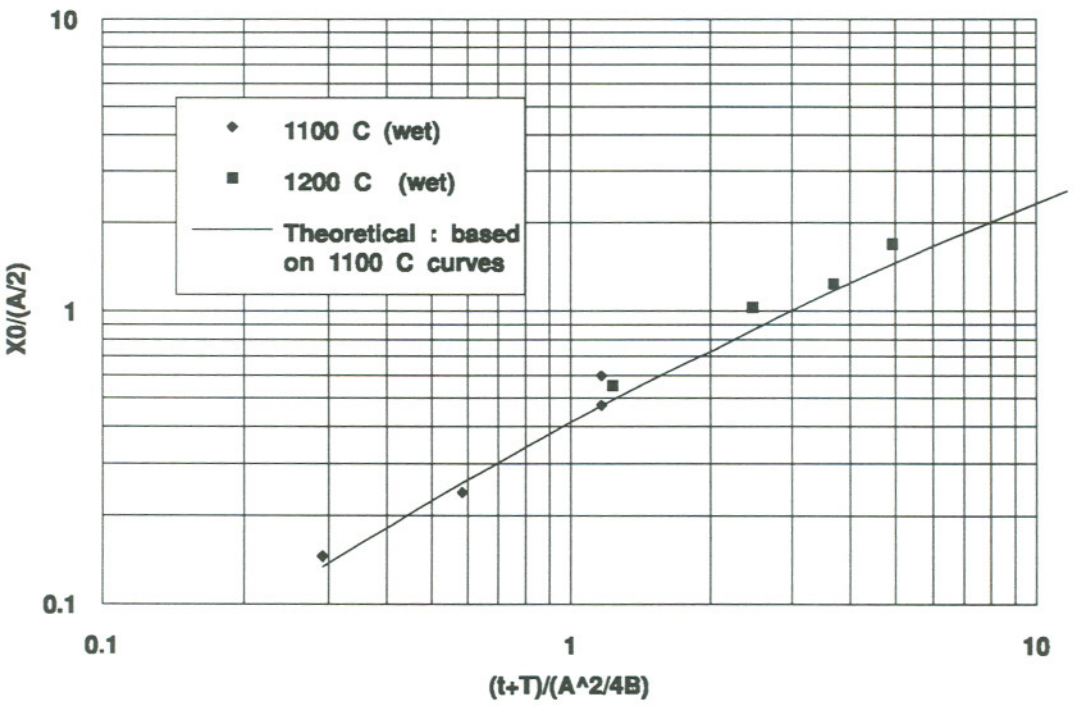


Figure 3.13 Normalized oxide thickness as a function of normalized oxide thickness for wet oxidation at 1100, 1150 and 1200 °C. The theoretical curve was obtained from 1100 °C oxidation data.

In equation 3.2, the value of B (the parabolic rate constant) depends on diffusion across the already formed oxide, and is independent of the orientation of crystal; the value of B/A (the linear rate constant) is related to breaking bonds at the semiconductor interface, and therefore depends on crystal orientation[6]. In our experiments, all substrates are <111>7°→<01$\underline{1}$> orientation; therefore, the orientation consideration was ignored. The oxidation diffusion activation energy (E_a), which is defined by Adamsky[7] as the energy necessary to initiate diffusion through the oxide, was calculated from the relation between E_a and B:

$$B = K \exp(-E_a/kT),[8] \qquad (3.4)$$

where K is a constant, k is the Boltzmann's constant, and T is the oxidation temperature in degrees Kelvin. Similarly, activation energy for breaking bonds (E_a') was calculated from

$$B/A = K \exp(-E_a'/kT).[8] \qquad (3.5)$$

The resulting E_a is 2.15 eV or 50 kcal/mole. This result is similar to 48 kcal/mole from wet oxidation of 6H-SiC by Suzuki et al.[3] or 47 kcal/mole from dry oxidation of 6H-SiC by Harris et al.[9] As predicted in the model, E_a in beta-SiC is higher than that in Si. For comparison, Deal and Grove found 16.3 kcal/mole for E_a in Si, which was shown to agree with the value of 18.3 kcal/mole reported for the activation energy for diffusion of H_2O in SiO_2.[6]

E_a' of beta-SiC was calculated to be 2.5 eV or 59 kcal/mole. To break a Si-C bond requires 69.3 kcal/mole[10], which is quite close to the calculated E_a', 59 kcal/mole, from our oxidation experiment. On the other hand, Suzuki et al.[3] reported 26 kcal/mole for E_a', which is much lower than the 69.3 kcal/mole required to break a Si-C bond. One possible explanation of this phenomenon is the dangling bonds on the 6H-SiC surface. These dangling bonds reduce significantly the energy required to break a SiC bond. However, further investigation is needed.

At present, calculation of activation energy is available only for two temperatures. Oxidation at other temperatures should be carried out in the future to increase the precision of activation energy calculation when TiC_x substrates are more readily available.

3.6 SUMMARY

In this chapter, we have described the necessary processing techniques for the beta-SiC MOS capacitor and MOSFET. The reactive ion etching rate of beta-SiC in SF_6 was found to be 800 Å /min. for both TiC and beta-SiC. TiC epi-growth experiment was discussed, and etching rate of TiC in titanium carbide etching solution was found about 1000 Å/hr. The procedure for evaporating gate and contact metal was described. The oxidation rate of beta-SiC was calibrated, and a model for beta-SiC oxidation process was developed. Oxidation results are found fitting the model very well.

CHAPTER 4

BETA-SIC MOS CAPACITOR FABRICATION AND CHARACTERIZATION

The Metal Oxide Semiconductor (MOS) capacitor is an important preliminary device for fabricating MOSFET devices. From measurements (listed in Table 4.1) of MOS capacitors, close to two dozen oxide properties can be obtained. These oxide properties can be used to understand the basic properties of beta-SiC and as a reference for beta-SiC MOSFET fabrication.

The background concentrations of the undoped beta-SiC epi-layers were about 10^{18} cm^{-3} (n-type). This was because the sizes of TiC_x substrates used for growths are usually less than 1 cm^2. The small TiC_x substrates resulted in auto doping effect from the gas flow eddies near the graphite mask (figure 2.4). Few large TiC_x substrates with low subgrain densities were available at the time this work was performed.

Table 4.1 Properties which can be determined from measurements of MOS capacitors

1*	Results of thermally activated chemical reaction and electrochemical reactions in SiO_2.
2*	Diffusion of water into SiO_2.
3*	Dielectric constant of semiconductor and SiO_2.

4*	Conductivity type of the semiconductor.
5*	Band-to-band tunneling in the semiconductor and tunneling into SiO_2.
6*	Oxide breakdown field.
7*	Oxide thickness.
8*	Doping profile in the semiconductor.
9*	Surface band bending and depletion layer width in the semiconductor as a function of gate bias.
10*	Charge configurations in the oxide such as oxide fixed charge and the charge at interface between SiO_2 and another insulator on top of it.
11	Voltage and field at avalanche breakdown in the semiconductor.
12*	Interface trap level density as a function of energy in the bandgap.
13	Interface trap capture probability for both electrons and holes as a function of energy in the bandgap.
14	Lifetime in the bulk semiconductor.
15	Surface recombination velocity.
16	Nonuniformities in the oxide charge distribution and nonuniformities of surface potential caused by the discrete nature of charge in the oxide.
17	Work function differences between semiconductor and gate.
18	Ionic drift polarization effects in SiO_2.
19	Quantum effects in the inversion layer at low temperatures (surface quantization).
20	Properties of electron and hole traps in SiO_2.

* Properties considered in this thesis.

4.1 BUILDING BLOCKS

The "Metal Oxide Semiconductor" capacitor consists a metal, an oxide and a semiconductor. The beta-SiC MOS capacitors measured in this thesis were comprised of Al for gate metal and beta-SiC wet thermal oxide for insulator.

Back contacts to the semiconductor affect the C-V measurement results significantly. Especially when the metal-semiconductor back contact is a rectifying junction instead of an ohmic or an injecting junction, the depletion layer of the interface makes C-V measurements unreliable. We were able to

obtain very good ohmic or injecting back contacts to beta-SiC, using TiC_x substrates as a n-type contact and platinum (Pt) as a p-type contact. A typical I-V curve of a TiC_x contact pad on highly doped n-type beta-SiC is shown in figure 4.1. The tested sample had a CVD grown TiC_x contact pad, a n-type beta SiC epi-layer and a TiC_x substrate structure. The measurement was done by positioning one probe on the CVD TiC_x pad and the other probe on the TiC_x substrate.

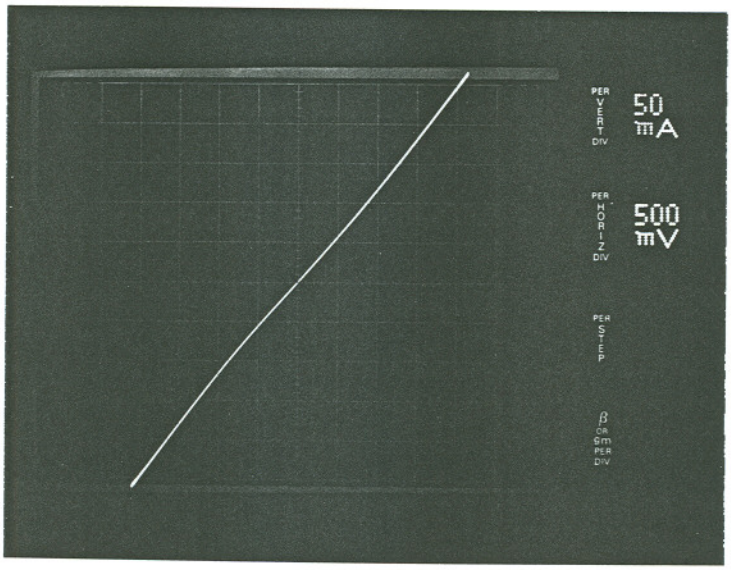


Figure 4.1 A typical I-V curve of a TiC ohmic contact pad on undoped beta-SiC and $4.2*10^{-3}$ sccm Al-doped beta-SiC. The tested sample had a (TiC_x contact pad) - (ß-SiC) - (TiC_x substrate) structure. The area of the TiC_x pad was $3*10^{-4}$ cm^2. This result shows a good ohmic or injecting contact.

4.2 PROCESSING

4.2.1 n-type beta-SiC MOS capacitor

Titanium carbide substrates were first chosen according to their X-ray rocking curves. Only substrates which have fewer than 2 subgrains/mm^2 were used in order to minimize the effect of subgrains. The substrates were cleaned by the standard cleaning procedure, followed by a 40 min. n-type beta-SiC growth (see chapter 3). This 40 min. epi-growth resulted in about 3.3 um beta-SiC epi-layers. The layers were then polished with 0.1 um diamond paste, followed by standard cleaning and oxidation (figure 4.2). The wet oxidation was performed at 1100 °C for 1 hour (see chapter 3 for details). Before removal from the furnace, the samples were annealed for 20 min. at 1050 °C to reduce oxidation-induced defects and oxide fixed charges. After removal from the furnace at 650 °C, the samples were immediately loaded into the vacuum evaporator to avoid contamination. About 3000 Å of Al was then evaporated on to the oxide. Finally, the Al was patterned with photoresist and etched with Al etching solution to define gate contact pads for beta-SiC MOS capacitors. The substrate contacts were achieved by removing the titanium oxide (TiO_x) on the backside of the samples before measurements.

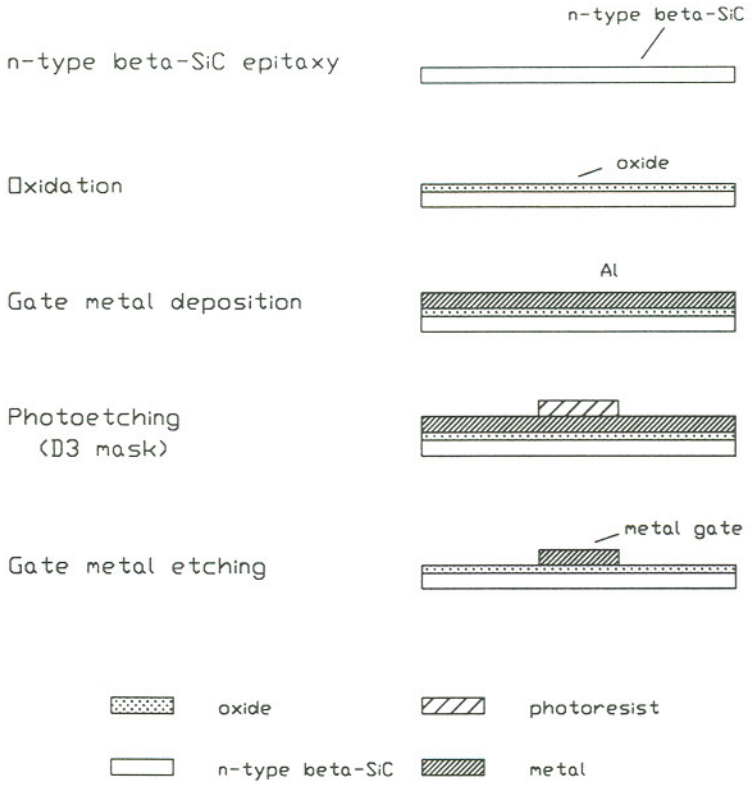


Figure 4.2 Processing steps of n-type Beta-SiC MOS capacitor.

4.2.2 p type beta-SiC MOS capacitor

The p-type beta-SiC MOS capacitors were processed quite differently from the n-type capacitors except for the substrate selection because TiC_x is a rectifying contact metal[8] for p-type beta-SiC. Boron-doped beta-SiC buffer layers, about 3.3 um, were first grown on TiC_x substrates to isolate the beta-SiC layers from the conducting TiC_x substrates, figure 4.3 and 4.4. The buffer layer was used to isolate the capacitor from the conducting TiC_x substrate (see chapter 5 for more detail information). The 3.3 um p-type beta-SiC epi-layers, the 600 Å

thick oxide and the gate metal deposition were achieved by using the same procedures as that for the n-type beta-SiC MOS capacitor described in the last section. However, in order to make a contact to p-type beta-SiC, contact cuts were first etched by using buffered HF, followed by sputter-deposition of Pt on the oxide (figure 4.3). The Pt was then patterned by photoresist and etching by platinum etching solution, $HCl : HNO_3 : H_2O = 7 : 1 : 8$, at 75 °C to define gate metal pads for measurements.

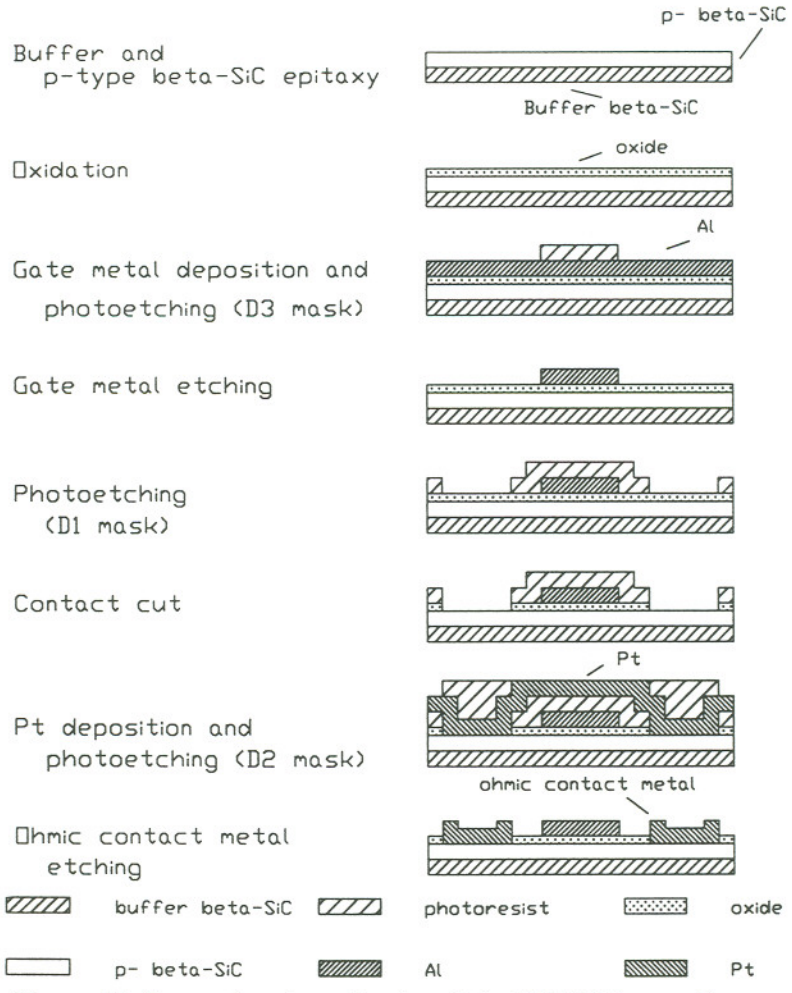


Figure 4.3 Processing steps of p-type Beta-SiC MOS capacitor.

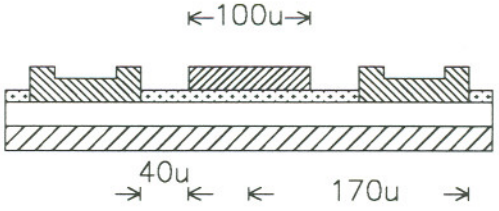


Figure 4.4 Critical Dimensions of p-type beta-SiC MOS capacitor.

4.3 CHARACTERIZATION

4.3.1 Oxide breakdown field and resistivity

The dielectric strength and resistivity are two important characteristics of oxide. These two properties were determined by current-voltage (I-V) and capacitance-voltage (C-V) measurements. I-V characteristics were obtained by applying one probe on the gate and the other probe on the back contact pad of beta-SiC MOS capacitors. Because the oxide has much higher resistivity than that of the beta-SiC layers, the voltage drop across the MOS capacitor is mostly on the oxide. The resistivity of the oxide was then estimated from Ohm's law. A typical I-V result for oxide on beta-SiC is shown in figure 4.5. Note the I-V curve is always asymmetrical because the areas of the contacts (the gate of the MOS capacitor and the ohmic contact) are different. The resistivity of thermal oxide on beta-SiC was between 10^{14} and $6*10^{14}$ Ω-cm at $1*10^{6}$ V/cm electric field.

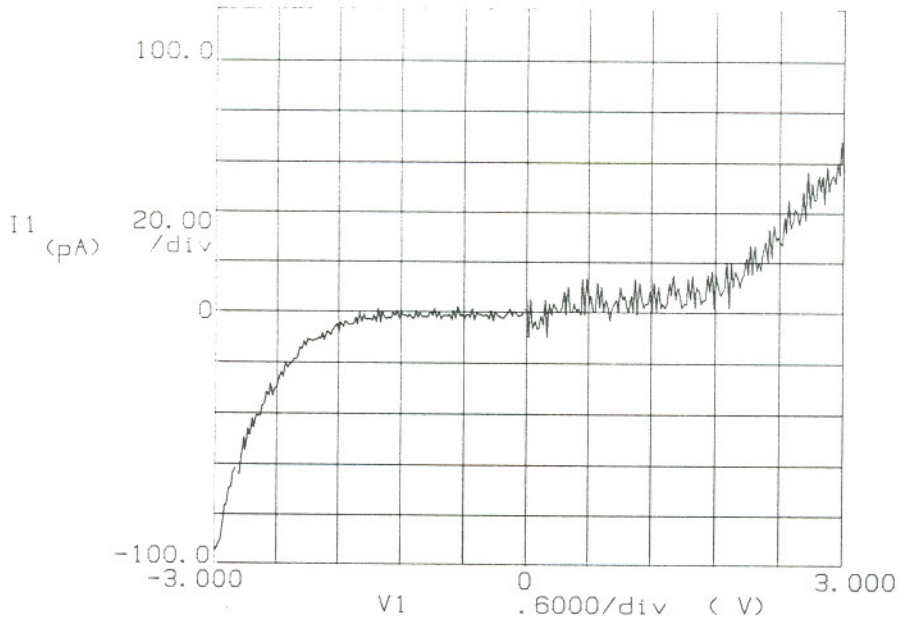


Figure 4.5 Oxide leakage current of $4.2*10^{-3}$ sccm doped beta-SiC. This leakage current is used to calculate the oxide resistivity. The oxide thickness on this sample is about 380 Å, and the metal gate's radius is 94 um.

The breakdown voltage, defined as the voltage at which the oxide is punched through, was determined by biasing the oxide to breakdown. The breakdown field of oxide on beta-SiC was between $2*10^6$ and $5*10^6$ V/cm.

4.3.2 Dielectric constant of oxide

The Auger analysis of thermal oxides on beta-SiC epi-layers showed 10% carbon atoms or 5% carbon with the consideration of carbon background noise (chapter 3) although several groups have reported carbon-free thermal oxide on beta-SiC[2,3,4]. Therefore, in spite of the fact that the breakdown field and resistivity of thermal oxide on beta-SiC show the oxide to be quite similar to

thermal oxide on Si, it is important to determine the dielectric constant of oxide in our material system because most of the important calculations for MOS capacitors are related to the dielectric constant of oxide.

The relative dielectric constant of oxide on beta-SiC was determined by measuring the maximum capacitance of MOS capacitors. The constant was calculated from

$$\varepsilon_{ox} = t_{ox} C_{max} / A_G, \qquad (4.1)$$

where t_{ox} is the oxide thickness, A_G is the area of gate metal, ε_{ox} is the permittivity of oxide and C_{max} is the maximum capacitance. The calculated relative dielectric constant from this method is between 3.3 and 4.2 with a 3.77 average value. Dielectric constant of thermal oxide on beta-SiC, 3.8, is used throughout this thesis. The wide range of calculated dielectric constant is due to the small sample size and the roughness of the oxide, which causes about 10% fluctuation in the oxide thickness measurement. In the future the dielectric constant of thermal oxide on beta-SiC should be determined from ellipsometry, which measures both thickness and refractive index of the oxide, and calculated for a more accurate dielectric constant when large TiC_x substrates and smooth beta-SiC epi-layers are available.

4.3.3 C-V measurements

4.3.3a Inversion

Capacitance-voltage (C-V) measurements of MOS capacitors were carried out by a Boonton 72BD 1 MHz capacitance meter and an HP4145B semiconductor analyzer, which is used as a voltage bias source and voltage meter for capacitance monitoring; the scan rate of the gate bias was 0.8 V/sec. Each sample was oxidized twice. The measurement results of first oxidation are shown in figure 4.6 for undoped n-type beta-SiC and figure 4.8 for lightly Al doped beta-SiC. The results for second oxidation are shown in figure 4.7 for undoped beta-SiC, figure 4.9 for lightly Al doped beta-SiC and figure 4.10 for heavily Al doped beta-SiC.

In the first oxidation, where the oxidation was carried out right after 0.1um diamond paste polishing, the low oxidation rate (about 330 Å for the undoped sample) and C-V result of beta-SiC MOS capacitor is similar to the results published by S. Zaima[17] et al. in 1990 and by K. Shibahara et al.[3] in 1984. This can be explained as due to the high defect density of beta-SiC layer. Because of this high defect density, the minority carriers, holes in n-type beta-SiC, are scattered by these defects, and the response time (τ_r) of minority carriers increased. Furthermore, the bandgap of beta-SiC is 2.2 eV, which results in the very low intrinsic carrier concentration(n_i) of 5.6 cm^{-3}. Because of this low n_i, the minority carrier concentration becomes very low, and τ_r becomes extremely long. With the very low minority density and high defect density in the crystal, the minority carriers are not able to generate near the oxide-semiconductor interface fast enough; hence, deep depletion phenomena were observed in the past.

The second oxidation was performed after removal of the Al metal contact pads and oxide. Inversion was obtained in the MOS capacitors after the second oxidations. The sample's surface, after the first oxidation, contained considerable damage because of the 0.1um diamond paste polishing. However, before the second oxidation, the damaged surface was removed, and the second oxide was able to grow on a low defect single crystal epi-layer. With the low defect density beta-SiC layer, the minority carries were able to effectively generate near the oxide-semiconductor interface, and the C-V results showed inversion in dark. Previous attempts at obtaining inversion in the absence of light by Kee et al.[4] and Shibahara et al.[3] were unsuccessful. The quality of beta-SiC crystal surface appears to be the key factor.

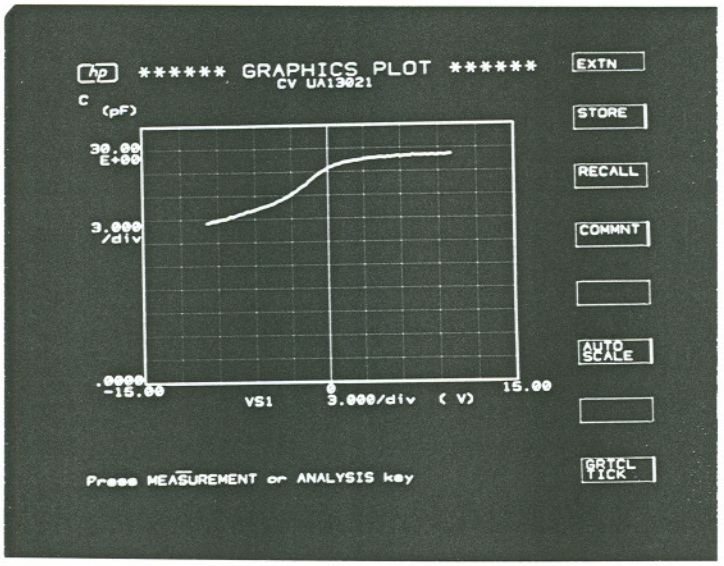


Figure 4.6 1 MHz C-V measurement of undoped beta-SiC after first oxidation. (See figure 4.16 for detail parameters.) The scan rate was 0.8 V/sec.

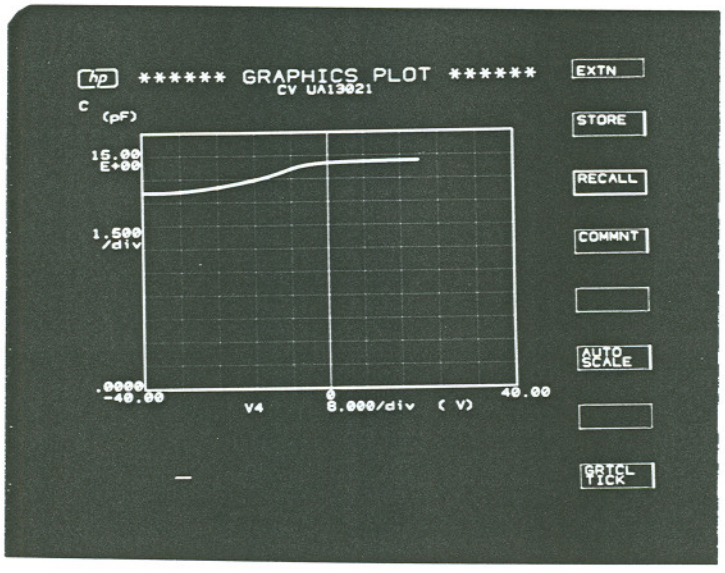


Figure 4.7 1 MHz C-V measurement of undoped beta-SiC after second oxidation. The scan rate was 0.8 V/sec.

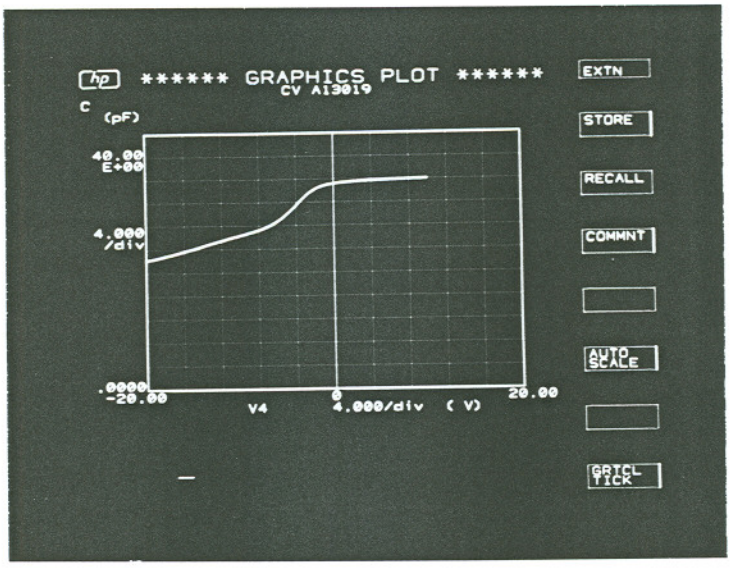


Figure 4.8 1 MHz C-V measurement of $4.2*10^{-3}$ sccm Al-doped beta-SiC after first oxidation. The scan rate was 0.8 V/sec. (See figure 4.17 for detail parameters.)

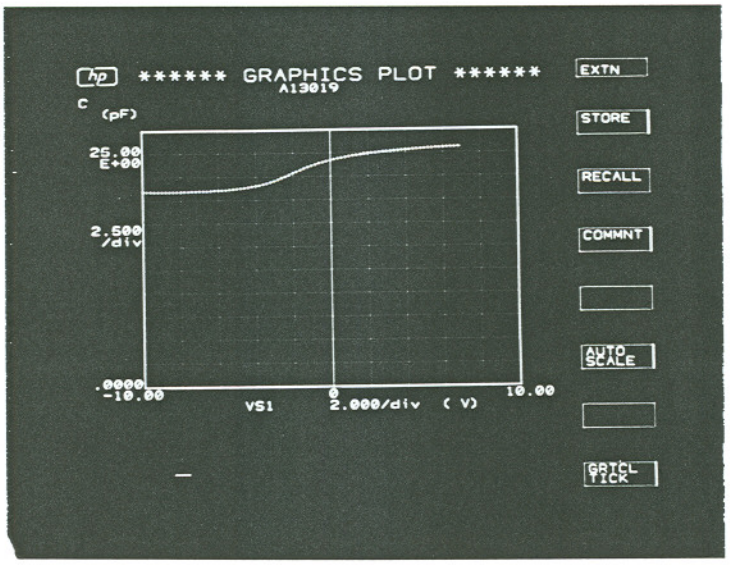


Figure 4.9 1 MHz C-V measurement of $4.2*10^{-3}$ sccm Al-doped beta-SiC after second oxidation. The scan rate was 0.8 V/sec.

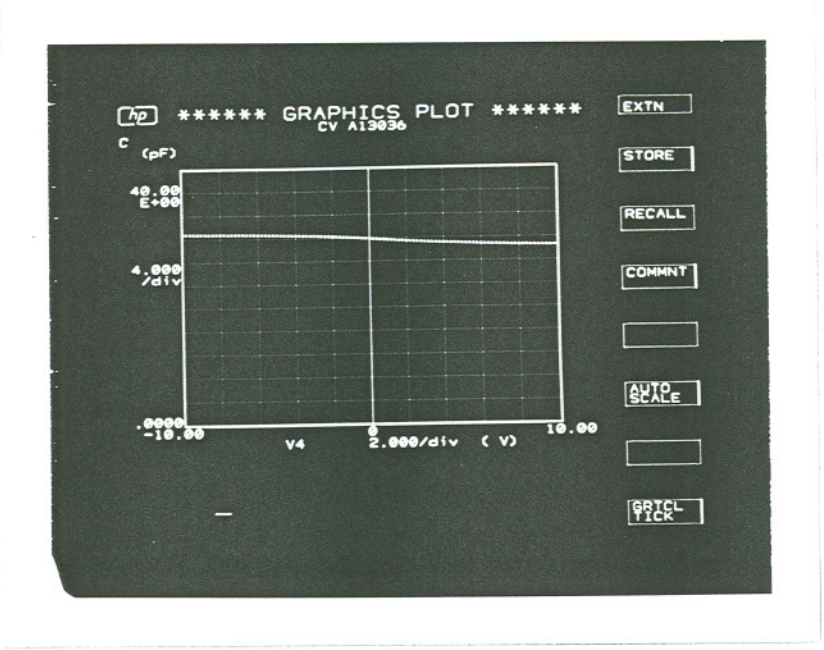


Figure 4.10 1 MHz C-V measurement of 0.21 sccm Al-doped beta-SiC after second oxidation. The scan rate was 0.8 V/sec. (See figure 4.18 for detail parameters)

In spite of the fact that inversion of beta-SiC MOS capacitors in dark was not obtained in the past, inversion mode n-channel beta-SiC MOSFETs were fabricated. The inversion characteristic of these beta-SiC MOSFETs was explained as the injection of electrons from source and drain[5]. However, because of the delay of electron injection, the electron mobility calculated from the I-V results of these MOSFETs[6] was in the low 100 $cm^2/(V.sec)$ range. In contrast, the inversion of MOS capacitors in our beta-SiC epi-layers shows that our synthesis technique gives lower defect density beta-SiC epi-layers than other approaches. With a better quality beta-SiC crystal, a n-channel beta-SiC MOSFET with high electron mobility may be seen in the future.

4.3.3b Deep depletion

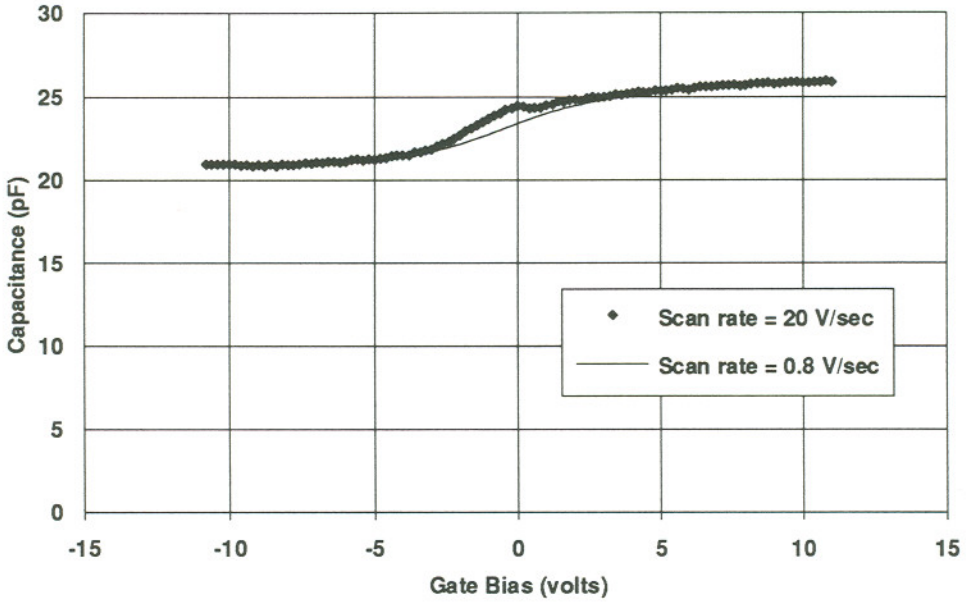


Figure 4.11 Capacitance as a function of gate bias on the $4.176*10^{-3}$ sccm Al-doped sample having a concentration of $1.3*10^{18}$ cm^{-3} and an oxide thickness of 380Å. The high frequency C-V measurement with a scan rate of 20 V/sec was measured at 1 MHz by manually changing gate bias.

The deep depletion of beta-SiC MOS capacitors was attempted using the same setup as the inversion measurement except the sweep rate of the gate bias was from 10 to 20 V/sec. A typical C-V result is shown in figure 4.11. No deep depletion phenomenon was observed in any of the three doping concentrations. This result was also verified by biasing the sample from -10 V to 10 V within 0.5 sec and measuring the capacitance for 30 min.; a typical result of this measurement is shown in figure 4.12. The total capacitance change within 30 min. was less than 1%, which is within the noise level of the measuring system. A

possible explanation of the absence of deep depletion on the beta-SiC MOS capacitors is the tunneling of minority carriers in the high dopant concentration beta-SiC.

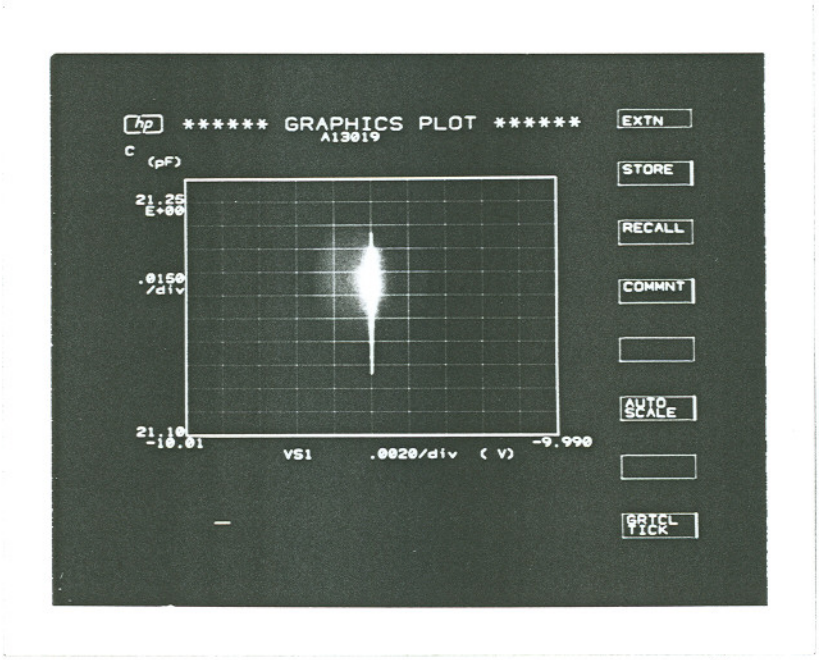


Figure 4.12 Capacitance as a function of time on $4.2*10^{-3}$ sccm Al-doped sample. The gate bias was manually changed from -10 V to 10 V within 0.5 sec. The capacitance was measured every 10 sec. for 30 min. at 10 V.

A review of the deep depletion theory states; "When gate bias of a MOS capacitor is changed too rapidly for thermal generation of minority carriers, the minority carriers cannot maintain the charge neutrality of the MOS capacitor. Instead, the charge neutrality is maintained by an increase in depletion layer charge and, therefore, in depletion layer width. The depletion layer width continues to increase with gate bias until the onset of oxide breakdown or

additional generation of minority carriers.[7]" All of the tested samples had carrier concentration of about 10^{18} cm^{-3}. It is very possible that tunneling occurred before the deep depletion in the C-V measurements because of the high doping concentrations. In another words, the tunneling of electrons or holes in the beta-SiC became the other source of minority carriers; therefore, the deep depletion of beta-SiC MOS capacitors was not observed.

A classical way to calculate the probability of tunneling is by assuming carriers tunneling through a triangle barrier, figure 4.13. The height of the energy barrier E_B decreases linearly from Eg at x=0 to 0 at L, where Eg is the bandgap of semiconductor.

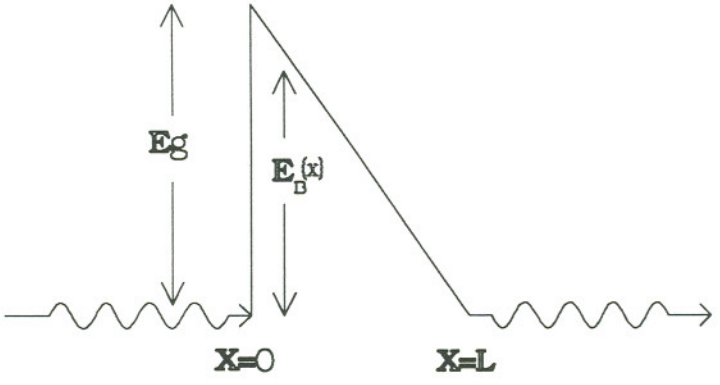


Figure 4.13 The probability of tunneling can be approximated by considering tunneling through a triangular barrier.

By using the Wentzel-Kramers-Brillouin (WKB) approximation[8], the probability of tunneling (Θ) can be approximated by using the barrier height in the equation

$$\Theta \approx \exp(-2\int_0^L \sqrt{\frac{2m^* E_B(X)}{h^2}}dx) \tag{4.2}$$

where $E_B(x)$ is the barrier height at position X, m^* is the effective mass of carrier and h is the Planck's constant. Carry out the integration,

$$\Theta = \exp(-P_e), \tag{4.3}$$

where

$$P_e = \frac{4\sqrt{2m^* E_g^{1/2}}L}{3h}. \tag{4.4}$$

The well known tunneling in Si MOS capacitors starts at about 10^{18} cm^{-3}[9]. By using the electron effective mass (0.6) and bandgap (2.2 eV) of beta-SiC, the P_e ratio between beta-SiC and Si is 1.1. This simple approximation suggests that the tunneling in beta-SiC MOS capacitors happens at roughly the same carrier concentration as in Si MOS capacitors. This deduction agrees with the C-V measurement of beta-SiC MOS capacitors where deep depletion was not observed because of the high carrier concentrations (about 10^{18} cm^{-3}) in beta-SiC layers.

4.4 Modeling of Beta-SiC MOS Capacitor

The Model for MOS capacitors is well developed, tested on Si MOS capacitors[13], and is in a generalized form, which can be used in any semiconductor material. Although beta-SiC possesses many properties different from Si, it is important to test this model on beta-SiC MOS capacitors; this

information can then be used in the future for modifying the high frequency C-V model of beta-SiC MOS capacitors (if needed). Furthermore, by modeling MOS capacitor, many oxide properties can be obtained. Therefore, the oxide thickness, dopant concentration, and flat band capacitance, which are necessary for modeling of MOS capacitors, are calculated according to the C-V measurement of MOS capacitors in section 4.4.1. A high frequency C-V Model is discussed in section 4.4.2 (figure 4.16a, figure 4.17a and fig 4.18a). Total oxide charge and interface trap density are derived in section 4.4.3. Important properties and constants used in the calculation and modeling of beta-SiC MOS capacitors are listed in Table 4.2. Table 4.3 summarizes the results of the modeling and calculation for all three different conditions of beta-SiC MOS capacitors.

Table 4.2 Important physical constants used for modeling beta-SiC MOS capacitors

Description	Value	Reference
Planck's constant (h)	$4.135*10^{-15}$ eV s	
Boltzmann's constant (k)	$8.62*10^{-5}$ eV K^{-1}	
Elementary charge (q)	$1.602*10^{-19}$ C	
Oxide dielectric constant (ε_{ox})	3.8	section 4.3.2
Al vacuum work function (Φ_m)	4.2 eV	
Beta-SiC		
Dielectric constant (ε_s)	9.7	[18]
Energy gap at 300 °K (E_g)	2.2 eV	[19]
Intrinsic carrier concentration (n_i)	5.6 cm^{-3}	section 4.4.1a
effective mass m^*/m_o		
electrons (m_n^*)	0.6	*
holes (m_p^*)	1.0	*

* not measured in beta-SiC; 6H-SiC values used.

4.4.1 Parameters for Modeling beta-SiC MOS capacitors

4.4.1a Intrinsic carrier concentration in beta-SiC

The intrinsic carrier concentration (n_i) in beta-SiC is very important for calculation of all basic parameters of beta-SiC; however, it has not been accurately measured. Nevertheless, n_i can be estimated by the following equations[10]:

$$N_c = 2M_c\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2}, \tag{4.5}$$

$$N_v = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2} \text{ and} \tag{4.6}$$

$$n_i = \sqrt{N_c N_v}\exp\left(\frac{-E_g}{kT}\right) \tag{4.7}$$

where N_C and N_V are the effective densities of states at the conduction- and valence-band edges, respectively, m_n^* and m_p^* denote the effective masses of electrons and holes, M_C is the number of equivalent minima in the conduction band, and k, T and h are the Boltzmann's constant, temperature and Planck's constant, respectively. Because the effective masses of electrons and holes in beta-SiC have not been measured accurately, the effective masses in 6H alpha SiC (0.6 for electrons and 1.0 for holes) were used for the approximate calculation, and M_C=1 was used for approximation. The above equations result in $N_C \sim 1.16*10^{19}$ cm^{-3}, $N_V \sim 2.5*^{18}$ cm^{-3}, and $n_i \sim 5.6$ cm^{-3} for beta-SiC.

4.4.1b Oxide thickness

The dielectric constant of thermal oxide on beta-SiC was determined to be 3.8. Using equation 4.1, the thickness of oxide was calculated. The results are listed in table 4.3.

Table 4.3 Properties of beta-SiC MOS Capacitor

Sample	Beta-SiC MOS Capacitor		
Property	undoped	$4.2*10^{-3}$ Al doped	0.21 Al doped
Oxide Thickness t_{ox} (Å)	720	380	590
Flat Band Capacitor C_{FB} (pF)	14.4	25.0	32.3
Flat Band Voltage V_{FB} (Volts)	-3.9	2.3	-5.6
Dopant Concentration N (cm^{-3})	$1.6*10^{18}$	$1.3*10^{18}$	$3 - 9*10^{18}$
Total Charge Density N_{ff} (cm^{-2})	$1.1*10^{12}$	$-1.4*10^{12}$	$1.3*10^{12}$
Minimum Interface Trap Density D_{it} ($cm^{-2}eV^{-1}$)	$2*10^{11}$	$1.4*10^{12}$	*

* negative value.

4.4.1c Average doping concentration

The maximum-minimum capacitance method, equation 4.8, was used to estimate average doping concentration in the depletion layer of n-type MOS

capacitors.

$$\frac{N_d}{\ln(N_d/n_i)+\frac{1}{2}\ln[\ln(N_d/n_i)-1]} = \frac{4kT\varepsilon_{ox}^2}{q^2\varepsilon_s t_{ox}^2}\left(\frac{C_{ox}}{C_{HF}(\min)}-1\right)^2 \quad (4.8)$$

where N_d is the donor concentration, ε_s is the permittivity of the semiconductor, C_{ox} ($=C_{max}$) is the oxide capacitance, and $C_{HF}(min)$ is the minimum capacitance from the high frequency C-V measurement. For p-type MOS capacitors, N_a instead of N_d was used. This equation originated with Van Gelder and Nicollian[11,12]. Because of the complexity of this equation, iteration was used to calculate the average doping concentration. The doping concentration was also obtained from a calculated chart (figure 4.14), which is derived from equation 4.8. The results are listed in table 4.3.

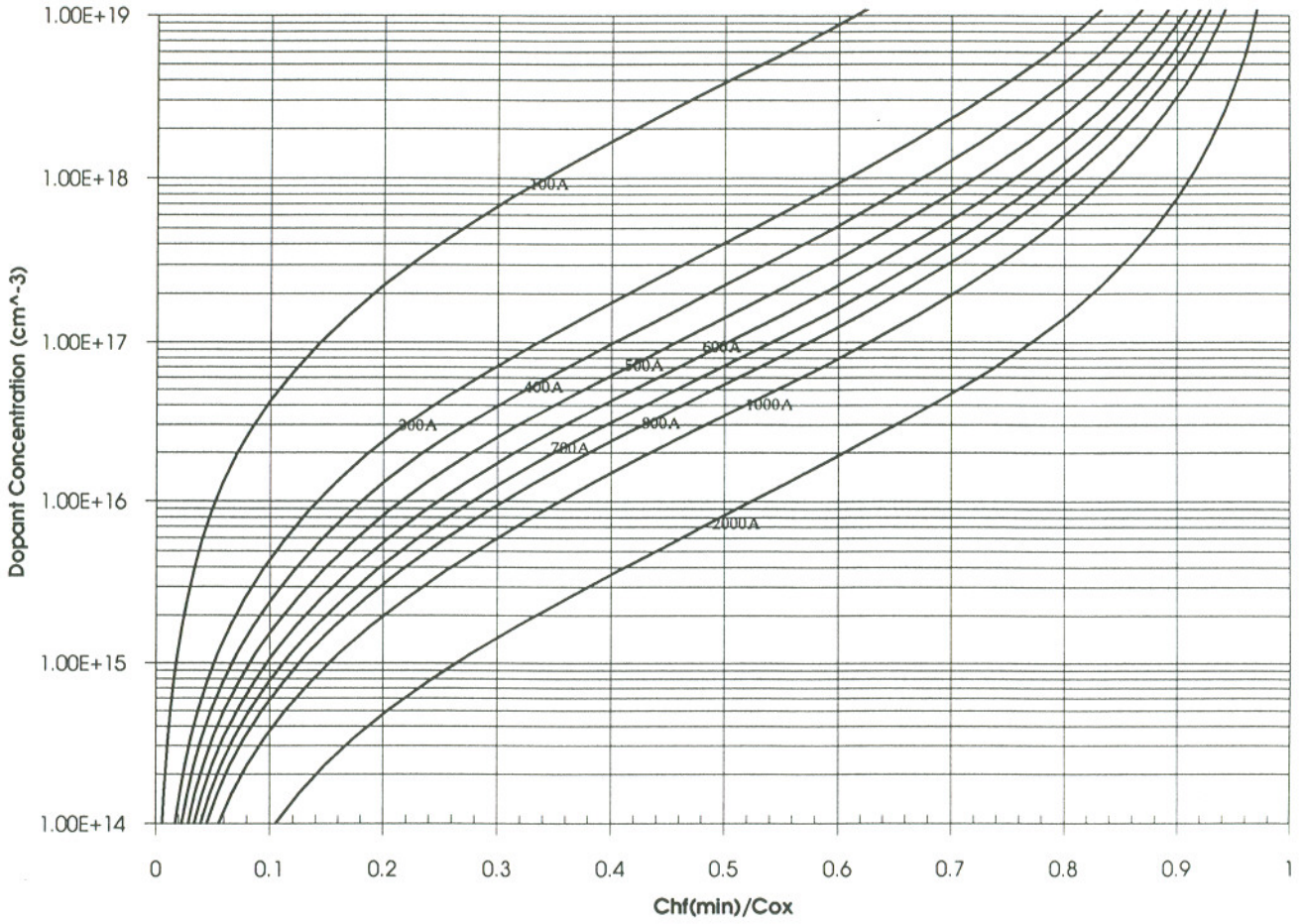


Figure 4.14 Doping concentration versus $C_{HF}(min)/C_{ox}$ with oxide thickness as parameter for beta-SiC.

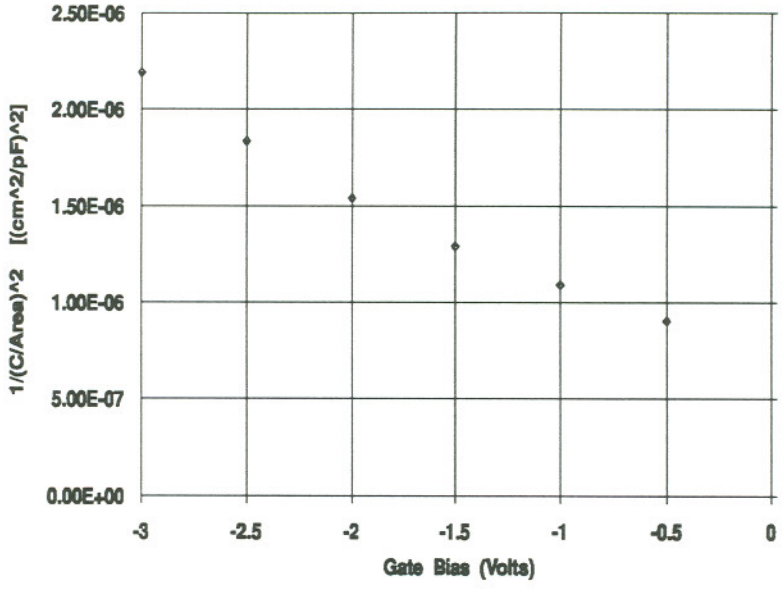


Figure 4.15 Plot of $1/C^2$ as a function of bias of an Ag Schottky diode on undoped beta-SiC. The diode's radius was 97.4 um.

The doping concentration calculated by this method was verified by C-V measurement of silver (Ag) Schottky diodes on undoped samples, figure 4.15; the measurement shows that its doping concentration is around $7*10^{17}$ cm^{-3}, which agrees with the MOS capacitor result ($1.6*10^{18}$ cm^{-3}) within an order of magnitude. Schottky diodes were also fabricated on beta-SiC epi-layers with other doping concentrations; however, because of leakage current, the concentrations could not be determined from the C-V measurements of these Schottky diodes. We also noticed that the breakdown voltages of back-to-back tungsten carbide (WC) diodes, obtained by probing WC probes on the epi-layers directly, were less than 5 volts on all three samples. A rough estimate by using

breakdown voltage for one-side abrupt junctions[13],

$$V_B \cong 60(\frac{E_g}{1.1})^{3/2}(\frac{N_B}{10^{16}})^{-3/4}, \quad (4.9)$$

where N_B is the background concentration in cm^{-3}, also indicates that the carrier concentrations in all three samples are about 10^{18} cm^{-3}.

4.4.1d Flat band capacitance and voltage

Flat band capacitance was calculated by the following three equations.

Debye length (λ_p):

$$\lambda_p = \sqrt{\frac{\varepsilon_s kT}{q^2 N_a}}. \quad (4.10)$$

For n-type MOS capacitor, N_d instead of N_a was used.

Flat band capacitance (C_{FBS}) in the depletion layer:

$$C_{FBS} = \frac{\varepsilon_s}{\lambda_p}. \quad (4.11)$$

Total high frequency flat band capacitance, which is the sum of oxide capacitance and flat band capacitor in depletion layer:

$$C_{FB} = \frac{C_{FBS}C_{ox}}{(C_{FBS} + C_{ox})}. \quad (4.12)$$

The calculated results are listed in Table 4.3.

4.4.2 High frequency C-V model

The measured high frequency capacitance $C(V_G)$ is a series combination of the oxide capacitance C_{ox} and the semiconductor surface capacitance C_S:

$$C = \frac{C_s C_{ox}}{C_s + C_{ox}}. \tag{4.13}$$

A generalized model[14] for all semiconductor materials was used to model the high frequency C-V measurement of beta-SiC MOS capacitors. The result of this model shows the semiconductor surface capacitance is

$$C_s = 2C_{FBS}\{1 - e^{-v_{so}} + (\frac{n_i}{N_a})^2[(e^{v_{so}} - 1)\frac{\Delta}{\Delta + 1} + 1]\}F^{-1}(v_{so}, u_B) \tag{4.14}$$

where

$$\Delta \approx \frac{F(v_{so}, u_B)}{e^{v_{so}} - 1}[\int_0^{v_{so}} \frac{e^{v_s} - e^{-v_s} - 2v_s}{F^3(v_s, u_B)} dv_s - 1] \text{ and} \tag{4.15}$$

$$F_S(v_s, u_B) = 2^{1/2}\{(u_B - v_s)\sinh(u_B) - [\cosh(u_B) - \cosh(v_s)]\}^{1/2}. \tag{4.16}$$

u_B and v_S are defined by

$$u_B = \ln(N_a / n_i) \text{ and} \tag{4.17}$$

$$v_s = -\frac{q\psi_s}{kT} = v_{so} + \delta v_s, \tag{4.18}$$

where v_{SO} is the normalized band bending set by gate bias, δv_S is the normalized small signal ac band bending set by the measuring capacitance meter, and ψ_S [v_S] is the [normalized] total band bending set by the gate bias and the capacitance meter at the oxide/semiconductor interface. Since v_{SO} is less than $2u_B$ at gate bias

between 40 and -40 V for all three beta-SiC MOS capacitors, C_S can be further simplified to

$$C_s = 2^{-1/2} Sgn(v_{so}) C_{FBS}(1-e^{-v_{so}})[(v_{so}-1)+e^{-v_{so}}]^{-1/2} \quad (4.19)$$

for p-type or

$$C_s = 2^{-1/2} Sgn(v_{so}) C_{FBS}(e^{v_{so}}-1)[-(v_{so}+1)+e^{v_{so}}]^{-1/2} \quad (4.20)$$

for n-type, where $Sgn(v_{SO})$ denotes the sign of v_{SO}; i.e., $Sgn(v_{SO})$ is 1 if $v_{SO} > 0$ and -1 if $v_{SO} < 0$. The result suggests that the simplified C_S is independent from the ac bias set by the capacitance meter and is a function of v_{SO}. Now, the problem is determining the relation between V_{SO} and V_G.

The gate bias at every corresponding v_{SO} can be calculated from the surface charge $Q_S(\psi_S)$. The surface charge (per unit area)[15] at the semiconductor-oxide interface of a MOS capacitor is

$$Q_s = -Sgn(\psi_s)\frac{\sqrt{2}\varepsilon_s kT}{q\lambda_p} F(\beta\psi_s, \frac{n_{po}}{p_{po}}), \quad (4.21)$$

where

$$F(\beta\psi_s, \frac{n_{po}}{p_{po}}) = [(e^{-\beta\psi_s} + \beta\psi_s - 1) + \frac{n_{po}}{p_{po}}(e^{\beta\psi_s} - \beta\psi_s - 1)]^{1/2}, \quad (4.22a)$$

and $$\beta = \frac{q}{kT}. \quad (4.22b)$$

Q_S is positive when $\psi_S < 0$ and negative when $\psi_S > 0$. Now that we know the relation between Q_S and ψ_S, the corresponding gate bias at this band bending can be calculated from the sum of the voltage drop across the oxide and total band bending at the interface:

$$V_G = -\frac{Q_s(\psi_s)}{C_{ox}} + \psi_s . \tag{4.23}$$

Therefore, in this thesis the measured high frequency capacitance $C(v_{SO})$ was calculated by equations 4.19 (or 4.20), 4.13 and 4.1. The gate bias V_G at the corresponding v_{SO} was calculated by using equations 4.21, 4.22, 4.23 and 4.18. The modeling results are shown in figures 4.16a, 4.17a and 4.18a.

The C-V model, which was developed for Si, was found to be very suitable for modeling the undoped and the lightly Al-doped beta-SiC MOS capacitors. However, the heavily compensated Al doped sample had a C-V characteristic very different from the ideal case. This could be due to the high doping concentration, which increases the defect density. Defects affect the interface state density, and thereby the characteristics of MOS capacitors.

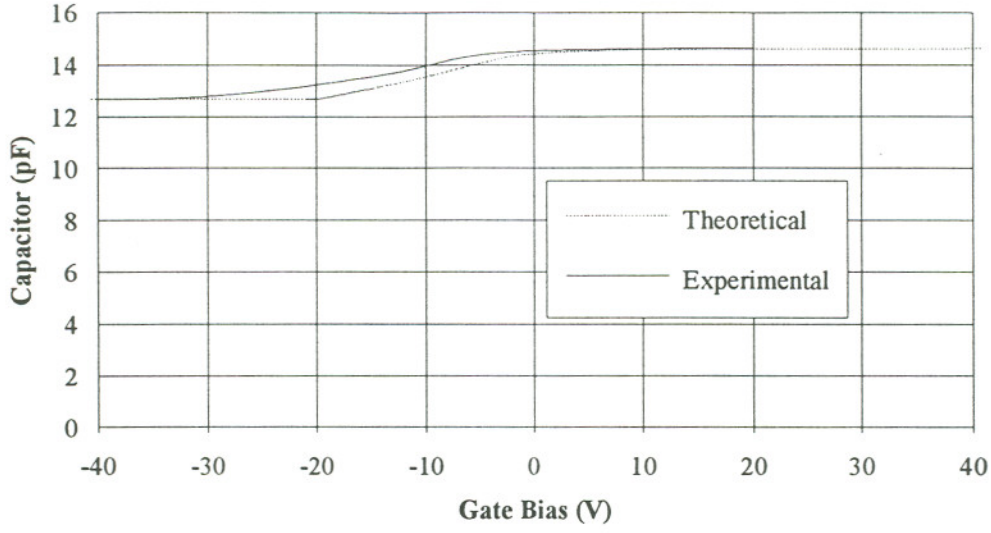


Figure 4.16a High frequency C-V measurement of the undoped beta-SiC MOS capacitor. The solid line is capacitance values measured at 1MHz on the undoped beta-SiC on TiC_x substrate, with a donor concentration of $1.6*10^{18}$ cm^{-3}, an oxide capacitance of 14.6pF, and a gate diameter of 100um.

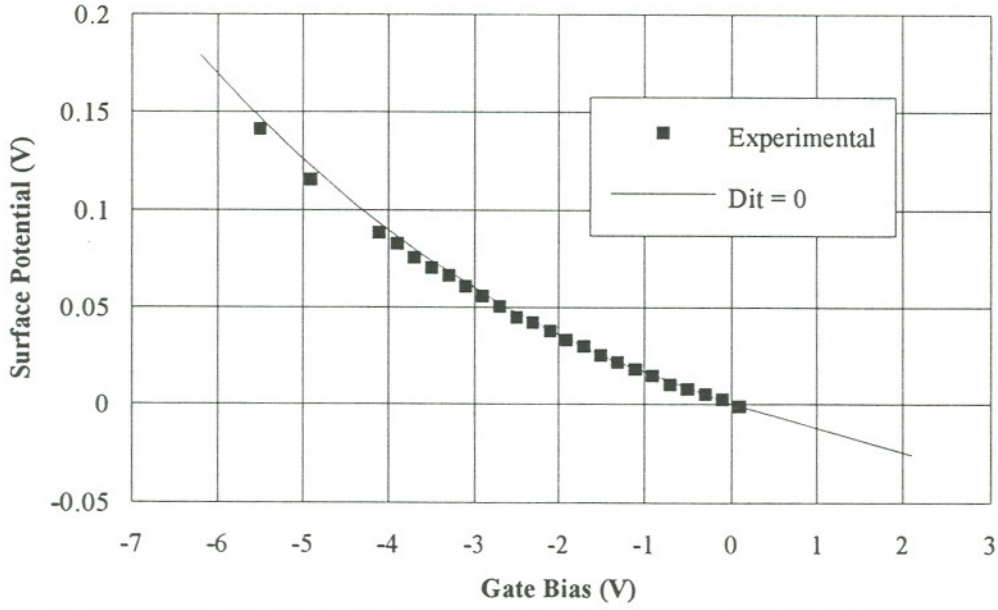


Figure 4.16b Plot of surface potential (Ψ_S) versus gate bias (V_G) for the sample in figure 4.16a. Note that the experimental results have been adjusted according to the flat band voltage for clarity. Minimum interface trap density of this sample is $2*10^{11}cm^{-2}eV^{-1}$.

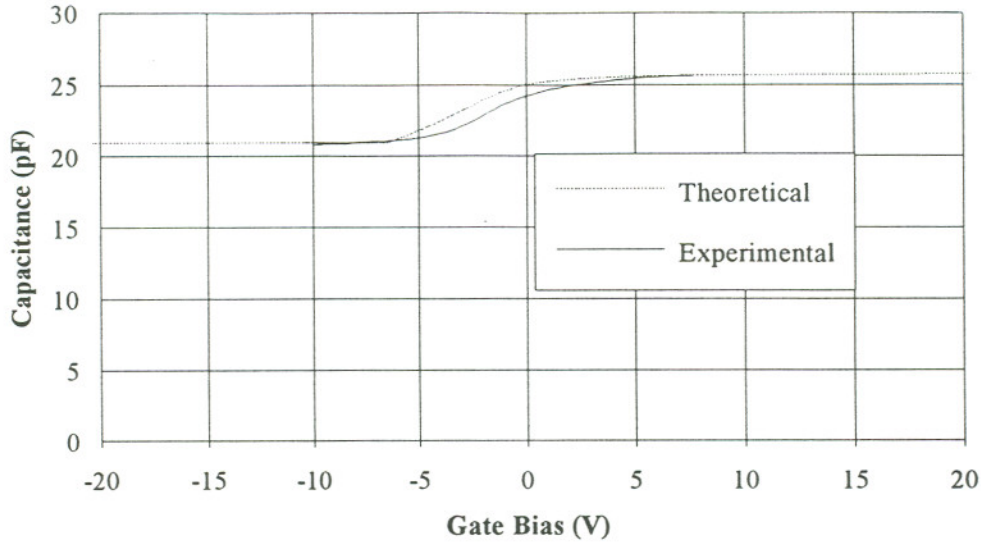


Figure 4.17a High frequency C-V measurement of the $4.2*10^{-3}$ sccm Al-doped beta-SiC MOS capacitor. The solid line is capacitance values measured at 1MHz on the Al doped beta-SiC on TiC_x substrate, with a donor concentration of $1.3*10^{18}$ cm^{-3}, an oxide capacitance of 24.9pF, and a gate diameter of 94um.

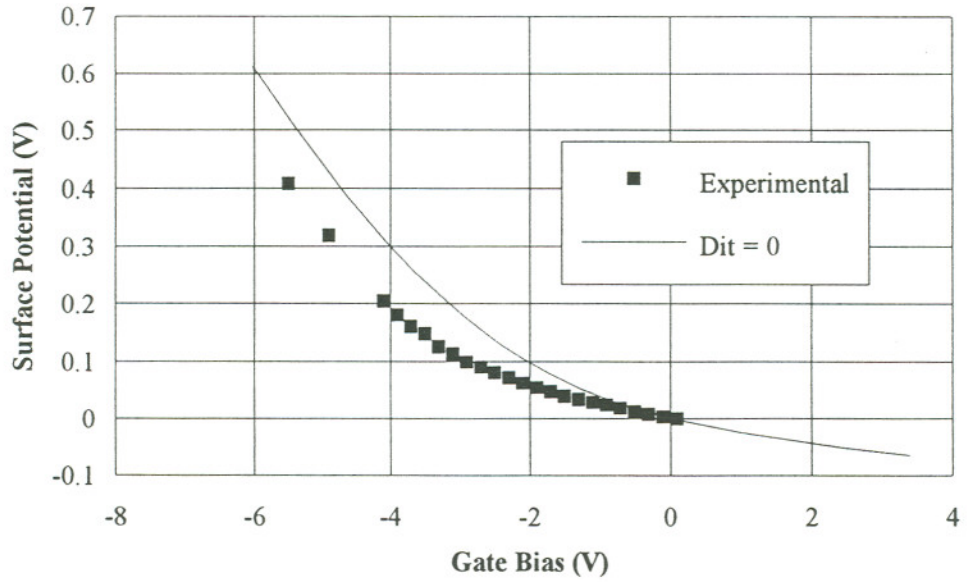


Figure 4.17b Plot of surface potential (Ψ_S) versus gate bias (V_G) for the sample in figure 4.17a. Note that the experimental results have been adjusted according to the flat band voltage for clarity. Minimum interface trap density of this sample is $1.4*10^{12}cm^{-2}eV^{-1}$.

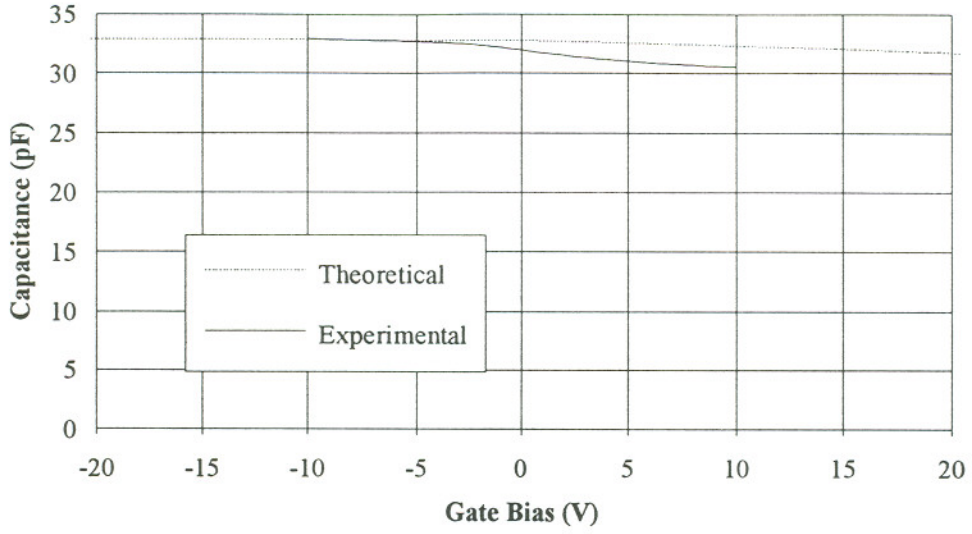


Figure 4.18a High frequency C-V measurement of the 0.21 sccm Al-doped beta-SiC MOS capacitor. The solid line is capacitance values measured at 1MHz on the Al-doped beta-SiC on TiC_x substrate, with an oxide capacitance of 30.3 pF, and a gate diameter of 94 um. The theoretical curve was calculated for dopant concentration $9*10^{18}$ cm^{-3}. The experimental values do not fit into the model.

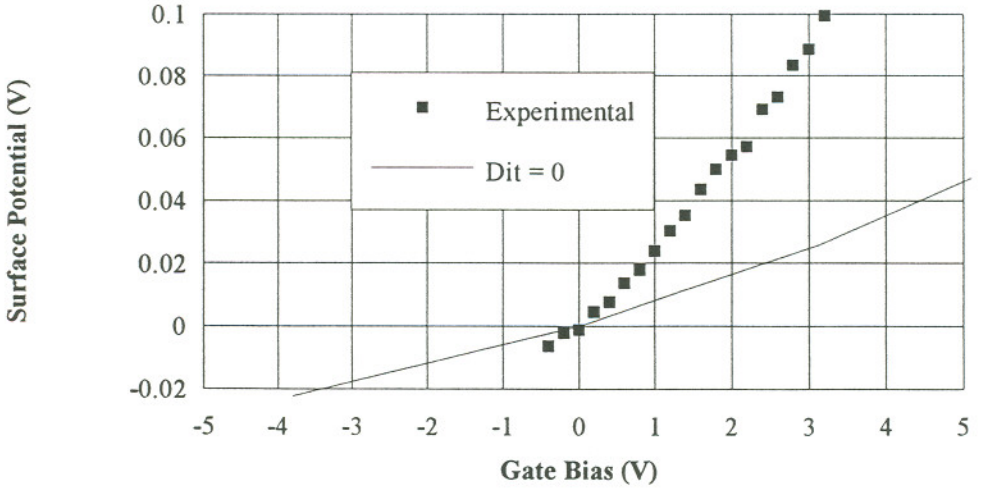


Figure 4.18b Plot of surface potential (Ψ_S) versus gate bias (V_G) for the sample in figure 4.18a. The experimental results have been adjusted according to the flat band voltage for clarity.

4.4.3 Charges in beta-SiC MOS Capacitors

4.4.3a Total charge density (N_{to})

Total charge density was calculated by the following equations:

$$N_{to} = C_{ox}(\Phi_{ms} - V_{FB}) \tag{4.24}$$

For p-type doping,

$$\Phi ms = \Phi m - (\chi + \frac{Eg}{2q} + |\phi_p|) \tag{4.25}$$

$$\text{where } \phi_p = \frac{-kT}{q} \ln(N_a / n_i). \tag{4.26}$$

For n-type doping,

$$\Phi ms = \Phi m - (\chi + \frac{Eg}{2q} - |\phi_n|) \tag{4.27}$$

$$\text{where } \phi_n = \frac{kT}{q} \ln(N_d / n_i). \tag{4.28}$$

In above equations, χ is the electron affinity of beta-SiC, Eg is the band gap of beta-SiC, and Φm is the vacuum work function for the gate metal (Al). χ = 4.0 V was used for approximation. The calculated results are listed in table 4.3. As expected, the undoped sample had a smaller total charge density than the Al doped samples.

4.4.3b Interface trap density (D_{it})

Since the undoped and lightly Al doped beta-SiC MOS capacitors fit the

high frequency C-V model very well, the Terman method[16] was used to estimate the oxide/semiconductor interface trap density (D_{it}). The Terman method uses the fact that the interface traps in a MOS capacitor do not respond to the small signal ac bias set by the capacitance meter; however, they do follow the slowly changing gate bias. This characteristic of interface traps results in a stretch-out along the gate bias axis of high frequency C-V curve of a MOS capacitor. By using this stretch-out, interface trap density can be calculated.

Plots of surface potential vs. gate bias were constructed in figures 4.16b, 4.17b and 4.18b by the Terman method. D_{it} was then determined from

$$D_{it} = \frac{1}{q}\{[(\frac{d\psi_s}{dV_G})^{-1} - 1] - C_s(\psi_s)\}. \qquad (4.29)$$

The calculated results of D_{it} are listed in table 4.3. The undoped sample had the lowest interface trap density, as expected. On the other hand, the surface potential vs. gate bias plot of the heavily Al-doped sample gave a negative D_{it}, which is undefined in the Terman method. This is because the C-V result of this highly compensated sample couldn't be fit into the C-V model; that is, the capacitor is not an ideal capacitor because of its high defect density. These results indicate that a low background concentration in the beta-SiC epi-layer is necessary for the best oxide quality.

4.5 SUMMARY

In this chapter, the fabrication procedures of both n-type and p-type beta-SiC MOS capacitors were described. The dielectric constant of oxides on beta-

SiC was found to be about 3.8. The C-V measurements of these capacitors were discussed. Inversion of beta-SiC MOS capacitors in dark was obtained for the first time. Deep depletion in these beta-SiC MOS capacitors, whose carrier concentrations were about 10^{18} cm^{-3}, was found to be impossible because of the tunneling effect. Modeling of the high frequency C-V curve was discussed; the generalized model was found to be quite adequate for beta-SiC MOS capacitors. Finally, interface charge and trap density conclude that oxide on the undoped n-type beta-SiC epi-layer has the best quality.

CHAPTER 5

N-CHANNEL BETA-SIC MOSFET FABRICATION AND RESULTS

5.1 INTRODUCTION

The fabrication procedure and parameters of beta-SiC MOSFETs discussed here are not optimized. However, it is important to show the possibility of fabricating MOSFETs using current available technology on this material. Later, beta-SiC MOSFETs may be optimized based on this experience. Basic components of beta-SiC are discussed in section 5.2. A novel beta-SiC MOSFET fabrication process is discussed in section 5.3, in which an in-situ doping technique during the CVD growth was used, and a TiC_x "lift-off" layer was used to define the source and drain. Processing results for these beta-SiC MOSFETs are discussed in section 5.4. Finally, section 5.5 summarizes the device fabrication results.

5.2 BASIC COMPONENTS

Properties of an MOSFET's components affect its characteristics. The following sections discussed the basic components of a beta-SiC MOSFET, which were investigated before fabrication.

5.2.1 Buffer layer

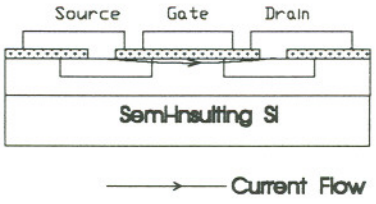


Figure 5.1 Current flow in a Si MOSFET on a semi-insulting Si substrate. The current flow is limited to the channel.

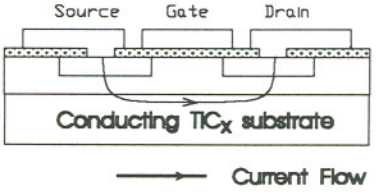


Figure 5.2 Current flow in a beta-SiC MOSFET on a conducting TiC_x substrate. The current flow passes through the conducting substrate.

A common MOSFET structure uses rectifying p-n junctions or a semi-insulating substrate, figure 5.1, to isolate the device from the substrate. The rectifying property of a p-n junction or the high substrate resistivity causes the current injected from the source or drain to be limited to the channel, where the gate voltage can bias and modulate the charges. On the other hand, if we consider a lateral structure beta-SiC MOSFET in a 5 um thick beta-SiC epi-layer, which is directly grown on a conducting TiC_x substrate (and without a buffer layer), a deduction from the simple Ohm's law states that the current flowing from the source or drain passes through the channel only if the channel length is less than 5

um. Otherwise, the current travels from the source or drain to the conducting substrate and, then, from the substrate to the drain or source; see figure 5.2. In the latter case, the current does not pass through the channel, where the bias voltage can control it. Therefore, the gate bias cannot modulate the current, and the MOSFET fails. Attempts to use rectifying p-n junctions for isolation did not succeed because the beta-SiC p-n junctions have been very leaky; see section 5.4.1. Three solutions to this problem are:

(a) grow a beta-SiC epi-layer thicker than the MOSFET channel length.

(b) decouple the beta-SiC epi-layer totally from the substrate.

(c) find a semi-insulating buffer layer.

Approach (a) is very difficult to achieve because the present growth rate of beta-SiC is about 5 um per hour. For a very long channel device, this would require more than one day to grow the layers; besides, we are presently not able to grow beta-SiC epi-layers for such long periods.

Attempts to decouple beta-SiC epi-layers from TiC_X substrates used either oxidation or TiC_X etching solution to remove the TiC_X substrates. In the oxidation approach, the substrates were polished down to a thickness of about 25 um from the TiC_X side of the sample. Then the TiC_X substrates were transformed into TiO_X, by 1100 °C wet oxidation. The beta-SiC epi-layer did not adhere to the TiC_X, and we were able to remove the beta-SiC epi-layer. In the TiC_X etching approach, the same thinning procedure was used to reduce the total etching time,

and the samples were etched at 50°C in TiC_x etching solution for 10 hours. The TiC_x etching solution consumed the entire TiC_x substrate so that only the beta-SiC layers remained in the solution. However, in both approaches, the epi-layers cracked into small pieces having sizes less than 0.5 mm^2. This was due to the difference in thermal expansion coefficients of beta-SiC and TiC_x. This approach should be tried in the future when thick (>100 um) beta-SiC layers are available because the strength resulting from thick epi-layers may prevent the beta-SiC layers from cracking.

Approach (c) was quite appropriate for the present technology. The semi-insulating buffer was realized by boron (B) compensation doping to electrically isolate undoped and Al-doped beta-SiC epi-layers from the conductive TiC_x substrates. The growth procedure for the B-doped buffer isolation layer is described in chapter 3.

To identify the optimal boron flow rate for the buffer layer, B-doped layers, about 3.3um thick, at several different flow rates of B_2H_6 were grown. Their breakdown voltages were measured by 1.2 um (in diameter) WC probes, which formed back-to-back Schottky diodes. The breakdown voltage of the Schottky diode indicates the degree of compensation; that is, the ideal buffer layer should have the lowest doping concentration and, therefore, the highest breakdown voltage. The 45 sccm B_2H_6 doped beta-SiC epi-layer had the highest breakdown voltage of 450 V. The buffer isolation layers were therefore doped at this flow rate.

Transmission line measurements were used to characterize the buffer

isolation layers. To perform transmission line measurement, an undoped or Al-doped beta-SiC epi-layer was grown on top of the buffer isolation layer, followed by evaporation of Al onto the epi-layers. The Al transmission line patterns (TLP), figure 5.3, were patterned on top of the undoped or Al-doped layers and annealed in Ar at 500 °C for 1 min. in an RTA furnace.

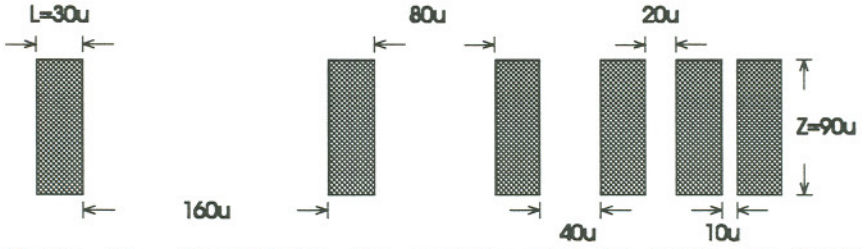


Figure 5.3 Transmission line patterns used for MPD and TLM measurements.

Current-voltage measurements were performed at different pad distances. From a plot of resistance (V/I) vs. pad distance, we obtained for each sample the maximum penetration distance (MPD). The MPD is the maximum lateral distance a current can travel through the device before shorting through the conducting substrate. Figure 5.4 illustrates this method.

In figure 5.4a, all currents pass through the conducting substrate before reaching another pad. Since the currents in all three cases travel through almost the same distance in the beta-SiC, which has much higher resistivity than the TiC_X substrate, the measured resistance (V/I) will also be similar. Therefore, the resistance vs. pad distance plot shows very little increase; see the inserted curve in figure 5.4a.

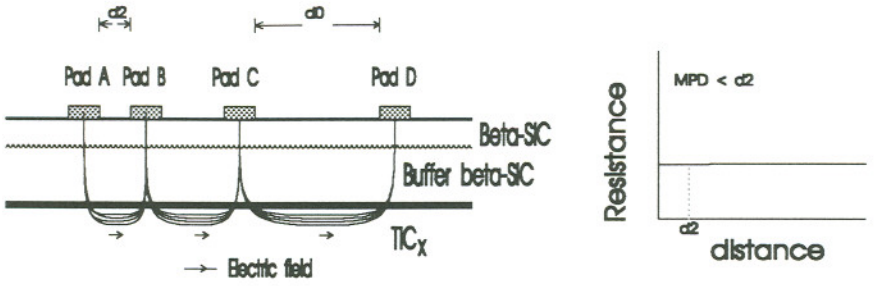


Figure 5.4a Sample with an MPD less than d2

In figure 5.4b, all currents are confined inside the layer; also note that the currents are limited in beta-SiC not in the buffer SiC because the buffer SiC has much higher resistivity. Since the current measured at longer pad distance travels longer distance in the beta-SiC, the resistance vs. pad distance plot shows a linear increase.

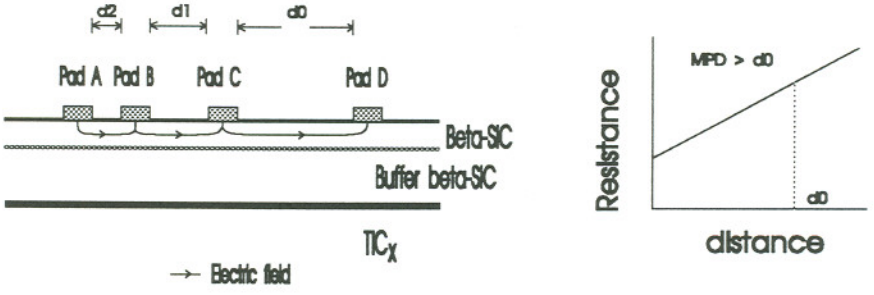


Figure 5.4b Sample with an MPD larger than d0. Note that only the major electric field is shown in figure 5.4b and 5.4c.

In figure 5.4c, the currents are confined inside the layer when the measurement is between pads A,B and pads B,C. But the current passes through the conducting substrate upon measuring pads C,D. Therefore, the resistance vs. pad distance plot shows a linear increase before the measuring distance is larger than the MPD.

The MPD here is between d1 and d0.

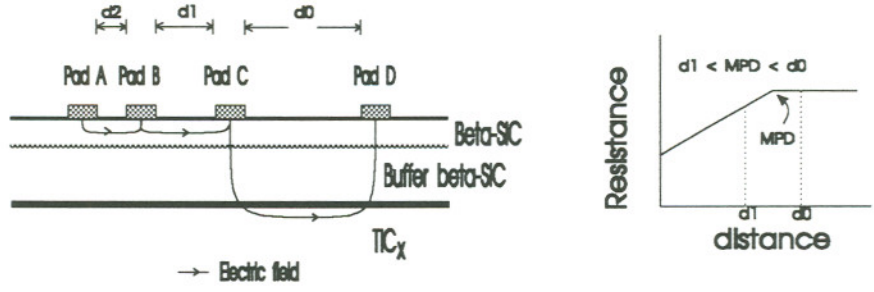


Figure 5.4c Sample with an MPD between d0 and d1.

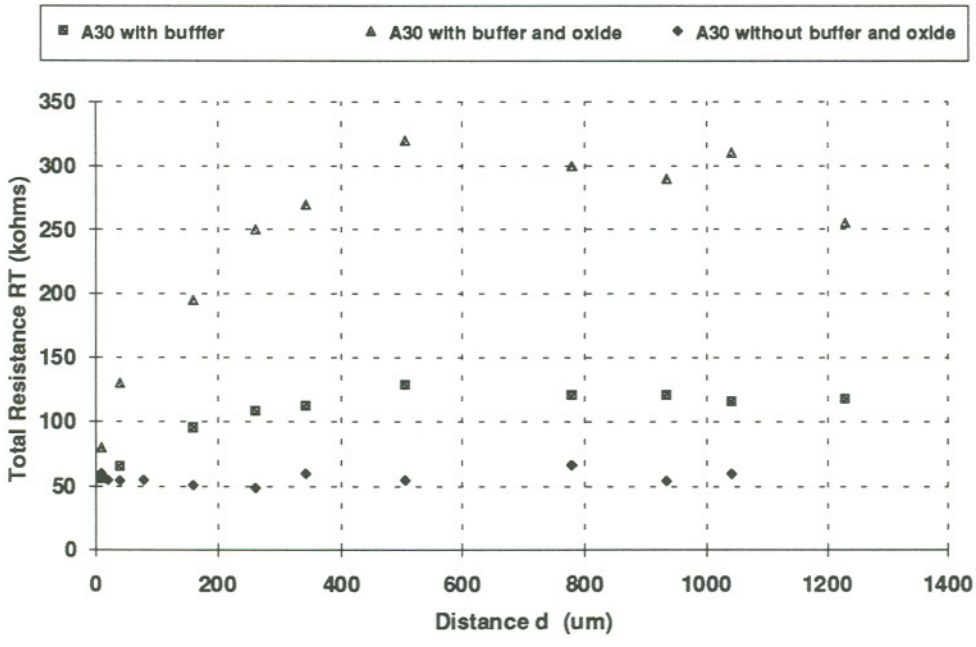


Figure 5.5 MPD measurement of 0.042 sccm Al doped beta-SiC.

An MPD measurement of the 0.042 sccm Al-doped beta-SiC layer is

shown in figure 5.5. The Al-doped beta-SiC layer without a buffer isolation layer has an MPD close to zero. This is because the epi-layer thickness was about 3.3 um, which is smaller than the minimum distance between TLP. A sample with the same Al doping but having a 3.3 um buffer isolation layer showed a 220 um MPD, and the same sample with buffer isolation and wet oxide passivation, done at 1100 °C with 70 °C H_2O for 1 hr., exhibited an MPD of more than 400 um. This suggests that the surface leakage current on the beta-SiC epi-layer significantly affected this measurement.

From the MPD measurement of 0.042 sccm Al doped beta-SiC, the 3.3 um boron doped beta-SiC buffer isolation layer is suitable for isolating devices of up to 400 um channel length. Therefore, the boron doped beta-SiC buffer layer was used for MOSFETs, whose channel lengths are much shorter than 400 um.

5.2.2 Channel

An MOSFET channel should have a low dopant concentration and, therefore, high resistivity. Since we are not able to determine the carrier concentration by either Schottky diode or MOS capacitor measurements (because of the high background concentration, or non-optimized ohmic contacts in beta-SiC epi-layers), the breakdown voltage was used to estimate the dopant concentration of the 0.042 sccm Al doped beta-SiC channel. The estimated carrier concentration from equation 4.9 is in the low 10^{16} cm^{-3} range, and the carrier type as determined by a hot probe measurement is p-type. The sheet resistance of this sample was determined by using the above transmission line measurement;

this method of determining sheet resistance and specific contact resistance is known as the transfer length method (TLM), originally proposed by Shockley[1].

Assuming identical contact resistance for all contact pads allows the total resistance (R_T), the resistance measured between two pads, to be written as

$$R_T = \frac{\rho_s d}{Z} + 2R_c \tag{5.1}$$

where $$R_c = \frac{\sqrt{\rho_s \rho_c}}{Z} \coth(\frac{L}{L_T}).[2,3] \tag{5.2}$$

Z and L are the width and length of the contact pad, respectively (see figure 5.3). d is the pad distance, ρ_S is the substrate sheet resistance, ρ_C is the specific contact resistance from the contact metal to the substrate, and $L_T = (\rho_C/\rho_S)^{1/2}$. Using equations 5.1 and 5.2 with the results of transmission line measurement in figure 5.5, the sheet resistance of the 0.042 sccm Al doped beta-SiC is estimated at 40 kΩ/square. This result shows that the 0.042 sccm Al-doped beta-SiC has high resistivity and is suitable as a channel material.

5.2.3 Source, drain and contacts

Ideally, the source and drain should be highly doped to yield low resistivity. Also, the contact metal should have a low contact resistivity to the source and drain.

The undoped beta-SiC epi-layer was used for the source and drain of the MOSFET. The background carrier concentration of undoped beta-SiC is around 10^{18} cm^{-3}, which was found by measuring both MOS capacitors and Schottky

diodes in chapter 4. Its sheet resistance was determined by using the transfer length method. The results are shown in figure 5.6.

The undoped beta-SiC epi-layer sheet resistance calculated from equations 5.1 and 5.2 is roughly 0.54 kΩ/square, and the specific contact resistance of Al on undoped beta-SiC is around 1 uΩ-cm^2. These results show that Al was acceptable as a contact metal for the undoped beta-SiC sources/drains tested here and that undoped (but n-type) beta-SiC is suitable for source and drain.

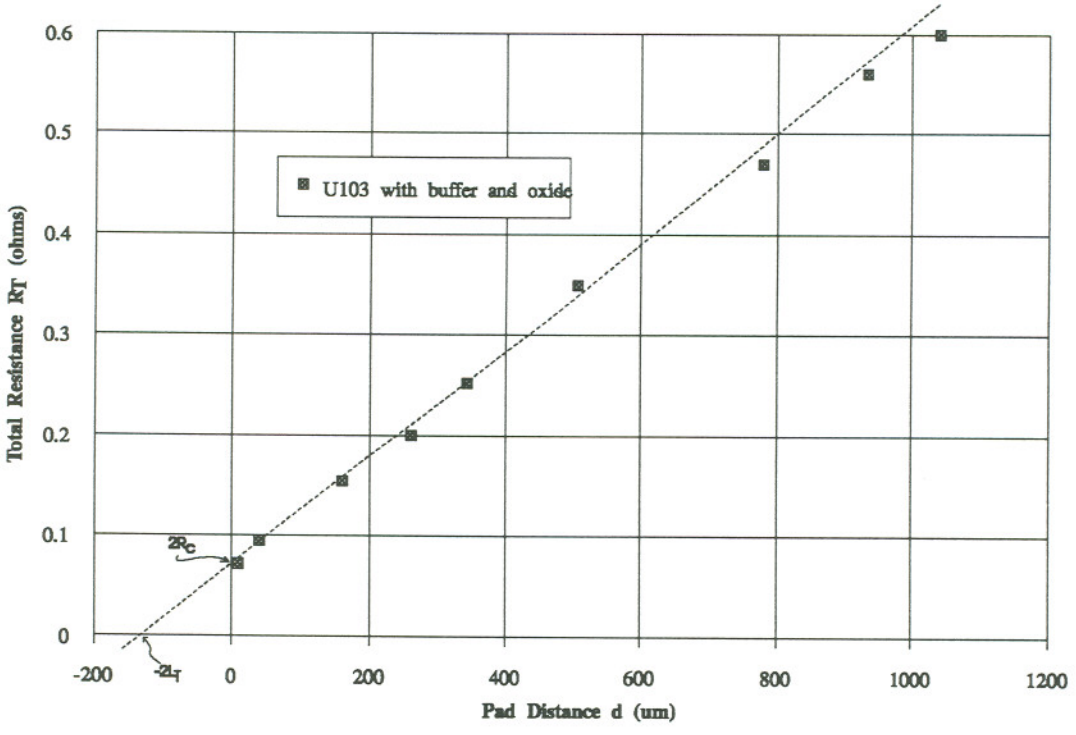


Figure 5.6 Transmission line measurement of Al on undoped beta-SiC epi-layer.

5.2.4 Gate oxide

The C-V measurements of MOS capacitors in chapter 4 indicate that wet thermal oxide on beta-SiC is suitable for oxide devices. The gate oxide of the beta-SiC MOSFETs was grown using the same procedure as that for the MOS capacitors.

5.3 N-CHANNEL BETA-SIC MOSFET PROCESSING

The beta-SiC MOSFET process was modeled after the Si MOSFET process. However, the final processing steps were quite different from those for Si. We describe the beta-SiC MOSFET processing here. The device cross sections shown in the following sections use the legends defined in figure 5.7. The mask set used in the MOSFET processing is shown in table 5.1 in the end of this chapter.

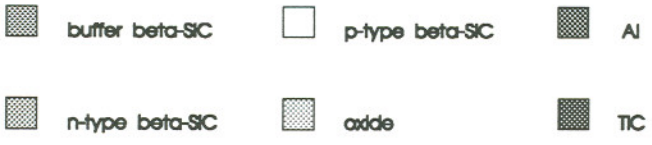


Figure 5.7 Legend of beta-SiC MOSFET process.

5.3.1 Substrate selection through Al deposition

The titanium carbide substrates used for the beta-SiC MOSFETs were first chosen according to their subgrain and pit densities. Only substrates having subgrain densities lower than 2 mm^{-2} and very few pits (< 2 mm^{-2}) were used for

the processing. After the standard cleaning procedure, a 3.3 um buffer isolation beta-SiC epi-layer was grown on top of the substrate to isolate the channel from the conducting TiC_x substrate. On top of the buffer isolation layer, 1.6 um thick 0.042 sccm Al-doped p-type beta-SiC was grown. The surface was then polished with 0.1 um diamond paste. After the polishing, a 2000 Å thick TiC_x "lift-off" epi-layer was grown on top of the p-type beta-SiC to define sources and drains. For device isolation, mesas were created around the devices by reactive ion etching in SF_6 using 4000 Å thick Al as a masking material. The device cross section then looked as shown in figure 5.8.

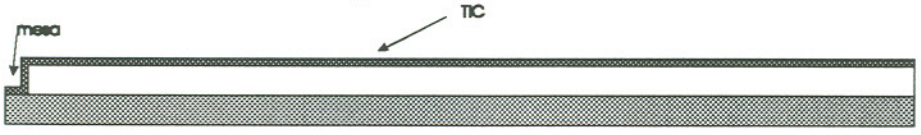


Figure 5.8 The TiC_x substrate as grown with buffer, p-type and TiC_x "lift-off" layer. Note that the mesa is only shown on the left-hand side because the mesa on the right-hand side is made far from the device and, therefore, is not shown here.

5.3.2 Source/drain formation

5.3.2a Current approach

The source and drain of the beta-SiC MOSFET were achieved by an in-situ growth of undoped (but n-type) beta-SiC. The procedure is described in this section. The sample was first evaporated with 4000 Å thick Al, which was used to define the sources and drains. It was subsequently patterned with photoresist, which defined the source and drain windows, then etched in the Al etching

solution and the TiC etching solution. After the definition of source and drain windows, the sample was loaded into the RIE system and etched for 8 min., resulting in about 5600 Å deep source/drain recesses (figure 5.9).

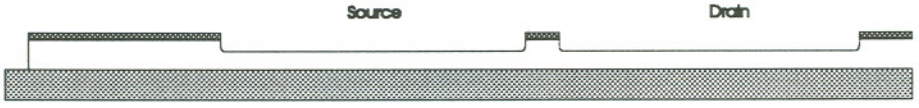


Figure 5.9 Side view of the MOSFET after RIE defining the source/drain recesses.

The sample was next loaded into the CVD system, where an undoped beta-SiC layer was grown; see figure 5.10. Since the TiC etching solution does not attack beta-SiC, the sample was first polished with 0.1 um diamond paste until the shining metal surface of TiC epi-layer was exposed. After the TiC epi-layer was exposed, the sample was etched in the TiC etching solution, and the TiC layer was removed. The sample then looked like figure 5.11.

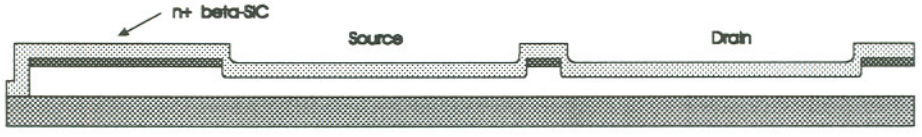


Figure 5.10 Side view of the MOSFET after the undoped beta-SiC epi-growth.

Figure 5.11 Side view of the MOSFET after the polishing by 0.1 um diamond paste and the etching in TiC etching solution.

It is important to verify the characteristics of the source/drain and channel structure next. One simple test of this structure is to use tungsten carbide probes to probe directly on the channel region and on the source/drain region. Typical I-V results are shown in 5.12a and 5.12b. The results are similar to those obtained from the same doping conditions of undoped or Al doped beta-SiC epi-layers after CVD growths (and without further processing). Therefore, the source/drain formation using this technique is acceptable for the present technology.

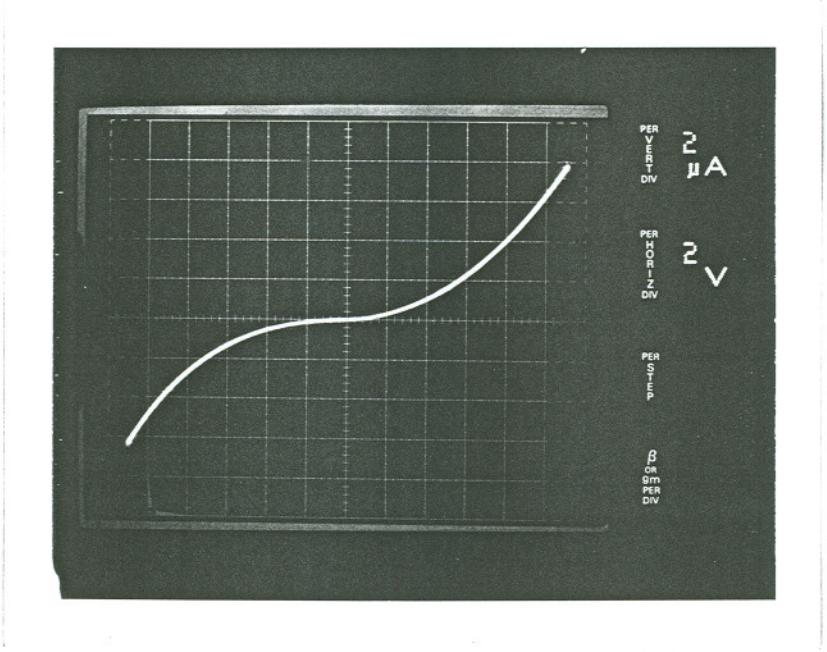


Figure 5.12a I-V plot of the channel region in the A038 MOSFET using two WC probes.

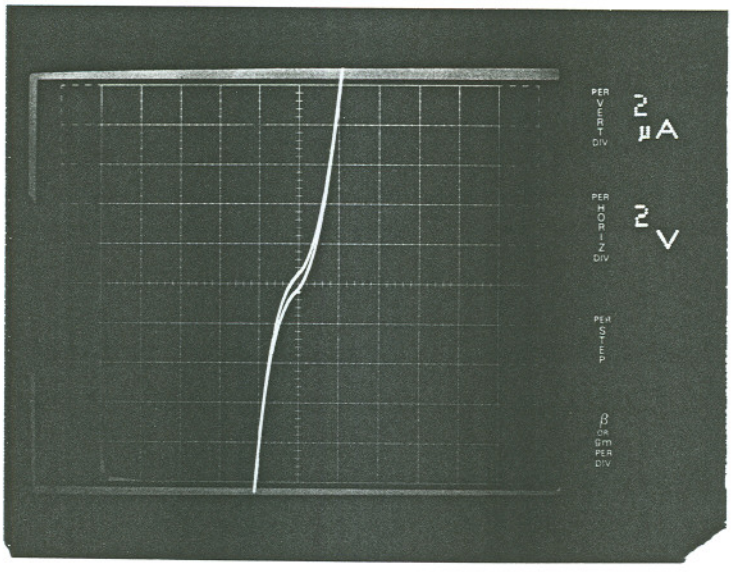


Figure 5.12b I-V plot of the source region in the A038 MOSFET using two WC probes.

5.3.2b Other approaches

We attempted to use the thermal oxide of beta-SiC for the lift-off process of MOSFETs. However, the hydrogen gas, used to carry the organometallic sources, etches thermal oxide above 1100 °C. A 2000 Å thermal oxide was completely etched off before the epi-growth started. Therefore, we were not able to use oxide for the lift-off process. Silicon nitride, which is known to be stable at higher temperatures, should be investigated in the future.

Other alternative approaches, besides the in-situ doping technique described above, should also be studied to optimize the source and drain. Ion implantation seems very successful in the past for phosphorous[4] and nitrogen[5]

n-type dopants. However, ion implantation of p-type dopants, such as boron and Al, is yet to be investigated since activation of implanted p-type dopants in beta-SiC requires temperatures higher than 1400 °C. At such temperatures, most common dielectrics used in device processing will melt. The laser annealing technique[6] seems to be a promising way to activate these ion-implanted p-type dopants. This laser annealing technique uses laser pulses which have a duration of a few nanoseconds; therefore, the samples can be heated to a high temperature. And because of the short duration of the heating process, the heating is limited to a few tenths of a micrometer on the unmasked area. Consequently, the annealing process can be localized without damaging other structures on the sample.

Gas immersion laser doping (GILD) involves immersing a substrate in a dopant gas and forcing the dopant into the substrate with a laser. GILD has recently been very successful in Si[7]. It has the advantages of both laser annealing and ion implantation. Also, because of the short heat cycle, formation of other SiC polytypes can be avoided. Therefore, GILD seems very promising for doping beta-SiC devices.

Both ion implantation and gas immersion laser doping have their advantages. They should be investigated on beta-SiC grown on TiC_x substrates in the future to determine the optimal source/drain formation technique.

5.3.3 Oxidation and metallization

As mentioned in the MOS capacitor study, the wet thermal oxide has better quality after a second oxidation. Therefore, each sample was oxidized

twice; both oxidations used the same procedure. The wet oxidations (70 °C water) were performed at 1100 °C for 1.5 hours. After the oxidation, the sample's cross section then looked like figure 5.13.

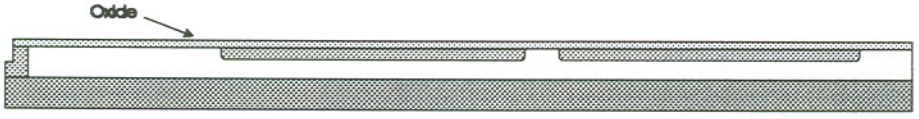


Figure 5.13 Side view of the MOSFET after the oxidation.

The final step in the process was fabrication of the Al the contact metal pads. A 4000 Å thick Al layer was evaporated on the oxide right after the oxidation to ensure clean gate-oxide interfaces. This was followed by defining the gate metal. After the gate metal definition, the contact cuts for sources and drains were defined. The cross section of the sample then looked like figure 5.14.

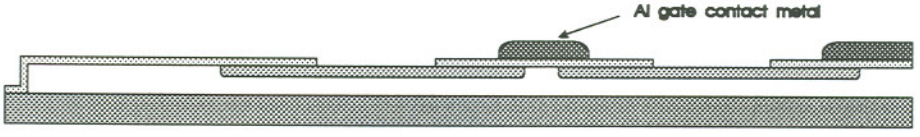


Figure 5.14 Side view of the MOSFET after defining the contact pads. Note that the other Al gate contact metal on the right is belonged to the next MOSFET because the processed structure contains an MOSFET array (see table 5.1).

Next, the contact pads to sources and drains were defined by first evaporating 4000 Å thick Al. A wet etch was subsequently performed to remove unwanted Al, and form the Al contact pads. The device's final cross section is shown in figure 5.15a. Figures 5.15b and 5.15c show the top view of the actual

process results. The critical dimensions of the MOSFET are shown in figure 5.16. A complete illustration of beta-SiC MOSFET process is also shown in table 5.2 in the end of this chapter. Now the devices are ready for testing.

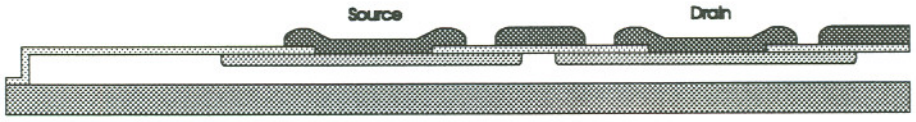


Figure 5.15a Final cross section of the beta-SiC MOSFET.

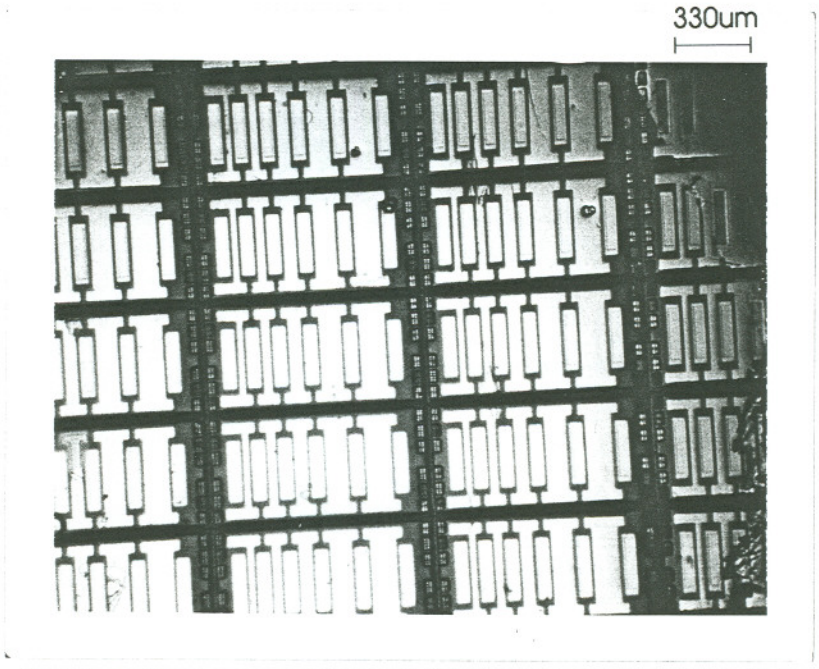


Figure 5.15b Top view of the final MOSFET processing result. The rectangle bars are the sources or drains, and the "I" shape metal between the rectangle bars is the gate contact metal. Note that each MOSFET cell contains 5 MOSFET devices.

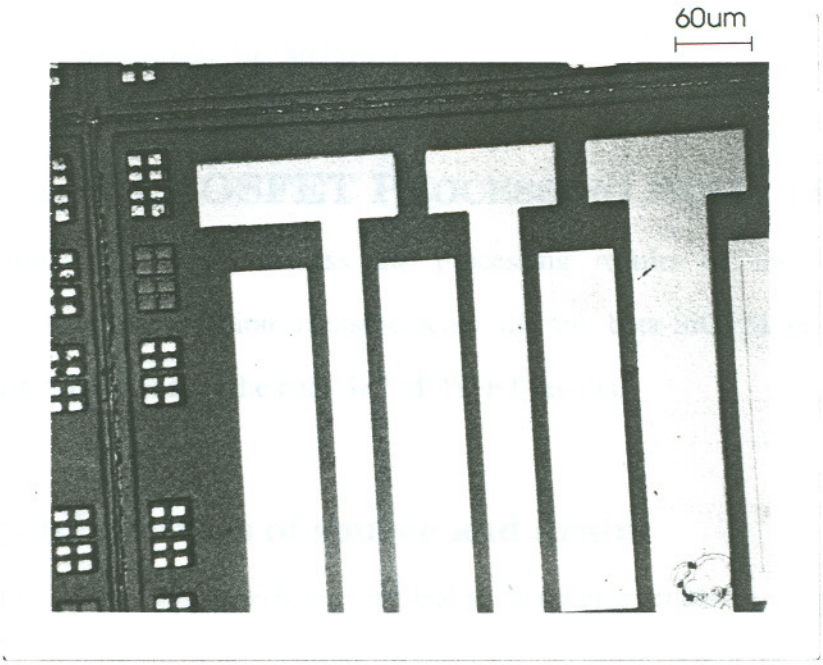


Figure 5.15c Enlarge view of figure 5.15b. Note the small squares on the left are alignment marks for photolithography.

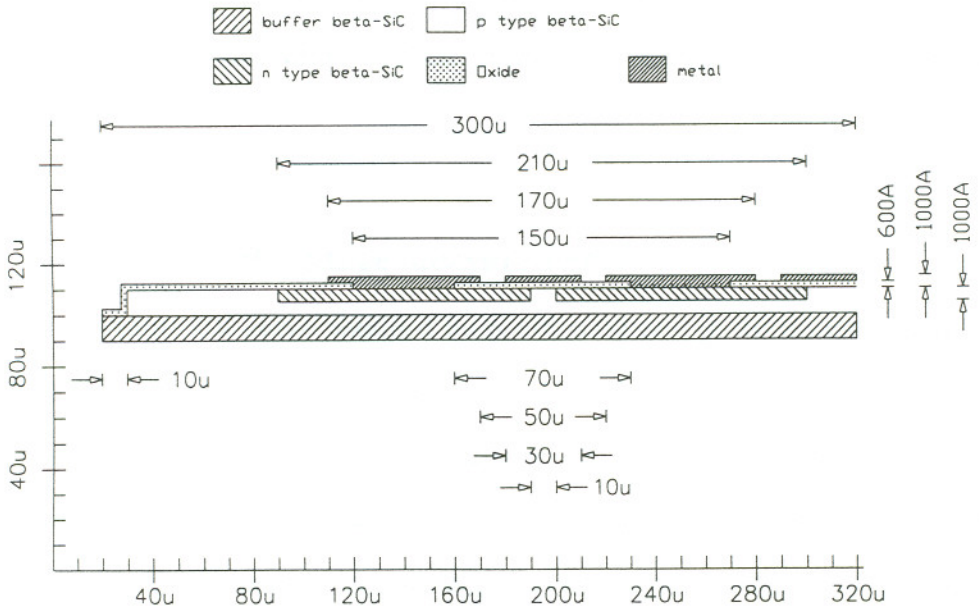


Figure 5.16 Critical dimensions of Beta-SiC MOSFET

5.4 BETA-SIC MOSFET PROCESSING RESULTS

In this section we discuss the processing results of the beta-SiC MOSFETs. The p-n junction measurements of the beta-SiC MOSFET are discussed first, followed by the beta-SiC MOSFET results.

5.4.1 p-n junctions of source and drain

The p-n junctions have been very leaky. Another member in our group is working on improving p-n junctions in beta-SiC devices. To date, no better results have been obtained.

I-V and C-V measurements were used to study the p-n junctions under the MOSFET sources and drains. Their results are described in the following sections.

5.4.1a Current-voltage measurement

A typical I-V curve obtained by positioning one probe on the source and the other probe on the drain is shown in figure 5.17. Since this is a measurement of a n-p-n (source-channel-drain) structure, the results of this measurement should be explained as a back-to-back p-n diode; that is to say, the diode is under reverse bias under both positive and negative bias. The results show no reverse saturation current and are similar to results from a back-to-back beta-SiC p-n diode.

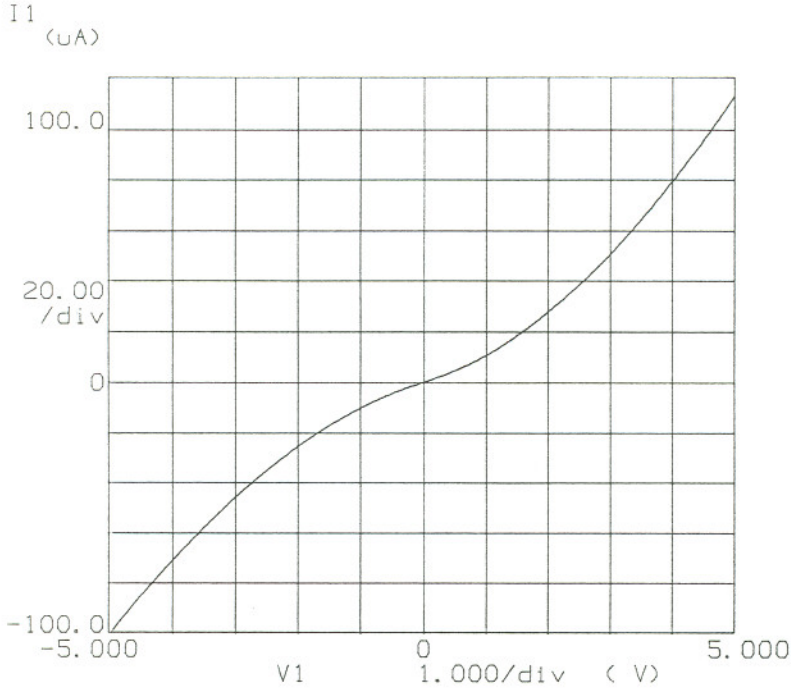


Figure 5.17 I-V measurement between the source and drain of A038 MOSFET. No reverse saturation current was observed.

The C-V results for MOS capacitors, discussed in the last chapter, suggest that heavily compensated p-type beta-SiC has a high defect density. Therefore, one possible explanation of this leaky p-n interface is the high background concentration in beta-SiC epi-layers, which is caused by the auto-doping effects explained in chapter 4. Another possible explanation of this leaky interface is due to the surface leaky. However, more studies are necessary to identify the major cause.

5.4.1b Capacitance-voltage measurement

The structure between the source and drain of the MOSFET is a back-to-

back p-n diode. The C-V measurements on this diode are shown in figures 5.18a and 5.18b. In figure 5.18a, capacitance (C) is plotted against gate bias (V), and $1/C^2$ is plotted against V in figure 5.18b. Figure 5.18b shows an excellent linear relationship between $1/C^2$ and V. This indicates that the sources and drains formed by our in-situ doping technique form abrupt junctions with the channel. The carrier concentration in the channel calculated by the one-sided abrupt p-n junction model from this C-V result is around $5*10^{16}$ cm^{-3}, which is very close to the result obtained by the breakdown voltage measurement.

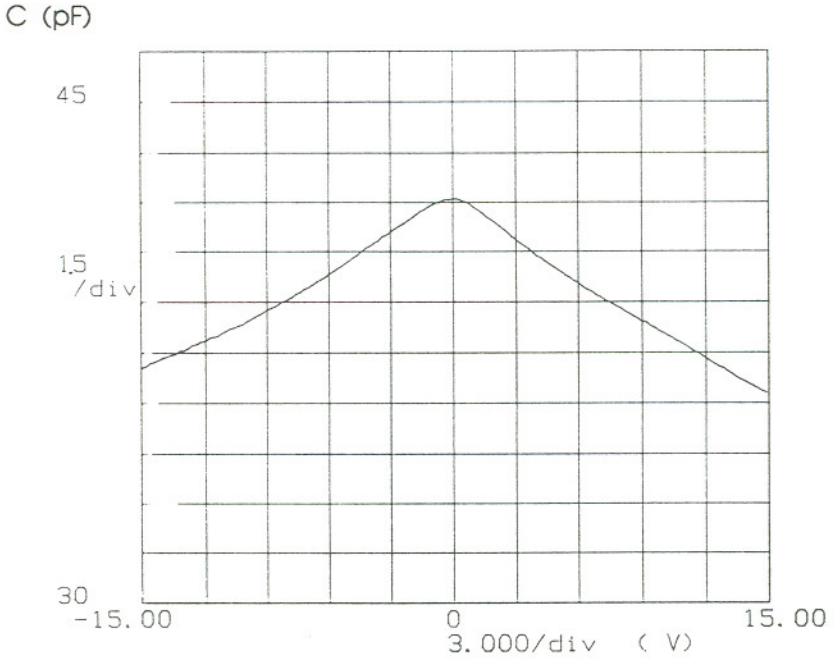


Figure 5.18a C-V measurement between the source and drain of A038 MOSFET.

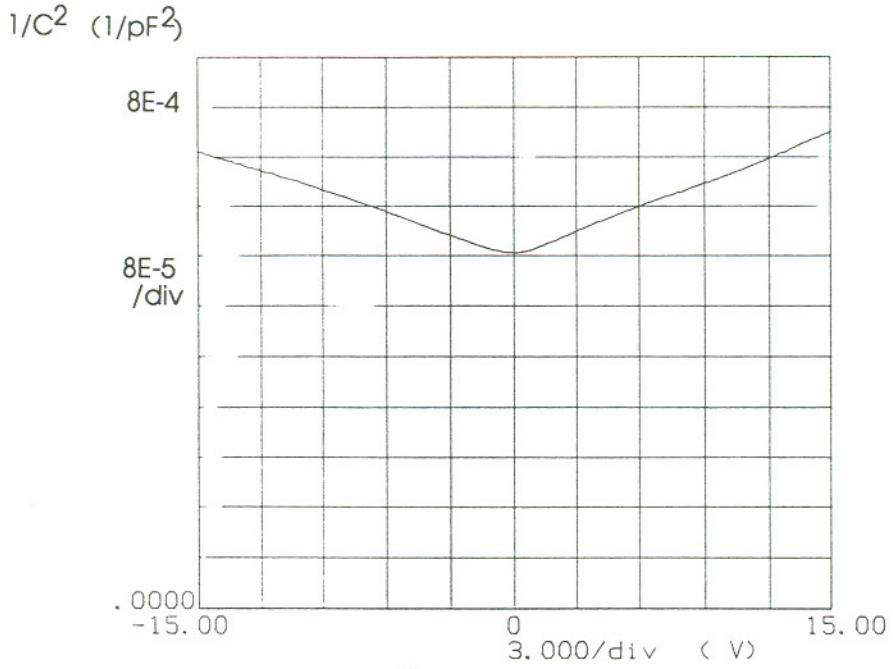


Figure 5.18b Plot of $1/C^2$ as a function of gate bias for A038 MOSFET in figure 5.18a. The excellent linear result suggests the p-n junctions under the source and drain are abrupt junctions.

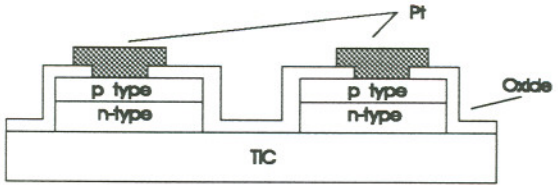


Figure 5.19 Structure of a back-to-back beta-SiC p-n diode.

We were not able to obtain such a simple $C^n \propto V$ relationship in the C-V measurement of either back-to-back Schottky diodes or back-to-back p-n diodes. In the case of back-to-back Schottky diodes, we could not obtain such a result because of the non-optimized metal-semiconductor interface. On the other hand,

we couldn't obtain such a result for back-to-back p-n diodes, which have non-recessed structures (figure 5.19), because of the non-optimized ohmic contacts.

5.4.2 MOSFET

Since we could not obtain low leakage p-n interfaces, the results of the beta-SiC MOSFETs were affected by the non-saturated reverse current. The I-V measurement of a beta-SiC MOSFET with a buffer layer is shown in figure 5.20a. Also, the I-V result of a beta-SiC MOSFET without a buffer layer is shown in figure 5.20b. The I-V curve of the beta-SiC MOSFET without a buffer layer showed no modulation due to the gate bias and a higher leakage current, as predicted in section 5.2.2. On the other hand, because the source/drain current passed through the channel, the beta-SiC MOSFET with a buffer layer showed a lower leakage current, and that the gate bias voltage did modulate the channel charges, as predicted in the C-V measurement of the beta-SiC MOS capacitors.

These results suggest that a beta-SiC MOSFET on TiC_X is possible. Formation of the source/drain by the in-situ doping technique is quite adequate for the present technology. The wet thermal oxide on beta-SiC is suitable as an insulator for MOS devices. A buffer isolation layer is necessary for lateral devices on TiC_X substrates. The boron doped buffer isolation layer is appropriate as a buffer isolation layer for lateral devices in beta-SiC on TiC_X substrates. With better control of surface leakage and p-n junctions in the future, beta-SiC MOSFETs on TiC_X can be improved.

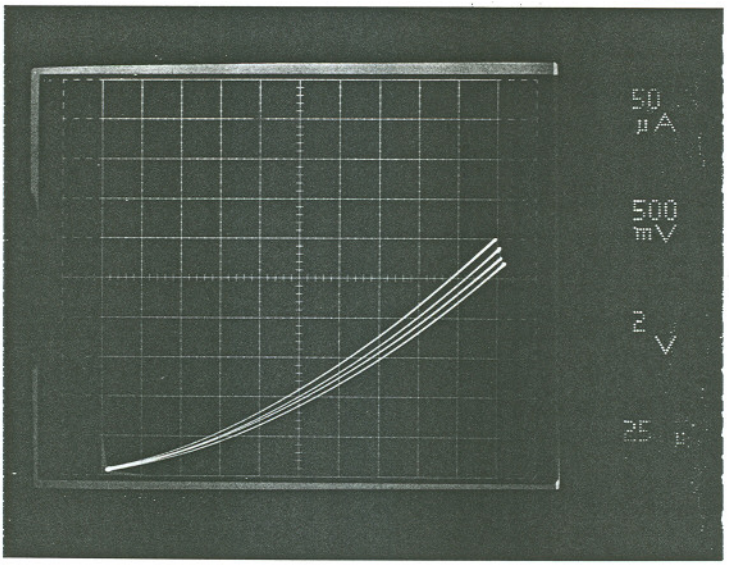


Figure 5.20a Drain current as a function of drain voltage for various gate voltages of the A038 beta-SiC MOSFET. The channel length of this MOSFET was 10 um.

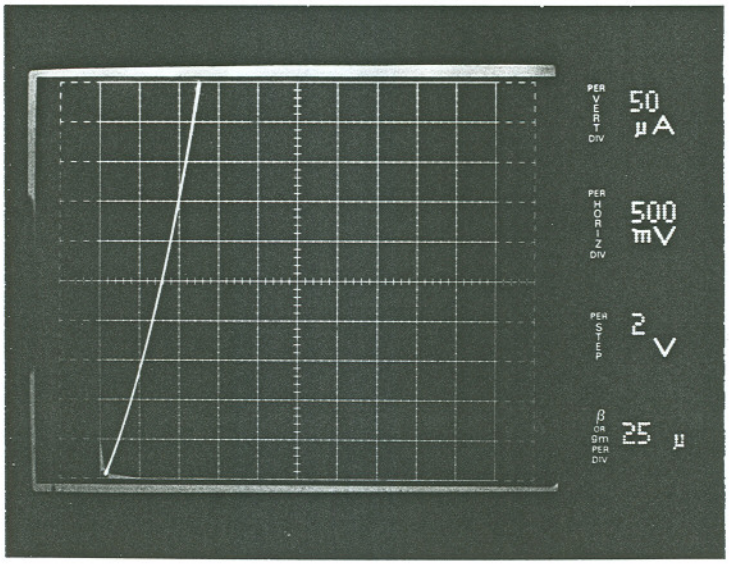


Figure 5.20b A typical result of drain current as a function of drain voltage for various gate voltages for a beta-SiC MOSFET without a buffer layer. The drain current was not modulated by the gate bias.

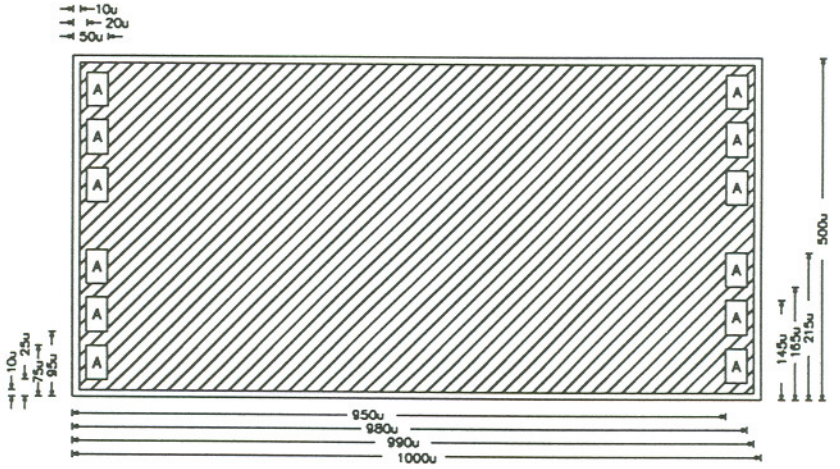
5.5 SUMMARY

In this chapter, we have described the first successful fabrication of n-channel beta-SiC MOSFETs on TiC_x substrates. The formation of source and drain was by in-situ growth of undoped beta-SiC. The channel of the MOSFET was doped with about 6 x 10^{16} cm^{-3} Al. Al was used as a contact metal to the source and drain; the contact resistance of Al on undoped beta-SiC was about 1uΩ-cm^2. A boron doped buffer isolation layer was used to isolate lateral MOSFET devices from the conducting TiC_x substrates. The maximum penetrating depth (MPD) measurement was developed to evaluate the beta-SiC buffer isolating layers. The B doped buffer isolation layer was found to adequately isolate lateral devices up to 400 um from the conducting TiC_x substrates.

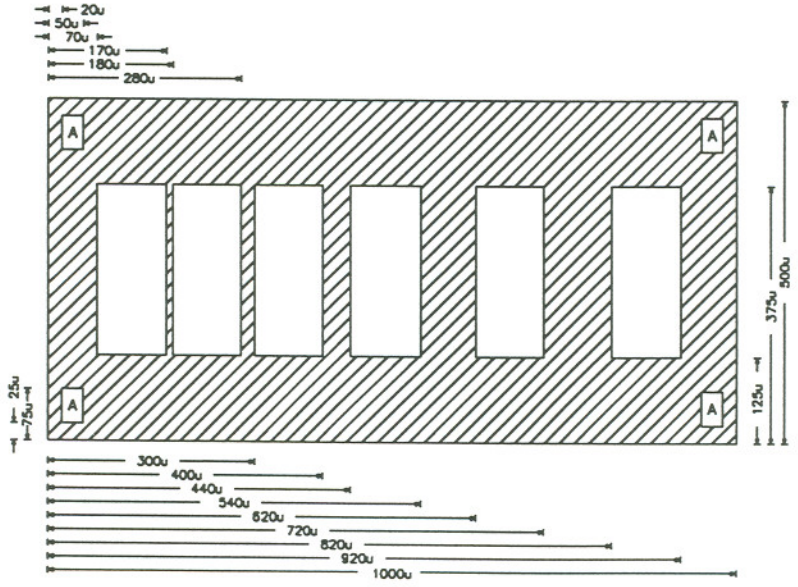
Table 5.1 Mask set used for beta-SiC MOSFET fabrication

Note: Hatched area is dark field.

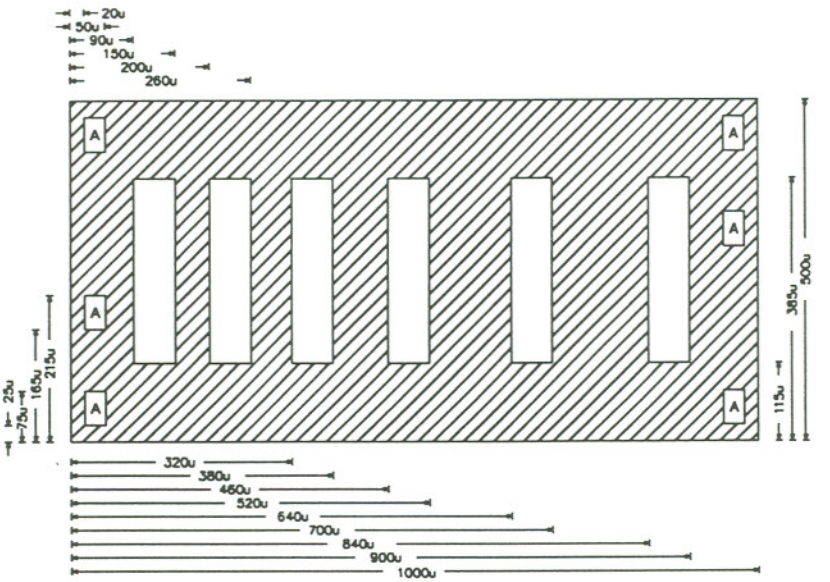
Squares with "A" inside are alignment marks for photolithography.



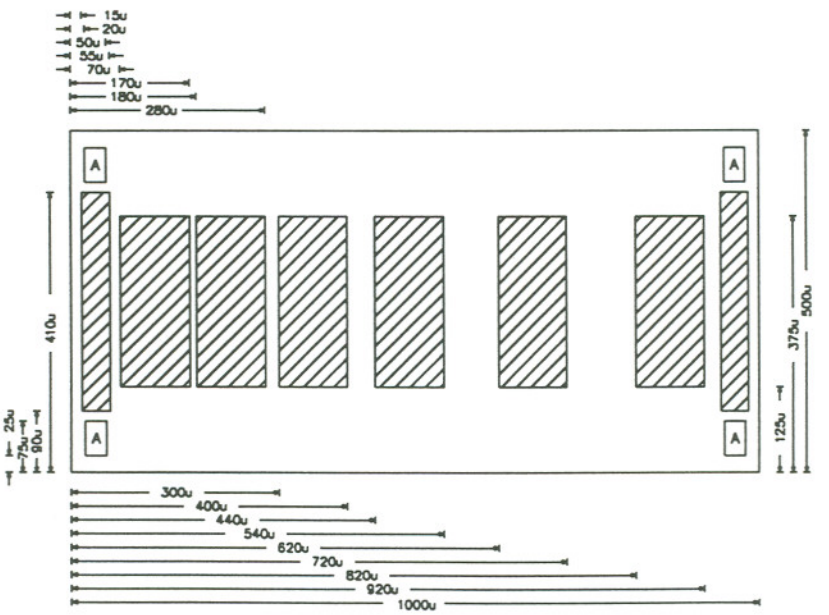
Ob1



Ob2

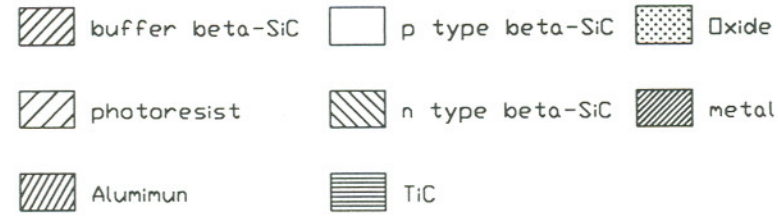

20u
50u
90u
150u
200u
260u
A
25u
75u
165u
215u
320u
380u
460u
520u
640u
700u
840u
900u
1000u
385u
500u
115u

0b5

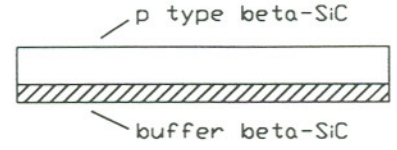

15u
20u
50u
55u
70u
170u
180u
280u
A
25u
75u
90u
410u
300u
400u
440u
540u
620u
720u
820u
920u
1000u
375u
500u
125u

06

Table 5.2 Processing steps of beta-SiC MOSFET

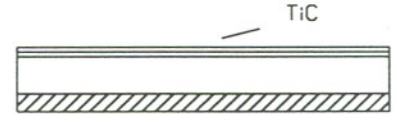


Buffer and p type beta-SiC

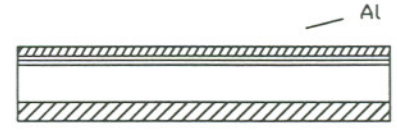


Device island mesa etching (mask Ob1)

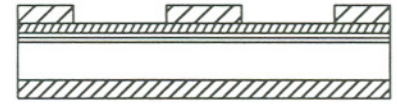
TiC growth for lift-off



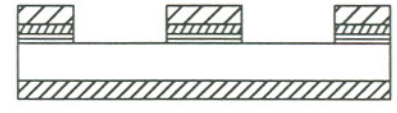
Alumimum Deposition



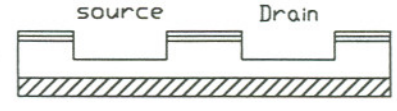
photoetching (mask Ob2)

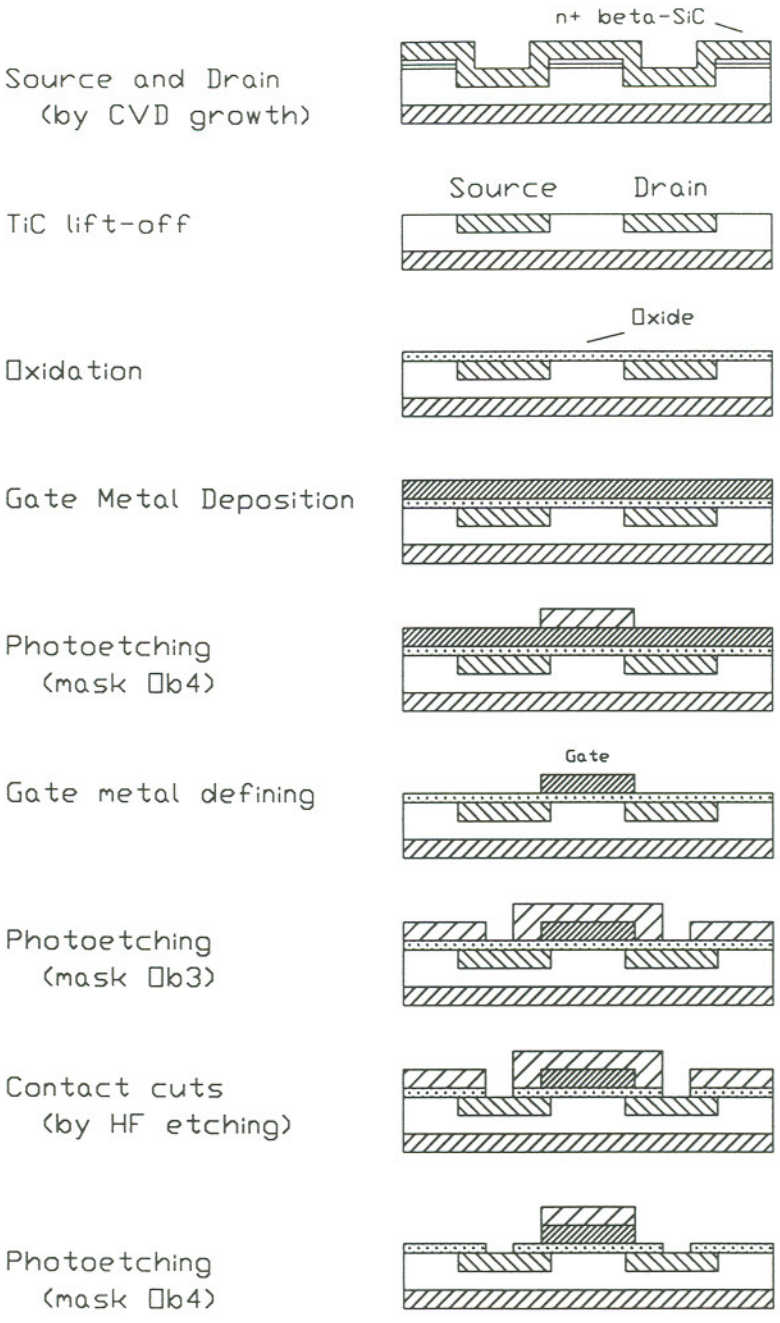


Souce and Drain windows (by Al etching solution)

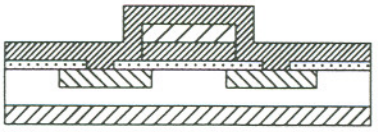


Source & Drain windows (by RIE)

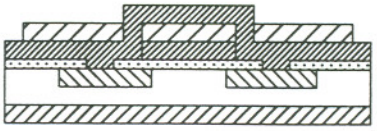



n+ beta-SiC
Source and Drain
(by CVD growth)
Source
Drain
TiC lift-off
Oxide
Oxidation
Gate Metal Deposition
Photoetching
(mask b4)
Gate
Gate metal defining
Photoetching
(mask b3)
Contact cuts
(by HF etching)
Photoetching
(mask b4)

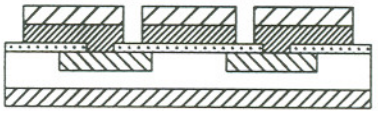
Ohmic contact metal deposition



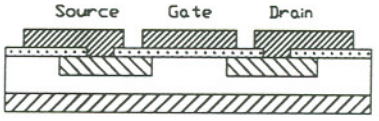
Photoetching (mask Ob4 and Ob5)



Ohmic contact metal etching



Photoresist removal



CHAPTER 6

CONCLUSIONS AND SUGGESTIONS

6.1 CONCLUSIONS

1. Results of current studies suggest that beta-SiC epi-layers grown on TiC_x substrates have better crystal quality than any of the other approaches, and that the characteristics of beta-SiC epi-layers on TiC_x substrates are quite different from those on Si or 6H alpha-SiC.

2. A model oxidation process on beta-SiC is developed. Our experimental results fit the model very well. The activation energies (to initiate diffusion H_2O through the oxide and to break Si-C bonds) calculated from oxidation results suggest that the beta-SiC crystal grown on TiC_x is closer to the ideal crystal than those obtained from any other approach.

3. Inversion of beta-SiC MOS capacitors is possible if a low defect beta-SiC crystal is available. And the high frequency C-V measurements of beta-SiC MOS capacitors can be easily modeled using the existing model. This modeling result

shows that the thermal oxide on undoped beta-SiC has a very low interface trap density.

4. All basic components for fabricating a beta-SiC MOSFET are available although they have not been optimized. Processing of MOSFETs or MOS capacitors on beta-SiC grown on TiC_x substrates is possible in spite of extra steps and precautions required.

5. The high background carrier concentration of these beta-SiC epi-layers was a key problem. Availability of larger diameter TiC substrates may eliminate this problem.

6.2 CONTRIBUTIONS

The major contributions of this work are:

. Measurement and characterization

1. Obtained basic properties of thermal oxides grown on beta-SiC grown epi-layers.
2. Developed models for beta-SiC oxidation process.
3. Demonstrated inversion of beta-SiC MOS capacitors in dark at room temperature for the first time, ever.

4. Developed testing procedures for buffer isolation layers on conducting substrates.

. Device processing

1. First MOSFET in beta-SiC grown on TiC_x substrate.
2. First recessed source/drain beta-SiC MOSFET by the in-situ doping technique.

6.3 SUGGESTIONS FOR FUTURE WORK

. p-n junction

Optimized p-n junctions are necessary for both unipolar and bipolar devices (except for MIS diodes). Once optimized p-n junctions are available, other device structures, such as JFETs, MESFETs, MOSFETs, bipolar transistors and thyristors, can easily be fabricated. High background concentration of beta-SiC epi-layer and surface leakage are the two obstacles. Investigations on surface passivation and on reducing background doping concentration should be performed.

. Processing

Processing procedures need refinement. The roughness of TiC_x after oxidation must be eliminated. Approaches to this problem include removal of beta-SiC epi-layers from the TiC_x substrates, and protecting the TiC_x substrates with other materials. Both of them need investigation.

REFERENCES

Chapter 1.

1. Neil Weste and Karmran Eshraghian, "Principles of CMOS VLSI Design," Addison-Wesley, p125 (1985).

Chapter 2.

1. E. M. Conwell, Proc. IRE, 46 p1281 (1958).

2. L. A. Hemstreet and C. Y. Fong, Proc. 3rd Int. Conf. on SiC, Miami Beach, FL., p284 (1973).

3. H. R. Phillip and E. A. Taft, "SiC, A high Temperature Semiconductor," Ed. J. R. O'connor and J. Smithens, Pergamon Press, p366 (1960).

4. S. M. Sze, "Physics of Semiconductor Devices," Second Ed., John Wiley and Sons, New York (1981).

5. S. M. Sze and J. C. Irwin, Sol. St. Electron. 11 p599 (1968).

6. W. E. Nelson, et. al., Contract No. Nobsr-87235, DDC AD-428 005 (12/13/1963).

7. G. N. Violina, et. al., Sov. Phys. - Solid State, 5 12 p2500 (1964).

8. M. Yamanaka, H. Diamon, E. Saluma, S. Misawa and S. Yoshida, J. Appl. Phys., 81 2 p599 (1987).

9. J. A. W. Van Der DOES De BTE, Phillips Res. Repts., 17 5 p418 (1962).

10. D. K. Ferry, Phys. Rev. B., 12 6 p2361 (1975).

11. M. Shinohara, M. Yamanaka, H. Daimon, E. Sakuma, H. Okumura, S. Misawa, K. Endo and S. Yoshida, Japanese J. Appl. Phys., 2, Lett., 27 3 LA34 (1988).

12. A. Suzuki, A. Ogura, K. Furukawa, Y. Fiji, M. Shigeta and S. Nakajima, J. Appl. Phys., 64 5 p2818 (1988).

13. K. Sasaki, E. Sakuma, S. Misawa, S. Yoshida and S. Gonda, Appl. Phys. Lett., 45 1 p72 (1984).

14. J. D. Parsons, A. T. Hunter and D. C. Reynolds, Proc. Int. Symp. GaAs and Related Compounds, Karuizawa, Japan, 1985; Inst. Phys. Conf. Ser. 79 p211 (1986).

15. D. M. Caughey, and R. E. Thomas, Proc. IEEE. 55 p2192 (1967).

16. W. Von Muench and E. Pettenpaul, J. Appl. Phys. 48 11 p4823 (1977).

17. C. Van Opdorp and J. Vrakking, J. Appl. Phys. 40 5 p2320 (1969).

18. K. Thiessen, et. al., Phys. Stat. Sol., 3 3 p529 (1963).

19. L. Patrick, and W. J. Choyke, Phys, Rev., B2 p2255 (1970).

20. G. H. Glover, J. Appl. Phys., 46, 11 p4842 (1975).

21. M. M. Anikin, M. E. Levinshtein, I. V. Popov, V. P. Rastegaev, A. M. Strel'chuk, and A. L. Syrkin, Sov. Phys, Semicond., 22 9 p995 (1988).

22. G. A. Slack, J. Appl. Phys, 35 12 p3460 (1864).

23. Vodakov, A. Yu and E. N. Mokhov, " DIffusion and Solubility of Impurities in Silicon Cardbide," Proceedings of the Third International Conference on Silicon Carbide, p508-519 (1973).

24. J.W.Palmour, H.S. Kong, and R.F. Davis, J. Appl. Phys. 64 (4), p2168 (1988).

25. J.D. Parsons, "Beta-SiC Power Impatt Development: Interim Techincal Annual Report 3" submited to Naval Weapons Center, China Lake, CA, Contract N60530-85-C-0163, p24 (1989).

26. R. W. Kee, K. M. Geib, C. W. Wilmsen, and D. K. Ferry, "Interface Characterics of Thermal SiO_2 on SiC," J. Vac. Sci Technol. 15(4), p1520 (1978).

27. A. Suzuki, H. Ashida, N. Furui, K. Mameno and H. Matsunami, "Thermal Oxidation of SiC and Electrical Properties of Al-SiO_2-SiC MOS Structure," Japanese J. of Applied Physics, Vol.21, No.4, p579 (1982).

28. K. Shibahara, S. Nishino and H. Matsunami, "Metal-Oxide-Semiconductor Characteristics of Chemical Vapor Deposited Cubic-SiC," Japanese J. of Applied Physics, Vol.23, No.11, L862 (1984).

29. J. W. Mayer, L. Erikson and J.A. Davies, "Ion Implantation in Semiconductors," Academic Press, N.Y. (1970).

30. J. O. Marsh, "Ion Implantation in SiC, " Proc. Third Int. COnf. SiC, p471-485, (1973).

31. R. R. Hart, H. L. Dunlap and O. J. Marsh, "Back-scattering Analysis and Electrical Behavior of SiC Implanted With 40Kev Indium," II Int. Conf. Ion Implantation in Semiconductors, Garmisch-Parten-Kirchen, Germany, p134 (1971).

32. O. J. Marsh, "Ion Implantation in SiC," Silicon Carbide, Columbia, SC, Univ. of South Carolina Press, p471-485 (1973).

33. J. A. Edmond and R. F. Davis, "Ion Implantation and Thermal Annealing of P and Al Dopants in High Purity Beta Silicon Carbide Single Crystal Films," Electrical Materials Conf., The Metallurgical Soc. of AIME, p80-83 (1985).

34. Y. Kondo, T. Takahashi, E. Sakuma, S. Misawa, H. Daimon, S. Yoshida and Y. Hayashi, "Ion Implantation in ß-SiC Single Crystal," 46th Autumn Meeting Japan Soc. Appl. Phys., Kyoto, Japan, 2p-C-11, p569 (1985).

35. S.Y. Chou, Y. Chang, T.W. Sigmon and J.D. Parsons, "Application of Excerimer Laser Processing in SiC Device Fabication", Amorphous and Crystalline Silicon Carbide II, Spring Proceedings in Physics 43, Ed. M. M. Rahman, C.Y.-W Yang and G. L. Harris, (1989).

36. R. I. Scace and G. A. Slack, "Silicon Carbide - a High temperature semiconductor," Ed. J. R. O'Connor, J. Smiltens, Pergramon, p24 (1960).

37. V. E. Straughan and E. F. Mayer, " Growth of Silcon Carbide by Gaseous Cracking," Silicon Carbide Proc. Conf., Boston (1955).

38. Yu. M. Tairov and V. F. Tsvetkov, "General Principles of Growing Large-Size Single Crystals of Various Silicon Carbide Polytypes," Jour. Crys. Growth, Vol. 52, p146-150, (1981).

39. W. E. Nelson, F. A. Halden, and A. Roseengreen, "Growth and Properties of ß-SiC Single Crystals," Jour. Appl. Phys., Vol. 37, No. 1, p333-336 (1966).

40. " Proceedings of the Third International Conference on Silicon Carbide," Appendix II, p669(1973).

41. Von Muench, W. Gillessen and K. Gillessen, "Liquid-Phase Expitaxy of Silicon Carbide by Travelling Heater Method," Porc. Third Int. Conf. SiC, p. 51-57, Sept. 17-20 (1973).

42. M. Dubey, "Study of Recrystalliztion of SiC thin Films," Mat. Res. Bull., Vol. 11, p. 197-202 (1976).

43 S. Nishino, Y. Hazuki, H. Matsunami and T. Tanaka, " Chemical Vapor Deposition of Single Crystalline ß-SiC Films on Silicon Substrate with Sputtered SiC Intermediate Layer," J. Electrochem. Soc., Vol. 127, No. 12, p. 2674-2680 (1980).

44. M. Balog, A. Reisman and Berkenblit, "The Formation of ß-SiC on Si," J. Electronic Materials, Vol. 9, No. 3 (1980).

45. A. J. Learn and I. H. Kahn, "Growth Morphology and Crystallographic Orientaion of ß-SiC films by Chemical COnversion," Thin Solid Films, Vol. 5, p145-155 (1970).

46. J. D. Parsons, "Vapor Phase Epitaxy of Beta Silicon Carbide on Titanium Carbide, " Ph.D. Dissertation, ULCA, Dec. 1981.

47. S. Nishino, J. A. Powell, H. A. Will, "Production of Large-Area Single-Crystal Wafers of Cubic SiC for Semiconductor Devices," Appl. Phys. Lett., Vol. 42 (5), p. 460-62 (1983).

48. S. Nishino, H. Suhara and H. Matsunami, "Reproducible Preparation of Cubic-SiC Single Crystals by Chemical Vapor Deposition", Proc. 15th Conf. Solid State Devices and Materials, Tokyo, p. 317-20 (1983).

49. P. Liaw and R.F. Davis, J. Electronchem Soc. (Mar 1985).

50. H.S. Kong, J.T. Glass and R.F. Davis, Appl. Phys. Lett. 49 (17) (1986).

51. J.D. Parsons, "Inverted-Vertical OMVPE reactor:design and characteriztion", J. Crystal Growth 116, p387(1992).

52. S. M. Sze, "Physics of Semiconductor Devices," Second Ed., Appendix H, John Wiley and Sons, New York (1981).

53. R.W.G. Wyckoff, "Crystal Structures," Wiliey & Sons, N.Y., Vol. 1, pp. 114 (1961).

54. A. Tayor and R.M. Jones, "Silicon Carbide, A High Temperature Semiconductor," Ed. J.R. O'Connor and J. Smiltens, Pergamon Press, N.Y., p147 (1960).

55. "HandBook of Chemisty & Physics," 72nd Edition, Ed. D.R. Lide, CRC Press, p12-132 (1991).

56. E.L. Kern, D.W. Hamill, H.W. Deem and H.D. Sheets, Mat. Res. Bull., 4, S25 (1969).

57. O.H. Krikorian, "Thermal Expansion of High Temperature Materials," Contract No. W-7405-eng-48, 7 pages, Sept. 6 (1960).

58. R.I. Scace G.A. Slack, "Silicon Carbide, A High Temperature Semiconductor," Ed. J.R. O'Connor and J. Smiltens, Pergamon Press, N.Y., p24 (1960).

59. G. A. Slack, J. Appl. Phys, 35 12,p3460 (1964).

60. C. H. Carter, Jr. J.A. Edmond, J.W. Palmour, J. Ryu, H.J. Kim, and R.F. Davis, "Microscopic Identification of Electronic Defects in Semiconductors", Material Reserch Society Symposium Proceedings, edited by N.M. Johnson, S.G. Bishop, and G. Watkin (North Holland, Amsterdam), Vol. 46, p456 (1984).

61. J. W. Palmour, H. S. Kong and R. F. Davis, "Characterization of Device Parameters in High-Temperature Metal-Oxide-Semiconductor-Field-Effect Transistors in ß-SiC Thin films," J. Appl. Phys. 64 (4), p2168, 15 (1988).

62. H. S. Kong, B. L. Jiang, J. T. Glass, G.A. Rozgonyi and K.L. More, "An examination of double positioning boundaries and interface misfit in beta-SiC films on alpha-SiC substrates," J. Appl. Phys. 63 (8), p2645, (1988).

63. J.D. Parsons, G.B. Kruaval and J.A. Vigil, "ß-SiC on Titanium Carbide for Silid State Devices," Amorphous and Crystalline Silicon Carbide II, Spring Proceedings in Physics 43, Ed. M. M. Rahman, C.Y.-W Yang and G. L. Harris, (1989).

Chapter 3.

1. M. I. Chaudhry, " Ohmic Contacts and MOS structures on beta-SiC," Ph.D. Dissertation, Univ. Notre Dame (1987).

2. Her-Song Chen and J. D. Parsons, to be published.

3. A. Suzuki, H. Ashida, N. Furui, K. Mameno and H. Matsunami, " Thermal Oxidation of SiC and Electrical Properties of Al-SiO2-SiC MOS structure," Jpn. J. Appl. Phys., Vol.21, No.4, pp579(1982).

4. K. Shibahara, S. Nishino and H. Matsunami, "Metal-Oxide-Semiconductor Characteristics of Chemical Vapor Deposited Cubic -SiC," Jpn. J. Appl. Phys., Vol.23, No.11, p579(1984).

5. E. Fitzer and R. Ebi, "Silicon Carbide-1973," eds. R.C. Marshall, J.W. Faust, Jr. and C.E. Ryan (University of South Carolina Press, Columbia), p320 (1974).

6. B.E. Deal and A.S. Grove, J. Appl. Phys. 36, p3770 (1965).

7. R.F. Adamsky, "Oxidation of Silicon Carbide in the Temperature Range 1200 C to 1500 C, " J. Phys. Chem. 63 (1959).

8. E.H. Nicollian and J.R. Brews, "MOS (Metal Oxide Semiconductor) Physics and Technolgy" (Wiiey, New York), p684 (1982).

9. R.C.A. Harris and R.L. Call: Silicon Carbide-1973, eds. R.C. Marshall, J.W. Faust, Jr. and C.E. Ryan (University of South Carolina Press, Columbia), p329 (1974).

10. L. Pauling, "The Nature of the Chemical Bond and the Structure of Molecules and Crystals", Cornell University Press, New York, p85 (1960).

Chapter 4.

1. J.D. Parsons, U.S. patent 4,738,937 (1988).

2. A. Suzuki, H. Ashida, N. Furui, K. Mameno and H. Matsunami, " Thermal Oxidation of SiC and Electrical Properties of Al-SiO2-SiC MOS structure," Jpn. J. Appl. Phys., Vol.21, No.4, pp579 (1982).

3. K. Shibahara, S. Nishino and H. Matsunami, "Metal-Oxide-Semiconductor Characteristics of Chemical Vapor Deposited Cubic -SiC," Jpn. J. Appl. Phys., Vol.23, No.11, p579(1984).

4. R. W. Kee, K.M. Geib, C. W. Wilmsen and D. K. Ferry, "Interface Characrteristics of Thermal SiO2 on SiC," J. Vac. Sci. Technol. 15(4), p1520 (1978).

5. K. Shibarhara, T. Saito, S. Nishino, and H. Matsunami, "Fabrication of Inversion-Type n-Channel MOSFET's Using Cubic-SiC on Si(100)," IEEE Electron Device Lett., vol. EDL-7, No. 12, p692 (1986).

6. H. Fuma, A. Miura, H. Tadano, S. Sugiyama and M. Takigawa, "High Temperature Operated Enhancement-Type beta-SiC MOSFET," Jpn. J. Appl. Phys., Vol. 27, No. 11, L2143 (1988).

7. E. H. Nicollian and J. R. Brews, "MOS (Metal Oxide Semiconductor) Physics and Technology," Wiley, New York, p374 (1982).

8. L. I. Schiff, " Quantum Mechanics," 3rd edition, McGraw-Hill, Inc., p269 (1975).

9. E. H. Nicollian and J. R. Brews, "MOS (Metal Oxide Semiconductor) Physics and Technology," Wiley, New York, p378 (1982).

10. R. S. Muller and T. I. Kamins, " Device Electronics for Integrated Circuits," 2nd Edition, Wiley, p20 and p17 (1986).

11 W. Van Gelder and E. H. Nicollian, J. Electrochem. Soc., 119, 1068 (1972).

12. E. H. Nicollian and J. R. Brews, "MOS (Metal Oxide Semiconductor) Physics and Technology," Wiley, New York, p407 (1982).

13. S. M. Sze, "Physics of Semiconductor Devices," 2nd Ed., Wiley, p104 (1981).

14 E. H. Nicollian and J. R. Brews, "MOS (Metal Oxide Semiconductor) Physics and Technology," Wiley, New York, p161 (1982).

15. S. M. Sze, "Physics of Semiconductor Devices," 2nd Ed., Wiley, p368 (1981).

16. L. M. Terman, Solid-State Electron., 5, p285 (1962).

17. S. Zaima, K.Onoda, Y. Koide and Y. Yasuda, "Effects of Oxidation conditions on Electrical Properties of SiC-SiO_2 Interfaces," J. Appl. Phys. 68 (12), p6304 (1990).

18. " Proceedings of the Third International Conference on Silicon Carbide," Appendix II, p668(1973).

19. H.P. Phillipp and E.A. Taft, "Silicon Carbide, A High Temperature Semiconductor," edited by J.R. O'Connor and J. Smiltens (Pergamon, New York, 1960), p371.

Chapter 5.

1. W. Shockley, A. Goetzberger, and R.M. Scarlett, "Research and Investigation of Inverse Epitaxial UHF Power Transistors," Rep. No. AFAL-TDR-64-207, Air Force Avionics Lab., Wright-Patterson Air Force Base, OH (1964).

2. H.H. Berger, "Models for Contacts to Planar Devices," Solid-State Electron. 15, p145 (1972).

3. D.K. Schroder, "Semiconductor Material and Device Charactization," John Wiley and Sons, p120 (1990).

4. K. Shibahara, T. Saito, S. Nishino, and H. Matsunami, "Fabrication of Inversion-Type n-Channel MOSFET's Using Cubic-SiC on Si(100)," IEEE Electron Device Lett., Vol. EDL-7, No 12, p692 (1986).

5. J.W. Palmour, H. S. Kong and R. F. Davis, " Characterization of Device Parameters in High Temperature Metal-Oxide-Semiconductor Field-Effect Transistors in Beta-SiC Thin Films," J. Appl. Phys. 64 (4), p2168 (1988).

6. S.Y. Chou, Y. Chang, T.W. Sigmon, and J.D. Parsons, "Application of Excimer Laser Processing in SiC Device Fabrication," Amorphous and Crystalline Silicon Carbide and Related Materials II, Springer Proceedings in Physics, Vol.43, Ed.: M.M. Rahman, C.Y.-W Yang and G.L. Harris, p229 (1989).

7. P.G. Carey, K. Bezjian, T.W. Sigmon, P. Gildea and T.J. Magee, "Fabrication of Submicrometer MOSFETs Using Gas Immersion Laser Doping," IEEE Electron Device Lett., Vol. EDL-7, p440 (1986).

8. J.D. Parsons, "Beta-SiC Power Impatt Development: Interim Techincal Annual Report 3" submited to Naval Weapons Center, China Lake, CA, Contract N60530-85-C-0163, p66 (1989).