Synthesis and Characterization of p-n Junction Diodes in β-SiC Epilayers Grown on TiC_x

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To My Parents

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ABSTRACT

Synthesis and Characterization of p-n Junction Diodes in β-SiC Epilayers Grown on TiC_x

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A β-SiC p-n junction fabrication process, including material synthesis, doping calibration, reactive ion etching, oxide passivation and metal contact formation, was developed and characterized.

A metal-organic chemical vapor deposition (MOCVD) system, with an inverted vertical reactor, was designed and built. The MOCVD process, using single reactant source 1,2-disilylethane (DSE or $Si_2C_2H_{10}$), was optimized and used to grow p-n junction structures on TiC substrates. Studies of β-SiC films by Nomarski microscope, scanning electron microscope (SEM) and electron channeling contrast pattern (ECCP) showed that the optimum growth temperatures were in the range of 1240°C to 1290°C, and that the maximum β-SiC epitaxial growth rate was 6μm/hr. The β-SiC epilayers grown under optimized growth conditions were free of antiphase domains and stacking faults.

Electrical properties of undoped and *in-situ* doped β-SiC epilayers were investigated by hot probe measurement, and by I-V and C-V measurements of Ag/β-SiC Schottky diodes. Undoped and nitrogen doped β-SiC epilayers showed n-type conduction.

P-type β-SiC was obtained by *in-situ* aluminum doping. As determined by C-V measurement, the background concentration of undoped β-SiC was about 1×10^{18} cm^{-3}.

Reactive ion etching of β-SiC was performed in $CF_4/O_2/Ar$ and SF_6 plasmas. Etching properties were studied as functions of applied power, total pressure and O_2 concentration. Conditions for etching β-SiC at useful rates (100-1000Å/min.) were established. Studies of β-SiC etching surface morphologies and wall profiles by Nomarski microscope and SEM showed that β-SiC etching was highly anisotropic, and SF_6 etching resulted in much better surface morphology than $CF_4/O_2/Ar$ etching.

Two methods, thermal oxidation of β-SiC and thermal oxidation of a Si/β-SiC structure, were employed to grow SiO_2 on β-SiC for surface passivation. The thermal oxidation of the Si/β-SiC structure included two steps: (1) Si CVD deposition on β-SiC; and (2) thermal oxidation of the Si layer.

Mesa type β-SiC p-n diodes were fabricated by integrating the optimized material synthesis and device processing conditions. I-V characteristics of the β-SiC diodes showed rectification with relatively high reverse leakage current, an ideality factor about 3.5 and series resistance on the order of 1kΩ. Both oxide growth approaches reduced the leakage currents of the diodes. However, Si/β-SiC oxidation appeared to be more effective. The cause of the leakage current was attributed to the high background impurity concentrations in the DSE reactant source and to the subgrains in the TiC_x substrates.

Chapter 1

Introduction

It has long been recognized that β-SiC is a material with tremendous potential for electronic device applications[1-3]. This is based on its many unique features, in particular, its wide band gap, high saturated electron drift velocity, high breakdown field, high thermal conductivity and excellent physical and chemical stability. The combination of these properties makes β-SiC an excellent choice for high temperature, high power and high frequency devices that can operate well beyond the limits of other semiconductor devices.

In recent years, significant progress has been made in β-SiC single crystal synthesis and in device processing[4,5]. Single crystal β-SiC thin films were successfully grown on Si[6], 6Hα-SiC[7] and TiC[8,9] substrates. Device technologies, including doping, reactive ion etching, oxidation and metal contacts were investigated and played important roles in making β-SiC prototype devices.

However, considerable technological difficulties have been encountered in producing high quality β-SiC single crystals and in developing device processes specific to β-SiC. Therefore, in spite of great interest and significant advances in the field of β-SiC electronics, up to now high power, high temperature and high frequency β-SiC devices are still not commercially available.

Further development of β-SiC device technology requires further reductions in defect concentrations in β-SiC epilayers. Substrate choice, among Si, 6Hα-SiC and TiC, is

the critical issue in this effort. β-SiC grown on Si has high defect density because of the large lattice mismatch between Si (a_0=5.4301Å) and β-SiC (a_0=4.3596Å)[10-11]. 6Hα-SiC has a hexagonal crystal structure, while β-SiC has a cubic crystal structure. This fact results in the formation of double position boundary defects in the β-SiC thin film grown on 6Hα-SiC[7]. The properties of Si and 6Hα-SiC have limited the possibility of producing a low defect density β-SiC epilayer. On the other hand, TiC has a lattice parameter mismatch to β-SiC of about 0.7% and a cubic crystal structure. There is no fundamental limit to minimizing defect densities in β-SiC grown on TiC substrates. The successful development of a β-SiC growth process on TiC[8,9] has demonstrated that the device technology based on the β-SiC/TiC structure is a promising approach.

The purpose of this project is to develop the process specifically for fabricating p-n junction diodes in β-SiC epilayers grown on TiC. The major steps involved in this fabrication are:

(1) β-SiC p-n junction structure synthesis by metalorganic chemical vapor deposition (MOCVD) with *in-situ* doping technique;

(2) reactive ion etching to selectively remove β-SiC for diode isolation;

(3) surface passivation by thermal oxidation to reduce possible surface leakage;

(4) ohmic contact formation.

The extensive investigation was performed to determine the optimum conditions of each process step and to integrate these process steps for β-SiC p-n diode fabrication.

This thesis is divided into six chapters including this introduction. Chapter 2 contains a review of β-SiC advantages as a semiconductor material, the recent progress in β-SiC research, and the main difficulties involved in β-SiC electronics device technology. Chapter 3 presents the technical approach to β-SiC material synthesis and the

experimental results of the process optimization. Chapter 4 describes the β-SiC reactive ion etching process development. Chapter 5 consists of the detailed β-SiC p-n diode fabrication steps, and diode characterization results and discussion. Conclusions are presented in Chapter 6.

Chapter 2
Background of β-SiC Device Technology

β-SiC has been of interest as a potential semiconductor material for high performance device applications since the early 1950s. However, systematic studies in the field of β-SiC electronics have been undertaken only in last several years, following successful solution of its synthesis problem[6-9]. It is the purpose of this chapter to review and to discuss the recent development of β-SiC device technology. The crystal structure of β-SiC (Section 2.1) and the advantages of β-SiC as a semiconductor material (Section 2.2) will be presented to provide a basis for choosing β-SiC for device applications. Major advances and associated difficulties in β-SiC material synthesis (Section 2.3) and device processing (Section 2.4) will be reviewed. Electrical performance of β-SiC devices fabricated during the last several years will be discussed (Section 2.5).

2.1. Crystal structures of SiC and β-SiC

Silicon Carbide (SiC) is the only stable chemical compound of carbon and silicon existing in the solid phase. It crystallizes in one of the four crystal structures[12-14]: cubic(C), hexagonal(H), rhombohedral(R) and trigonal(T). The cubic form of SiC is a zincblende structure and is known as β-SiC; the other three crystal structures of SiC are all known as α-SiC.

An unusual aspect of SiC is that it exhibits the phenomenon of polytypism[13]. Polytypism is characterized by a repeat stacking sequence of close-packed planes of atoms[15]. In SiC, a specific polytype is identified according to the stacking sequence of

double layers of Si and C atoms. Each double layer consists of a plane of close-packed Si over a plane of close-packed C. Only three possible relative positions for the double layers are allowed in a close-packed stacking arrangement. These positions are normally labeled A, B, and C. The cubic form of SiC (β-SiC) has only one possible stacking sequence, ABC. For the other three crystal structures of SiC (α-SiC), more than 170 stacking sequences have been identified in all. The most common SiC polytypes are listed in Table 2.1. In the notation of each polytype, the number preceding the crystal structure designator (C, H, or R) is the number of double layers in a stacking repeat sequence.

Table 2.1. Selected SiC Polytypes.

	Notation	Stacking Sequence
(cubic or beta)	3C	ABCABC...
(alpha)	2H	ABAB...
	4H	ABACABAC...
	6H	ABCACBABCACB...
	15R	ABCBACABACBCACB...

Different types of SiC have similar physiochemical properties, but different bandgap energies and electrical properties[16]. In order to address the merit for electronic device applications of SiC, we must specify its crystal structure and its polytype. β-SiC and 6Hα-SiC are the two most important types of SiC. Almost all reported SiC semiconductor development work is focused on these two SiC structures.

2.2. Advantages of β-SiC as a semiconductor material

β-SiC has the potential to become the most important semiconductor since Si. This potential is due to the many outstanding properties of β-SiC which are important for advanced electronic device and integrated circuit performance.

β-SiC is a primary candidate for high temperature, corrosion and radiation resistant device applications. Si and other commercial semiconductors have met very limited success in these areas. Si devices cannot be used at temperatures in excess of 300° C in any environment. Most corrosive species etch or easily diffuse into Si and thereby change its semiconductor properties at temperatures as low as 100°C. III-V and II-VI materials have severe stability problems at high temperature. On the other hand, β-SiC devices can operate at temperatures up to 600°C because of the wide bandgap (2.35eV)[17,18] and excellent physical and chemical stability of the material. The intrinsic carrier concentration of β-SiC does not exceed 10^{14} cm^{-3} at 1100°K. High Si-C bonding energy in silicon carbide (~5eV) makes it resistant to corrosion and radiation. The low diffusion rates of dopants and host atoms in β-SiC make it an ideal diffusion barrier. Owing to these properties, β-SiC devices can operate in hostile environments for extended periods of time with excellent reliability.

Furthermore, β-SiC has tremendous advantages for high power, high frequency and high speed device applications because of a unique combination of its properties. Table 2.2 presents a comparison of the important material properties and device parameters for β-SiC, Si, GaAs and 6Hα-SiC.

β-SiC or 6Hα-SiC has a larger bandgap energy (E_g) than Si and GaAs as shown in Table 2.2. This allows SiC to accommodate higher current density (J). Its device characteristics are less sensitive to elevated temperatures and it is less susceptible to

thermal runaway. Large bandgap energy also imparts to SiC a high breakdown electric field (E_B), which is desirable for power devices. The primary importance of E_B in power switches is to maximize the reverse blocking voltage or to reduce the channel length required to block a given voltage. In high frequency power FETs, however, the high value of E_B allows smaller device dimensions for a given power output.

Thermal conductivity (σ_T) is a limiting factor in the duty cycle and maximum packing density of high frequency, high power devices. SiC has a clear advantage over Si and GaAs in this regard, as shown in Table 2.2. In qualitative terms, β-SiC or 6Hα-SiC can dissipate 3.3 times more power than Si and 10 times more power than GaAs for the same cooling.

The dielectric constant (κ) of a semiconductor is important to high frequency device operation through its effect on the dielectric relaxation time. This is because the amount of charge required to set up a given potential is directly proportional to κ. In contrast to a dielectric constant of 11.8 for Si and 12.8 for GaAs, SiC exhibits a dielectric constant only 9.7. This lower value significantly reduces capacitive parasitic losses associated with the charging/discharging of transmission lines in circuits fabricated of SiC, and enables the reduction in size of the transistors needed to drive electrical signals down the microminiature transmission lines interconnecting the transistors on chip and between chips. The decreased size further reduces power requirements and reduces power supply size and cost.

Small devices generally operate at higher electrical fields where the maximum operating frequency depends on saturated drift velocity (v_s). β-SiC has a theoretical v_s of approximately 2.5×10^7 cm/sec, which is superior to Si, GaAs and 6Hα-SiC.

Low field mobility (μ) is important in the active and contact regions of a power device, and plays an important role in the high frequency limits of a device. The reported values of mobility for β-SiC and 6Hα-SiC have considerable uncertainty (shown in Table 2.2) because of variations in material quality. However, it is believed that β-SiC has a higher mobility than 6Hα-SiC. This is the most important advantage of β-SiC over 6Hα-SiC. β-SiC may have a mobility close to that of Si, which is suitable for most applications. The more important fact is that β-SiC has a higher Debye temperature than Si or GaAs as shown in Table 2.2. This means it will experience much less mobility reduction per unit temperature increase. β-SiC devices are able to perform with near optimum characteristics beyond power levels and duty cycles that would initiate thermal runaway in Si and GaAs.

In today's semiconductor industry, designers have pushed temperature and power capabilities of existing commercial semiconductors, such as Si and GaAs, almost to the limits imposed by their fundamental material properties[40]. On the basis of the above discussions, it is obvious that β-SiC is the material of choice to meet the additional requirements of advanced device applications.

Table 2.2. Comparison of important properties of β-SiC, Si, GaAs and 6Hα-SiC for electronic applications.

Properties(300°K)		Units	β-SiC	Si	GaAs	6Hα-SiC	References
Bandgap Energy		eV	2.35	1.12	1.43	2.86	17-19
N-type Dopant E_d		meV	20	39	6	63	19-21
P-type Dopant E_a		meV	160	45	26	210	19,21,23,24
Drift	Electrons	cm^2 v-sec	> 800	1380	8500	≤ 400	19,25,26
Mobility	Holes	cm^2 v-sec	?	495	400	?	19, 25
Hall	Electrons	cm^2 v-sec	750-4670	1500	9000	400-607	19,22,27-31
Mobility	Holes	cm^2 v-sec	50-650	450	450	50	19,31,32
Breakdown Electric Field E_B		v/cm	$>5x10^6$	$3x10^5$	$4x10^5$	$> 5x10^6$	19,33
Saturated. Drift Velocity(e^-) v_s		cm/s	$2.5x10^7$	$1x10^7$	$2x10^7$	$2x10^7$	19,27,34,35
Dielectric Constant κ ($\varepsilon_s/\varepsilon_0$)			9.7	11.8	12.8	≥ 9.7	36
Thermal Conductivity σ_T		w/cm °K	4.9	1.5	0.5	4.9	37
Debye Temperature		°K	1430	636	360	1270	12,38,39

2.3. β-SiC material synthesis

High performance β-SiC device fabrication requires semiconductor quality material with good crystallinity, and extremely low defect density and background impurity concentration. The difficulty in producing such high quality material has been the main obstacle in β-SiC device technology development.

SiC does not melt at atmospheric pressure, but rather sublimes at temperature above 1800°C[4]. Therefore the conventional melt crystal growth methods, such as the *Czochralski method* [41] and the *floating-zone method* [42], are not suitable for SiC crystal growth. Sublimation process, first developed by Lely in 1955[43], is the only approach which has obtained bulk single polytype SiC. 6Hα-SiC bulk crystals have been successfully produced by a modified Lely sublimation process[44-46]. However, the effort to grow bulk crystal β-SiC by sublimation has been unsuccessful. This is mainly due to the fact that β-SiC tends to convert to alpha SiC polytypes above 1600°C[47], which is much lower than the temperature required by the sublimation process.

The successful synthesis approach for single crystal β-SiC is to grow β-SiC on foreign substrates by chemical vapor deposition(CVD). In recent years, the major efforts have been concentrated on the β-SiC growth processes using Si, 6Hα-SiC and TiC as the substrates. In this section, we will review the development of these processes and discuss the advantages and the difficulties in each process based on substrate choice.

2.3.1. β-SiC growth on Si substrate

Since large area bulk β-SiC substrates were not available, researchers have long tried to grow on other substrates, in particular, on Si. Large area heteroepitaxial growth of β-SiC on Si was first achieved by Nishino *et al.* in 1983 using a two-step CVD process[6].

A "buffer" or "converted" layer is initially formed on a Si substrate surface via a reaction with propane (C_3H_8) followed by the growth of thin films of β-SiC using SiH_4 and C_3H_8. Because single crystal Si substrates are readily available and reasonably inexpensive, this approach was duplicated or modified worldwide [48-53].

Extensive investigation of the β-SiC films grown on Si have indicated problems in film quality. A major problem is a high density of defects. Transmission electron microscopy (TEM) studies have identified misfit dislocations, twins, stacking faults, and antiphase boundaries(APB's) [10,11,54]. The first two are generally found at the interface between the β-SiC and Si or within a few μm of the interface[55]. However, the latter two frequently extend all the way to the surface of the film. The situation is similar to the growth of other polar compounds (e.g. GaAs[56] and GaP[57]) on Si. These defects are generally attributed to lattice mismatch and the difference in thermal expansion coefficients[54,55].

Another problem with the β-SiC films is the apparent high concentration of residual donors and compensating acceptors. Hall measurements indicate that while the net electron carrier concentration in unintentionally doped material is in the low 10^{16} cm^{-3} range, the actual donor and acceptor concentration are about 10^{18} cm^{-3} (i.e. greater than 90% compensation of the donors by the acceptors)[31,58]. The source of the compensating acceptors is unknown.

2.3.2. β-SiC growth on 6Hα-SiC substrate

In the effort to avoid problems caused by lattice mismatch, the use of 6Hα-SiC substrate has been investigated. Single crystal growth was achieved on the basal plane of 6Hα-SiC [(0001) Si face and $(000\bar{1})$ C face][7]. Compared with growth on Si, β-SiC

epilayers grown on the (0001) 6Hα-SiC surfaces contain lower defect density. The only significant defects were double positioning boundary (DPB) defects[59,60].

The DPB defect can be explained as follows. There are six atoms on the surface of the hexagonal basal plane to which depositing atoms can bond. If the depositing atoms nucleate as a cubic structure, then there can be only three bonds attached to the 6 surface plane atoms. Thus, to form a cubic structure, the nucleating atoms must attach to every other atom in the basal plane of the hexagonal lattice. This causes the random nucleation of two β-SiC epilayer orientations. Both orientations are identical perpendicular to the 6H α-SiC substrate, but they are misorientated 60° with respect to each other in the plane of the substrate surface. The DPBs between these two orientations are incoherent and are released by formation of stacking faults. These stacking faults seriously degrade the electronic transport properties of the β-SiC epilayer, and they make the development of lateral integrated circuits highly unlikely.

In an attempt to eliminate DPB defects, the film growth on inclined surfaces was tried. Growth on large area 6Hα-SiC surfaces that were a few degrees off the basal plane yielded homoepitaxial 6Hα-SiC film, rather than β-SiC[61-63]. To obtain β-SiC on inclined 6Hα-SiC wafers, Powell *et. al.* patterned a 6Hα-SiC substrate with $1mm^2$ die sized areas[64,65]. CVD growth on this substrate produced a mixture of $1mm^2$ β-SiC epilayer mesas and 6Hα-SiC epilayer mesas. Most β-SiC mesas were DPB-free. The stacking fault density was also reduced. However, the distribution of β-SiC mesas versus 6Hα-SiC mesas on the wafer was random and uncontrollable. Therefore, this process is not suitable for mass production.

A recent report presents evidence that (001) β-SiC epilayers free of DPB can be grown on the (0114) 6Hα-SiC surface by molecular beam epitaxy[66]. The preliminary data

contained in this report suggest that this may be a viable approach to nucleation of β-SiC, but at this time it is inconclusive as to whether it can yield antiphase domain free β-SiC and good crystalline quality in β-SiC thicknesses required for device applications.

2.3.3. β-SiC growth on TiC substrate

As discussed above, extensive experimental studies have suggested that Si and 6H α-SiC substrates are not suited for high quality β-SiC epitaxial growth. Parsons *et. al.* selected TiC as the substrate for β-SiC epitaxy[67,68] based on its physical properties (detailed in chapter 3). TiC has a lattice parameter mismatch to β-SiC of about 0.7% and a cubic crystal structure (rock salt). There is no fundamental limit to minimizing defect densities in β-SiC grown on TiC substrates.

β-SiC growth on TiC by CVD was demonstrated by Parsons *et al.*[8,9,67,68]. Epitaxial growth was confirmed by the existence of electron channeling contrast patterns (ECCP). Compared to the films grown on Si and 6Hα-SiC substrates, the β-SiC films grown on TiC have much lower defect density and smoother morphology. The main difficulty associated with this approach is to precisely control the Si to C ratio in the gas phase to achieve complete nucleation[68]. To solve this problem, a single reactant source 1,2-disilylethane (DSE or $Si_2C_2H_{10}$), which contains equal numbers of Si and C atoms, was developed for β-SiC growth[8,9]. Use of this reactant source has dramatically improved the growth process, so that controlled, repeatable β-SiC epitaxial growth on TiC has been achieved. Still higher quality β-SiC thin films can be obtained by optimizing the growth process and improving the substrate quality. Therefore, TiC is the best choice for β-SiC epitaxy growth.

2.4. β-SiC device process

β-SiC device process development has progressed along the same lines as that of Si. Some existing techniques used in Si process, such as photolithography, can be applied to β-SiC directly. However, the physical hardness and chemical inertness impose a number of constraints on β-SiC device fabrication techniques. Many techniques have to be developed which are specific to β-SiC and which make the fabrication more complex and difficult. In this section, the major advances in β-SiC device process technologies, including (1) doping, (2) oxidation, (3) reactive ion etching, and (4) ohmic contacts will be reviewed .

2.4.1. Doping

For β-SiC device fabrication, impurity conduction, both n-type and p-type, needs to be controlled over a wide range. In β-SiC, among all the dopant elements nitrogen has smallest donor activation energy E_d (20 meV), and aluminum has smallest acceptor activation energy (160 meV). Boron has an acceptor level of 0.7 eV, and has been used as a compensator to produce high resistivity β-SiC material[69]. The techniques that can be employed to introduce dopants into β-SiC include diffusion, ion implantation and *in-situ* doping during thin film growth.

The solubility and diffusivity of impurities in different SiC polytypes are very similar[15]. Only small size light atoms dissolve markedly in SiC[70-72]. Boron, nitrogen[73] and probably beryllium substitute for carbon atoms, while aluminum, gallium[74] and most other impurity atoms substitute for silicon. Small inter atomic distances and high bond energy result in a low migration ability for dopant atoms in the SiC lattice. The diffusion coefficients for most dopants in SiC are negligible at temperatures below 1800°C[75].

Therefore, diffusion for doping purposes in SiC requires temperature in excess of 1800°C. At these temperatures, material stability and control of junction profiles become problems, so this technique is not recommended.

The process of ion implantation in SiC has been investigated, and appears very complex[76-79]. It leads to changes not only in composition but also in structure of the implanted material, such as damage accumulation, amorphization and polytype transformation. Thermal annealing studies of implanted β-SiC have revealed a number of problems,[76,77] among others (1) incomplete recovery of the crystalline structure; (2) incomplete activation of dopants; and (3) redistribution and/or out-diffusion of dopants away from the implanted layer. To reduce residual damage and eliminate amorphization, β -SiC was implanted at different temperatures. Studies by Edmond *et al.*[78] showed that at 77-1023K, an increase in the substrate temperature during implantation of β-SiC single crystal with Al, N, Si, and C to 10^{13}-10^{15} ions/cm^2 resulted in reduction of lattice damage. Implantation above 623K resulted in structural recovery. In contrast, for room temperature implantation, structural recovery of amorphized β-SiC took place only at 1973-2073K during post-implantation annealing. Further studies on ion implantation in β-SiC are needed to optimize the ion implantation temperature and annealing process.

In-situ doping has been the most successful method of introducing impurities into β-SiC[80]. Either n-type or p-type β-SiC can be obtained by introducing appropriate doping material during growth. For example, during CVD, n-type β-SiC can be grown by adding the doping gas NH_3, and p-type β-SiC can be grown by transferring vapor of a liquid aluminum source into the reactor chamber. One complication of this approach is that a selective growth technique has to be developed for recessed device structures.

2.4.2. Oxidation

Thermal oxidation is one of the most important processes in SiC semiconductor technology. Its role is very similar to that in Si processing. For example, an oxide layer can be used to electrically passivate the surface[81], it can be used as a dielectric layer in an MOS structure[82], and it can serve as a mask for photolithography processes. Oxidation has also been used to remove polishing damage in SiC substrates prior to epitaxial growth[62].

SiC offers higher resistance to thermal oxidation than Si. Under the conditions used in Si oxidation procedures (an oxygen atmosphere, wet or dry, and temperatures 800-1200°C) it takes up to several hours to obtain a sufficiently thick oxide film on SiC. Oxidation rate has been reported to be a function of SiC polytype, crystal orientation, defect density, and doping level[82-89]. An Auger electron spectroscopy (AES) study[85] of the thermal oxides of β-SiC found that the wet thermal oxide is almost stoichiometric but contains about 14% carbon. Dry oxide , on the other hand, has less than 3% carbon but is highly nonstoichiometric due to oxygen deficiency. The growth of SiO_2 on β-SiC follows the generalized linear-parabolic model of Deal and Grove[90]. According to this model, diffusion of either species through a thick oxide is the rate-limiting process resulting in a parabolic law variation of the oxide thickness with time. The growth of thick oxide films is considered to be limited by diffusion through the film of CO produced in a chemical reaction of carbon and oxygen. On the other hand, the growth of thin oxide films (short oxidation times) is limited by the oxidation kinetics at the oxide/semiconductor interface. In this case the oxide thickness increases linearly with time. The activation energy of the linear rate constant varies with the polytype and orientation. It is found that for β-SiC(100) layers this energy is approximately 74 kCal mol^{-1} [89].

2.4.3. Reactive ion etching

In order to fabricate β-SiC devices, selective surface removal and mesa etching are required. Chemical etching of β-SiC can only proceed at high temperatures. β-SiC has been etched[91,92] by molten salts at 500° C, by high temperature gaseous etching (in chlorine or chlorine-containing gases at 1000°C or in H_2 at 1300°C), and by electrolytic etching. However, these methods are not suitable for the fabrication of devices, especially at the micron and sub micron level. Hence, alternate methods for dry etching of β-SiC have been under extensive investigation in recent years.[93-98]

The main requirements of the etching process, when used to make a device, are as follows: (i) low temperature, (ii) high quality of the surface treatment, (iii) high selectivity of etching with respect to the mask material and (iv) high resolution and anisotropy.

Studies of reactive ion etching in fluorine-containing gases, such as CF_4, CF_4+O_2[93-95] , SF_6[96], $CHF_3+O_2+H_2$[97], and NF_3[98], have shown that this method can produce usable etch rates (~10-100 nm/min) with a high degree of etching anisotropy. The basic mechanism for the β-SiC etching process in fluorinated plasma consists of a combination of chemical (reaction with F and O) and physical (energetic ions) removal processes. Studies of reactive ion etching of β-SiC in CF_4+O_2 plasma discharge show that etch rate is a function of the percentage of O_2 in the gas mixture. A maximum etch rate was found at 40% O_2 by Padiyath *et al.*[94], and at 69% O_2 by Dohmae *et al.*[95]. Padiyath *et al.*[94] compared the reactive ion etching of monocrystalline β-SiC, polycrystalline β-SiC and hydrogenated amorphous α-SiC:H in CF_4+O_2 mixtures. The degree of crystallinity has a strong influence on the etch rate of SiC at all compositions of the CF_4+O_2 etchant mixture. The monocrystalline β-SiC had the lowest etch rate and the α-SiC:H had the highest etch rate at any concentration of oxygen. Etching SiC in pure

CF_4 resulted in a "thick carbon-rich layer" due to the inefficiency of carbon removal by fluorine atoms.[93] Since the carbon-rich layer resisted oxidation even at 1437K and did not etch in hot HNO_3, it was assumed to be residual SiC with a C-rich surface. Kelner *et al.* reported that etching of β-SiC in SF_6 plasma showed no carbon residue on the surface when examined by Auger electron energy spectroscopy[96]. Steckl *et al.* found that while using Al as etching mask, a low-level(~10%) addition of H_2 in CHF_3+O_2 can prevent the formation of residues in the etched regions[97].

2.4.4. Ohmic contacts

One of the key problems in β-SiC device technology is the production of highly stable low-resistance ohmic contacts. Devices capable of continuous operation at temperatures approaching 600°C place several restrictions on the metal used to form the ohmic contacts. First, the metal must have a high softening temperature. The second and probably the more difficult requirement is that the metal must form a contact that has low resistance and does not change significantly during high temperature operation. Thus, the metal/β-SiC interface has to be both physically and chemically stable at elevated temperatures in order to insure electrical stability.

Contact systems based on refractory metals, such as nickel[99], titanium[100], tantalum[100], tungsten[100-102] and molybdenum[102], have been chosen for β-SiC ohmic contact studies because refractory metals usually have high melting temperatures, and are capable of forming carbides and silicides to achieve better adhesion of the contact metal. Studies have demonstrated that physical and chemical properties and electrical characteristics of the contacts are affected by the following factors: (1) enrichment of the β-SiC surface with either Si or C as a result of various treatments; (2) orientation and

doping level of the substrate; (3) temperature and duration of the anneal of the deposited metals. High stability was exhibited by W/β-SiC and Mo/β-SiC contacts. According to Auger electron spectroscopy interface studies, no appreciable changes occurred in the interfacial chemistry in the W/β-SiC and Mo/β-SiC systems up to annealing temperatures of 800°C and 850°C, respectively[102]. The Au/W/β-SiC system has the lowest reported contact resistance value, $8x10^{-4}$ ohm-cm^2 for n-type β-SiC ohmic contact, and also showed good electrical stability in thermal cycling tests at 600°C[100].

Instead of using elemental metals, direct deposition of carbide or silicide on β-SiC was investigated by Parsons *et al.*[103-105] for the purpose of achieving better stability and lower contact resistance. The results of experimental studies show that TiC is the preferred contact material to n-type β-SiC. TiC is a low resistivity semi-metal which lattice matches β-SiC. A TiC layer can be deposited on β-SiC either by epitaxial growth or by sputtering from a TiC target. The TiC/β-SiC interface was demonstrated to be stable at temperatures up to 800°C at Hughes Research Labs (HRL)[105] and at Nortre Dame[106]. Preliminary measurements made at HRL show that contact resistance of TiC to epitaxial n-type β-SiC is less than 10^{-5} ohm-cm^2, which is better than other contact systems. For p-type β-SiC ohmic contacts, PtSi has been suggested as a preferred choice. Pt exhibited good contact behavior. However, the Pt contact was not stable at elevated temperatures because of silicide formation. Direct deposition of PtSi would offer much better interface stability so that better electrical stability could be achieved.

2.5. β-SiC device fabrication

In the last few years, various prototype devices have been demonstrated in β-SiC. They are Schottky diodes[107-111], p-n junction diodes[77,112-116], and field effect transistors (FETs)[117-124]. The electrical parameters of these devices (leakage current, breakdown voltage, diode ideality factor and FET transconductance) are very sensitive to the presence of various structural defects, and therefore they are considered good indicators of the quality of β-SiC fabricated by different technologies.

Great expectations were associated with the technology for fabrication of heteroepitaxial β-SiC/Si structures. However, research along these lines has shown that high defect densities in the epilayer have prevented fabrication of high quality β-SiC devices.

Investigations of Schottky rectifying contacts on β-SiC/Si involved Au[107-110] and Pt[111]. Yoshida *et al.*[107] and Edmond *et al.*[108] reported a barrier height of 1.15eV for Au contacts on chemically prepared n-type β-SiC surfaces. A subsequent study of thermally treated Au Schottky contacts on β-SiC showed that the rectification characteristics of these diodes degraded at temperatures as low as 350°C[109,110]. Another problem associated with Au contacts is the poor adhesion of the metal to the β-SiC, which makes the contacts susceptible to scratching and peeling during processing and probing. Pt/n-β-SiC Schottky rectifying contact were demonstrated by Papanicolaou *et al.*[111]. Rectification characteristics were observed after post-deposit thermal treatment in the range 450°C-800°C. As the annealing temperature increased, the barrier height increased from 0.95 to 1.35 eV. This fact was attributed to the formation of $PtSi_x$ and PtC at the Pt/ β-SiC interface. For Au and Pt Schottky diodes, high reverse leakage currents were

exhibited and the ideality factor remained definitely larger than 1 under all thermal treatment conditions.

β-SiC p-n diodes in β-SiC/Si structures were fabricated using high temperature ion implantation[77,112] or *in-situ* doping[113,114] techniques. These diodes were very leaky, exhibiting milliampere per square centimeter current densities at less than 10-V reverse bias. Studies by Edmond *et al.*[112] and Avila *et al.*[77] on the ion implanted diodes showed that the devices possessed characteristics that could not be satisfactorily explained in terms of the ideal current mechanism. In particular, the forward I-V curve showed an ideality factor n>2, which depended on both current and temperature. The reverse current of the diodes revealed a power-law dependence on voltage, with a component resulting from thermal generation of carriers within the space-charge region ($J \sim V^{1/2}$). From these observed current-voltage characteristics, a model of space-charge limited currents was suggested and the presence of high concentrations of shallow and deep traps was assumed.

High defect densities were also believed to result in the poor performance of β-SiC FETs produced in β-SiC/Si structures.[117-123] The best device had a transconductance of 0.64 mS/mm and low drain-source voltage of 5-8V, which is far inferior to typical Si transistors.

Improved β-SiC devices were fabricated in β-SiC/6Hα-SiC structures, which have lower defect densities than β-SiC/Si structures[116,124]. An n-channel depletion-mode MOSFET fabricated by Palmour *et al.*[124] exhibited stable saturation and low subthreshold current at drain voltages exceeding 25V. Stable transistor action was observed at temperatures up to 923K, a maximum value for solid-state devices of any type. Another instance of good β-SiC device performance is a p-n junction fabricated by Neudeck *et*

al.[116] in a selected small area of a β-SiC/6Hα-SiC structure. A 6Hα-SiC substrate with low tilt angle from basal plane was patterned with $1mm^2$ die sized areas. CVD growth on this substrate produced a mixture of $1mm^2$ β-SiC epilayer mesas and 6Hα-SiC epilayer mesas. Some DPB-free epitaxial β-SiC mesas were obtained. β-SiC p-n diodes fabricated on these sites show rectification to 200V, and exhibit substantial improvements in reverse leakage and forward saturation current densities over previously reported β-SiC. Although at present, the distribution of good β-SiC mesas on the wafer is random and uncontrollable, and growth areas are limited, improved performance of β-SiC p-n diodes is clear evidence of the importance of material quality.

Chapter 3

β-SiC Epitaxial Growth on TiC_x Substrate

A successful material synthesis technique is the key for β-SiC device technology development. The approach used in this work is to epitaxially grow β-SiC on TiC substrates, using 1,2-disilylethane (DSE or $Si_2C_2H_{10}$) as the reactant source, in an inverted-vertical MOCVD reactor. Growth process development and optimization are described in this chapter. The included subjects are the MOCVD system description (section 3.1); the TiC substrate properties and preparation procedures (section 3.2); the β-SiC CVD growth process optimization (section 3.3); and *in-situ* doping of β-SiC and carrier concentration determination (section 3.4).

3.1. MOCVD system design and construction

In an effort to produce high quality β-SiC thin films and device structures, we designed and built an atmospheric pressure metalorganic chemical vapor deposition (MOCVD) system, as schematically shown in Fig. 3.1.

The design of the MOCVD system is dictated by the nature of the sources used in the crystal growth. A reactant source can be either in gas phase or in liquid phase. Usually, a gas type reactant source is contained in a high pressure cylinder, and a liquid source is stored in a stainless steel bubbler, which is kept in a temperature controlled bath to maintain constant liquid vapor pressure. The method of transport for a liquid reactant source is to have H_2 gas bubble through the liquid, saturate with the vapor, and carry the

vapor to the reactor. The amount of the liquid source transferred can be calculated by knowing the H_2 flow rate and the vapor pressure of the source at the bath temperature. The reactant sources installed in our MOCVD system are listed in Table 3.1. A single reactant source 1,2-disilylethane (DSE or $Si_2C_2H_{10}$) is used for β-SiC epitaxial growth. Ammonia (NH_3), dimethylaluminum hydride (DMAH or $Al_2C_2H_7$) and diborane (B_2H_6) are selected for *in-situ* doping to produce n-type, p-type and high resistivity β-SiC, respectively. The system also has the ability to grow TiC using $TiCl_4$ and C_2H_4, and Si using SiH_4. A TiC epitaxial layer grown on the TiC substrate serves as a buffer layer in the β-SiC growth process (see section 3.2). Si deposition is one of the surface passivation steps in β-SiC p-n diode fabrication (see chapter 5). Among all the reactant sources, $Si_2C_2H_{10}$, $Al_2C_2H_7$ and $TiCl_4$ are in liquid form, and the others are in gas form.

Table 3.1. Selected reactant sources in β-SiC MOCVD system.

Purpose	β-SiC growth				TiC growth		Si growth
	β-SiC growth	n-type doping	p-type doping	high ρ doping			
Reactant source	$Si_2C_2H_{10}$ (DSE)	NH_3	$Al_2C_2H_7$ (DMAH)	B_2H_6	$TiCl_4$	C_2H_4	SiH_4
Source type (stored temp.)	liquid (0°)	gas (R.T.)	liquid (15°C)	gas (R.T.)	liquid (15°C)	gas (R.T.)	gas (R.T.)

The fundamental requirement for the CVD process is to deliver appropriate reactant sources to the reactor in a controlled manner. Timing and composition of the gas entering the reactor is the primary determinant of the physical composition and structure of the growing layer. In addition, the leak-tight integrity of the system is essential when

mixing and transporting these reactant sources. Oxygen contamination of the growing film inevitably leads to degradation of the film properties. To insure cleanliness and integrity in the β-SiC MOCVD system, all plumbing is 316 stainless steel and all joints are welded or high vacuum VCR connections using stainless steel gaskets. The system has a leak integrity of better than 10^{-9} cc/min helium. Gas purifiers are installed in all gas lines to reduce impurity concentrations of the gases.

Precise gas flow control is accomplished by using regulators to maintain the gas pressures and using electric mass flow controllers (MFC) to meter the gas flow rates. As shown in Fig. 3.1 a two-stage regulator is used to control the outlet pressure of a gas cylinder, where the downstream, low pressure, stage is employed to maintain a constant inlet pressure to a MFC which controls gas flow from the gas cylinder to the reactor. In each liquid reactant source line, a second single stage regulator is used in series with the H_2 gas cylinder regulator to control inlet pressure of the MFC which controls the H_2 flow through the liquid bubbler. The reason for the second regulator is to prevent pressure fluctuations from occurring when two or more liquid source lines are fed by the H_2 carrier gas. The inlet manifold of the system has a run-vent configuration, which allows for the development of a steady-state flow of gas to a vent line prior to its introduction into the feed flow to the reactor. During the growth, the appropriate reactive process gases are directed to the feed flow, further diluted by H_2 carrier gas, mixed, and subsequently introduced into the reactor.

A special feature of the β-SiC MOCVD system is the water-cooled inverted-vertical (i-v) reactor, as shown in Fig. 3.2. This reactor configuration provides a true stagnation point flow pattern, theoretically ideal for achieving the best possible uniformity over the largest possible area, at atmospheric pressure. In addition, it eliminates

backstreaming eddy currents by allowing the natural buoyancy of hot gases to cause them to exit the reactor at high velocities[125,126]. Experimental results from GaAs growth using the same reactor configuration showed uniformity of thickness and carrier concentration of better than ±0.1% over the growth surface of a 2 inch diameter substrate[126].

In the i-v arrangement, the substrate is supported by placing it, growth face downward, on a graphite mask which rests on the inside bottom of a high purity pyrolytric boron nitride (PBN) cup ("pedestal"). The pedestal is coaxially supported within the reactor by a support collar which rests on a pedestal supporting ring fused to the inside wall of the reactor chamber. An induction heated graphite susceptor rests on top of the back side of the substrate. Two PBN heat shields are mounted over the graphite susceptor, between the susceptor and the pedestal vertical wall, to reduce heat loss. During a growth, carrier gas and gaseous reactant sources enter from bottom of the reactor. After the reactant source pyrolysis, the gaseous reactant products are pushed radically outward until they reach the edge of the pedestal, the pressure gradient in the reactor and buoyancy carry the reactant products upwards, through the annular volume between the outer pedestal wall and the inside wall of the reactor chamber. The reactant products exit this volume through holes at the top of the pedestal, after which they exit through the exhaust port in the reactor cap.

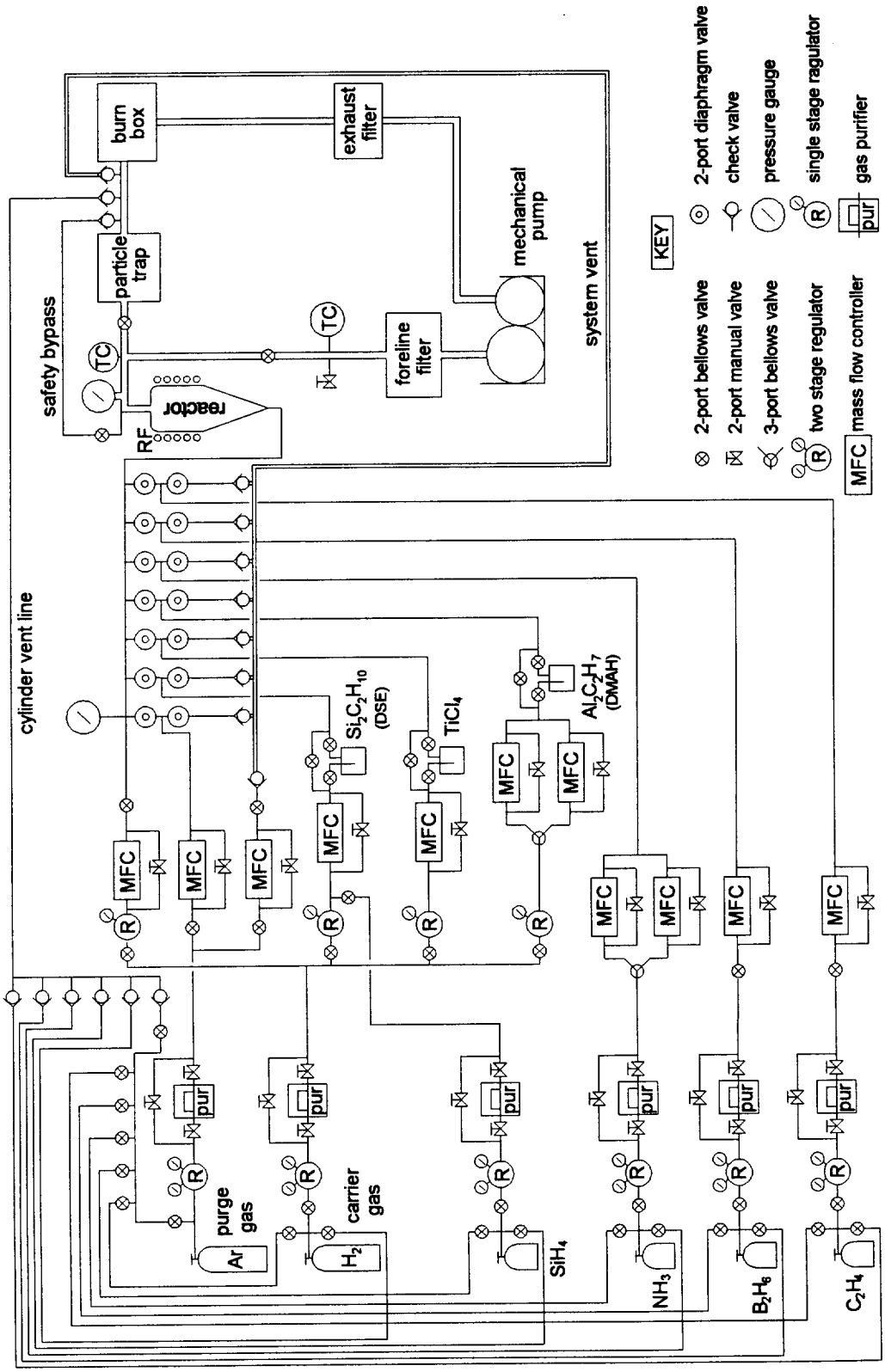


Fig. 3.1. Schematic diagram of β-SiC MOCVD system.

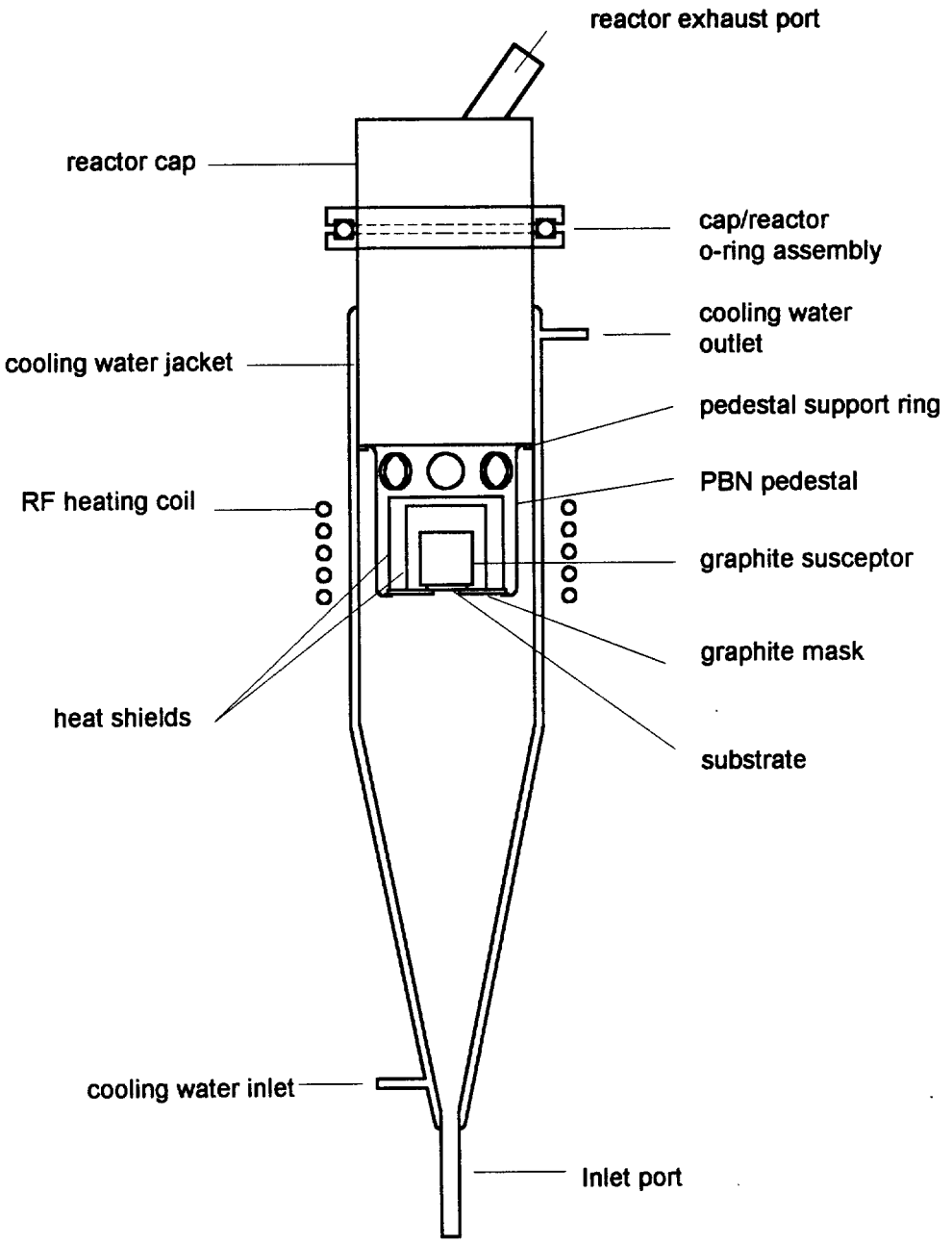


Fig. 3.2. Cross-sectional view of inverted-vertical CVD reactor tube.

3.2. Titanium carbide substrate preparation for β-SiC epitaxial growth

3.2.1. Substrate choice and properties of titanium carbide

The substrate choice is one of the most important issues in the β-SiC epitaxial growth process. As discussed in chapter 2, β-SiC grown on Si has high defect density because of the large lattice mismatch between Si and β-SiC. 6Hα-SiC has hexagonal crystal structure, while β-SiC has a cubic crystal structure. This fact results in the formation of double position boundary defects in the β-SiC thin film grown on 6Hα-SiC. The fundamental properties of Si and 6Hα-SiC substrates have limited the possibility of improving the quality of β-SiC epilayer. The key to epitaxial growth of semiconductor device quality β-SiC therefore lies in choosing a substrate that possesses physical properties favorable to β-SiC epitaxy.

The most favorable situation for β-SiC nucleation and growth on a foreign substrate is obtained when: (1) the lattice parameter mismatch is ≤ 1%; (2) crystal structure is cubic; (3) the thermal expansion coefficient (α_t) of the substrate closely matches that of β-SiC; and (4) the substrate is chemically and thermally stable in the β-SiC epitaxial growth environment.

Based on above criteria, TiC has been chosen as a substrate for β-SiC epitaxial growth in this work. As illustrated in Table 3.2, the lattice parameter of TiC is close to that of β-SiC. At room temperature, the lattice mismatch between TiC and β-SiC is less than 0.7%. TiC has cubic structure (rock salt). This offers flexibility of growth orientation and reduces interface defect density. The melting temperature of TiC (3150°C) exceeds the sublimation temperature of β-SiC (~1800°C). The growth temperature of β-SiC is below 1400°C. The thermal expansion coefficient (α_t) of TiC does not closely match that

of β-SiC. Some thermal stresses at the growth interface may occur. However, the fact that α_t(TiC) is larger than α_t(β-SiC) reduces the chances of epilayer cracking because of the epilayer is compressionally loaded. Overall, the properties of TiC are well within the limits of epitaxial single crystal growth requirements.

Table 3.2. Physical properties of β-SiC and TiC.

	Lattice parameter (300K)	Crystal structure	Melting point	Thermal expansion coefficient (300K)
β-SiC	4.3596 Å	cubic (zincblende)	sublimes at >1800 °C	2.77×10^{-6} K^{-1}
TiC	4.328 Å	cubic (rock salt)	3150 °C	7.4×10^{-6} K^{-1}
Reference	127,128	127,128	127,128	128,129

Furthermore, TiC is a semimetal with very low work function (~ 2.7 eV). TiC/β-SiC can form ideal ohmic contact for a vertical device structure. The thermal conductivity of TiC is higher than that of β-SiC, which ensures effective heat dissipation from the β-SiC device through the substrate. TiC is stable at elevated temperatures in H_2 or inert gas environments, but not stable in oxygen at the temperatures above 500°C.

3.2.2. Titanium carbide substrate evaluation and preparation

Titanium carbide has been determined to be a preferred substrate for β-SiC epitaxial growth. However, the success of this synthesis approach largely depends on the quality of the TiC substrate. At present, TiC substrates are not commercially available. Development of the TiC crystal growth process is underway. TiC substrates available to

us were produced by an unoptimized growth process[130-132]. They are usually nonstoichiometric with C deficiency, thus referred to as TiC_x ($x<1$). The crystal quality of each piece of TiC_x is unpredictable. Therefore, evaluation and preparation of TiC_x substrates is a critical step in β-SiC growth process.

3.2.2.1. Problems of current TiC_x

The problems of current TiC_x are mainly related to its defects. The structural defects that are often found in current TiC_x substrates are pits, grain boundaries and subgrain boundaries[133].

Pits in TiC_x are usually attributed to impurity precipitates or pinholes, which can be caused by precipitate removal during etching or by incomplete densification of TiC_x rods. β-SiC does not nucleate at these pit sites, and this results in pinholes in the β-SiC epilayer. These pinholes provide electrical shorting paths to the conducting TiC_x substrate which make device processing impossible.

A grain boundary is an interface at which the crystallographic orientation changes. If the change in orientation is on the order of 1°, then it can be detected by grain boundary etching and subsequent inspection by optical microscope. Subgrains are grains within the grains described above. The orientation changes at the boundaries of subgrains are on the order of 0.1°. The number of subgrains that constitute a grain can be anywhere from 2 to several hundred, and can be detected by X-ray rocking curves. Possible causes of subgrain growth are constitutional supercooling and cellular growth.

Device fabrication can be achieved within a grain as long as the grain size is larger than the device structure. However, subgrains are simply too small. There is very high probability that the device structure will cross subgrain boundaries, and thus provide

electrical shorting paths to the conductive TiC_x substrate. Further, it is impossible to deliberately miss subgrain boundaries during processing because they cannot be seen by microscopic inspection of the β-SiC epilayers. A very low subgrain density is therefore a primary requirement for the TiC_x substrate which will be used for β-SiC device structure growth.

3.2.2.2. TiC_x substrate annealing

In order to improve TiC_x crystal quality, especially to reduce subgrain density, an annealing treatment was performed before use as a substrate for β-SiC epitaxial growth. As mentioned above, the possible causes of subgrain growth are constitutional supercooling and cellular growth, which can result in accumulation of C vacancies to form subgrain boundaries. Reduction of C vacancy density will probably reduce the subgrain density. Therefore, the annealing treatment was designed to heat TiC_x in a C environment so that C could diffuse into TiC_x. As shown in Fig. 3.3, a TiC_x sample was sandwiched by two high purity graphite wafers and placed on a graphite block. Heating was accomplished by having current pass through the graphite block in an argon atmosphere. Sample temperature was read by optical pyrometer through a window on the process chamber. The typical annealing condition was to keep TiC_x sample at 2300°C for 24 hours.

The effects of TiC_x substrate annealing were studied by comparing Laue pictures and rocking curves of the TiC_x substrates obtained before and after annealing. It was found that through the annealing process, the crystallinity of the TiC_x substrates was improved as clearly shown in the Laue pictures in Fig. 3.4. Note that the mosaic appearance in the before anneal pattern has nearly vanished in the after anneal pattern. The

annealing also resulted in reduction of the subgrain densities in the substrate. In Fig. 3.5, a comparison of the rocking curves before and after annealing is displayed. The number of the peaks in a rocking curve corresponds to the number of the subgrains in a single crystal. However, Fig. 3.5 represents one of the few TiC_x samples whose subgrain density was greatly reduced through the annealing process. In most cases, the annealing treatment only resulted in Laue picture improvement, but had little effect on subgrain density reduction.

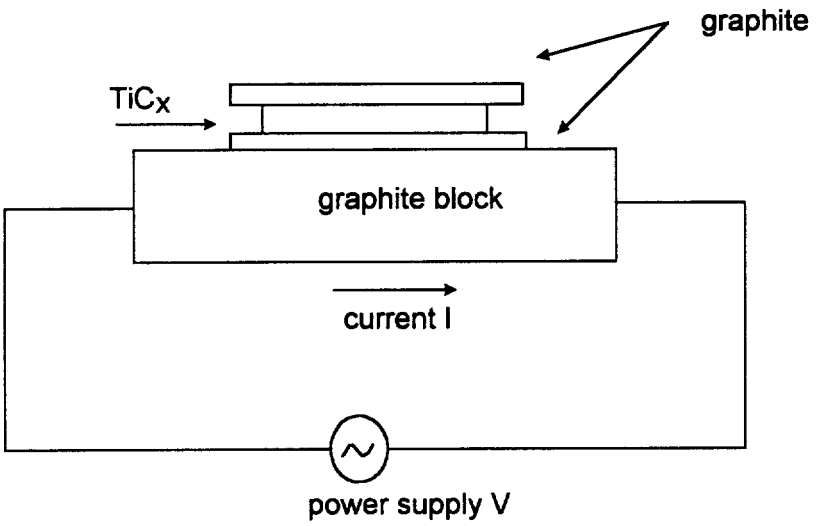
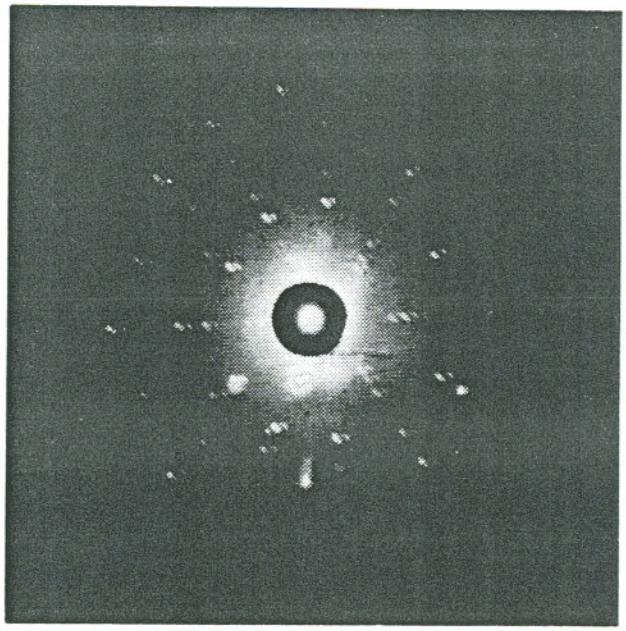
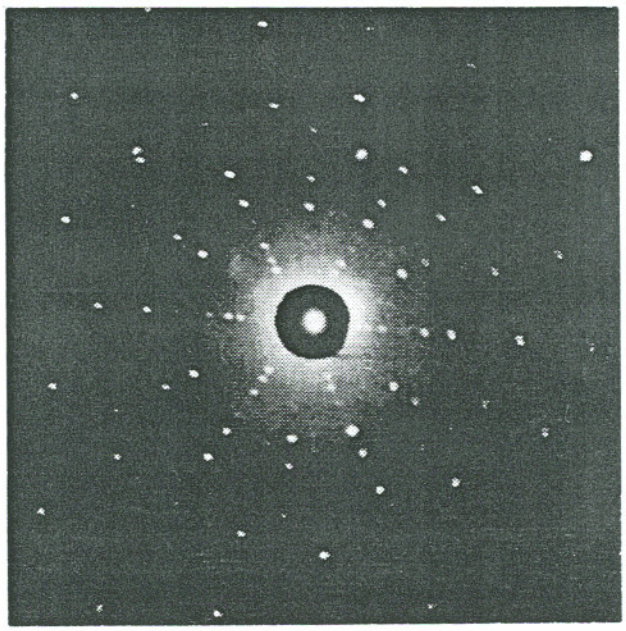


Fig. 3.3. TiC_x annealing set-up.

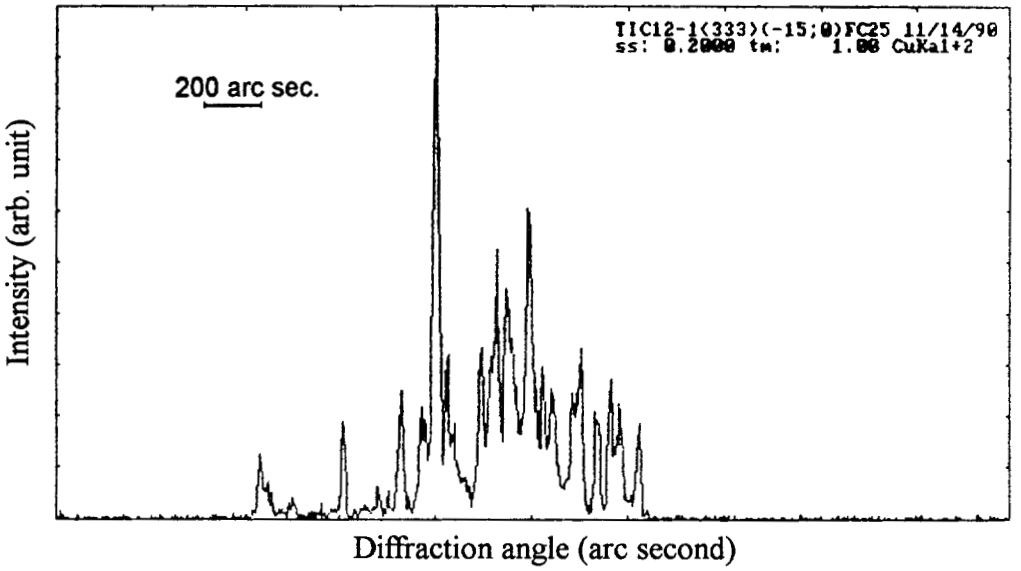


(a)

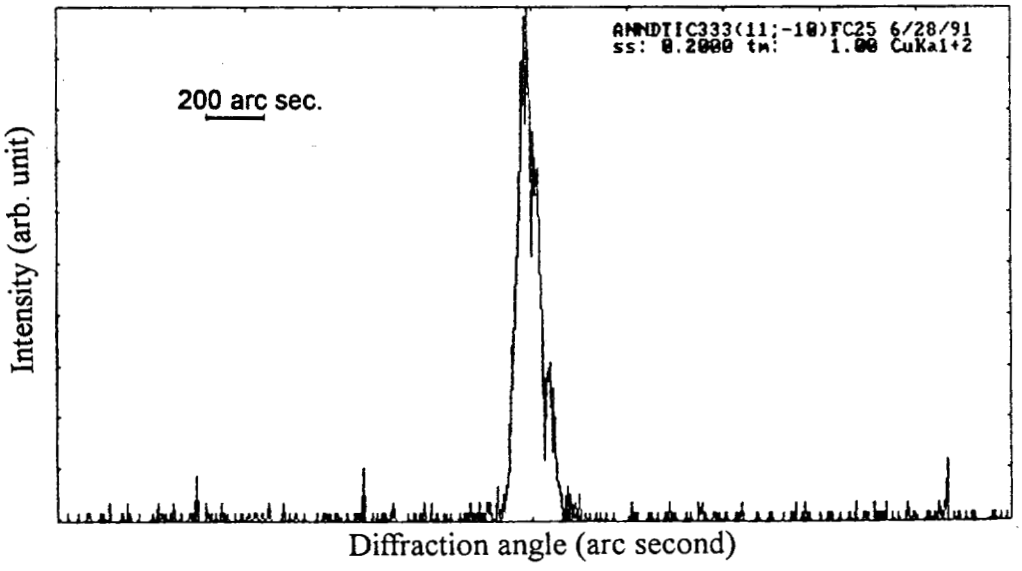


(b)

Fig. 3.4. X-ray Laue pictures of a TiC_x substrate taken before (a) and after (b) annealing treatment.



(a)



(b)

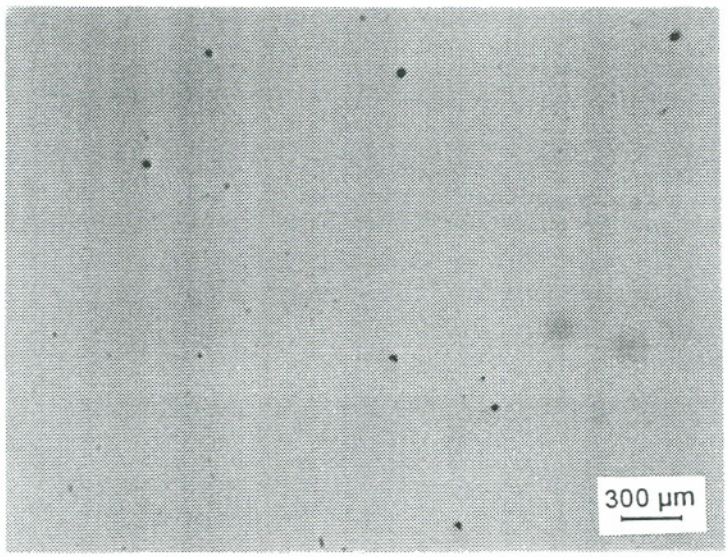
Fig. 3.6. X-ray rocking curves of a TiC_x substrate taken before (a) and after (b) annealing treatment.

3.2.2.3. TiC_x substrate evaluation and preparation procedures

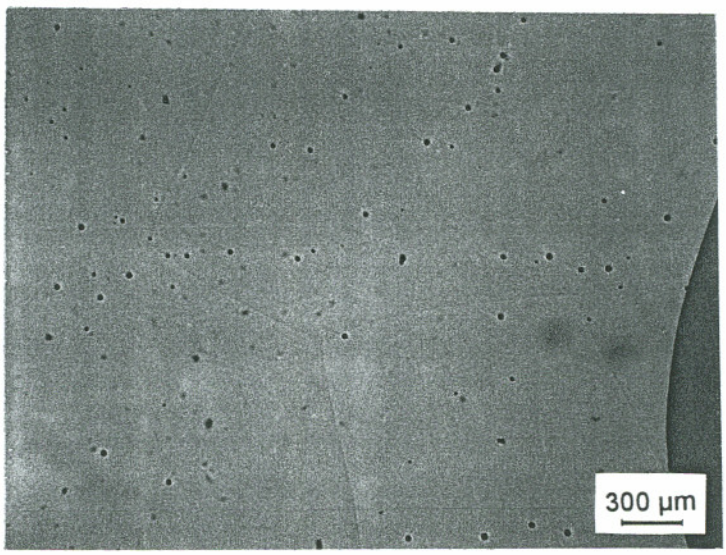
The purpose in evaluating TiC_x is to choose suitable TiC_x for β-SiC device structure growth. Grain size and pit density were first determined by visual or optical microscope examination. Typically, the shapes of the TiC_x substrates are irregular. The size of TiC_x used for β-SiC growth varies from 30 to 70 mm^2. Usually, there are pits, non uniformly distributed on TiC_x surfaces, as shown in Fig. 3.6. The pit density varies from ~ $10^{-3}/mm^2$ to ~$10^2/mm^2$. Grain boundaries are clearly visible on polished TiC_x surfaces, as shown in Fig. 3.6(b). TiC_x substrates containing areas with pit density less than $10^{-2}/mm^2$ and grain size larger than 10 mm^2 were considered to be suitable for β-SiC device structure growth.

For each TiC_x, a Laue diffraction pattern was taken to determine the crystal orientation and an X-ray rocking curve was recorded to identify the subgrain density. The orientations of the available TiC_x substrates, determined by x-ray Laue pictures, are in a very wide range. TiC_x substrates are cataloged into four groups according to their orientation: (1) [111]; (2) [111] 5°-7° toward [100]; (3) [111] 14°-17° toward [110]; (4) [111] 13°-15° toward [100]. More than one grain is often found in a single TiC_x substrate. The orientation difference between these grains varies from 1° to 20°.

The TiC_x substrates with large grain size and low pit densities were annealed as described above in order to improve their crystal quality. To investigate the effects of annealing treatment, x-ray Laue pictures and rocking curves were taken both before and after annealing. Finally, TiC_x substrates with large grain size, low pit density, clear Laue pattern and relatively low subgrain density were chosen to grow β-SiC device structures. Other substrates were used for β-SiC growth or other process studies.



(a)



(b)

Fig. 3.6. Photographs of the typical polished TiC_x substrate (a) with low pit density, (b) with high pit density and multigrains.

The standard TiC_x substrate preparation procedure for β-SiC epitaxial growth consisted of 3 steps: (1) polishing; (2) degreasing; and (3) wet chemical etching.

The TiC_x substrate was first lapped with 15 μm diamond paste on a steel wheel, followed by 6 μm diamond paste polishing on a polishing cloth until a specular surface was obtained. Then a chemical-mechanical polishing on a polishing cloth for 1.5 minutes was performed to remove the mechanical damage caused by diamond polishing. The chemical polishing solution composition suggested by Parsons[68] was as follows: 45 g of $K_3Fe(CN)_6$, 1g of KOH, 200 cm^3 of H_2O, and 0.5 g of 0.05μm Al_2O_3 powder.

Before β-SiC epitaxial growth, the polished TiC_x substrate surface was degreased in hot TCE, acetone and methanol for 5 minutes each, then thoroughly rinsed in deionized (ID) water, and blow dried with nitrogen (N_2). Subsequently, two wet chemical etching procedures were performed on the substrate surface. The first procedure removed most foreign oxides that may be present on the substrate surface. It consisted of a 3 minute etch in 4.8% HF, followed by DI rinsing and N_2 drying. Next, the substrate surface was etched in a HNO_3:H_2SO_4 =1:4 acid mixture for 5 minutes at room temperature to remove TiO_x on the surface and about 50Å TiC_x surface layer. Finally TiC_x was rinsed with DI water, blow dried with N_2, and immediately loaded into CVD reactor.

3.2.3. TiC epitaxial growth on TiC_x

An approach to obtaining better quality titanium carbide substrates for β-SiC growth was to grow a buffer TiC epilayer on bulk TiC_x substrates. TiC_x substrates are nonstoichiometric and have a high defect density that would affect the epitaxial quality of the subsequent β-SiC layer. The growth of a thin layer of homoepitaxial TiC preceding β-

SiC growth could produce a stoichiometric, lower defect density TiC surface for β-SiC nucleation and growth; therefore, the quality of the β-SiC film would be improved.

The growth sources used for TiC growth are $TiCl_4$ and C_2H_4. The H_2 is the carrier gas. The TiC_x substrate was heated to 1230°C in 2.9 slm H_2 and stabilized for TiC growth. Before growth started, 0.54 sccm of C_2H_4, the carbon source, was introduced into the reactor. Thirty seconds later, 0.85 sccm $TiCl_4$ vapor carried by 100 sccm H_2 was introduced into the reactor to start the TiC growth. C/Ti ratio was about 1.3. The growth rate of the TiC thin film was 1.6 μm/hr.

The surface morphology of the as-grown TiC layer was investigated by SEM. Fig. 3.7 shows the surface morphology of a TiC film grown on a <111> TiC_x surface. The surface was mirror-like and silver in color. Under the microscope, no stacking faults, hillocks and roughness structures were observed on the surface.

Electron channeling contrast pattern (ECCP)[134] technique was used to determine whether or not the growth layers were single crystal epitaxial films. For a single crystal epitaxial film, a ECCP with the symmetry of the substrate can be obtained. The penetration depth of the channeling electrons is about 500Å. This technique is therefore well suited for thin film crystallinity characterization. Fig. 3.8 is a ECCP obtained from a 3000Å TiC layer grown on a <111> TiC_x substrate, which indicates that the growth layer is epitaxial.

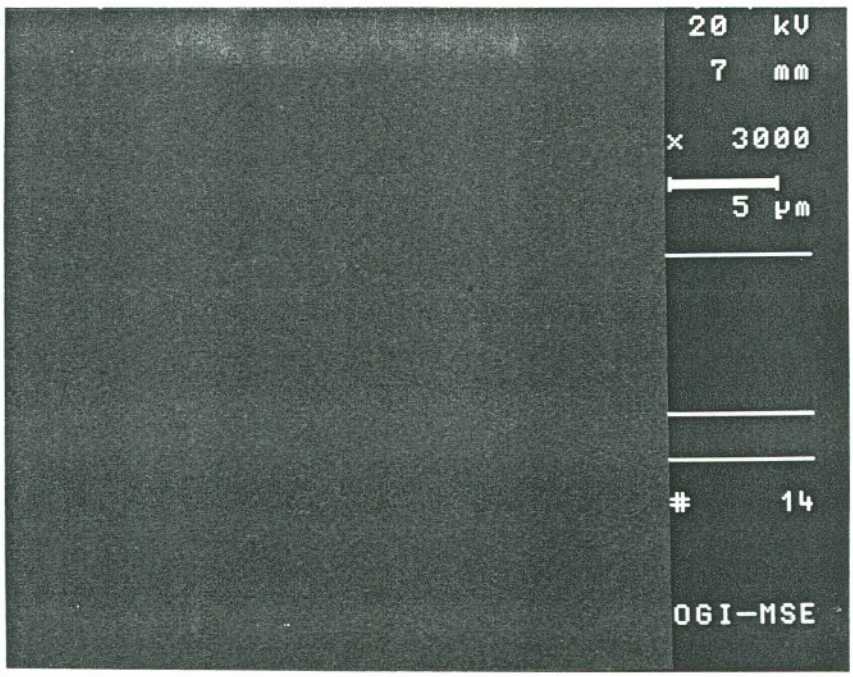


Fig. 3.7. SEM micrograph of a TiC epilayer grown on TiC_x.

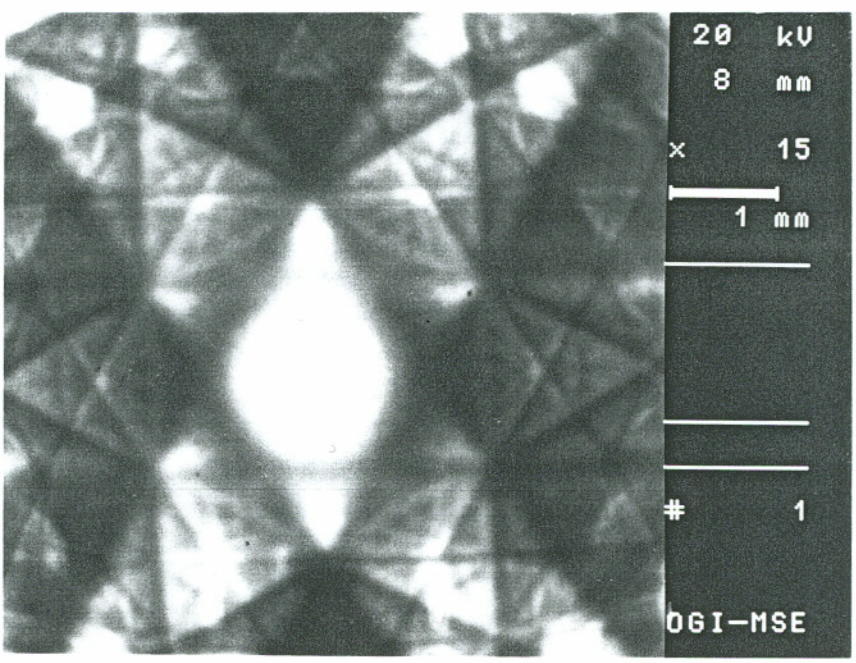


Fig. 3.8. ECCP of a TiC layer grown on TiC_x.

3.3. β-SiC thin film growth

The epitaxial technique for β-SiC growth on TiC employed in this work was first developed at Hughs Research Labs[8,9]. The single reactant source 1,2-disilylethane was used for β-SiC growth. This reactant source, containing equal numbers of Si and C in the same molecule, was specially developed to precisely control the Si/C ratio in the gas phase so that the complete nucleation of β-SiC on TiC could be achieved. The purpose of our growth investigation is to optimize this growth process so that it can be used for device structure growth.

3.3.1. β-SiC thin film growth procedures

The β-SiC epitaxial growth was conducted in the inverted vertical reactor as shown in Fig. 3.3. The TiC_x substrate was heated by RF inductive heating through a graphite susceptor. The substrate temperature was measured through the reactor chamber water cooling jacket with a Leeds and Northrup disappearing filament optical pyrometer. The angle of observation was about 20° from the reactor chamber axis.

The growth structure for growth process studies included a layer of buffer TiC and a subsequent layer of β-SiC. After loading the substrate, the system was pumped down to less than 1 millitorr and leak-checked, then backfilled with Ar. Using the standard condition described in the section above, a 3000Å TiC buffer layer was grown on the TiC_x substrate. After TiC buffer growth, the substrate was heated to about 1600°C for 10 minutes to remove chlorine reactant products from the previous growth, and then reduced to the temperature required for β-SiC growth. β-SiC growth was started by introducing the DSE ($Si_2C_2H_{10}$) source carried by H_2 into the reactor. The DSE bubbler temperature was kept at 0°C. The H_2 flow rate though the bubbler varied from 2 sccm to 6 sccm. The

vapor flow rate of DSE was not determined because its vapor pressure has not been measured. Growth was terminated by bypassing the DSE source.

3.3.2. β-SiC growth process optimization

The goal of β-SiC growth process optimization was to find controllable and repeatable growth conditions yielding unpolytyped, single crystal, epitaxial β-SiC possessing the best possible as-grown morphology; to minimize the epitaxial growth temperature; and to maximize the growth rate of epitaxial β-SiC. Lower growth temperature is preferred because dopant incorporation is more easily controlled at lower temperature. Growth rate is an important parameter for determination of efficiency of the process. However, very high growth rate could cause polycrystalline formation.

Growth temperature is one of the most critical parameters in β-SiC nucleation and growth process. It directly controls the cracking behavior of the reactant source DSE. The cracking properties of the DSE reactant source are such that, within a certain range of TiC substrate temperatures, it cracks to yield equal amount of Si and C atoms for epitaxial β-SiC growth. On the other hand, if the growth temperature is too low, the source would provide excess Si, and if the growth temperature is too high, the source would provide excess C. Both cases would result in non-stoichiometric SiC layers that would deteriorate the growth morphologies and the epilayer crystal quality, and even cause amorphous SiC formation.

To determine the optimum growth temperature, β-SiC thin films were grown at different growth temperatures on <111> TiC substrates with 4 sccm H_2 gas flowing through the DSE bubbler. The films grown at temperatures in the range $1240°C<T_s<1280$ °C has a specular appearance to the naked eye. The films grown above 1290°C showed

brownish but reflective appearance. The films grown below 1240°C had very rough surfaces and could not be polished to a smooth surface. Detailed as-grown surface morphologies were studied with a Nomarski microscope, as shown in Fig. 3.9 for different growth temperatures – 1230°C (a), 1250°C (b), and 1300°C (c). Rather smooth surface morphology was observed for film grown at 1250°C. Similar surface morphologies were observed for all films grown in the range $1240°C<T_s<1280°C$. Therefore, β-SiC growth temperature was optimized around 1250°C. The minimum growth temperature was determined to be about 1240°C.

Further optimization of the β-SiC growth process was accomplished by employing *in-situ* thermal treatment of the TiC_x substrate, by growth of the TiC buffer layer, by insuring the stable growth temperature, and by controlling the cooling rate after the growth. The optimized thermal cycle for β-SiC growth is illustrated in Fig. 3.10. The TiC substrate was heated to 1600°C in H_2 environment for about 20 minutes. The purpose of this *in-situ* substrate preparation step was to create a more stoichiometric TiC_x surface by thermal evaporation of free Ti . A buffer layer TiC about 3000Å thick was first grown on the TiC_x substrate at 1230°C using $TiCl_4$ and C_2H_4. TiC epilayer possessed better crystal quality and lower impurity concentration compared to the substrate. After the TiC growth , the sample was heated to 1600 °C for 10 minutes to remove chlorine reactant products from the previous growth, and then the temperature was reduced to about 1250° C for β-SiC growth. After growth was terminated, the sample was slowly cooled to room temperature. Fast cooling could cause high thermal stress, which would be released as defects in the epilayer.

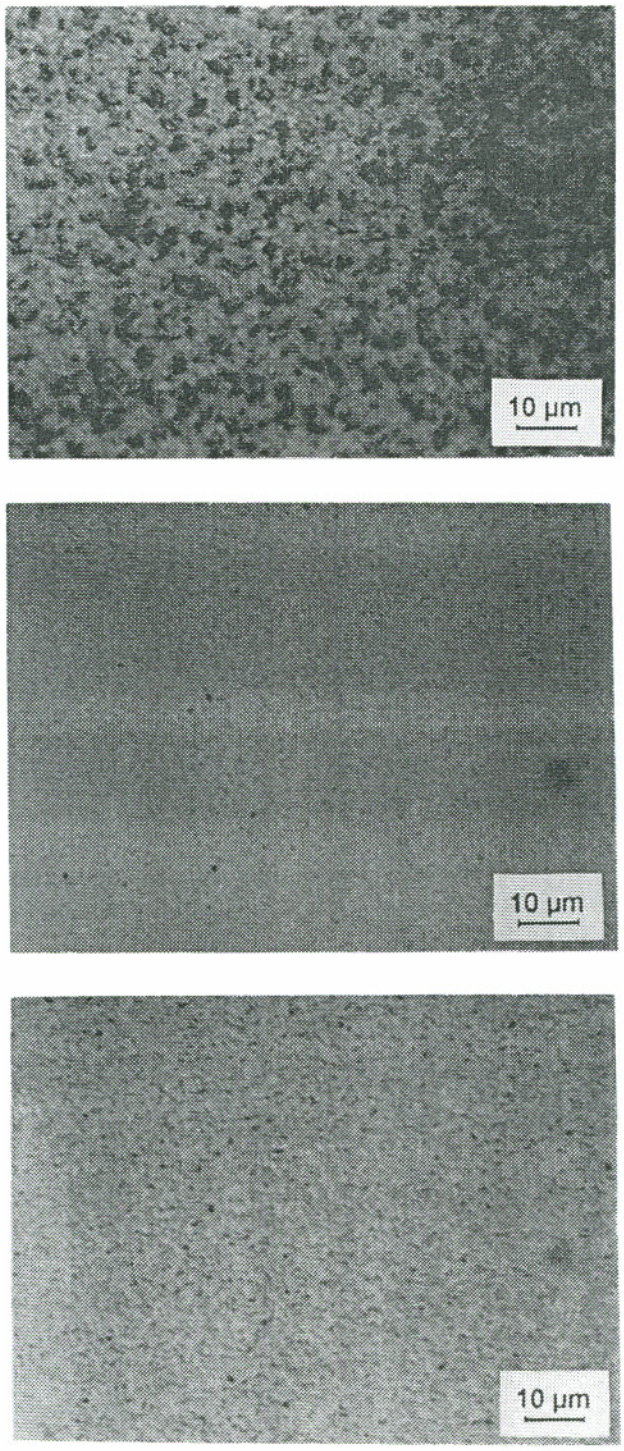


Fig. 3.9. Nomarski micrographs of as-grown β-SiC grown at 1230°C (a), 1250°C (b) and 1300°C (c).

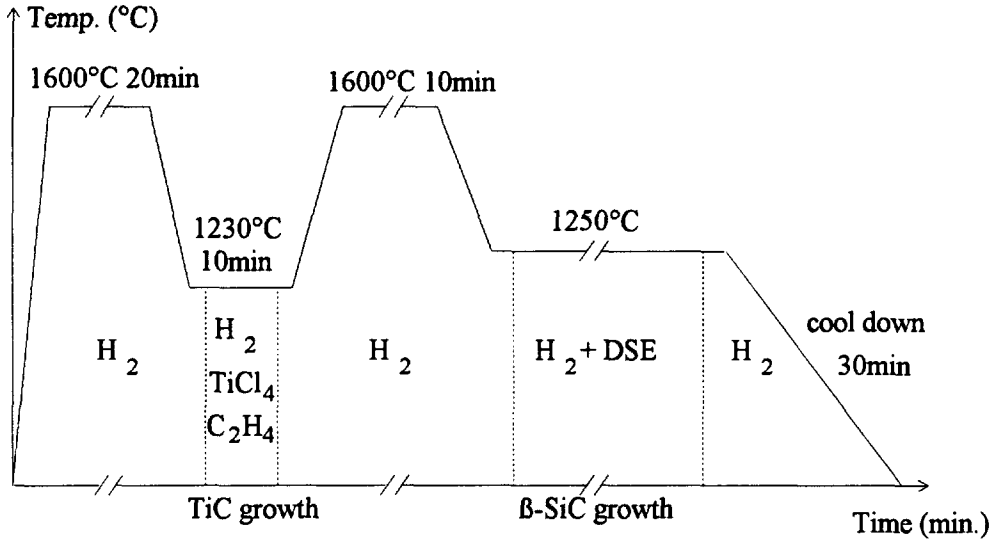


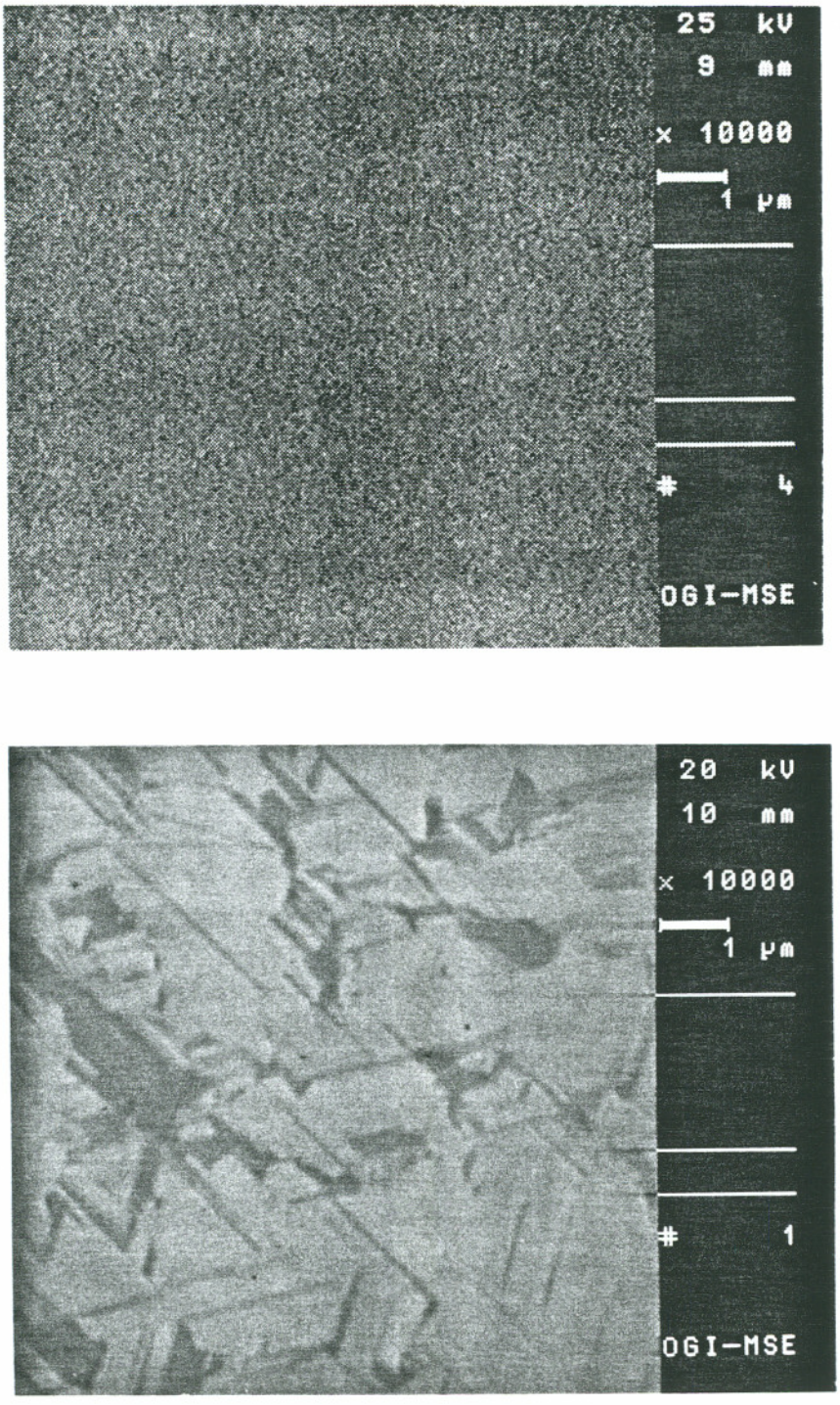
Fig. 3.10. The optimized thermal cycle for β-SiC growth on TiC_x substrate.

More detailed surface morphologies of β-SiC epilyaers were studied by SEM to identify possible defects. The 4μm β-SiC films were grown at 1250°C. Typically, the as-grown films were shiny with little milky apparence. Determined by Dektak measurements, the surface roughness was on the order of 1000Å. Before the SEM sutdies, the as-grown filim was polished by 0.1 μm diamond paste and then chemical-mechanically polished, as described in chapter 3, to obtain a very smooth surface. The surface layer removed by polishing was less than 0.3μm. Fig 3.11 shows typical micrographs of polished β-SiC surfaces grown at 1250°C under different growth conditions. As shown in Fig. 3.11 (a), no structural defects such as anti-phase domains or stacking faults, which are typical defects in β-SiC grown on Si substrate, were observed in β-SiC grown on TiC substrates under controlled optimum growth conditions. Stacking faults were found in β-SiC grown on TiC substrates, as shown in Fig. 3.11(b), if an unoptimized growth condition was used intentionally or unintentionally. For example, temperature drift during the nucleation and

growth, or an improperly prepared TiC substrate surface, or fast cooling rate could result in the formation of stacking faults in β-SiC epilayers.

Fig. 3.12 shows an ECCP of a 3μm thick β-SiC film grown on a (111) TiC substrate at 1250°C. The clear six-fold symmetry indicates that the β-SiC thin film has repeated the substrate crystal structure, and thus the growth was epitaxial.

Growth rate of a β-SiC thin film was determined by examining the cross sectional view of the sample by SEM. Fig. 3.13 is the SEM micrograph of the β-SiC layer grown for 45 minutes, with 4 sccm H_2 flow rate through the DSE bubbler. The growth rate determined is thus about 5 μm/hour. It was found that the growth rate has significant effects on crystallinity and the nucleation process. The films grown at the growth rates higher than 6 μm/hour at 1200°C were not single crystal, as shown by ECCP. The films grown at the growth rates lower than 2.5 μm/hour were incompletely nucleated. Island structures were observed on the film surfaces. This is probably due to lack of sufficient reactant species at the initial stage of the growth to form a continuous β-SiC layer.



(a)

(b)

Fig. 3.11. SEM micrographs of morphologies of polished β-SiC grown under optimized conditions (a) and unoptimized conditions (b).

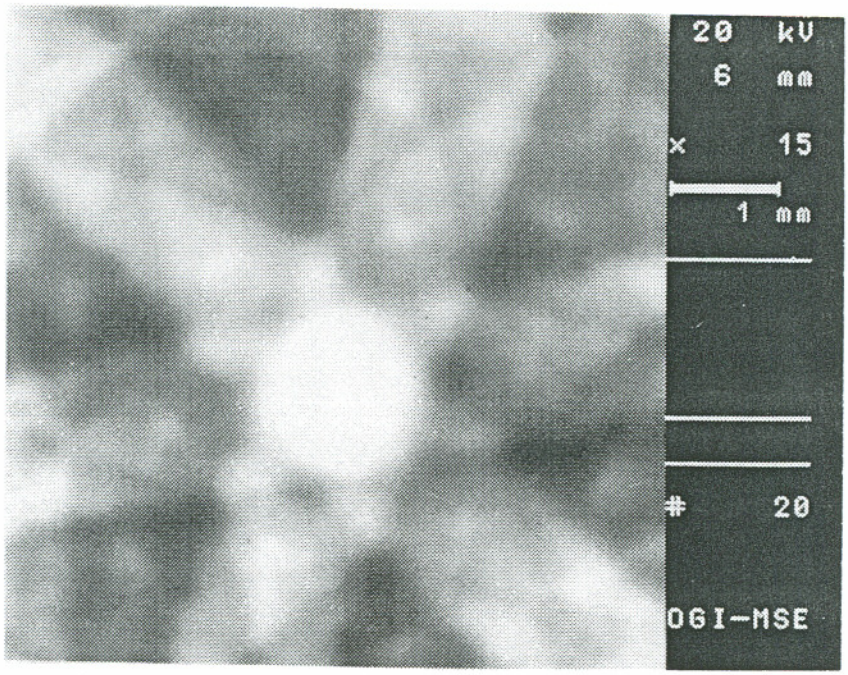


Fig. 3.12. ECCP of a (111) β-SiC epilayer.

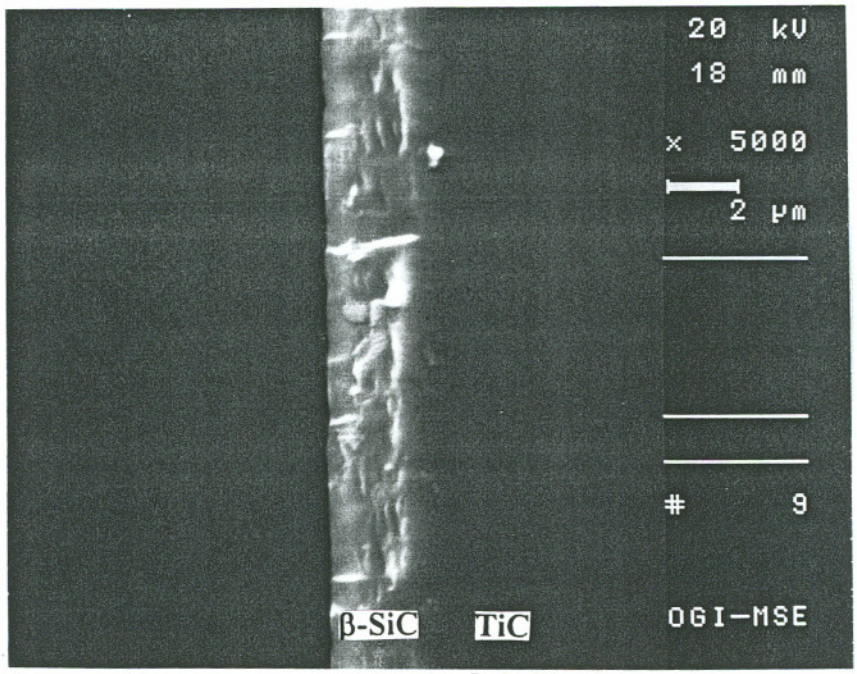


Fig. 3.13. Cross-sectional view of a β-SiC/TiC growth structure.

3.4. Electrical properties of undoped and *in-situ* doped β-SiC

Electrical properties of undoped, nitrogen doped and aluminum doped β-SiC films were evaluated by hot probe, current-voltage (I-V), and capacitance-voltage (C-V) measurements. Conduction polarity of β-SiC film was determined by the hot probe technique. Silver (Ag) Schottky diodes were fabricated on β-SiC to determine the carrier concentrations of β-SiC layers

3.4.1. *In-situ* doped β-SiC growth

Intentionally doped β-SiC was grown by introducing the desired dopant sources along with the DSE ($Si_2C_2H_{10}$) source during the growth. Ammonia (NH_3) and dimethylaluminum hydride (DMAH or $Al_2C_2H_7$) were used for *in-situ* doping to produce n-type and p-type β-SiC, respectively. In β-SiC nitrogen has the shallowest donor activation energy (20 meV), and aluminum has the smallest acceptor activation energy (160 meV)[22,23].

All β-SiC epilayers used for electrical measurements were grown at 1250°C using optimized growth condition described in Fig. 3.10. The H_2 flow rate through the DSE source bubbler was kept at 4 sccm, which correspondent to the growth rate of 5μm/hr. The flow rate of the nitrogen for n-type doping varied from 10^{-5} to 10^{-3} sccm. The flow rate of the Al for p-type doping varied from 0.012 sccm to 1.2 sccm.

3.4.2. Ag/β-SiC Schottky contact formation and characterization methods

Prior to making Schottky contacts on β-SiC, the as-grown β-SiC was mechanically polished using 0.1 μm diamond paste until a smooth optically flat surface was obtained. The sample was then carefully cleaned sequentially in TCE, acetone and methanol, and

finally flushed with high purity deionized water and blow dried with nitrogen. An oxide layer was grown to serve as a surface passivant for the diode structures. The oxidation was carried out in a wet oxygen flow at 1150°C for 1 hour to form 1400Å silicon oxide on the β-SiC surface. The contact geometry used consisted of circular dots with different diameters (100μm, 120μm, 160μm and 280μm). A standard photolithography process was employed to define the Schottky dots on the oxide using AZ-1512 positive photoresist. Windows in the oxide were cut by etching in buffered HF solution, then the samples are rinsed in deionized water and dried in N_2. The Ag evaporation was performed in a diffusion-pumped physical evaporation system at a pressure of about 3×10^{-7} torr. The metal thickness was about 1500 Å. Unwanted metal was removed by a standard liftoff procedure. The ohmic contact of the Schottky diode was formed at the TiC/β-SiC interface during the epitaxial growth.

I-V curves of β-SiC Schottky diodes were measured by a Tek 371 curve tracer or by a computer controlled HP4145B semiconductor parameter analyzer. The HP4145B uses a source monitor unit (SMU) to supply a bias voltage and measures the corresponding current output internally. C-V characteristics of the diodes were measured by a Boonton capacitance meter combined with a HP4145B semiconductor parameter analyzer. The operating frequency of the Boonton capacitance meter is 1MHz. The bias of the diode was supplied by the HP4145B. The output of the capacitance meter was recorded by the HP4145B voltage monitor channel.

3.4.3. Electrical characteristics of β-SiC epilayers

Current-voltage (I-V) characteristics of an Ag/undoped β-SiC Schottky diode are shown in Fig. 3.14. The Schottky barrier characteristics and hot probe measurement both

indicate that the material is n-type. The measured breakdown voltage is soft and varied form 2.5 to 5V. Capacitance-voltage (C-V) measurement shown in Fig. 3.15 indicates a 1.1×10^{18} cm^{-3} carrier concentration.

Due to the high background n-type carrier concentration, Al-doped β-SiC films show n-type characteristics when the dopant source DMAH flow rate is below 0.3 sccm. When the dopant source DMAH flow rate exceeds 0.3 sccm, Al-doped β-SiC shows p-type conduction. I-V characteristics of an Ag/p-type β-SiC diode are shown in Fig. 3.16. The measured breakdown voltage is about 3V. The breakdown is fairly abrupt. The p-type carrier concentration in the film grown with 0.3 sccm DMAH flow rate is 7.8×10^{18} cm^{-3}, as calculated from the C-V results in Fig. 3.17.

All nitrogen doped β-SiC layers show n-type characteristics, determined by hot probe measurements. Attempts to determine the carrier concentration in nitrogen doped β -SiC and Al doped β-SiC grown with Al source flow rates higher than 0.3 sccm were unsuccessful, because of high leakage currents in Schottky diodes.

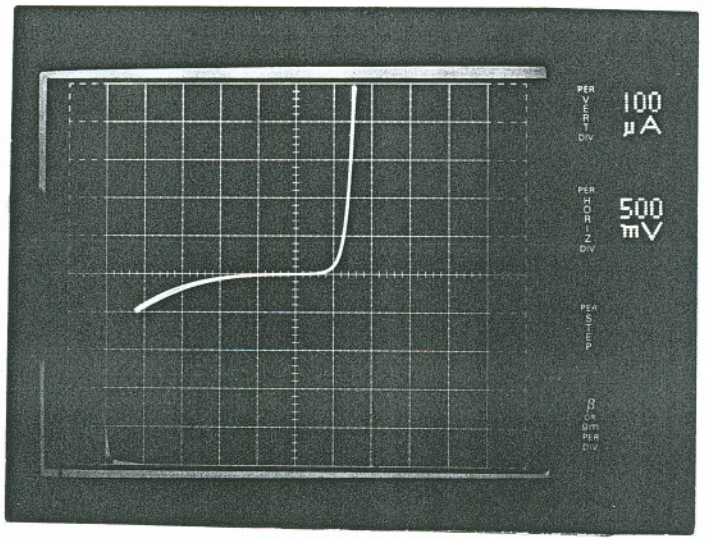


Fig. 3.14. I-V characteristics of an Ag/undoped β-SiC Schottky diode.

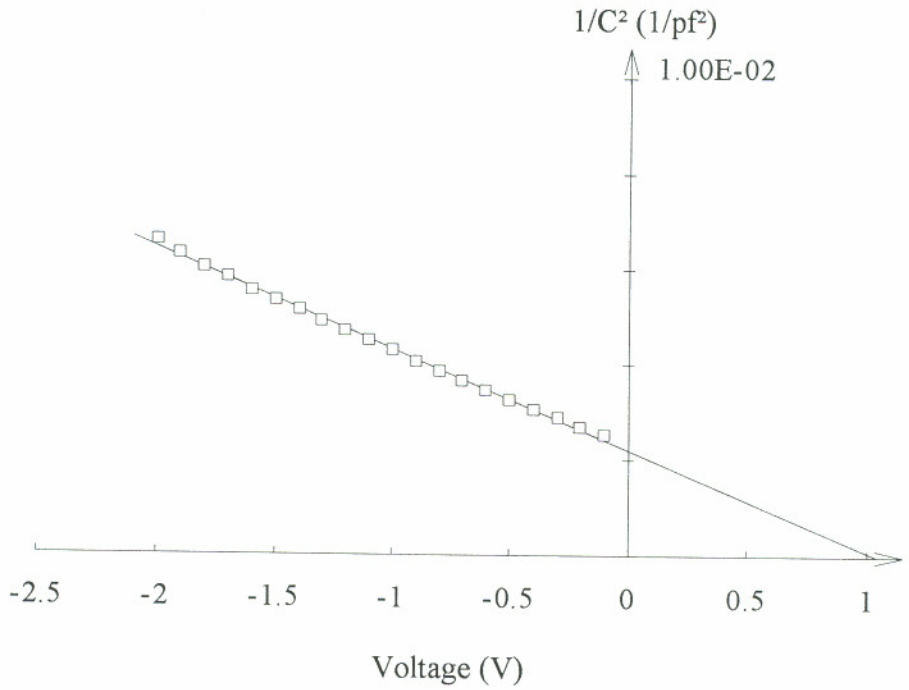


Fig. 3.15. $1/C^2$ vs. V plot for Ag Schottky contact on undoped β-SiC.

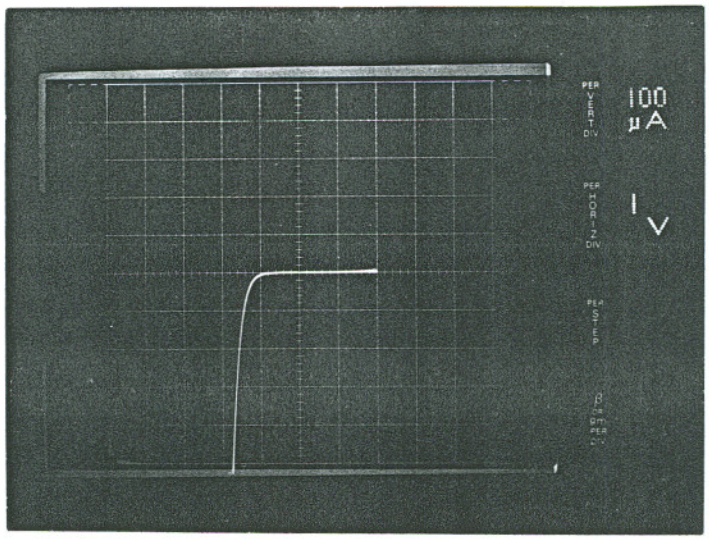


Fig. 3.16. I-V characteristics of an Ag/p-type β-SiC Schottky diode.

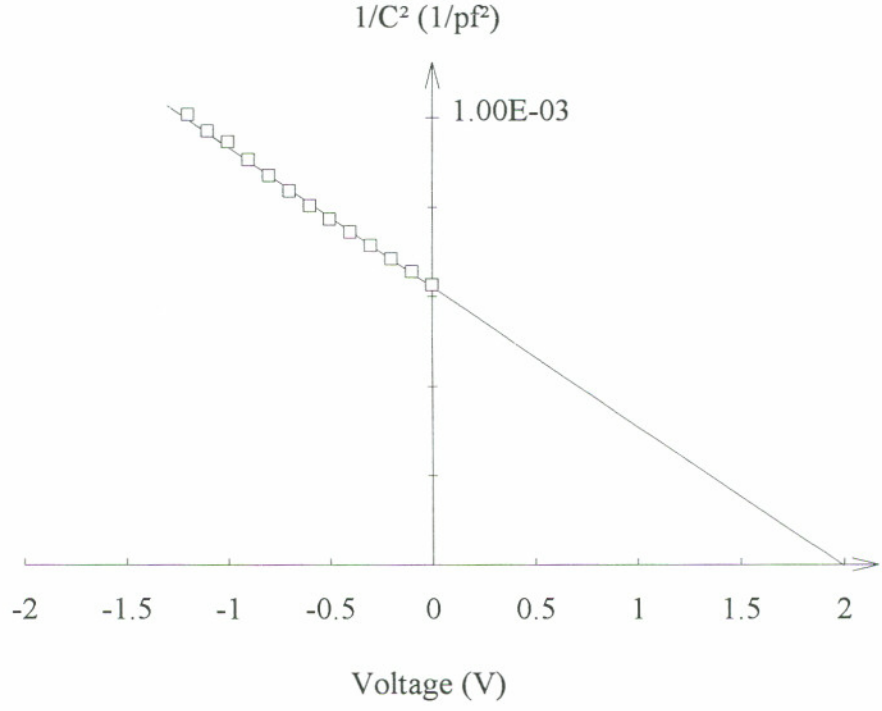


Fig. 3.17. $1/C^2$ vs. V plot for Ag Schottky contact on 0.3sccm Al-doped p-type β-SiC.

3.5. Summary

A β-SiC epitaxial growth process, using TiC as substrate and 1,2-disilylethane (DSE) as reactant source, was optimized in an inverted-vertical atmospheric pressure CVD reactor. TiC was selected as substrate material mainly because its lattice parameter is close to that of β-SiC (mismatch < 0.7%). Procedures for TiC substrate evaluation and preparation for β-SiC epitaxial growth were developed as part of this research. DSE reactant source was selected because it contains an equal number of C and Si atoms and its reported decomposition characteristics suggest that C and Si could be obtained from it at approximately equal rates. Repeatable nucleation and epitaxial growth conditions, giving complete substrate coverage and controlled growth, were established. Substrate temperatures of 1240°C to 1290°C were found to be optimum for β-SiC epilayer nucleation and growth. The maximum β-SiC epitaxial growth rate obtained was 6μm/hr.

Electrical properties of undoped and doped β-SiC epilayers were investigated. Undoped and nitrogen doped β-SiC epilayers showed n-type characteristics. P-type β-SiC was obtained by *in-situ* aluminum doping. Ag Schottky diodes were fabricated on undoped and Al-doped p-type β-SiC. As determined by C-V measurement, the background concentration of undoped β-SiC is about 1×10^{18} cm^{-3}.

Chapter 4
Reactive Ion Etching of β-SiC/TiC

In β-SiC device fabrication, reactive ion etching (RIE) is the only useful technique to selectively remove β-SiC because most widely used acids and other liquid etchants do not attack β-SiC at or near room temperature[91,92]. Several fluorine based reactant sources, including CF_4, CF_4+O_2[93-95], SF_6[96], $CHF_3+O_2+H_2$[97] and NF_3[98] have been used to etch β-SiC. However, most work has concentrated on etching rate studies and is inconclusive with respect to which gas mixture is the best choice to achieve high quality β-SiC etching. Furthermore, differences in reactor geometry and β-SiC thin film quality make it difficult to reproduce the reported results. Therefore, development of an RIE process was necessary to obtain useful or optimum conditions for device fabrication.

4.1. General considerations for RIE process development

Reactive ion etching (RIE) can be described as follows: A glow discharge (plasma) is used to generate chemically reactive species (atoms, radicals, ions) from a relatively inert molecular gas. These species react chemically with the solid surface to form a volatile reaction product. The etch product then spontaneously desorbs from the etched material into the gas phase where it is removed by the vacuum pumping system. A conventional RIE system contains two parallel electrodes. The reactive ions are created by an RF (13.56 MHz) voltage applied to one of the electrodes, on which the sample to be etched is placed.

The main requirements of the reactive ion etching process are: (1) high quality surface treatment, (2) high selectivity of etching with respect to the mask material and (3) high resolution and anisotropy. Development of an RIE process to meet these requirements depends on the simultaneous control of gas composition, gas flow rate, reactor chamber pressure, and RF power. A physical understanding of the mechanism of the process and of the effects of the process variables is very important for efficiently designing the experiment to obtain useful or optimum process conditions.

Reactive ion etching behavior is controlled by a combination of chemical mechanisms and physical mechanisms. Chemical reactions between the reactive species and the etched material depend on the composition and density of the reactive species in the plasma, which are determined by the composition and the flow rate of feed gas, the chamber pressure and the RF power. An RIE process dominated by chemical mechanisms usually results in isotropic etching and may have a low etching rate when the etched material possesses strong atomic bonding. Physical bombardment by energized ions on the etched surface can enhance chemical reactions and also result in anisotropic etching. The average potential distribution between the two electrodes for an RF plasma in an RIE system is shown in Fig. 4.1. The powered electrode is self-biased with a negative potential, referred to as DC bias. An electric field is built up near the self-biased electrode. Positive ions in the plasma acquire energy from this electric field and subsequently impact on the etched surface. Therefore, the DC bias is directly related to the energy of the ions and should be measured as a control parameter to evaluate the effect of physical mechanisms in a reactive ion etching process. Usually, DC bias increases with increasing RF power and/or decreasing chamber pressure. However, very high DC bias should be avoided to prevent ion bombardment damage occurring in the etched material.

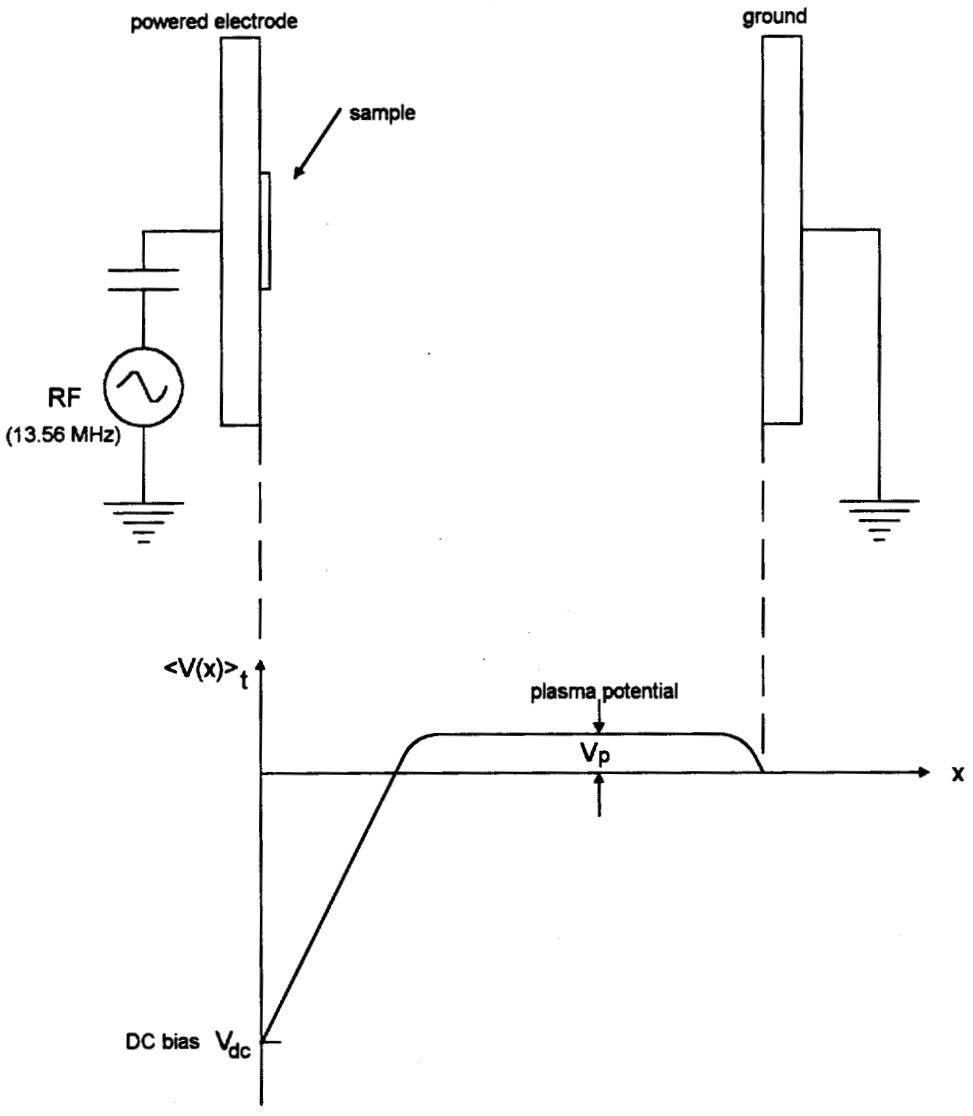


Fig. 4.1. Time-averaged potential distribution of an RF plasma in an RIE system.

4.2. RIE apparatus and experimental procedures

Detailed studies on reactive ion etching of β-SiC grown on TiC_x were performed using both $CF_4/O_2/Ar$ gas mixture and SF_6 gas. Gas mixture contained CF_4+O_2 is one of the most popular reactant gases for etching Si contained materials, such as Si, SiO_2 and SiC. It was proposed that for β-SiC etching[93-95], the Si was etched away as SiF_4, while the carbon was removed by CO, CO_2 or CF_x. Comparing with CF_4, SF_6 contains larger amount fluorine atoms, therefore it is expected to be more chemically aggressive for β-SiC etching, by removing the Si as SF_4 and removing the C as CF_x. The principle objective of our investigation was to establish the conditions for β-SiC RIE using both $CF_4/O_2/Ar$ gas mixture and SF_6 gas, and to compare the etching results in terms of etching efficiency, morphology and wall profile so that one of these two reactant gases could be chosen for β -SiC device structure fabrication.

The apparatus used in β-SiC RIE studies is a PLASMTRAC 2406 commercial system, schematically shown in Fig. 4.2. The system operates in a conventional reactive ion etching mode. The lower electrode is energized with a maximum of 500W RF power at 13.56 MHz supplied through a matching network; the upper electrode is grounded. The spacing between the two aluminum electrodes (each 6 inches in diameter) is 1.5 inches. A mechanical pump is connected to the chamber through a gate valve and a throttle valve. The chamber pressure is monitored with a capacitance manometer and can be controlled automatically by adjusting the opening of the throttle valve through a pressure controller while gas is flowing through the chamber. The flow rates of gases into the chamber are maintained with standard mass flow controllers. During etching experiments, both electrodes are cooled by a circulating fluid to prevent overheating by the plasma. RF voltage of the plasma and DC voltage on the lower electrode are monitored with the

meters on the front panel. The system includes the load locks, through which a 4 inch wafer can be transferred into or out of the chamber automatically.

Aluminum was chosen as mask material because it does not react with fluorinated gases to form volatile species. Aluminum was evaporated on to β-SiC/TiC_x, then patterned by photoresist and etched by a commercial Al etching solution, which contains H_3PO_4:HNO_3:CH_3COOH:H_2O=16:1:1:2.

The samples were mounted by wax on a 4 inch Si wafer and loaded into the etching chamber. The system was first pumped down to its base pressure of 5 millitorr or less. Subsequently, either the SF_6 gas or the CF_4/O_2/Ar gas mixture was introduced into the chamber, and the throttle valve controller was turned on to stabilize the chamber pressure at a preset value. The RF power was then applied to the lower electrode to start plasma and etching. At the end of etching, the RF power was shut down first. Then the gas flow was stopped, the pressure controller was turned off, and the system was pumped down to its base pressure. Finally, the sample was unloaded through the unload lock.

After reactive ion etching, the Al mask was removed by wet chemical etching. Etch depths of β-SiC were measured with a Dektak depth profiler, to determine etch rates. The etching surface morphologies and wall profiles were studied by Nomarski microscope and scanning electron microscope (SEM).

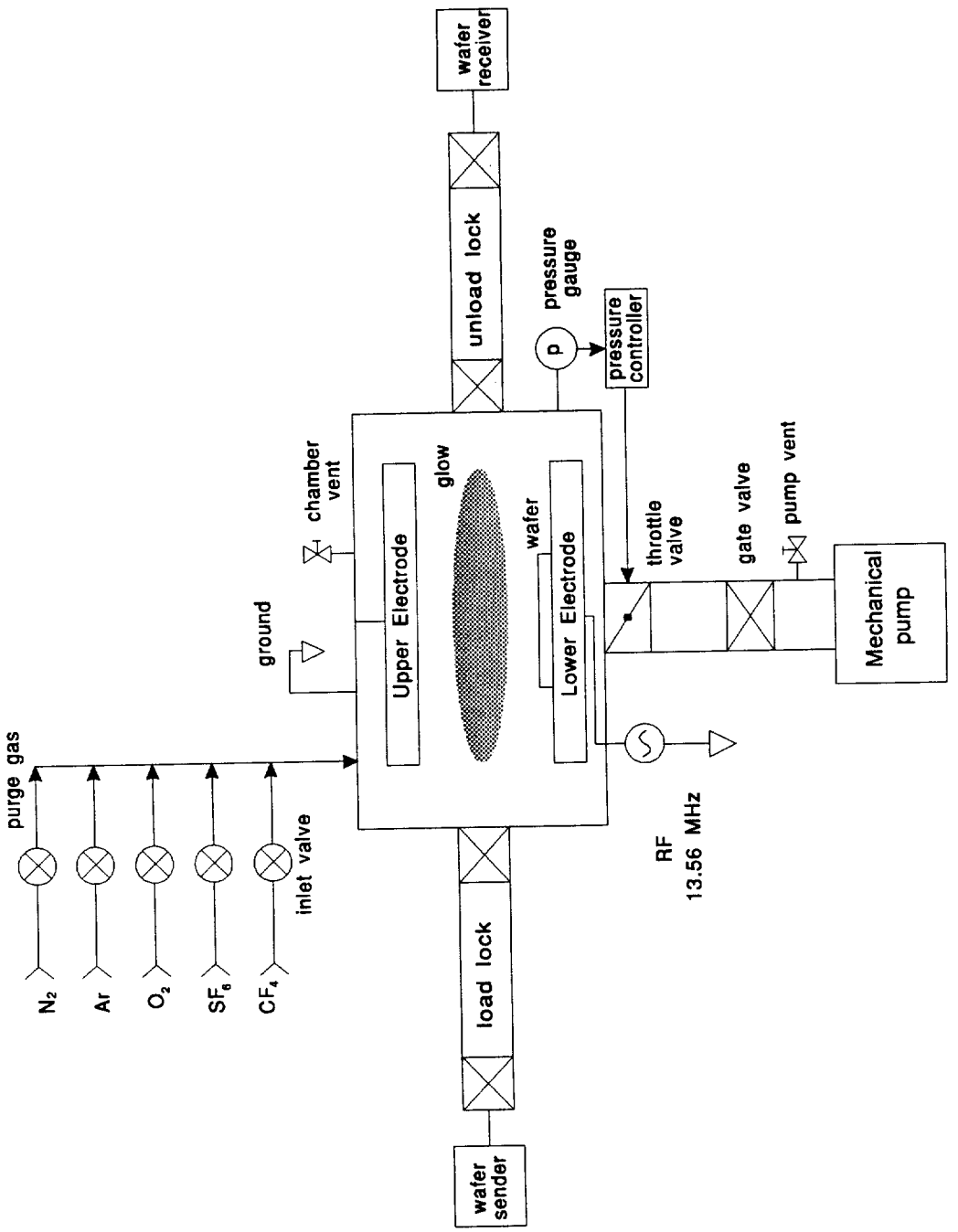


Fig. 4.2. Schematic diagram of reactive ion etching system.

4.3. Experimental results and discussion

The etch process of β-SiC was characterized in $CF_4/O_2/Ar$ and SF_6 gases. Preliminary experiments were performed by adjusting RF power, chamber pressure and gas flow rate to insure that the plasmas were stable and that useful etch rates might be obtained. The ranges of independent variables were established for detailed studies of β-SiC etch rates, and are given in Table 4.1.

Table 4.1. Range of variables for β-SiC etch rate studies.

Gas mixture	CF_4+O_2 (sccm)	Ar (sccm)	SF_6 (sccm)	Pressure (mtorr)	RF power (W)
$CF_4/O_2/Ar$	10	10	—	60	30-70
SF_6	—	—	25	80	50-170

It was found that the Ar additive to CF_4/O_2 improved the plasma stability, and thus the etch uniformity. In the $CF_4/O_2/Ar$ mixture, the Ar percentage was kept at 50 %. The total flow rate of CF_4+O_2 was 10 sccm. The etch rate of β-SiC was determined as a function of O_2 percentage in total CF_4+O_2 flow rate at pressure 60 mtorr and RF power 50W, as shown in Fig. 4.3. The etch rate starts from 100 Å/min at 0% oxygen, increases monotonically with O_2 percentage increase, up to its maximum value 380 Å/min at 50 % oxygen, then decreases with further O_2 percentage increase, and finally reduces to zero at 100% oxygen. The DC bias V_{dc} was also measured during the etching experiments. As illustrated in Fig. 4.3, V_{dc} is not affected by oxygen concentration.

The role of oxygen in the $CF_4/O_2/Ar$ plasma can be explained as follows. The O_2 removes CF_x radicals, preventing their recombination with F atoms, thereby increasing the F-atom concentration in the discharge and eliminating polymerization. The O_2 also reacts with C to form CO or CO_2, therefore decreasing the C concentration. Both effects result in increasing the etch rates of β-SiC due to the greater effective F-atom concentration at the sample surface. Fig. 4.3 shows that the etch rate reaches its maximum value when 50% O_2 is added. At greater concentrations, the additional O_2 dilutes the F concentration, and causes the etch rate to decrease.

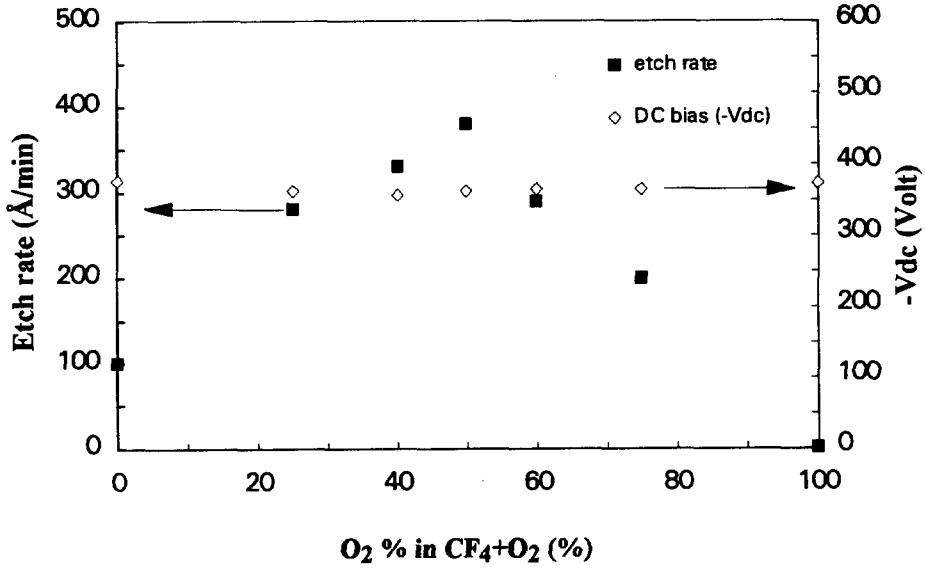


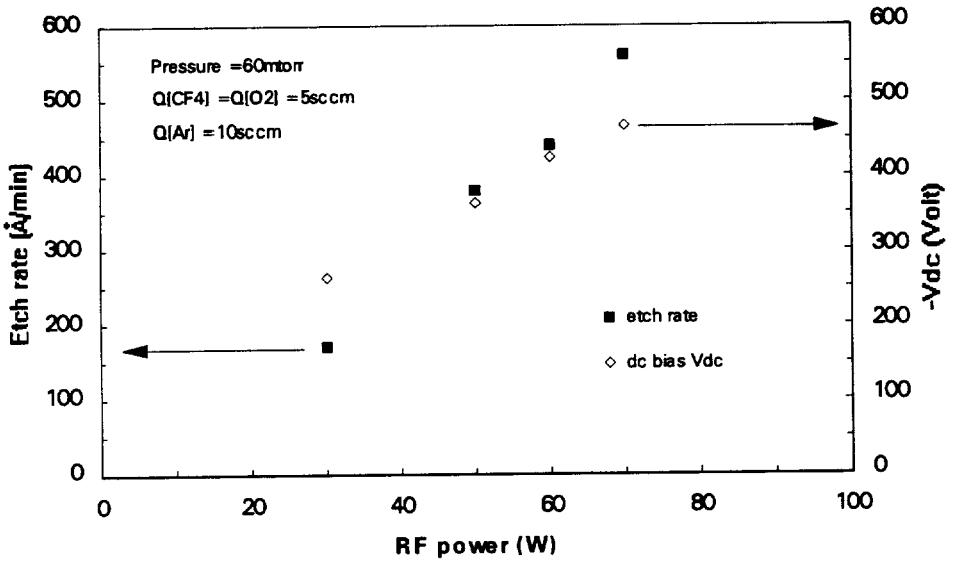
Fig. 4.3. Etch rate of β-SiC and DC bias V_{dc} as a function of oxygen percentage in CF_4+O_2.

In Fig. 4.4, the etch rates versus RF power are shown with the DC bias V_{dc} for $CF_4/O_2/Ar$ (25% : 25% : 50%) [Fig. 4.4(a)] at pressure 60 mtorr, total flow rate 20 sccm,

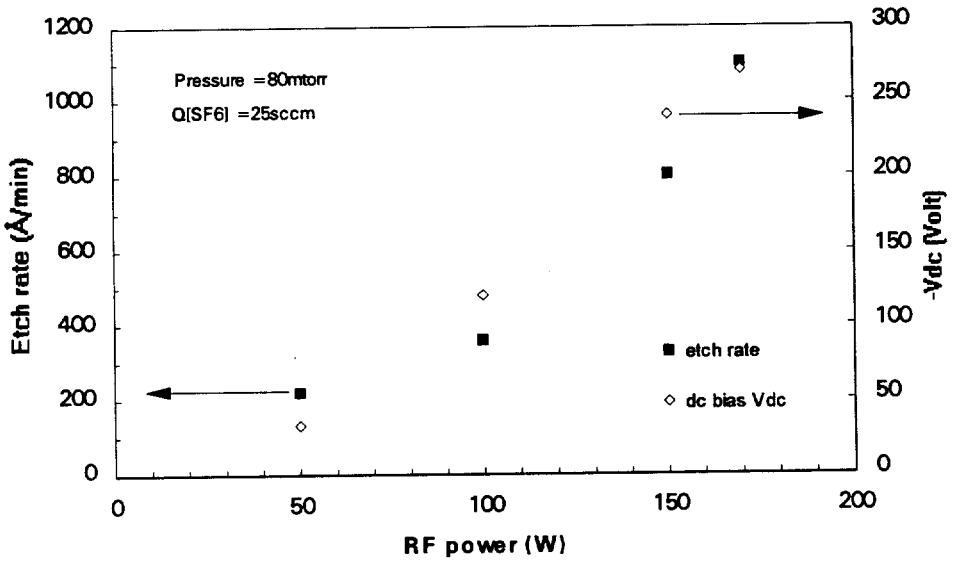
and SF_6 [Fig. 4.4(b)] at pressure 80 mtorr, flow rate 25 sccm. As one would expect, in both cases the etch rates of β-SiC increase with RF power. The observed $-V_{dc}$ also increases with RF power. For the $CF_4/O_2/Ar$ etch, the maximum etch rate obtained was about 570 Å/min at power = 70W. A further increase in power resulted in the $-V_{dc}$ exceeding 500V, a regime in which the plasma was unstable. High ion bombardment energy caused very rough etched surfaces. In the case of SF_6 plasma etching, the maximum etch rate obtained was about 1100 Å/min at a power = 170W. The corresponding $-V_{dc}$ in this case was only about 280V, which would not cause significant surface damage.

Fig. 4.5 and Fig. 4.6 show the surface morphology and the wall profile of a β-SiC/TiC structure created by $CF_4/O_2/Ar$ (25% : 25% : 50%) with total flow rate 20 sccm, etching at 50W and 60 mtorr. The etching rates of β-SiC and TiC under these conditions were determined to be 380Å/min and 1500Å/min, respectively. In general, $CF_4/O_2/Ar$ etching produced a rough β-SiC surface as shown in Fig. 4.5. The etched β-SiC shows a vertical wall profile (Fig. 4.6). The TiC substrate underneath the β-SiC is removed by isotropic etching. No backside etching of the β-SiC film is observed.

Fig. 4.7 and 4.8 show the surface morphology and the wall profile of the β-SiC/TiC structure after SF_6 etching at RF power 150W, pressure 80 mtorr and flow rate 25 sccm. The etching rates of both β-SiC and TiC under these conditions were determined to be 800Å/min. A very smooth β-SiC surface is obtained (Fig. 4.7). A vertical wall profile of β-SiC is also observed in an SF_6 plasma etching. In contrast to the results obtained in the $CF_4/O_2/Ar$ plasma, in the SF_6 plasma, the TiC substrate underneath the β-SiC is removed by anisotropic etching and no undercut is observed in the TiC substrate, as shown Fig. 4.8.



(a)



(b)

Fig. 4.4. Etch rates of β-SiC and DC bias V_{dc} as a function of RF power in $CF_4/O_2/Ar$ (a) and SF_6 (b).

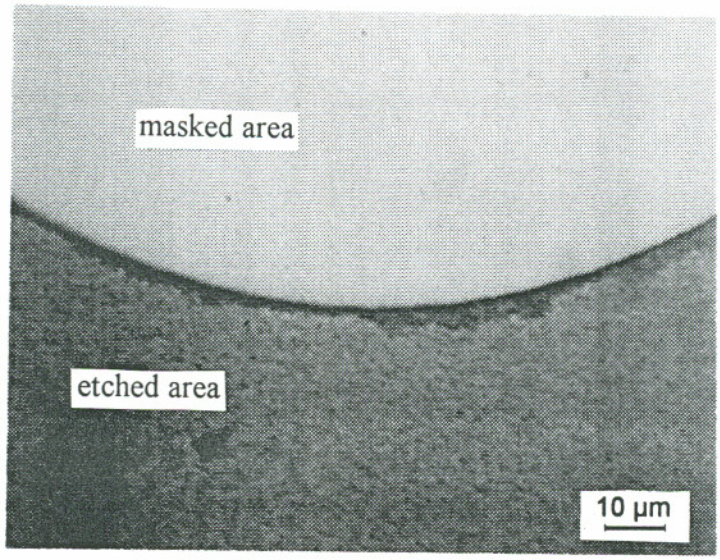


Fig. 4.5. Nomarski micrograph of etched β-SiC surface morphology from $CF_4/O_2/Ar$ etching at 50W and 60 mtorr.

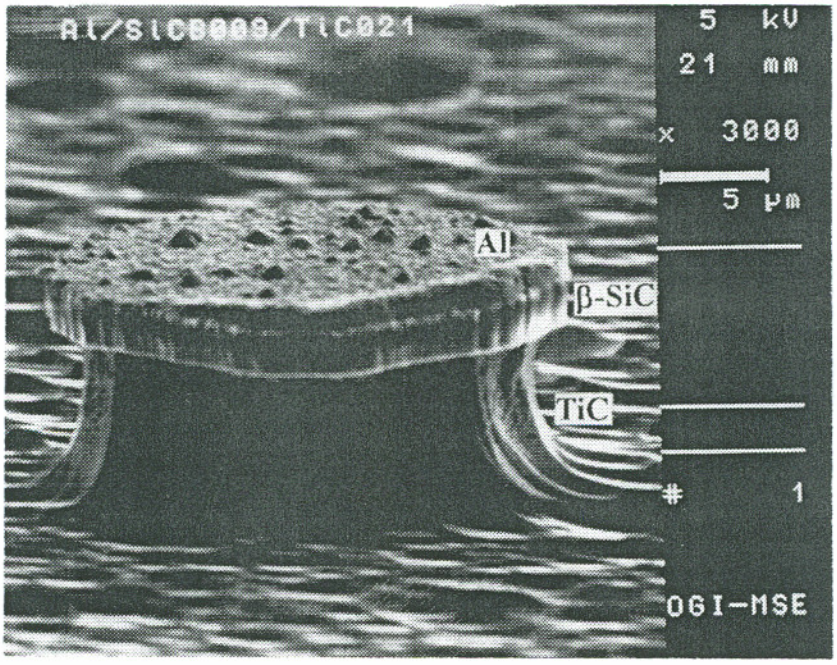


Fig. 4.6. SEM micrograph of an etched wall profile of a β-SiC/TiC structure from $CF_4/O_2/Ar$ plasma etching at 50W and 60 mtorr.

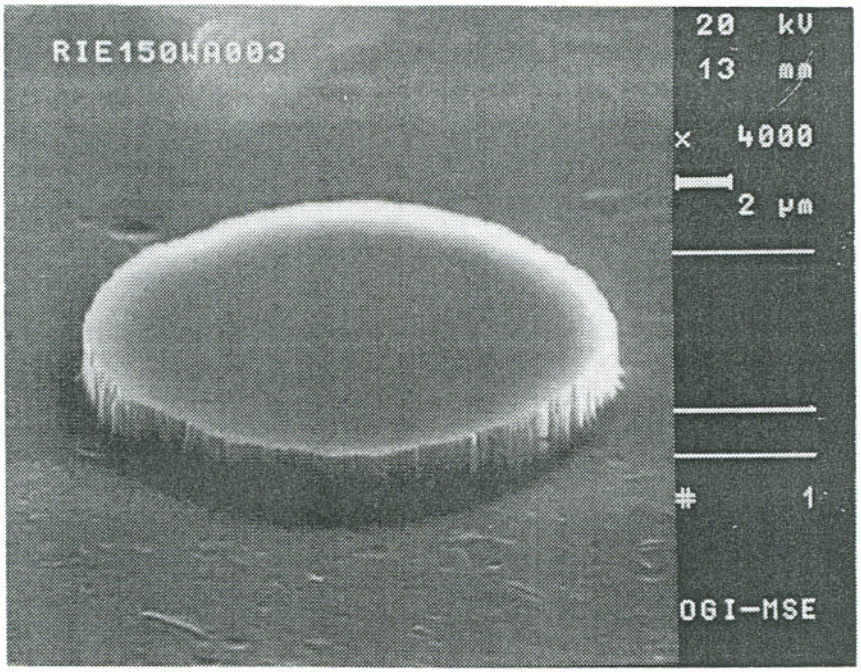


Fig. 4.7. SEM micrograph of an etched β-SiC surface and wall profile from SF_6 plasma etching at 150W and 80 mtorr.

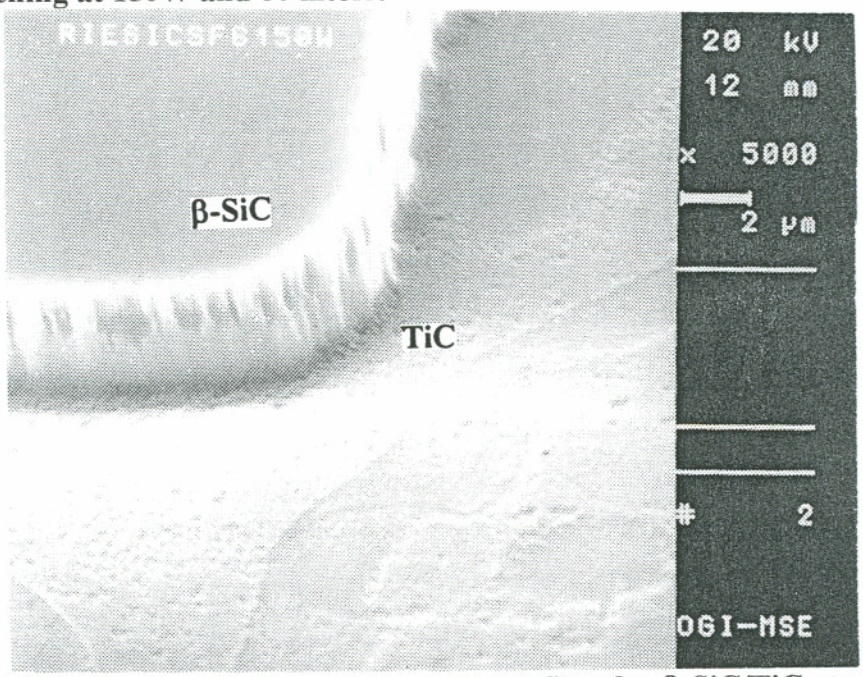


Fig. 4.8. SEM micrograph of an etched wall profile of a β-SiC/TiC structure from SF_6 plasma etching at 150W and 80 mtorr.

To understand the etching behavior of $CF_4/O_2/Ar$ and SF_6 plasmas, the etching chemistry needs to be considered. The decomposition processes of CF_4/O_2 and SF_6 base gases and the reaction processes for Si and C etching are as follows:

Decomposition processes		Reaction processes	
$CF_4+O_2 = CF_x+F+O+(CO, CO_2)$	(1)	$Si +4F = SiF_4$	(3)
$SF_6 = F+SF_x$	(2)	$C+xF = CF_x$	(4)
		$C+xO = (CO,CO_2)$	(5)

In CF_4/O_2 both decomposed plasma and reaction products include the same species, such as CF_x, CO and CO_2, but in SF_6 base gas there are no such species in decomposed plasma. Since these reactions are reversible in the plasma, Eqs. (1), (4), (5) do not go to completion and thus the reaction between SiC and CF_4/O_2 should be slow. On the other hand, in SF_6 there is no such limitation, and the reaction is faster than that in CF_4/O_2. In general, for SiC etching F/C ratio in the plasma should be maximized to enhance surface etching and prevent polymer or residue formation. Because of the large amounts of fluorine formed by SF_6 dissociation, it offers advantages for the SiC RIE process.

In the SiC RIE processes, the DC bias is the key factor controlling the etch rates, surface morphologies, and wall profiles. For SiC etch to occur, the atomic bond between Si and C must be broken and then each atom must be removed. This means that we can treat the etching of SiC as the etching of Si and the etching of C. It was suggested[135] that since the etch rate of Si is much higher than SiC, a carbon rich surface layer tends to be

formed during etching, and the removal of this layer is a rate-limiting step for SiC etching. Therefore, a sufficiently energetic ion bombardment on the SiC surface is required to remove the C blocking layer by a combination of physical sputtering and ion-assisted chemical reaction, so that the etching can progress. Our experimental results agree well with this model. Useful etch rates were only obtained when the DC biases were higher than 100V in SF_6 plasma, and 250V in $CF_4/O_2/Ar$ plasma. The lower DC biases, usually corresponding to low RF powers or high chamber pressures, result in very low etch rates, and sometimes surface residue formation. However, very high DC bias causes rough surface morphologies.

The physical etching mechanism can also be used to explain the anisotropic etching of the β-SiC structures. The incident energetic ions generally arrive in a direction perpendicular to the sample surface, and hence they strike the bottom surfaces of the etched features. However, ion bombardment is less effective at removing material from the side wall (parallel to the ion direction). As a result, the vertical β-SiC etching structure was created.

It was found that both $CF_4/O_2/Ar$ and SF_6 plasmas can also be used to etch TiC. Our experiments showed that $CF_4/O_2/Ar$ etching produced a higher TiC etch rate and an isotropic TiC etching, while SF_6 resulted in a high degree of anisotropic etching. This is probably implied that oxygen is a very active etching species for TiC etching. Therefore, in $CF_4/O_2/Ar$ plasma, the chemical mechanism is dominant, and relatively low DC bias is required to etch off TiC. The detailed TiC etching mechanisms need to be further investigated.

4.4. Summary

The reactive ion etching processes, using fluorinated gases $CF_4/O_2/Ar$ and SF_6, have been developed for β-SiC/TiC etching. The dependence of the etch rate on applied power and O_2 concentration has been studied. The β-SiC etch rate appears to be controlled by a combination of the chemical reaction of β-SiC with fluorine and/or oxygen radicals and the ion bombardment (DC bias). By comparing $CF_4/O_2/Ar$ and SF_6 etching results, we have concluded that etching β-SiC using SF_6 has higher efficiency, introduces less damage and results in better surface morphology.

$CF_4/O_2/Ar$ and SF_6 can also be used to etch TiC. Our preliminary studies show that $CF_4/O_2/Ar$ etching has a higher TiC etch rate than SF_6 etching, $CF_4/O_2/Ar$ results in an isotropic TiC etching, while SF_6 produces an anisotropic etching.

Chapter 5
β-SiC p-n Diode Fabrication and Characterization

The purpose of this work is to develop a process for β-SiC p-n junction diode fabrication. The included process steps are: (1) β-SiC p-n junction structure growth; (2) diode isolation; (3) surface passivation; and (4) ohmic contact formation. The fabricated vertical β-SiC p-n junction diode structure is shown in Fig. 5.1. The β-SiC p-n structure is doped *in-situ* during MOCVD growth. Diode isolation is achieved by reactive ion etching. The surface passivation layer is SiO_2. Contact metals for n-type and p-type β-SiC are TiC and Pt, respectively.

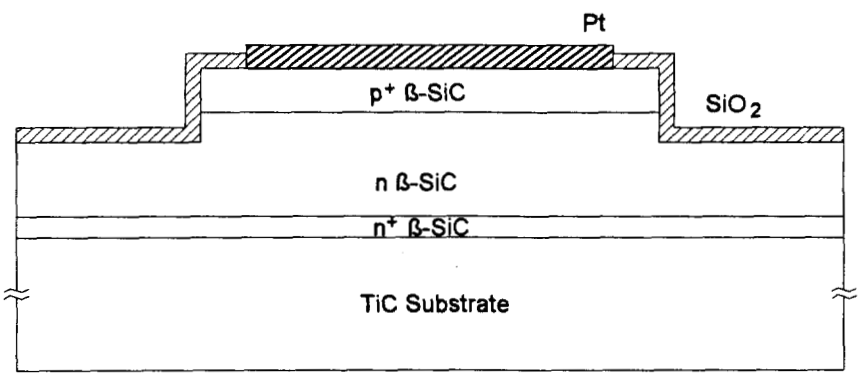


Fig. 5.1. Cross-sectional view of a β-SiC p-n junction diode.

In this chapter, the detailed process conditions for p-n diode fabrication are described. The characterization results are presented and discussed.

5.1 β-SiC p-n diode fabrication

β-SiC p-n junction diodes were fabricated using optimized growth and device process conditions. The process steps for the complete fabrication process are shown in Fig. 5.2.

The β-SiC p-n structure was composed of four epitaxial layers grown on a (111) TiC_x substrate: (1) 3000Å TiC buffer layer, (2) 2000Å nitrogen doped n^+ β-SiC, (3) 4μm undoped β-SiC, which appeared to be n-type, and (4) 1μm Al doped p^+ layer. All four layers were grown in the same growth run. A TiC buffer layer was grown first at 1230°C. The n^+ β-SiC layer, the undoped β-SiC layer, and the Al-doped p^+ β-SiC layer were grown at 1250°C.

The flow rate of H_2 through the $Si_2C_2H_{10}$ source bubbler was kept constant at 4 sccm for all β-SiC growth. This gave a growth rate of 5μm/hour. The flow rate of NH_3 was 0.0001 sccm for n^+ layer growth. The flow rate of $Al_2C_2H_7$ vapor was 0.3 sccm for p^+ layer growth. The carrier concentrations of the undoped β-SiC and the p^+ β-SiC, determined by C-V measurements of Ag/β-SiC Schottky diodes (Section 3.4.3), were 1×10^{18} cm^{-3} and 8×10^{18} cm^{-3}, respectively. After growth was completed, the layer was polished by 0.1μm diamond paste, degreased and HF etched to obtain a specular, clean surface.

The β-SiC p-n epitaxial structure was processed by reactive ion etching to form circular mesas for device isolation. About 3000Å of Al was evaporated on β-SiC by a vacuum evaporator and patterned by photolithography processes to serve as an etching mask. The mesa sizes defined by the Al pattern were 60μm, 80μm, 120μm and 240μm in diameter.

The RIE process was carried out in a SF_6 plasma. The flow rate of SF_6 was 25 sccm. The chamber pressure was 80 mtorr. The RF power was 150 W. Under these conditions, the etch rate of the β-SiC is about 800Å/min. The total etched depth of a β-SiC p-n mesa was 1.2 μm. After reactive ion etching, the Al mask was etched off in Al etching solution (H_3PO_4:HNO_3:CH_3COOH:H_2O=16:1:1:2).

The β-SiC p-n mesa structure surfaces were passivated by SiO_2. Two approaches were employed to grow thermal oxide. One was direct thermal oxidation of the β-SiC/TiC epilayer. The other was the CVD deposition of Si on β-SiC/TiC and then thermal oxidation of the Si/β-SiC/TiC.

β-SiC was thermally oxidized at 1150°C in wet oxygen for one hour. The sample was loaded into the oxidation furnace at about 800°C in 1.9 slm Ar flow, and then the furnace was heated to 1150°C. The oxidation was started by introducing 1.6 slm O_2, passing through a water bubbler, into the furnace and bypassing Ar flow. The water temperature was kept at 70°C and the flow rate of water vapor carrier by dry O_2 was 391 sccm. The oxidation was terminated by introducing Ar and bypassing O_2. After oxidation, the sample was annealed in Ar for 30 min. at the oxidation temperature and then cooled down to about 800°C before the sample was unloaded from the reactor. The oxide thickness from one hour oxidation, measured by Dektak depth profiler, was 1400 Å.

The Si/β-SiC/TiC structure oxidation process included two steps: (1) Si deposition on β-SiC/TiC; (2) thermal oxidation. Si deposition was performed in the MOCVD reactor using SiH_4. β-SiC was heated to 950°C in 2.9 slm in H_2. After temperature stabilization, 1 sccm SiH_4 was introduced into the reactor chamber to start growth. Growth was terminated by bypassing SiH_4. Then 2.9 slm Ar was introduced into the reactor and H_2 was bypassed. This caused the temperature to ramp from 950°C to about 1100°C because

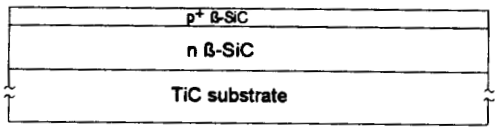
Ar has lower heat capacity than H_2; this was done to enhance the Si/β-SiC interface reaction. Then the sample was cooled in Ar. To determine the Si deposition rate, the Si/β-SiC sample was patterned by photoresist and etched by a Si etching solution (HNO_3:HF:H_2O=15:1:15). The growth rate, determined by Dektak profiler measurement was 150Å/min.

The procedures for Si/β-SiC/TiC oxidation were similar to those for β-SiC/TiC oxidation as described above, except the oxidation temperature was much lower, typically 950°C. At this temperature, the β-SiC oxidation rate is extremely low and oxidation was expected to terminate at the Si/β-SiC interface. The required Si oxidation time was estimated from the Si thickness and the Si oxidation rate as determined by Dektak measurement. To grow a SiO_2 layer of thickness x, a layer of 0.44x of Si is consumed.

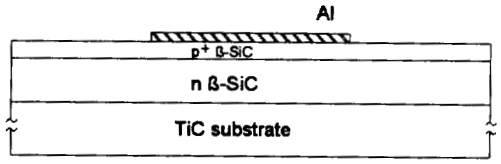
For the diode passivation, 750Å Si was first deposited on the mesa surfaces by CVD and then oxidized at 950°C in wet oxygen for 45 min. to grow about 1700Å SiO_2.

Ohmic contacts for n-type and p-type β-SiC were TiC and Pt, respectively. The epitaxial growth interface of n^+ β-SiC/TiC formed the n-type ohmic contact. To form the p-type ohmic contact, an oxide window was opened on the β-SiC p-n mesa. The Pt was deposited by DC sputtering. To insure good adhesion of Pt to β-SiC, a DC Ar plasma was established in the chamber for 10 min. to sputter clean the β-SiC sample surface prior to Pt sputtering. The chamber pressure during the Pt sputtering was $2x10^{-2}$ torr and the DC power was 600W. 1000Å Pt was sputter-deposited on the sample at a rate of about 350 Å/minute, after which the unwanted metal was lifted off in acetone.

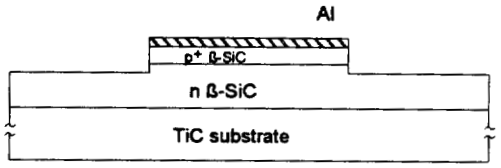
1. ß-SiC pn structure epitaxial growth



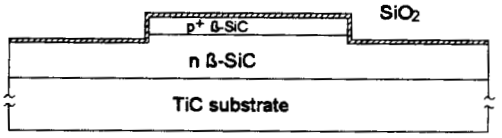
2. Al deposition and patterning



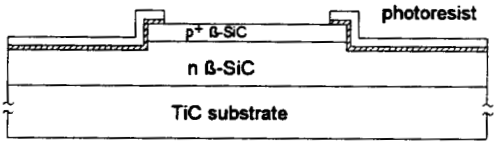
3. Reactive ion etching ß-SiC



4. Surface passivation



5. SiO_2 etch for contact



6. Pt sputtering and lift-off

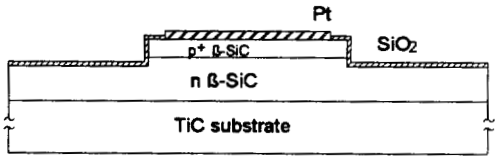


Fig. 5.2. Process steps for β-SiC p-n junction diode fabrication

5.2 β-SiC p-n diode characterization

Fig. 5.3 is a typical linear I-V curve obtained from a β-SiC p-n diode with a radius of 30μm. Measurement was mad at room temperature. Clearly, the diode is rectifying with relatively high reverse leakage current (I_L). At a reverse bias of 5V, the room temperature I_L is about 40μA. The ideality factor of the diode is about 3.5. The series resistance is on the order of 1KΩ.

To further investigate the possible cause of the large reverse leakage current, the effects of surface passivation and junction area on the diode I-V characteristics were studied.

Fig. 5.4 shows the reverse current density of the β-SiC p-n diodes fabricated using different surface passivation processes: no oxide passivation; β-SiC oxidation; and Si oxidation. Clearly, the surface passivation can reduce the leakage current. The Si/β-SiC structure oxidation process appears more effective than the β-SiC oxidation process.

Fig. 5.5 shows the reverse leakage current density of the β-SiC p-n diodes with different diode areas. The diodes were fabricated using different surface passivation conditions. In case of no passivation (Fig. 5.5 (a)), the diodes with the smallest size (r=30μm) have the largest leakage current density. For the diodes passivated by β-SiC oxidation (Fig. 5.5 (b)) or Si/β-SiC oxidation (Fig. 5.5 (c)) process, diodes with the smallest size have the smallest leakage current density. This implies that surface passivation is more effective for small size diodes, probably because that small diodes have larger percentage of side wall area to junction area ratios.

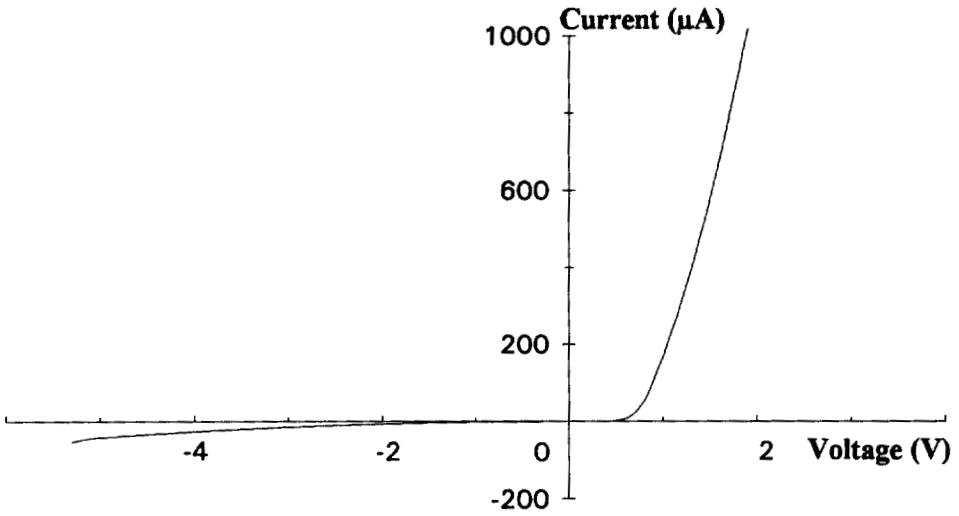


Fig. 5.3. The typical β-SiC p-n diode I-V curve.

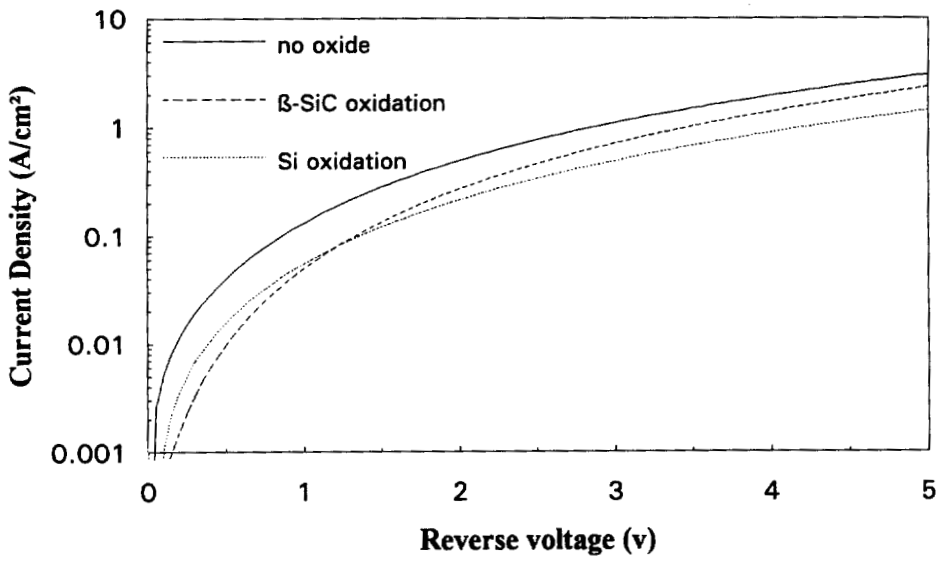


Fig. 5.4. Reverse current density of β-SiC p-n diodes fabricated using different surface passivation processes.

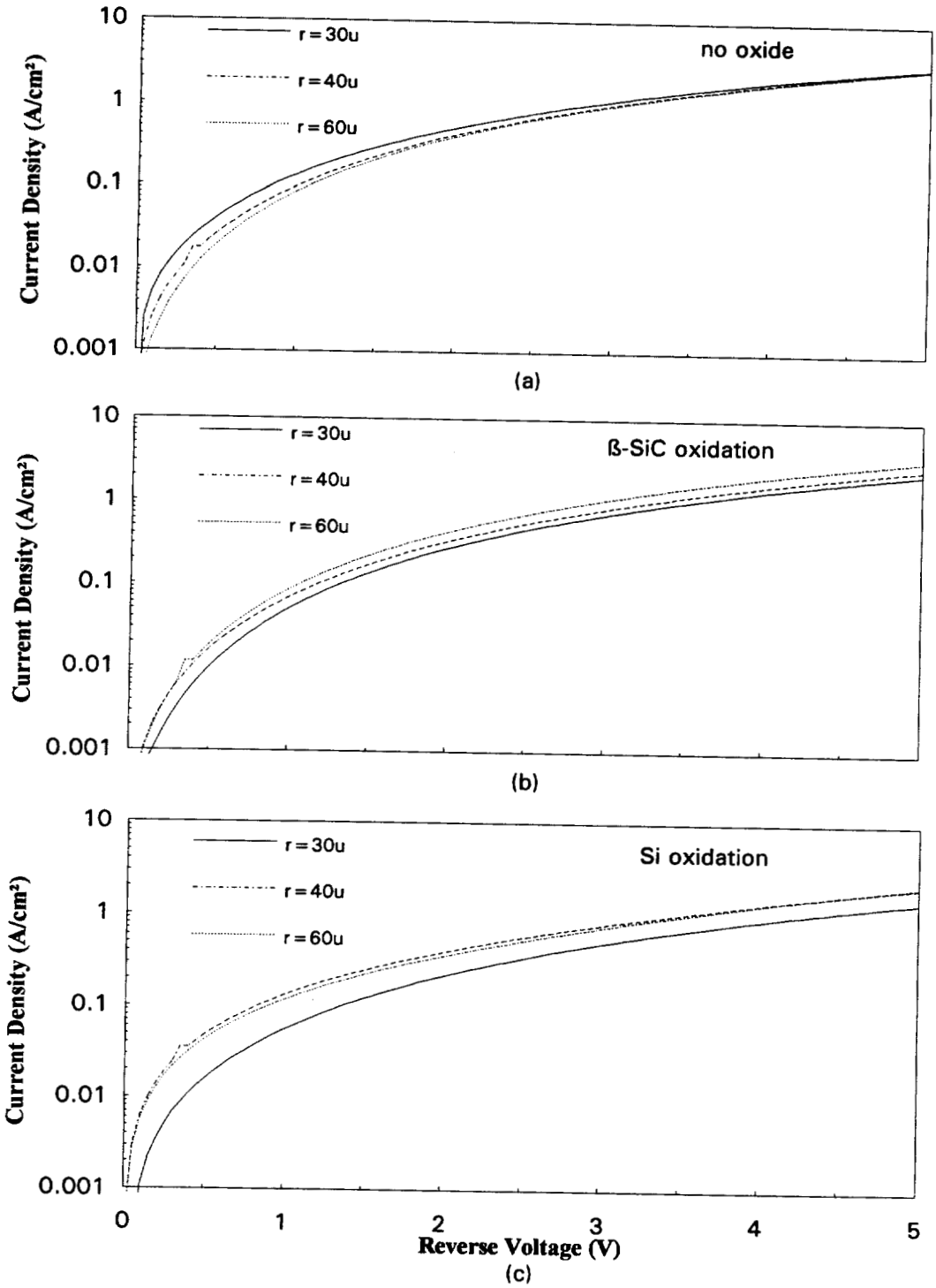


Fig. 5.5. Reverse current density of β-SiC p-n diodes with different diode areas.

5.3 Discussion of the experimental results

To understand the characteristics of the β-SiC p-n diodes described above, consider the mechanisms for the current flow across a semiconductor p-n junction and their relations to the process conditions employed in the β-SiC p-n diode fabrication.

The current flow across a semiconductor p-n junction has been treated in the literature in detail, for example, by Shockley[136], Sah *et al.*[137], and Sze[19]. The mechanisms of the current flow across the p-n junction are:

(1) Diffusion of minority carrier across the space charge region;

(2) Recombination or generation of carriers in the space charge region;

(3) Surface-leakage currents;

(4) Tunneling effect;

(5) series resistance.

In most common cases, for a p-n junction diode, the current in the forward direction can be written as:

$$J_F \sim \exp\frac{qV}{nkT}.$$

Where q is the electron charge, k is Boltzmann's constant, T is temperature, n is the diode ideality factor, and V is the voltage across the p-n junction.

When the diffusion current dominates, n equals to 1; and when the recombination current dominates, n equals to 2. The ideality factor of our β-SiC p-n junction diode is about 3.5. This n value dose not fall within the range $1<n<2$, which means that neither diffusion nor recombination current dominates the β-SiC diode forward I-V characteristics.

For a p^+-n junction, only considering diffusion component in the neutral region and the generation current in the depletion region, the total reverse current can be approximately given by:

$$J_R = J_s + J_{R-G} = q\frac{n_i^2}{N_D}\cdot\frac{D_P}{L_P} + \frac{qn_i w}{\tau_{eff}}.$$

Where n_i is the intrinsic carrier concentration, D_p is the minority carrier diffusion coefficient for holes, L_p is the diffusion length for holes ,and N_D is the donor concentration. w is the width of the space charge region. τ_{eff} is an effective lifetime which is reversely proportional to the concentration N_t of the R-G center in the middle of the band gap, according to the Shockley-Read-Hall (SRH) model[137-139].

For semiconductors with large bandgap and small value of n_i, the generation current is dominant. In case of β-SiC, the diffusion current component can be totally ignored. Since the generation current is proportional to $1/\tau_{eff}$ or N_t, reverse leakage current in a β-SiC p-n diode could be relatively high if the material has a small τ_{eff} or a high impurity concentration. However, from our experimental data, assuming that all reverse leakage currents are due to the generation current, the estimated τ_{eff} is on the order of 10^{-23} s, which is unreasonably small. This indicates that generation current component is not a dominant factor in the reverse leakage current of our β-SiC p-n junction diode.

The fact that the I-V characteristics of our p-n junction diodes can not be quantitatively explained by the ideal diffusion and recombination-generation mechanisms could imply problems in the β-SiC materials. We suspect that the high impurity density in the DSE ($Si_2C_2H_{10}$) reactant source and subgrain boundaries in the TiC_x substrate could be the causes for the problems.

Commonly used reactant sources for β-SiC grown on Si and 6Hα-SiC substrates are high purity SiH_4 and C_2H_4 (or other hydrocarbon gas). The background carrier concentrations of those β-SiC materials are below 1×10^{17} cm^{-3}. However, extensive experimental studies led to the conclusion that these reactant sources could not be used to achieve complete nucleation and epitaxial growth of β-SiC on TiC substrates[68]. The single reactant source used in this work, DSE, was specially developed for the β-SiC growth on TiC substrates. The total concentration of the trace element impurities in the DSE, including N, Al, Sb, Mn, As, Hg and P, is about 20 ppb. This high concentration of impurities can cause a high background carrier concentration (1×10^{18} cm^{-3}) and/or a high density of trap levels in the β-SiC epilayers. High carrier concentration usually corresponds to high field in the junction which would cause band-to-band tunneling to occur. The deep trap levels can serve as available states in the band gap for carrier hopping through the junction, which will dramatically increase the tunneling probability. Any or all of these mechanisms can cause the high reverse leakage currents measured in our β-SiC p-n junction diodes.

The subgrain in the TiC substrate is another problem associated with the β-SiC materials. The epitaxial β-SiC layer reproduces the subgrain structure from the substrate. The subgrain boundaries can act as unpassivated surface area or result in deep level states in the band gap to provide shorting paths for the current across the junction. Although many efforts have been made to carefully evaluate and prepare TiC substrates as described in Chapter 3, the TiC substrates free of subgrains are very limited and often have other problems, such as small size and high pit densities, and are thus not suitable for device fabrication.

Surface leakage current is another component of the reverse leakage current. Surface passivation has always been an important issue in semiconductor device fabrication. Dangling bonds or nonstoichiometry of a semiconductor surface may induce a high density of charged states and recombination centers which degrade the performance of electronic devices. Early studies on Si p-n junction and transistor characteristics indicated that surface recombination and/or channel current was part of the reason that the ideality factor of the p-n junction forward current-voltage curve was larger than one and might be greater than 4 for large channels, and that the reverse leakage current was larger than the theoretically predicted value[140]. Silicon dioxide (SiO_2) has been successfully used to passivate Si surfaces so that device performance can be controlled and stabilized.

The properties of β-SiC surfaces are expected to be more complicated than those of Si, which is very common for a compound semiconductor. Detailed studies on β-SiC surface behavior have not been reported. However, it is known that RIE produces a C-rich β-SiC surface which is very conductive[93]. Therefore, surface passivation of the mesa structure after RIE is an important step in β-SiC p-n diode fabrication. Our experimental results have shown that both surface passivation methods, β-SiC oxidation and Si/β-SiC oxidation, can reduce the leakage current in β-SiC p-n diodes. This is an indication that the surface leakage current is one of the important components in the total reverse leakage current in the diodes.

Our preliminary results also show that Si/β-SiC oxidation is more effective than β-SiC oxidation as a passivation process. This is not unexpected. The reported results indicate the existence of carbon in the thermal oxide grown on β-SiC and at the SiO_2/β-SiC interface[85]. This means that there are carbon-related defects in the oxide which degrade oxide quality. On the other hand, Si/β-SiC oxidation seems to be an effective

passivation method. CVD Si can react with the C-rich β-SiC surface to reduce the free C density. Subsequently, high quality SiO_2 can be obtained using a standard Si oxidation process, which requires relatively low temperature so that the β-SiC underneath the Si would not be oxidized.

Although both passivation processes have shown the effects on reducing the β-SiC p-n diode leakage current, at this point, we can not conclude that surface leakage current has been totally eliminated. The high diode leakage current existed after passivation (Fig. 5.5 (b), (c)) could be still partly due to the surface leakage current. Further investigation for β-SiC surface passivation should be performed. The dependence of the passivation effects on oxidation conditions, such as temperature, oxide thickness, annealing treatment of the oxide, should be determined and optimized to minimize the surface leakage current in β-SiC devices.

Chapter 6
Conclusions

A metalorganic chemical vapor deposition (MOCVD) process was used to synthesize β-SiC p-n structures grown on TiC_x substrates. Mesa type p-n junction diodes were fabricated in these device structures, using reactive ion etching, oxide passivation, and metallization techniques.

A β-SiC epitaxial growth process, using TiC_x as substrate and 1,2-disilylethane (DSE) as reactant source, was optimized in an inverted-vertical atmospheric pressure MOCVD reactor. Repeatable nucleation and epitaxial growth conditions were established. This includes *in-situ* TiC_x surface preparation, TiC buffer layer growth, and β-SiC CVD growth conditions. Studies of β-SiC films by Nomarski microscope, SEM and ECCP showed that the optimum growth temperatures were in the range of 1240°C to 1290°C, and the maximum β-SiC epitaxial growth rate was 6μm/hr. The β-SiC epilayers grown under optimized growth conditions were free of antiphase domains and stacking faults.

β-SiC epilayers were doped with nitrogen and aluminum to produce n-type and p-type β-SiC, respectively. The electrical properties of undoped and doped β-SiC epilayers were investigated. The undoped and nitrogen doped β-SiC epilayers were n-type as determined by hot probe. P-type β-SiC was obtained when the Al source (DMAH) flow rate was higher than 0.3 sccm at a β-SiC growth rate of 5μm/hr. Ag Schottky diodes were fabricated on undoped and Al-doped p-type β-SiC. As determined by C-V measurement, the background concentration of undoped β-SiC was about 1×10^{18} cm^{-3} n-type.

The reactive ion etching processes, using fluorinated gases $CF_4/O_2/Ar$ and SF_6, were developed for β-SiC/TiC etching. The β-SiC etch rate appeared to be controlled by a combination of the chemical reaction of β-SiC with fluorine and/or oxygen radicals and the ion bombardment (DC bias). The β-SiC etching under established conditions was highly anisotropic with etch rates of 100-1000Å/min. SF_6 gas was determined to be the preferred reactant source over the $CF_4/O_2/Ar$ gas mixture for β-SiC RIE process because SF_6 etching had higher efficiency, introduced less damage, and resulted in better surface morphology

Two surface passivation processes, thermal oxidation of β-SiC and thermal oxidation of a Si/β-SiC structure, were employed in p-n junction diode fabrication. Both approaches reduced leakage currents in the diodes. However, Si/β-SiC oxidation appeared to be more effective.

The I-V characteristics of the β-SiC p-n junction diodes fabricated showed rectification with relatively high reverse leakage current, an ideality factor ~3.5 and series resistance on the order of 1kΩ. The cause of the high leakage current was attributed to the high impurity concentration in the DSE reactant source, to the subgrains in the TiC_x substrates, and possibly to the surface leakage current.

Further development of β-SiC device technology based on β-SiC/TiC structures will require purification of the DSE reactant source, elimination of the subgrains in TiC substrates, and further investigation of β-SiC surface properties to optimize β-SiC surface passivation process. Along with this development, more detailed characterization should be performed to well understand the mechanism and to monitor the progress in β-SiC material quality improvement and in device process optimization. The useful measurements include p-n junction I-V characteristics versus temperature measurement to

determine the current flow mechanism; Hall measurement to determine the carrier concentration, impurity compensation and carrier mobility; β-SiC MOS structure temperature-dependent C-V measurement to determine the interface state density of a SiO_2/β-SiC structure. With all these efforts, we expect that β-SiC p-n junction performance will be dramatically improved and β-SiC device technology based on β-SiC/TiC structure will fully exhibit its advantages.

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