Investigation of Parameters Affecting Polysilicon Characteristics for Laser Annealed Polysilicon Thin Film Transistors

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c	heat capacity
C_{OX}	oxide capacitance per unit area
d	density
d_{ch}	gate induced channel thickness
D_n	diffusion constant for electrons
E	energy variable
e_n	electrons emitted per second from electron occupied generation-recombination centers
e_p	holes emitted per second from hole occupied generation-recombination centers
E_B	potential barrier height at grain boundary
E_c	energy of conduction band edge
E_F	Fermi energy
E_{GA}	Location in bandgap of deep, acceptor-like trapping states
E_{GD}	Location in bandgap of deep, donor-like trapping states
E_i	intrinsic Fermi energy
E_t	trap energy level
E_v	energy of valence band edge
F	electric field
$f(E,n,p)$	occupancy function of a trap level
f_t	probability of electron occupancy of a trap at energy E_t
G_n	electron generation rate

G_p	hole generation rate
H	latent heat of melting
h	Planck's constant
$\hbar$	h/2π
I_D	drain current
I_{leak}	leakage current in the off-state
I_{Off}	minimum drain current as a function of gate voltage
I_{On}	maximum drain current as a function of gate voltage
I(-20)	drain current when gate voltage = -20 V
J_n	electron current density
J_p	hole current density
k	Boltzmann constant
L	true length of channel region
L_{mask}	mask length of channel
m_e^*	electron effective mass
N	electron free carrier concentration
N_A	number of occupied acceptor states per unit volume
N_{AG0}	maximum density of deep, acceptor-like trap states in bandgap
$N_{AG}(E)$	energy distribution of the acceptor, deep trap state density
$N_{AT}(E)$	energy distribution of the acceptor, tail trap state density
N_D	number of occupied donor states per unit volume
N_{DG0}	maximum density of deep, donor-like trap states in bandgap

$N_{DG}(E)$	energy distribution of the donor, deep trap state density
$N_{DT}(E)$	energy distribution of the donor, tail trap state density
$N(E)$	distribution for the areal density of trap sites
N_{GA}	total density of acceptor-like deep states
N_{GD}	total density of donor-like deep states
n_i	intrinsic carrier concentration
N_t	grain boundary trap density
N_{TA}	conduction band edge intercept density of states
N_{TD}	valence band edge intercept density of states
p	free hole concentration
q	electronic charge
Q_{BIT}	fixed charge on backside polysilicon/SiO_2 interface
Q_f	mobile charge per unit area
Q_{it}	fixed charge density at the polysilicon/SiO_2 gate oxide interface
R	optical reflectivity at 308 nm
R_D	series resistance of drain
R_n	electron recombination rate
R_p	hole recombination rate
R_S	series resistance of source
R_{ser}	contact series resistance of channel (series resistance of source region + series resistance of drain region)
R(I)	regime of operation within which the poly-Si film is annealed with a low energy density and characterized by a stratified film

R(II)	regime of operation within which the poly-Si film is annealed with an intermediate energy density and characterized by large, uniform grain growth.
R(III)	regime of operation within which the poly-Si film is annealed with a high energy density and characterized by bi-modal grain growth
S	subthreshold swing
s_n	poly-Si/gate oxide interface recombination velocity for electrons
s_p	poly-Si/gate oxide interface recombination velocity for holes
T	absolute temperature
t	time variable
U	rate of emission of carriers into the bands
U_e	total rate of emission of electrons from traps to conduction band
$U_e(E)$	rate of emission of electrons from traps to conduction band
U_h	total rate of emission of holes from traps to valence band
$u(t-\tau)$	step function which turns laser pulse instantaneously off at time τ
V_{DS}	drain-source voltage
V_{FB}	flat band voltage
V_G	gate voltage relative to source
Vol	volume over which the average vertical electric field is large enough to cause significant thermionic field emission
V_T	threshold voltage
V_{th}	carrier thermal velocity
W	channel width
W_{GA}	characteristic decay energy for acceptor-like deep states
W_{GD}	characteristic decay energy for donor-like deep states
W_{TA}	characteristic decay energy for acceptor-like tail states

W_{TD}	characteristic decay energy for donor-like tail states
x	position variable parallel to top poly-Si surface
y	position variable perpendicular to top poly-Si surface
α	optical absorption coefficient at 308 nm
ε_{si}	dielectric constant of silicon
$\vartheta(T)$	unit step function changing from 0 to 1 at the melting temperature
ϕ_f	Fermi potential
κ	thermal conductivity
μ	field-effect mobility
μ_{eff}	total effective channel mobility
μ_G	intra-grain mobility
μ_{GB}	mobility at the grain boundary
μ_{LF}	low frequency conductivity mobility
μ_n	electron carrier mobility used in ATLAS
ρ	charge density
Σ	source term for laser melting model
σ_{ijE}	capture cross-section for electron where i is either T for tail distribution of G for Gaussian and j is either D for donor-like state or A for acceptor like state
σ_{ijH}	capture cross-section for hole where i is either T for tail distribution of G for Gaussian and j is either D for donor-like state or A for acceptor like state
τ	laser pulse duration
$\tau_e(E)$	time constant for an electron tunneling from E to the conduction band edge
$\tau_h(E)$	tunneling time constant for a hole into the valence band

ψ	electrostatic potential
ψ_i	intrinsic electrostatic potential
ψ_n	quasi-Fermi level for electron
ψ_s	surface potential

List of Acronyms and Abbreviations

AFM	atomic force microscopy
AMLCDs	active matrix liquid crystal displays
AR	anti-reflection (coating)
a-Si	amorphous silicon
CRT	cathode ray tube
DOS	density of states
ED	energy density
ELA	excimer laser annealing
FPDs	flat panel displays
GS	grain size
HT	high temperature
ITO	indium tin oxide
LCs	liquid crystals
LCDs	liquid crystal displays
LIPSS	laser induced periodic surface structure
LT	low temperature
MOSFET	metal oxide semiconductor field effect transistor
PECVD	plasma enhanced chemical vapor deposition
PMLCD	passive matrix liquid crystal display
poly-Si	polycrystalline silicon (polysilicon)
RT	room temperature

RTA	rapid thermal annealing
SIMS	secondary ion mass spectroscopy
SLG	super lateral growth
SPC	solid phase crystallization
SSELA	single shot excimer laser annealing
STN	supertwist nematic
TEM	transmission electron microscopy
TEOS	tetraethylorthosilicate
TFTs	thin film transistors
TN	twisted nematic

Abstract

Investigation of Parameters Affecting Polysilicon Characteristics for Laser Annealed Polysilicon Thin Film Transistors

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Thin-film transistors (TFTs) are a class of field-effect devices produced on insulating substrates rather than single crystal silicon. The channel of such devices is typically made of either polysilicon (poly-Si) or amorphous silicon (a-Si), and for this reason, the performance is inferior to their single crystal counterparts. However, TFTs find widespread use in display applications, where the substrate must be translucent. Because of this, and due to the proliferation of portable, flat-panel displays (FPDs), research on TFTs has increased rapidly over the last quarter century.

As a result of the limitations of amorphous silicon devices, including low carrier mobility and on-current, interest in polysilicon TFTs has grown. Polysilicon films for use in TFTs can be prepared using a variety of methods, but excimer laser annealing (ELA) of an initially amorphous thin film has, to date, produced the best performing devices. In this thesis, the effect of various parameters on the qualities of laser annealed polysilicon and polysilicon TFTs was investigated. These included the laser annealing ambient, use of low temperature substrate heating during laser annealing, the effect of SiO_2 barrier layers, laser activation of implanted dopants, use of an anti-reflective coating, and multiple laser scans.

By pursuing the three-fold effort of materials characterization, modeling and device characterization, the underlying features determining device performance were uncovered. In fundamental terms, three qualities influenced most directly the ultimate capabilities of laser annealed poly-Si TFTs: the grain size, the interface characteristics and the incorporation of impurities. By maximizing the grain size, the density of grain boundary defects was reduced. This improved the on-state and off-state qualities by

presenting fewer trap states to fill and limiting the availability of intermediate energy states in the band-gap for carrier tunneling. Interface qualities, stemming from the choice of dielectric materials and possible interface damage, have been shown to affect the subthreshold characteristics. By studying the affect of various ambients on the ELA process, it was determined that incorporation of oxygen into the poly-Si thin film increased the number of scattering centers and also increased the trap state density by disturbing the Si matrix.

Chapter 1
Introduction

1.1 Motivation

Thin-film transistors (TFTs) are a class of field-effect devices produced on insulating substrates, usually glass or quartz, rather than single crystal silicon. The channel of such devices is typically made of either polysilicon (poly-Si) or amorphous silicon (a-Si), and for this reason, the performance is inferior to their single crystal counterparts. However, TFTs find widespread use in display applications, where the substrate must be translucent. Because of this, and due to the proliferation of portable, flat-panel displays (FPDs), research on TFTs has increased rapidly over the last quarter century. FPDs, and in particular active matrix liquid crystal displays (AMLCDs), are expected to challenge and eventually surpass the production of standard cathode ray tube (CRT) displays in the near future. In 1993, approximately 11 billion CRT displays were sold versus only 2 billion AMLCDs[1]. By 1998, between 10 and 15 billion AMLCDs were sold versus 18 billion CRTs. Development of less expensive and more functional TFTs is necessary to meet the demands of the FPD industry. This is, in essence, the impetus for this body of work.

The emphasis of this project was on the optimization of a process to produce laser-annealed poly-Si TFTs. Using the available tools, the parameters that affect the quality of the poly-Si film were varied and conditions that enhanced beneficial characteristics were applied to produce devices. The material properties were then related to device performance, and causal relationships established. Throughout the study, an eye was maintained on manufacturability and cost effectiveness. In the end, prescriptions were developed which struck a balance between performance and throughput.

1.2 History of the Thin-Film Transistor

Unbeknownst to most people, the TFT was the first solid state amplifier ever patented[2]. In 1933 a patent was issued to J. E. Lilienfeld and in 1934 another was issued to O. Heil for devices fitting the description of TFTs. Though there is no evidence that these devices ever worked, the concept for their operation was sound. At that time however, the quality of semiconductor materials was poor at best, and processes for making the devices were undeveloped.

The first report of an operational TFT was made in 1961 by P. K. Weimer[3], with CdSe as the semiconductor[2]. This was only one year after the first report of an operational metal-oxide-semiconductor field-effect transistor (MOSFET)[4], though the announcement of the point-contact transistor had occurred as early as 1948. After being successfully fabricated, both the TFT and the MOSFET stood as possible successor to the bipolar transistor. Companies such as RCA, GE, Hughes, IBM, Westinghouse and Zenith, to name a few, were working on both technologies in the early 1960s, but because MOSFETs were being made with a better understood material (silicon) and using more mature processes, the competition was not even close. By the mid 1960s, many of the problems associated with MOSFETs had been solved while TFTs suffered from poor reproducibility and instability. In 1971, Westinghouse was the only company still involved in TFT research.

Redemption for TFTs came through the development of FPDs. As early as 1972, using their TFT technology, Westinghouse produced the first operating AMLCD having dimensions 6 inches on a side and capable of both digital and gray scale operation. By 1973 they had a similarly sized active matrix electroluminescence display[5].

Work on liquid crystal displays (LCDs) was increasing rapidly in the early 80's based, among other things, on the need to generate displays for the portable computer market. Around this time, amorphous silicon (a-Si) began to emerge as a possible successor to CdSe for TFTs, and somewhat later polysilicon (poly-Si) came into fruition. The structure and materials used in modern TFTs were emerging, and globally, companies were taking interest. The blossoming FPD market has been the driving force behind TFT research until this day.

1.3 Liquid Crystal Displays

Because of the important role played by LCDs in the development of TFTs, this section gives a brief account of LCD technology. Liquid crystals are a class of organic materials in and of themselves that exhibit properties somewhere between those of a liquid and a solid crystal[6]. Though LCs flow like a liquid, the molecules can possess a long range, crystalline order, like a solid. They do not however exhibit the full three-dimensional order of ordinary crystalline solids. LC molecules are highly elongated, and because of this, certain physical properties, including the dielectric constant and the index of refraction, are anisotropic. As a result, the polarization direction of light passing through LC material can be rotated. The director of a liquid crystal is defined to be a vector parallel with the long axis of the molecule. Due to the permanent or induced dipolar nature of the molecules, the director tends to align itself with the direction of an applied electric field. These important qualities allow LCs to be used as optical switches in a liquid crystal cell.

LCs can be found in different phases. The nematic phase is characterized by parallel directors and random positional orientation of the molecules. This phase has a single degree of macroscopic order. In the cholesteric phase the director rotates in a spiral fashion from layer to layer, through the bulk of the material, and as with the nematic phase, the molecules can be found at random positions. The smectic phase is generally characterized by parallel director alignment and positional ordering of the molecules. This phase more closely resembles a solid than a liquid and has two degrees of macroscopic order.

1.3.1 LC Cells

The simplest LC cell is the twisted nematic (TN) type[7,8], as shown in figure 1-1[9].

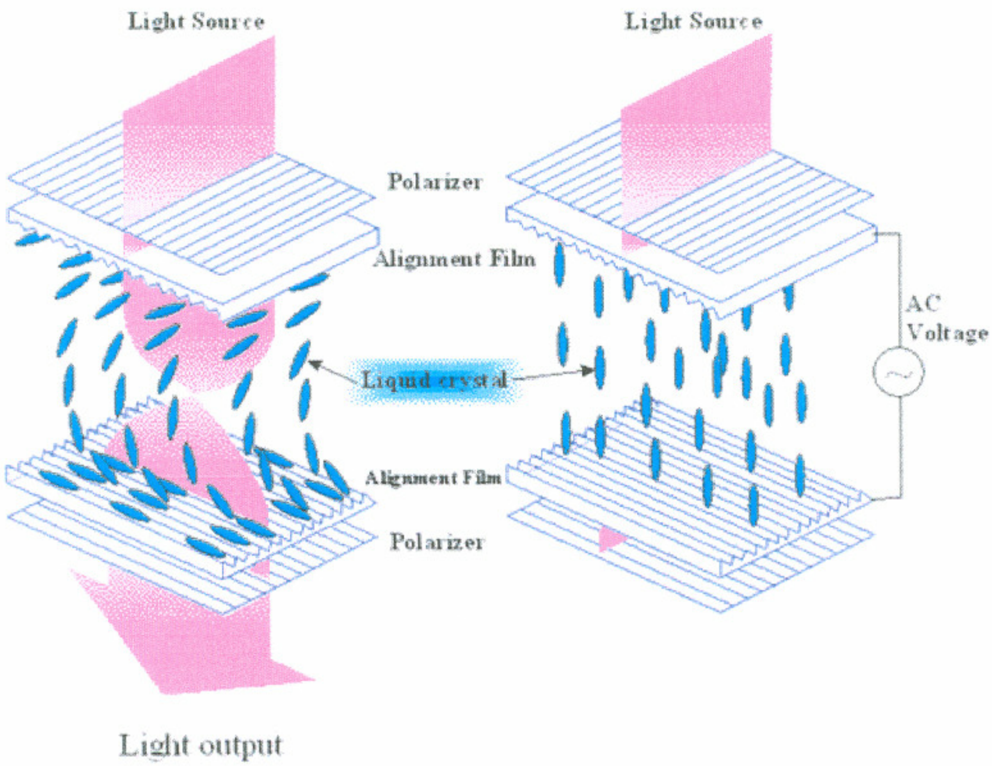


Figure 1-1: Schematic of a TN LC cell. On the left is the on state and on the right is the off state.

The nematic LC is sandwiched between 2 glass plates separated by 8 μm, or less. The outer surface of the glass is laminated with polarizing sheets. The inner surfaces are coated with patterned, transparent conductors, usually Indium-Tin Oxide (ITO). The ITO is covered with a thin polyimide layer, which is typically several hundred angstroms thick, and is unidirectionally rubbed. The rubbing serves to align the local director axis of the liquid crystal at the surface parallel to the rubbing direction. Since the upper glass plate is rubbed at a right angle to the rubbing direction of the lower plate, the director undergoes a 90° twist in the region between the substrates. If the polarizers are aligned in the rubbing directions, the cell will be 'normally on', meaning that in the absence of an applied field, light passing through the top polarizer will have its polarization rotated as it passes through the LC such that it will also pass through the bottom polarizer, as on the left side of figure 1-1. If a voltage difference of 3-5 volts is applied to the electrodes, an electric field perpendicular to the glass plates will be set up, and the LC molecules will align themselves with this field. Therefore, light passing through the top polarizer will then not be rotated and will not pass through the bottom polarizer. This is the off state, as shown on the right side of figure 1-1.

1.3.2 Addressing Schemes

In an LCD, cells are laid out in a matrix of pixels. For a black and white VGA display, the number of rows and columns is 640 by 480 respectively, meaning there are about 300,000 pixels total. In a simple *passive matrix liquid crystal display* (PMLCD), shown in figure 1-2[9], the two glass plates are patterned with strips of ITO that run at right angles to each other.

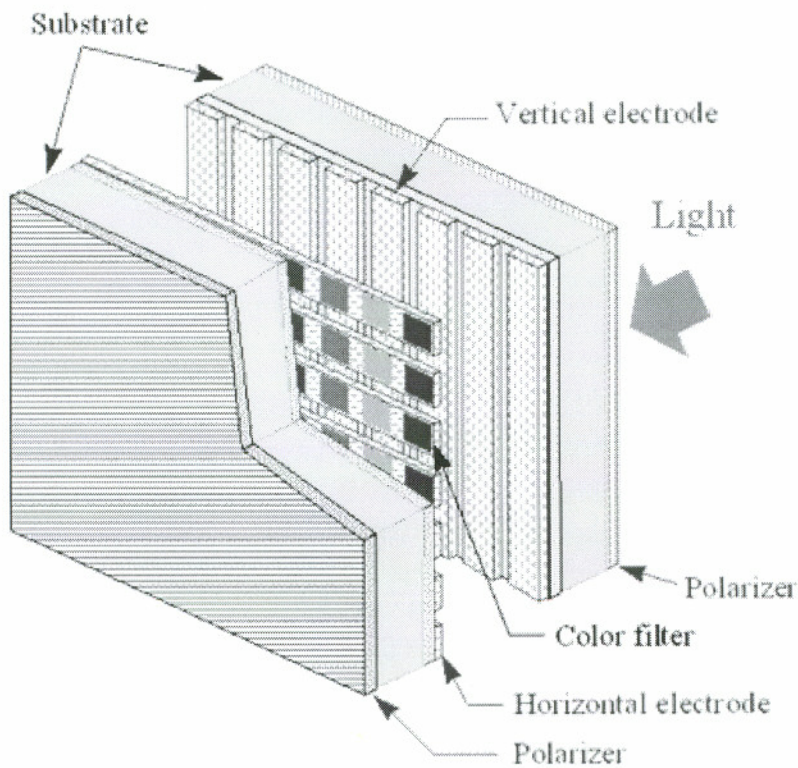


Figure 1-2: Schematic of a simple color PMLCD.

One strip is referred to as the data line and the other is the scan line. The areas where the strips overlap define the areas of the pixels. Through multiplexing, the $M \times N$ number of pixels can be addressed by $M + N$ electrical contacts to the display. The primary disadvantage of PMLCDs is that voltages cannot be arbitrarily changed at one element without affecting the voltages at other elements. This is known as crosstalk. The crosstalk problem creates a tradeoff between resolution and contrast, as it increases with the number of rows addressed.

To combat the problem of crosstalk, supertwist nematic (STN) displays were developed[10]. STN displays use cholesteric phase LCs to rotate the director up to 270° from the top to the bottom glass plate. In so doing, a steeper electro-optical curve is achieved, meaning that a smaller voltage difference is needed to change the state of a pixel from on to off or vice versa. This leads to a higher contrast ratio. A disadvantage of STN displays is that they are more expensive. In addition, cell response time is still problematic for large area applications.

Crosstalk is effectively eliminated with an *active-matrix liquid crystal display* (AMLCD), a schematic of which is shown in figure 1-3[9].

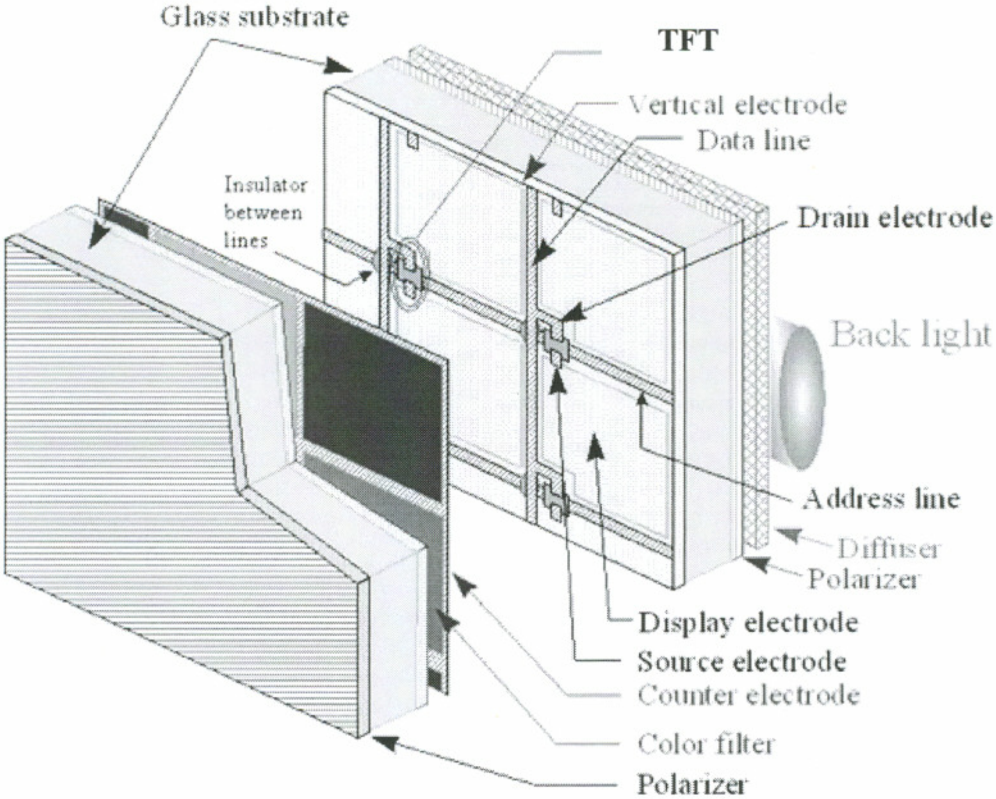


Figure 1-3: Schematic of a color AMLCD

In such a display, the pixels are arranged in an x-y matrix on the bottom glass substrate. The front panel is not patterned and acts as a ground electrode. Each pixel typically has a TFT, which operates as an analog switch to turn the pixel on or off. More specifically, the scan line is used to turn the TFT either on so that the LC cell can be charged to the voltage on the data line, or off to store the charge on the cell. In most cases, a storage capacitor is used in parallel with the LC to slow the pixel potential decay due to transistor leakage between frames. AMLCDs allow for simpler drive circuits than PMLCDs, better resolution, higher brightness and can supply high-speed video. At the same time, the fabrication cost is still greater. However, if the scanning and driving circuits can be implemented on the glass substrates, the cost could be lowered by forming all of the necessary circuitry in one process.

1.4 Amorphous Silicon vs. Polysilicon TFTs

TFTs can be separated into three classes: amorphous silicon TFTs, high temperature polysilicon TFTs, and low temperature polysilicon TFTs. Currently, most AMLCDs are built with a-Si, but an increasing proportion of the research being conducted on TFTs is directed towards poly-Si[11]. If a-Si is the material of today, poly-Si promises to be the material of the future.

Amorphous silicon TFTs enjoy several advantages over poly-Si. Due to the larger bandgap of a-Si (around 1.7 eV) versus poly-Si (around 1.1 eV), the leakage current is considerably less. For this reason, when used in an LCD array, the voltage across the LC cell is maintained more effectively between frames. Amorphous silicon technology is also fully compatible with inexpensive glass substrates. A standard a-Si TFT processing sequence does not require temperatures above 300 °C[4], making them ideally suited to cheaper, low-temperature glass substrates. In addition, because a-Si is a more mature technology, due in part to its use in the solar cell industry, manufacturing costs of a-Si TFTs are less than poly-Si. Specifically, polysilicon TFTs require 2 additional large area processes, namely hydrogenation and ion implantation, which raise production costs.

Despite the disadvantages, the advantages of poly-Si over a-Si TFTs will likely increase their use over time. The on-state characteristics of poly-Si TFTs are far superior to their a-Si counterparts. Hole and electron mobilities are higher, the drive current is larger and the subthreshold slope is improved. As a result, devices can be made smaller, increasing the aperture ratio, producing brighter and lower power displays. Moreover, shorter pixel charging times increase the maximum display speed.

Other advantages of poly-Si TFTs can be derived from the ability to build circuits using these devices, other than simple switches[12]. Displays with scan circuits, data-address circuits, and drivers integrated along the sides of the display matrix have already been demonstrated[13]. Because both n-channel and p-channel poly-Si TFTs can be fabricated, CMOS structures, and therefore shift registers, are possible.

1.5 Polysilicon TFTs

Polysilicon TFTs are classified according to the maximum temperature used during processing. In a truly low temperature (LT) process, all processing must be done below 450 °C, in order to use low cost glass substrates. Operating below 600 °C is also classified as LT but requires a more expensive high melting point glass. Above 600 °C, quartz substrates are necessary, and the process is classified as high temperature (HT). In this case, the substrates are too expensive for large displays and thus find use in small displays, as in projection systems or viewfinders.

When producing poly-Si for manufacturing, it is necessary to consider throughput, uniformity and the maximum processing temperature. The desired films have a large grain size, with a narrow grain size distribution, low surface roughness, and a low density of intra-grain defects. In an LT process, polysilicon can be formed by (a) direct deposition of poly-Si, or (b) deposition of a-Si followed by subsequent crystallization. To date, process (b) has yielded better results in terms of TFT performance. Conversion of a-Si to poly-Si can be done by solid phase crystallization (SPC) furnace annealing, rapid thermal annealing (RTA), or excimer laser annealing (ELA).

For SPC, implantation with Si atoms precedes a long (≈ 40 hr.) furnace annealing step. Grain sizes can be as large as 2 μm, though the grains are heavily defected. The uniformity of the films is acceptable. Maximum field effect mobilities for n-type devices of around 100 cm^2/Vs have been achieved, though values between 25-50 cm^2/Vs are more typical[14]. Advanced techniques to control nucleation and create devices on single crystals have also being investigated[15]. Due to the length of the annealing step, throughput remains a problem.

Throughput is greatly improved when RTA crystallization is performed using Xenon arc lamps, with annealing times of only a few minutes for temperatures between 675-750 °C. RTA systems can anneal around 60 substrates/hr., and TFT performance is nearly identical to those annealed in a conventional oven[16]. However, during processing, a thin layer of the substrate is heated beyond the strain temperature of the glass. For this reason, warpage due to uneven heat distribution is difficult to avoid, leading to problems with subsequent lithography steps.

In ELA of a-Si, pulses of ultra-violet radiation are directed at the wafer surface. The pulses melt the irradiated area, and thus the poly-Si crystallizes out of a liquid, rather than a solid state, creating grains with a low level of intra-grain defects and maximum grain sizes on the order of 1 μm. This in turn leads to TFTs with high electron and hole mobilities. With ELA, it is not uncommon to see n-type devices with field effect mobilities around 200 cm^2/Vs. Due to the short pulse duration and hence melt duration caused by ELA, film temperatures can reach as high as 1400 °C without damaging the underlying substrate. Additionally, it is possible to effectively activate implanted dopants with an excimer laser. ELA is the most promising technique for creating high quality TFTs on inexpensive substrates.

Despite recent advances, there are still many problems to overcome associated with ELA. Due to the narrow range of energy densities needed to achieve large grain growth, pulse to pulse variations and beam non-uniformities can lead to a wide distribution in grain sizes on an annealed wafer. For this reason, device uniformity is problematic. In addition, surface roughness of ELA poly-Si is greater than SPC. Throughput remains a problem, especially with systems using a high pulse to pulse overlap (> 90%). Some equipment manufacturers apply substrate heating to increase the average grain size of the annealed film, which again hinders throughput. 20-30 substrates/hr. are common.

1.6 Overview of Dissertation

The remainder of this dissertation focuses on laser crystallization of amorphous silicon thin films, and applications in thin film transistors. In chapter 2, the properties of ELA polysilicon are studied. Samples are laser annealed under various conditions, and the important parameters relevant to device functionality are measured. In chapter 3, characteristics of devices produced using ELA are presented and the qualities are related to the materials attributes. In addition, some theoretical aspects of TFT operation are discussed and a two dimensional simulation of a poly-Si TFTs is produced. A summary of important conclusions is given in chapter 4, along with possible directions of future work.

Chapter 2

Excimer Laser Annealed Polysilicon Thin Films

2.1 Introduction

In order to produce high quality ELA poly-Si TFTs, a thorough understanding of the active poly-Si layer is necessary. For this purpose, ideally, a poly-Si film should have a large average grain size. The larger the grains, the closer the devices approach single crystal transistor characteristics. The surface roughness of the film should also be kept to a minimum. Rougher surface may lead to the creation of poly-Si/SiO_2 interface traps and a reduction in carrier mobility due to surface scattering. In addition, poly-Si films need to be uniform, both macroscopically and microscopically. The sensitive nature of the laser annealing process can lead to inhomogeneties, which create large variations in device performance. Obviously, implementation of solid-state devices in either a circuit or as switches requires a high degree of uniformity.

The most common problem that plagues ELA is the narrow process window associated with the development of a large and uniform grain size[17]. Moreover, the surface roughness inherent to this process is also troublesome[18]. Currently, equipment manufacturers promote ELA at elevated temperatures and under high vacuum. An exception to this trend is the so-called single-shot ELA (SSELA), where room temperature (RT) and air ambient are utilized. In any case, the selection of ambient affects material characteristics and is intimately related to process simplicity and film quality. The choice of substrate temperature during ELA is another important consideration in terms of throughput and film quality. To simplify the process, it is necessary to eliminate substrate heating, with minimal compromise on the film characteristics. The effectiveness of ELA is ultimately related to efficient heat distribution during the heat-up step, and slow cooling during the cool-down step. Both processes are affected by a multitude of factors. Clearly, process optimization is essential for satisfying the various constraints while maintaining quality.

In this chapter, a study of poly-Si films annealed by a XeCl excimer laser as a function of key process parameters is presented. In particular, the use of different ambients, SiO_2 anti-reflective coatings, substrate heating, multiple scans and barrier layers to improve film quality was examined. In the end, a better understanding of how to fabricate large grained poly-silicon films with a high degree of uniformity and low surface roughness was developed, which was later applied to fabricate poly-Si TFTs.

2.2 Experimental Procedure for Laser Annealing Amorphous Silicon

Using plasma enhanced chemical vapor deposition (PECVD), 50 nm thick layers of a-Si were deposited, at a temperature of 390 °C and a corresponding deposition rate of 60 nm/min, on 1737 Corning glass substrates. If a barrier layer was needed, SiO_2 was deposited using PECVD, at a temperature of 390 °C and a deposition rate of 120 nm/min, on the glass prior to silicon deposition. After Si deposition, samples were pre-heated to 450 °C for 2 hours in a conventional furnace under nitrogen flow to dehydrogenate the deposited silicon film. Otherwise, during laser annealing, the film would ablate from explosive hydrogen evolution, due to the high hydrogen content of PECVD deposited a-Si (around 10 at.%). Following dehydrogenation, the hydrogen content of the film was reduced below 2 at.%.

The laser processing took place in a custom-made stainless-steel chamber with a quartz window on top. The system was attached to a roughing pump, which could be isolated by means of a slot valve. The base pressure was approximately 1 mTorr, as measured with a convectron gauge. Purified gasses could be bled into the chamber through a separate opening. Samples were inserted through an o-ring sealed faceplate using a vacuum wand. The wafers were placed on a polished ½" thick molybdenum sample holder, which could be heated to 500 °C by means of a coil attached to the backside of the block. The chamber was water cooled to prevent any unwanted heating effects or damage to the quartz window, and was connected to an x-y, motor driven stage with 0.1-micron step resolution and variable speed control. The motion of the stage was controlled by user defined programs written and stored on a PC attached to the x-y control unit.

The amorphous silicon was crystallized by XeCl excimer laser pulses (308 nm), with a 25 ns pulse duration, from a Lambda Physik laser. The laser is capable of repetition rates from 1 to 50 Hz. The average energy of the beam, over 50 pulses, was measured with a Molectron solid-state energy monitor. The power of the laser could be changed by adjusting the voltage of the discharge, from 19 kV to 28 kV. However, for our purposes, this did not allow sufficient range of energy. For this reason, a series of attenuators (beam splitters, neutral density filters and quartz plates of varying degrees) could be placed in the path of the beam to reduce the energy. By knowing the size of the beam spot, the energy density (ED) was calculated.

When performing ELA, to maximize the uniformity, the energy density should be constant over the beam area. To this end, the laser pulses must have a uniform energy profile, often times described as a flattop. Typically, excimer lasers produce pulses with Gaussian profiles, and thus a beam homogenizer was used to even out the energy distribution. The homogenizer splits up the initial beam spatially into different components using an array of quartz lenses and recombines them at the surface to be processed. In this way, the spatial and temporal variations in energy density can be smoothed out over the whole irradiated area. To monitor the condition of the beam, a CCD camera and Beamview software were installed. From Beamview, figure 2-1 shows a typical three-dimensional energy profile of one pulse.

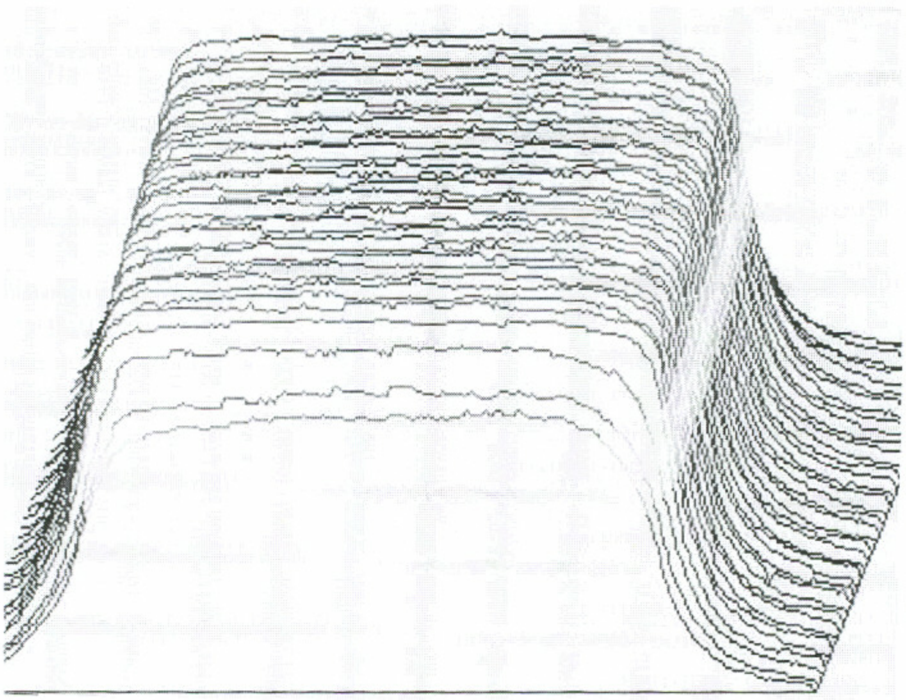


Figure 2-1: Three-dimensional energy profile of laser pulse

As is evident, the energy density was constant, with only minor variations. After passing through the homogenizer, the beam was focused down to a spot size of 5mm x 6mm.

In a typical scenario, samples were placed in the chamber and scanned perpendicularly to the leading beam edge, with a 96% overlap from pulse to pulse, for a variety of different conditions. The repetition rate of the laser was kept constant at 35 Hz. Beam overlapping was used to even out some of the pulse to pulse variations inherent with excimer lasers. The substrate temperature was maintained either at 400 °C or at room temperature (RT). A schematic of the complete system is shown in figure 2-2.

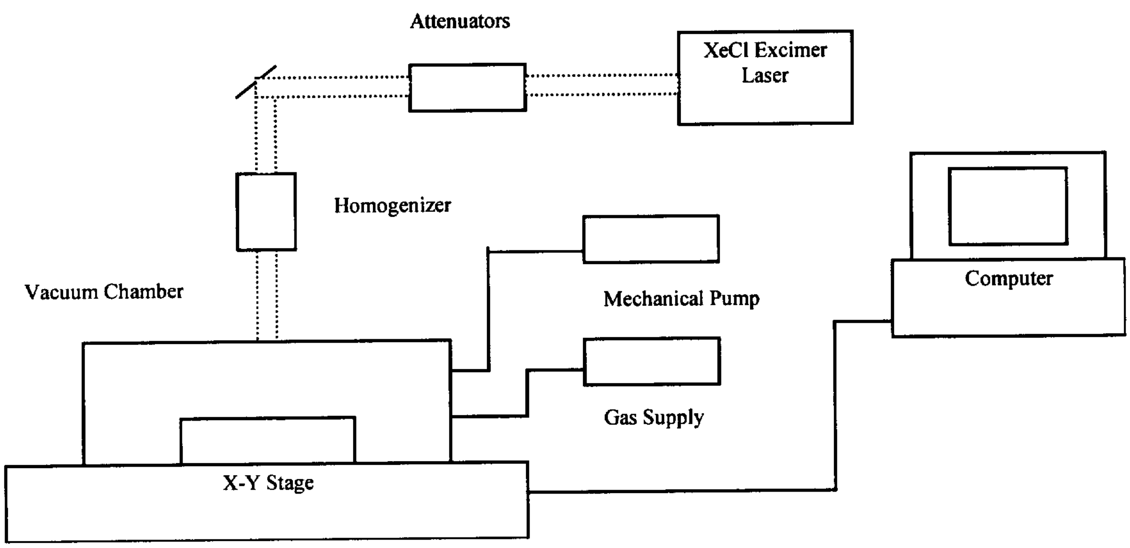


Figure 2-2: Schematic of Laser Annealing Apparatus

After the annealing was completed, transmission electron microscopy (TEM) was used to determine crystalline quality and size and atomic force microscopy (AFM) was used to study the effect of different annealing conditions on surface roughness. Usually, several TEM samples were inspected to study uniformity. The size of the measured area for AFM was 10 μm x 10 μm. For some samples, secondary ion mass spectroscopy (SIMS) was employed to examine if impurities were being incorporated into the silicon during the annealing process, either from the ambient, or from the substrate.

2.3 Results and Discussion

It is well known that large grains can enhance the performance of polysilicon TFTs. The melt duration of the molten film and the number of pulses on a given area are primarily responsible for allowing large grains to form in laser annealed polysilicon films. One method to affect the melt duration is to heat the substrate. Another is to change the cooling rate or thermal conductivity of the surrounding medium. In our investigation, several variables were studied in an attempt to produce high quality poly-Si films. These included different energy densities, use of an SiO_2 barrier layer, substrate heating, multiple passes, annealing ambient, and SiO_2 anti-reflective coatings. Based on the results from this study, TFTs were made and the material characteristics were related to device performance.

2.3.1 Modeling Laser Melting of a-Si

During excimer laser annealing of amorphous silicon, the majority of the photon energy is absorbed within the first 20 nm, as a consequence of the high absorption coefficient of silicon in this part of the spectrum (2×10^6 cm^{-1}). Once the energy is absorbed, it spreads through the film and substrate by thermal conduction. The maximum melt depth is on the order of 0.1 μm[19].

To gain a better understanding of the melting process, a two-dimensional, transient solution to Fourier's heat conduction equation (2-1) was obtained using a commercial partial differential equation solver, employing a finite element method[20]. The structure investigated was composed of two layers, the top-most being silicon, and the bottom-most glass.

$$d_i \times c_i \times \frac{\partial T}{\partial t} = \frac{\partial}{\partial x}\left(\kappa_i \times \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(\kappa_i \times \frac{\partial T}{\partial y}\right) + \Sigma \qquad (2\text{-}1)$$

In this expression, d is the density, c is the heat capacity, T is the absolute temperature, κ is the thermal conductivity, x and y are the position variables (x parallel to the surface and y perpendicular), t is the time variable and Σ is the source term. The subscript ι refers to either glass, SiO_2 or silicon. The laser pulse is incident parallel to the y-direction. We concentrated on conditions away from the edges of the beam, meaning the source term was not a function of x. The source term can be more explicitly expressed as equation (2-2)[21],

$$\Sigma = (1-R)\times\left(\frac{ED\times\alpha}{\tau}\right)\times\exp(-\alpha y)\times u(t-\tau)+\frac{\partial(H\times\theta(T))}{\partial t} \tag{2-2}$$

where R is the reflectivity, ED is the energy density of the laser pulse, α is the laser absorption coefficient, τ is the pulse duration, $u(t-\tau)$ is a step function which turns the pulse instantaneously off at time τ, H is the latent heat of melting and $\Theta(T)$ is a dimensionless unit step function changing from 0 to 1 at the melting temperature. The first term on the right is the power per unit volume supplied by the laser and the second term is the power per unit volume due to phase changes. To improve the accuracy of the simulation, the material properties of the silicon varied depending on whether the silicon was liquid or solid. Some of the values used in the simulation are listed in table 2-1.

Table 2-1: Material Constants

Material	Melting Point (°K)	Reflect.	Specific Heat (cal/g-°K)	Density (g/cm^3)	Therm. Conduct. (cal/cm-s-°K)	Latent Heat (cal/cm^3)	Absorption at 308 nm (cm^{-1})
a-Si(l)	----	0.7	0.3075	2.53	1.0755	693	$1.8x10^{-6}$
a-Si(s)	1480	0.6	0.1673	3.33	0.3585	693	$1.8x10^{-6}$
Glass	1113	----	0.1309	2.76	0.0120	----	$2.0x10^{-3}$
SiO_2	1993	----	0.1309	2.76	0.00956	----	$2.0x10^{-3}$

Throughout these simulations, a substrate temperature of 400 °C was assumed and thermal conduction and/or radiation from the top a-Si surface was neglected.

Figure 2-3 shows a typical simulated temperature versus time profile, for a point located in the middle of the film, with a time scaled normalized to the pulse duration, τ =0.04.

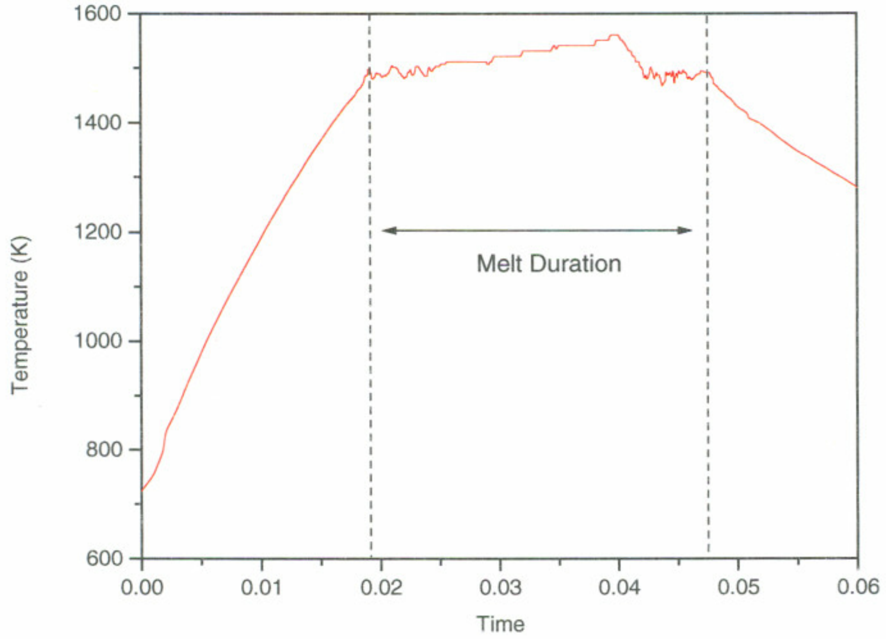


Figure 2-3: Simulated temperature versus time profile for a beam pulse with a duration τ=0.04 incident on a silicon surface. The duration of the melt is also indicated. The initial substrate temperature was 673 °K

At time t=0, the source term was activated. Initially, with the a-Si still solid, the beam energy was absorbed and the temperature increased abruptly. As the temperature approached 1480 °K, the silicon gradually melted. During the phase transformation, the temperature fluctuated somewhat as the solid material was consumed, but increased very little until the change was complete at around t=0.025. At this point, the temperature began to rise again, though more slowly, due to the increased reflectivity and high thermal conductivity of the liquid phase. The increase in temperature continued until the pulse was shut off at t=0.04, whereby it decreased sharply. Again, at around 1480 °K, the liquid began to transform back into solid form. The temperature changed very little until the entire film solidified, and afterwards, a slow decrease in the temperature continued.

The time between melting and recalesence is perhaps the most important parameter in determining the quality of ELA poly-Si. A longer melt duration can lead to a larger average grain size and better uniformity. However, super-heating the liquid silicon during the melting process may have the opposite consequence. Excessive elimination of potential nucleation sites and/or damage to the substrate can have deleterious effects, as explained later in the chapter.

2.3.2 Effect of Laser Energy Density on Poly-Si Characteristics

The most straightforward way to control the grain size in a laser annealed poly-Si film is by changing the energy density of the incident beam. By increasing the energy density, the melt duration of the film is also increased, as confirmed through simulations, and shown in figure 2-4.

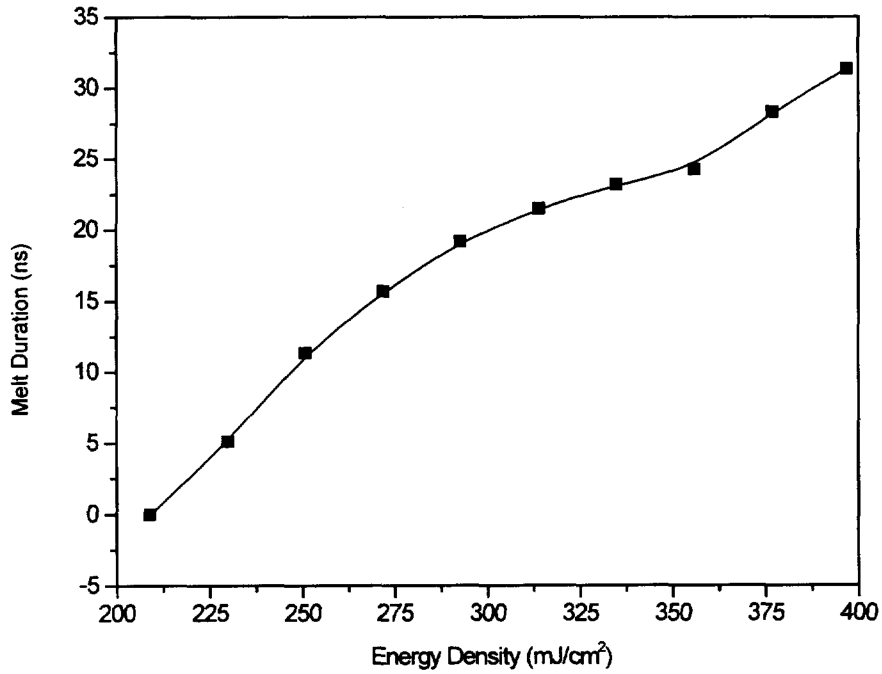


Figure 2-4: Results from simulation showing the effect of laser energy density on melt duration of silicon film (τ=25 ns).

The extent of the simulated melt durations agrees fairly well with experimentally measured values[22]. Somewhat surprisingly though, in the actual laser annealing process, the grain size does not increase steadily as a function of energy density or melt duration. Instead, large grains form through a very narrow range of fluences, as shown in figure 2-5, where the average grain size as a function of energy density is plotted for samples annealed in vacuum at 400 °C.

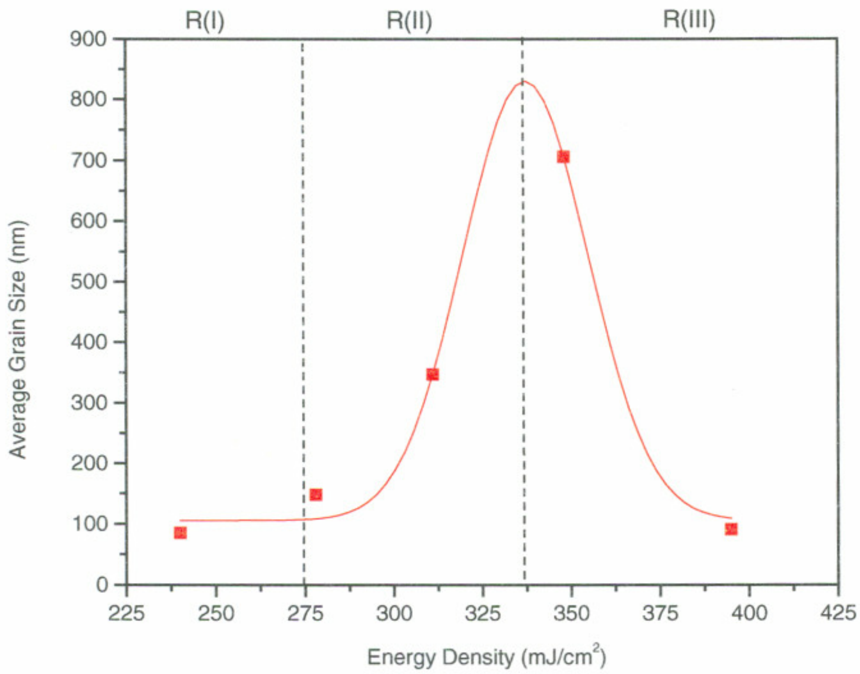
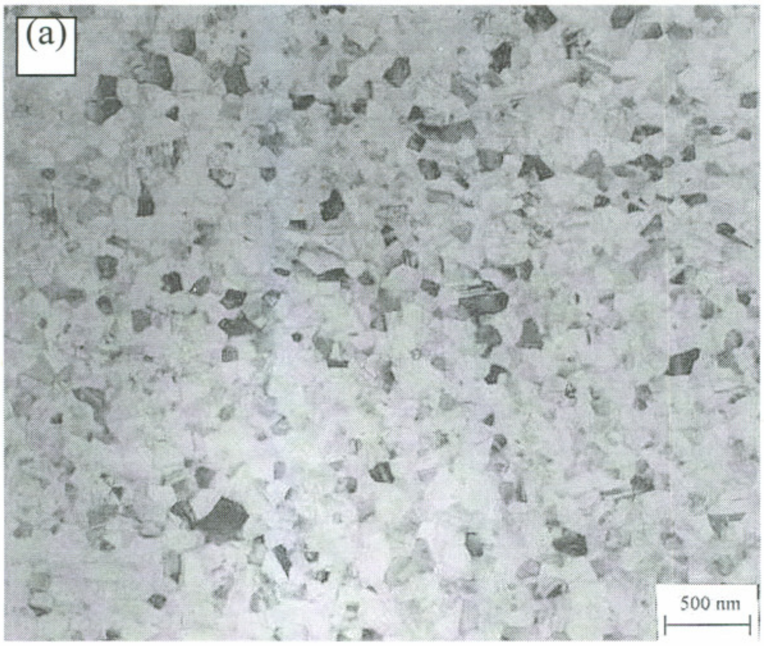
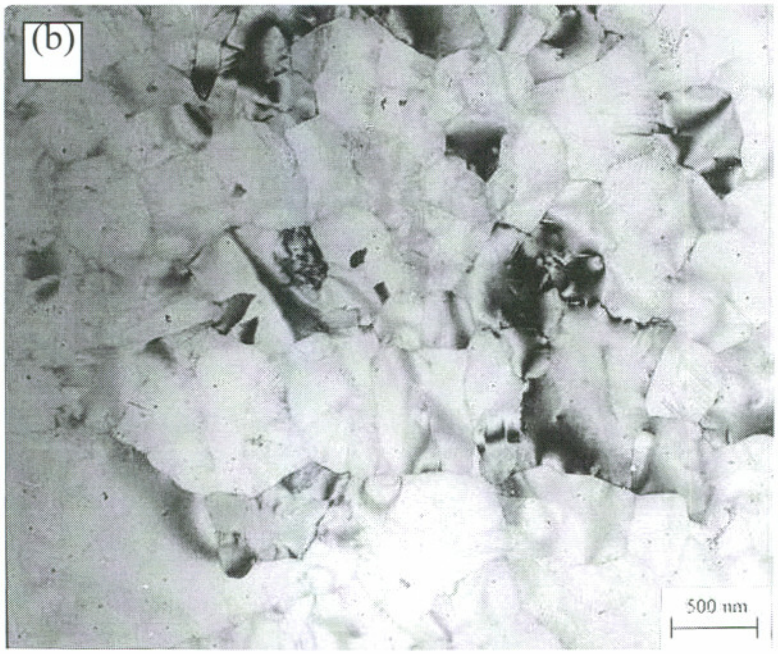


Figure 2-5: Grain size (GS) as a function of energy density for samples annealed at 400 °C in vacuum with 200 nm SiO_2 barrier layer.

The reason for the sharp increase and subsequent drop in grain size is not obvious, and there is still some ongoing debate as to why it occurs. As an initial pointer though, notice that the position of peak in grain size (near 340 mJ/cm^2) corresponds well to the plateau and subsequent steep increase in melt duration as a function of energy density shown in figure 2-4. Indeed, a sudden increase in the melt duration has been observed at the transformation from partial melting and regrowth of the silicon film to complete melting[22]. This is an indication that the decrease in average grain size as a function of energy density for energy densities above 340 mJ/cm^2 occurs concurrently with a complete melting of the Si film.

Laser annealed poly-Si films can be classified as falling into one of three regimes, as indicated in figure 2-5, depending on the energy density used to anneal them[23]. In the first regime R(I), the energy density is low, and only the surface of the film is melted. As the liquid solidifies into poly-Si, the latent heat released in the phase transformation melts the a-Si underneath. But because this newly melted material is severely under-cooled, it crystallizes as fine-grained poly-Si, and more heat is released. This process, termed *explosive crystallization*, continues, and thus a layer of liquid Si (l-Si) propagates through the material until it reaches the Si/substrate interface, leaving fine-grained poly-Si behind[24]. The result is a stratified film, with larger grains on top and smaller grains beneath. As the laser energy density is increased, and the depth of the primary melt begins to reach the back interface, large columnar grains form. The direction of grain growth initiates from the back interface toward the top surface, presumably seeded by small, discontinuous, un-melted crystalline clusters. Other authors suggest that the seeds result from explosive crystallization, which precedes significant melting and the growth of large crystals[22]. In any case, this is the second regime R(II), sometimes referred to as the super lateral growth (SLG) regime[25]. Under these conditions, the *average* grain size reaches its maximum values. As the laser energy density is further increased, the l-Si becomes super-heated and eventually the clusters serving as seed sites are effectively eliminated. Due to the extended melt duration, the few nucleation sites remaining result in the growth of very large (~3 μm) grains. However because the grains are too far apart to have their boundaries form a continuous layer, the regions between the grains cool, becoming severely under-cooled. As a result, homogeneous nucleation occurs, resulting in the formation of fine-grained material. This is the third regime R(III), and is characterized by a bimodal grain size distribution and thus a highly non-uniform film. Figure 2-6 (a)-(c) shows three characteristic TEM samples annealed at different energy densities, and clearly demonstrates the differences between the three regimes described above.


(a)
500 nm


(b)
500 nm

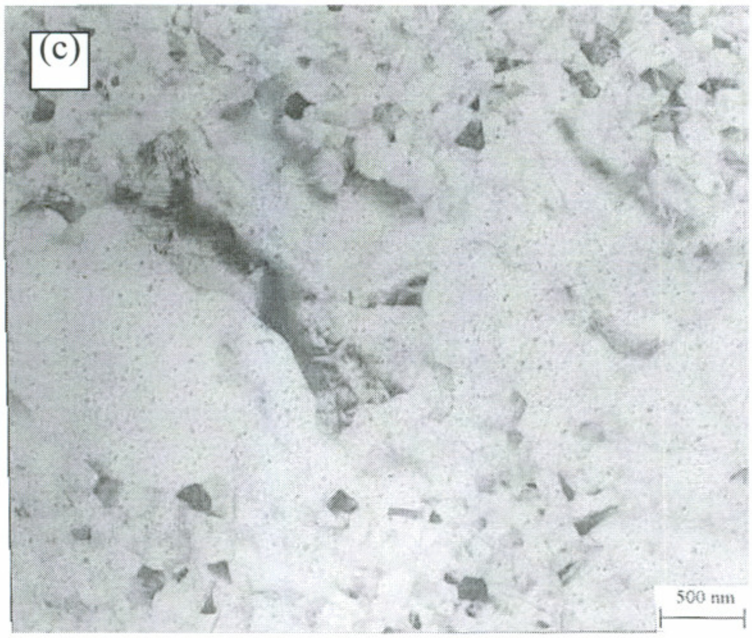


Figure 2-6: Planar TEM images of polysilicon from (a) R(I), (b) R(II), and (c) R(III). All samples annealed in vacuum at 400 °C. The energy densities in each case were (a) 235 mJ/cm^2, (b) 305 mJ/cm^2, and (c) 350 mJ/cm^2.

2.3.3 Use of an SiO_2 Barrier Layer

When high temperature processes are needed to crystallize amorphous silicon films, quartz substrates must be used because typical strain temperatures for glass are around 600 °C[8]. However, quartz substrates are expensive. In terms of applications toward large screen FPDs, the high cost of quartz makes it impractical to use. In addition, not only is it desirable to utilize cheaper glass substrates, but recent trends indicate a migration to flexible substrates for future display applications based on polysilicon technology[26]. In these cases, the thermal constraints imposed by the substrate are even more severe. As a result of the high temperatures reached in the film, the Si/substrate interface can experience temperatures up to 1700 °C for very short durations. At these temperatures, glass may deform and even melt, thus influencing the nucleation and recrystallization process in the top silicon layer. To alleviate these problems, an SiO_2

barrier layer can be added. In this manner, the temperature at the surface of the substrate can be moderated. A question exists, however, as to the effects of the barrier layer on the structural characteristics of the annealed silicon film. To address this question, the characteristics of excimer laser annealed polysilicon films with barrier layers ranging from 100 nm to 400 nm were studied in detail, over a wide range of energy densities, and compared to samples made without a barrier.

Figure 2-7 shows how the GS was affected by barrier layers of different thicknesses, over a range of energy densities.

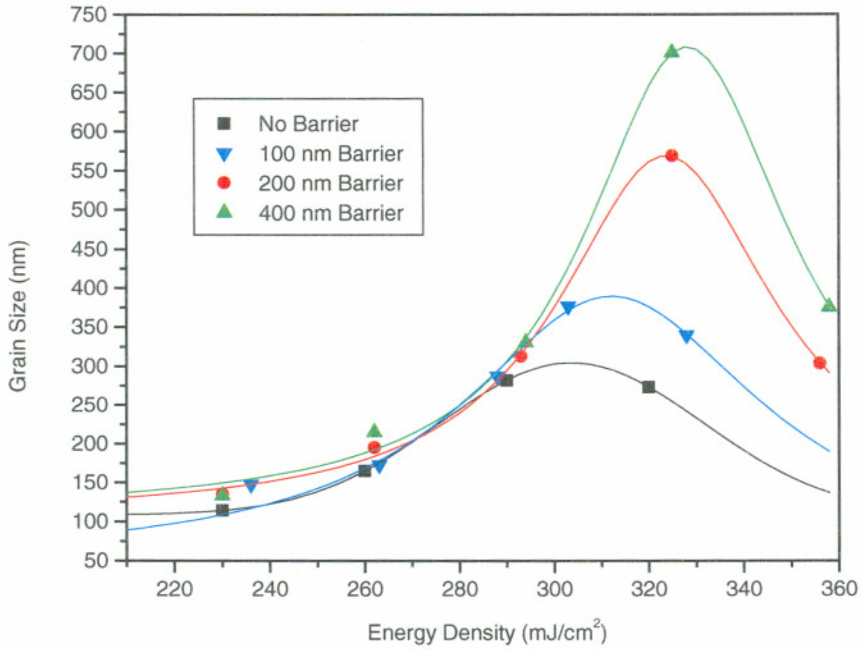


Figure 2-7: Grain Size as a function of energy density for samples with different SiO_2 barrier thicknesses. All samples annealed at 400 °C in vacuum.

The two most noticeable features from the plot are an increase in grain size and an increase in the energy density at which the maximum grain size is achieved for thicker barriers. Both of these results can be explained by using a simple heat transfer argument and relating this to the crystal growth mechanism as described by Im et al[27]. It has been reported that the thermal conductivity for deposited SiO_2 is lower than glass over the entire temperature range of interest[28]. As a result, the addition of a barrier layer leads to slower cooling and hence a longer melt duration for energy densities which can cause liquefaction of the top silicon layer. Figure 2-8 illustrates the result of a rapid cool as opposed to a slower one.

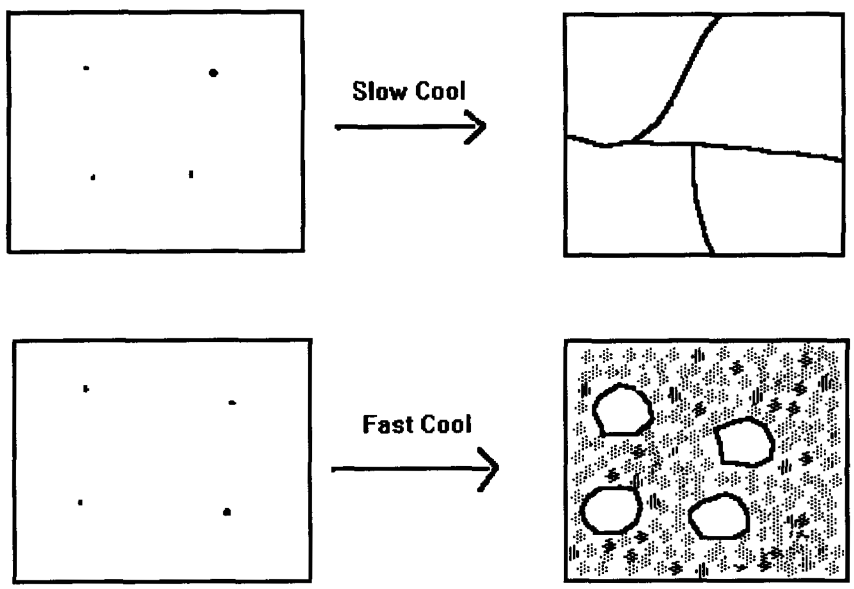


Figure 2-8: Depiction demonstrating effect of cooling rate on grain morphology

On the left are nucleation sites at the silicon-SiO_2/glass interface which have survived the partial melting of the silicon film. With a slow cool, the grains grow until their boundaries impinge resulting in a *monomodal* grain size distribution and a large average grain size, indicative of an R(II) film. For a fast cool, the grains grow until the unsolidified material becomes supercooled, whereby homogenous nucleation can occur. This results in a *bimodal* grain size distribution, where a few large grains are surrounded by an abundance of much smaller grains, and thus a smaller average grain size, as in an

R(III) film. Experimentally, as higher energy densities were used, fewer nucleation sites remained and so longer grain growth periods were needed to maintain R(II) grain growth. This was accomplished by using progressively thicker barriers.

Computer simulations were performed to verify the relationship between the melt duration and barrier thickness. From these simulations, the melt duration as a function of barrier thickness was determined and is plotted in figure 2-9.

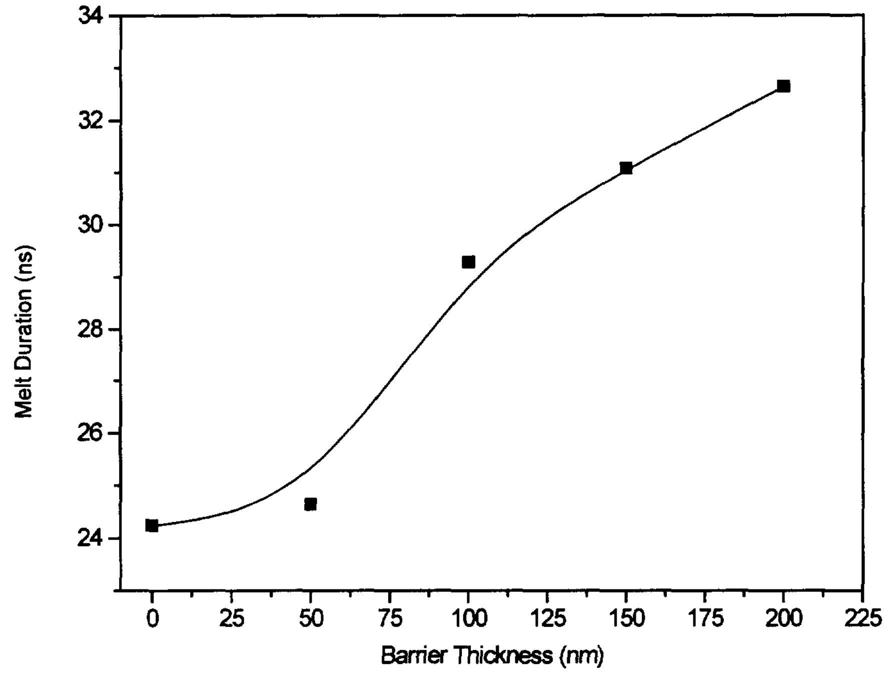


Figure 2-9: Simulated melt duration as a function of SiO_2 barrier thickness (τ=25 ns, ED=335 mJ/cm^2).

In this case we used a three-layer structure composed of Si/SiO_2/glass. This figure makes it apparent that, as suggested above, thicker barriers allow longer melt durations, which in turn allow larger grains to form.

Another benefit of using a barrier layer is the reduction in impurities segregating into the silicon from the glass. From SIMS analysis, the concentrations of aluminum

(Al), sodium (Na) and potassium (K) at the poly-Si/SiO_2 interface as a function of barrier layer thickness were determined. These results are shown in figure 2-10.

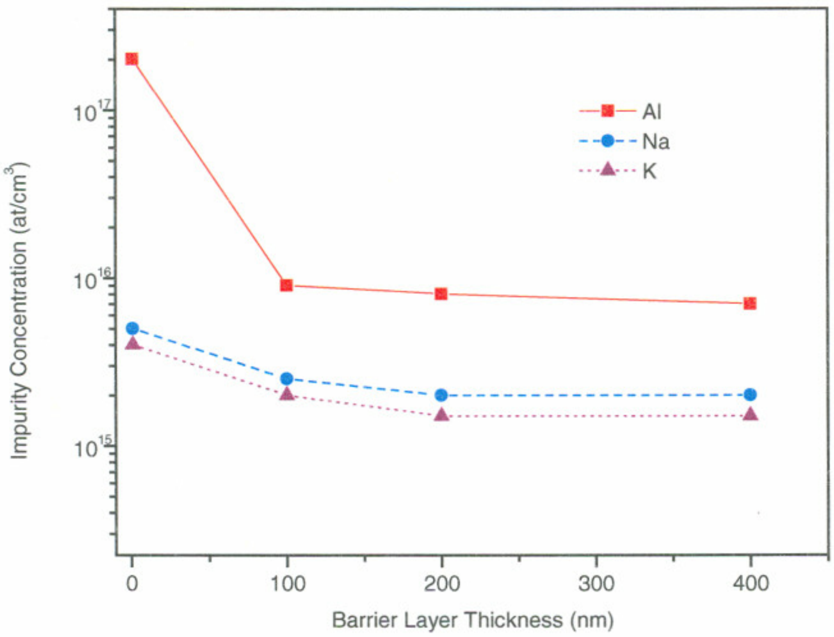


Figure 2-10: Impurity concentration of aluminum (Al), sodium (Na) and potassium (K) at the poly-Si/SiO_2 back interface as a function of the SiO_2 barrier layer thickness.

The particular glass used was Corning 1737, which is an alumina-silicate, with low alkaline concentration. It can be seen that the amount of aluminum at the interface declined markedly from no barrier to 100 nm and changed very little for thicker barriers. Sodium and potassium concentrations at the interface declined until the barrier was 200 nm thick, and changed very little as the barrier thickness was increased to 400 nm. It was concluded from these results that a 200 nm thick film would be sufficient to maximize the impurity blocking effect of the barrier layer.

2.3.4 Effect of Annealing Ambient on Poly-Si Characteristics

The choice of annealing ambient can significantly affect the grain growth characteristics of laser annealed polysilicon films. The presence of gas in the annealing chamber cools the sample surface directly, which can change both the melt duration and the energy density threshold where melting occurs. As with the barrier layer study, and for the same reasons, a faster cooling rate limits the maximum achievable grain size. In this investigation, nitrogen, helium, air, argon and rough vacuum were studied. The effect on grain size is shown in figure 2-11, where for this experiment, a 200 nm barrier was employed.

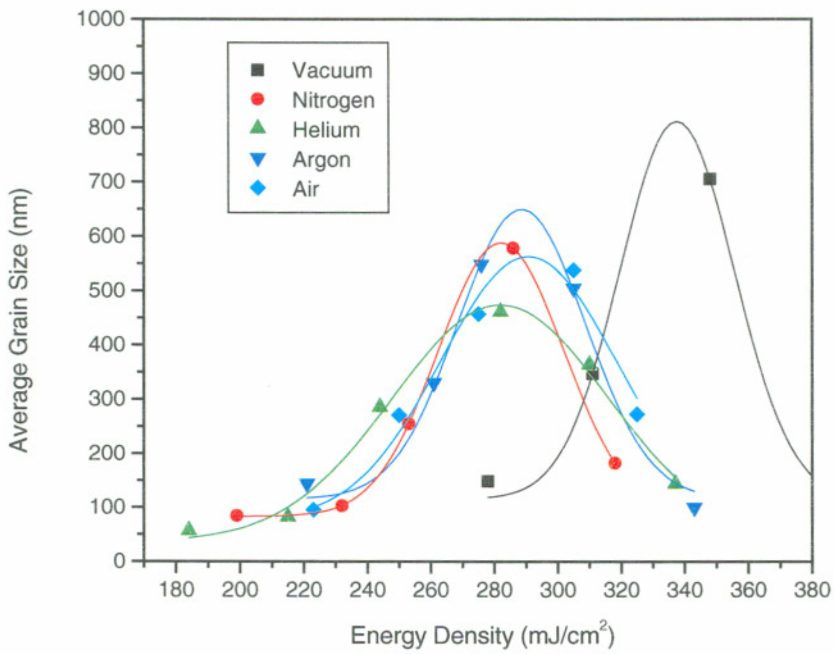


Figure 2-11: Effect of energy density on grain size for samples annealed in different ambients. All samples annealed at 400 °C with a 200 nm SiO_2 barrier layer.

Figure 2-12 shows the relationship between the maximum grain size from figure 2-11 and the thermal conductivity (κ) of the ambients, assuming $\kappa \approx 0$ for vacuum.

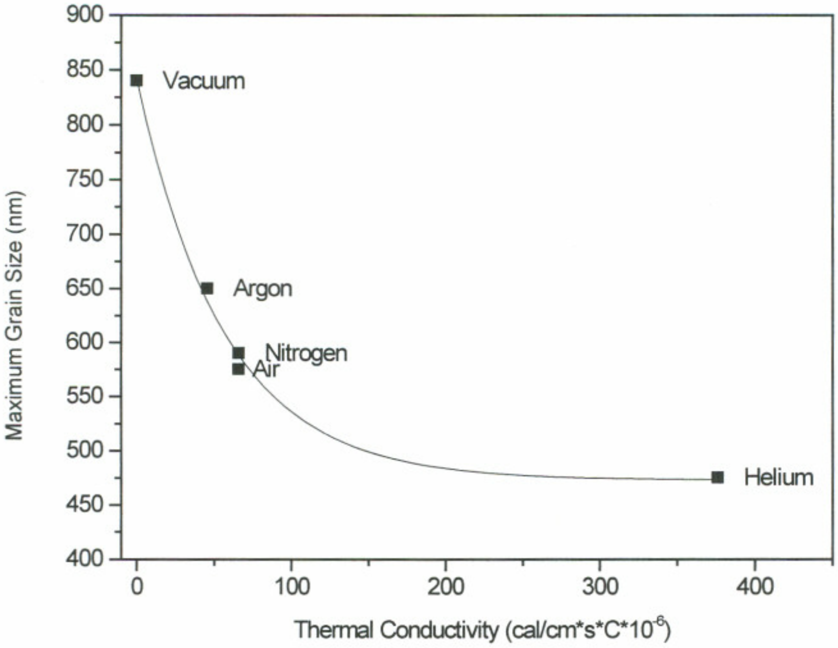


Figure 2-12: Relationship between the thermal conductivity and the maximum poly-Si grain size (from figure 2-11) of samples annealed in different ambients.

This figure emphasizes the importance of heat transfer in limiting grain size: slower cooling increases the maximum achievable grain size.

It can also be seen from figure 2-11 that large grain growth initiated at a lower energy density for samples made in either nitrogen, air, helium or argon as opposed to vacuum. This may have been due to a delay in the onset of liquefaction during the pulse duration, from the cooling effect of the gas. The delay could have prevented the increased reflectivity of the liquid phase to an extent that more energy of each pulse was absorbed, the effect being a shift of the curves depicting grain size versus energy density toward lower energy densities.

Another source of concern when an ambient other than vacuum was used is uniformity. Especially with helium, it became difficult to create films composed entirely of large grains. Due to the increased cooling, small grains formed, as in R(III) films, could be found under almost any condition, creating regions with vastly different structural characteristics. Figure 2-13 depicts such a situation.

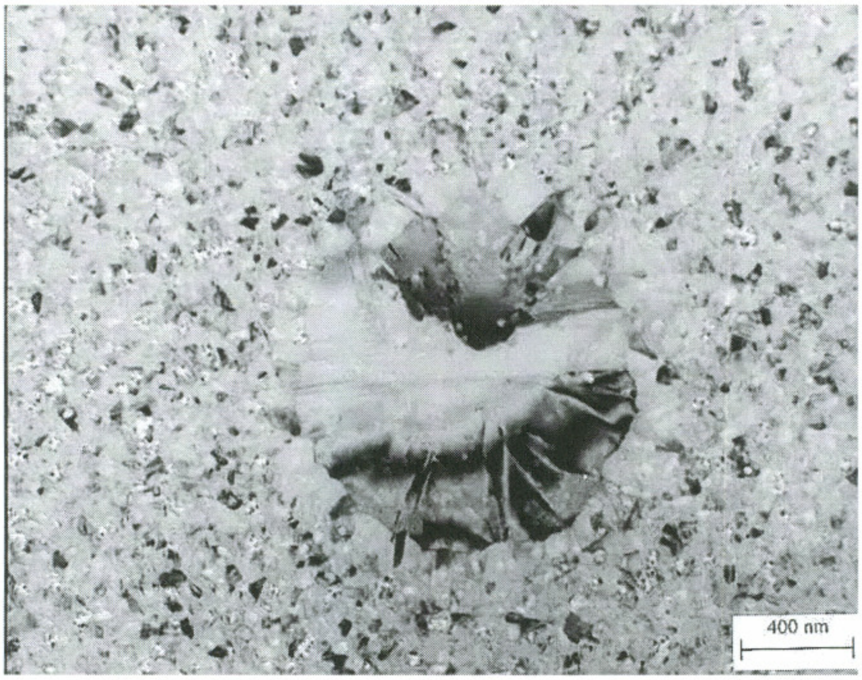


Figure 2-13: Planar TEM image of polysilicon annealed in Helium at 400 °C showing bi-modal grain size distribution (ED=335 mJ/cm^2).

The problem was less severe with nitrogen, air and argon and could be avoided entirely with a careful selection of energy density.

Depending on the particular ambient used, different amounts of gasses were incorporated into the poly-Si during annealing. In particular, other authors have suggested that oxygen incorporation is detrimental to surface roughness[18]. For this reason, SIMS analysis was performed on several samples laser annealed in different ambients, with a-Si layers 100 nm thick. The results are shown in figure 2-14.

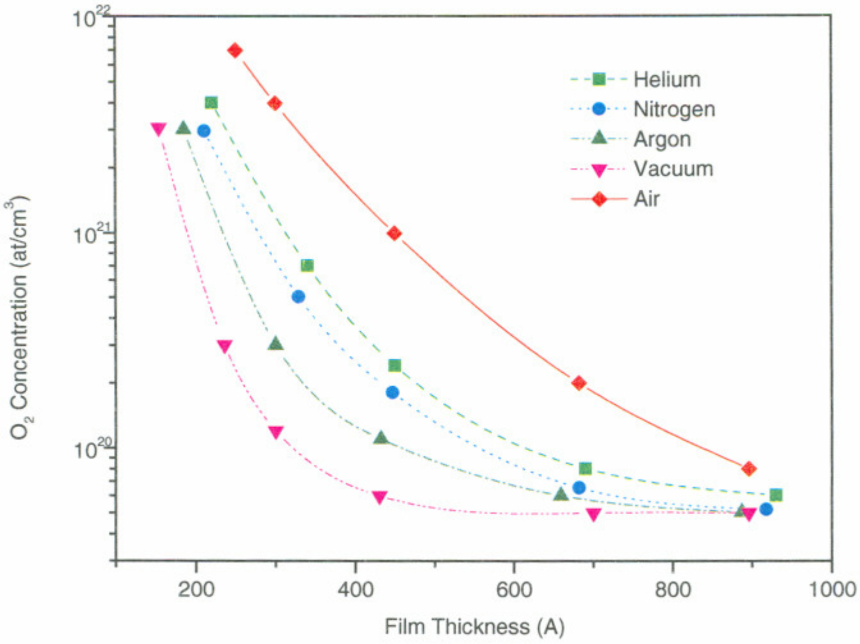


Figure 2-14: SIMS results showing oxygen concentration as a function of depth into the poly-Si film from the top surface, for samples annealed in different ambients.

As one would expect, annealing in rough vacuum produced the lowest levels of oxygen, air produced the highest, and the other ambients fell somewhere in-between. AFM analysis was also done on several samples, and correlated with the atomic percentage of oxygen, at a depth of 50 nm, and shown in figure 2-15.

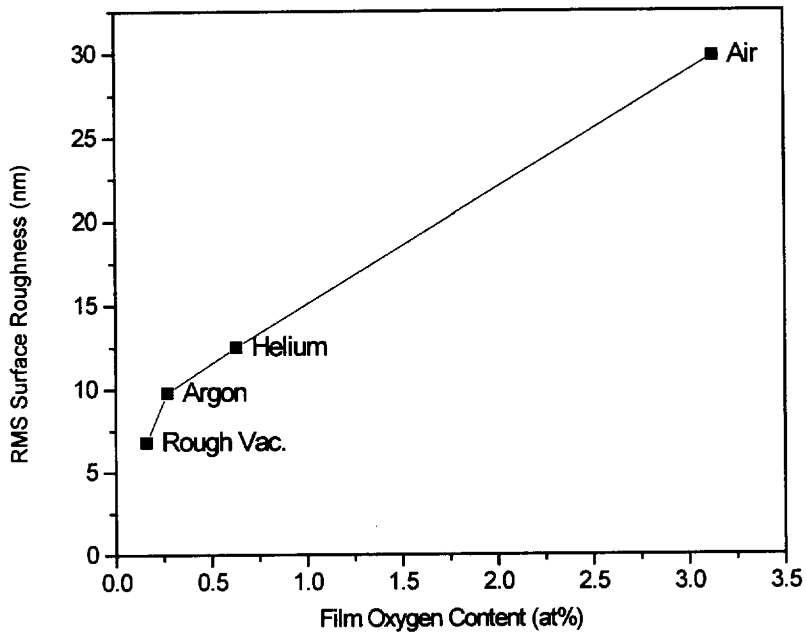
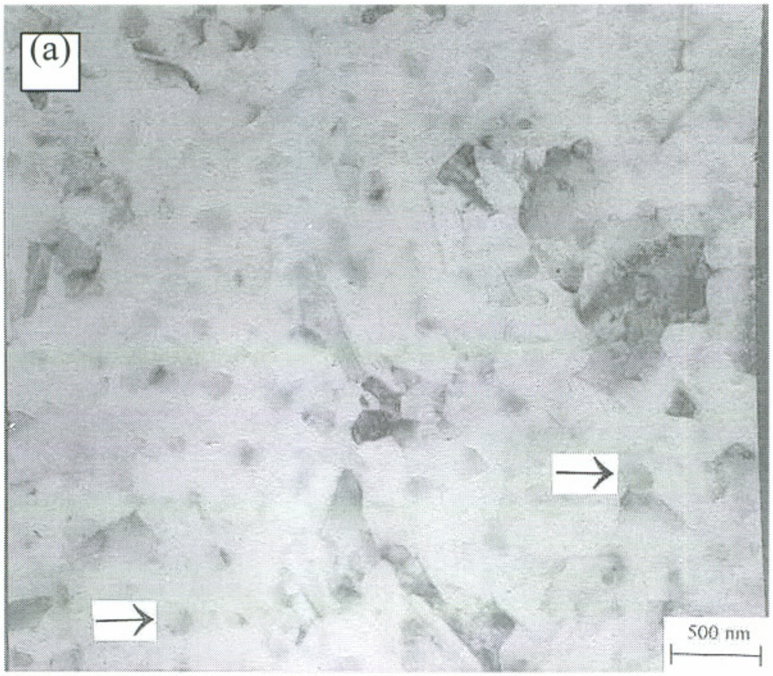
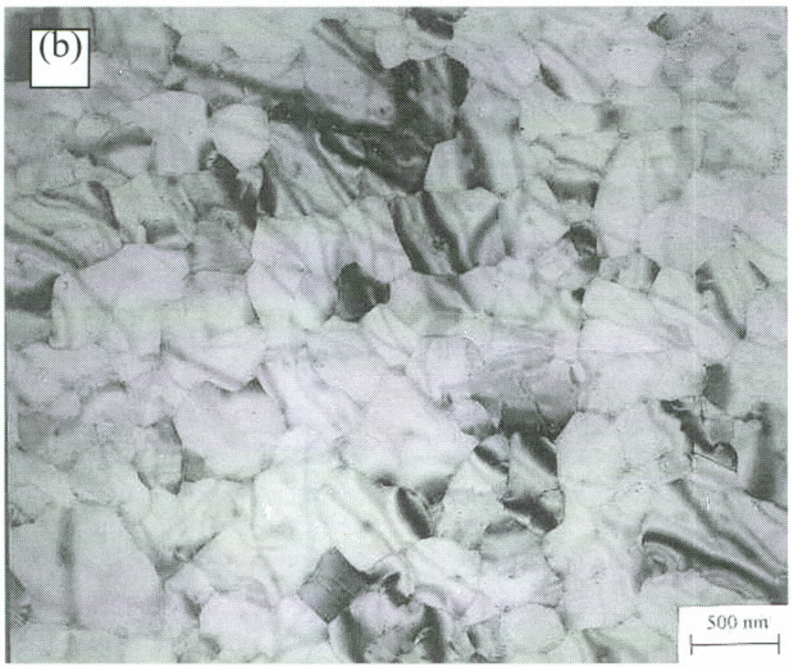


Figure 2-15: Relationship between poly-Si surface roughness and atomic oxygen concentration in the film at a depth of 50nm.

This figure makes it clear that oxygen does indeed enhance surface roughness

In addition to having rougher surfaces, samples annealed in air have a unique grain morphology. Figure 2-16 (a)-(c) shows TEM images of samples annealed in different environments.


(a)
500 nm


(b)
500 nm

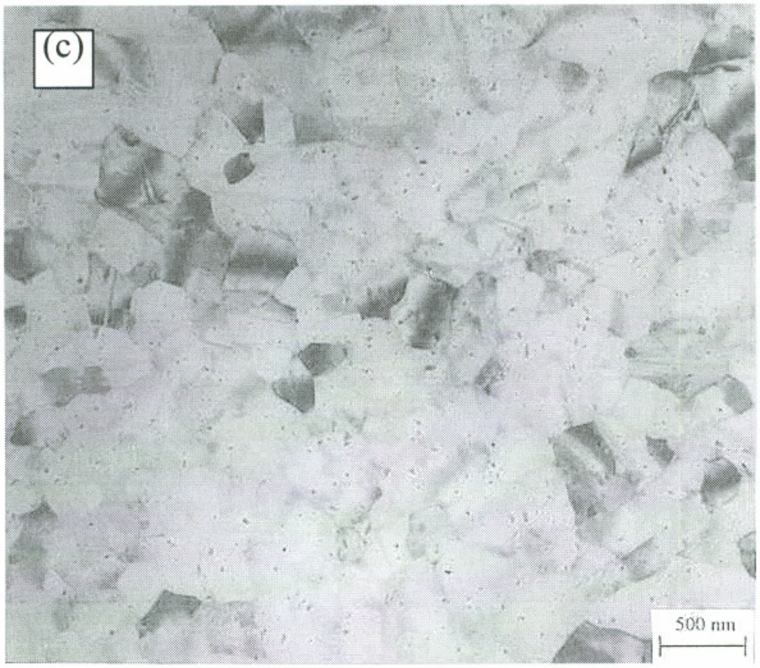


Figure 2-16: Planar TEM images of samples laser annealed with ED=270 mJ/cm^2 at 400 °C in (a) air, (b) argon and (c) nitrogen. The sample annealed in air has grain boundaries that are more difficult to recognize and unique, possibly amorphous structures, as indicated by the arrows.

Close inspection reveals several characteristics, which distinguish the air sample in part (a) from the argon and nitrogen samples in (b) and (c). For one, there is a general haziness to the image: the grain boundaries are less easily identifiable and intra-grain features are harder to make out. Also, there are structures, as indicated with arrows in (a), that are not present in (b) or (c). Because they do not show up under dark-field TEM and do not form a characteristic poly-Si diffraction pattern, it was determined they are amorphous, and may in fact be micro-clusters of SiO_2. One could speculate, that these structures are also be the source of the enhanced roughness resulting from oxygen incorporation.

2.3.5 SiO_2 Anti-Reflective (AR) Coatings

There are two primary advantages of using AR coatings when performing ELA of a-Si. Firstly, the coating allows use of a lower ED to crystallize the film. This is beneficial, in that less damage is incurred by the laser optics. Second, and more importantly, AR coatings can prevent impurity incorporation, especially oxygen, from the top a-Si/SiO_2 interface during annealing. As mentioned above, oxygen in particular has deleterious effects on the sample surface. For these reasons, AR coatings uniformly deposited over a-Si were studied. The SiO_2 was 52 nm thick, and a series of samples were laser annealed at different energy densities to study the grain size and grain morphology. Figure 2-17 shows how the GS varied as a function of ED.

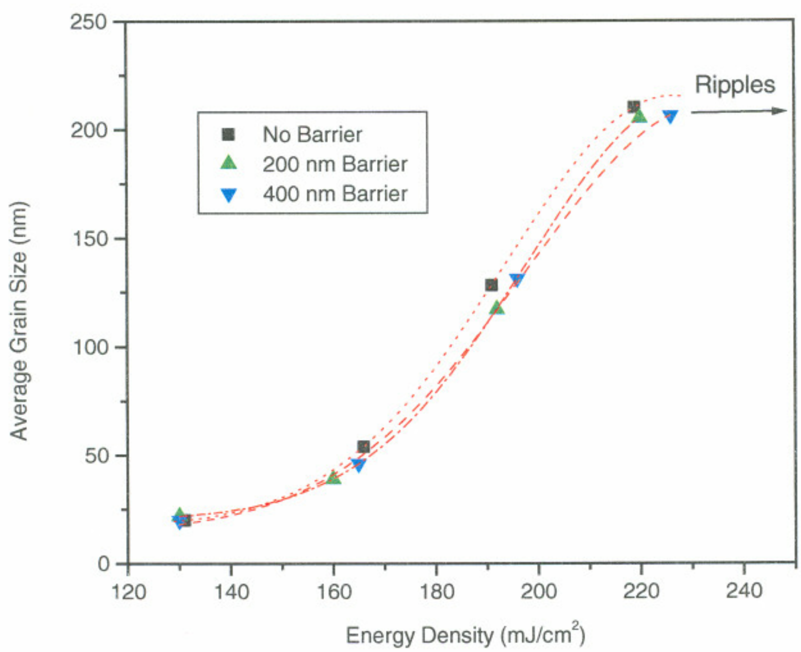


Figure 2-17: Grain Size as a function of energy density for samples annealed with an SiO_2 AR coating, and different barrier thicknesses. All samples annealed in vacuum at 400 °C. Above 220 mJ/cm^2, the film was severely distorted.

As expected, the crystallization of the film initiated at a lower ED when the AR film was in place. Referring back to figure 2-5, without an AR coating, the curve peaked at around 340 mJ/cm^2, while with the coating, it occurred at 220 mJ/cm^2. With an increase in ED, the average GS grew, but as the samples were reaching the SLG regime, a ripple pattern in the poly-Si began to form, shown in figure 2-18 and indicated in figure 2-17.

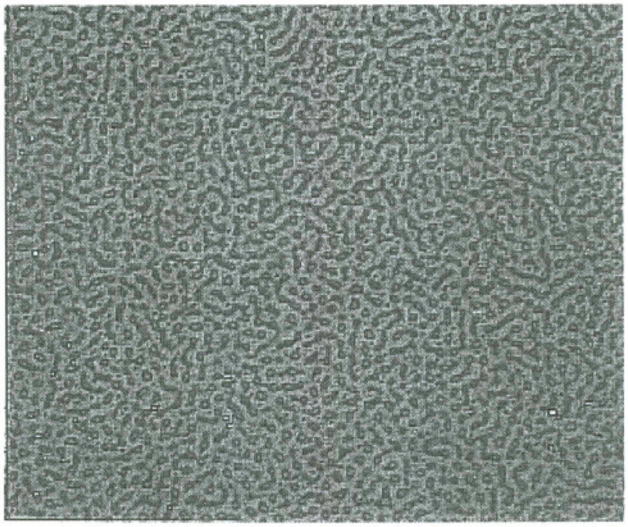


Figure 2-18: Photograph taken through a microscope of deformed oxide layer.

The ripples were large enough to be seen with an optical microscope and were observed, most noticeably, under conditions when the entire thickness of the Si irradiated region was melted. It is likely that after the film melted, because the AR coating was free floating on l-Si, as it cooled, lateral strain caused buckling to occur[29], and the buckling created a ripple pattern in the poly-Si layer. Therefore, use of uniform AR coatings precludes use of energy densities that maximize the GS of the film. However, other authors have demonstrated that patterned AR coatings can be more effectively employed[30]. In smaller structures, the AR film can spread outwards and avoid buckling, thus maintaining a smooth surface.

2.3.6 Effect of Multiple Laser Passes on Poly-Si Characteristics

To study the effect of multiple passes on poly-Si characteristics, a section of the wafer was scanned repeatedly using the same energy density. Regions were scanned from one to 16 times and the grain size was measured for each case. The results are shown in figure 2-19.

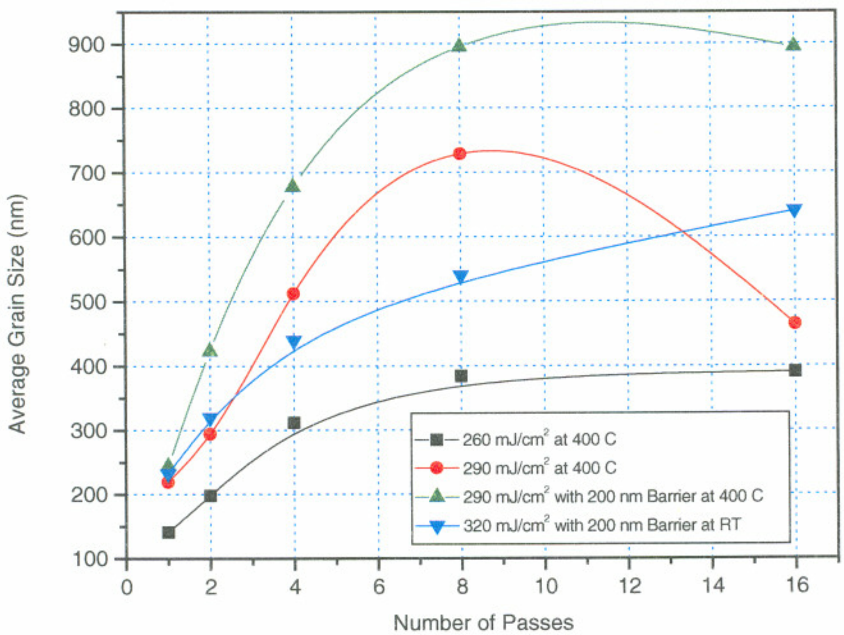
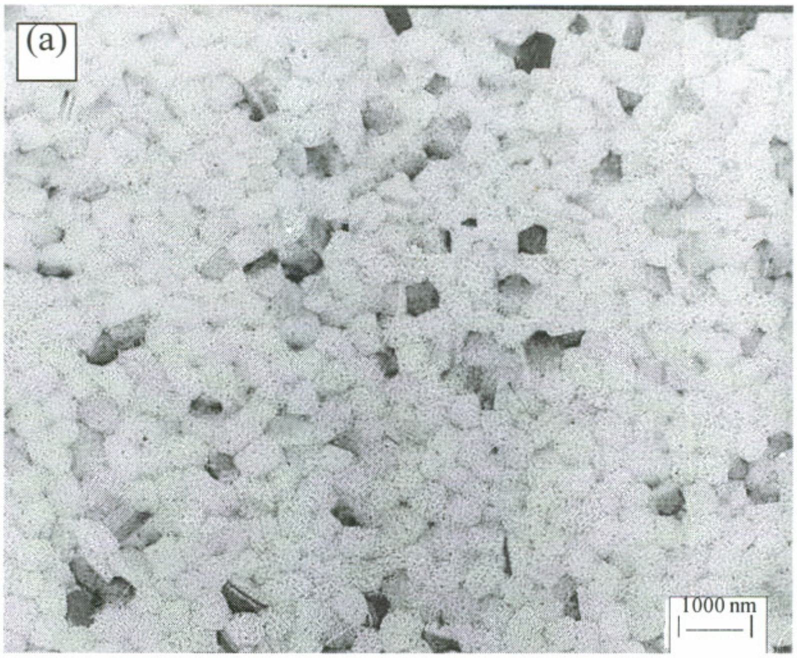


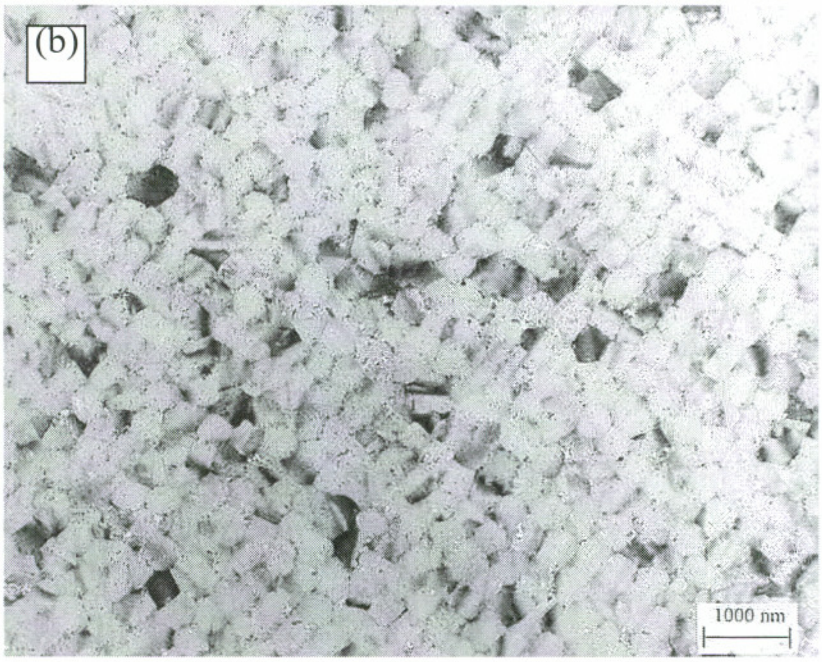
Figure 2-19: Average grain size as a function of the number of scans on a given area for samples annealed at 400 °C or RT with or without an SiO_2 barrier layer, and at different energy densities. All samples processed in vacuum.

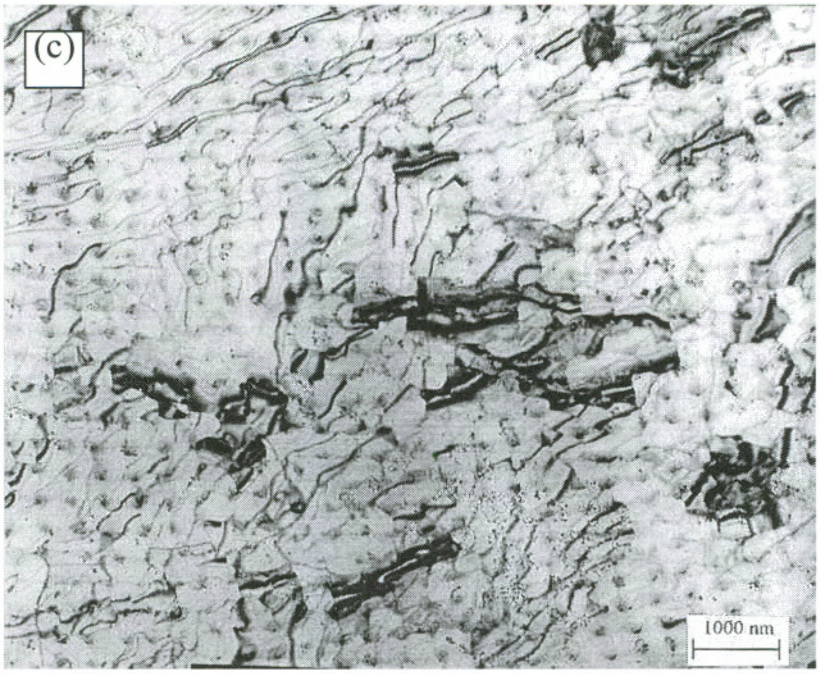
From the plot, most noticeably, multiple passes lead to an increase in the average grain size. Other authors have reported similar results in regards to the effect of the number of pulses for a given area on grain size[19,28]. When using a lower energy density (260 mJ/cm^2) with no barrier and substrate heating, the average grain size first increased then saturated. When a higher energy density (290 mJ/cm^2) was used, the average grain size increased initially and then decreased with more passes. This decrease in average grain size was likely due to the kind of substrate surface roughening described by Boyce et al[31]. That is, damage to the glass interface generated nucleation sites, which reduced the average grain size. This is not to say that this mechanism of grain size reduction was the source of small grains in single passes at high energy densities, as in R(III) films. On the contrary, two step experiments where small grains were created by an initial scan at a high energy density (around 400 mJ/cm^2) then a second scan was made at a lower energy density (around 310 mJ/cm^2) and large grains were recovered suggests otherwise. But interface roughening can create enough nucleation sites to limit large grains which would form if a smooth interface were maintained. From TEM images, it appeared that some of the largest crystals which formed after the 8th pass were broken up after 16 passes. When the same conditions were applied to a sample with a 200 nm barrier, a decrease in grain size did not occur from 8 to 16 passes. The higher melting point of SiO_2 makes it more resistant to thermal damage, and hence, it provided a thermal buffer between the silicon and glass, leading to a lesser likelihood of damage induced nucleation sites.

Figure 2-19 also shows the results of using a multiple scan process on a sample annealed at RT. For comparison purposes, a higher energy density was used so that the grain size after the first scan would be approximately the same as the sample crystallized at 400 °C using 290 mJ/cm^2. In this case, the grain size continually increased as more passes were completed. The lack of substrate heating caused the average grain size to grow at a slower rate, but after the 16th pass, the transformation to a film composed entirely of large grains was nearly finalized. With this technique, and the use of a barrier layer, the average grain size was increased to upwards of 650 nm without substrate heating, while maintaining uniformity.

From inspection of TEM images, it can also be seen that multiple passes can enhance two dimensional granular ordering in laser annealed polysilicon films, as shown in figure 2-20 (a)-(c).


(a)
1000 nm


(b)
1000 nm



2-20: Planar TEM images of polysilicon annealed at 305 mJ/cm^2 showing granular ordering after (a) 1 scan, (b) 2 scans and (c) 8 scans (substrate temperature =400 °C).

Figure 2-20 (a) shows that after 1 scan, grains were randomly located. But as seen in 2-20 (b), after 2 scans, the grains in a significant portion of the film became organized into well-defined perpendicular rows and columns. Under these conditions, uniformity was excellent, and coupled with the ordering effect, the film took on a honeycomb appearance. With more passes, the grains grew, but not necessarily uniformly. Rather, a few grains became quite larger than the rest. After 8 and 16 passes, shown in 2-21 (c) for 8 passes, the grains had all grown large, some on the order of several microns, and they appeared entirely different from grains formed initially, being less regularly shaped. Remnants from the ordered structure were still quite noticeable, though the relationship between ordering and the grain size was less obvious.

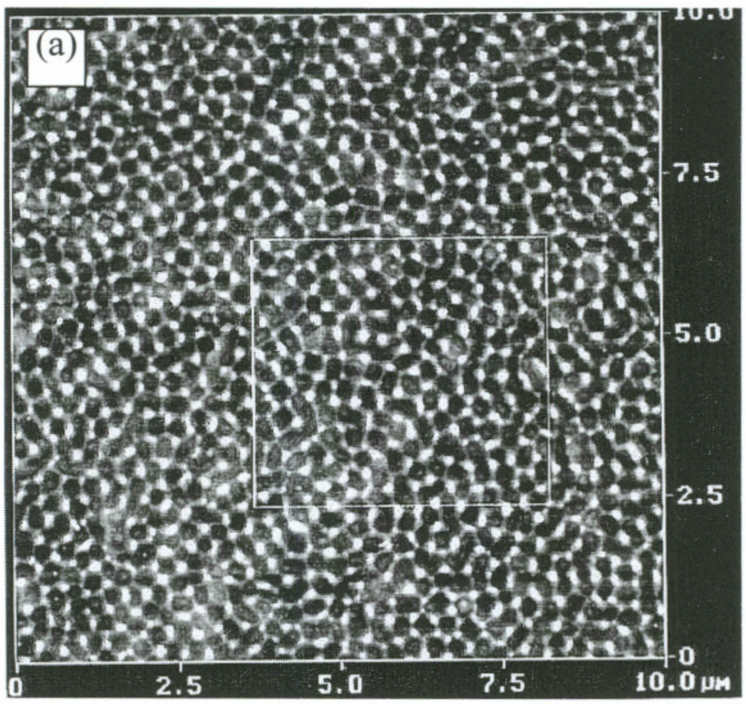
It may be that this ordering phenomenon is related to the so-called laser induced periodic surface structure or LIPSS[32]. Other authors have produced LIPSS using a similar process, and this conjecture has support in that the wavelength of the ordering is approximately equal to the wavelength of the incident radiation (308 nm), as one would expect for LIPSS[19]. It should be noted that this effect only occurred over a narrow range of energy densities. It also occurred under certain conditions in both argon and nitrogen and strongly in samples annealed at RT.

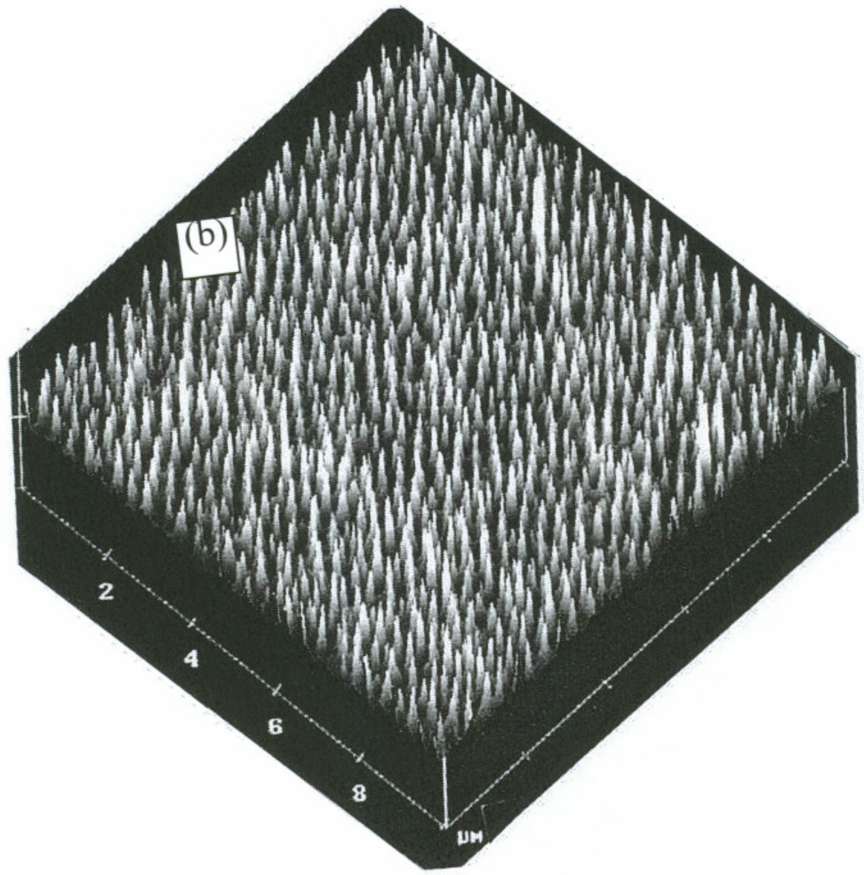
To see the effect of multiple passes on grain boundary surface roughness, AFM measurements were performed. The results are shown in table 2-2.

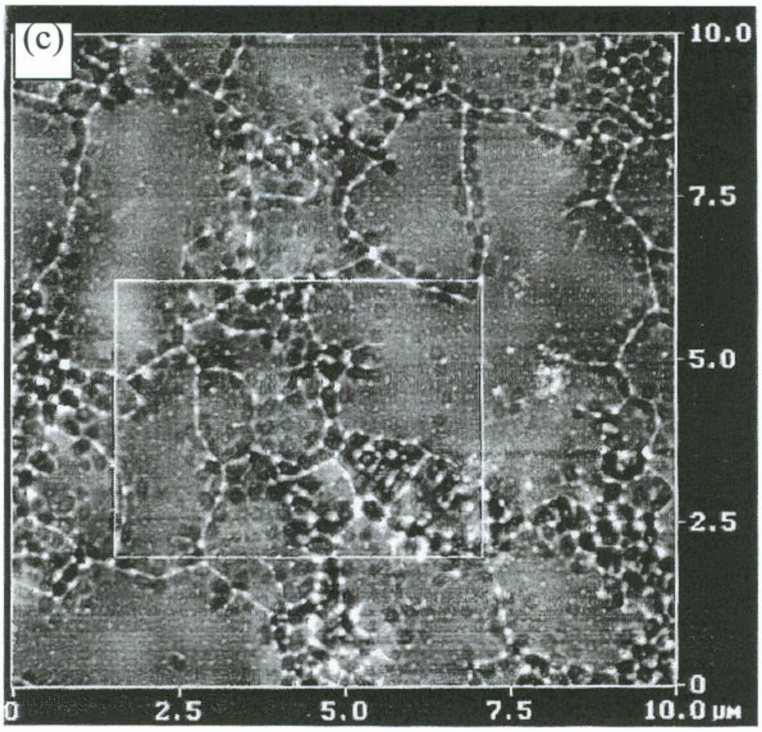
Table 2-2: RMS surface roughness for samples scanned multiple times at 305 mJ/cm^2 (all films annealed at 400 °C in vacuum)

	Number of Scans		
	1	2	8
RMS Surface Roughness (nm)	12.8	12.3	5.7

Notice that the surface roughness dropped dramatically from the second pass to the eighth. In many cases, surface roughness increases as the average grain size increases, but, as our results indicate, this is not always so. What is more important in relating surface roughness, as measured with AFM, to film characteristics, as seen with TEM, is the particular grain structure itself. Four AFM images are shown in figure 2-21 (a)-(d).




(b)
2
4
6
8
UM


(c)
10.0
7.5
5.0
2.5
0
0
2.5
5.0
7.5
10.0 μm

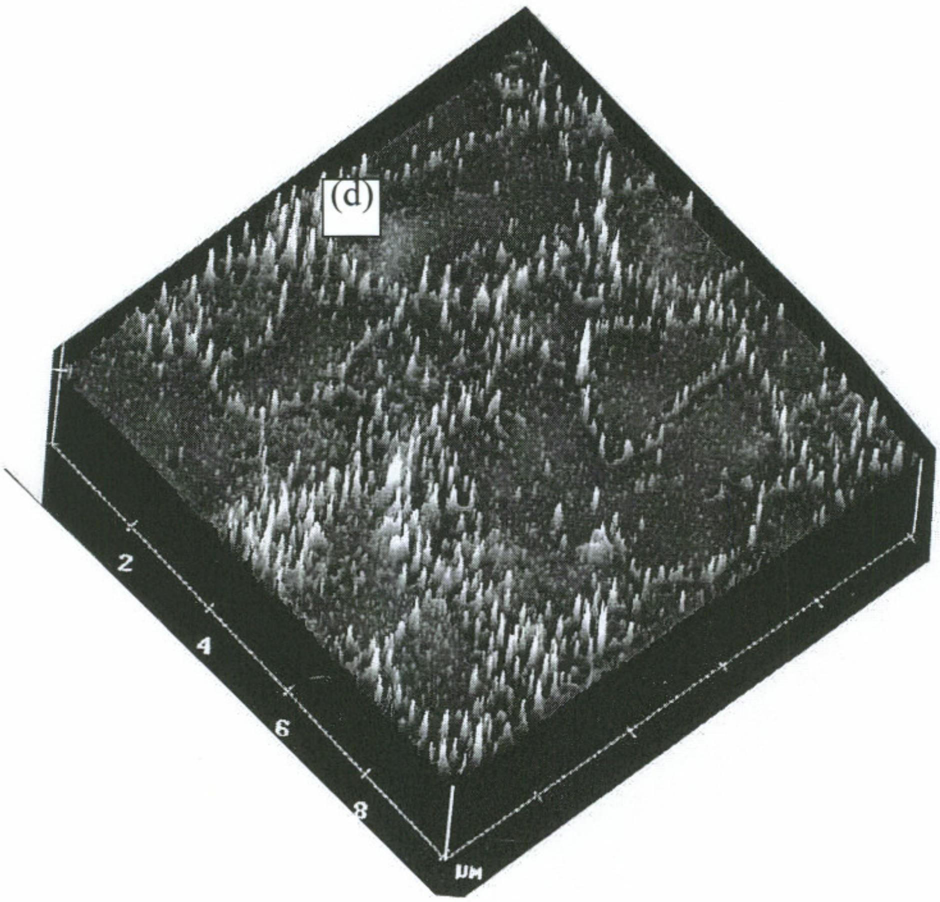


Figure 2-21: AFM images of polysilicon scanned at 305 mJ/cm^2 (a) planar view of sample scanned twice, (b) 3D view of sample scanned twice, (c) planar view of sample scanned eight times, (d) 3D view of sample scanned eight times (substrate temperature=400 °C).

2-21 (a) and 2-21 (b) are a planar and three dimensional view taken from a sample, with a 200 nm barrier, scanned twice (2x) at 305 mJ/cm^2 with a substrate temperature of 400 °C. 2-21 (c) and 2-21 (d) are likewise taken from a sample scanned 8 times (8x). Though the grain size was smaller in the 2x sample, the roughness was greater. The major cause of this increased roughness was not the grain boundaries, but rather the *intersection* of grain boundaries. The regularity of the structure in the 2x sample created an abundance of points where many grain boundaries converged. It was also at these vertices where the largest surface features were located, as seen in 2-21 (b). In the 8x sample, the grains were more irregular and there were fewer points where multiple grain boundaries intersected. An explanation of the relationship between grain boundaries and surface roughness was given by Fork et al[33]. In the 2x sample, at the points, where several melt fronts would have been converging upon solidification, the liquid silicon was squeezed from *several* directions by the expanding, solidified silicon into a sharply peaked bump. At a typical grain boundary, the force on the melted area only comes from only *two* directions, thus the magnitude of the feature is less.

2.3.6 Effect of Low Temperature Substrate Heating on Poly-Si Characteristics

Presently, some researchers advocate the use of low temperature (<450 °C) substrate heating to maximize the grain size of ELA poly-Si[28]. Simulations performed by other authors have suggested that heating the substrate to temperatures as low as 400 °C can extend the melt duration by as much as a factor of 2 versus annealing at RT, and as mentioned previously, longer melt durations allow the creation of larger grains. The major drawback with this technique is the amount of time needed to heat up the wafer. Implementing such a procedure into a fabrication process would greatly hinder throughput. For this reason, it is important to know how much benefit can be gained by low temperature heating. To find out, samples annealed at RT and 400 °C with a 200 nm thick SiO_2 barrier layer were studied for a variety of different energy densities. Figure 2-22 summarizes the results.

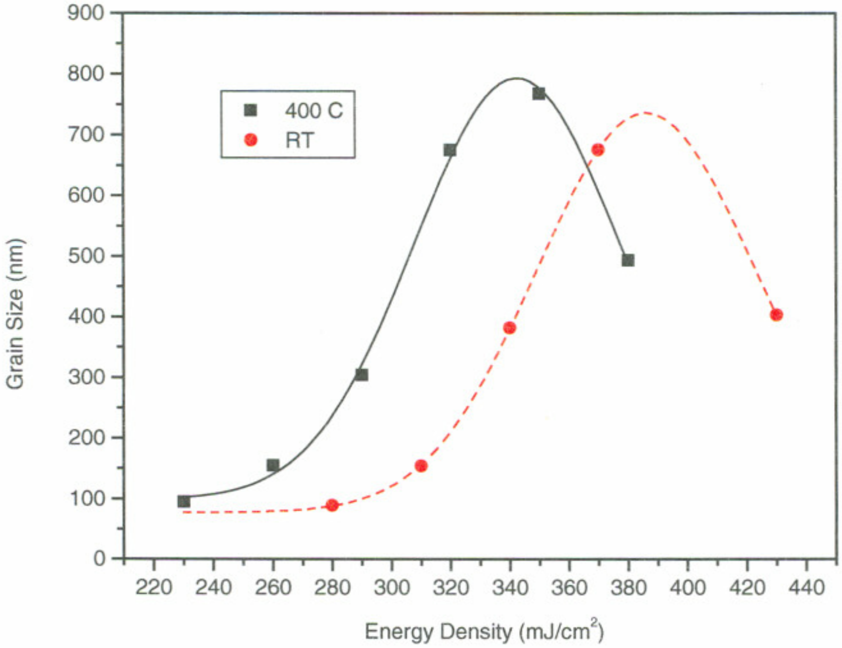


Figure 2-22: Effects of substrate temperature on grain size for ELA poly-Si. Samples annealed in vacuum at room temperature (RT) or 400 °C with a 200 nm SiO_2 barrier layer.

Somewhat surprisingly, only small improvements in the GS or grain structure for samples annealed at 400 °C were witnessed. More prominently, what occurred was a simple shifting of the peak position to higher energy densities for RT samples. Thus low temperature substrate heating does not appear to lead to any major improvement in grain size or grain morphology. Though using a lower ED to anneal samples is somewhat beneficial, the cost in processing time is too great to warrant its usage.

2.4 Summary

Several methods have been studied in an attempt to produce high quality laser annealed polysilicon films and to improve throughput. SiO_2 barrier layers allowed the formation of larger grains by slowing the cooling rate. Barriers also provided an effective means of blocking contaminant segregation from the glass. Laser annealing in a nitrogen or argon ambient allowed the formation of films with qualities comparable to vacuum. Uniformity was generally good and despite smaller grains, most of the films were indistinguishable from samples made in vacuum. Helium, on the other hand, did not produce high quality samples. Almost without exception, the films were non-uniform, as there were unavoidably regions where large grains began to grow, but were halted by the rapid cooling. Multiple passes created ordered structures and increased grain size at the same time. However, due to the points where many grain boundaries converged in the ordered films, the roughness was quite high. This continued until very large grain growth was initiated, whereupon the roughness was dramatically reduced. Multiple passes, especially when a barrier layer was employed, proved to be a viable technique to produce large grains. Use of substrate heating was shown to be unnecessary.

Chapter 3

Laser Annealed Poly-Si TFTs: Device Fabrication and Analysis

3.1 Introduction

The primary goal of this project was to fabricate high quality, laser annealed poly-Si TFTs. Through our materials analysis, several variables were isolated, related to the laser annealing process, on which to focus the investigation, in order to optimize device performance. These included

1) laser energy density
2) use of multiple passes
3) barrier layers
4) laser activated dopant
5) substrate temperature
6) annealing ambient

Because of the originality of the product, special emphasis was placed on the annealing ambient and use of multiple passes.

In the end, not only was it important to produce devices that functioned well, but also to develop a technology that enhanced reliability and uniformity. A useful technology should also ensure adequate throughput, if it is ever to be used in manufacturing. In addition, reducing the maximum temperature used in fabrication to a minimum was consequential. This could make it possible to implement a process on glass rather than quartz substrates, and in so doing, lower the manufacturing cost significantly. For these reasons, the pros and cons of each variable were carefully weighed.

3.2 Experimental Procedure

The experimental procedure described below was representative of our 'control' condition or standard. Many of the details used to laser anneal the poly-Si were explained in section 2.2. The control condition was modified by changing one of the variables mentioned above, and its effect on device performance was examined.

3.2.1 Laser Annealing

Unless otherwise stated, the poly-Si TFTs were fabricated on quartz substrates with a 200 nm thick TEOS SiO_2 barrier layer. 50 nm of amorphous silicon was deposited on the barrier layer using plasma enhanced chemical vapor deposition (PECVD), at a deposition rate of 60 nm/min and a temperature of 390 °C. To remove excess hydrogen, which could lead to ablation upon crystallization, samples were preheated to 450 °C for 2 h in a diffusion furnace, under nitrogen flow. The laser annealing took place in an evacuated chamber, at a pressure of 1 mTorr and a temperature of 400 °C. Pulses from a XeCl excimer laser (308 nm) operating at 35 Hz were used to crystallize the amorphous silicon. The beam was passed through a homogenizer and focused down to a spot size of 5 mm x 6 mm. Samples were scanned with the laser using a 96% overlap from pulse to pulse. Device wafers were either scanned completely at a single energy density, or three separate regions were processed using different energy densities. The former case gave us the opportunity to measure more devices, while the latter case allowed us to examine a greater number of conditions using fewer wafers.

3.2.2 Device Fabrication

Using a four-mask process, n-channel TFTs, having a top-metal-gate structure, as shown in figure 3-1, were fabricated.

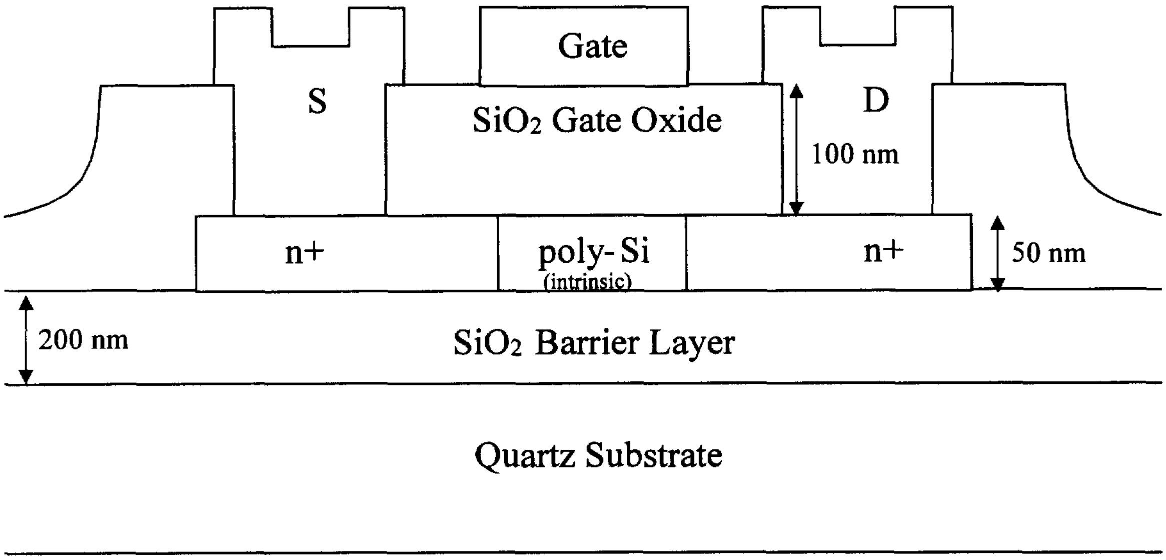


Figure 3-1: Structure of fabricated poly-Si TFTs

A planar view photograph, taken through a microscope, of an actual device is shown in figure 3-2.

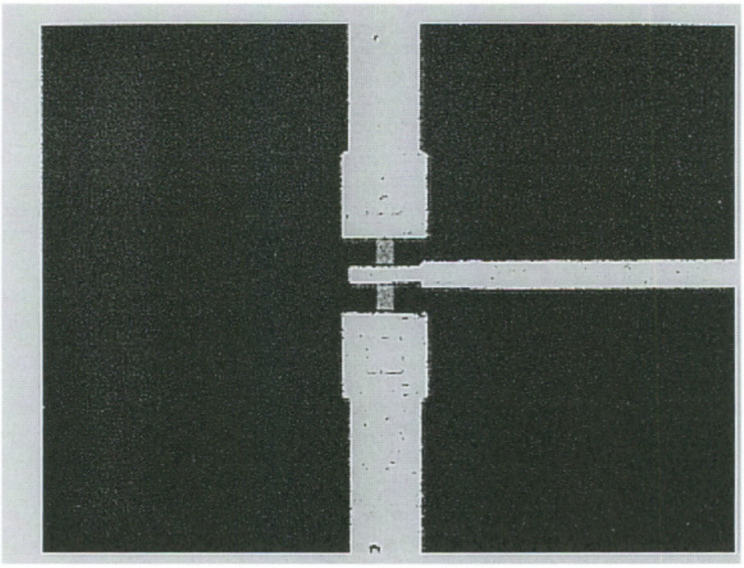


Figure 3-2: Magnified photograph of a 5 μm x 5 μm poly-Si TFT

After ELA crystallization, poly-Si islands were defined by dry etching using fluorine based chemistry ($CF_4 + O_2$). Subsequently, a 100 nm thick SiO_2 gate oxide was deposited by PECVD from a silane/nitrous-oxide gas mixture at 400 °C. Following the gate insulator deposition, source and drain regions were formed by ion implantation of phosphorous through a mask with a dose of 1×10^{16} cm^{-2}, through the oxide. The dopant was activated by a furnace anneal at 800 °C for 20 minutes, which also served to densify the gate oxide layer. This short, high temperature step has little or no effect on grain size or grain structure. Contact holes were opened by wet etching in a dilute buffered HF solution (50:1) for 6-8 minutes and immediately thereafter, a 1 μm thick stack of AlCu/TiN/Ti was deposited by sputtering at 400 °C. Patterning the metal layer using chlorine based dry etching simultaneously formed the gate, source and drain electrodes. Finally, a forming gas anneal was performed at 450 °C for 30 minutes to sinter the metal contacts. Unless otherwise stated, no hydrogen passivation was carried out.

3.2.3 Device Characterization

The TFTs were characterized using a Hewlett Packard semiconductor analyzer. Anywhere from thirty to seventy-five 5 μm x 5 μm devices were measured for each laser annealing condition, to ensure accurate statistics for the device characteristics. The devices were chosen from positions all over the wafer to maximize variability. The majority of the measurements consisted of I_D-V_G data taken at room temperature with $V_{DS} = 0.1V$, where the gate voltage was varied from +20V to -20V. The field effect mobility (μ) and threshold voltage (V_T) were determined, in the usual way, from the slope and intercept of a linear fit on a linear-linear plot, fitted at the point where the transconductance reached a maximum. An example of how the transconductance varied as a function of gate voltage is shown in figure 3-3.

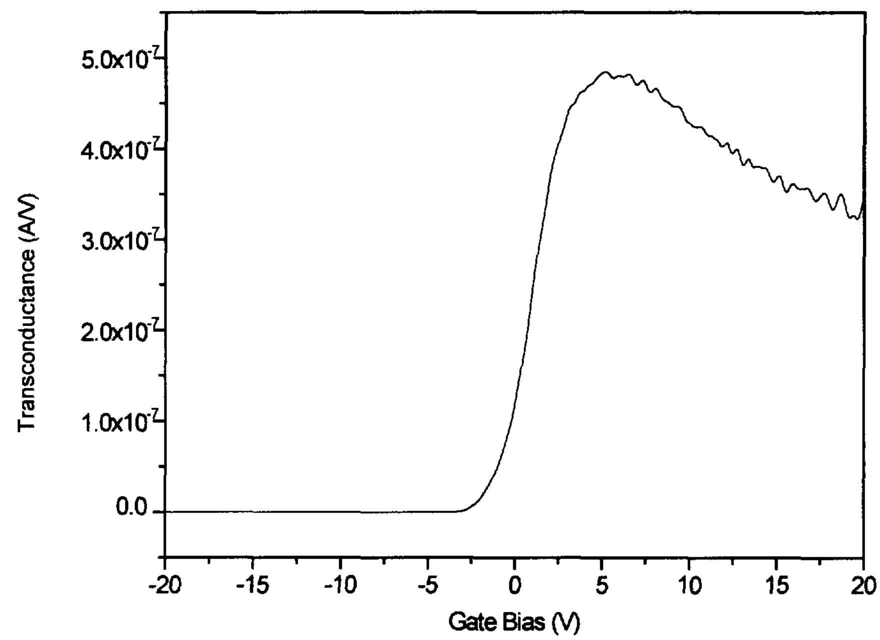


Figure 3-3: Transconductance of ELA poly-Si TFT. The device was annealed at 400 °C in vacuum with a 200 nm thick SiO_2 barrier, using a single scan at 305 mJ/cm^2.

The transconductance first increases with gate voltage as the potential barriers at the grain boundaries lower[34], and decreases at higher gate voltages, as the current becomes limited by surface roughness scattering. The on and off currents were taken to be the maximum and minimum currents, respectively, over the gate voltage range. The leakage current was determined for V_{DS} = 10V and V_{DS} = 0.1V. The subthreshold swing (S) was derived from the subthreshold slope, as measured from the maximum slope of I_D-V_G on a log-linear plot, fitted with an exponential function. For selected devices, measurements were made at elevated temperatures from 20 °C to 100 °C. By using a linear fit of a log(I_D) vs. 1/kT plot, where T is the absolute temperature and k is the Boltzmann constant, the source-drain current activation energy was determined (with V_{DS}=0.1V). An example of this technique is shown in figure 3-4, measured from a sample laser annealed in air at 280 mJ/cm^2 and 400 °C.

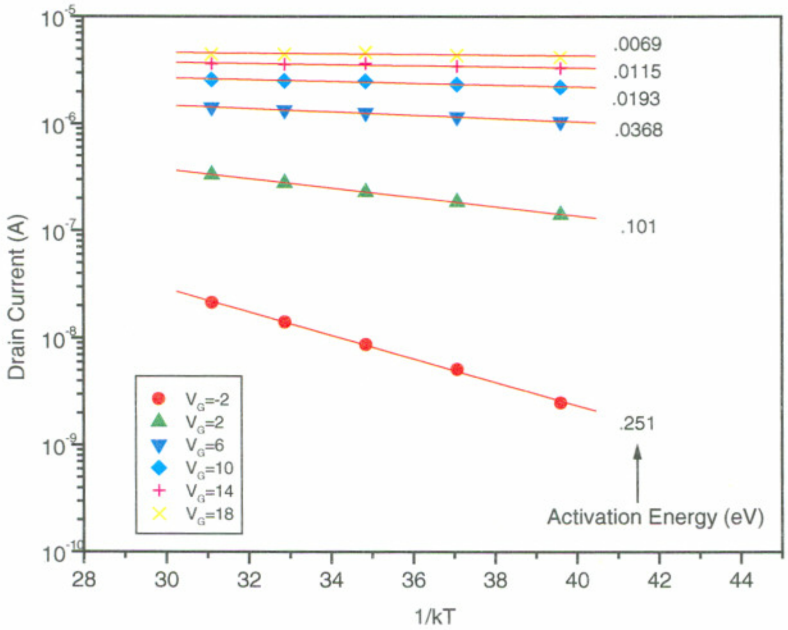


Figure 3-4: Demonstration of source-drain current activation energy extraction. This sample was laser annealed using a single scan (280 mJ/cm^2) in air at 400 °C.

3.3 Modeling Poly-Si TFTs

Thin film transistors can be modeled in many ways. The presence of grain boundaries makes the analysis of poly-Si TFTs more complicated than that of bulk silicon devices. Grain boundaries are lined with dangling bonds, which can act as hole or electron traps. In addition, intra-grain defects must be accounted for. All of the analysis presented hereafter focuses on undoped polysilicon material.

The two most general methods for modeling TFTs are the distributed method, which is essentially a 1-D treatment, where traps are considered to be uniformly spread throughout the channel, and the two-dimensional approach, where the position of grain boundaries in the channel is considered[35]. The distributed method is more straightforward and works well in small grained material. The 2-D approach is more accurate for large grained poly-Si, though the equations defining operation are complicated, resulting in less efficient calculations.

The presence of grain boundaries and intra-grain defects leads to a distribution of trapping energy levels within the band structure of the poly-Si material. Evidence suggests that so-called deep states, located near the center of the bandgap, are caused by dangling bonds and correctly represented by a Gaussian distribution[36]. Intra-grain strained bonds give rise to tail states, which decay exponentially from the conduction and valence band edges[37]. Even so, for simplicity, trapping level are often represented by single energy levels. This approach speeds up the calculation at the cost of accuracy.

For the 1-D and the 2-D approaches, the electrostatic analysis of the on-current is different from standard MOSFETs due to the presence of trapped charge. This charge affects Poisson's equation and may lead to the formation of 2-D barrier potentials. It is widely believed that the enhanced leakage current in poly-Si TFTs arises from the emission of charge carriers from trapping states[38]. Opinions differ, however, as to the mode of emission and the source and location of the trap sites. An analytical development of the electrical characteristics of poly-Si TFT is presented in the appendix (A1).

3.3.1 Computer Simulations of Polysilicon TFTs

The ATLAS and ATHENA[39] software programs present a simple but powerful package for modeling electronic devices. In ATHENA, a device is built up as it would be in a fab using CVD, sputtering, implantation, etching or any other processing technique. The device structure is then transferred to ATLAS which solves the relevant equations for current versus voltage, the electric field, the electrostatic potential, the quasi-Fermi level as a function of position, or a variety of other quantities. All of the models used in both ATLAS and ATHENA are physical models. For this reason, by simulating the behavior of a device, insight into the mechanisms causing certain behavior can be studied.

Development of a simulator is a necessary and essential step because, unlike most experiments, simulators point to the source of behavior rather than simply showing the behavior itself. Though development of realistic numbers that mimic device behavior is important, the qualitative features are often more so. For this reason, the trends that ensue, when a parameter related to the characteristics of the poly-Si is varied, have been studied and are explored below.

3.3.2 Model for Simulation

Using ATLAS and ATHENA, an n-channel, top-gate polysilicon thin film transistor with a 100 nm thick gate oxide was fabricated and simulated. To reduce the computing time, the channel length was fixed at around 1 μm, though some simulations were also performed for a 5 μm device. The silicon and oxide regions were deposited by CVD. The dopants were implanted and fully activated. Aluminum was used for the metal layer. To isolate the effects of the polysilicon, the source and drain series resistance (R_S and R_D respectively) were neglected for most of the simulations. The 50 nm thick active region was defined to be silicon with the inclusion of trap states within the bandgap. For simplicity, the traps were uniformly distributed throughout the channel, as in the distributed method above. This is an approximation to the real world situation, and one that becomes less accurate as the grain size of the poly-Si approaches the channel length. The simulated device is shown in figure 3-5.

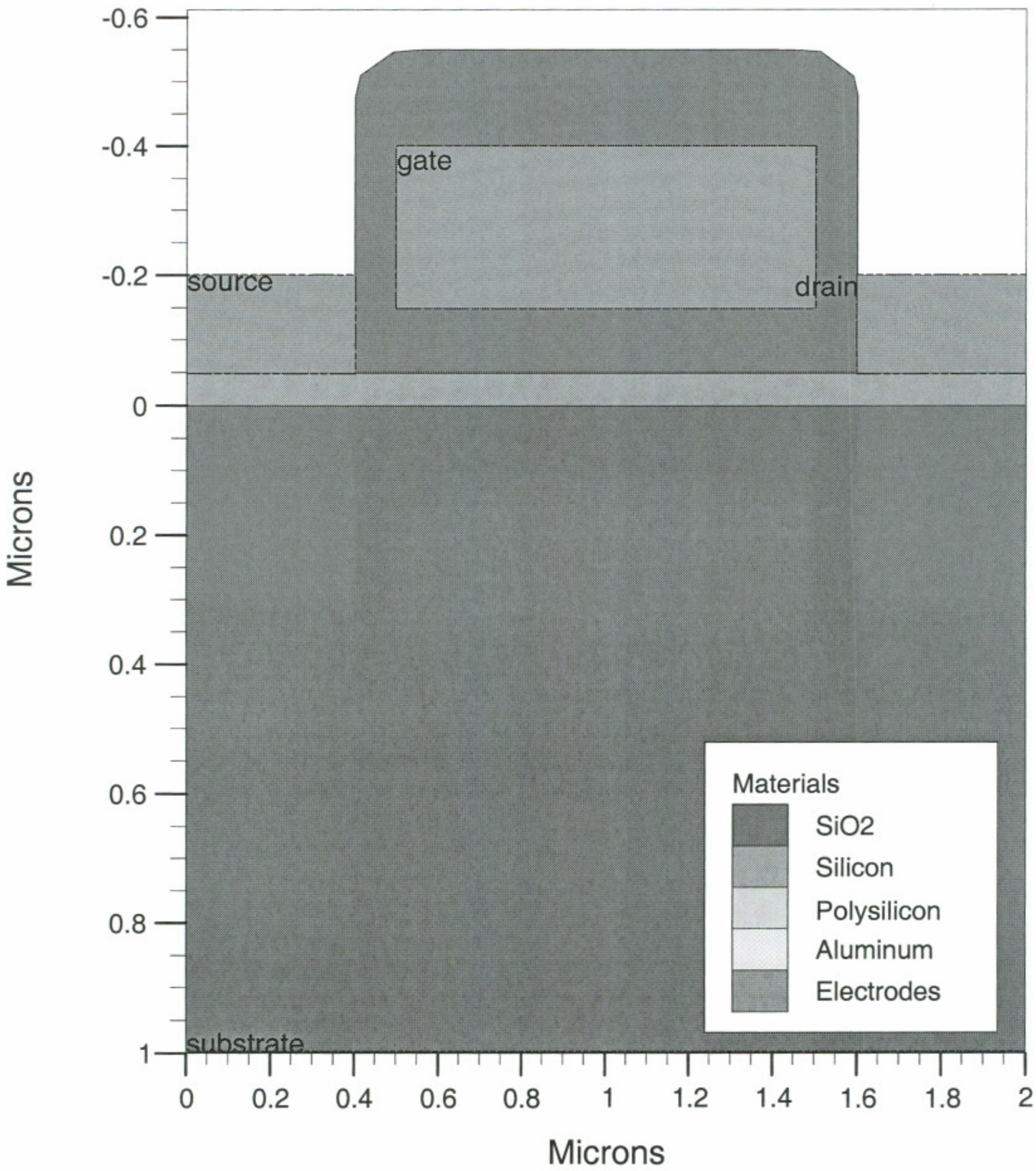


Figure 3-5: Structure of simulated poly-Si TFT

In general, ATLAS solves Poisson's equation (3-1) and the continuity equations for electrons and holes, shown in (3-2), using a finite element method.

$$\nabla^2 \psi(x,y) = -\frac{\rho(x,y)}{\varepsilon_{si}} \tag{3-1}$$

$$\frac{\partial n}{\partial t} = G_n - R_n + \frac{1}{q}\nabla \bullet J_n \tag{3-2}$$

$$\frac{\partial p}{\partial t} = G_p - R_p - \frac{1}{q}\nabla \bullet J_p$$

where x is the position variable perpendicular to the poly-Si surface, y is the position variable parallel to the surface, $\rho(x,y)$ is the charge density, ε_{si} is the dielectric constant of silicon and $\psi(x,y)$ is the electrostatic potential. In the above equations, $\boldsymbol{J}_n$ and $\boldsymbol{J}_p$ are the electron and hole current densities, n and p are the electron and hole carrier concentrations, G_n and G_p are the electron and hole generation rates, and R_n and R_p are the electron and hole recombination rates. In the finite element method, a user defined grid is applied to the two dimensional area of the device and solutions are approximated by simple functions over the sub-domains. By matching solutions of the individual elements, the total solution is built up.

Depending on the particular physical models selected, charge transport is further refined by using a Boltzmann transport equation, the simplest of which is the drift-diffusion model. The conventional formulation of drift-diffusion for conduction electrons is

$$J_n = nq\mu_n F + qD_n \nabla n \tag{3-3}$$

where D_n is the diffusion constant for electrons, μ_n is the electron mobility model selected by the user, F is the local electric field, ∇n is the electron concentration gradient, and the electron carrier concentration can be expressed using Boltzmann statistics as

$$n = n_i \times \exp\left[{q(\psi_i - \phi_f)} \Big/ {kT} \right] \tag{3-4}$$

and where ψ_i is the intrinsic potential and ϕ_f is the Fermi potential. If the Quasi-Fermi level ψ_n is introduced, n can be re-formulated as

$$n = n_i \times \exp\left[{q(\psi_i - \psi_n)} \Big/ {kT} \right] \tag{3-5}$$

where $\psi_n = \psi_i - \frac{kT}{q} \times \ln\left(n \big/ n_i \right)$

The current density can then be expressed as

$$J_n = -q\mu_n n \nabla \psi_n \tag{3-6}$$

Equation (3-6) is used directly by ATLAS.

For the TFT simulations, the trap states in the bandgap consisted of both deep and tail states and acceptor type states and donor type states. The deep donor and acceptor states were modeled as Gaussians with the center of the Gaussians at approximately 0.35 eV above the valence band edge. The positioning is based on work done by others[36]. The deep states are generally associated with dangling bonds due to the existence of grain boundaries within the channel region. The tail DOS were modeled as exponentials decaying from the band edges. Tail states are associated with intra-grain defects and thought to arise from strained Si bonds. Capture cross-sections for both electrons and holes in the deep and tail states were defined separately, and based on work done by others[40]. The presence of interfacial defects at the Si/SiO_2 gate oxide junction were also accounted for by assigning values for the electron and hole surface recombination velocities (s_n and s_p respectively) and the fixed charge density at the interface (Q_{it}). The effect of fixed oxide charge on the back interface (Q_{BIT}) was also examined.

The energy distribution of the total defect density N(E) in the bandgap is the sum of the acceptor tail states $N_{AT}(E)$, the donor tail states $N_{DT}(E)$, the acceptor deep states $N_{AG}(E)$, and the donor deep states $N_{DG}(E)$, where $E_V<E<E_C$:

$$N(E) = N_{AT}(E) + N_{DT}(E) + N_{AG}(E) + N_{DG}(E) \tag{3-7}$$

and

$$N_{AT}(E) = N_{TA} \times \exp\left(\frac{E - E_C}{W_{TA}}\right) \tag{3-8}$$

$$N_{DT}(E) = N_{TD} \times \exp\left(\frac{E_V - E}{W_{TD}}\right) \tag{3-9}$$

$$N_{AG}(E) = N_{AG0} \times \exp-\left(\frac{E - E_{GA}}{W_{GA}}\right)^2 \tag{3-10}$$

$$N_{DG}(E) = N_{DG0} \times \exp-\left(\frac{E - E_{GD}}{W_{GD}}\right)^2 \tag{3-11}$$

The values for N_{TA} and N_{TD} are selected by the user. The parameters N_{AG} and N_{DG} are evaluated by ATLAS from equations (3-12) and (3-13), where N_{GA} and N_{GD} are user specified:

$$N_{GA} = \int_{-\infty}^{\infty} N_{AG}(E)dE \tag{3-12}$$

$$N_{GD} = \int_{-\infty}^{\infty} N_{DG}(E)dE \tag{3-13}$$

The probability of occupation of a trap level at energy E_t is given by[44]:

$$f(E_t, n, p) = \frac{V_{th} \times \sigma_{ijE} \times n + e_p}{V_{th}(\sigma_{ijE} \times n + \sigma_{ijH} \times p) + e_n + e_p} \tag{3-14}$$

where

$$e_n = V_{th} \times \sigma_{ijE} \times n_i \times \exp\left(\frac{E_t - E_i}{kT}\right) \tag{3-15}$$

$$e_p = V_{th} \times \sigma_{ijH} \times n_i \times \exp\left(\frac{E_i - E_t}{kT}\right) \tag{3-16}$$

and e_n and e_p are the electron and holes emitted per second from electron and hole occupied generation/recombination centers respectively. V_{th} is the carrier thermal velocity, σ_{ijE} and σ_{ijH} are the capture cross-sections for electrons and holes respectively where i is either T for tail distributions or G for Gaussian and j is either D for donor-like states or A for acceptor like states. Typical values for the user-defined parameters are shown in table 3-1.

Table 3-1. Nominal values for parameters used in ATLAS poly-Si TFT simulations

Parameter	Description	Units	Value
$N_{TA}=N_{TD}$	Conduction and valence band edge intercept density of states	cm^{-3}	1×10^{20}
$N_{GA}=N_{GD}$	Total density of deep acceptor-like and donor-like states	cm^{-3}	1×10^{18}
Q_{it}	Trapped charge density at gate oxide/poly-Si interface (/q)	cm^{-2}	1×10^{11}
Q_{BIT}	Trapped charge density at barrier layer/poly-Si interface (/q)	cm^{-2}	0
$s_n=s_p$	Interface recombination velocity	cm/s	0
σ_{ijE}	Capture cross section for electrons	cm^2	1×10^{-16}
σ_{ijH}	Capture cross section for holes	cm^2	1×10^{-14}
$W_{TA}=W_{TD}$	Characteristic decay energy for acceptor-like and donor-like tail states	eV	0.020
$W_{GA}=W_{GD}$	Characteristic decay energies for acceptor-like and donor-like deep states	eV	0.015
$R_S=R_D$	Source and drain series resistance	ohms	0

A comprehensive model developed by J.T. Watt[41] was used to describe the majority and minority carrier mobilities. The Watt model takes into consideration phonon scattering, surface roughness effects caused by deviations from an ideally planarized Si/SiO_2 interface, and charged impurity scattering caused by interaction between inversion layer carriers and ions, as well as electric filed effects. Other models included were impact ionization and band to band tunneling, each of which become more significant for large values of V_{DS} and/or V_G. In addition, Shockley-Read-Hall (SRH) recombination/generation was also employed[42]. For the tabulated results below, the following definitions apply:

I_{off} = minimum drain current density in A/μm as a function of gate voltage

$I(-20)$ = drain current density in A/μm for V_G=-20 V

I_{on} = maximum drain current density in A/μm as a function of gate voltage

V_T = threshold voltage in V (extracted from linear plot)

S = subthreshold swing in V/decade

μ = field-effect mobility in cm^2/Vs

Unless otherwise stated, $N_{TA}=N_{TD}=1\text{x}10^{20}$ cm^{-3}, $N_{GA}=N_{GD}=1\text{x}10^{18}$ cm^{-3}, $Q_{it}=1\text{x}10^{11}$ cm^{-2}, $s_n=s_p=0$ cm/s, $Q_{BIT}=0$ and $R_S=R_D=0$ ohms. Both transfer characteristics and tabulated results were obtained for $V_{DS}=0.1$ V. The source contact was used as a reference potential (ground) throughout.

3.3.3 Simulation Results

Table 3-2 shows the effect of the tail DOS on the device characteristics, for $V_{DS}=0.1$ V, and transfer characteristics are shown in figure 3-6, where the gate voltage was varied from +20V to –20V.

Table 3-2: Effect of tail DOS on device characteristics for simulated poly-Si TFTs

$N_{TA}=N_{TD}$	I_{off}	I(-20)	I_{on}	V_T	S	μ
$1\text{x}10^{17}$	$2.00\text{x}10^{-16}$	$5.37\text{x}10^{-16}$	$3.72\text{x}10^{-5}$	1.18	0.64	679
$1\text{x}10^{18}$	$1.62\text{x}10^{-16}$	$5.89\text{x}10^{-16}$	$3.71\text{x}10^{-5}$	1.18	0.64	679
$1\text{x}10^{19}$	$2.00\text{x}10^{-16}$	$3.24\text{x}10^{-16}$	$3.67\text{x}10^{-5}$	1.20	0.64	664
$1\text{x}10^{20}$	$5.37\text{x}10^{-17}$	$1.82\text{x}10^{-15}$	$3.29\text{x}10^{-5}$	1.33	0.65	552
$5\text{x}10^{20}$	$3.72\text{x}10^{-16}$	$1.62\text{x}10^{-15}$	$2.10\text{x}10^{-5}$	2.62	0.69	350
$1\text{x}10^{21}$	$1.62\text{x}10^{-16}$	$7.94\text{x}10^{-16}$	$1.28\text{x}10^{-5}$	3.18	0.73	181
$1\text{x}10^{22}$	$1.67\text{x}10^{-16}$	$7.94\text{x}10^{-16}$	$1.11\text{x}10^{-6}$	4.42	0.99	18
$1\text{x}10^{23}$	$4.68\text{x}10^{-16}$	$4.48\text{x}10^{-16}$	$1.02\text{x}10^{-7}$	6.01	1.47	1.7

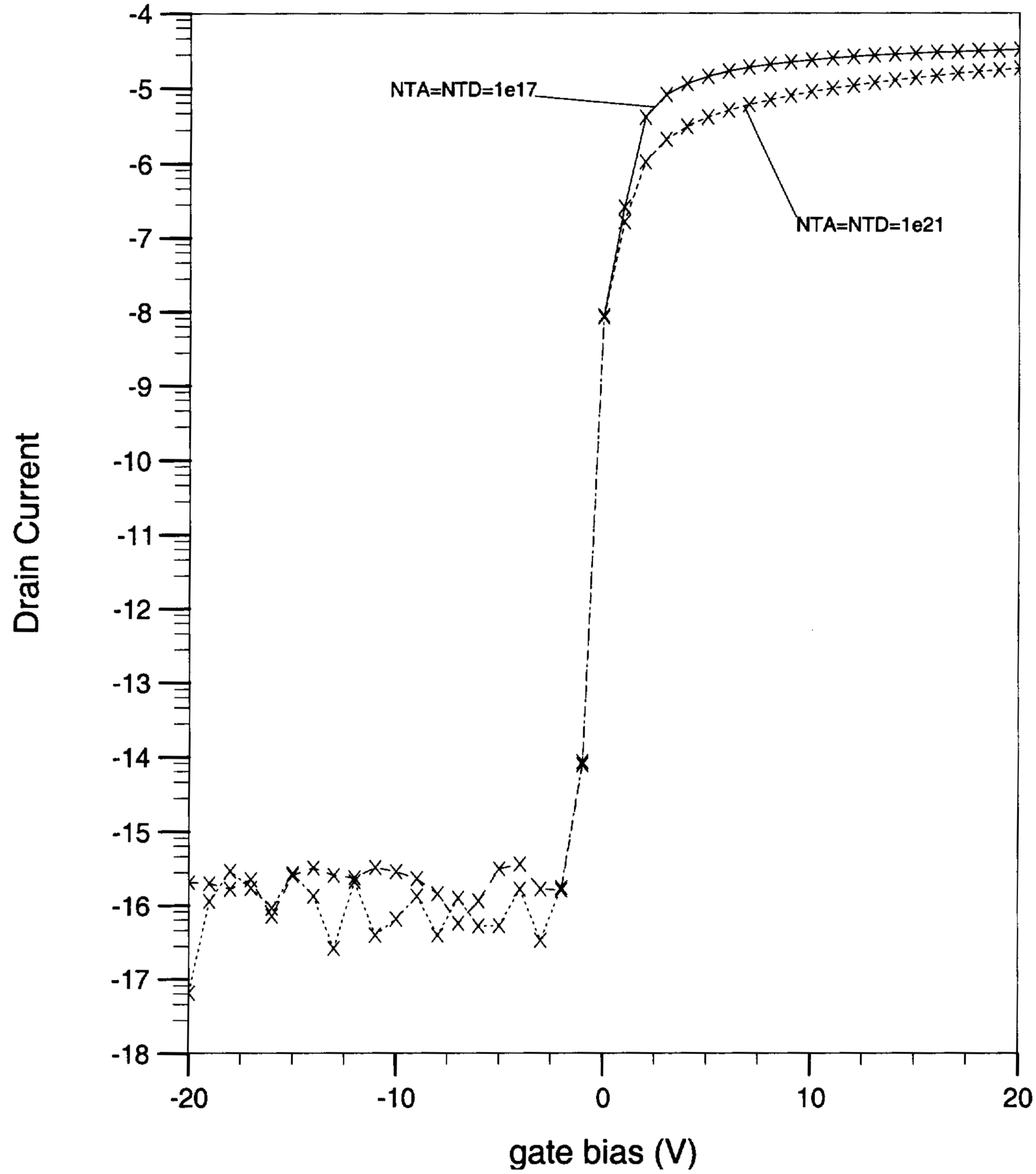


Figure 3-6: Simulated poly-Si TFT transfer characteristics for 2 devices where N_{TA}=N_{TD}=1x10^{21} cm^{-3} or N_{TA}=N_{TD}=1x10^{17} cm^{-3}.

From the chart and figure, it is evident that all of the on-state characteristics are sensitive functions of the tail DOS, though the subthreshold slope is less so. The mobility, in particular, changed abruptly from around 550 cm^2/Vs at N_{TA}=N_{TD}=1x10^{20} cm^{-3} to around

18 cm^2/Vs at $N_{TA}=N_{TD}=1x10^{22}$ cm^{-3}. The off-state characteristics, on the other hand, varied independently of the tail DOS. Because the current values were so low, any differences are more likely the results of the solution method rather than the physical parameters.

Table 3-3 shows how the deep states affect device performance for V_{DS}=0.1 V, and transfer characteristics are in figure 3-7.

Table 3-3: Effect of deep DOS on device characteristics for simulated poly-Si TFTs

$N_{GA}=N_{GD}$	I_{off}	I(-20)	I_{on}	V_T	S	μ
$1x10^{17}$	$2.00x10^{-17}$	$2.47x10^{-16}$	$3.48x10^{-5}$	0.29	0.51	549
$1x10^{18}$	$5.37x10^{-17}$	$1.82x10^{-15}$	$3.29x10^{-5}$	1.33	0.65	552
$5x10^{18}$	$1.91x10^{-17}$	$2.39x10^{-16}$	$2.74x10^{-5}$	4.12	1.16	528
$1x10^{19}$	$7.59x10^{-16}$	$8.17x10^{-16}$	$2.34x10^{-5}$	5.98	1.35	497
$5x10^{19}$	$7.94x10^{-15}$	$7.94x10^{-15}$	$8.00x10^{-6}$	13.8	2.57	373
$1x10^{20}$	$1.82x10^{-14}$	$1.82x10^{-14}$	$1.15x10^{-6}$	17.5	3.17	136
$1x10^{21}$	$2.29x10^{-13}$	$2.29x10^{-13}$	$1.17x10^{-10}$	19.1	6.23	54

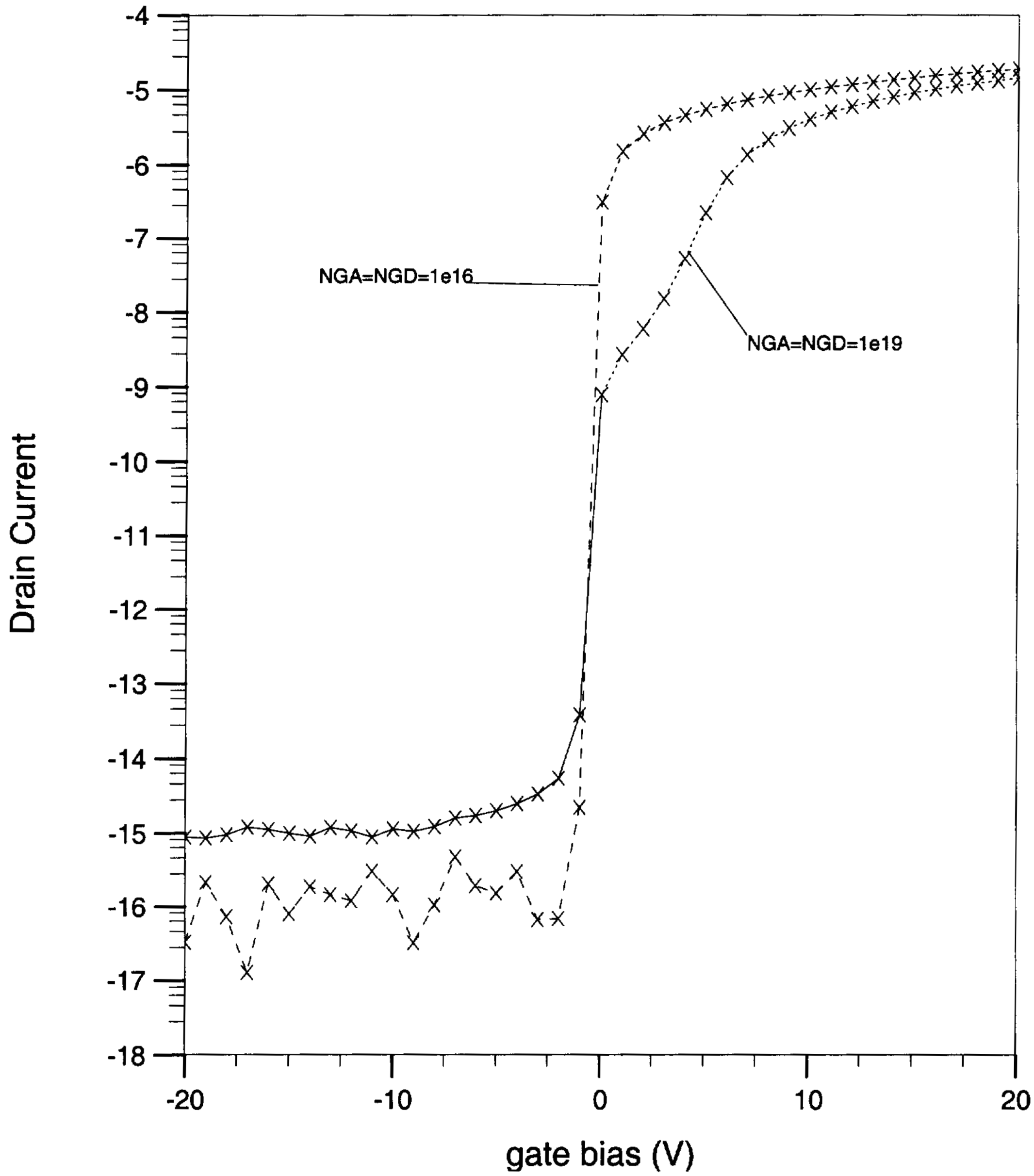
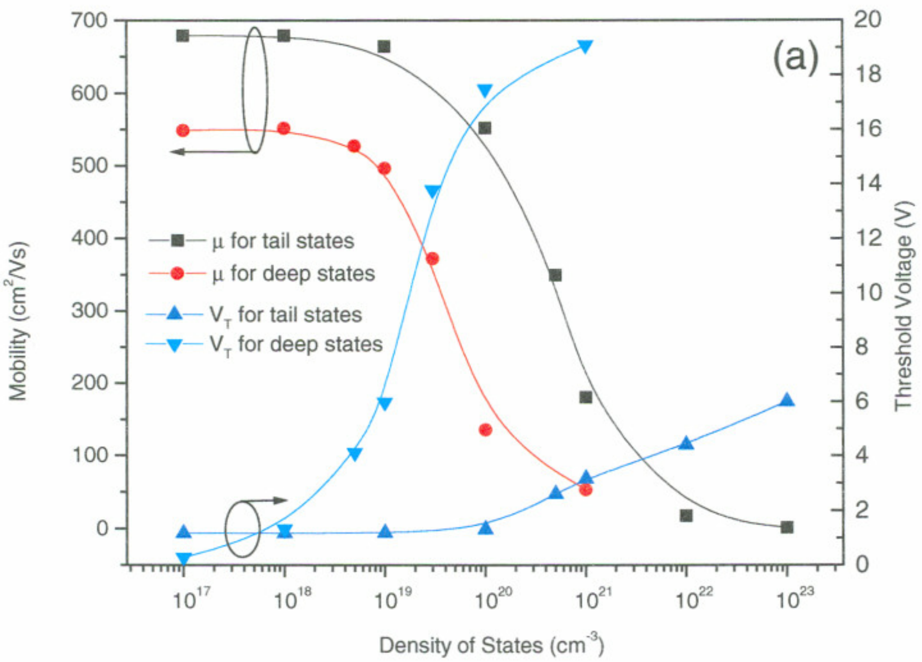


Figure 3-7: Simulated poly-Si TFT transfer characteristics for 2 devices where $N_{GA}=N_{GD}=1x10^{16}$ cm^{-3} or $N_{GA}=N_{GD}=1x10^{19}$ cm^{-3}.

Again, the on-state characteristics, and particularly the subthreshold swing and the threshold voltage, are strongly influenced. Comparing to the previous case, the subthreshold slope and threshold voltage are influenced more heavily by the deep DOS than the tail DOS, while the mobility and on-current are affected more equally. Similar to the tail DOS, over a range of values, the deep DOS had little control of the off-state characteristics. However, starting with a deep DOS of $1x10^{19}$ cm^{-2}, a trend in the leakage current developed, which continued as the value was further increased, due to SRH generation. The magnitude of the deep DOS required for this to happen though was too large to give realistic on-state characteristics, in a physical sense, as exemplified by the threshold voltage around 19 V.

Figure 3-8 (a) and (b) show a graphical comparison of the device characteristics as a function of both the tail and deep DOS.



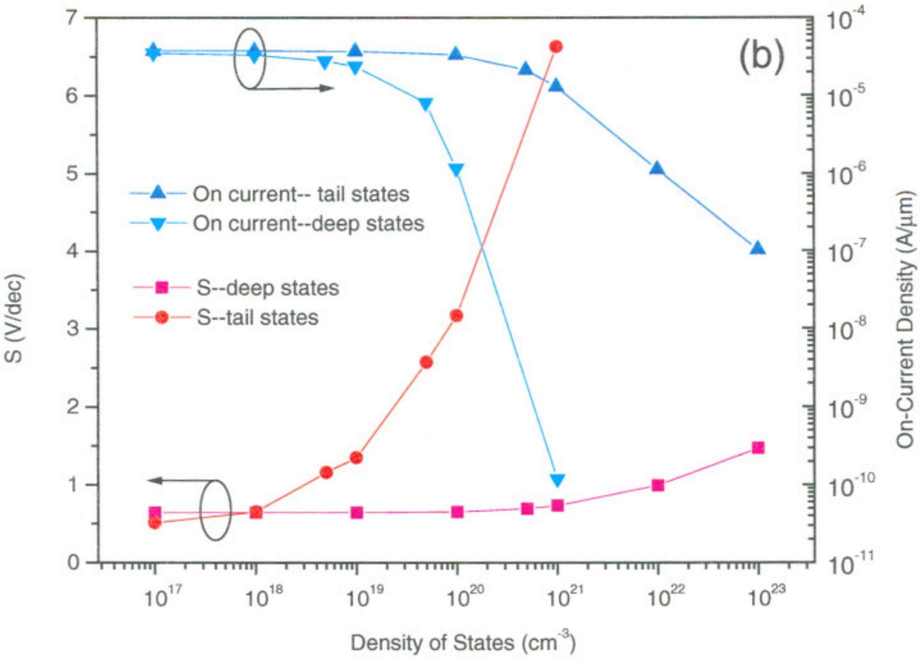


Figure 3-8: Simulated device characteristics showing the effect of deep and tail density of states on (a) field-effect mobility and threshold voltage and (b) subthreshold swing and on-current density.

This figure suggests several important results. First, looking at the threshold voltage, the deep DOS influences this value much more strongly than the tail DOS. Therefore, all other quantities being equal, the grain size should play an important role in determining the threshold voltage. At first glance, it appears that the deep and tail DOS play equally important roles in determining the field effect mobility. Notice though that the range of values over which the mobility changes significantly as a function of the deep DOS lead to unrealistically high threshold voltages. Much above 5×10^{19} cm^{-3}, V_T becomes exceedingly large. Confining the deep DOS to below this value suggests that the tail DOS plays a more vital role in determining the mobility. The same can be said for the on current. Even though the deep DOS can influence this value strongly, it can not do so while maintaining realistic values for the threshold voltage. The subthreshold slope, on the other hand is strongly affected by the deep DOS, even at relatively low values.

From table 3-4, again for V_{DS}=0.1 V, the fixed charge on the gate oxide/poly-Si interface changed the threshold voltage, and had a small impact on the subthreshold slope, but little else, while the surface recombination velocity at the interface only affected the leakage current at large, negative gate voltages.

Table 3-4: Effect of fixed interface charge and Si/SiO$_2$ surface recombination velocity on characteristics of simulated poly-Si TFTs.

Q_{it}	s_n=s_p	I_{off}	I(-20)	I_{on}	V_T	S	μ
$1x10^{11}$	$1x10^{4}$	$5.37x10^{-17}$	$1.82x10^{-15}$	$3.29x10^{-5}$	1.31	0.66	561
$1x10^{11}$	$1x10^{5}$	$5.37x10^{-17}$	$1.82x10^{-15}$	$3.29x10^{-5}$	1.31	0.66	561
$1x10^{11}$	$1x10^{6}$	$5.37x10^{-17}$	$3.63x10^{-14}$	$3.29x10^{-5}$	1.31	0.66	561
$1x10^{11}$	$1x10^{7}$	$5.37x10^{-17}$	$3.71x10^{-13}$	$3.29x10^{-5}$	1.31	0.66	561
$1x10^{11}$	$1x10^{8}$	$5.37x10^{-17}$	$3.63x10^{-12}$	$3.29x10^{-5}$	1.31	0.66	561
$1x10^{11}$	$1x10^{9}$	$5.37x10^{-17}$	$3.55x10^{-11}$	$3.29x10^{-5}$	1.31	0.66	561
$1x10^{9}$	$1x10^{4}$	$1.62x10^{-16}$	$3.26x10^{-16}$	$3.23x10^{-5}$	1.78	0.47	551
$1x10^{10}$	$1x10^{4}$	$1.07x10^{-16}$	$5.89x10^{-16}$	$3.23x10^{-5}$	1.74	0.52	551
$1x10^{12}$	$1x10^{4}$	$4.27x10^{-16}$	$7.41x10^{-16}$	$3.85x10^{-5}$	-0.28	0.69	552
$2x10^{12}$	$1x10^{4}$	$5.15x10^{-16}$	$6.32x10^{-16}$	$4.36x10^{-5}$	-7.69	0.70	546

With a low level of interface traps, the leakage current for V_{DS}=0.1 V did not increase as V_{GS} approached -20 V, whereas for values of s_n=s_p in the 10^7 range or above, the leakage current increased approximately exponentially, as shown in figure 3-9.

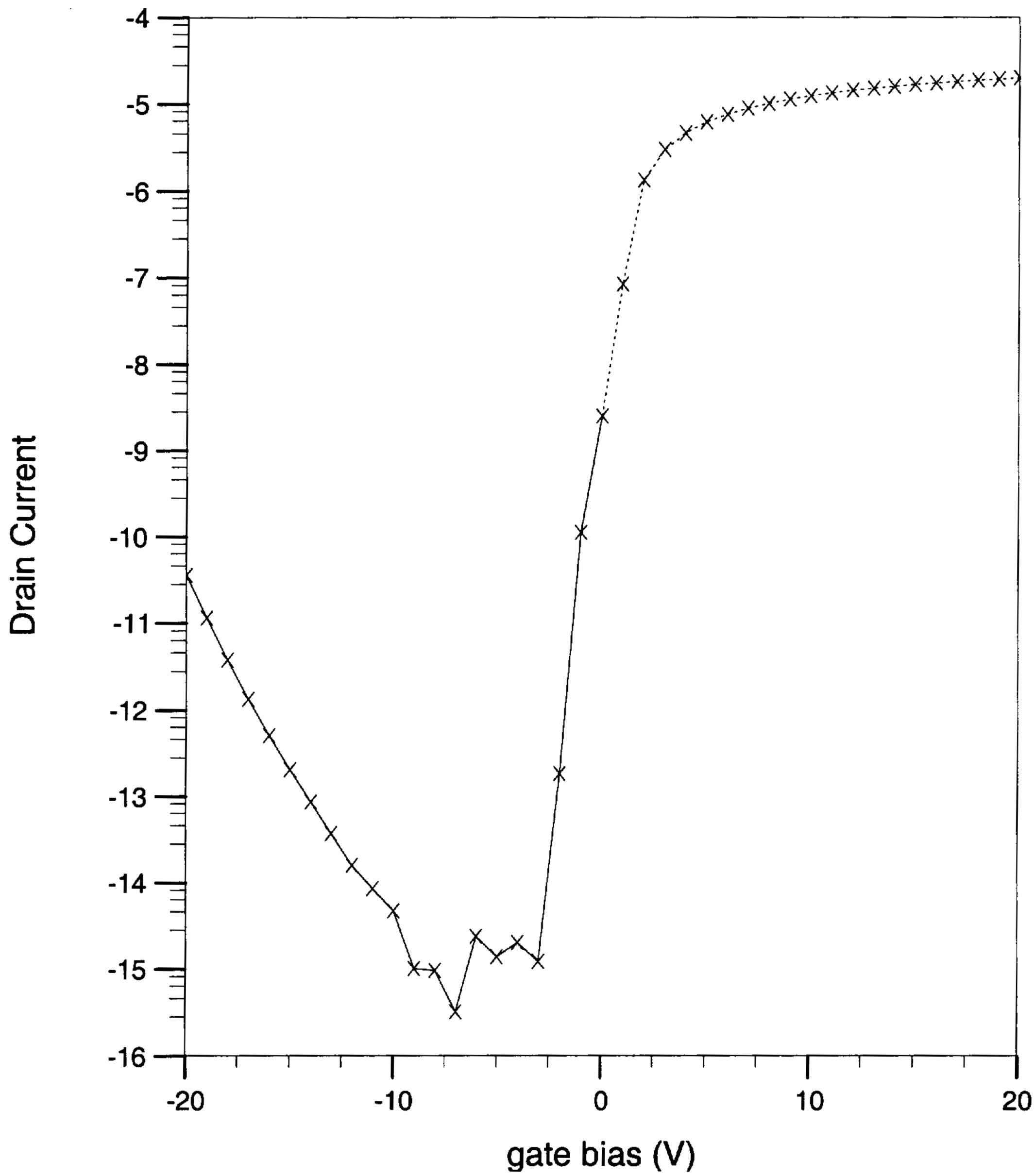


Figure 3-9: Simulated poly-Si TFT transfer characteristics for a device where s_n=s_p=1x10^9 cm/s.

This was due to a greater number of holes recombining at the interface, which in turn, gave rise to a recombination current. Thus for these simulations, the condition of the interface largely determined the leakage current. This is not entirely unrealistic, as other authors have suggested that it may be traps at the Si/SiO_2 gate oxide interface which affect the leakage current, though it is still unclear[38].

ATLAS falls short in its ability to accurately simulate the off-state of TFTs because it does not have a model to describe field emission from traps under equilibrium conditions. In real world devices, for n-channel poly-Si TFT, the leakage current increases almost exponentially for large negative gate biases due to field-emission in the drain region[43]. Band to band tunneling did come into play, but only for large values of V_{DS}, as shown in figure 3-10.

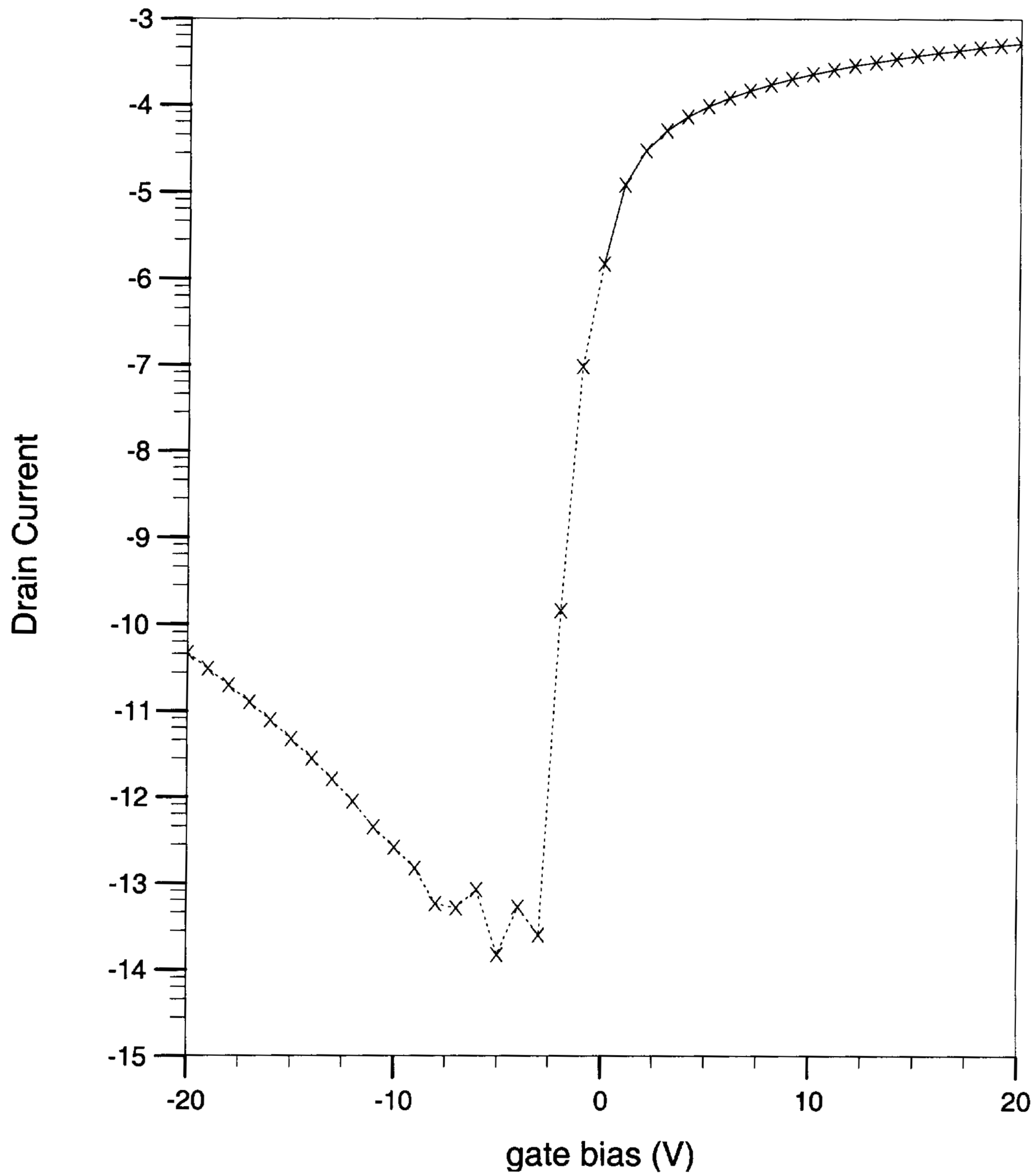


Figure 3-10: Simulated poly-Si TFT transfer characteristics for a device where V_{DS}=10V. As V_G approached –20 V, the leakage current increased approximately exponentially, even with s_n=s_p=0, due to band to band tunneling.

Under these circumstances the correct leakage current behavior was modeled (exponentially increasing drain leakage current for large negative gate bias), though in actual devices, this same behavior exists for low V_{DS} values.

To further refine the model, a lumped value for the contact resistance was applied to the source and drain electrodes. The effect of this modification could be seen for high drain current values, where the drain current deviated from the linear region of operation, as a function of the gate voltage, at lower current levels. I_D-V_G characteristics for an actual device laser annealed in vacuum at 305 mJ/cm^2 and 400 °C can be seen in figure 3-11. This is shown along with a best fit for a 5 μm simulated device, assuming Q_{BIT}=0

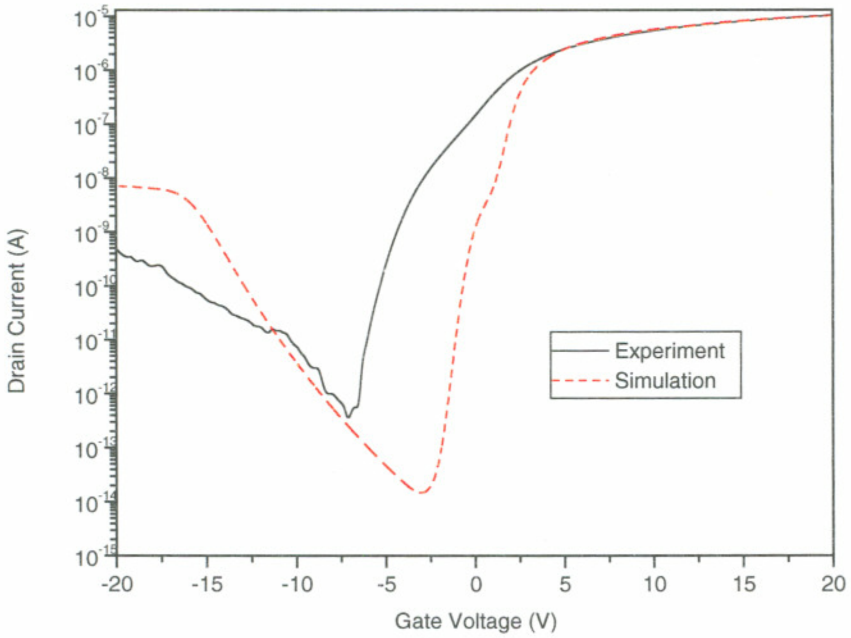


Figure 3-11: Comparison between simulated poly-Si TFT transfer characteristics for a 5 micron device and an actual device laser annealed at 400 °C in vacuum using an energy density of 305 mJ/cm^2.

For this simulation, the following values for the user-defined parameters were used:

$N_{TA}=N_{TD}=1x10^{19}$ cm^{-3} $s_n=s_p=1x10^{11}$ cm/s

$N_{GA}=N_{GD}=1x10^{18}$ cm^{-3} $R_S=R_D=2x10^3$ ohms

$Q_{it}=1x10^{10}$ cm^{-2} $Q_{BIT}=0$

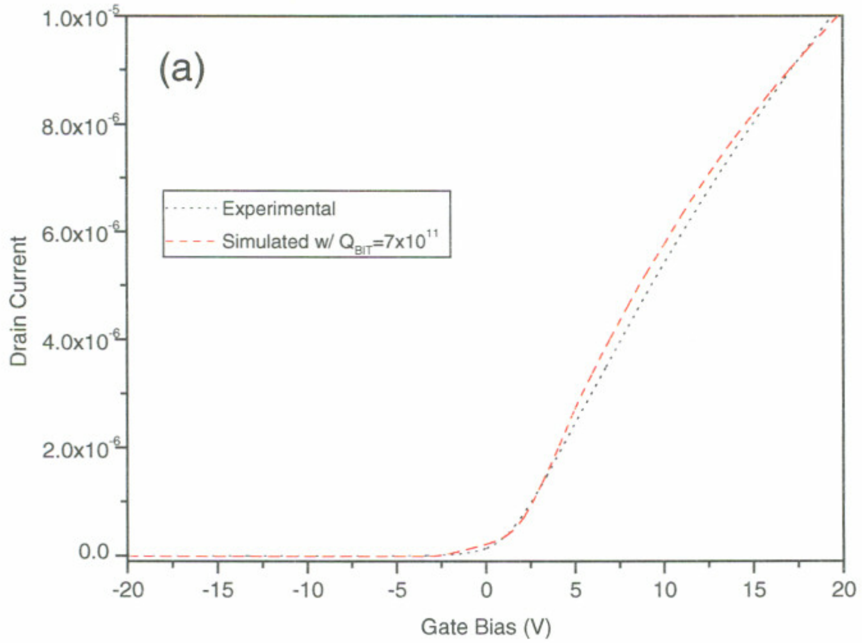
A comparison of the performance criteria for the actual device and the simulated one are shown in table 3-5.

Table 3-5: Device characteristics of an actual poly-Si TFT laser annealed in vacuum at 400 °C using an energy density of 305 mJ/cm^2 and a best fit simulated device, excluding back interface fixed charge.

	Mobility (cm^2/Vs)	V_T (V)	S (V/dec)	I_{max}	I_{min}
Simulated	160	1.65	.60	$9.96x10^{-6}$	$1.12x10^{-14}$
Experiment	151	1.16	.73	$1.02x10^{-5}$	$5.0x10^{-13}$

As seen in the table and looking at figure 3-11, even though most device characteristics match fairly well, the transfer functions are noticeably different. The leakage current of the simulated device, in particular, drops to lower values and climbs more quickly as the gate voltage becomes more negative. In this voltage range (less than V_T), accurate fitting to real devices is difficult due to the limitations of the physical models employed in the program, as discussed previously.

To achieve a better fit, the properties of the barrier layer/poly-Si back interface must be considered. In particular, the quantity of fixed oxide charge (Q_{BIT}) affects the off state characteristics strongly. Figure 3-12 shows the I_D-V_G relationship, as both a linear and a log plot, for the same device from figure 3-11 with a best fit simulated 5 μm device, including fixed oxide, back interface charge.



(a)
Experimental
Simulated w/ Q_{BIT}=7x10^{11}
Drain Current
Gate Bias (V)
1.0x10^{-5}
8.0x10^{-6}
6.0x10^{-6}
4.0x10^{-6}
2.0x10^{-6}
0.0
-20
-15
-10
-5
0
5
10
15
20

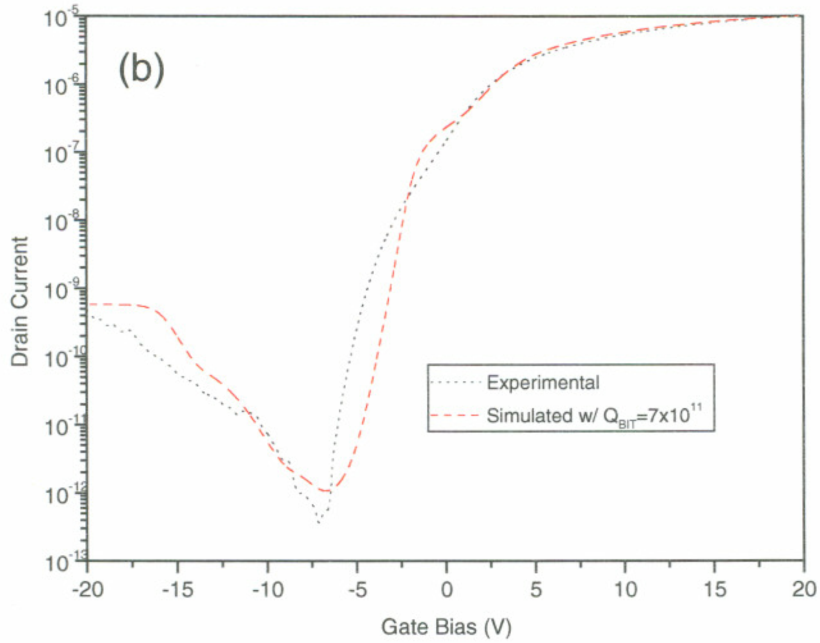


Figure 3-12: Transfer characteristics for a simulated poly-Si TFT with a 5 μm channel length and an actual device laser annealed at 400 °C in vacuum using 305 mJ/cm². For the simulation, backside poly-Si/barrier layer interface fixed charge was included. Part (a) is shown on a linear-linear plot and part (b) is shown on a log-linear plot.

In this case, a good match has been achieved over the entire gate voltage range. The other values used in the simulation are listed below:

$N_{TA}=N_{TD}=1x10^{19}$ cm^{-3}	$s_n=s_p=1x10^{11}$ cm/s
$N_{GA}=N_{GD}=3x10^{18}$ cm^{-3}	$R_S=R_D=2x10^{3}$ ohms
$Q_{it}=0$	$Q_{BIT}=7x10^{11}$ cm^{-2}

A comparison of the performance criteria is shown in table 3-6.

Table 3-6: Device characteristics of an actual poly-Si TFT laser annealed in vacuum at 400 °C using 305 mJ/cm^2 and a best fit simulated device, including back interface fixed charge.

	Mobility (cm^2/Vs)	V_T(V)	S (V/dec)	I_{max}	I_{min}
Simulated	159	1.18	.70	1.01x10^{-5}	9.33x10^{-13}
Experiment	151	1.16	.73	1.02x10^{-5}	5.0x10^{-13}

Again, excellent results have been achieved.

Q_{BIT} influences the device characteristics in several ways, as shown in figure 3-13.

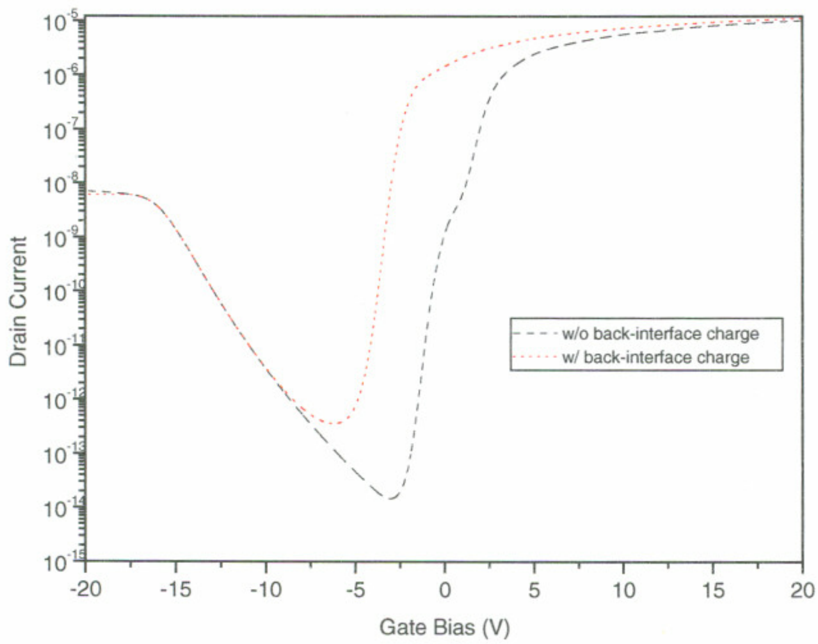


Figure 3-13: Transfer characteristics for 2 simulated 5 μm devices, one with backside poly-Si/barrier layer interface trapped charge, and one without.

For one, the gate voltage which minimizes the drain current is shifted lower, along with the threshold voltage. In addition, the magnitude of the leakage current is increased.

With an abundance of positive charge at the back interface, depleting the entire thickness of the poly-Si active region is more difficult. Also, the subthreshold swing is affected. With an increase in Q_{BIT}, the devices turned on more slowly, and thus S increased.

3.4 Results from Device Characterization

3.4.1 Initial Measurements

Three important parameters affecting all devices were the lateral diffusion of dopants into the channel, the channel series resistance and the contact sheet resistance. By plotting the source-drain resistance for V_{DS}=.1V as a function of mask length for different gate voltages, the contact series resistance (R_{ser}) and the true channel length ($L=L_{mask}-\delta L$) were determined, as in figure 3-14, using a standard procedure [44].

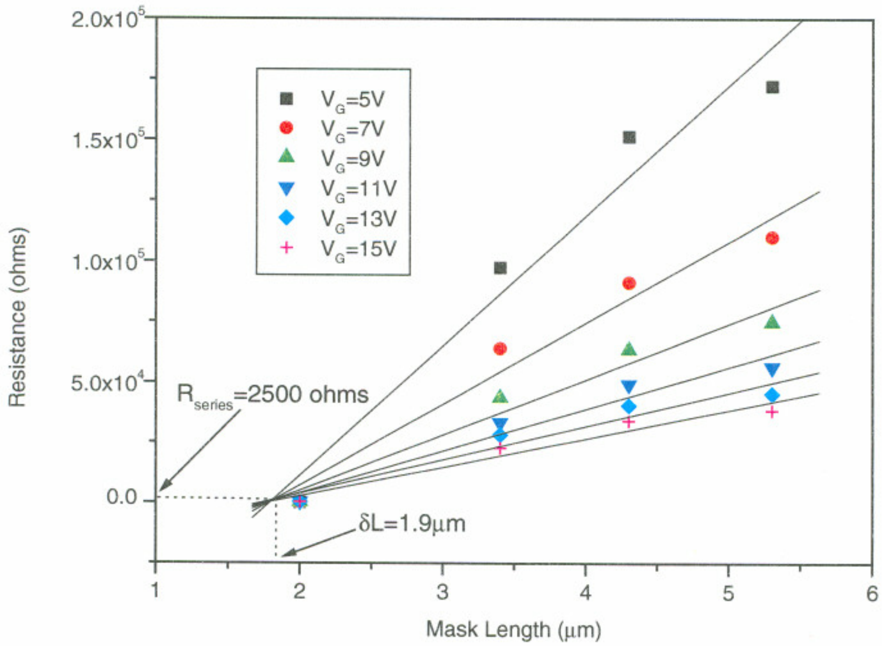


Figure 3-14: Channel resistance as a function of mask length for different gate voltages, where V_{DS}=0.1V. The x-coordinate of the intercept point determines the correction to the channel length and the y-coordinate of the intercept point determines the series resistance.

From this, it was determined that $\delta L \approx 1.9$ μm and $R_{ser} \approx 2500$ Ω. The correction to the mask length was taken into account when computing the field effect mobility, and came about due to dopant segregation (side diffusion) from the source and drain, after implantation, through subsequent heating cycles. Importantly, the series resistance was well within acceptable parameters. As a measure of the effectiveness of dopant activation, a van der Pauw structure was used to determine the contact sheet resistance. Our standard activation procedure lead to a sheet resistance of approximately 650 Ω/sq., which was, once again, adequate for our purposes.

3.4.2 Effect of Energy Density on Poly-Si TFT Performance

As mentioned in section 2.3.2, laser crystallized poly-Si films can be classified into one of three regimes, depending on the laser energy density used during annealing:

R(I) stratified film corresponding to a 'low' energy density

R(II) large grain growth corresponding to an intermediate energy density

R(III) bi-modal grain growth, associated with a 'high' energy density

Because R(I) and R(III) present obviously undesirable qualities, including a small grain size in R(I) and gross non-uniformities in R(III), the study was concentrated on R(II). This was true whenever devices were fabricated, irrespective of which laser annealing parameter was being examined.

Table 3-7 displays the important device parameters, along with the average grain sizes, for samples scanned one time at different energy densities.

Table 3-7: Average device parameters and grain sizes (GS) for poly-Si TFTs made from single scan processes, at different energy densities. Wafers were laser annealed in vacuum, with a substrate temperature of 400 °C.

Wafer	Energy Density (mJ/cm^2)	GS (nm)	Mobility (cm^2/Vs)	V_T (V)	Leakage Current (A)	Log (I_{On}/I_{Off})	S (V/dec)
01-1	275	90	95	2.36	1.21×10^{-12}	6.67	0.90
01-2	305	330	151	1.16	8.00×10^{-13}	7.14	0.73
01-3	335	540	217	0.53	1.90×10^{-13}	7.96	0.65

The corresponding transfer curves (I_D-V_G) are shown in figure 3-15.

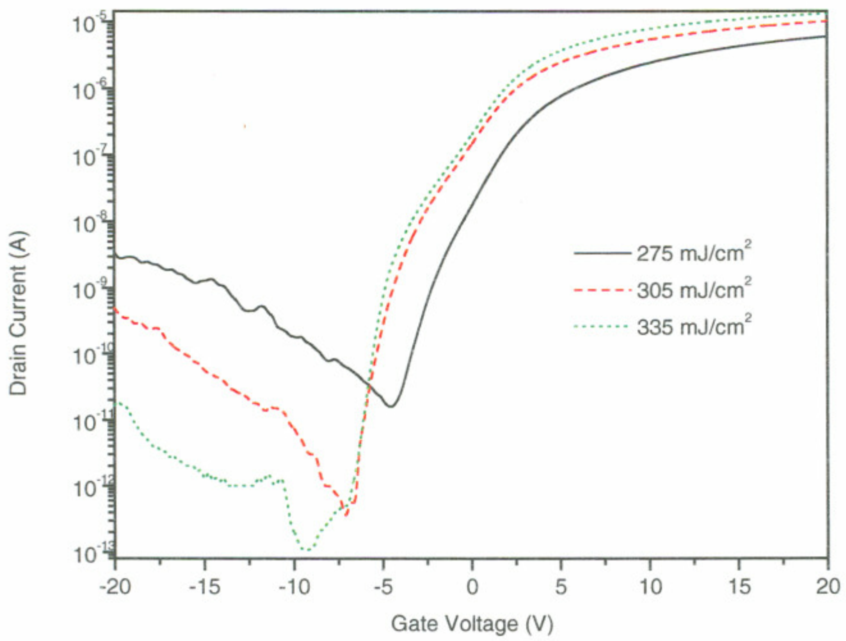


Figure 3-15: Transfer characteristics for poly-Si TFTs laser annealed using different energy densities, at 400 °C in vacuum.

For these samples, there was a steady improvement in all the pertinent characteristics as the average grain size increased with the laser energy density, within the specified range. This agrees with work done by others[45]. As mentioned previously, large grains reduce the number of dangling bonds and thus defects in the poly-Si layer. In our ATLAS model, this corresponds to a reduction in the density of deep trapping states, N_{GA} and N_{GD}. Hence, larger grains should

a) improve the mobility because of fewer scattering centers to slow the carriers
b) improve the subthreshold slope and threshold voltage because of a lower number of trap states to fill as the Fermi level moves across the bandgap towards the conduction band
c) reduce the leakage current because of a reduction in trap assisted thermionic emission

Given this, the overall improvement in all the measured characteristics was to be expected.

However, the improvement in average characteristics was also accompanied by greater variability, as shown in figure 3-16, using the field effect mobility as an example.

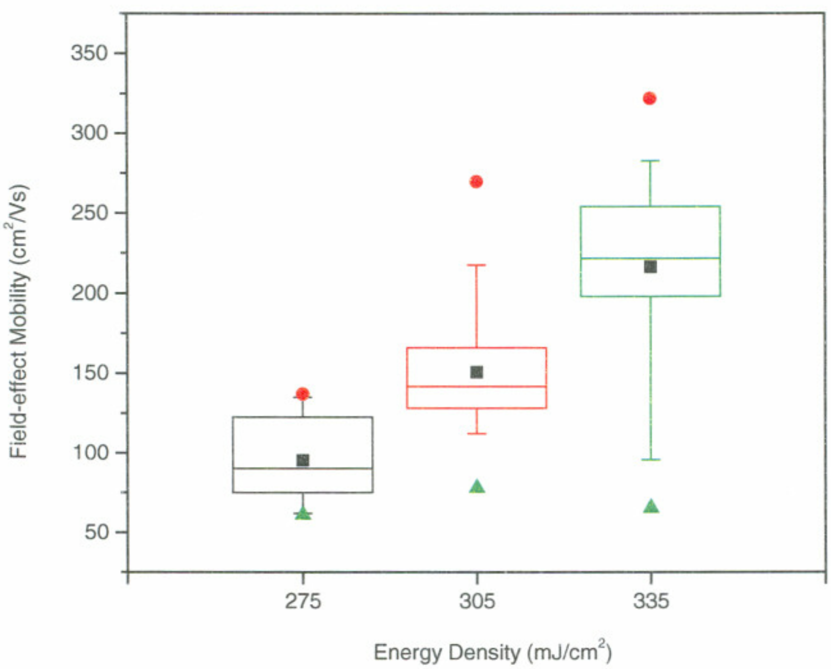


Figure 3-16: Field-effect mobility as a function of laser energy density for poly-Si TFTs. The dot in the center of the box represents the mean and the solid line is for the median. The box itself shows the 25% to 75% data range and the error bars include the 5% to 95% range. Also shown are the maximum and minimum values.

This was anticipated to some degree because, as mentioned in section 2.3.2, the spread in grain size increased at higher energy densities. Also, as the dimensions of the grains approach the channel length, the *relative* number of grain boundaries within the channel can vary significantly from device to device. For example, one device may have two grain boundaries obstructing current flow while another may have three. Due to the strong interaction between current carriers and grain boundaries, variations in device performance would be expected. This degradation in uniformity was troubling and presented an undesirable trade-off with performance.

3.4.3 Effect of Multiple Passes on Poly-Si TFT Performance

The goal of many researchers optimizing a poly-Si laser annealing process is to maximize the grain size of the film because, in most cases, larger grains lead to better device characteristics[45]. Two methods to create large grains by ELA are application of a single scan (single pass) with an energy density which maximizes the average grain size or application of multiple scans (multiple passes) using a lower energy density. For single scans, the creation of very large grains requires a near complete melting of the irradiated area, down to the substrate, as in R(II). However, as discussed previously, even with a 96% overlap, the resultant poly-Si layer typically has a wide distribution of grain sizes due to the inherent pulse to pulse variations associated with excimer lasers[46,47]. If the energy density of a particular pulse is high enough to melt the film entirely, the reduction in the number of nucleation sites can lead to the creation of small crystallites through homogenous nucleation of the molten layer after it has become significantly super-cooled[27]. Multiple scans avoid this problem by increasing the grain size gradually. In so doing, large grains are formed as grains from previous scans conglomerate. What is unclear though is how the corresponding TFT performance will compare for a single scan and multiple scan process.

In this investigation, the characteristics of poly-Si TFTs annealed by a multi-scan ELA process were examined. The impetus was to try and improve the average device characteristics while maintaining uniformity. In a multi-scan process, as it was practiced, some or all of the wafer was scanned as many as eight times at the same energy density. Devices were then fabricated using our standard procedure. Although the use of multiple scans to produce large grains in poly-Si material has been previously studied[28,47], the effect on device performance is not fully understood. TFTs were fabricated using laser crystallized poly-Si at conditions identified and optimized in our materials work, presented in section 2.3.6. Devices were characterized extensively and it was found that the grain size itself was not the only attribute determining device performance, especially for multi-scan ELA. The quality of the grains is a sensitive function of the annealing conditions, and under certain circumstances, advantages derived from larger grains can be effectively overtaken by an increasing number of intra-grain defects and interface trap states, resulting in poorer transistor performance.

Characteristics for devices formed with a multi-scan process are shown in table 3-8, and figure 3-17 shows typical transfer curves.

Table 3-8: Average device parameters and grain sizes (GS) for poly-Si TFTs made with one or more scans at 305 mJ/cm^2. Wafer were laser annealed in vacuum, with a substrate temperature of 400 °C.

# of Scans	Energy Density (mJ/cm^2)	GS (nm)	Mobility (cm^2/Vs)	V_T (V)	Leakage Current (A)	Log (I_{On}/I_{Off})	S (V/dec)
1	305	330	151	1.16	8.00×10^{-13}	7.14	0.73
2	305	390	179	0.90	8.25×10^{-13}	7.08	0.79
4	305	500	194	-0.04	3.02×10^{-12}	6.61	1.05
8	305	600	212	-0.80	2.46×10^{-11}	5.72	1.68

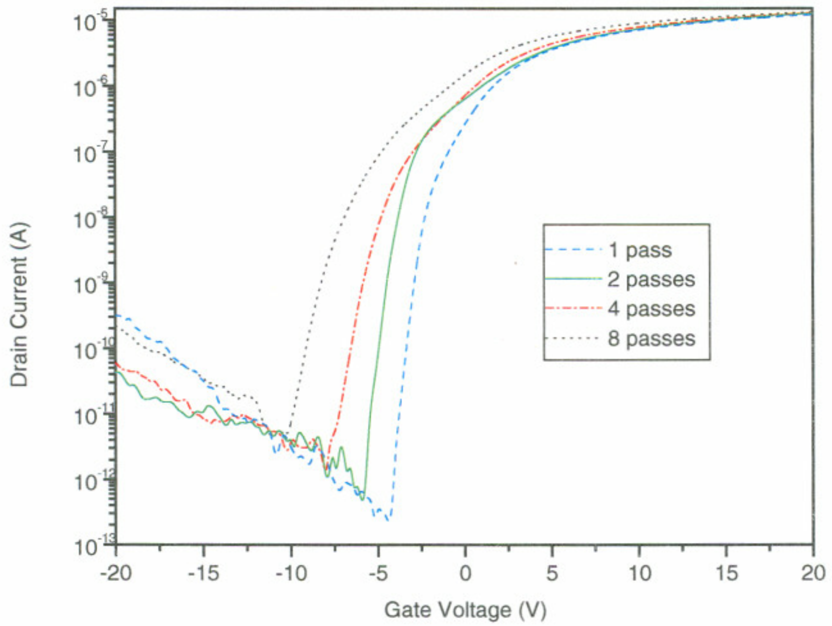


Figure 3-17: Transfer characteristics for devices made using 1, 2, 4, or 8 passes at 400 °C in vacuum. The laser energy density was maintained at 305 mJ/cm^2.

In figure 3-18, a box plot of field-effect mobility as a function of the number of scans is shown.

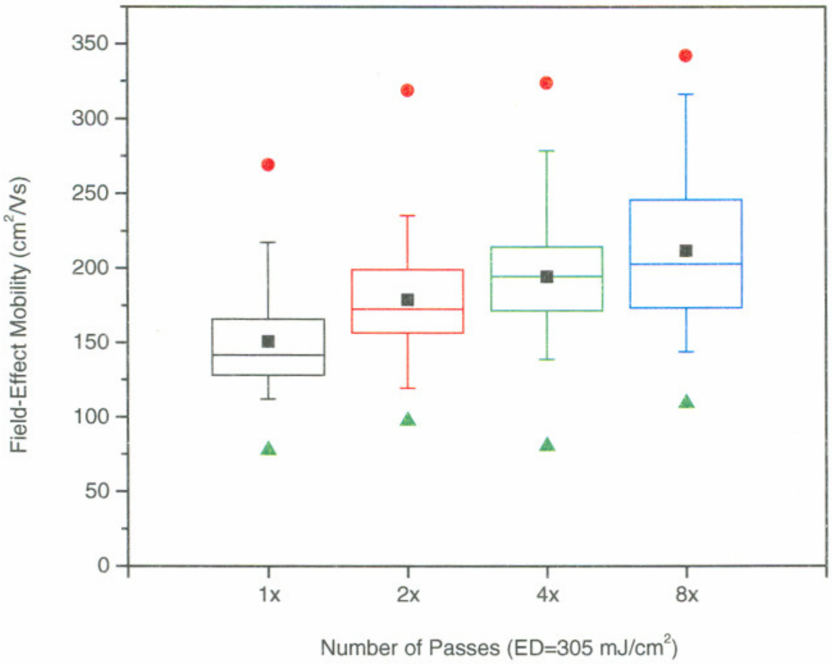


Figure 3-18: Field-effect mobility as a function of the number of scans using 305 mJ/cm^2 in vacuum for poly-Si TFTs. The dot in the center of the box represents the mean and the solid line is for the median. The box itself shows the 25% to 75% data range and the error bars include the 5% to 95% range. Also shown are the maximum and minimum values.

As seen in this figure, in contrast to the single scan case, the average field-effect mobility improved while uniformity was maintained. This is a distinct advantage of this technique. However, again in contrast to the single-scan case, the on-off ratio, subthreshold swing and leakage current degraded markedly as shown in table 3-8, despite the increase in average grain size. Moreover, the threshold voltage became decidedly negative. The relationship between mobility and grain size is shown in figure 3-19, with the field effect mobility steadily increasing as the average grain size grew.

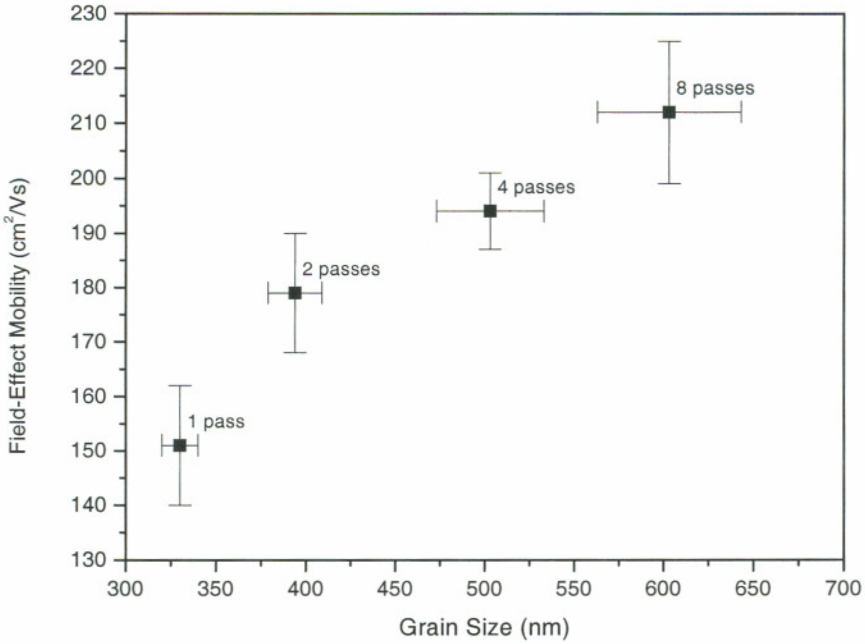


Figure 3-19: Variation in field effect mobility with grain size for poly-Si TFTs scanned one or more times at 305 mJ/cm^2 in vacuum at 400 °C.

Importantly though, comparing the average mobility of samples annealed at 305 mJ/cm^2 (8 passes) and 335 mJ/cm^2 (1 pass), despite the larger grain size in the former case, the device performance was poorer. The reason for this effect was not immediately clear.

Through extensive materials analysis, as presented in section 2.3.6, it was determined that even though the grain size in the poly-Si film was increasing with each scan, artifacts from previous scans remained in the interior of the newly formed grains. In a multi-scan process, large grains develop as grains from previous scans conglomerate, often without complete elimination of the original grain boundaries. The original grain boundaries can act as intra-grain defects and thus hinder device performance. Residual intra-grain sub-boundaries from a sample scanned 8 times can be seen by atomic force microscopy (AFM), as shown in figure 3-20, reproduced from figure 2-22 (c).

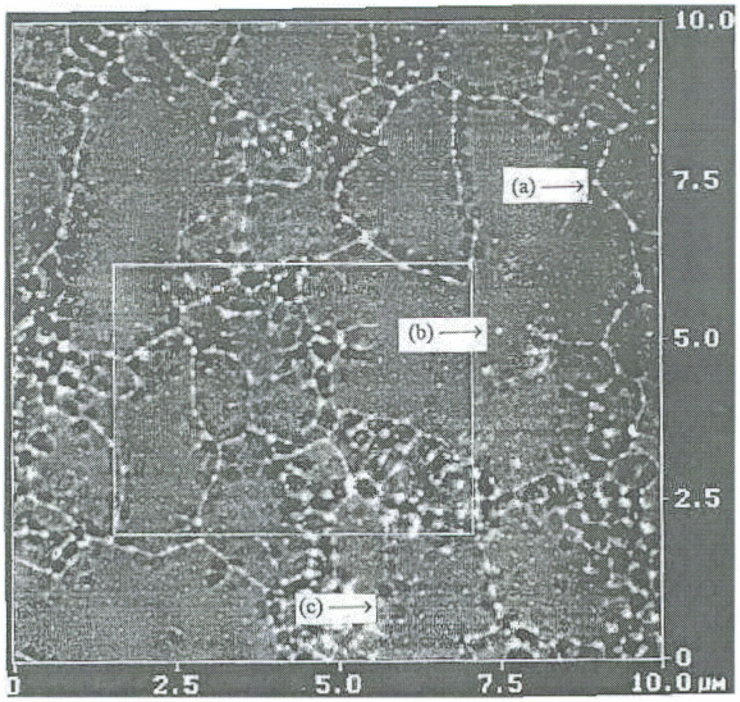


Figure 3-20: AFM image of ELA poly-Si showing large grains conglomerated from smaller grains in a sample scanned eight times at 305 mJ/cm2. Sub-boundaries and point-like defects are visible throughout the grains. Arrow (a) indicates a primary grain boundary. Arrow (b) points to a point-like defect. Arrow (c) is showing sub-boundaries formed from partially conglomerated grains. The measured area was 10 µm x10 µm.

The same sort of intra-grain defects can be seen in the TEM image of figure 3-21, reproduced from figure 2-21 (c).

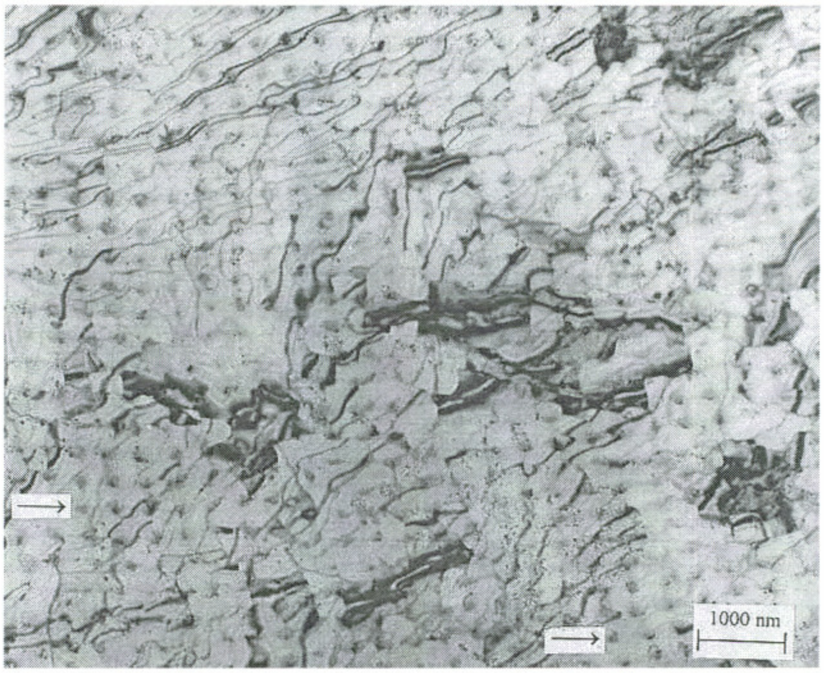


Figure 3-21: TEM image of ELA poly-Si showing large grains of a sample scanned eight times at 305 mJ/cm^2. Defects resulting from grains conglomerated from previous scans are evident throughout the image, as both sub-boundaries and point-like defects. The point-like defects often form in a regular array, as in the figure. The arrows indicate two such defects.

Previous studies of poly-Si TFTs fabricated with SPC suggest the dominance of intra-grain defects over grain boundary defects with respect to their effect on carrier transport in the channel[48,49]. A recent work, however, points out that for sufficiently low intra-grain defect density, the carrier mobility can become grain boundary trap limited[50]. Typically, this is the case for ELA poly-Si material, where the intra-grain defect density tends to be very low, resulting in fast carrier transport within the grains. Our simulations, in section 3.3.3, further suggest that both the deep and tail states can influence the mobility significantly.

To investigate the mobility variations as a function of the annealing conditions, the method proposed by Levinson et al. was used to evaluate the trap density at the grain boundaries[51]. Levinson et al. modeled the poly-Si film as a linear chain of identical crystallites, with grain boundaries of negligible thickness containing a concentration of traps located at a single energy level. Based on this formulation, the potential barrier height at the grain boundary is given by equation (3-17):

$$E_B = \frac{q^3 \times N_t^{\,2} \times d_{ch}}{8 \times C_{OX} \times V_G \times \varepsilon_{Si}} \tag{3-17}$$

where q is the electronic charge, N_t is the grain boundary trap density, d_{ch} is the induced channel thickness (assumed to be 10 nm), ε_{Si} is the dielectric constant of Si, C_{OX} is the capacitance of the gate insulator, and V_G is the applied gate voltage. Levinson et al. assumed a grain boundary mobility of the form shown in eq. (3-18):

$$\mu_{GB} = \mu_0 \times \exp\left(- E_B / kT \right) \tag{3-18}$$

where k is the Boltzmann constant, T is the absolute temperature and μ_0 is a pre-factor. Thus the total effective mobility in the channel (μ_{eff}), being a function of scattering occurring within the grains and at the grain boundaries, can be expressed as:

$$1/\mu_{eff} = 1/\mu_G + 1/\mu_{GB} \tag{3-19}$$

where μ_G is the intra-grain mobility and μ_{GB} is the mobility at the grain boundary.

Based on Levinson's model, the grain boundary trap density (N_t) was calculated from the slope of $\ln(I_D/V_G)$ vs. $(1/V_G)$, for V_{DS}=0.1V. Furthermore, the intercept of this line was used to calculate the parameter μ_0 in eq. (3-18). A plot of the field effect mobility versus trap density at the grain boundary is shown in figure 3-22.

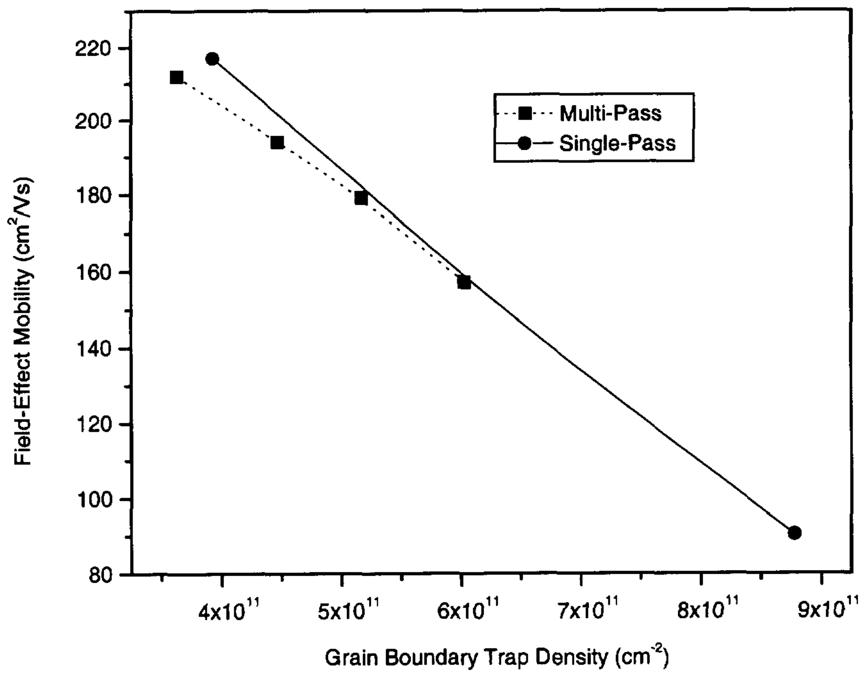


Figure 3-22: Field-effect mobility as a function of grain boundary trap density, as derived from the Levinson model, for devices made from single and multi-scan processes.

It is evident from the figure, that as a general trend, the mobility and trap density were inversely related. Notice, however, the distinction between single-pass and multi-pass ELA. For the same trap density, films annealed by multi-pass ELA, with more than 4 passes, demonstrated a lower mobility than films annealed by single pass ELA at a higher energy density. For example, the average mobility of the devices annealed at 335 mJ/cm^2 (1 pass) was higher than the average mobility of the film annealed at 305 mJ/cm^2 (8 passes). This is a very interesting result, in light of the fact that the latter film had a lower grain boundary defect density *and* a larger average grain size. As suggested above, a multi-pass ELA process increases the defect density within the grains. Since a higher number of defects decreases the mobility along the length of the grain, and because the grains were becoming larger, it is likely that the transport of carriers became intra-grain limited as the film was subjected to more passes.

To assess the validity of this hypothesis, the magnitude of the grain boundary potential barrier height was evaluated at the value of the gate voltage corresponding to the peak in the transconductance, for $V_{DS} = 0.1V$. In figure 3-23, the TFT mobility is plotted as a function of the barrier height.

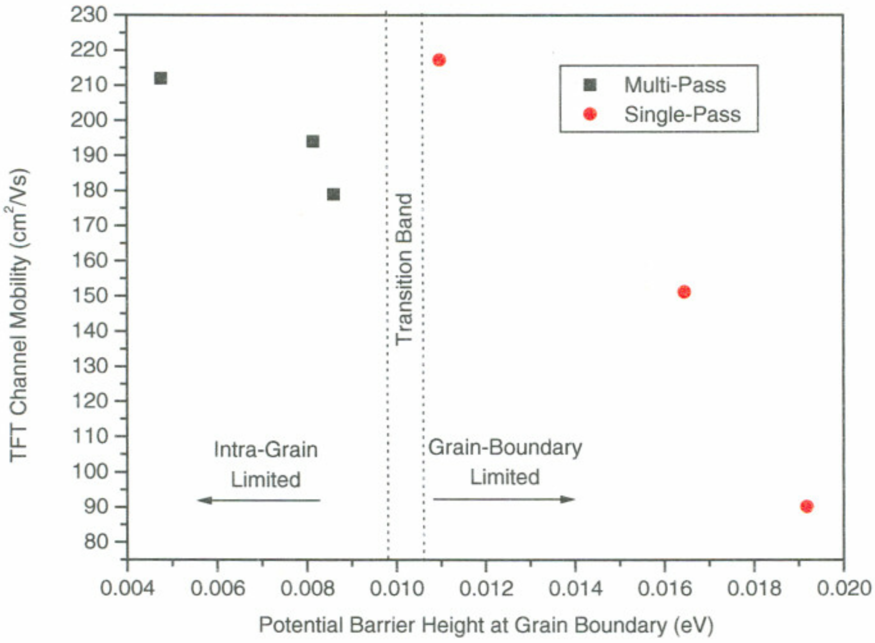


Figure 3-23: TFT channel mobility as a function of the potential barrier height at the grain boundary for devices made from single and multi-scan processes. Samples in the intra-grain limited regime (squares) were scanned, from right to left, 2 times, 4 times and 8 times respectively at 305 mJ/cm^2. The samples in the grain boundary limited regime (circles) were scanned 1 time at, from right to left, 275, 305 and 335 mJ/cm^2 respectively. Also shown is the transition band separating the regimes where mobility is limited by intra-grain or grain boundary defects.

It is evident that even though the grain boundary barrier height was significantly decreased for the case of the multi-pass process, the TFT mobility was not correspondingly increased. Since lower grain boundary barriers strengthen the influence of the intra-grain defects, the conduction was intra-grain limited in this case, while for high barrier heights, it was grain boundary limited. Based on our data, a transition band, separating these two regimes was identified in the range of 0.0097-0.0107 eV. This range is close to the value for the potential barrier height reported by other authors, for a similar transition[48]. This previous study concluded that grain boundaries dominated the carrier transport in the channel when the grain boundary potential barrier height was larger than 0.0124 eV.

Using the experimentally measured TFT mobility and the calculated grain boundary mobility from eq. (3-18), an order of magnitude calculation was made of the ratio μ_G/μ_{GB}, using eq. (3-19). Figure 3-24 plots this ratio as a function of the potential barrier height at the grain boundary. As expected, in the intra-grain limited regime, the ratio decreased with decreasing barrier height, confirming the increasing importance of intra-grain defects in the conduction process. An extreme in this regime would be a TFT dominated by intra-grain defects, as from SPC poly-Si.

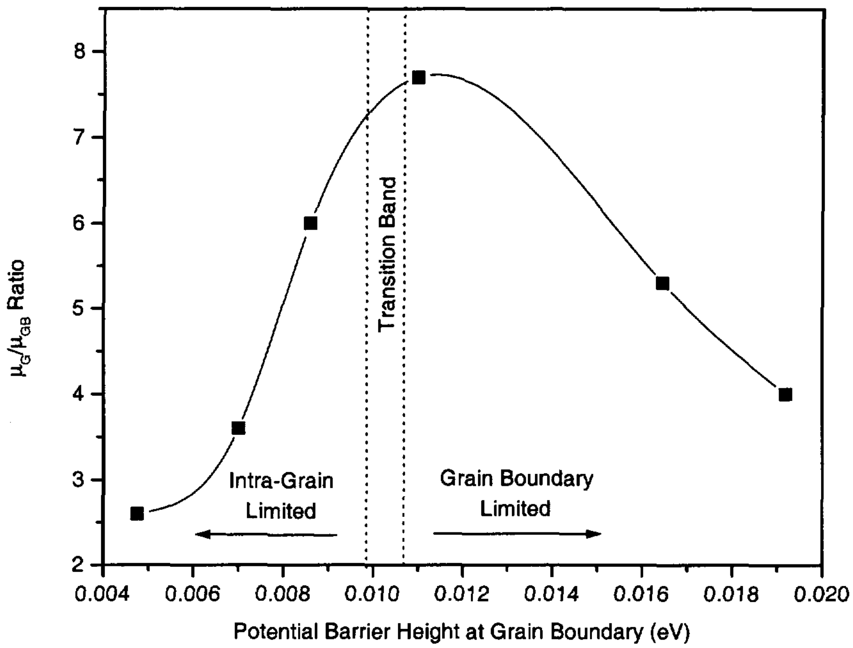


Figure 3-24: Ratio of intra-grain mobility (μ_G) to the grain boundary mobility (μ_{GB}) as a function of the potential barrier height at the grain boundary. Samples in the intra-grain limited regime were scanned, from right to left, 2 times, 4 times and 8 times respectively at 305 mJ/cm^2. The samples in the grain boundary limited regime were scanned 1 time at, from right to left, 275, 305 and 335 mJ/cm^2 respectively. Also shown is the transition band separating the regimes where mobility is limited by intra-grain or grain boundary defects.

At the other extreme, it is anticipated that the barrier height will saturate as the size of the associated depletion regions approach the size of the grains. At this point, the carrier density will be greatly reduced and the field effect mobility will be correspondingly low.

Though the increase in grain size coupled with the increase in intra-grain trap density explains the on-state characteristics of the devices scanned multiple times fairly well, it does not explain why many of the off-state characteristics worsen with each scan. Referring back to table 3-8 and figure 3-17, notice that the average value of the subthreshold swing (S) increased by more than a factor of 2 for the samples scanned 8 times as compared to the samples scanned once. This behavior was unexpected, because in most cases, S improves as the grain size increases and the density of deep trapping states decreases, as shown in table 3-3. Also notice that the leakage current is increased and the gate voltage which minimizes the drain current is shifted to more negative values for the samples scanned multiple times. Referring back to figure 3-13, these same characteristics are evident when the density of back interface fixed oxide charge is increased. This is strong evidence suggesting that, with each scan, damage is being done to the back interface and hence, fixed interfacial charge is accumulating. The interface charge is, in turn, creating problems with the subthreshold characteristics of the devices.

The relationship between the grain boundary trap density and threshold voltage (V_T) is shown in figure 3-25.

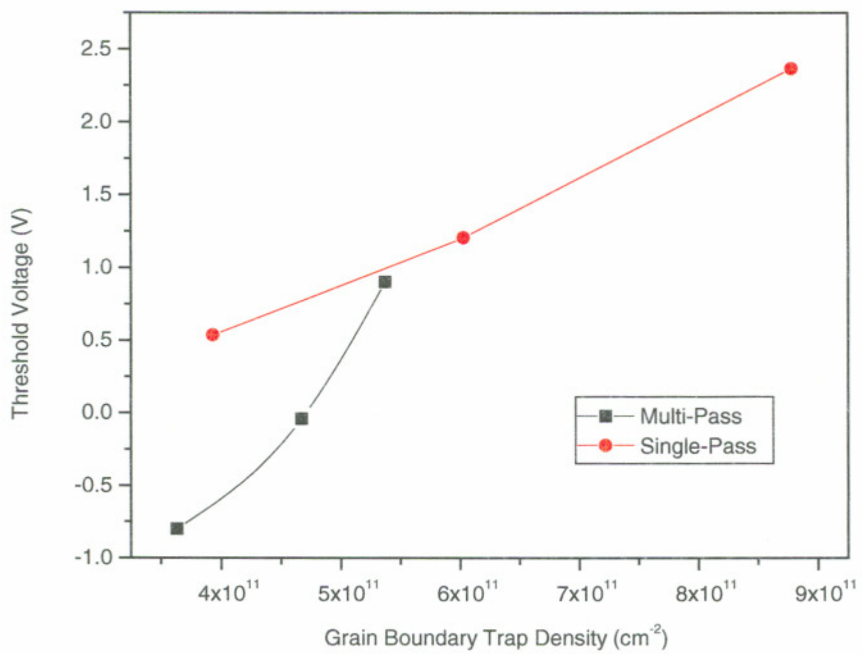


Figure 3-25: Relationship between grain boundary trap density and threshold voltage for poly-Si TFTs made from a single and multi-scan process. Squares represent samples scanned, from right to left, 8 times, 4 times and 2 times respectively at 305 mJ/cm^2. Circles represent samples scanned one time at, from right to left, 335, 305, and 275 mJ/cm^2 respectively.

As a general trend, and in agreement with previous studies, the threshold voltage decreased as the trap density decreased[52]. Notice, however, that the threshold voltage for multi-scans became increasingly negative at a higher rate in relation to the grain boundary trap density than for single scans. In addition, the samples scanned 8 times had an average V_T well below 0 V. These results are consistent with the idea that positive charge accumulated with each scan at the barrier layer/poly-Si interface. As stated in section 3.3.3, this charge shifts the threshold voltage towards more negative values. Also supporting this claim, note that V_T *increased* following hydrogenation of the wafer scanned 8 times, for devices with negative threshold values. After measuring 15 TFTs where the average V_T was equal to –2.16 V before hydrogenation, it rose to –1.52 V after. In most cases, because hydrogen reduces the number of dangling bonds, the threshold voltage *decreases* for n-channel devices following hydrogenation[48,53]. However, in this case, a reduction in the density of the fixed interface charge increased V_T.

By making I_D-V_G measurements at various temperatures, the source-drain current activation energy of each annealing condition, as a function of gate voltage was also determined for the same devices as in figure 3-17, and is shown in figure 3-26.

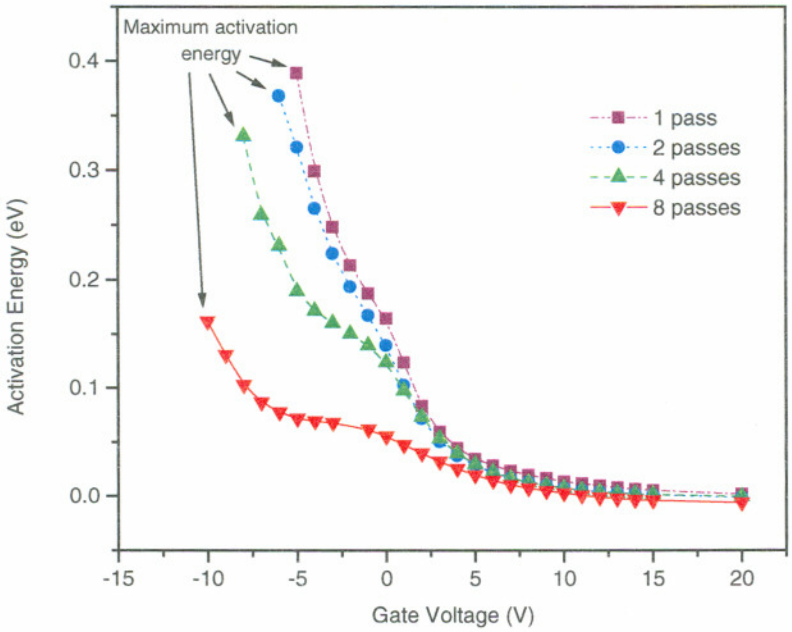


Figure 3-26: Source-drain current activation energy as a function of applied gate voltage for samples scanned 1, 2, 4 or 8 times in vacuum at 400 °C. The laser energy density was maintained at 305 mJ/cm^2. The maximum activation energy for each condition is also indicated.

For each annealing condition, a range of activation energies is shown, up to the maximum value. With lower gate voltages (more negative), the activation energy begins to decrease due to field-enhanced carrier emission from trap sites[54]. Therefore, the largest value in each case marks the beginning of the leakage current regime. The activation energy is, in essence, a measure of how sensitively the current varies with temperature[55]. Due to the different components affecting I_D (drift, diffusion and leakage), depending on the gate voltage, the activation energy exhibits the corresponding temperature behavior. Important to the present discussion, in the leakage current regime, the activation energy is to first order, a measure of the proximity of the Fermi level to the conduction band edge. Therefore, the steady decrease in the activation energy with each scan suggests that the Fermi level is moving progressively closer to the conduction band edge. This can be accounted for by either a growing layer of positive interfacial charge or accumulation of n-type dopant in the channel. The dopant could only come from the source and drain regions, but series resistance measurements have confirmed that this is not the case. It is also possible that incorporated oxygen is acting as a thermal donor, and as the oxygen level increases with each scan, the effect is magnified. However, this same drop in activation energy is not witnessed for TFTs laser annealed in air, thus disaffirming this theory. This leaves positive interfacial charge at the back interface as the likely culprit. The charge would have the effect of drawing electrons into the channel, shifting the Fermi level in the bandgap towards the conduction band, and thus lowering the activation energy.

3.4.4 Effect of Barrier Layer on Poly-Si TFT Performance

As discussed in section 2.3.3, the presence an SiO_2 barrier layer underneath the a-Si during ELA can lead to the formation of larger grains and prevent impurity segregation from the substrate. For these reasons, barrier layers are regularly used[56,57]. Nevertheless, it is important to find out what if any additional effects the barrier layer has on poly-Si TFT performance, and whether the expected benefits from the extra deposition step are realized. Two TFT wafers (03-1 and 03-2) were fabricated similarly, using our standard procedure, with the exception that 03-2 had a 200 nm thick TEOS deposited SiO_2 barrier layer and 03-1 did not. The results from device measurements are shown in table 3-9.

Table 3-9: Average device parameters and grain sizes for poly-Si TFTs made with and without an oxide barrier layer. The polysilicon active layer was crystallized at different energy densities, with a substrate temperature of 400 °C.

Wafer	Energy Density (mJ/cm^2)	Grain Size (nm)	Max Id (μA)	V_T (V)	S (V/dec)	Mobility (cm^2/Vs)	Log (I_{On}/I_{Off})
03-1	260	130	1.87	8.17	0.835	45.9	6.04
No Barrier	290	290	5.08	4.52	0.497	102.3	5.89
	320	400	6.66	3.71	0.449	136.5	6.08
03-2	260	160	2.40	7.10	1.43	54.0	6.07
200 nm SiO_2	290	300	7.53	2.20	0.818	146.9	6.03
barrier	320	680	9.40	1.70	0.773	197.9	6.61

Representative transfer characteristics are shown in figure 3-27.

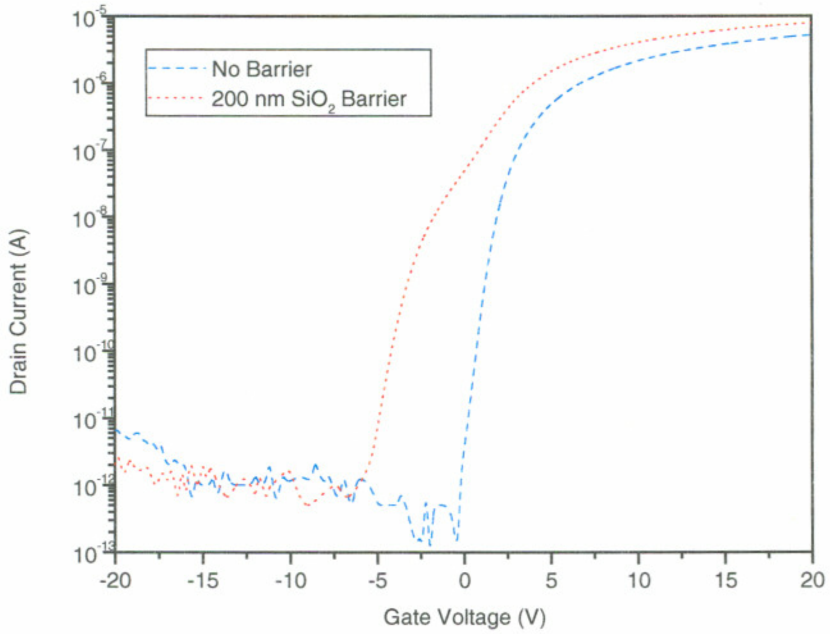


Figure 3-27: Transfer characteristics for devices fabricated with and without a 200 nm thick SiO_2 barrier layer. In each case, the wafers were annealed in vacuum at 400 °C with an energy density of 290 mJ/cm^2.

First of all, notice that the mobility is lower for 03-1 in comparison to 03-2. This may be due, in part, because the grain size is slightly smaller and it may also be due to impurity incorporation from the substrate, as discussed in 2.3.3. Both neutral and charged impurities can increase carrier scattering and hence, lower the mobility. Also notice that the threshold voltage is higher for wafer 03-1. In addition, despite the fact that the grain size is smaller, the subthreshold swing for 03-1 is much lower that 03-2. Looking at figure 27, the characteristics for the device made with a barrier layer is shifted toward negative gate voltages, in comparison to the device made without a barrier layer. These results can be explained by considering the situation at the poly-Si/back side interface. As discussed in section 3.3.2 and presented by other authors[58], backside fixed interface charge degrades the subthreshold swing and decreases the threshold voltage. Our simulations have further shown (see figure 3-13) the kind of shifting shown in figure 3-27, can result from backside fixed interface charge. This suggests that the quartz/poly-Si interface of 03-1 is of a higher quality and less susceptible to fixed interface charge than the TEOS SiO_2/poly-Si interface of wafer 03-2. The presence of fixed charge may be due in part to the plasma cleaning procedure used to prepare the SiO_2 surface before silicon deposition.

3.4.5 Laser Activation of Dopants

To take full advantage of the excimer laser in producing TFTs, processing temperatures above 600 °C should not be utilized, and ultimately, temperatures should not go above 400 °C. This would allow devices to be manufactured on inexpensive, low temperature glass substrates. In our control procedure, a single high temperature step was implemented to simultaneously activate the implanted phosphorous at the source and drain and densify the gate oxide. An alternative to this step would be to use the laser to accomplish both purposes. This could be done by scanning the laser over the wafer after implantation had been carried out, with the gate oxide still in place.

To test the feasibility of this process, quartz substrates were uniformly coated with 100 nm of SiO_2 on top of 50 nm of SPC poly-Si. Phosphorous was then implanted at a dose of 5×10^{15} cm^{-2} and an accelerating voltage of 100 keV. The wafers were scanned using different energy densities, in vacuum at room temperature, and the SiO_2 was subsequently stripped off. The sheet resistance of the resulting material was then measured and compared to the sheet resistance for furnace activated dopant. The results are shown in figure 3-28.

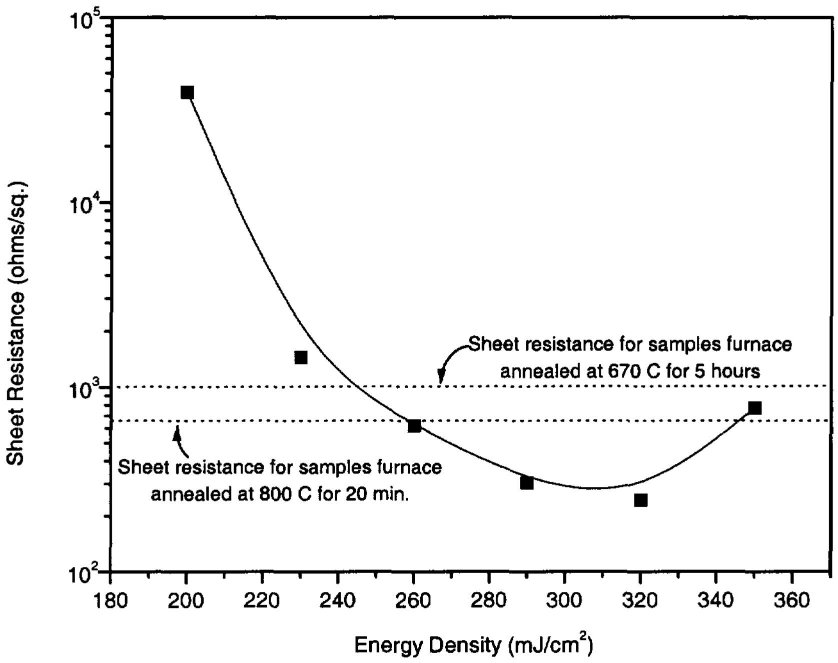


Figure 3-28: Sheet resistance measured with a van der Pauw structure, as a function of laser energy density for dopants activated at room temperature.

The rise in sheet resistance for high energy densities (above 320 mJ/cm^2) was due to ablation of the poly-Si film. As is evident, the sheet resistance for the laser activated material decreased well below the furnace-annealed level, using energy densities at or near 300 mJ/cm^2. Thus, it became possible not only to reduce our maximum processing temperature, but also to improve device performance by lowering the junction series resistance as well.

Using this experiment as a basis, a similar procedure was carried out to produce laser-activated devices. Two wafers were scanned in three sections, using different energy densities, in vacuum at room temperature. The gate oxide was then deposited and patterned. Phosphorous ions were implanted, and the wafers were laser processed once more. One of our concerns in implementing this step was the possibility of oxide deformation, similar to what had been seen when using an SiO_2 AR coating, as discussed in section 2.3.5. It was hoped that because patterning had been done prior to the laser activation, the smaller oxide regions would relax without buckling, as they cooled. Unfortunately though, upon examining one of the wafers after the laser activation was complete, using energy densities which optimized the sheet resistance led to warpage of the gate oxide. This may have been due in part because, after patterning, a portion of the laser pulses passed completely though the quartz substrate and was reflected by poly-Si on the *backside* of the wafer, towards the patterned islands. This idea is supported in that even when using moderate energy densities (around 300 mJ/cm^2) without an oxide coating, some damaged occurred to the patterned poly-Si. However, with our current set-up, the backside poly-Si is necessary so that the lithography tools can locate the wafer. By trying several energy densities, the highest one that did not cause any damage (210 mJ/cm^2) was selected.

The results from those devices are shown in table 3-10, and compared to similarly fabricated devices with furnace activated dopant.

Table 3-10: Average device parameters for poly-Si TFTs made with laser activated or furnace activated dopants. The polysilicon active layer was crystallized using different energy densities (ED), in vacuum at room temperature.

Dopant Activation	**ED (mJ/cm^2)**	**Max I_D (μA)**	**I_D at V_G=-20 V (pA)**	**V_T (V)**	**S (V/dec)**	**Mobility (cm^2/Vs)**	**Log (I_{On}/I_{Off}) V_{DS}=10V**
Furnace 800 °C for 20 min	310	1.79	1.90	9.15	1.485	45.44	6.53
	340	7.57	3236	1.84	0.831	156.17	7.02
	370	9.09	1614	1.19	0.717	195.97	6.59
Laser 210 mJ/cm^2	310	2.37	1.1x10^4	8.05	0.987	58.88	7.14
	340	6.14	2.5x10^4	5.25	0.832	134.43	7.57
	370	8.43	1.6x10^4	4.48	0.890	189.99	7.59

Figure 3-29 shows the transfer characteristics for typical transistors.

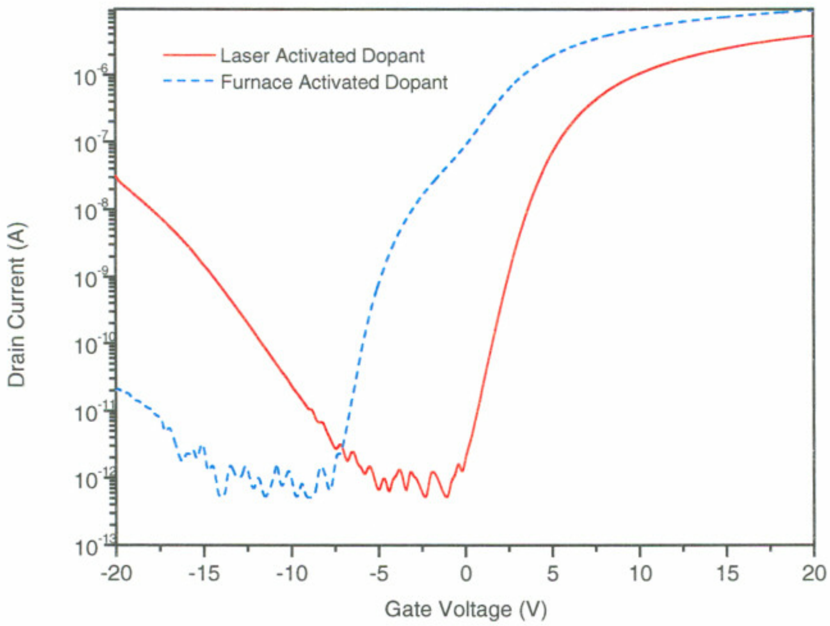


Figure 3-29: Transfer characteristics (with V_{DS}=0.1V) for devices made with dopants activated by furnace (at 800 °C) or with the laser (at 210 mJ/cm^2). The laser annealing took place at room temperature in vacuum.

From the table and figure, the average characteristics for the laser activated transistors were noticeably inferior to their furnace activated counterparts. Because 210 mJ/cm^2 was the maximum energy density that could be used for laser activation, the correspondingly high sheet resistance affected the mobility and drive current, and also the threshold voltage. Even more importantly, the degradation in leakage current at high gate voltages and low drain voltages for the laser activated sample was relatively severe. This was due to an excessively large gate leakage current (in the high nA range versus pA range for furnace densification) occurring presumably because the gate oxide was ineffectively densified. This effect washed out at higher drain-source voltages, when other leakage current generating mechanisms became predominant. In fact, the laser activated devices had one of the smallest average minimum leakage currents and one of the best average on/off ratios of any condition at V_{DS}=10 V.

3.4.6 Effect of Substrate Heating on Poly-Si TFT Performance

In reference to the crystallization of a-Si using an excimer laser, for our setup, the most time consuming step often carried out is the heating of the substrate. In most cases, substrates are heated to temperatures between 400-500 °C, and this step alone could take upwards of 10 minutes before thermal equilibrium was achieved. As mentioned in section 2.3.7, our materials work demonstrated that there was no noticeable improvement in grain size or grain structure for samples annealed using substrate heating. Rather, what occurred was a simple shifting of the energy densities where large grain growth initiated towards larger energy densities for lower temperatures. This being the case, it was prudent to follow through with the investigation and see whether device characteristics followed this same relationship.

Energy densities were chosen which optimized the poly-Si grain size for samples laser annealed at 400 °C and RT. Device fabrication then proceeded identically. The results are shown in table 3-11.

Table 3-11: Average device parameters and grain sizes (GS) for poly-Si TFTs laser annealed in vacuum, with different energy densities (ED), at 400 °C or room temperature (RT).

Annealing Condition	ED	GS (nm)	Max I_D (μA)	I_D at V_G=-20 (pA)	V_T (V)	S (V/dec)	Mobility (cm^2/Vs)
Vacuum	260	160	2.40	2.375	7.1	1.433	53.9
400 °C	290	300	7.53	9.184	2.2	.818	146.9
	320	680	9.40	4.000	1.7	.773	197.9
Vacuum	310	150	1.79	1.896	9.1	1.485	45.4
RT	340	380	7.57	3236	1.8	.831	156.1
	370	680	9.09	1614	1.1	.717	195.9

Somewhat unsurprisingly, the device characteristics were nearly identical, including the mobility, subthreshold swing, and the threshold voltage. The only characteristic which differed significantly was the leakage current at large negative gate voltages, which was greater for devices laser annealed at room temperature. This suggests that some sort of field emission process was occurring more frequently in the RT samples, pointing to the presence of a greater number of active trap sites, though this is still unclear.

3.4.7 Effect of Annealing Ambient on Poly-Si TFT Performance

The choice of annealing medium, in conjunction with excimer laser annealing, seems to be quite important from the point of view of performance and process simplicity. For example, it is highly desirable to anneal in air, and eliminate the vacuum system altogether, without compromising the quality of the polysilicon film. However, there are some reports in the literature that indicate certain detrimental effects of ELA in air on the polysilicon structure[18]. To the best of our knowledge, only scattered results exist on the effect of the annealing ambient on polysilicon film structure and corresponding TFT characteristics[59,19]. Thus, in this section these issues were addressed by performing a careful and systematic evaluation of the structural and electrical properties of thin polysilicon films that have been annealed by ELA in various environments.

Prior to laser annealing, the sample chamber was pumped down to approximately 1 mTorr. The vacuum was valved off, and another valve was opened, letting in either air or purified argon, nitrogen or helium. The gas flow was then shut off, and the a-Si was crystallized with the excimer laser. Device fabrication then proceeded, as with the control condition.

Table 3-12 summarizes the key characteristics of typical TFT devices, fabricated with polysilicon films that were laser-annealed in the various environments investigated in this study.

Table 3-12: Characteristics of TFTs fabricated by ELA process in various annealing media. In all cases, the substrate temperature during ELA was 400 °C.

Ambient	ED (mJ/cm^2)	GS (nm)	Mobility (cm^2/Vs)	V_T (V)	S (V/dec)	Log (I_{on}/I_{off})
Vacuum	335	650	216.4	0.53	0.65	7.96
Argon	270	450	204.3	0.55	0.56	8.15
Nitrogen	270	450	182.7	0.69	0.63	7.76
Helium	270	450	182.4	1.17	0.79	7.40
Air	280	550	134.8	2.32	1.08	5.66

The characteristics listed in table 3-12 were obtained from as-fabricated TFTs, prior to any H_2-plasma passivation process. Figure 3-30 shows the field-effect mobility distribution for the conditions listed in table 3-12, as a function of the annealing ambient.

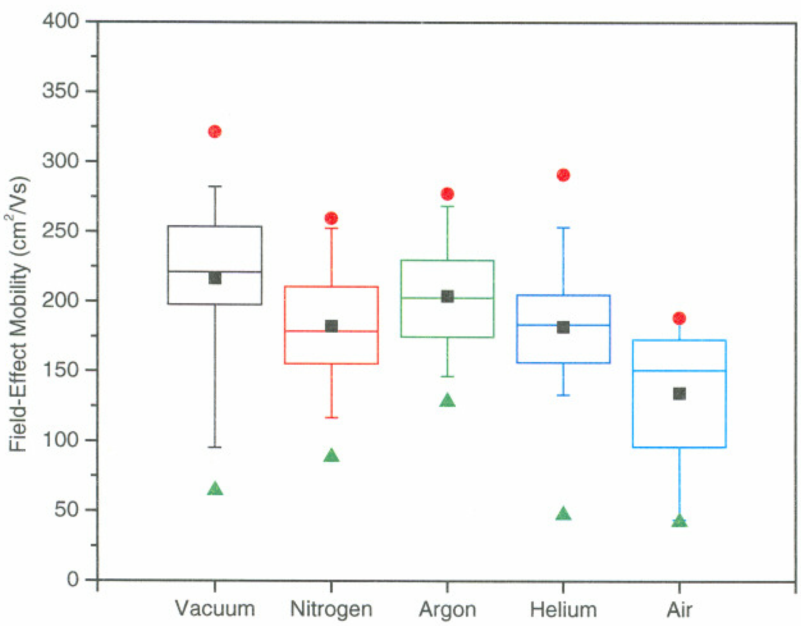
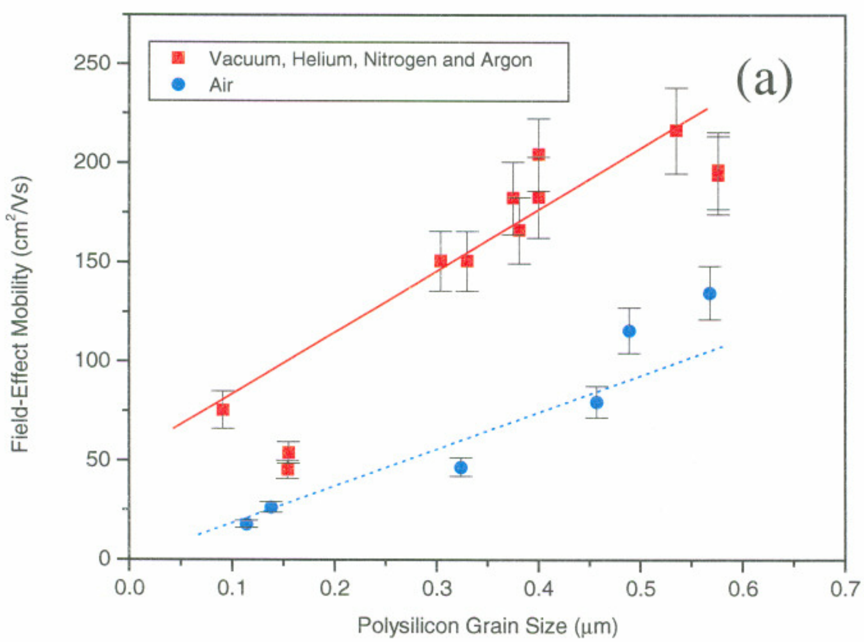
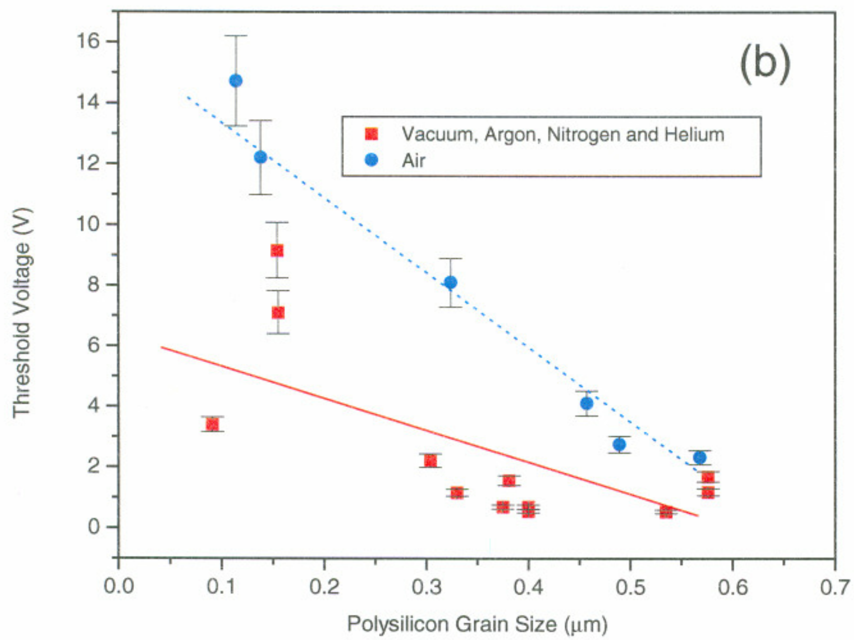


Figure 3-30: Field-effect mobility distribution for samples annealed in different ambients. The dot in the center of the box represents the mean and the solid line is for the median. The box itself shows the 25% to 75% data range and the error bars include the 5% to 95% range. Also shown are the maximum and minimum values.

Taking the field-effect mobility as an example, the choice of annealing ambient is shown to affect the transistor performance in two main ways: (1) the average mobility value was found to decrease when air was used for the ELA process. On the other hand, differences among vacuum and inert gas ambient seem to be statistically insignificant. (2) The optimal level of energy density, that maximized mobility, was found to decrease when inert gas or air is used, instead of vacuum, for the ELA process (i.e. 290 mJ/cm² for inert gas instead of 335 mJ/cm² for vacuum). This observation is consistent with the data reported in section 2.3.4, regarding the reduction in the optimum energy density (that maximizes grain size) during laser anneal in an inert ambient.

Even though, in selecting the energy densities, care was taken to produce polysilicon films with *similar* grain size, the offset in the average grain size of films produced in the various annealing environments could not be completely eliminated (see table 3-12). In an effort to de-couple the effect of the grain size from a possible "pure" ambient effect, the TFT performance attributes (field-effect mobility and threshold voltage) were plotted in figure 3-31 (a,b) as a function of the polysilicon film's grain size and the relevant annealing ambient.





Figures 3-31: Polysilicon TFT characteristics as a function of the polysilicon film grain size and annealing ambient: (a) field-effect mobility, (b) threshold voltage.

As expected, the data favored higher mobility and lower threshold voltage as the grain size of the polysilicon film increased. Notice, however, the offset between films annealed in vacuum and films annealed in air, in both mobility values [fig. 3-31(a)] and threshold voltage [fig. 3-31(b)]. Moreover, notice the characteristics of TFTs annealed in inert gas ambient: they tend to align very well with the trend line of the vacuum-annealed TFTs. These results elucidate the important conclusion that, for a given grain size, TFTs made of polysilicon films formed by ELA in air demonstrate inferior characteristics to those of TFT annealed in vacuum *or* inert gas. As a result, if vacuum is not an option, the presence of an inert gas seems necessary for the ELA process to be effective in producing high quality TFTs. As has been shown before, oxygen results in increased surface roughness of the ELA polysilicon film, which can enhance carrier scattering at the interface between the active layer (polysilicon) and the gate insulator [18,50,52]. Furthermore, it is possible that the placement of oxygen within the polycrystalline structure is not uniform and that oxygen preferentially tends to segregate at the grain boundaries of the polysilicon film. TEM results, as shown in figure 2-16, support this claim. It has been proposed that such segregation may be beneficial for the polysilicon film, acting as a sort of grain boundary "passivation"[14]. However, in this work it was found that polysilicon films annealed in air demonstrate the poorest performance and, therefore, this proposal must be discarded.

The most probable cause for the observed phenomena is likely to be the generation of trapping sites in the polysilicon film due to the presence of oxygen atoms in the silicon host. The generation of these traps can be related to stress fields in the polysilicon film due to mismatch in the silicon lattice induced by the incorporated oxygen atoms. These traps, upon filling, act as scattering centers, effectively decreasing the carrier conduction rate through the silicon network. In this manner, the quality of the polysilicon film decreases as the amount of incorporated oxygen increases. Studies of oxygen effects in Czochralski grown Si wafers suggest that above 1200 °C, as would be the case in ELA, oxygen forms large polyhedral precipitates, identified as being amorphous. In the TEM image of figure 2-16, amorphous precipitates can be seen quite clearly. The SiO_2 plastically compresses the lattice, generating dislocations plus large stacking faults[60]. Dislocations, in particular are harmful to device performance. Dangling bonds around dislocations are generally viewed as acceptors that capture electrons, and in the process, are surrounded by a positively charged space charge region. These regions result in increased carrier scattering and reduced mobility.

Using the approach introduced by Levinson and co-workers, and discussed in 3.3.3, the grain boundary trap density of our polysilicon films was estimated from the slope of the straight-line portion of a $\ln(I_D/V_G)$-vs.-$1/V_G$ plot[51]. The same TFTs were measured as fabricated and after a 15 minute hydrogen plasma treatment. The pertinent results are shown in figure 3-32, where the grain boundary trap density is plotted against the oxygen concentration in the polysilicon film, as measured using SIMS analysis, and presented in figure 2-14.

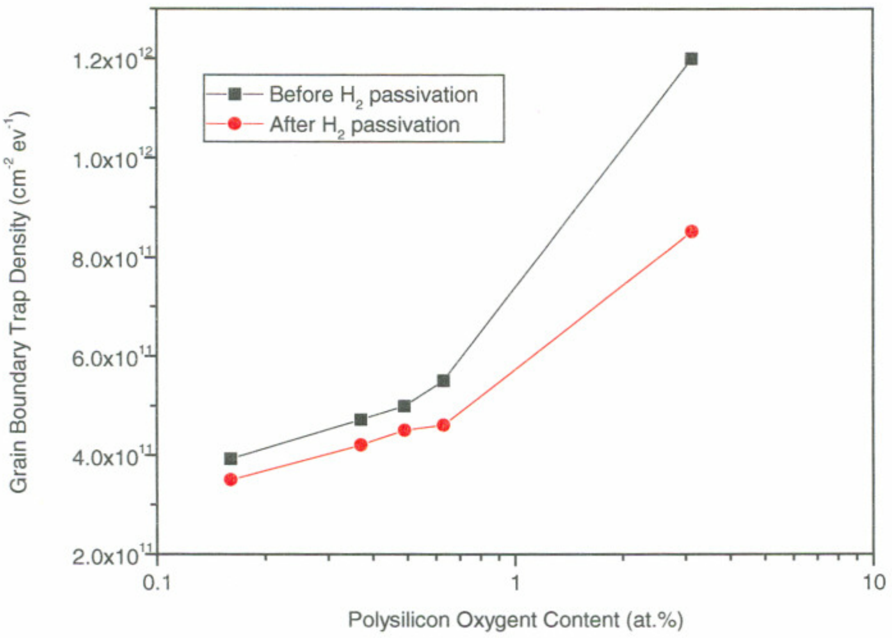


Figure 3-32: Polysilicon grain boundary trap density as a function of the oxygen concentration in the film. Trap densities were determined using the Levinson method[51]. Data are shown before (squares) and after (circles) hydrogen plasma passivation.

Worth noticing, the trap density is shown to increase with increasing amount of oxygen incorporated in the film. It is possible that oxygen, upon segregating at polysilicon grain boundaries, introduces localized stress fields that result in an increase of the density of strained silicon bonds at the grain boundaries. These strained bonds are generally unstable and can locally break and rearrange to give rise to unsaturated silicon bonds (dangling bonds) in the network. In this manner, the density of deep states (states near mid-gap) will increase in polysilicon films with high oxygen content. Similar results have been previously reported for TFTs fabricated with polysilicon films that were intentionally doped with varied doses of oxygen by ion implantation[61]. In an analogous manner, the mid-gap states were found to significantly increase with increasing oxygen dose in the film.

TFT performance attributes (field-effect mobility and threshold voltage) were also correlated to the oxygen content in the polysilicon film, before and after hydrogen passivation. These results are shown in figure 3-33.

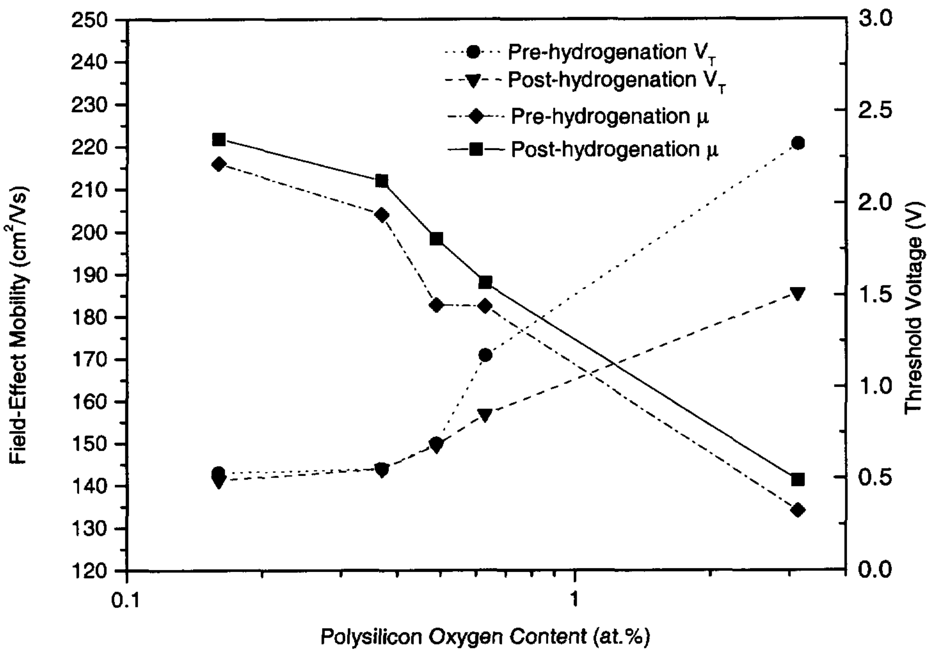


Figure 3-33: Polysilicon TFT field-effect mobility and threshold voltage as functions of the oxygen concentration in the film. Data sets are shown before and after hydrogen plasma passivation.

As expected, both characteristics show improvement as the oxygen content of the film decreases. However, one of the most notable features of the figures relates to the effect of hydrogenation: the threshold voltage of the devices is strongly influenced by the hydrogenation process only at high oxygen concentration (i.e. above 1-2at%). Moreover, the mobility is shown to be only marginally affected by the hydrogenation process.

From the device simulations shown in figure 3-8 (a), the threshold voltage is much more sensitive to trap states deep in the bandgap than tail states, while the mobility is affected more equally. Tail states are believed to emanate mostly from defects within the grains of the polysilicon material[50]. In contrast, deep states are typically related to grain boundary defect sites, especially dangling bonds[48,62.] From these conjectures and our results, it is obvious that oxygen incorporation in the polysilicon film increases both types of defects. Hydrogen plasma seems to be effective in passivating at least part of the grain boundary defects, thus improving the threshold voltage and subthreshold characteristics of the TFTs. In contrast, its effect on intra-grain defects is very minimal. Therefore, one of the main effects of increased oxygen concentration in the film is the increased generation of intra-grain defects in the material. This is, potentially, an irreversible deterioration mechanism and, thus, not possible to compensate with post-fabrication, passivation treatments. From this point of view, the mechanism may relate to the development of structural defects, such as micro-twins[63], or other types of structural anomalies, such as micro-roughness, that are not possible to annihilate through passivation. Since the deterioration in the materials properties manifests itself primarily through a reduction in the carrier mobility, it was concluded that these types of structural deficiencies develop within polysilicon grains (and enhance the concentration of tail states). This can be the result of strain in the silicon network, caused by the incorporation of significant amount of oxygen atoms.

Again, referring to figure 3-33, the field-effect mobility depends strongly on the oxygen content of the film and is not improved much through hydrogenation. Because hydrogenation is typically more effective at eliminating defects which create trap sites deep in the bandgap, there is reason to believe that the mobility is being controlled by trapping states close to the conduction band edge. To investigate further, source-drain current activation energy measurements of samples produced in nitrogen, argon, helium and air were made, after hydrogenation was performed. The results are shown in figure 3-34 on a log scale.

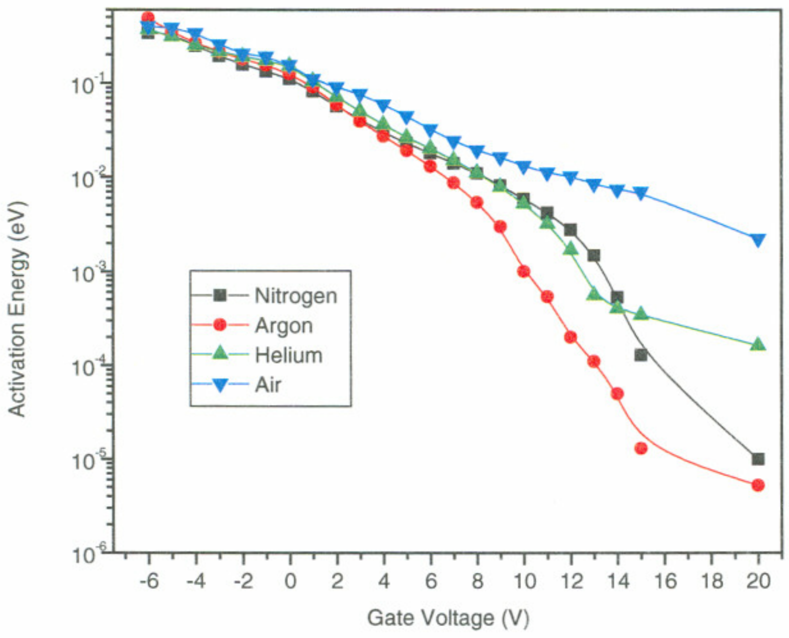


Figure 3-34: Source-drain current activation energy as a function of gate voltage for samples laser annealed in nitrogen, argon, helium and air, shown on a log scale.

Inspection of 3-30 reveals that above V_G=8 V, the activation energy of the sample made in air decreases at a much slower rate than the samples laser annealed in nitrogen, argon or helium. Other researchers have shown that the presence of a large number of band-tail states gives rise to a slow decrease in the activation energy, as a function of gate voltage[64]. Therefore, this is a strong indication that, after hydrogenation, tail states are still abundant, and are limiting both the on-current and mobility of the samples laser annealed in air.

Not to be overlooked, grain-boundary surface roughness may also contribute to the inferior performance of oxygen-rich polysilicon films. In this case, grain boundaries have been found to demonstrate much higher dangling bond density than those of films annealed in vacuum or inert gas, a fact that was related to the higher oxygen segregation at the grain boundaries. Upon hydrogen plasma treatment, the majority of these defects are passivated, as evidenced by the significant improvement in the TFT threshold voltage. However, even after hydrogen passivation, a performance offset is still clearly obvious between polysilicon films laser-annealed in air and films laser-annealed in vacuum or inert ambient. It was estimated that the oxygen concentration in the polysilicon film has to be lower than approximately 0.5at% for best TFT performance. Thus, for scanning ELA method, inert gas ambient is the best compromise between TFT performance and ELA process simplicity.

3.5 Summary

Several different techniques to improve poly-Si TFT device performance using an excimer laser have been studied. Through the investigation, important ideas for producing TFTs that performed well and could be realistically implemented in a mass production process were uncovered. Perhaps the most important parameter in optimizing an ELA process in the laser energy density. As we have shown in table 3-6, even small changes in the energy density (60 mJ/cm^2) can lead to large changes in the device characteristics (average field effect mobility more than doubles). For this reason, it is imperative that the energy density is chosen carefully. However, even with a meticulous selection of energy density, variance in performance should be expected as average quantities improve, as shown in figure 3-16.

Use of multiple scans to grow larger grains presents some intriguing advantages, however, trade-offs become apparent. A distinct benefit resulting from the use of this technique was an improvement in grain size, drive current and mobility with each scan while uniformity was maintained. On the downside, the off current and subthreshold slope became worse. It was determined that fixed positive backside poly-Si/SiO_2 interface charge accumulated through successive scans. The result was a degradation in the subthreshold characteristics, including the subthreshold swing and leakage current. It may be possible that using a lower energy density (as in R(I)) or a different barrier layer material could correct some of the problems encountered.

From a performance perspective, use of an SiO_2 barrier film is necessary, and involves only one extra deposition cycle. Because of the larger average grain size possible with an SiO_2 barrier layer, all of the on-state characteristics improved. The average mobility, in particular was as high as 198 cm^2/Vs with a barrier and was only 137 cm^2/Vs without one. However, because of fixed interface charge on the poly-Si/SiO_2 back interface, the devices made with a barrier layer turned on more slowly. Therefore, an alternative to TEOS SiO_2 should be sought which could lead to better subthreshold features.

Through activation of dopants using the laser, the possibility of having a fully low-temperature process has been shown. However, the leakage current was unacceptably large, often times much greater than a nA for V_G=-20V. This was due to a large gate current, presumably resulting from ineffective densification of the gate oxide during the dopant activation step. It is possible that using a shorter laser wavelength may have worked better, for this process. A shorter wavelength (λ=193 nm using ArF for example) would be absorbed by the gate oxide and thus heat it more effectively in the process. A two-step process where the dopant is laser activated initially and a low temperature furnace anneal is used to density the gate oxide could also work. In any case, laser activated and furnace activated dopants showed similar characteristics over a range of conditions, including the subthreshold swing, mobility and drive current, as seen in table 3-9.

Our results revealed that substrate heating, was an unnecessary and time consuming step, and advantages gained were small if any. Because the grain size could be made to be nearly equal by adjusting the energy density, all of the device characteristics for the samples made at room temperature and at 400 °C were nearly identical, as seen in table 3-10.

Upon fabrication and evaluation of TFTs using polysilicon material formed by ELA in different ambients, significant differences among the various materials were observed. Whereas the performance attributes of polysilicon films annealed in vacuum or inert ambient were quite similar, the performance of polysilicon annealed in air was drastically inferior to all, as shown in figure 3-31. This result was attributed to the increased oxygen incorporation in the film, in the case of ELA process in air. As our findings suggest, oxygen increases the density of both deep states and tail states in the polysilicon band-gap; its effect on the latter being more pronounced and not possible to compensate through conventional passivation techniques. Thus, for scanning ELA method, inert gas ambient is the best compromise between TFT performance and ELA process simplicity.

Chapter 4
Conclusions and Recommendations

In an effort to develop a process to optimize the overall performance of laser annealed poly-Si TFTs, while at the same time considering cost issues, account was taken of the salient issues. As a starting point, a considerable amount of effort was spent getting to understand the poly-Si film itself. Devices were then produced and attempts were made to relate the materials characteristics to device performance. This was done through extensive device characterization, along with the outgrowth of a poly-Si TFT model.

What stood out as paramount throughout this study was the need for uniformity. Often times, in the literature, values are quoted describing the qualities of the poly-Si film or the TFTs, in terms of the best case scenario. Usually, this means that the maximum grain size, along with a corresponding TEM image are suggested to be representative of the process as a whole or that only the best performing devices are discussed. In reality though, the distribution of the attributes and the worst case scenario is just as, or more important. For these reasons, the utmost care must be taken to ensure that a large number of samples are examined so that a true average can be derived, both when examining the grain structure and when measuring devices. This demands a great deal of time and painstaking effort, but its importance cannot be overlooked.

Alongside this effort, care must be taken to ensure reproducibility. The laser annealing process, in its nature, is in some ways inherently unstable, due to a combination of pulse to pulse energy density variations, and the sensitivity of the resulting average grain size to the laser power. This instability can be overcome, but not easily. Attention to detail is absolutely necessary. The notable details include characterization of the beam itself, including its shape and uniformity, a precise and accurate measurement of the energy density, understanding how the energy density is affected by prolonged use of the laser and the pressure in the resonant cavity. Of course, as with any device-related technology, insuring the cleanliness of the system, and especially the optics is obligatory.

By pursuing the three-fold effort of materials characterization, modeling and device characterization, the underlying features determining device performance were uncovered. In fundamental terms, three qualities influenced most directly the ultimate capabilities of laser annealed poly-Si TFTs: the grain size, the interface characteristics and the incorporation of impurities. By maximizing the grain size, the density of grain boundary defects was reduced. This improved the on-state and off-state qualities by presenting fewer trap states to fill and limiting the availability of intermediate energy states in the band-gap for carrier tunneling. However, some care must be taken not to allow intra-grain defects to form, otherwise improvements from the reduction of deep-states is compensated by the increase in the density of tail-states. Interface qualities, stemming from the choice of dielectric materials and processes that may damage the dielectric have been shown to affect the subthreshold swing, threshold voltage, and leakage current, by increasing the density of fixed interface charge. Incorporation of oxygen into the poly-Si thin film increases the number of scattering centers and also increases the trap state density by disturbing the Si matrix.

Four factors, previously discussed, also affect the throughput, and may affect the cost of producing devices: multiple passes, substrate temperature, additional processing steps and the annealing ambient. To optimize the process from this standpoint, an air ambient, without substrate heating, a barrier layer or post-hydrogenation, together with a single annealing step would be carried out. It is also important to consider whether a fully low temperature process should be implemented, thus demanding the need for laser activated dopants.

Based on the above considerations, a balance between performance and processing time can be arrived at through the following recipe. To eliminate the need for vacuum equipment, a laminar flow blower of some sort can flood the processing area with either nitrogen or argon prior to and during the annealing to reduce oxygen contamination. Substrate heating is unnecessary and thus annealing should be done at room temperature. A 200 nm thick SiO_2 barrier layer should be used, preferably deposited by CVD, to improve the grain size and prevent impurity segregation from the substrate. A single laser scan is sufficient to crystallize the film. In addition, a post-hydrogenation step is important. If a fully low temperature process is sought, activation of dopants using a shorter wavelength (193 nm for example) may prove beneficial.

The possible directions of future work are practically unlimited, and may include the study of p-channel devices and thus CMOS structures. In addition, performing the laser dopant activation, as described in section 3.4.5, in two steps, could prove beneficial. A study of different barrier materials and gate oxides, including SiN, could help to reduce the density of fixed interface charge, and improve the subthreshold qualities. Improving the quality of the barrier layer has been shown to be especially important. Coming up with different device structures, possibly including a lightly doped drain (LDD) configuration, could drastically reduce the leakage current, making the devices better suited for AMLCD applications. Characterization of the devices can be carried further by carefully analyzing the I_D-V_{DS} characteristics, including the kink effect[65]. Stress testing of the devices should also be performed.

In addition, further refinement of the TFT models developed and presented in this work is necessary. The two-dimensional ATHENA/ATLAS model can be improved upon by concentrating grain boundary defects at specific locations, and not spreading them evenly throughout the channel. In this way, the position of the grains themselves become important, as in physical devices. It is also important to develop a compact model for both n-channel and p-channel poly-Si TFTs which could be implemented in a circuit simulator. Incorporating the effects of grain size and interface properties for instance, into the model would prove useful in examining how well these devices would work in realistic applications, such as a shift registers or a CMOS buffers.

Appendix

A1 Analytical Model for Poly-Si TFT I-V Characteristics Using Distributed Method

The models in the analysis below are developed from first principles. The main objective in developing these models is not only to emulate TFT characteristics but also to give insight as to how and why. Other models, which fit the behavior of poly-Si TFTs to the behavior of standard MOSFETs, are well developed, and find use in circuit simulators. For simplicity, in this study only the distributed model is examined, and only n-channel devices are considered. Though the 2-D approach is often used[53], most of the important theoretical points necessary to understand the working of poly-Si TFTs are brought out in examining the distributed method.

A1.1 On Current

In the distributed case, discussion of the on current usually begins with Poisson's equation[66], which appears as it does for single crystal MOSFETs with the addition of a charge trapping term. This term reduces the number of free carriers in the channel and leads to the higher threshold voltage and lower mobility, characteristic of poly-Si TFTs. More often than not, a distribution of trapping sites within the bandgap is used. The gradual channel approximation is invoked, leading to a pseudo-1D solution. Numerical methods are used to arrive at a final solution.

In Poisson's equation:

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{\rho}{\varepsilon_{si}} \tag{A-1}$$

x is the distance along the film thickness, ρ is the charge density, ε_{si} is the dielectric constant of silicon and ψ is the electrostatic potential. The charge density is written as

$$\rho = q\left(p - n + N_D - N_A\right) \tag{A-2}$$

where qN_D is the charge of the occupied, hole grain boundary traps (or donor traps), qN_A is the charge from the occupied, electron grain boundary traps (or acceptor traps), n is the free electron concentration and p is the free hole concentration. Since the charge traps are usually distributed over some range of energies, the total trapped charge can be written

$$qN_D = q\int_{Ev}^{Ec} \frac{N_D(E)}{1+\exp[(E_F - E)/kT]} dE \tag{A-3}$$

and

$$qN_A = q\int_{Ev}^{Ec} \frac{N_A(E)}{1+\exp[(E - E_F)/kT]} dE \tag{A-4}$$

where E_F is the Fermi energy, k is the Boltzmann constant, T is the absolute temperature, E_c is the energy of the conduction band edge and E_v is the energy of the valence band edge. Often, $N_A(E)$ is modeled as an exponential function decaying from the conduction band edge and $N_D(E)$ is likewise an exponential function decaying from the valence band edge. The free carrier concentrations, n and p are given in the Boltzmann approximation by

$$n = n_i \exp\left(q\psi/kT\right) \quad \text{and} \quad p = n_i \exp\left(-q\psi/kT\right) \tag{A-5}$$

where $\psi = \frac{E_F - E_i}{q}$

and E_i is the intrinsic Fermi energy. For small drain-source voltages, V_{DS}, the boundary condition at the surface between the gate oxide and polysilicon film at x=0 is

$$\frac{\partial \psi}{\partial x} = \frac{C_{ox}}{\varepsilon_{si}}(V_G - V_{FB} - \psi_s) \tag{A-6}$$

where V_{FB} is the flat band voltage, V_G is the voltage applied to the gate electrode with respect to the source, ψ_s is the surface potential and C_{OX} is the oxide capacitance per unit area. The second boundary condition is typically defined as in equation (3-7):

$$\frac{\partial \psi}{\partial x} \to 0 \quad \text{for large x} \tag{A-7}$$

The resulting non-linear Poisson's equation together with the two boundary conditions can be solved using a numerical technique to find ψ as a function of x. Frequently, this consists of substituting finite-difference approximations for derivatives together with a linearization step, as with Newton's method, and a successive over-relaxation scheme to solve the resulting simultaneous equations. Otherwise, a finite element method is used, as described later in the chapter.

To determine the drain current (I_D), an expression can be written for the increment of voltage across a small section of the channel:

$$dV(y) = I_D \times dR = \frac{I_D \times dy}{W \times \mu_{LF} \times Q_f(y)} \tag{A-8}$$

where μ_{LF} is the low-frequency drift mobility, W is the width of the channel, and Q_f is the mobile charge per unit area. As is commonly done for standard MOSFETs, the contribution of diffusion to the total current has been neglected. Q_f can be determined by integration, as in equation (A-9), after $\psi(x)$ is known

$$Q_f = \int_0^{\infty} n_i \times \exp(q\psi(x)/kT)dx \qquad \text{(A-9)}$$

where n_i is the intrinsic carrier concentration. Because the analysis thus far has been carried out neglecting the potential drop across the channel, taking this into account requires replacing the gate voltage (V_G) by V_G-V at an arbitrary point y between the source and drain. Integrating across the length of the channel, and assuming that μ_{LF} is not a function of y, leads to equation (A-10):

$$I_{ON} = q \times \left(\frac{W}{L}\right) \times \mu_{LF} \int_0^{V_D} Q_f(y)dV \qquad \text{(A-10)}$$

where L is the channel length. From the equations above, the relationship between the on current and applied voltages can be determined, for a given distribution of traps.

A1.2 Off Current

The off current in poly-Si TFTs is considerably higher than single crystal MOSFETs and conventional wisdom has it that the presence of defects is the culprit[67]. These defects create energy levels within the silicon bandgap, which serve as traps. The traps may be used by electrons (holes) as intermediate steps to reach the conduction (valence) band. As the field increases, leakage current generation through trap sites becomes more prevalent due to field enhanced tunneling.

Other authors have pointed out, that under low fields, near V_G=0, the leakage current varies linearly with the channel length, which suggests that it is determined by the channel resistivity[68]. For large gate voltages, the off-state current is independent of channel length, but dependent on channel width, suggesting it is determined by thermionic emission, thermionic field emission or pure tunneling via traps in the high electric field region of the drain junction.

As mentioned above, the three most likely candidates for the leakage mechanism in poly-Si TFTs are: 1) thermal emission from traps, 2) field emission (tunneling) from traps, and 3) thermionic field emission, all of which are depicted in figure A-1.

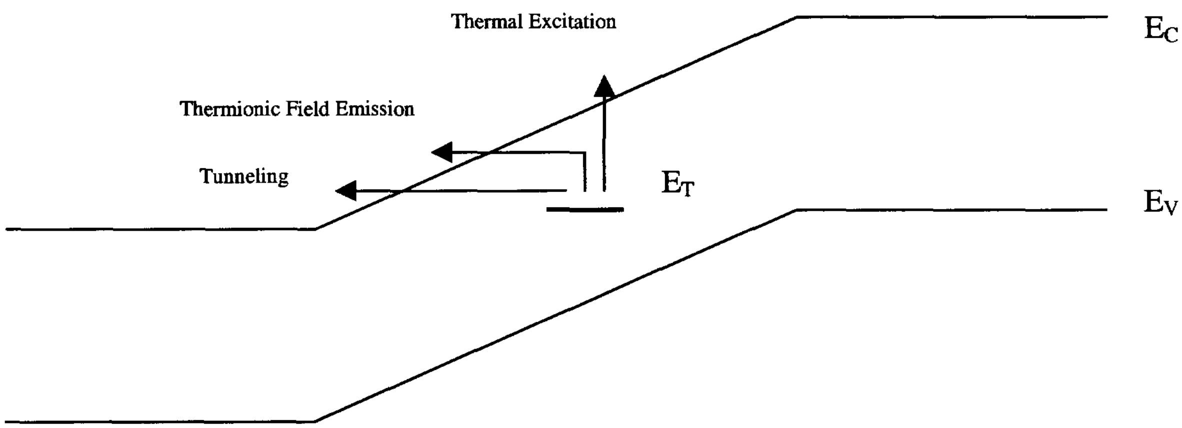


Figure A-1: Depiction of various leakage current generation mechanisms for an energy level within the bandgap (E_t) into the conduction band.

Thermionic field emission is the most general case, being in essence a combination of thermal and field emission. For tunneling, the rate of emission of electrons from traps to the conduction band may be written[69,70]

$$U_e(E) = \frac{N(E) \times f_t(E)}{\tau_e(E)} \tag{A-11}$$

where N(E) is the distribution for the areal density of trap sites, $f_t(E)$ is the probability of electron occupancy of the trap at energy E, and $\tau_e(E)$ is the time constant for tunneling for an electron tunneling from E to the conduction band edge, E_c. For a triangular barrier in the WKB approximation[71,72],

$$\tau_e(E) = \frac{q \times F}{4[2m_e^* \times (E_C - E)]^{1/2}} \times \exp\left[(\frac{4(2m_e^*)^{1/2}}{3}) \times \frac{(E_C - E)^{3/2}}{q \times \hbar \times F} \right] \qquad \text{(A-12)}$$

where E is measured from the conduction band edge, $\hbar$ equals h/2π where h is Planck's constant, m_e^* is the effective mass, and F is the average vertical electric field (y-direction) in the region of interest. Similar expressions as those above can be written for holes. The normalized probability for thermal excitation is

$$n(E) = \frac{1}{kT} \times \exp(\frac{E_t - E}{kT}) \qquad \text{(A-13)}$$

where E_t is the trap level energy. Combining these expressions, and assuming all of the trap states are at a single energy E_t, the rate of emission of electrons from the traps via a virtual, excited state of energy E is given by

$$U_e(E) = \frac{N \times f_t}{\tau_e(E)} \times \frac{1}{kT} \times \exp(\frac{E_t - E}{kT}) \qquad \text{(A-14)}$$

where N is the total surface density of trap sites. Now, the total rate of emission of electrons via all possible virtual states, U_e, can be determined by integrating this expression from E_t to infinity, but the complexity of the expression for $\tau_e(E)$ prevents a closed form solution. However, if τ_e is assumed to be independent of energy, which is equivalent to ignoring thermal excitations and only considering tunneling, U_e can be solved for and the analysis carried out further.

$$U_e = \int_{E_t}^{\infty} U_e(E)dE = \frac{N \times f_t}{\tau_e} \tag{A-15}$$

If the same operation is performed for holes,

$$U_h = \frac{N \times (1 - f_t)}{\tau_h} \tag{A-16}$$

where τ_h is the tunneling time constant for a hole into the valence band, and U_h is the total rate of emission of holes from E_t to the valence band. The occupancy factor can be determined by realizing that in steady-state, the total rate of emission of electrons into the conduction band equals the total rate of emission of holes into the valence band. Setting $U_h = U_e$ leads to

$$f_t = \frac{\tau_e}{\tau_e + \tau_h} \tag{A-17}$$

Substituting this back into the expression for U_e or U_h gives

$$U = \frac{N}{\tau_h + \tau_e} \tag{A-18}$$

where U is the rate of emission of carriers into the bands. Finally, to find the leakage current, use

$$I_{leak} = q \times Vol \times U \tag{A-19}$$

where Vol is the volume over which the average vertical electric field is large enough to cause significant thermionic field emission.

The above analysis illustrates the important points in the theory, yet is incomplete. It is still necessary to find the relationship between the electric fields and the applied voltages, and in so doing, determine Vol as a function of the V_G and V_D. This is difficult to do analytically, and either simulators or numerical methods are used for this purpose.

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Vita

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Aaron entered Arizona State University in 1993 on a Graduate Assistantship in Areas of National Need grant. During his time at ASU, he investigated thin metal films deposited on silicon substrates in ultra-high vacuum using a scanning tunneling microscope. He went on to graduate with an M.S. degree from the Department of Physics in the spring of 1995.

Aaron entered the Oregon Graduate Institute to pursue a Ph.D. in the fall of 1995. Afterwards, he became involved in a project sponsored by Sharp Laboratories of America, investigating the characteristics of laser annealed polysilicon thin film transistors. In his final year at OGI, he was sponsored by an Intel Foundation Fellowship.

During the course of his time at OGI, Aaron contributed the following publications:

- A.T. Voutsas, A.M. Marmorstein and R. Solanki, "Characteristics of excimer laser annealed polysilicon films for application in polysilicon thin-film-transistor devices", *Proc. SPIE*, No. 3014, p. 112, (1997).

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