Comparison of CMOS XOR and XNOR Gate Design

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Table of Contents

List of Tables

List of Figures

Abstract

Comparison of CMOS XOR and XNOR Gate Design

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Two new methods are proposed to implement the exclusive-OR and exclusive-NOR functions at the transistor level. The first method uses non-complementary signal input and the least number of transistors. The second method improves the performance but two additional transistors are utilized. The proposed method uses the same number of transistors but adds with more drive capability. These circuits were first implemented using a Physical Layout Design tool produced by Mentor Graphics. These layouts were extracted and simulated using circuit simulator HSPICE and ACCUSIM. Delay and power consumption of these circuits were characterized and compared with previously known designs.

1.0 Synopsis

Complementary Metal Oxide Semiconductor (CMOS) technology is advancing for microprocessors. Supply voltage (V_{dd}) and transistor size continue to scale smaller sizes with lower power dissipation and faster microprocessors. The exclusive-OR (XOR) and exclusive-NOR (XNOR) functions are popular gates in microprocessors. The XOR/XNOR gates are fundamental unit circuits used in comparators, parity checkers, error detectors and correctors, multipliers, adders (ALU, AGU), etc. Many circuit implementations of XOR/XNOR gates have been proposed previously. One circuit that is implement the XOR/XNOR gates was published by Jyh-Ming Wang, Sung-chuan Fang, and Wu-shiung Feng [12]. In their work, Jyh-Ming Wang compared several circuit implementations using supply voltage (V_{dd} = 5volt) with TSMC 0.8μm fabrication technology.

This thesis proposes several circuit-level implementations of XOR/XNOR gates. These circuits were simulated using a circuit simulator (HSPICE) with various supply voltages. The various supply voltages are important because as technology continues to scale to smaller feature size, supply voltage (V_{dd}) also needs to scale down for reliability and power reduction [9].

The optimizations in this thesis have been performed through simulations with HSPICE using various supply voltages from V_{dd} = 1volt to V_{dd} = 2.5volt on TSMC 0.35μm fabrication technology. First part in thesis simulations with HSPICE using TSMC 0.35μm fabrication technology is devoted to re-evaluation of these circuit implementations using more advanced technology. Second part of the thesis proposes two new combination XOR/XNOR circuit implementations and simulated with Mentor Graphic using TSMC 0.25μm fabrication technology. The Design Architecture (DA) tool was used for designing the circuits and the ACCUSIM tool was used for simulation. The optimization in this thesis has also been performed through simulations with Mentor Graphics Software using various supply voltages from V_{dd} = 1volt to V_{dd} = 2.5volt on TSMC 0.25μm fabrication technology.

1.1 Physical Layout

The Mentor Graphics Physical Layout tool was used to design the XOR/XNOR circuits. The Lambda value was used, specifying Lambda equal to 0.125μm (λ=0.125). In addition, the supply voltage used was V_{dd} = 2.5volt with TSMC 0.25μm fabrication technology for this Physical Layout Design [5]. The stick rule was used for the component layout and applied the design rule applied for the component layout space requirements. The dimension-width scaling of the gate-area ratio in Complementary Metal Oxide Semiconductor P-channel (CMOSP) and Complementary Metal Oxide Semiconductor N-channel (CMOSN) is 3:1. The physical W/L sizes of CMOSP and CMOSN are 2.1μm/0.35μm and 1.05μm/0.35μm respectively, in order to meet the optimal design of low power with high performance.

1.2 Fan-Out

The term "fan-out" as used with digital circuits describes the maximum number of load gates (circuits) of similar design as the driver gate that can be connected to the output of XOR/XNOR thus helping to drive the output signal for the driver gate [12].

1.3 Input Vector Generation

Non-complementary [12] inputs, signal A and signal B vectors, were generated so as to test the design in four cases: AB=00, AB=01, AB=10, and AB=11. Also the complementary inputs, signal A and signal A', signal B and signal B' vector, were generated to test the design in four cases: AB=00, AB=01, AB=10, and AB=11. The XOR logic gate operates based on a truth table where if input signal A and signal B are the **same** value then the output signal is "LOW." If input signal A and signal B are **different** values then the output signal is "HIGH." The exclusive-OR and exclusive-NOR functions are shown in Table 1.1. Assuming the input signals are A and B, then the exclusive-OR of A and B,

denoted A$\oplus$B is logically equivalent to A'B+AB'; and the exclusive-NOR of A and B, denoted as A $\otimes$B, is logically equivalent to AB+A'B'.

Table 1.1
Functions of XOR and XNOR

A	B	XOR	XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

Exclusive-OR A XOR B = A $\oplus$ B
= A'B+AB'

Exclusive-NOR A XNOR B= A$\otimes$ B
= AB + A'B'

1.4 MOSFET Scaling

MOSFET Scaling determines how threshold voltage should be decreased by the scaling factor, K, in proportion to the power supply voltage. In this work, MOSFET Scaling is applied to CMOSN and CMOSP from the TSMC 0.25μm fabrication technology. According to the fundamentals of modern VLSI devices by Yuan Taur and Tak H. Ning [9], when the TSMC fabrication technology scales down the threshold voltage (V_{th}), it is also necessary to scale down the physical dimension.

1.5 Adder Experiment

The XOR gates that were chosen for the design of the adders listed in appendix A were the XOR transmission gate (Figure 2.1) and the proposed XOR structure (Figure 2.5). The advantage of the proposed XOR structure is the Pass-Transistor and the ability to transmit the signal HIGH (or "1") and signal LOW (or "0") directly from the input. The disadvantage of the proposed XOR structure

is that the Pass-Transistor does not scale well. The advantage of the XOR transmission gate is that it is a powerful device that scales well, and has a full swing signal level. The disadvantage of the XOR transmission gate is its complementary inputs. As in Figure 1.1, the 8-bit adder given a general idea of how many XOR gates need to use. Microprocessors use the XOR gate everywhere so they are very important.

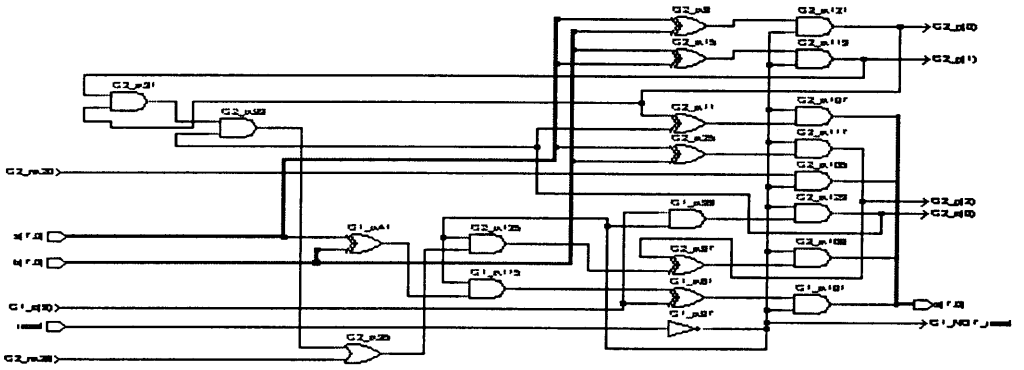

Figure 1.1, Logic Gate of 8-bit Adder

1.6 Comparison of Results

Results were compared between our proposed XOR gates and other conventional XOR gates, comparing average power dissipation and average delay measuring from 50 percent of the waveform between the inputs and the outputs. We also compared average rising time delay measuring from 10 to 90 percent of the waveform between the inputs and the outputs and average falling time delay measuring from 90 to 10 percent of the waveform between the inputs and the outputs [12]. Compared data analysis was also done for the average power dissipation, average delay, and average rising/falling delay time. For average delay and average rising/falling delay time must fit in the negative linear slope. Also, the average power dissipation must fit in the positive linear slope [11].

2.0 Background

The exclusive-OR (XOR) and exclusive-NOR (XNOR) functions are fundamental for various circuits used in comparators, parity checkers, full adders, multipliers, etc. There are two kinds of MOS; the N-channel Metal Oxide Semiconductor (NMOS) and the P-channel Metal Oxide Semiconductor (PMOS). It is well known that NMOS transistor can transmit the signal "LOW" (or "0") completely, but it has poor performance when transmitting the signal "HIGH" (or "1"). If one takes a NMOS transistor to implement a switch device, a control signal is added to the gate terminal and sets one end of the signal "HIGH", where the other end will drop to the threshold voltage of NMOS, V_{nth}. The PMOS transistor can pass a signal "HIGH" fully but handles a signal "LOW" poorly. As a switch device, if a signal "LOW" appears on the source end of the PMOS transistor, the destination end will not sink to signal "LOW", as it will keep a higher than threshold voltage of PMOS, $|V_{pth}|$.

Based on the transmission gate theory, the realized XOR/XNOR circuit uses transmission gates (Figure 2.1). This structure needs only four transistors, but the complementary inputs can lose driving capacity. In general if the output signal of a circuit comes from V_{dd} or V_{ss} directly, this circuit has drive capability. However, it is well known that a transmission gate has no drive capability. Using this technique, the circuit can have configurations of XOR and XNOR as in Figure 2.1, but adds an inverter behind each case. Therefore, the improved versions of the transmission gates shown in Figure 2.1 are illustrated in Figure 2.2 as transmission gates with driving output.

2.1 Fan-Out of XOR/XNOR Gates

The fan-out of a logic gate is the total number of gate inputs that are driven by a gate output. This is usually expressed in terms of some default gate size. For instance, one might express the loading of a minimum-sized inverter as unity, and capacitor load are between 1pF and 5pF. The circuit implementations

shown in Figures 2.2, 2.4b, 2.6, 2.12a, 2.12c, and 2.12d with two input XOR/XNOR gates and four input XOR/XNOR gates all have a fan-out of one. Also, in the combination-circuits implementations shown in Figures 2.M2, 2.M3, and 2.M5, the two input XOR/XNOR gates and the four input XOR/XNOR gates all have a fan-out of one.

When the amount of fan-out is small, the poor signal level can still drive other circuits correctly. If the amount of fan-out is no longer small or the poor signal has to pass through several improper transistors, i.e., transmit signal "HIGH" by NMOS or pass signal "LOW" by PMOS, then the poor signal level may degenerate and no longer be guaranteed to work right. In order to overcome the individual defects, combining the NMOS and the PMOS yields a transmission gate that can pass both signal "HIGH" and signal "LOW" with excellent performance.

2.2 Transmission Gates

Although a CMOS transmission gate has better quality, there is full swing signal in a CMOS transmission gate, i.e., it needs complementary signal values to control the gates of PMOS and NMOS. Usually, an inverter is needed to generate a complementary input. Conventionally, a logical circuit can be realized with a canonical CMOS transistor. According to transmission gate theory [7] if a high impedance state is available, fewer transistors can be used. The performances with the proposed design are better than the past designs [5] and are proven after a careful analysis of appropriate simulations.

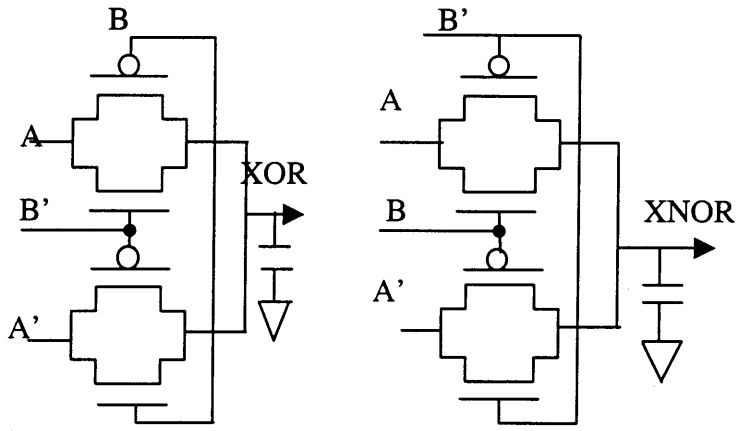

Figure 2.1 The XOR and XNOR Functions Implemented by Transmission Gates.

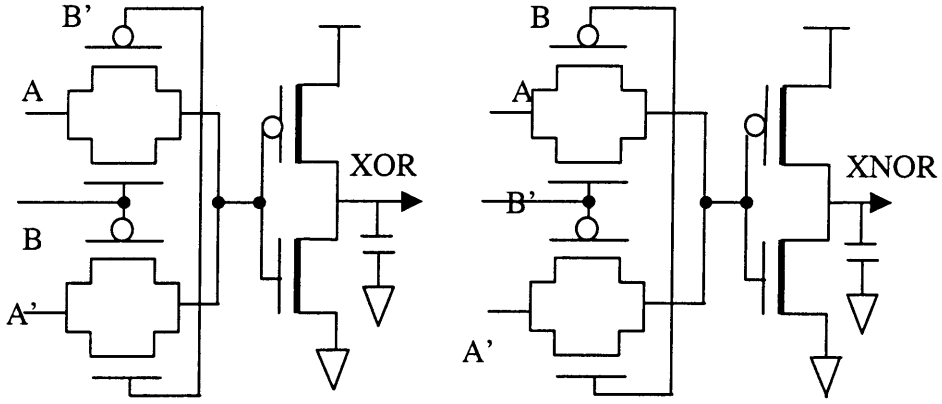

Figure 2.2 The XOR and XNOR Functions Implemented by Transmission Gates with Driving Output.

2.3 Inverter-Base Gates

Based on the inverter configuration, two inverters can be arranged appropriately for the XOR function as well as the XNOR structure. The circuits are shown in Figure 2.3. For the structure shown in Figure 2.3(a), when input signal A is "HIGH", input signal A' must be "LOW". The signal A and signal A'

are connected to the V_{dd} end of PMOS and the V_{ss} end of NMOS in the second inverter. The second inverter functions like a standard inverter, and outputs the signal B' is the output signal of XOR/XNOR gates. Therefore, the output signal of the XOR/XNOR gates will be a perfect AB' signal. On the other hand, when the input signal A is "LOW", input signal A' must be "HIGH". The output of the inverter will be a poor signal B because it transmits a signal "HIGH" by NMOS and a signal "LOW" by PMOS. That is, if only four transistors are used to implement an XOR function based on the inverter configuration, its output will be complete on signal AB' but poor on an A'B signal. An additional transmission gate can correct the problem. In Figure 2.4(a) [7], when input signal A is "HIGH" the output of the structure is signal B', as described above, the additional transmission does nothing. It will be a good AB' signal level. When input signal A is "LOW", the transmission gate will pass signal B to the output end directly and fully. Hence the output will be a good A'B signal level. This function will be complete on all of the input cases. In Figure 2.4(b), an additional tailing inverter can also improve the poor signal coming from the output end of the four transistors XNOR structure, and output the good signal level. For these two cases, they do not need the complementary signal inputs and the driving property is better than Figure 2.1 as well. However, these structures have some disadvantages such as not having full driving capability on the output end, or more delay time.

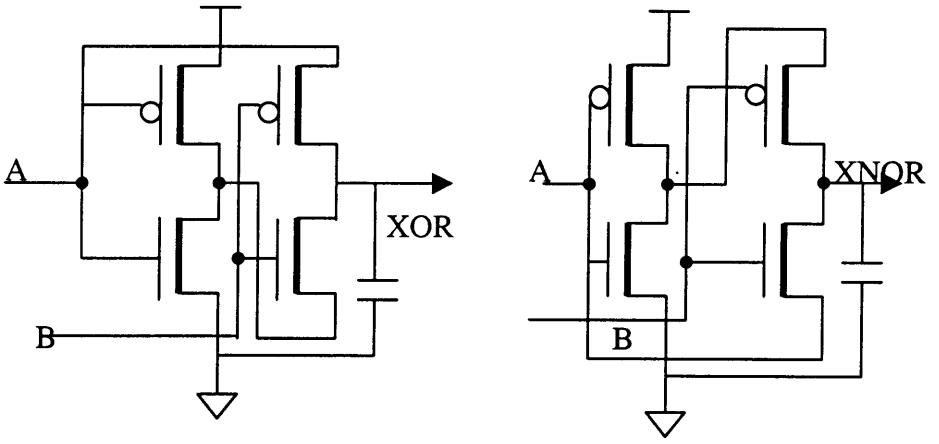

Figure 2.3(a) Inverter-Base XOR Structure (b) Inverter-Base XNOR Structure.

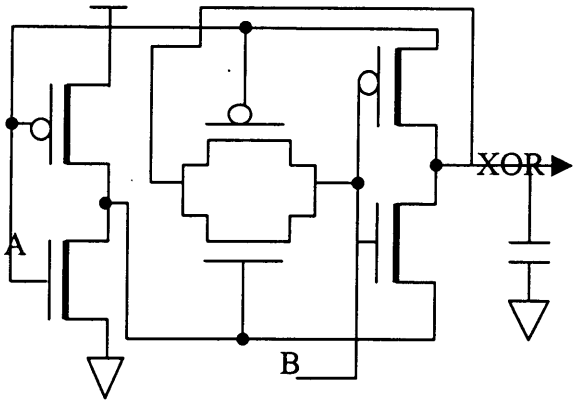

Figure 2.4(a) Improved Version of XOR Structure.

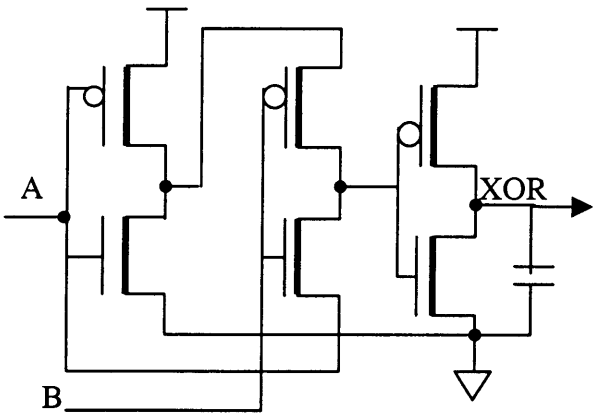

Figure 2.4(b) Another Improved Version of XOR Structure.

2.4 Proposed Structures

For the four transistor designs, the proposed structures require non-complementary inputs and their output is nearly perfect [12]. The configurations for the proposed XOR and XNOR structures are shown in Figure 2.5. For analysis of the XOR structure the output signals are applied to the inputs to test the XOR gates with the values as AB=01, AB=10, and AB=11 were completed with good output signals. For an incomplete output signal, when applied the input signal to test the XOR gates with the values as AB=00, each PMOS will be on and will pass a poor "LOW" signal level to the output end. That is, if the input signal to test the XOR gates with the values as AB=00, the output will have a threshold voltage $|V_{pth}|$, a little higher than "LOW." For the XNOR function, the output signal in the case of AB=00, AB=01, and AB=10 will be complete. When AB=11, each NMOS will be on and pass the poor "HIGH" signal level to the output end.

The proposed structure discussed above uses four transistors and does not have driving output. By cascading a standard inverter (fan-out) to the XNOR circuit, a new type of XOR, as shown in Figure 2.6 will have a driving output, and the signal level at the output end will be perfect in all cases. The same technique may use structure as shown in Figure 2.7.

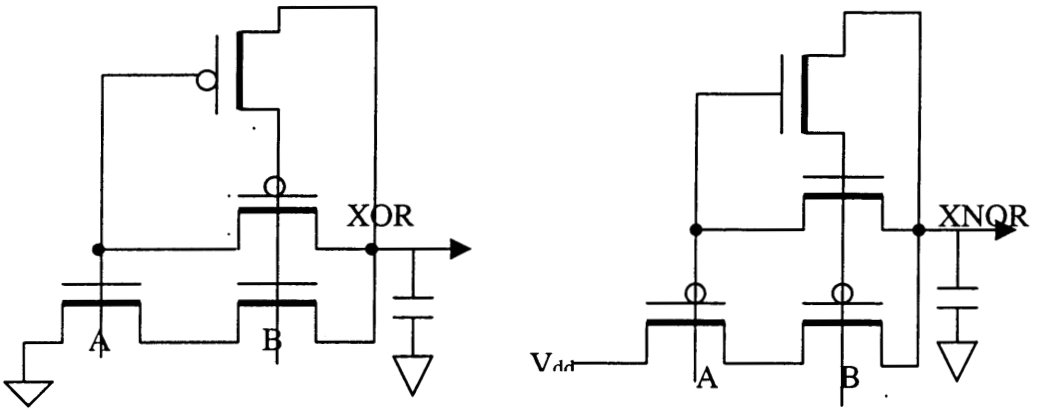

Figure 2.5 Proposed XOR and XNOR Structures.

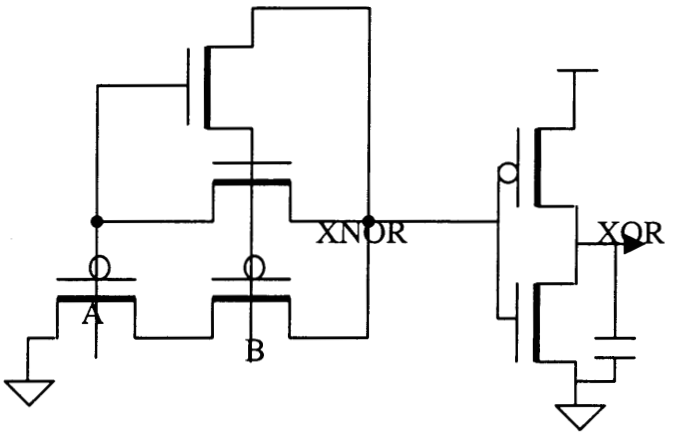

Figure 2.6 The Proposed XOR Structure with Driving Output.

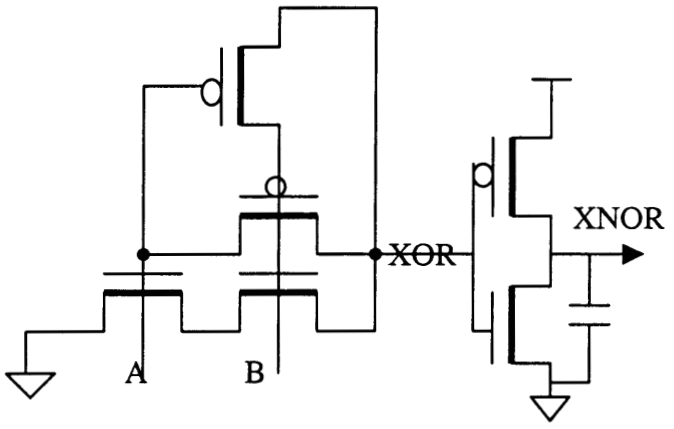

Figure 2.7 The Proposed XNOR Structure with Driving Output.

2.5 Realistic Gates

All of the six transistor structure and the previous ones using transmission gates with driving output (Figure 2.2), improved version of XOR structure (Figure 2.4(a)), another improved version of XOR structure (Figure 2.4(b)), and the proposed XNOR structures with driving output (Figure 2.6) were simulated under nearly realistic conditions to determine drive capability. For the XOR structure, the circuit was redesigned as a realistic-simulated circuit as shown in Figure 2.2 (Figure 2.12(a)), Figure 2.4(a) (Figure 2.12(b)), Figure 2.4(b) (Figure 2.12(c)), and Figure 2.6 (Figure 2.12(d)).

The output waveform of an inverter will be a more realistic signal in the physical design. For convenience, we generate input signal A' and input signal B' from actual simulated realistic inverters. The signals displayed at the input ends of the XOR function will be signal A and signal B, and the output value at the output end of the XOR function will be $(A \oplus B)$. In order to determine the driving capability, an additional capacitor is connected to the output end of each case. Then the driving capability can be determined by the capacitor rising time and falling time. If a circuit has strong driving output, the rising time and falling time will be shorter than the one with poor driving output. If one uses the proposed methods of four transistors to drive canonical CMOS circuits, it can still work correctly. When the output levels of both four transistor cases are poor, an added tailing inverter can improve the defect, and the driving capability is present for the proposed six transistor version, and one can utilize it as a generalized XOR or XNOR function.

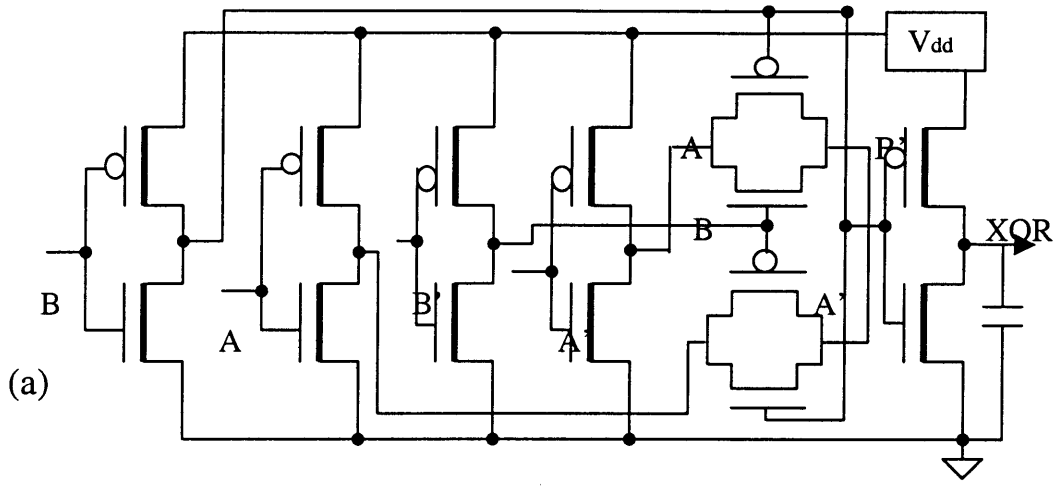

Figure 2.12a Realistic-Simulated Circuit for Figure 2.2.

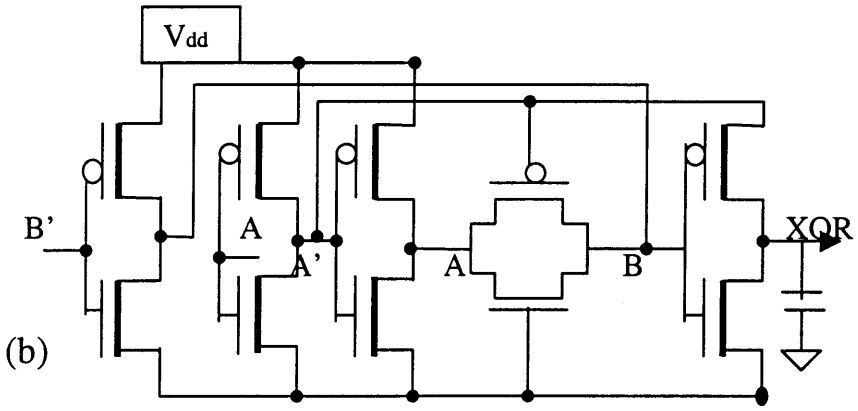

Figure 2.12b Realistic-Simulated Circuit for Figure 2.4a.

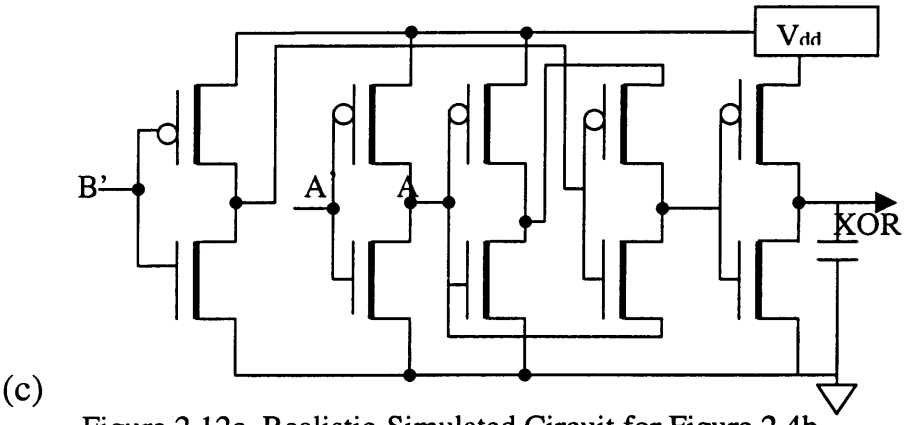

Figure 2.12c, Realistic-Simulated Circuit for Figure 2.4b.

(d)

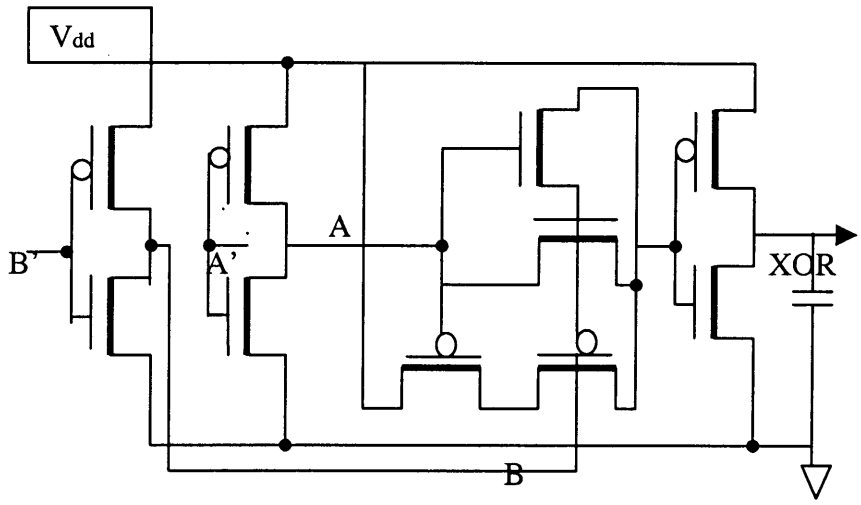

Figure 2.12d Realistic-Simulated Circuit for Figure 2.6.

2.6 Combination Circuit Design XOR/XNOR

Combination XOR/XNOR circuit designs are shown in Figures 2.M1, 2.M2, 2.M3, 2.M4, and 2.M5. The XOR/XNOR gates are given the structure names off full restored combination circuit design XOR/XNOR (Figure 2.M1), complementary pass gate logic (Figure 2.M2), complementary pass gate logic cross bar (Figure 2.M3), swing restored gate logic (Figure 2.M4), and full restored Combination circuit design XOR/XNOR with driving output (Figure 2.M5). A comparison of the advantages and disadvantages for the circuits in Figures 2.M1, 2.M2, 2.M3, 2.M4, and 2.M5 are shown on Table 2.1.

	Table 2.1 Circuit Comparison	
	Advantage	Disadvantage
Figure 2.M1	static gate for low power circuit design	slow circuit
Figure 2.M2	high speed and fewer stages of delay	body effect
Figure 2.M3	improved cross bar current	high power
Figure 2.M4	low standby current/less delay	less output drive
Figure 2.M5	more driving output	hard scaling

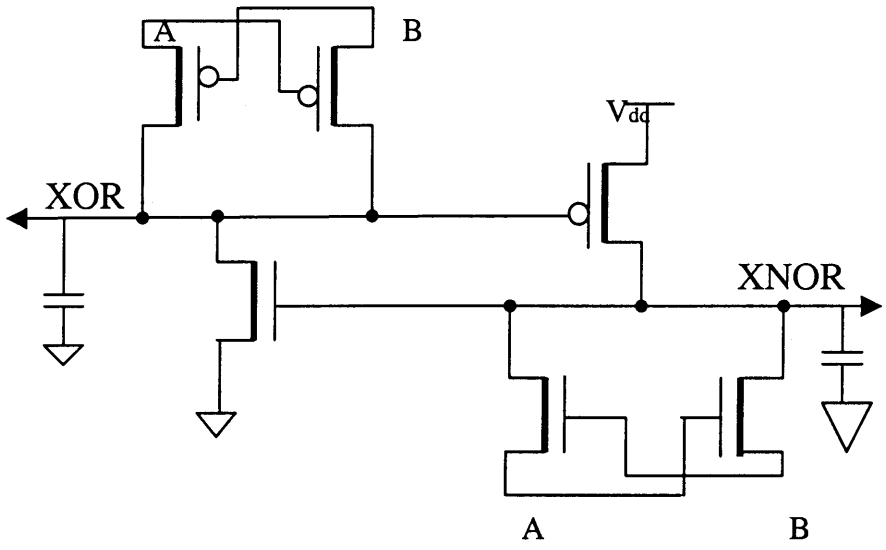

Figure 2.8/Figure 2.M1 Full Restored Combination Circuit Design XOR/XNOR (HSPICE and Mentor).

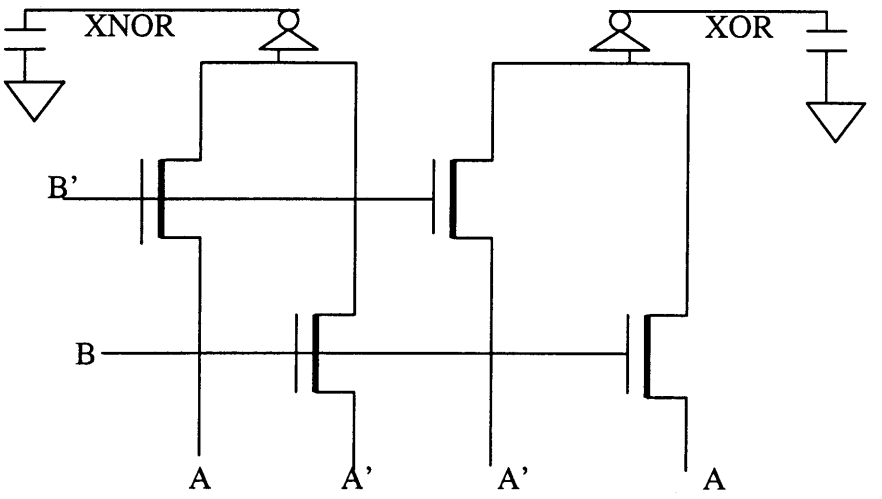

Figure 2.M2 Complementary Pass Gate Logic.

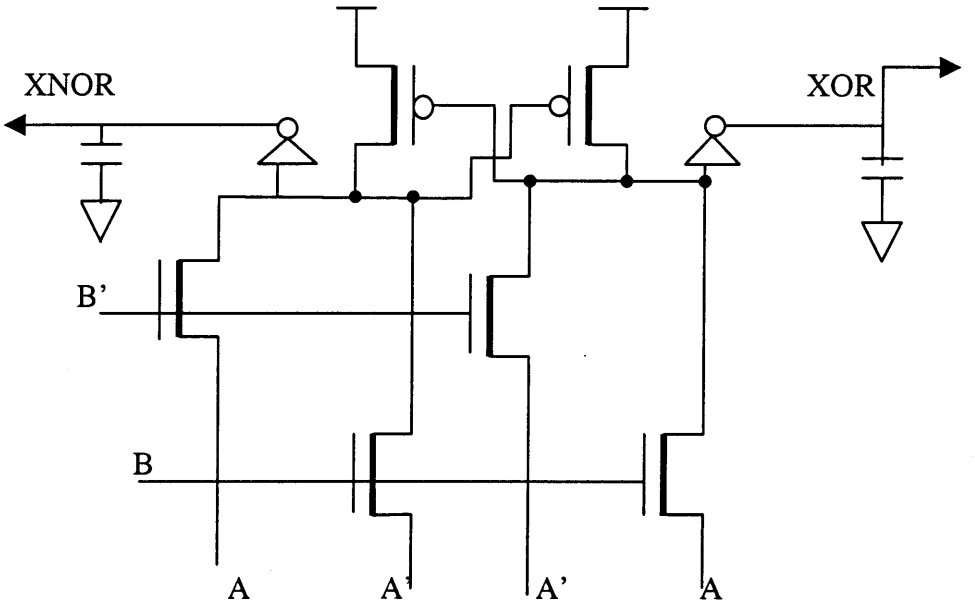

Figure 2.M3 Complementary Pass Gate Logic Cross Bar.

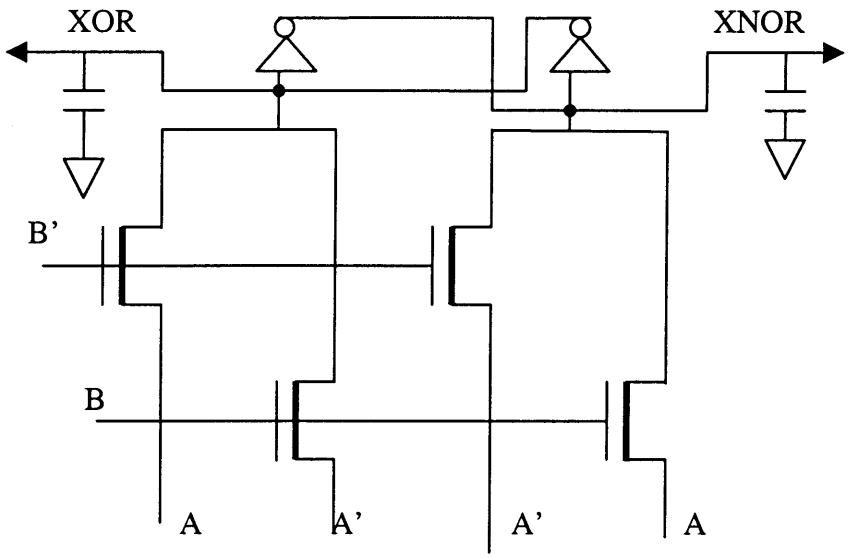

Figure 2.M4 Swing Restored Pass Gate Logic.

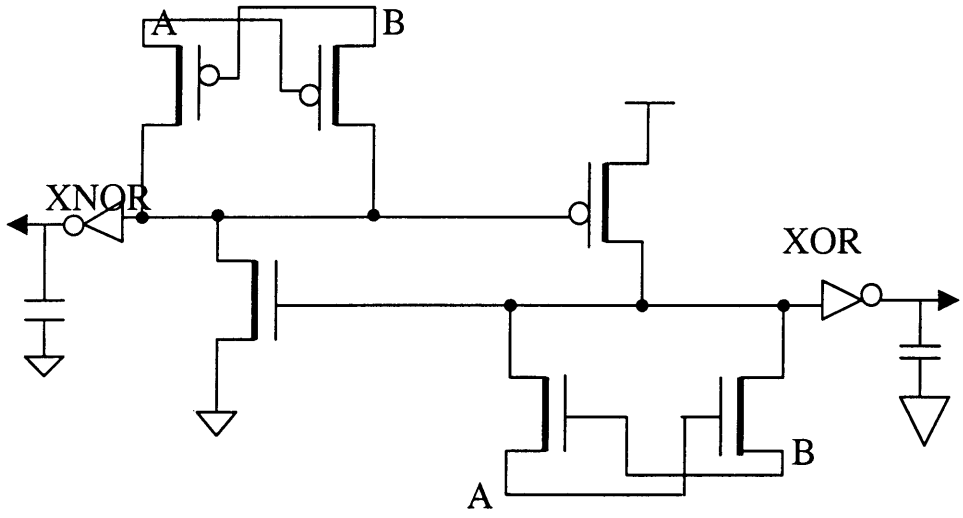

Figure 2.M5 Full Restored Combination Circuit Design XOR/XNOR Driving Output.

2.7 Basic Physical Layout Design of XOR/XNOR Gates

We will examine the physical layout of CMOS gates in a general sense to study the impact of the physical structure on the behavior of the circuit. These XOR/XNOR gates begin with an outline of **inverter** layout forms. To simplify layouts, "unit" sized transistors will generally be shown. In actual layouts, the correct dimension transistors would be arrived at via detailed circuit design. p-transistors will often be shown to be double in "unit" size. A symbolic layout style is used to show most layouts. Wires and transistors are arranged on a grid and actual layouts would space the grid proportionately to design results.

By examining the circuit diagram for the two inverters (Figure 2.3(a)), we should be able to lecture a physical layout by substituting layout symbols for the schematic symbols [5]. Any non-planar situation is dealt with by simply crossing two lines, i.e., the connection between the drain of the n-transistor and the drain of the p-transistor. However, in a physical layout, we have to concern ourselves with the interaction of physical different interconnection layers. We know from our consideration of the fabrication process that the source and drain of the n-transistor are n-diffusion regions and the p-transistor uses p-diffusion regions for these connections. Additionally in a bulk CMOS process we cannot make a direct connection from n-diffusion to p-diffusion. Thus we have to implement the simple inter-drain connection in the structural domain with at least one wire and two contacts in the physical domain. Assuming that the process does not have local interconnect or buried contacts, this connection has to be in metal.

Alternatively, if a metal line is to be passed from left to right at the top or bottom of the cell, the power and ground connections to the transistors may be made in the appropriate diffusion layer (Figure 2.3(a)-layout). This in effect makes the inverter transparent to horizontal metal connections that may have to be routed through the cell. From considerations that affect performance, the previous deviations from the original layout have little effect. In the case of a vertical poly-silicon drain connection, an extra connection resistance is incurred.

This would be approximately (2R-contact) + (R-poly) where R-contact is the resistance of a metal poly-silicon contact and R-poly is the resistance of the poly-silicon runner. Additionally, a slight extra capacitance may be incurred. Usually the result of both of these effects would be inconsequential. For the power and ground diffusion connections, the penalty is a series-connection resistance and increased capacitance. The layout designs developed are listed in Appendix D: Inverter-base XOR structure (Figure 2.3(a)), Inverter-base XNOR structure (Figure 2.3(b)), Inverter-base XNOR structure with driving output (Figure 2.3(a)), and Inverter-base XOR structure driving output (Figure 2.4(b)).

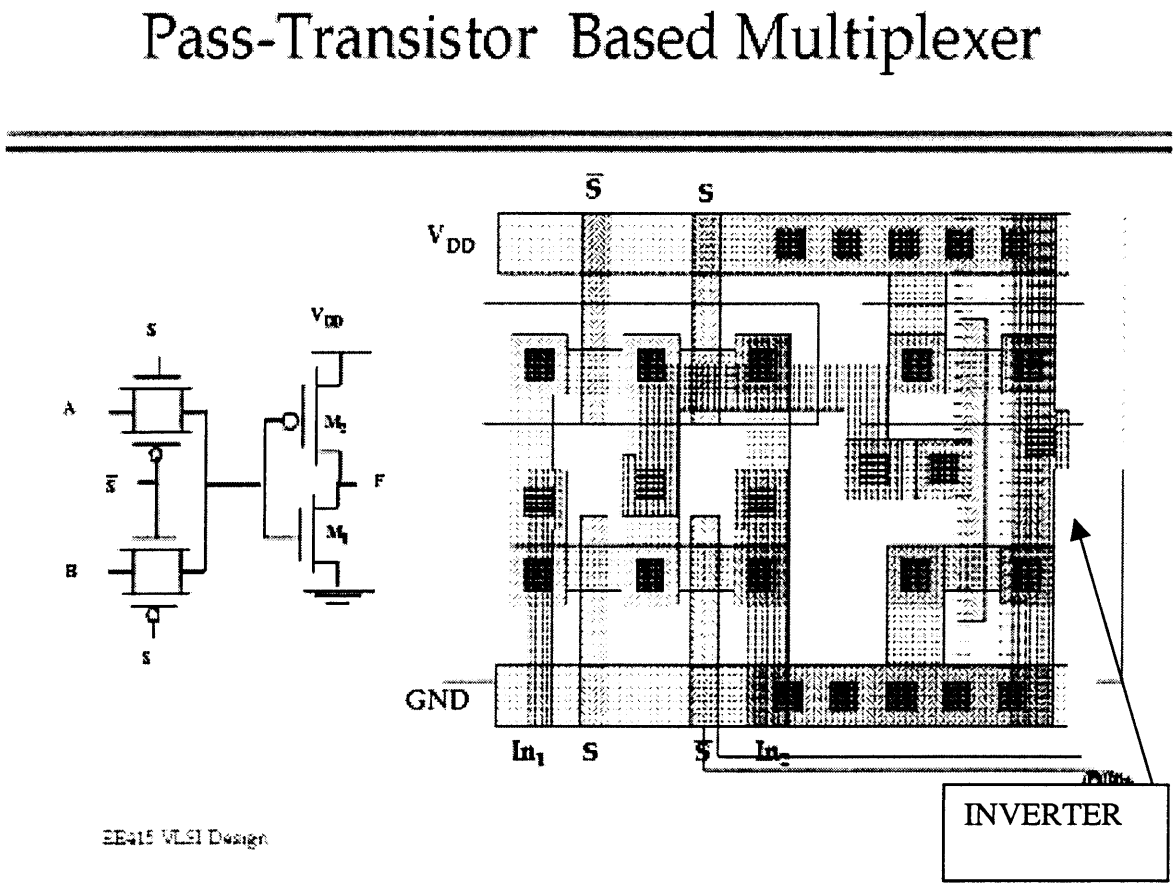

Figure 2.13, Layout Design of Figure 2.2

3.0 Results of Simulation

The process technology used is "CMOS TSMC" 0.35μm fabrication technology with parameters in CMOSN and CMOSP transistors listed in Appendix B in Table 1. The input signals depicted as the input signals A and B (Figure 3.1) cover four types of combinations; i.e., AB=00, AB=01, AB=10, and AB=11. The output simulation waveforms of the design results are shown in Figure 3.2 and Figure 3.3 where the worst case occurs on the both input signals AB=00. The output signal level in the XOR structure cannot sink to "LOW." In such a condition the poor signal level can still drive the next inverter stage correctly, as in the waveform in Figure 3.2 where the worst case happens on the both input signals AB = 11. The output signal level cannot pull-up to "HIGH", but is still able to make the next inverter stage work correctly.

The results can improve if the threshold value $|V_{th}|$ decreases. The lower $|V_{th}|$ is, the smaller the gap between the defect case and the normal case. In the Figure 3.2 and Figure 3.3, V_{nth} = 0.49 volt and V_{pth} = -0.66 volt as shown in Appendix B on Table 1. Figure 3.4 shows the simulation result of the proposed XOR structure with the same parameters as in Appendix B on Table 1 except decreasing the value of V_{nth} = 0.25 volt and V_{pth} = -0.36 volt. From the waveform shown in Figure 3.2 and Figure 3.4, it can be concluded that the smaller $|V_{th}|$ used, the better the performance achieved, such as increasing the signal level and decreasing the delay time.

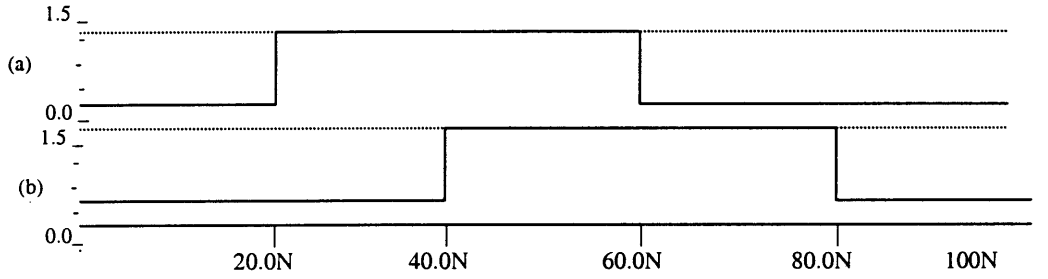

Figure 3.1 The input signal A and B.

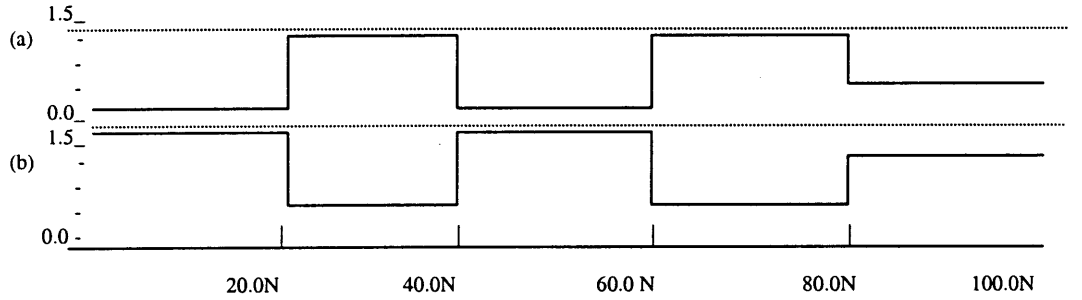

Figure 3.2 (a) The output of 4 transistors XOR and (b) 6 transistors XNOR.

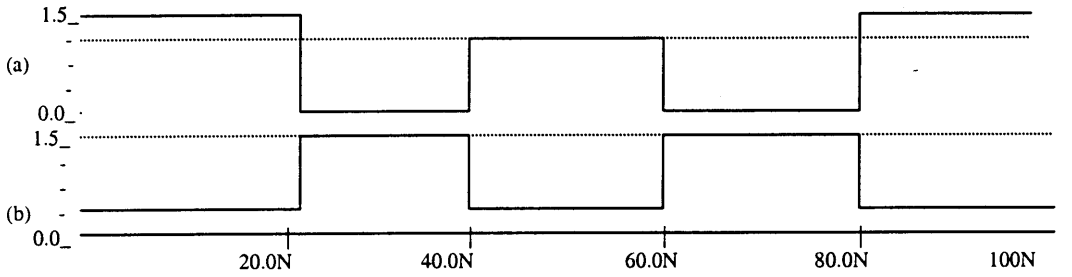

Figure 3.3 (a) The output of 4 transistors XNOR and (b) the 6 transistors XOR.

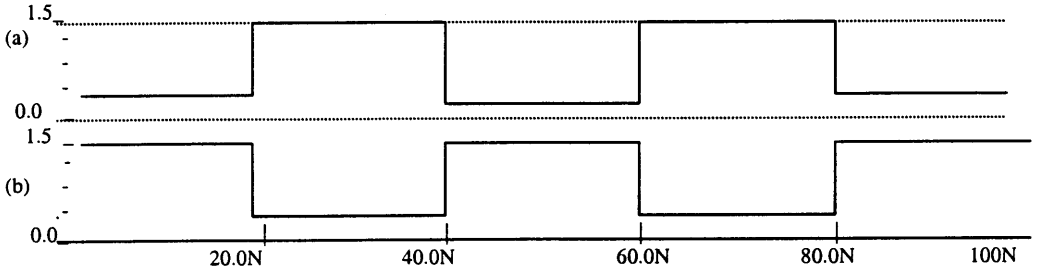

Figure 3.4 (a) The output of 4 transistors XOR and (b) the 6 transistors XNOR.

3.1 MOSFET Scaling

In MOSFET Scaling the threshold voltage should be decreased by the scaling factor "k" in proportion to the power supply voltage [9]. When the TSMC 0.35μm fabrication technology scales down the threshold voltage (V_{th}), it also needs to scale down physical dimensions as well. Table 3.2 lists the output simulation file of the transistor parameter model for CMOSN and CMOSP relating to the threshold voltage, sub threshold voltage, and mobility. Table 3.1 lists the generalized MOSFET Scaling theory. The circuit delay scales down by a factor between "k" and "f•k", depending on degree of velocity saturation. The most serious issue with generalized scaling is the increase of the power density by a factor of "f^{2}" to "f^{3}". The power density increase puts a great burden on VLSI packaging technology to dissipate the extra heat generated on the chip. The power delay product is also a factor of "f^{2}" higher than for constant field scaling.

Table 3.1

Generalized MOSFET Scaling Theory

MOSFET Device and Circuit Parameters			Multiplication Factor
			(k>1)
Scaling assumptions: Device dimensions			
	(T_{ox}, L, W, x_j)		1/k
Doping concentration (N_a, N_d)			f•k
	Voltage(V)		f/k
Derived scaling:	Electric field (E_{-field})		f
Behavior of device:	Depletion layer width (W_d)		1/k
Parameters:	Capacitance ($C = \epsilon A/t$)		1/k
	Inversion layer charge density (Q_i)		f
		Long channel	Velocity Saturation
	Carrier velocity	f	1
	Current, drift (I)	f^2/k	f/k
Derived scaling:	Circuit delay time (t_{au}~CV/I)	1/f•k	1/k
Behavior of circuit:	Power dissipation per circuit (p~VI)	f^3/k^2	f^2/k^2
Parameters:	Power delay product per circuit ($P•t_{au}$)	f^2/k^3	
	Circuit density (f•L/A)	k^2	
	Power density (P/A)	f^3	f^2

Table 3.2
Output simulation file of the transistor parameter model for
CMOSN and CMOSP, TSMC 0.25um fabrication technology

****

*** Threshold voltage related model parameters of CMOSP ***

****

VTH0 = -6.01E-01 V	DELVTO = 0 V	K1=5.85E-01 V^1/2
K2 = 1.48E-02	NCH = 4.16E+17 At/cm^3	K3= 0
K3B = 7.78E+0 1/V	DVTO = 2.35E+0	DVT1=7.16E-01
DVT2= -1.13E-01 1/V	DVTOW = 0	DVT1W= 0 1/m
DVT2W= 0 1/V	DSUB = 1.37E+0	ETA0 = 1
ETAB= -2.22E-01 1/V		

****

Sub threshold voltage related model parameters of CMOSP

****

NFACTOR = 1.15	CDSC = 2.4E-04 F/m^2	CDSCB =0
CDSCD = 0	VOFF = -1.19E-01 V	CIT = 0
PDIBLC1 = 1	PDIBLC2= 1.00E-02	PDIBLCB = 5.64E-21/V
DROUT = 9.31E-1	VSAT = 1.36E+05 m/s	PSCBE1= 3.21E8V/m
PSCBE2= 8.7E-8m/V	PRWB=-2E-1 V^-1/2	PRWG = 1.15E-1 1/V
RDSW = 2.86E+2	AGS = 3.01E-01 1/V	

****

*** Threshold voltage related model parameters of CMOSN ***

****

VTH0 = 4.1E-01 V	DELVTO = 0 V	K1 = 5E-1V^1/2
K2 = 1.46E-02	NCH=2.35E+17 At/cm^3	K3 = 1.00E-03
K3B = 7.78 1/V	DVTO = 0	DVT1=1.68E-03
DVT2= 5.00E-01 1/V	DVTOW = 0	DVT1W = 0 1/m
DVT2W= 0 1/V	DSUB = 1.47E+02	ETA0 = 1.09E-03
ETAB = 5.50E-05 1/V		

****

Sub threshold voltage related model parameters of CMOSN

****

NFACTOR = 1.09	CDSC = 2.4E-04 F/m^2	CDSCB =0
CDSCD = 0	VOFF = -1.05E-01 V	CIT = 0

****

Mobility related Model parameters CMOSN

****

UA =1.04E02	UB=1.27E10	UC=2.39E18(m/V)^2	11 m/V^2
U0 =3.92E			

4.0 Results of XOR Gates with HSPICE

Results of average delay, rising delay time, and falling delay time of the XOR gates are illustrated in Tables 4.1 and 4.2, respectively. When either signal A or signal B changes state due to propagation delay, the **ON** or **OFF** of the transmission gate element would not be fully synchronized to the first inverter in the XOR structure of the improved version XOR structure (Figure 4a). It results in both the NMOS transistor and the PMOS transistor turning on instantly. Comparisons of the XOR gates are summarized in Table 4.3. The competing factors are the number of transistors, the driving capability, non-complementary signal inputs, and the output signal levels. From Table 4.3, it is obvious that these designs are the most competitive ones among all methods. The measured average power dissipation of each XOR gates is shown in Table 4.4. For the data shown in Tables 4.1 to 4.4 and Figures 4.1 to 4.4, all the XOR gates are listed in the Figures 2.2, 2.4(a), 2.4(b), 2.6, and 2.7. These XOR gates have been fully simulated at the HSPICE Level 49 with TSMC 0.35μm fabrication technology.

Table 4.1 @2.5volt
Delay Time Analysis of Each XOR Structure at 2.5Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.2	1.14	0.95	1.21	1.09	1.10
Figure 2.4a	2.26	0.51	1.12	1.00	1.22
Figure 2.4b	2.88	3.0	1.07	1.09	2.01
Figure 2.6	1.15	0.66	1.08	0.38	0.85
Figure 2.8	1.45	1.31	1.35	1.17	1.32

Remark: 00->10: input signals AB change from 00 to 10, delay time = time difference between input transistor 50% level and the 50% output level. This is the time taken for a logic transition to pass from input to output.

Table 4.1 @2.0volt
Delay Time Analysis of Each XOR Structure at 2.0Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.2	0.74	1.05	1.31	1.19	1.20
Figure 2.4a	2.46	0.71	1.32	1.20	1.42
Figure 2.4b	2.98	3.20	1.17	1.39	2.18
Figure 2.6	1.45	0.86	1.28	0.58	1.04
Figure 2.8	1.65	1.51	1.55	1.37	1.52

Table 4.1 @1.5volt
Delay Time Analysis of Each XOR Structure at 1.5Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.2	1.44	1.25	1.51	1.39	1.40
Figure 2.4a	2.56	0.81	1.42	1.40	1.55
Figure 2.4b	3.08	3.32	1.97	1.79	2.54
Figure 2.6	1.55	1.06	1.48	0.78	1.22
Figure 2.8	1.75	1.61	1.65	1.47	1.72

Table 4.1 @1.0volt
Delay Time Analysis of Each XOR Structure at 1.0Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.2	1.74	1.55	1.81	1.69	1.71
Figure 2.4a	2.86	1.11	1.72	1.60	2.06
Figure 2.4b	3.28	3.70	2.17	1.99	2.78
Figure 2.6	1.85	1.36	1.78	0.88	1.46
Figure 2.8	2.15	2.01	2.05	1.87	2.11

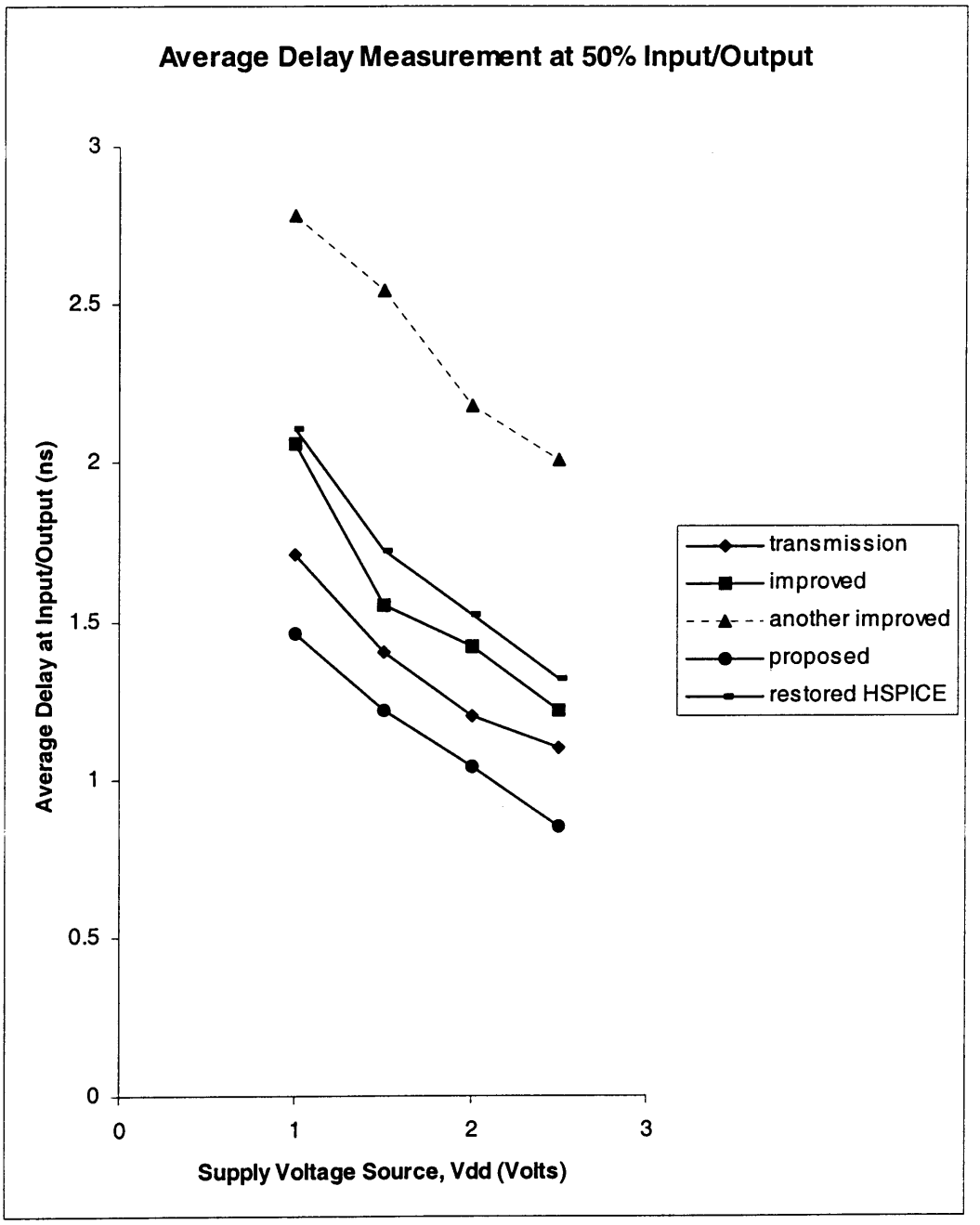

Figure 4.1 Average Delay

Table 4.2 @2.5volt
Rising/Falling Time Analysis of Each XOR Structure at 2.5volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.2	2.1	1.46	2.09	1.5	2.1	1.48
Figure 2.4a	4.79	3.11	3.86	2.65	4.33	2.88
Figure 2.4b	6.94	2.96	2.1	1.49	4.52	2.23
Figure 2.6	2.1	0.98	2.22	0.26	2.11	0.62
Figure 2.8	2.79	4.65	2.61	4.51	2.70	4.58

Remark: Rising time = time for a waveform to rise from 10% to 90% of its Steady-state value.
Falling time: time for a waveform to fall from 90% to 10% of its Steady-state value.

Table 4.2 @2.0volt
Rising/Falling Time Analysis of Each XOR Structure at 2.0volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.2	2.20	1.66	2.19	1.70	2.2	1.67
Figure 2.4a	4.89	3.31	3.96	2.85	4.43	3.08
Figure 2.4b	7.04	3.16	2.21	1.69	4.62	2.44
Figure 2.6	2.2	1.18	2.32	0.46	2.21	0.82
Figure 2.8	2.89	4.85	2.70	4.71	2.81	4.78

Table 4.2 @1.5volt
Rising/Falling Time Analysis of Each XOR Structure at 1.5volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.2	2.40	1.76	2.39	1.80	2.41	1.77
Figure 2.4a	5.09	3.41	4.16	2.95	4.63	3.18
Figure 2.4b	7.24	3.26	2.41	1.79	4.82	2.54
Figure 2.6	2.41	1.28	2.52	0.56	2.41	0.92
Figure 2.8	3.10	4.95	2.90	4.81	3.02	4.88

Table 4.2 @1.0volt
Rising/Falling Time Analysis of Each XOR Structure at 1.0volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.2	2.60	1.96	2.59	2.00	2.61	1.97
Figure 2.4a	5.29	3.61	4.36	3.15	4.83	3.38
Figure 2.4b	7.44	3.46	2.61	1.99	5.02	2.74
Figure 2.6	2.61	1.48	2.72	0.76	2.61	1.12
Figure 2.8	3.30	5.15	3.10	5.01	3.22	5.08

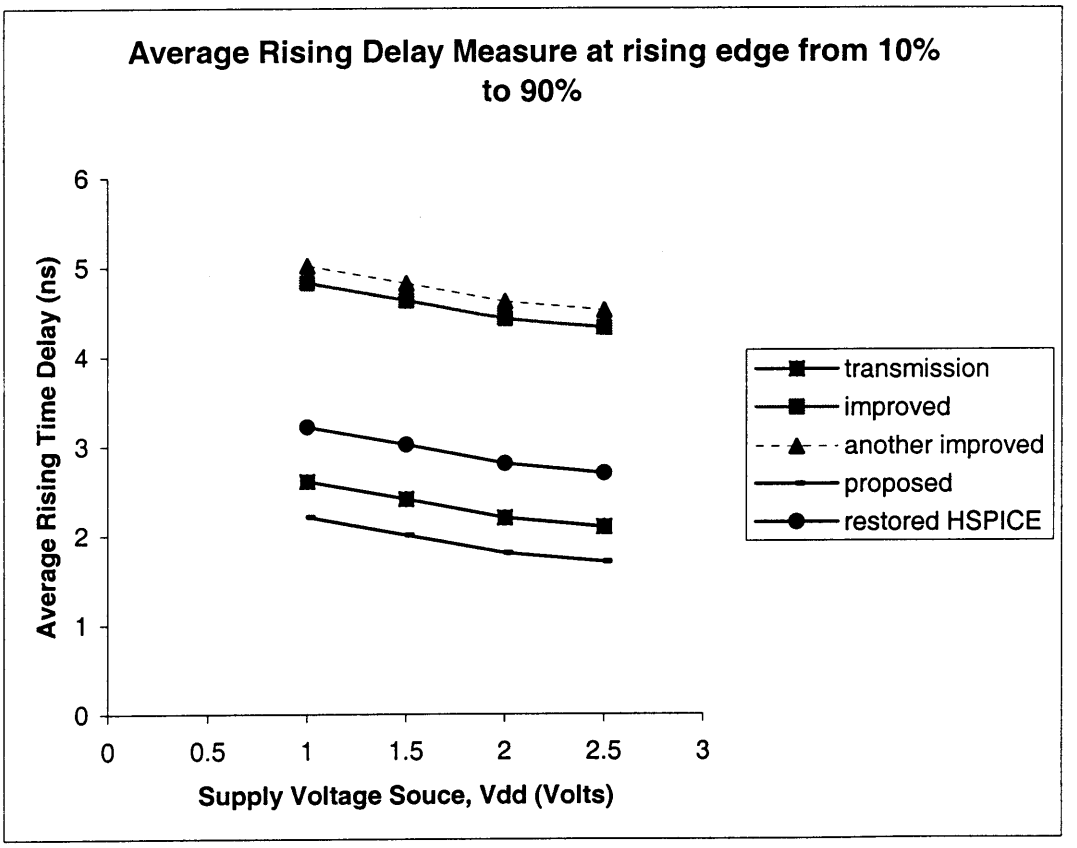

Figure 4.2 Average Rising Delay

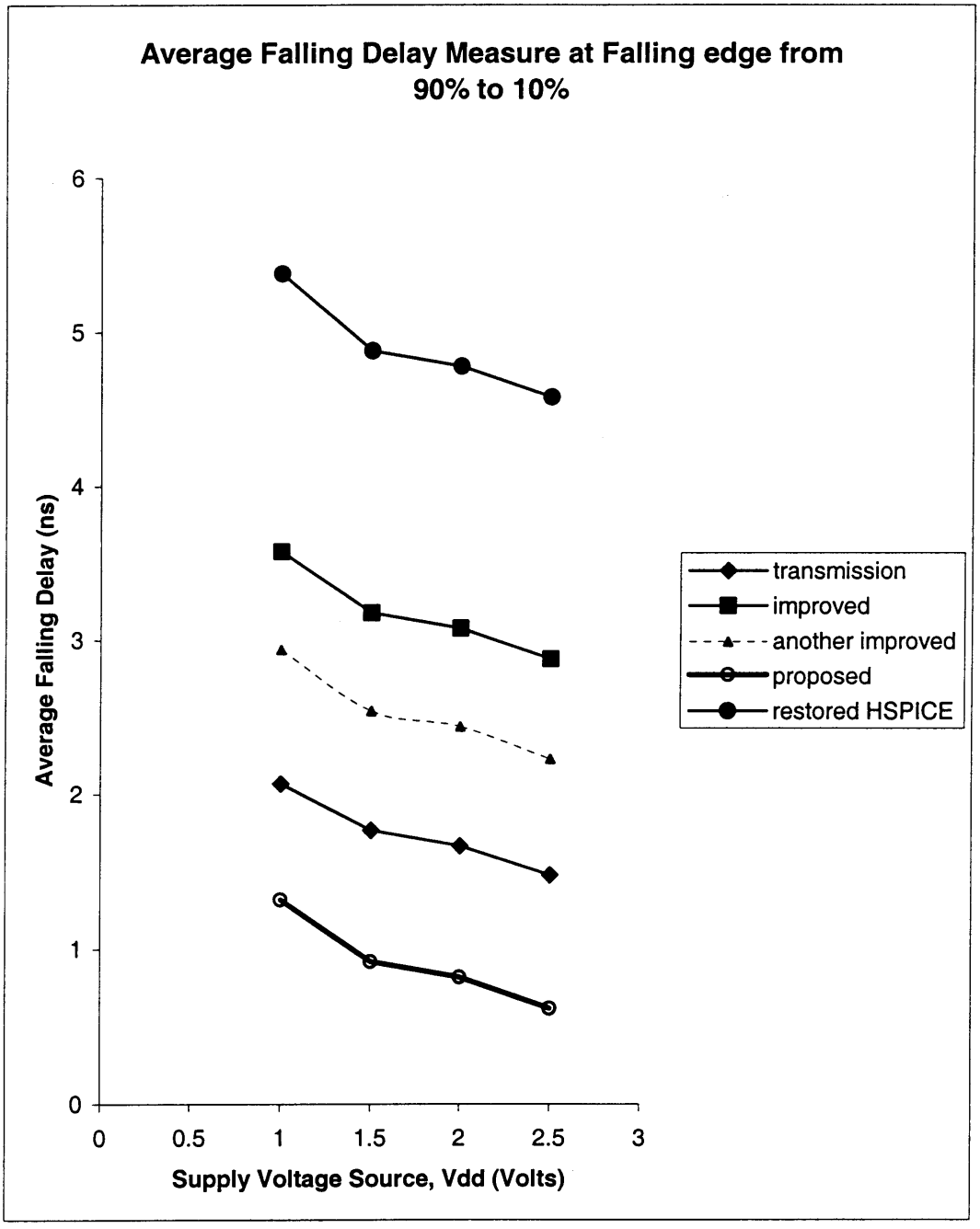

Figure 4.3 Average Falling Delay

Table 4.3
Comparison of Each XOR Function

	00	01	10	11	#Tr	Driving Output	Complement Output
Figure 2.1	O	O	O	O	4	No	Yes
Figure 2.2	O	O	O	O	6	better	Yes
Figure 2.3	X	X	O	O	4	No	No
Figure 2.4a	O	O	O	O	6	good	No
Figure 2.4b	O	O	A	O	6	worse	No
Figure 2.5	O	O	O	X	4	No	No
Figure 2.6	O	O	O	O	6	best	No
Figure 2.8	O	O	O	O	6	No	No

Symbols: AB= 00, 01, 10, 11. #Tr is number of transistors, O is good
X is poor signal level. A is nearly good signal level.

Table 4.4
Average Power Dissipation from 0 through 100ns of XOR Gates

Unit: uW,	Power@1v,	Power@1.5v,	Power@2v,	Power@2.5v,	Power@2.5v/Vth
Figure 2.2	15.21uW	30.42uW	40.92uW	62.98uW	68.98uW
Figure 2.4a	5.20uW	19.40uW	30.90uW	43.91uW	47.92uW
Figure 2.4b	8.41uW	15.63uW	26.13uW	53.13uW	58.23uW
Figure 2.6	7.31uW	12.53uW	20.03uW	48.03uW	53.09uW
Figure 2.8	15.32uW	30.52uW	45.02uW	70.02uW	76.03uW

Power Dissipation Equation measure from HSPICES:

```
.meas tran  avg_curr  avg I(Vdd)  from = 2.0ns  to = 100.0ns
.meas   avg_power  param = ' -avg_curr*Vdd'
```

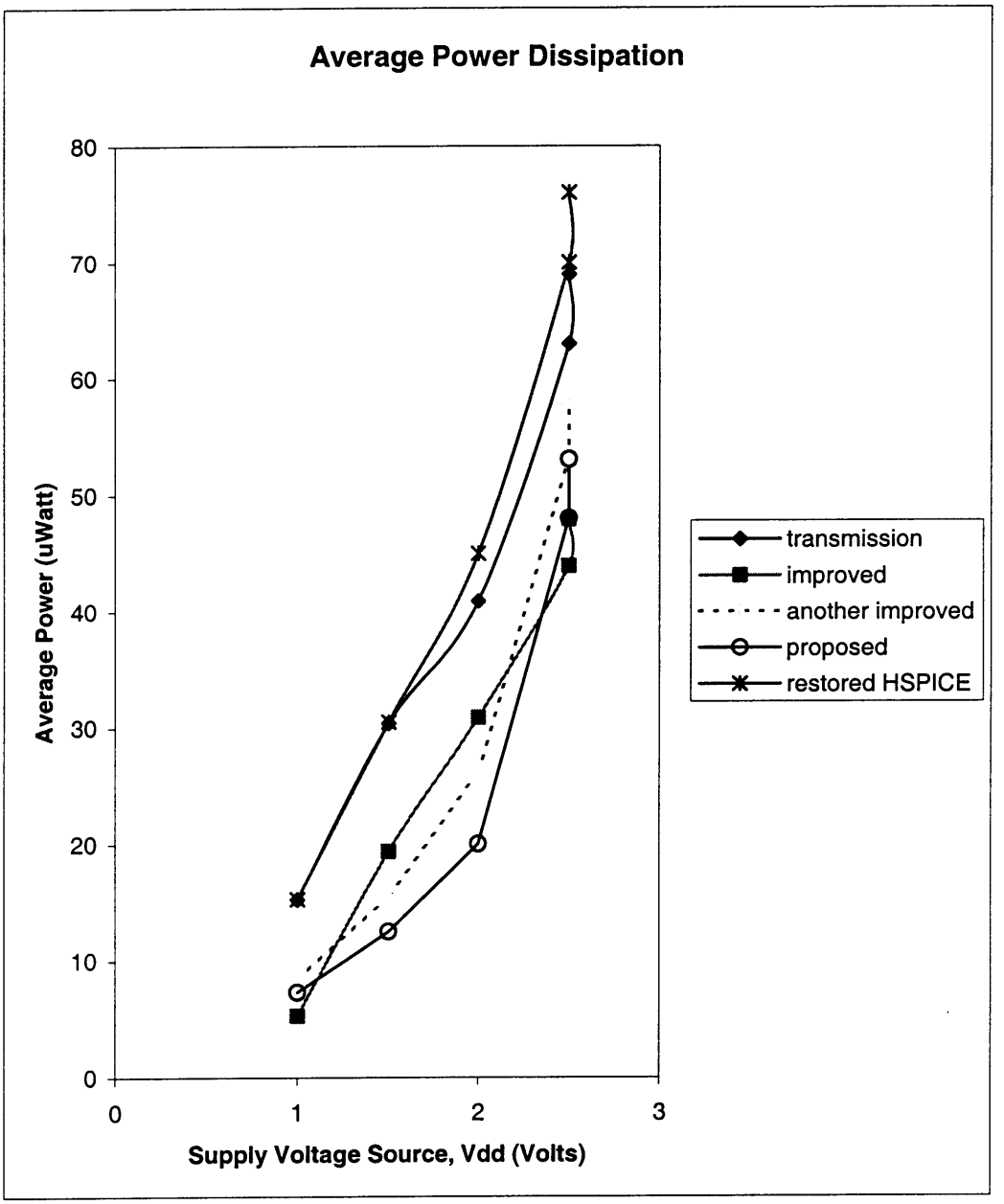

Figure 4.4 Average Power Dissipation

(Note: Two marks at V_{dd} = 2.5 volt was shown on the chart, for the bottom mark is simulated at V_{dd} = 2.5 volt and the top mark is simulated with decreased threshold voltage)

4.1 Results of XOR Gates with Mentor Graphics

Results of average delay, rising delay time, and falling delay time of XOR gates are listed in Table 4.5 and 4.6. The comparison of each XOR gate is summarized in Table 4.7. The average power dissipation of each XOR gate is summarized in Table 4.8. Charts for data analysis are shown in Table 4.5 to 4.8. For the data shown in Tables 4.5 to 4.8 and Figures 4.5 to 4.8, all the XOR gates are listed in the Figures 2.M1, 2.M2, 2.M3, 2.M4, and 2.M5. These XOR gates have been fully simulated at the Mentor Graphics Level 53 with TSMC 0.25μm fabrication technology.

Table 4.5 @2.5volt with scale V_{th}

Delay Time Analysis of Each XOR Structure at 2.5Volt with scale V_{th}

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.M1/Vth	1.80	2.01	1.97	2.00	1.94
Figure 2.M2/Vth	3.09	3.98	3.71	4.01	3.69
Figure 2.M3/Vth	1.21	1.41	1.22	1.39	1.31
Figure 2.M4/Vth	0.15	0.16	0.28	0.08	0.22
Figure 2.M5/Vth	2.50	2.40	2.50	2.40	2.45

Remark: 00->10: Input signals AB change from 00 to 10, delay time = time difference between input transistor 50% level and the 50% output level. This is the time taken for a logic transition to pass from input to output.

Table 4.5 @2.5volt

Delay Time Analysis of Each XOR Structure at 2.5Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.M1	2.20	2.21	2.27	2.43	2.03
Figure 2.M2	3.29	4.18	3.91	4.21	4.04
Figure 2.M3	1.41	1.61	1.42	1.59	1.51
Figure 2.M4	0.35	0.26	0.38	0.28	0.31
Figure 2.M5	2.80	2.70	2.80	2.70	2.75

Table 4.5 @2.0volt
Delay Time Analysis of Each XOR Structure at 2.0Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.M1	2.50	2.41	2.57	2.73	2.33
Figure 2.M2	3.49	4.38	4.11	4.41	4.24
Figure 2.M3	1.61	1.81	1.62	1.79	1.71
Figure 2.M4	0.65	0.56	0.68	0.58	0.60
Figure 2.M5	2.90	2.80	2.90	2.80	2.85

Table 4.5 @1.5volt
Delay Time Analysis of Each XOR Structure at 1.5Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.M1	2.80	2.71	2.87	3.03	2.63
Figure 2.M2	3.79	4.58	4.31	4.61	4.32
Figure 2.M3	1.81	2.01	1.82	1.99	1.91
Figure 2.M4	0.75	0.66	0.78	0.64	0.72
Figure 2.M5	3.00	3.10	3.00	3.10	3.05

Table 4.5 @1.0volt
Delay Time Analysis of Each XOR Structure at 1.0Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.M1	3.10	3.01	3.17	3.33	3.15
Figure 2.M2	3.99	4.88	4.61	4.81	4.57
Figure 2.M3	2.11	2.31	2.12	2.19	2.20
Figure 2.M4	1.05	0.96	1.08	0.94	1.02
Figure 2.M5	3.20	3.30	3.20	3.30	3.25

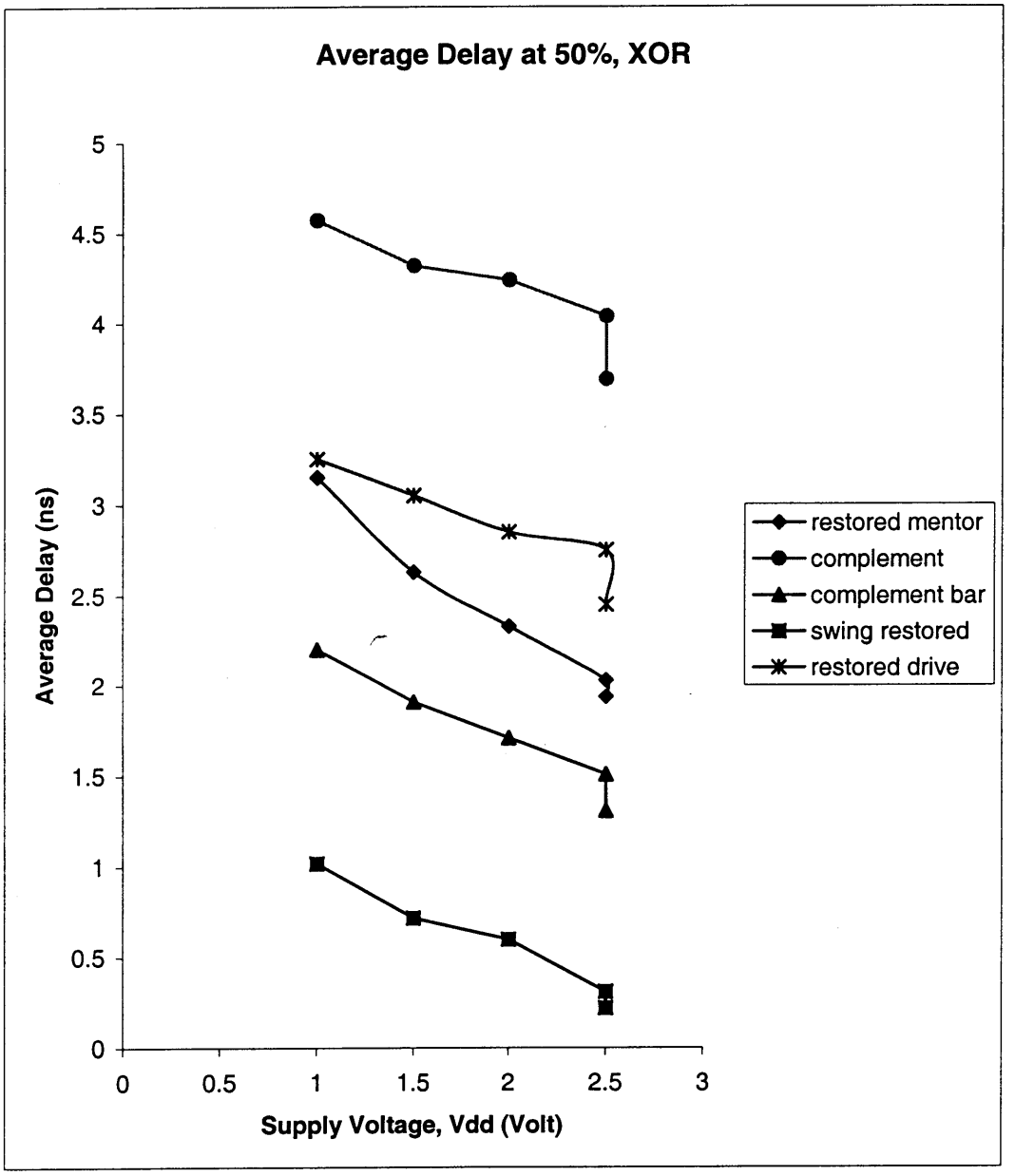

Figure 4.5 Average Delay XOR Gates

(Note: Two marks at V_{dd} = 2.5 volt was shown on the chart, for the bottom mark is simulated at V_{dd} = 2.5 volt and the top mark is simulated with decreased threshold voltage)

Table 4.6 @2.5volt with scale V_{th}

Rising/Falling Time Analysis of Each XOR Structure at 2.5volt with scale V_{th}

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.M1/Vth	2.30	2.73	2.31	2.74	2.31	2.74
Figure 2.M2/Vth	3.90	4.38	3.92	4.40	3.91	4.39
Figure 2.M3/Vth	1.40	1.63	1.42	1.64	1.41	1.63
Figure 2.M4/Vth	0.28	0.50	0.30	0.52	0.22	0.51
Figure 2.M5/Vth	2.80	2.70	2.80	2.70	2.80	2.70

Remark: Rising time = time for a waveform to rise from 10% to 90% of its Steady-state value.
Falling time: time for a waveform to fall from 90% to 10% of its Steady-state value.

Table 4.6 @2.5volt

Rising/Falling Time Analysis of Each XOR Structure at 2.5volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.M1	2.50	2.93	2.51	2.94	2.51	2.94
Figure 2.M2	4.10	4.58	4.12	4.60	4.11	4.59
Figure 2.M3	1.60	1.83	1.62	1.84	1.61	1.83
Figure 2.M4	0.58	0.80	0.60	0.82	0.52	0.81
Figure 2.M5	4.50	3.51	4.50	3.51	4.50	3.51

Table 4.6 @2.0volt

Rising/Falling Time Analysis of Each XOR Structure at 2.0volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.M1	2.75	3.18	2.76	3.19	2.76	3.18
Figure 2.M2	4.40	4.88	4.42	4.90	4.31	4.89
Figure 2.M3	1.80	2.03	1.82	2.04	1.81	2.03
Figure 2.M4	0.78	2.00	0.80	1.02	0.72	1.01
Figure 2.M5	4.70	3.71	4.60	3.71	4.65	3.71

Table 4.6 @1.5volt
Rising/Falling Time Analysis of Each XOR Structure at 1.5volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.M1	2.96	3.48	2.97	3.49	2.97	3.48
Figure 2.M2	4.60	5.08	4.62	5.10	4.61	5.09
Figure 2.M3	2.01	2.33	2.02	2.34	2.02	2.33
Figure 2.M4	0.98	2.30	1.00	1.32	0.92	1.81
Figure 2.M5	4.95	3.94	5.00	3.96	4.97	3.95

Table 4.6 @1.0volt
Rising/Falling Time Analysis of Each XOR Structure at 1.0volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.M1	3.16	3.78	3.37	3.89	3.27	3.84
Figure 2.M2	5.10	5.58	5.12	5.50	5.11	5.59
Figure 2.M3	2.61	3.03	2.62	3.04	2.62	3.03
Figure 2.M4	1.68	2.90	1.60	1.92	1.52	2.41
Figure 2.M5	5.20	4.10	5.30	4.20	5.25	4.15

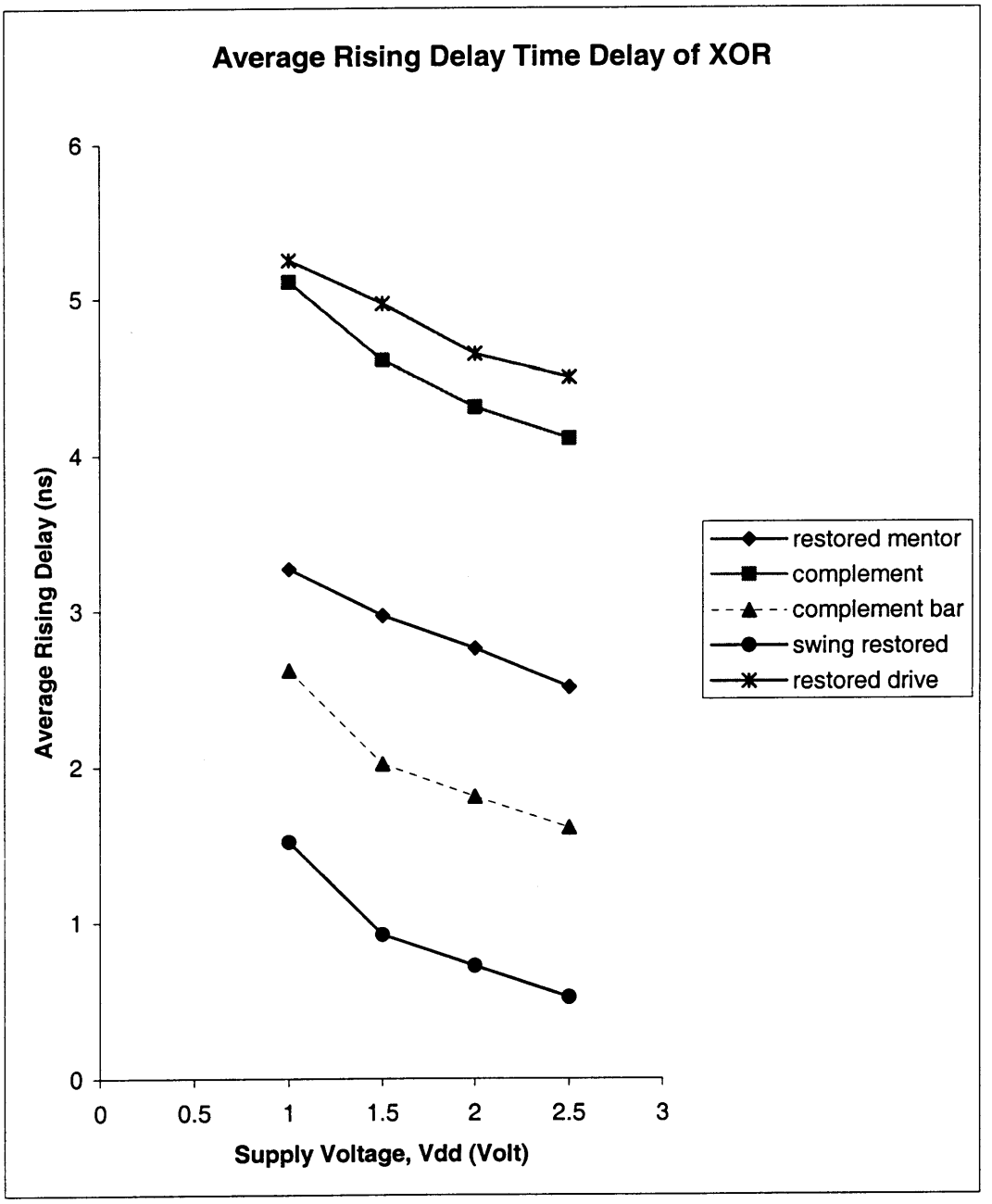

Figure 4.6 Average Rising Delay XOR Gates

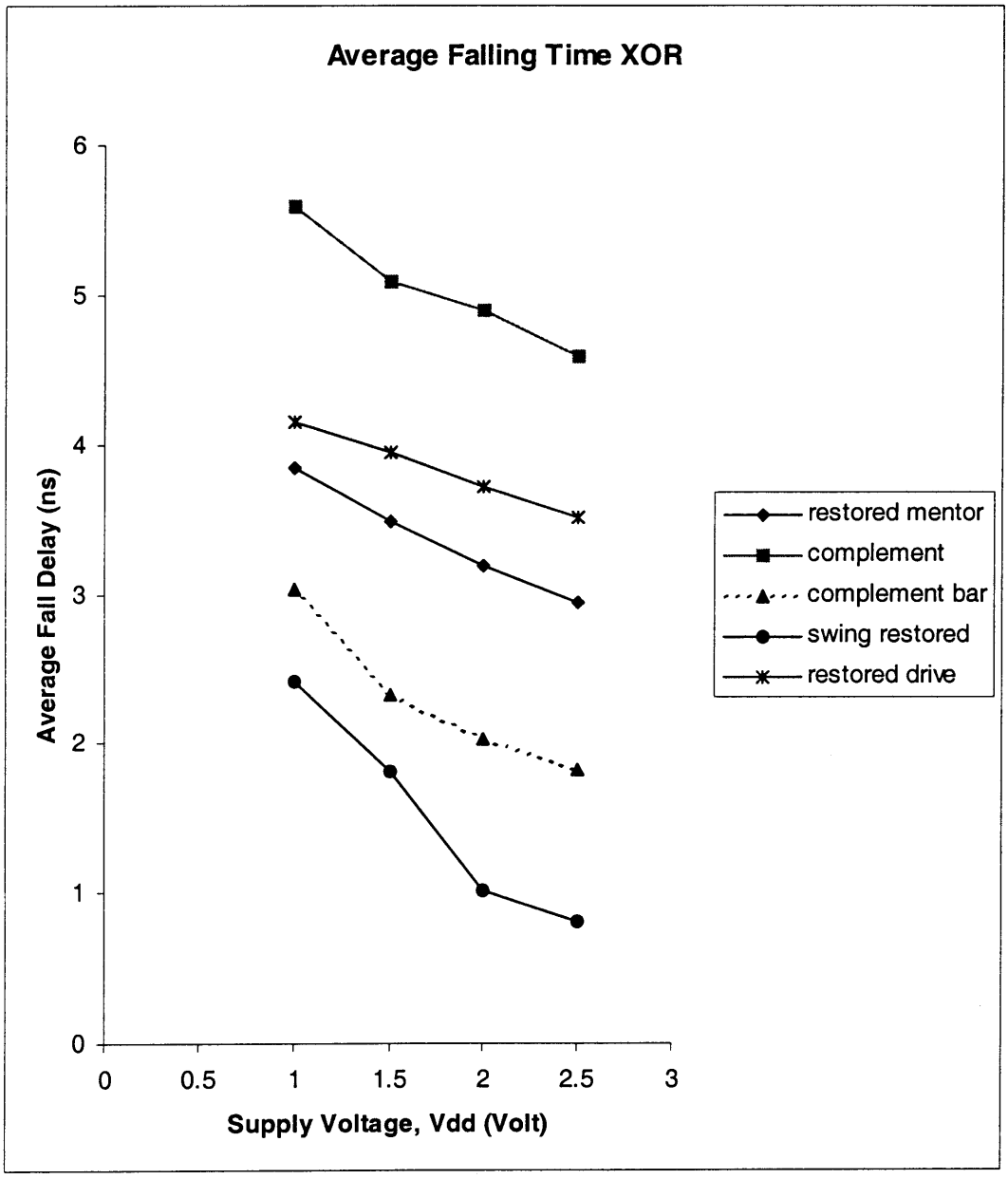

Figure 4.7 Average Falling Delay XOR

Table 4.7

Comparison of Each XOR Function

	00	01	10	11	#Tr	Driving Output	Complement Output
Figure 2.M1	O	O	O	O	6	No	No
Figure 2.M2	O	O	O	O	8	best	No
Figure 2.M3	O	A	O	O	10	best	No
Figure 2.M4	O	A	O	O	8	best	No
Figure 2.M5	O	O	O	O	10	best	Yes

Symbols: AB= 00, 01, 10, 11. #Tr is number of transistors, O is good signal level. X is poor signal level. A is nearly good signal level.

Table 4.8
Average Power Dissipation from 0 through 100ns XOR Gates

Unit: uW,	Power@1v	Power@1.5v	Power@2v	Power@2.5v	Power@2.5v V_{th}
Figure 2.M1	143.77uW	157.88uW	175.44uW	185.11uW	187.45uW
Figure 2.M2	27.28uW	38.40uW	49.67uW	62.25uW	67.54uW
Figure 2.M3	98.78uW	148.20uW	197.67uW	247.00uW	252.90uW
Figure 2.M4	13.00uW	19.50uW	26.00uW	32.50uW	37.50uW
Figure 2.M5	69.76uW	104.64uW	139.52uW	174.40uW	202.30uW

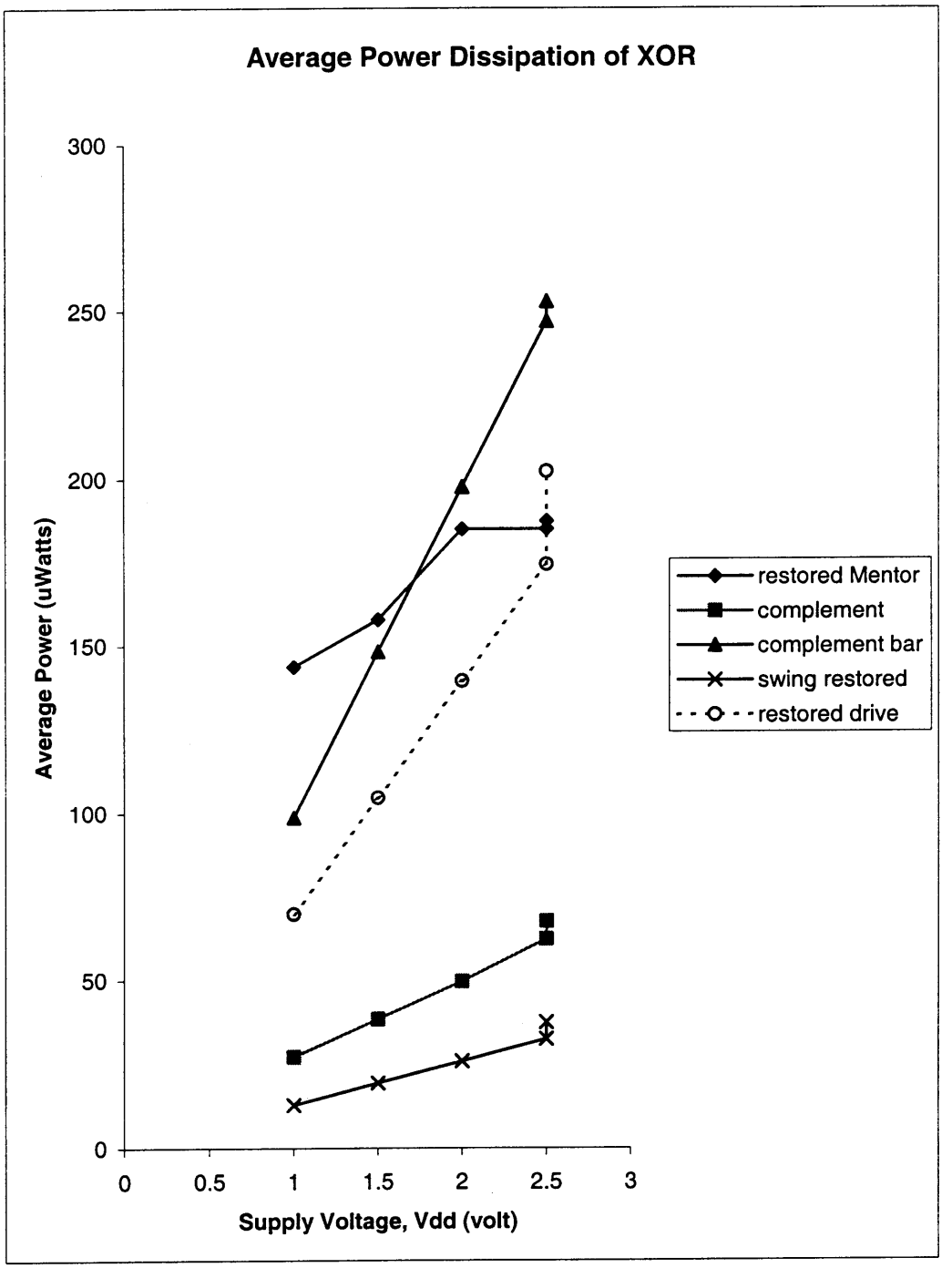

Figure 4.8 Average Power Dissipation XOR Gates

4.2 Results XNOR Gates with Mentor Graphics

Results of average delay, rising delay time, and falling delay time of **XNOR** gates in Table 4.9 and 4.10. The comparison of each XNOR gate is summarized in Table 4.11. The average power dissipation of each XNOR gates is summarized in Table 4.12. All the XNOR gates are shown in the Figures 2.M1, 2.M2, 2.M3, 2.M4, and 2.M5. These XNOR gates have been fully simulated on the Mentor Graphics Level 53 with TSMC 0.25μm fabrication technology.

Table 4.9@2.5volt with scale V_{th}
Delay Time Analysis of Each XNOR Structure at 2.5Volt with scale V_{th}

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.M1/V_{th}	1.11	1.08	1.37	1.43	1.24
Figure 2.M2/V_{th}	2.26	2.15	1.48	1.37	1.81
Figure 2.M3/V_{th}	2.51	2.52	1.33	1.34	1.92
Figure 2.M4/V_{th}	0.07	0.06	1.11	1.11	0.58
Figure 2.M5/V_{th}	2.50	2.40	2.50	2.40	2.45

Remark: 00->10: Input signals AB change from 00 to 10, delay time = time difference between input transistor 50% level and the 50% output level. This is the time taken for a logic transition to pass from input to output.

Table 4.9@2.5volt
Delay Time Analysis of Each XNOR Structure at 2.5Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.M1	1.21	1.18	1.47	1.53	1.34
Figure 2.M2	2.36	2.25	1.58	1.47	1.91
Figure 2.M3	2.61	2.62	1.63	1.64	2.22
Figure 2.M4	0.17	0.16	1.21	1.21	0.68
Figure 2.M5	2.80	2.70	2.80	2.70	2.75

Table 4.9@2.0volt
Delay Time Analysis of Each XNOR Structure at 2.0Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.M1	1.40	1.31	1.67	1.73	1.53
Figure 2.M2	2.56	2.45	2.78	1.67	2.11
Figure 2.M3	2.81	2.82	1.83	1.84	2.42
Figure 2.M4	0.37	0.36	1.81	1.81	1.28
Figure 2.M5	2.90	2.80	2.90	2.80	2.85

Table 4.9 @1.5volt
Delay Time Analysis of Each XNOR Structure at 1.5Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.M1	1.70	1.61	1.97	2.03	1.83
Figure 2.M2	3.16	3.05	2.98	2.27	2.87
Figure 2.M3	3.31	3.32	2.23	2.24	2.82
Figure 2.M4	0.87	0.86	1.91	1.91	1.38
Figure 2.M5	3.00	3.10	3.00	3.10	3.05

Table 4.9@1.0volt
Delay Time Analysis of Each XNOR Structure at 1.0Volt

Unit: ns	00->10	10->11	11->01	01->00	Average
Figure 2.M1	2.20	2.11	2.47	2.53	2.33
Figure 2.M2	3.66	3.55	3.20	2.57	3.24
Figure 2.M3	3.81	3.82	2.73	2.74	3.32
Figure 2.M4	1.37	1.36	2.41	2.41	1.88
Figure 2.M5	3.20	3.30	3.20	3.30	3.25

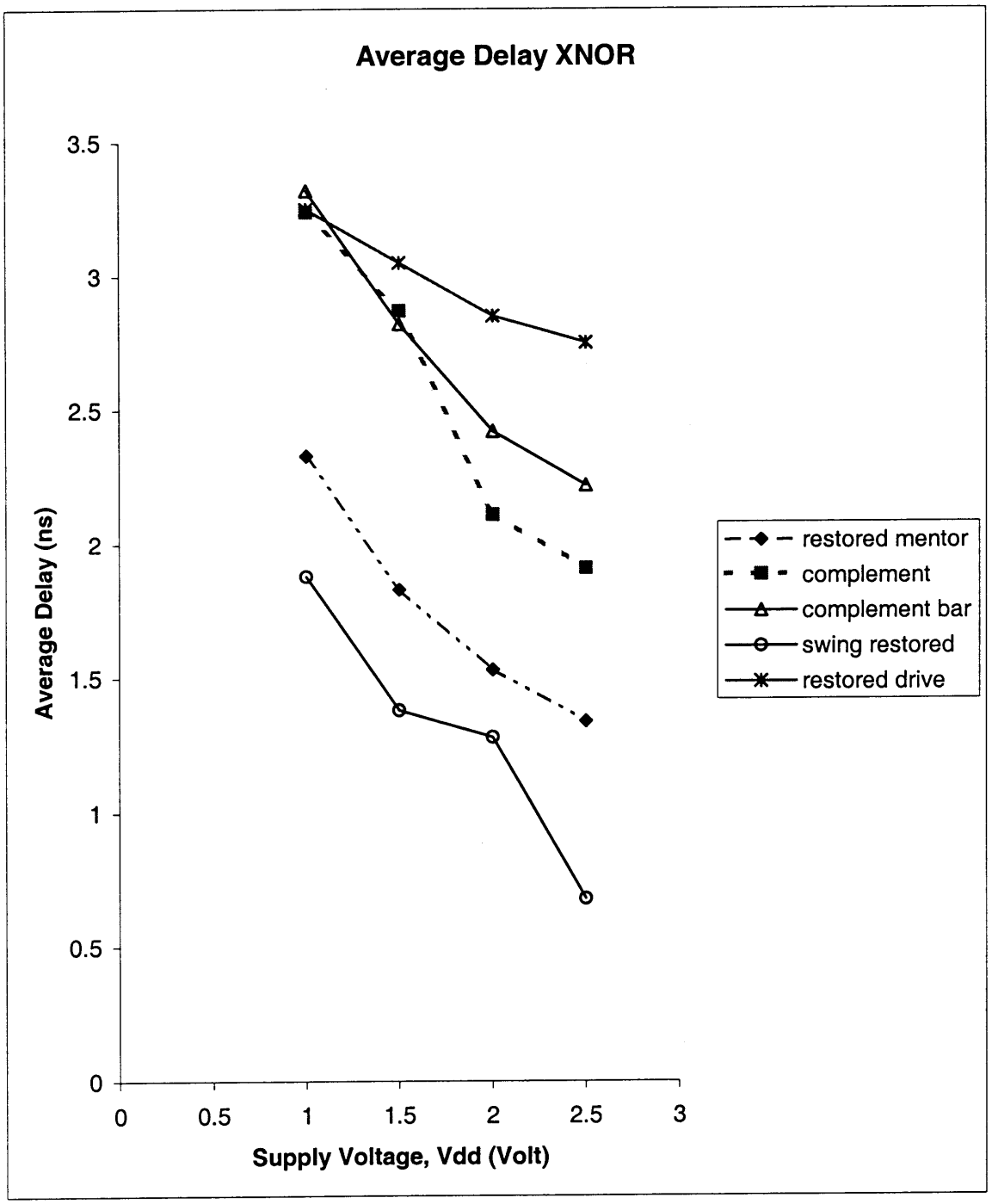

Figure 4.9 Average Delay XNOR Gates

Table 4.10 @2.5volt with scale V_{th}

Rising/Falling Time Analysis of Each XNOR Structure at 2.5volts with scale V_{th}

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.M1/V_{th}	1.70	1.83	1.81	1.84	1.75	1.84
Figure 2.M2/V_{th}	1.89	2.61	1.87	2.51	1.88	2.56
Figure 2.M3/V_{th}	1.40	1.63	1.42	1.64	1.41	1.63
Figure 2.M4/V_{th}	0.28	0.50	0.30	0.52	0.22	0.51
Figure 2.M5/V_{th}	2.80	2.70	2.80	2.70	2.80	2.70

Remark: Rising time = time for a waveform to rise from 10% to 90% of its Steady-state value.
Falling time: time for a waveform to fall from 90% to 10% of its Steady-state value.

Table 4.10 @2.5volt

Rising/Falling Time Analysis of Each XNOR Structure at 2.5volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.M1	1.90	2.03	1.91	2.04	1.90	2.04
Figure 2.M2	2.06	2.81	2.07	2.81	2.06	2.81
Figure 2.M3	1.70	2.93	1.74	2.94	1.73	2.93
Figure 2.M4	1.41	0.87	1.40	0.88	1.41	0.87
Figure 2.M5	4.50	3.51	4.50	3.51	4.50	3.51

Table 4.10 @2.0volt

Rising/Falling Time Analysis of Each XNOR Structure at 2.0volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.M1	2.20	2.33	2.21	2.34	2.20	2.34
Figure 2.M2	2.46	3.11	2.47	3.11	2.46	3.11
Figure 2.M3	2.00	3.23	2.04	3.24	2.03	3.23
Figure 2.M4	1.71	1.17	1.70	1.18	1.71	1.17
Figure 2.M5	4.70	3.71	4.60	3.71	4.65	3.71

Table 4.10@1.5volt
Rising/Falling Time Analysis of Each XNOR Structure at 1.5volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.M1	2.60	2.73	2.61	2.74	2.60	2.74
Figure 2.M2	2.86	3.51	2.87	3.41	2.86	3.46
Figure 2.M3	2.50	3.63	2.54	3.64	2.53	3.63
Figure 2.M4	1.91	1.50	1.90	1.49	1.91	1.49
Figure 2.M5	4.95	3.94	5.00	3.96	4.97	3.95

Table 4.10 @1.0volt
Rising/Falling Time Analysis of Each XNOR Structure at 1.0volt

Unit: ns	00->10 Rising	10->11 Falling	11->01 Rising	01->00 Falling	Average Rising	Average Falling
Figure 2.M1	2.90	3.03	2.91	3.04	2.90	3.04
Figure 2.M2	3.06	3.71	3.07	3.61	3.06	3.66
Figure 2.M3	2.90	4.03	2.94	4.04	2.93	4.03
Figure 2.M4	2.41	1.70	1.30	2.28	2.31	1.98
Figure 2.M5	5.20	4.10	5.30	4.20	5.25	4.15

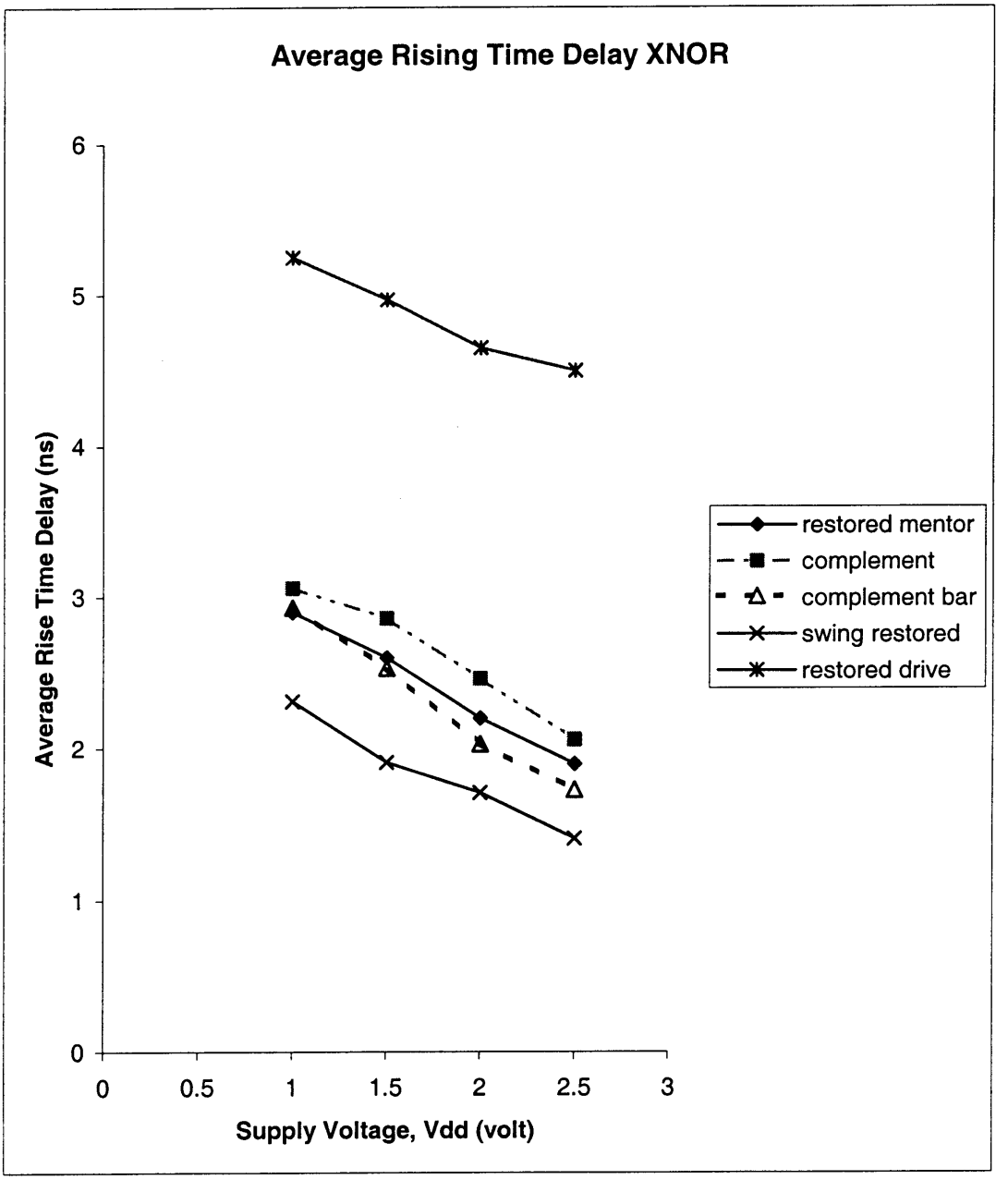

Figure 4.10 Average Rising Delay XNOR

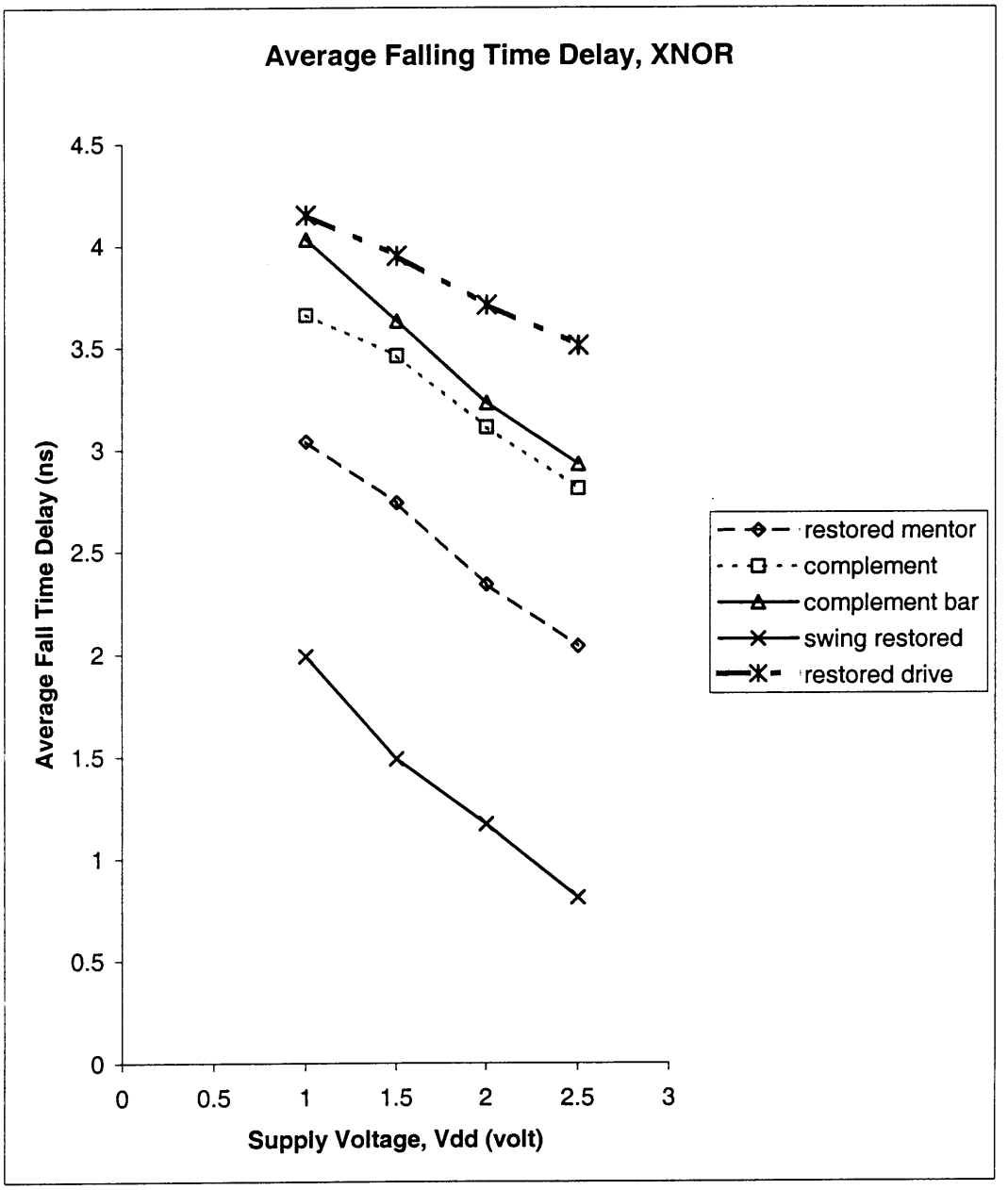

Figure 4.11 Average Falling Delay XNOR Gates

Table 4.11
Comparison of Each XNOR Function

	00	01	10	11	#Tr	Driving Output	Complement Output
Figure 2.M1	O	O	O	O	6	No	No
Figure 2.M2	O	O	O	O	8	best	No
Figure 2.M3	O	X	O	O	10	best	No
Figure 2.M4	O	A	O	O	8	best	No
Figure 2.M5	O	O	O	O	10	best	Yes

Symbols: AB= 00, 01, 10, 11. #Tr is number of transistors, O is Good signal level.X is poor signal level. A is nearly good signal level.

Table 4.12
Average Power Dissipation at 2ns-100ns of XNOR

Unit: uW	Power@1v	Power@1.5v	Power@2v	Power@2.5v	Power@2.5v V_{th}
Figure 2.M1	143.77uW	157.88uW	175.44uW	185.11uW	187.45uW
Figure 2.M2	27.28uW	38.40uW	49.67uW	62.25uW	67.54uW
Figure 2.M3	98.78uW	148.20uW	197.67uW	247.00uW	252.90uW
Figure 2.M4	13.00uW	19.50uW	26.00uW	32.50uW	37.50uW
Figure 2.M5	69.76uW	104.64uW	139.52uW	174.40uW	202.30uW

Power Dissipation measure from the Mentor Graphics Unit in Watt:
.meas tran avg_curr avg I(V_{dd}) from = 2.0ns to = 100.0ns
.meas avg_power param = ' –avg_curr*V_{dd}'

4.3 Experimental

This experiment used the full-restored combination circuit design XOR/XNOR (Figure 2.M1) designed for series connection of 128 XOR/XNOR-gates (Figure 4.12 and Figure 2.13). The first XOR gate has the name "XOR1" and the last XOR gate the name "XOR128". The series connections of 128 XOR/XNOR-gates are cascaded together such as the output of XOR1 connects to the input of XOR2 and so on. This experiment was devoted to a comparison of the output waveform from XOR1/XNOR1 to XOR127/XNOR127 gates. The output waveform shifts between the simulation graphs from XOR1 to XOR127. The simulation result was that the output waveforms worked correctly from XOR1 to XOR127 gates without degeneration. Appendix D lists the full schematic design of the series connection 128 XOR/XNOR-gates.

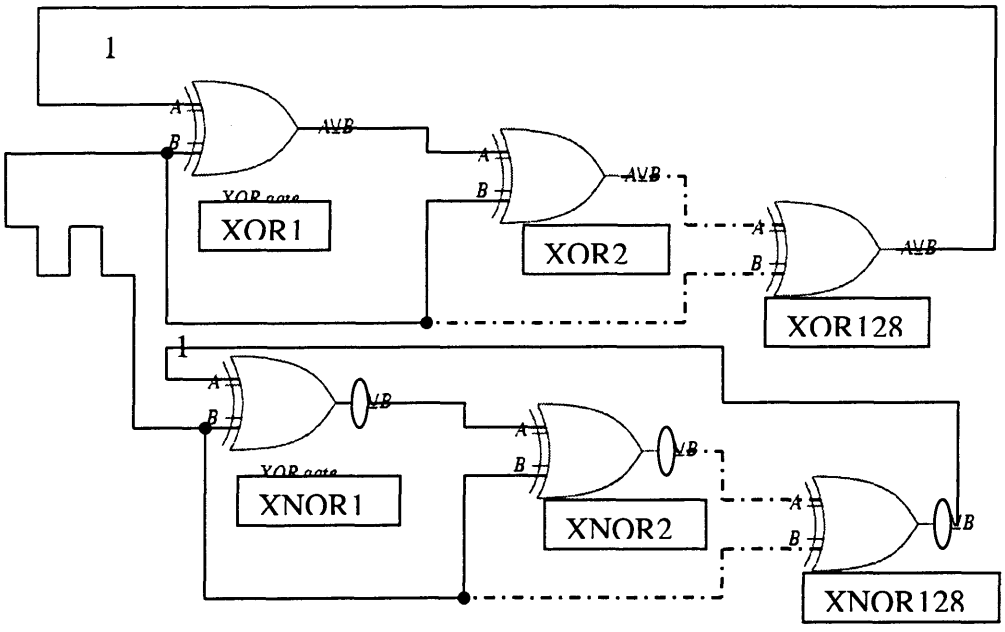

Figure 4.12 Series Connection of 128 XOR-Gates

5.0 Conclusion

In this thesis, the author has proposed new configurations of CMOS designs for the exclusive-OR and exclusive-NOR functions. For all four-transistor configurations, based on the output waveform results, the designs no longer need the complementary signal inputs and only one poor signal input. For the six transistor types that arise from adding the fan-out (inverter) connected to the output XOR/XNOR gates to help drive the output signal, the proposed designs have non-complementary inputs, good signal level outputs and the best driving capability. Based on the simulation results of both the four-transistor and six-transistor types, the designs are better and more competitive than traditional XOR circuits. An experiment where series connected 128 XOR/XNOR gates was designed with a static gate for low power circuit design and was verified by using the Mentor Graphics simulation. The simulation results showed the signal output waveforms working correctly from XOR1 gate to XOR127 gate without degeneration.

REFERENCE

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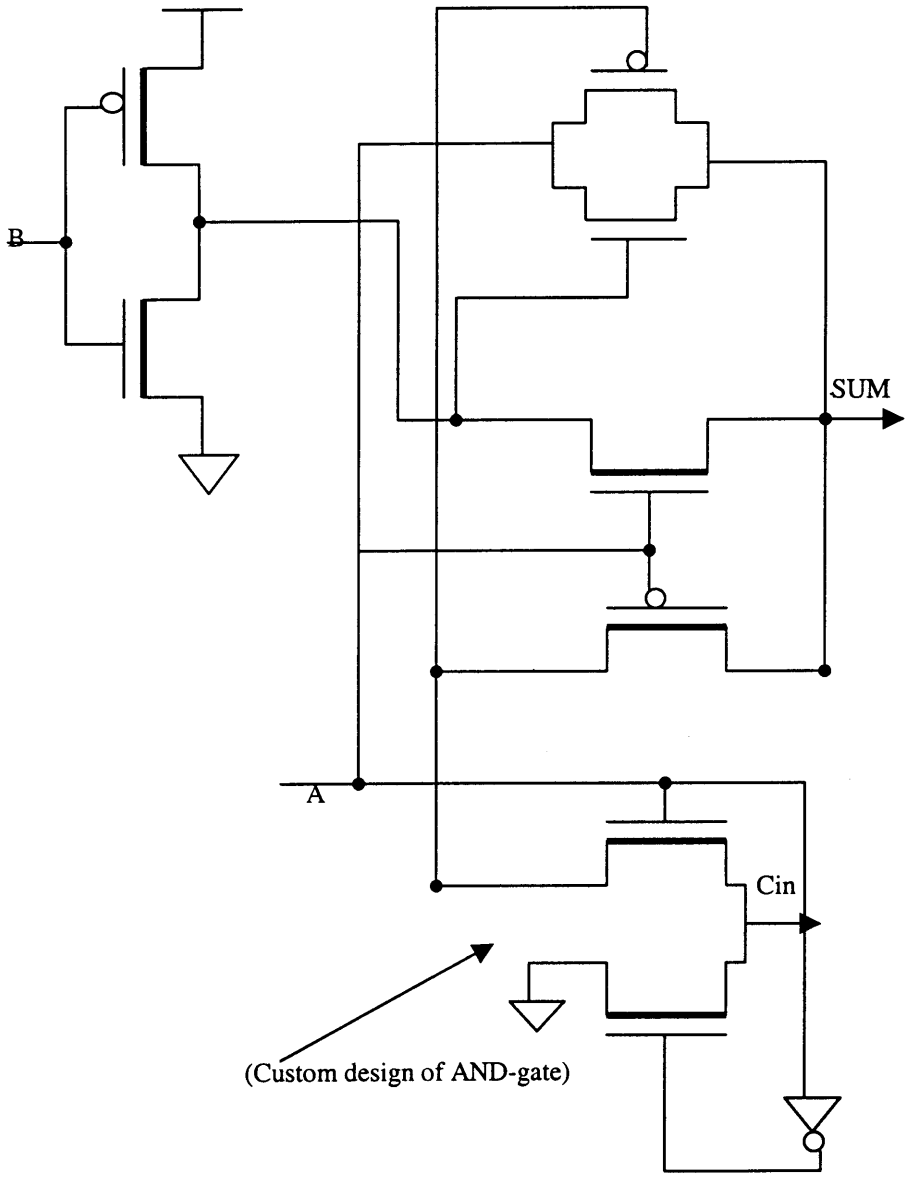
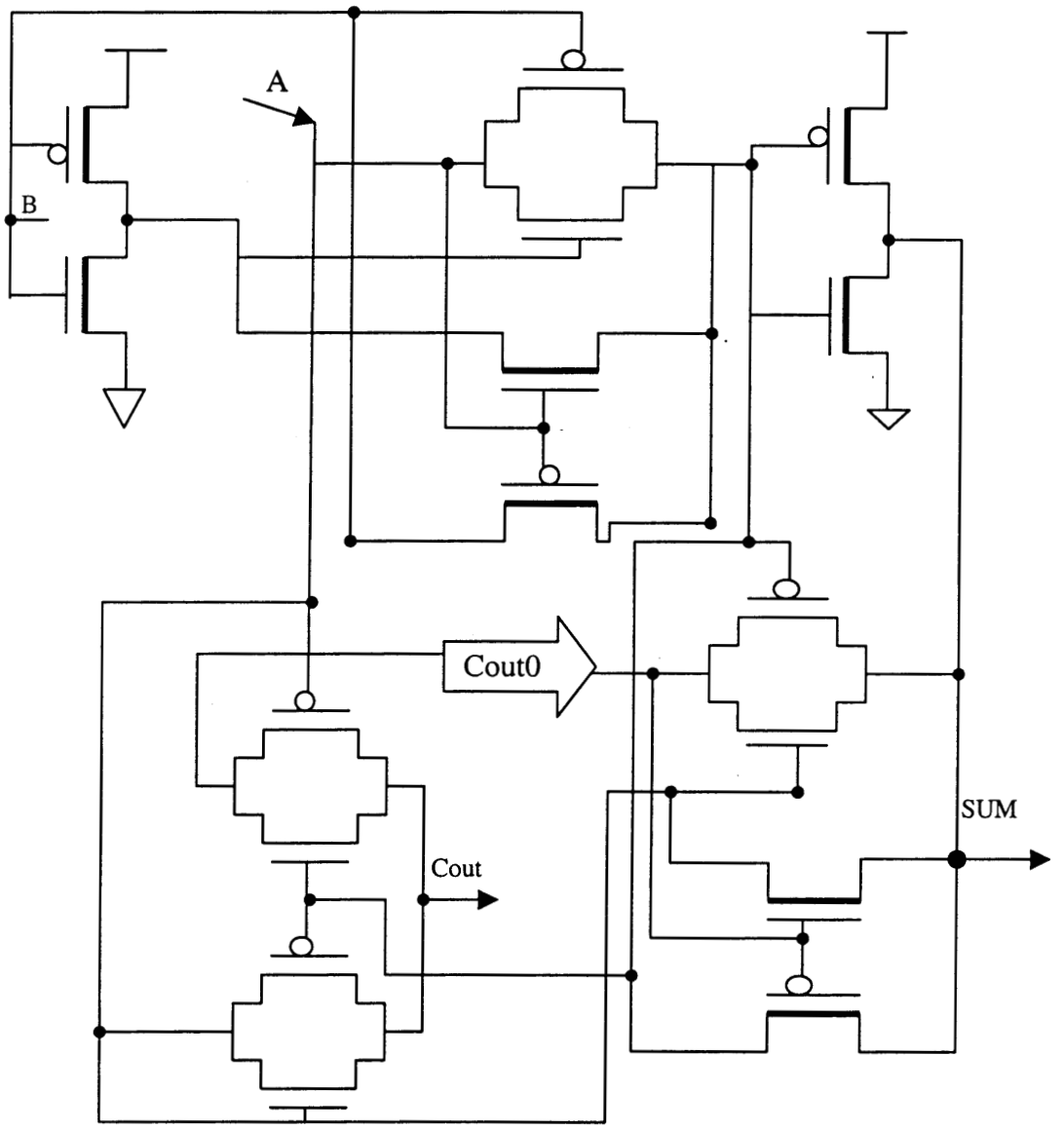
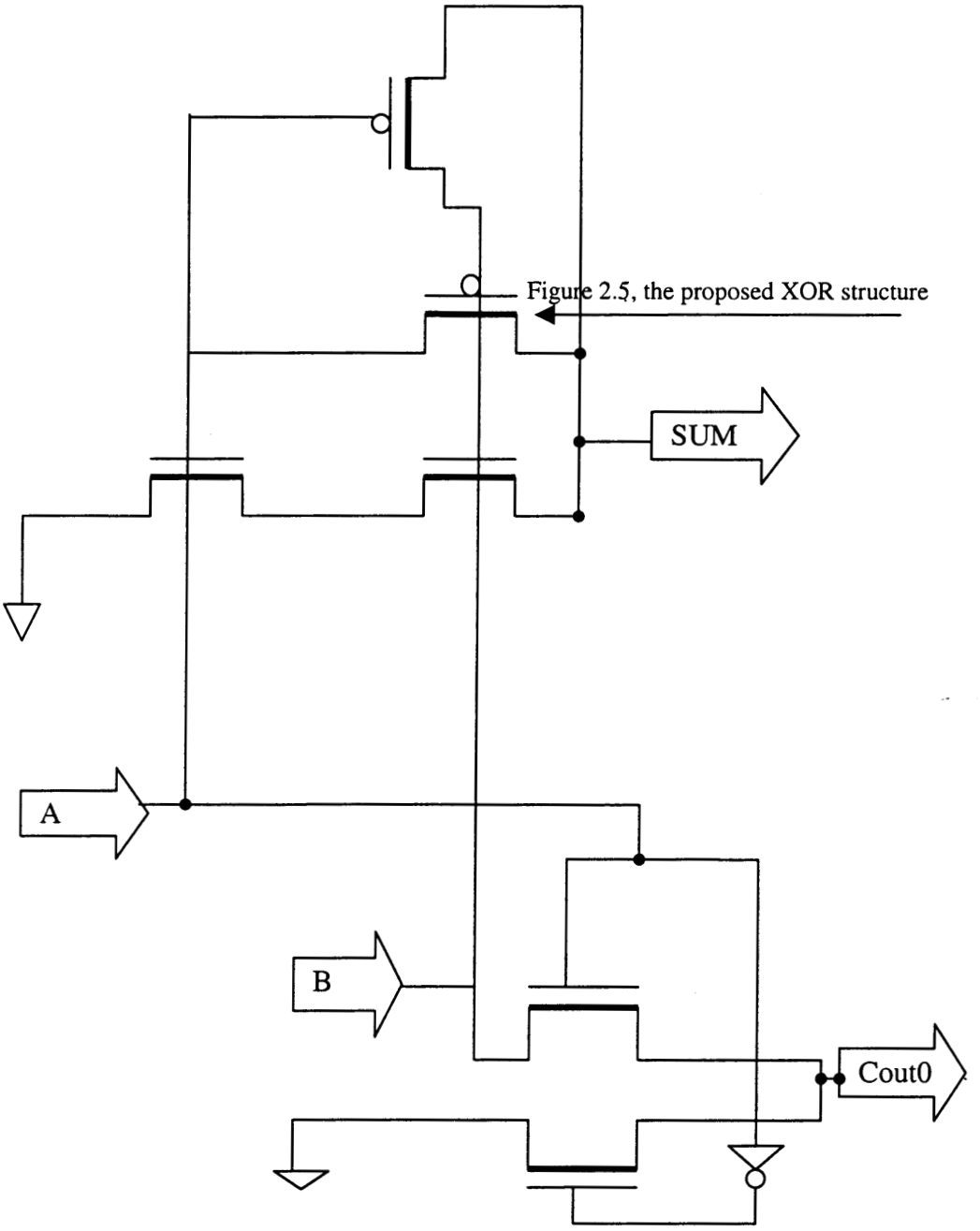
APPENDIX A: Carry Selected Full Adder
10 Transistors for Half Adder (Transmission Gate)



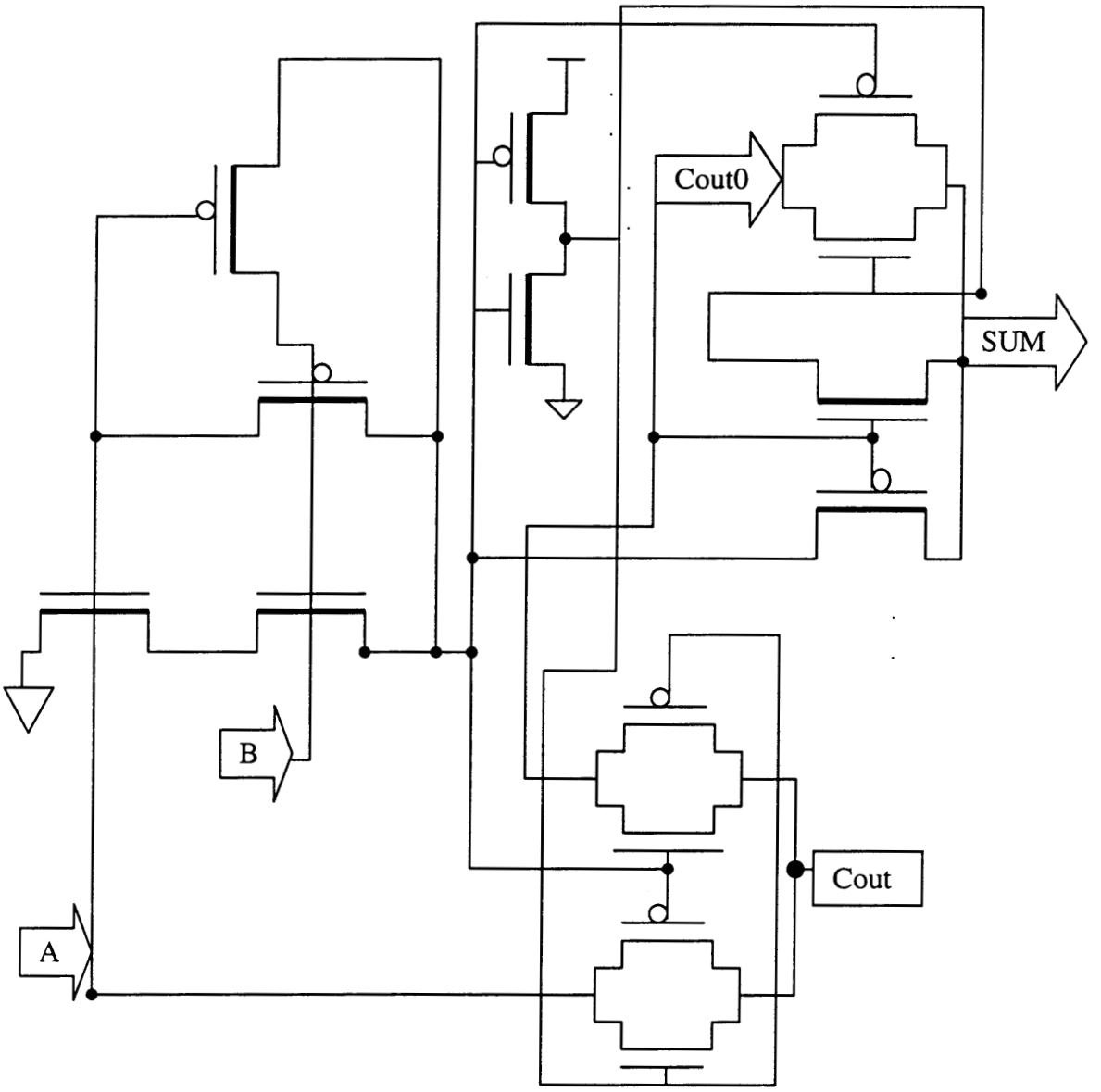
16 Transistors for Full Adder (Transmission Gate)



8 Transistors for Half Adder (Pass Transistors)



14 Transistors Full Adder (Pass Transistor)



APPENDIX B: TSMC CMOS Fabrication Technology

Table 1

TMSC 0.35μm Fabrication Technology

TSMC 0.35μm Typical SPICE Model

.MODEL CMOSN/NMOS Level 49

Web page: ftp://ftp.mosis.org/pub/mosis/vendors/tsmc-035/t08s_lp4m-params.txt

* DATE: Oct 30/98			
*LoT: n88y		WAF: 11	
* Temperature_parameters=Default			
.MODEL CMOSN NMOS (	LEVEL= 49		
+VERSION = 3.1	TNOM	= 27	**TOX= 7.6E-9**
+XJ = 1.5E-7	NCH	= 1.7E17	**VTH0= 0.4964**
+K1 = 0.5307769	K2	= 0.0199705	K3=0.2963637
+K3B = 0.2012165	W0	= 2.836319E-6	NLX=2.8942E-7
+DVT0W = 0	DVT1W	= 5.3E6	DVT2W=-0.032
+DVT0 = 0.112017	DVT1	= 0.2453972	DVT2=-0.1719
+U0 = 444.9381976	UA	=2.921E-10	UB=1.7732E-18
+UC = 7.067896E-11	VSAT	= 1.130785E5	A0=1.135
+AGS = 0.2810374	B0	= 2.844393E-7	B1= 5E-6
+KETA = -7.8181E-3	A1	= 0	A2= 1
+RDSW = 925.2701982	PRWG	= -1E-3	PRWB=-1E-3
+WR = 1	WINT	=7.186965E-8	LINT=1.7315E-9
+XL = 0	XW	= 0	DWG=-1.79E-8
+DWB = 5.851691E-9	VOFF	=-0.132935	NFACTOR= 0.5710
+CIT = 0	CDSC	= 8.607229E-4	CDSCD= 0
+CDSCB = 0	ETA0	= 2.128321E-3	ETAB= 0
+DSUB = 0.0257957	PCLM	= 0.6766314	PDIBLC1= 1
+PDIBLC2 = 1.787424E-3	PDIBLCB	= 0	DROUT=0.787
+PSCBE1 = 6.973485E9	PSCBE2=	1.46235E-7	PVAG = 0.05
+DELTA = 0.01	MOBMOD=	1	PRT= 0
+UTE = -1.5	KT1=	-0.11	KT1L= 0
+KT2 = 0.022	UA1=	4.31E-9	UB1=-7.61E-18
+UC1 = -5.6E-11	AT=	3.3E4	WL= 0
+WLN = 1	WW=	0	WWN= 1
+WWL = 0	LL=	0	LLN= 1
+LW = 0	LWN	= 1	LWL= 0
+CAPMOD = 2	CGDO	= 1.96E-10	CGSO=1.96E-10
+CGBO = 0	CJ	= 9.276962E-4	PB=0.8157962
+MJ = 0.3557696	CJSW	= 3.181055E-10	PBSW=0.6869149
+MJSW = 0.1	PVTH0	= -0.0252481	PRDSW=-96.428
+PK2 = -4.805372E-3	WKETA	= -7.643187E-4	LKETA=-0.014)
.MODEL CMOSP/PMOS Level 49			

.MODEL CMOSP PMOS (LEVEL= 49					
+VERSION	= 3.1	TNOM	= 27	**TOX=7.6E-9**	
+XJ	= 1.5E-7	NCH	= 1.7E17	**VTH0=-0.6636**	
+K1	= 0.4564781	K2	= -0.019447	K3=39.382919	
+K3B	= -2.8930965	W0	= 2.655585E-6	NLX=1.51E-7	
+DVT0W	= 0	DVT1W	= 5.3E6	DVT2W=-0.032	
+DVT0	= 1.1744581	DVT1	= 0.7631128	DVT2=-0.1035	
+U0	= 151.3305606	UA	= 2.061211E-10	UB=1.8277E-18	
+UC	= -8.97321E-12	VSAT	= 9.915604E4	A0=1.121053	
+AGS	= 0.3961954	B0	= 6.493139E-7	B1=4.2215E-6	
+KETA	= -9.27E-3	A1	= 0	A2	= 1
+RDSW	= 2.30725E3	PRWG	= -1E-3	PRWB	= 0
+WR	= 1	WINT	= 5.962233E-8	LINT=4.30928E-9	
+XL	= 0	XW	= 0	DWG=-1.5962E-8	
+DWB	= 1.378919E-8	VOFF	= -0.15	NFACTOR	= 2
+CIT	= 0	CDSC	= 6.593084E-4	CDSCD	= 0
+CDSCB	= 0	ETA0	= 0.0286461	ETAB	= 0
+DSUB	= 0.2436027	PCLM	= 4.3597508	PDIBLC1=7.44E-4	
+PDIBLC2	= 4.256073E-3	PDIBLCB	= 0	DROUT=0.012	
+PSCBE1	= 1.347622E10	PSCBE2	= 5E-9	PVAG=3.669793	
+DELTA	= 0.01	MOBMOD	= 1	PRT	= 0
+UTE	= -1.5	KT1	= -0.11	KT1L	= 0
+KT2	= 0.022	UA1	= 4.31E-9	UB1=-7.61E-18	
+UC1	= -5.6E-11	AT	= 3.3E4	WL	= 0
+WLN	= 1	WW	= 0	WWN	= 1
+WWL	= 0	LL	= 0	LLN	= 1
+LW	= 0	LWN	= 1	LWL	= 0
+CAPMOD	= 2	CGDO	= 2.307E-10	CGSO=2.307E-10	
+CGBO	= 0	CJ	= 1.420282E-3	PB	= 0.99
+MJ	= 0.5490877	CJSW	= 4.773605E-10	PBSW	= 0.99
+MJSW	= 0.1997417	PVTH0	= 6.58707E-3	PRDSW=-93.5582	
+PK2= 1.011593E-3		WKETA	= -0.0101398	LKETA	=6.027E-3)

*******************end of TSMC COMS 0.35μm***********************

APPENDIX C: HSPICE NETLIS Files

```
**********************************************************************
** HSPICE NETLIS of Fig 2.1 AXORB include TSMC 0.35μm Fabrication   **
**                                                          Technology   **
** Circuit: Fig.1 The XOR functions implemented by transmission gates      **
**********************************************************************
* File:axorb_fig1.sp
* Vcc = 1.5V
M1 out    b    a    Vdd CMOSP L=0.35u W=14u
M2 out    a    b    Vdd CMOSP L=0.35u W=14u
M3 out    out1  Vss   Vss CMOSN L=0.35u W=7u
M4 out1   a    b    Vss CMOSN L=0.35u W=7u
M5 out1   b    a    Vss CMOSN L=0.35u W=7u
M6 out1   out  Vdd   Vdd CMOSP L=0.35u W=14u

******WAVEFORM SETUP***********
Va   a  0 pulse(1.5 0 1ns 3.33ns 3.33ns 20ns 66.66ns)
Vb   b  0 pulse(1.5 0 1ns 3.33ns 3.33ns 40ns 86.66ns)
Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
C out Vss  1pF
.TRAN .02NS 100NS
.PRINT TRAN V(out)  I(Vdd) V(out1)
.probe tran  out=V(out) out1=V(out1) Vdd=I(Vdd)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=2.0ns to=100.0ns
.meas avg_power param = '-avg_curr*Vdd'

******* TSMC 0.35um fabrication technology *********
* DATE: Oct 30/98
*LoT: n88y              WAF: 11
* Temperature_parameters=Default
.MODEL CMOSN NMOS (          LEVEL   = 49
+VERSION    = 3.1            TNOM= 27          TOX= 7.6E-9
+XJ         = 1.5E-7           NCH= 1.7E17       VTH0= 0.4964448
+K1         = 0.53077          K2= 0.0199705     K3= 0.2963637
+K3B        = 0.20121          W0= 2.836319E-6   NLX= 2.8948E-7
+DVT0W      = 0              DVT1W= 5.3E6        DVT2W= -0.032
+DVT0       = 0.1120         DVT1= 0.2453972     DVT2= -0.171915
+U0         = 444.9381         UA= 2.921284E-10  UB= 1.7732E-18
+UC         = 7.0678E-11     VSAT= 1.130785E5      A0= 1.1356246
```

```
+AGS        = 0.28103          B0= 2.844393E-7    B1= 5E-6
+KETA       = -7.8181E-3       A1= 0              A2= 1
+RDSW       = 925.27019     PRWG= -1E-3        PRWB= -1E-3
+WR         = 1             WINT= 7.186965E-8  LINT= 1.73551E-9
+XL         = 0               XW= 0          DWG= -1.712973E-8
+DWB        = 5.8516E-9     VOFF=-0.13293  NFACTOR=0.57109
+CIT        = 0             CDSC= 8.60722E-4  CDSCD=0
+CDSCB      = 0              ETA0= 2.128321E-3  ETAB= 0
+DSUB       = 0.02579       PCLM= 0.6766     PDIBLC1= 1010
+PDIBLC2    = 1.7874E-3 PDIBLCB = 0           DROUT =0.7873539
+PSCBE1     = 6.9734E9 PSCBE2= 1.46235E-7      PVAG = 0.05
+DELTA      = 0.01        MOBMOD= 1              RT= 0
+UTE        = -1.5          KT1 = -0.11        KT1L= 0
+KT2        = 0.022         UA1= 4.31E-9       UB1= -7.61E-18
+UC1        = -5.6E-11       AT = 3.3E4        WL= 0
+WLN        = 1             WW= 0             WWN= 1
+WWL        = 0              LL= 0             LLN= 1
+LW         = 0             LWN= 1            LWL= 0
+CAPMOD     = 2            CGDO= 1.96E-10    CGSO= 1.96E-10
+CGBO       = 0              CJ    = 9.2769E-4   PB    = 0.815796
+MJ         = 0.3557       CJSW   = 3.181E-10   PBSW= 0.686914
+MJSW       = 0.1           PVTH0= -0.0252    PRDSW= -96.4502
+PK2        = -4.8053E-3    WKETA= -7.6431E-4 LKETA= -0.01291)
*
.MODEL CMOSP PMOS (   LEVEL  = 49
+VERSION  = 3.1          TNOM   = 27         TOX    = 7.6E-9
+XJ         = 1.5E-7          NCH= 1.7E17      VTH0= -0.6636594
+K1         = 0.456478         K2 = -0.019447      K3= 39.382919
+K3B        = -2.8930          W0 = 2.6555E-6    NLX = 1.5102E-7
+DVT0W     = 0             DVT1W= 5.3E6      DVT2W= -0.032
+DVT0       = 1.1744581       DVT1= 0.7631      DVT2= -0.1035171
+U0         = 151.3305606       UA= 2.061E-10     UB=1.8234E-18
+UC         = -8.973E-12       VSAT= 9.9156E4      A0 = 1.1210
+AGS        = 0.3961           B0= 6.4931E-7      B1= 4.273E-6
+KETA       = -9.27E-3         A1= 0              A2 = 1
+RDSW       = 2.307E3        PRWG = -1E-3       PRWB = 0
+WR         = 1              WINT  = 5.9622E-8  LINT  = 4.309E-9
+XL         = 0               XW   = 0           DWG = -1.596E-8
+DWB        = 1.378919E-8      VOFF = -0.15   NFACTOR = 2
+CIT        = 0               CDSC = 6.593E-4 CDSCD  = 0
+CDSCB      = 0              ETA0 = 0.0286       ETAB= 0
+DSUB      = 0.2436027      PCLM  = 4.3597    PDIBLC1 = 7.4470E-4
+PDIBLC2 = 4.256E-3     PDIBLCB = 0          DROUT  = 0.0120292
+PSCBE1  = 1.3476E10     PSCBE2  = 5E-9       PVAG   = 3.669793
```

```
+DELTA  = 0.01          MOBMOD  = 1           PRT    = 0
+UTE    = -1.5            KT1   = -0.11      KT1L   = 0
+KT2    = 0.022           UA1   = 4.31E-9    UB1    = -7.61E-18
+UC1    = -5.6E-11        AT    = 3.3E4      WL     = 0
+WLN    = 1               WW    = 0          WWN    = 1
+WWL    = 0               LL    = 0          LLN    = 1
+LW     = 0               LWN   = 1          LWL    = 0
+CAPMOD = 2             CGDO    = 2.307E-10  CGSO   = 2.307E-10
+CGBO   = 0               CJ    = 1.4202E-3  PB     = 0.99
+MJ     = 0.5490        CJSW    = 4.7736E-10 PBSW   = 0.99
+MJSW   = 0.1997        PVTH0   = 6.5870E-3  PRDSW= -93.5582228
+PK2    = 1.0113E-3     WKETA   = -0.01013   LKETA  = 6.0279E-3)
*
.option post
.end

*********************************************
** This file is HSPICES NETLIS of Fig 2.2, AXORB    **
** Circuit: Fig.2 The XOR functions implemented by    **
**          transmission gates with driving output        **
*********************************************
* File:axorb_fig2.sp
* Vcc = 1.5V
M1  out   b    a     Vdd   CMOSP L=0.35u W=14u
M2  a     bn   out   Vss   CMOSN L=0.35u W=7u
M3  out   bn   an    Vdd   CMOSP L=0.35u W=14u
M4  an    b    out   Vss   CMOSN L=0.35u W=7u
M5  out1  out  Vdd  Vdd CMOSP L=0.35u W=17u
M6  out1  out  Vss  Vss CMOSN L=0.35u W=7u
******WAVEFORM SETUP**********
Va  a  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 20ns, 66.66ns)
Van an 0 pulse(0, 1.5 1ns 3.33ns 3.33ns 20ns, 66.66ns)
Vb  b  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 40ns 86.66ns)
Vbn bn 0 pulse(0, 1.5 1ns 3.33ns 3.33ns 40ns 86.66ns)
Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
C out1 Vss
.TRAN .02NS 100NS
.PRINT TRAN V(out1)  I(Vdd)
.probe tran  out=V(out1) Vdd=I(Vdd)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=2.0ns to=10.0ns
.meas avg_power param = '-avg_curr*1.5'
.end
```

```
*********************************************
** This file is HSPICES NETLIS of Fig 2.2/AXNORB   **
** Circuit: Fig.2 The XNOR functions implemented by  **
**          transmission gates with driving output        **
 *********************************************
* File:axnorb_fig2.sp
* Vcc = 1.5V

M1 out    bn     a      Vdd CMOSP  L=0.35u W=14u
M2 a      b      out    Vss CMOSN  L=0.35u W=7u
M3 out    b      an     Vdd CMOSP  L=0.35u W=14u
M4 an     bn     out    Vss  CMOSN  L=0.35u W=7u
M5 out1   out    Vdd    Vdd CMOSP  L=0.35u W=21u
M6 out1   out    Vss    Vss  CMOSN L=0.35u W=7u

*WAVEFORM SETUP
Va  a  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 20ns, 66.66ns)
Van an 0 pulse(0, 1.5 1ns 3.33ns 3.33ns 20ns, 66.66ns)
Vb  b  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 40ns 86.66ns)
Vbn bn 0 pulse(0, 1.5 1ns 3.33ns 3.33ns 40ns 86.66ns)

Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
C out1 Vss  1pF
.TRAN .02ns 100ns
.PRINT TRAN V(out1)  I(Vdd)
.probe tran  out1=V(out1) Vdd=I(Vdd)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=2.0ns to=10.0ns
.meas avg_power param = '-avg_curr*1.5'
.end

*********************************************
** This file is HSPICES NETLIS of Fig 2.3/AXORB      **
**  Circuit: Fig. 3(a) Inverter-base XOR structure        **
*********************************************
* File:axorb_fig3.sp
* Vcc = 1.5V

M1 out    a      Vdd    Vdd CMOSP L=0.35u W=10u
M2 out    a      Vss    Vss CMOSN L=0.35u W=10u
M3 out1   b      a      Vdd CMOSP L=0.35u W=10u
M4 out1   b      out    Vss CMOSN L=0.35u W=10u
```

```
****WAVEFORM SETUP

Va  a  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 20ns 66.66ns)
Vb  b  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 40ns 86.66ns)
Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
R out1 Vss  100
*C  out1 Vss  1pF
.TRAN .02NS 100NS
.PRINT TRAN V(out1)  I(Vdd)
.probe tran  out1=V(out1) Vdd=I(Vdd)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=2.0ns to=10.0ns
.meas avg_power param = '-avg_curr*1.5'
.end

*********************************************
** This file is HSPICES NETLIS of Fig 2.3/AXNORB **
** Circuit: Fig. 3(b) Inverter-base XNOR structure      **
*********************************************
* File:axnorb_fig3.sp
* Vcc = 1.5V
M1 out    a     Vdd    Vdd CMOSP  L=0.35u W=30u
M2 out    a     Vss    Vss CMOSN  L=0.35u W=10u
M3 out1   b     out    Vdd CMOSP  L=0.35u W=3u
M4 out1   b      a     Vss CMOSN  L=0.35u W=1u
****WAVEFORM SETUP
Va  a  0 pulse(0 1.5 1ns 3.33ns 3.33ns 20ns 66.66ns)
Vb  b  0 pulse(0 1.5 1ns 3.33ns 3.33ns 40ns 86.66ns)

Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
R out1 Vss  550
.TRAN .02NS 100NS
.PRINT TRAN V(out1)  I(Vdd)
.probe tran  out1=V(out1) Vdd=I(Vdd)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=2.0ns to=10.0ns
.meas avg_power param = '-avg_curr*1.5'
.end
```

```
*********************************************
** This file is HSPICES NETLIS of Fig 2.4a/AXORB   **
** Circuit: Fig. 4a Improved version of XOR structure  **
*********************************************
* File:axorb_fig4a.sp
* Vcc = 1.5V
****** Inverted
M1 out    a   Vdd    Vdd CMOSP L=0.35U W=15u
M2 out    a   Vss    Vss CMOSN L=0.35U W=5u
********** Tranmission gate
M3  b    a    out1   Vdd CMOSP L=0.35U W=2u
M4  b    out  out1   Vss CMOSN L=0.35U W=2u
******* Inverter
M5  out1   b  a      Vdd CMOSP L=0.35U W=9u
M6  out1   b  out    Vss CMOSN L=0.35U W=3u
*WAVEFORM SETUP

Va  a  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 20ns, 66      .66ns)
Vb  b  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 40ns 86.      66ns)

Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
*C out1 GND  1pF
R out1 GND  600
.TRAN .02NS 100ns
.PRINT TRAN V(out1)  I(Vdd)
.probe tran  out1=V(out1) Vdd=I(Vdd)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=2.0ns to=100ns
.meas avg_power param = '-avg_curr*1.5'
.end

*****************************************************
** This file is HSPICES NETLIS of Fig 2.4b/AXORB              **
** Circuit: Fig. 4b Another improved version of XOR structure  **
*****************************************************
* File:axorb_fig4b.sp
* Vcc = 1.5V
M1 out    a     Vdd     Vdd CMOSP L=0.35U W=30u
M2 out    a     Vss     Vss CMOSN L=0.35U W=10u
M3 out1   b     out     Vdd CMOSP L=0.35U W=3u
M4 out1   b     a      Vss CMOSN L=0.35U W=1u
M5 out2   out1    Vdd     Vdd CMOSP L=0.35U W=9u
M6 out2   out1    Vss     Vss CMOSN L=0.35U W=3u
```

```
*WAVEFORM SETUP
Va  a  0 pulse(0, 1.5 1ns 3.33ns 3.33ns 20ns, 66.66ns)
Vb  b  0 pulse(0, 1.5 1ns 3.33ns 3.33ns 40ns 86.66ns)

Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
R out1  Vss  550
R1 out2 Vss   50
.TRAN .02NS 100NS

.PRINT TRAN V(out1)  I(Vdd)
.probe tran  out1=V(out1) Vdd=I(Vdd)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=2.0ns to=10.0ns
.meas avg_power param = '-avg_curr*1.5'
.end

*********************************************
** This file is HSPICES NETLIS of Fig 2.5/AXORB    **
** Circuit: Fig.5 Proposed XOR                     **
*********************************************
* File:axorb_fig5.sp
* Vcc = 1.5V
Vdd   Vdd   0   DC   1.5V
Vss   Vss   0   DC   0V
M1    out    B   y      Vss CMOSN L=0.35U W=1u
M2     y     A   Vss    Vss CMOSN L=0.35U W=1u
M3    out    B   A      Vdd CMOSP L=0.35U W=2.5u
M4    out    A   B      Vdd CMOSP L=0.35U W=2.5u
C  out   Vss  .1pF
V1 A 0 pulse(1.5, 0 1ns 3.33ns 3.33ns 20ns, 66.66ns)
V2 B 0 pulse(1.5, 0 1ns 3.33ns 3.33ns 40ns,  86.66ns)
.TRAN 0.020NS 100NS

.PRINT TRAN V(out)
.probe tran  out=V(out)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=1.0ns to=10.0ns
.meas avg_power param = '-avg_curr*1.5'
.end
```

```
**********************************************
** This file is HSPICES NETLIS of Fig 2.5/AXNORB   **
** Circuit: Fig. 5 Proposed XNOR                   **
**********************************************
* File:axnorb_fig5.sp
* Vcc = 1.5V
Vdd   Vdd   0   DC   1.5V
Vss    Vss    0    DC  0V

M1  out  B    y     Vdd  CMOSP L=0.35U W=25u
M2  y     A  Vdd  Vdd  CMOSP L=0.35U W=25u
M3  out  B   A     Vss   CMOSN L=0.35U W=10u
M4  out  A   B     Vss   CMOSN L=0.35U W=10u
C  out  Vss  .1pF

V1 A 0 pulse(0, 1.5 1ns  3.333ns 3.33ns 20ns,        66.66ns)
V2 B 0 pulse(0,1.5 1ns   3.33ns  3.33ns 40ns,        86.66ns)
.TRAN 0.020NS 100NS
.PRINT TRAN V(out)
.probe tran  out=V(out)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=1.0ns to=       10.0ns
.meas avg_power param = '-avg_curr*1.5'
.end

**********************************************
** This file is HSPICES NETLIS of Fig 2.6/AXORB   **
** Circuit: Fig. 6 The Proposed XOR structure with    **
**            driving output                          **
**********************************************
* File:axorb_fig6.sp, l=.35u, WP=2.1u
* Vcc = 1.5V
Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
M1  out1  out   Vdd    Vdd CMOSP L=0.35U W=15u
M2  out1  out   Vss    Vss CMOSN L=0.35U W=5u
M3  out   B     y      Vdd CMOSP L=0.35U W=2.1u
M4  y     A     Vdd    Vdd CMOSP L=0.35U W=2.1u
M5  out   B     A      Vss CMOSN L=0.35U W=1.05u
M6  out   A     B      Vss CMOSN L=0.35U W=1.05u
C1 out1   Vss   1pF
Va  A   0 pulse(0,1.5 1ns  3.33ns 3.33ns 20ns, 66.66ns)
Vb  B   0 pulse(0,1.5 1ns 3.33ns 3.33ns 40ns         , 86.66ns)
.TRAN 0.020NS 100NS
```

```
.PRINT TRAN V(out) V(out1)
.probe tran  out=V(out) out1=V(out1)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=1.0ns to=10.0ns
.meas avg_power param = '-avg_curr*1.5'
.end

*********************************************
** This file is HSPICES NETLIS of Fig 2.6/AXNORB    **
Circuit: Fig. 6 The Proposed XNOR structure with        **
**            driving output                                **
*********************************************
* File:axnorb_fig6.sp, l=.35u, WP=2.1u
* Vcc = 1.5V
Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V

M1   out1   out   Vdd  Vdd   CMOSP L=0.35U W=15u
M2   out1   out   Vss   Vss   CMOSN L=0.35U W=5u
M3   out    B     y     Vss   CMOSN L=0.35U W=1.05u
M4   y      A     Vss   Vss   CMOSN L=0.35U W=1.05u
M5   out    B     A     Vdd   CMOSP L=0.35U W=2.1u
M6   out    A     B     Vdd   CMOSP L=0.35U W=2.1u
C  out1  Vss   1pF
V1 A 0 pulse(1.5,0 3ns 3.33ns 3.33ns 20ns, 66.66ns)
V2 B 0 pulse(1.5,0 3ns 3.33ns 3.33ns 40ns, 86.66ns)

.TRAN 0.020NS 100NS
.PRINT TRAN V(out1)
.probe tran  out1=V(out1)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=1.0ns to=10.0ns
.meas avg_power param = '-avg_curr*1.5'
.end

*****************************************************
** This file is HSPICES NETLIS of Fig 2.7//Fig 2.M1 XOR/XNOR    **
** Circuit: Fig. 7/ Fig. M1 Full restored Combination circuit design    **
**            XOR/XNOR                                              **
*****************************************************
* File:axorb_fig12.sp
* Vcc = 1.5V
M1 out    b    a       Vdd CMOSP L=0.35u        W=5u
M2 out    a    b       Vdd CMOSP L=0.35u        W=5u
```

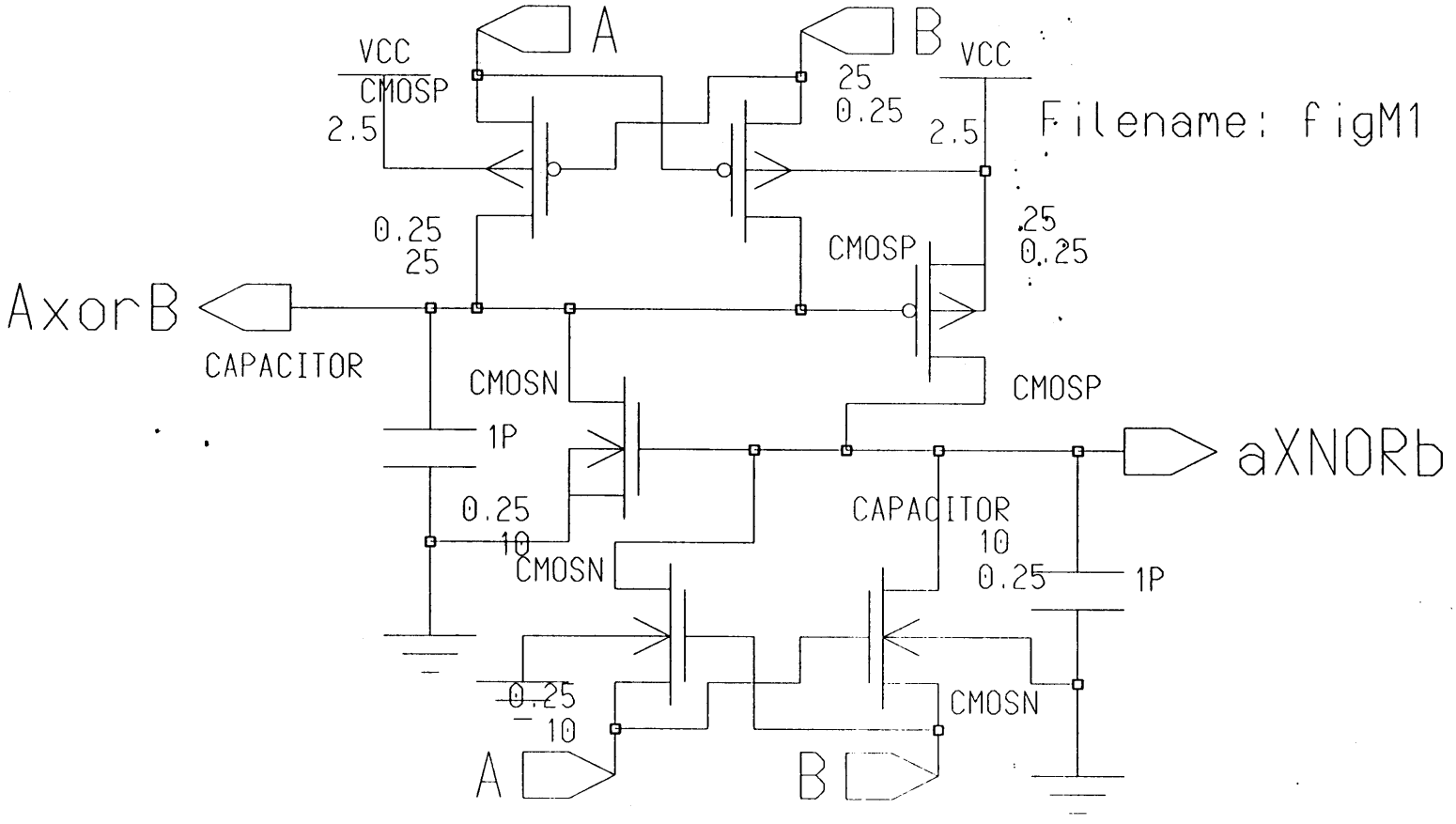
```
M3 out    out1  Vss   Vss CMOSN L=0.35u        W=12u
M4 out1   a     b     Vss CMOSN L=0.35u        W=2u
M5 out1   b     a     Vss CMOSN L=0.35u        W=2u
M6 out1   out   Vdd   Vdd CMOSP L=0.35u        W=30u
*WAVEFORM SETUP
Va   a  0 pulse(1.5 0   1ns 3.33ns 3.33ns      20ns 66.66ns)
Vb   b  0 pulse(1.5 0   1ns 3.33ns 3.33ns      40ns 86.66ns)

Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
C out Vss  1pF
.TRAN .02NS 100NS
.PRINT TRAN V(out)  I(V    dd) V(out1)
.probe tran  out=V(out)        out1=V(out1) Vdd=I(Vdd)
* let's measure average       power consumption
.meas tran avg_curr avg       I(Vdd) from=2.0ns to=10.0ns
.meas avg_power param =       '-avg_curr*1.5'
.end

************************************************
** This file is HSPICES NETLIS of Fig 2.12a/AXORB     **
** Circuit: Fig. 12a Realistic-simulated circuit for Fig. 2   **
************************************************
** File:axorb_fig12a.sp
* Vcc = 1.5V
M1 out    bn        a       Vdd CMOSP   L=0.35u  W=14u
M2 a      b         out     Vss CMOSN   L=0.35u   W=7u
M3 out    b         an      Vdd CMOSP   L=0.35u W=14u
M4 an     bn        out     Vss  CMOSN  L=0.35u W=7u
M5 out1   out       Vdd     Vdd CMOSP   L=0.35u W=21u
M6 out1   out       Vss     Vss  CMOSN  L=0.35u W=7u
**********input_a,  output_an
M7 an    a     Vdd    Vdd CMOSP L=0.35u W=6u
M8 an    a     Vss    Vss CMOSN L=0.35u W=2u
**********input_an,  output_a
M9  a    an     Vdd    Vdd CMOSP L=0.35u W=6u
M10 a    an     Vss    Vss CMOSN L=0.35u W=2u
**********input_b,  output_bn
M11 bn    b     Vdd    Vdd CMOSP L=0.35u W=6u
M12 bn    b     Vss    Vss CMOSN L=0.35u W=2u
**********input_bn,  output_b

M13  b    bn     Vdd    Vdd CMOSP L=0.35u W=6u
M14  b    bn     Vss    Vss CMOSN L=0.35u W=2u
```

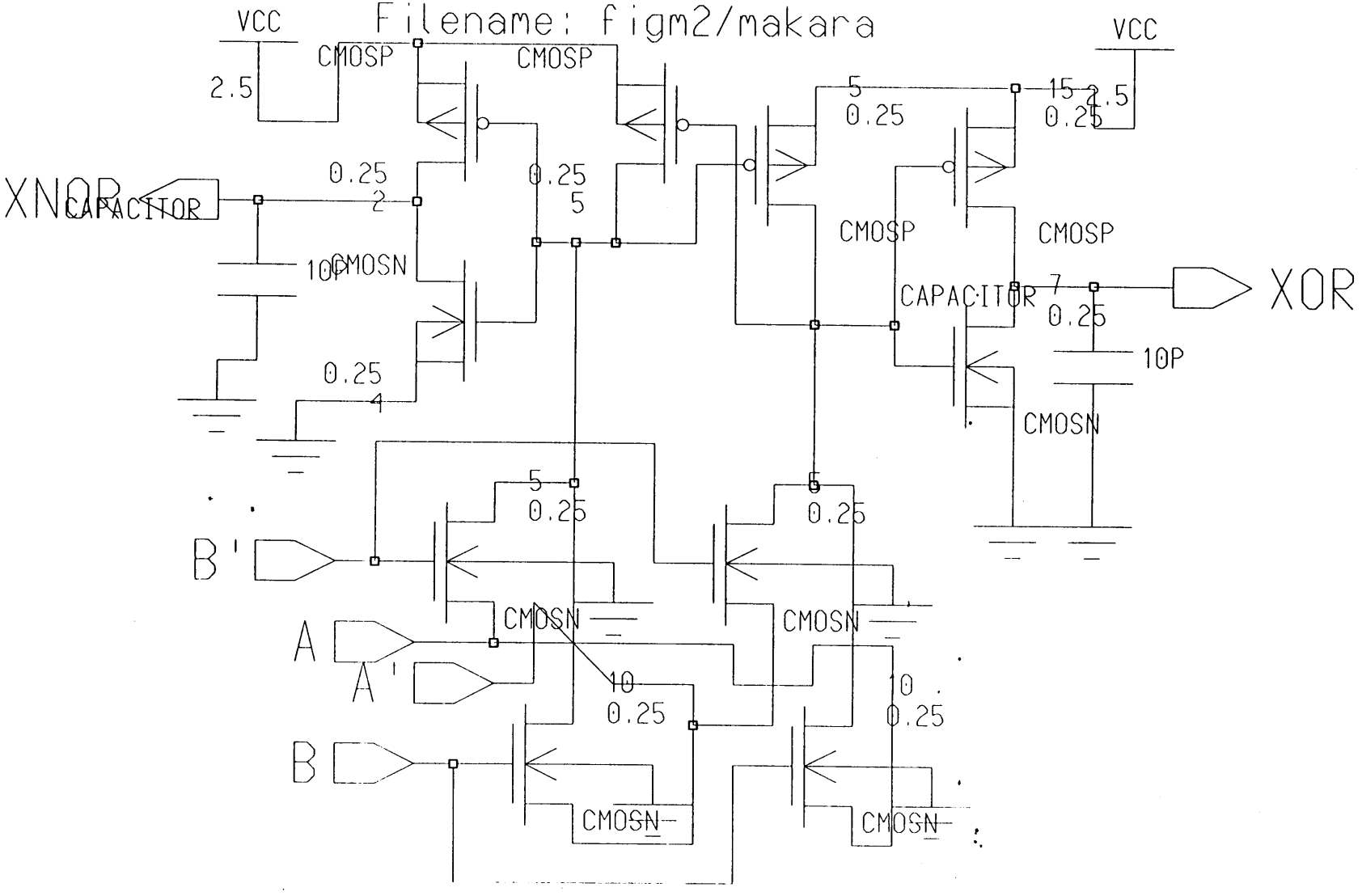
```
*WAVEFORM SETUP
Va  a  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 20ns, 66.66ns)
Van an 0 pulse(0, 1.5 1ns 3.33ns 3.33ns 20ns, 66.66ns)
Vb  b  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 40ns 86.66ns)
Vbn bn 0 pulse(0, 1.5 1ns 3.33ns 3.33ns 40ns 86.66ns)
Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
C out1 Vss  1pF
.TRAN .02NS 100NS
.PRINT TRAN V(out1)  I(Vdd)
.probe tran  out=V(out1) Vdd=I(Vdd)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=2.0ns to=10.0ns
.meas avg_power param = '-avg_curr*1.5'
.end

************************************************
** This file is HSPICES NETLIS of Fig 2.12b /AXORB    **
** Circuit: Fig. 12b Realistic-simulated circuit for Fig. 4    **
************************************************
* File:fig12b.sp
* Vcc = 1.5V
******  Inverter
M1 out     a   Vdd     Vdd   CMOSP L=0.35U W=15u
M2 out     a   Vss     Vss   CMOSN L=0.35U W=5u
********** Tranmission gate
M3 b       a   out1    Vdd CMOSP L=0.35U W=2u
M4 b       out  out1    Vss CMOSN L=0.35U W=2u
******* Inverter
M5 out1    b   a       Vdd CMOSP L=0.35U W=9u
M6 out1    b   out     Vss CMOSN L=0.35U W=3u
***********input_an,  output_a
M7  a    an     Vdd   Vdd CMOSP L=0.35u W=6u
M8  a    an     Vss   Vss CMOSN L=0.35u W=2u

**********input_bn,  output_b
M9   b    bn     Vdd   Vdd CMOSP L=0.35u W=6u
M10  b    bn     Vss   Vss CMOSN L=0.35u W=2u

*WAVEFORM SETUP
Va  a  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 20ns, 66.      66ns)
Vb  b  0 pulse(1.5, 0 1ns 3.33ns 3.33ns 40ns 86.6     6ns)
Van  an  0 pulse(0, 1.5 1ns 3.33ns 3.33ns 20ns, 6     6.66ns)
```

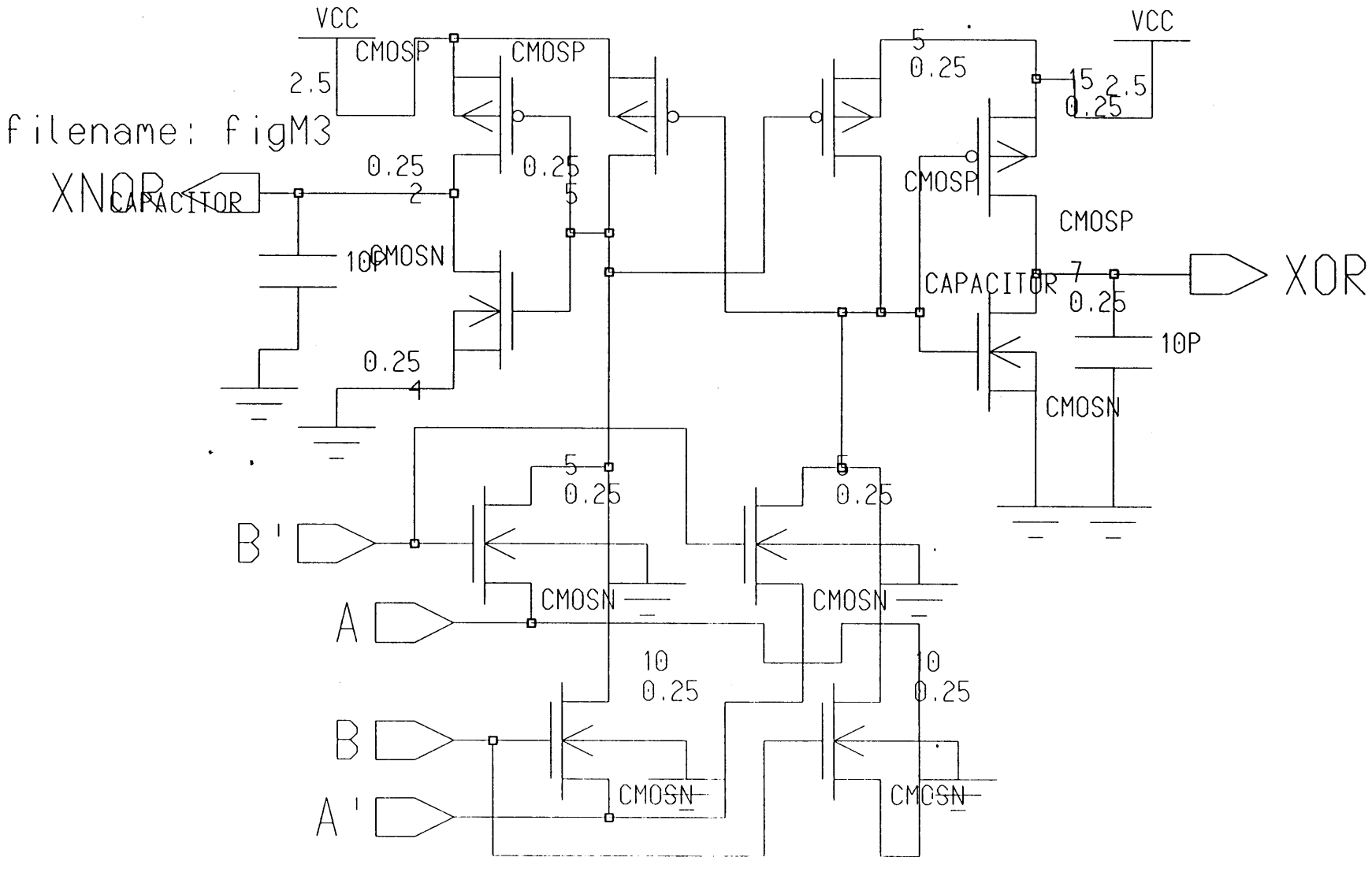
```
Vbn  bn  0 pulse(0,1.5 1ns 3.33ns 3.33ns 40ns 86.   66ns)

Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC  0V
*C out1 GND  1pF
R out1 GND  600
.TRAN .02NS 100NS
.PRINT TRAN V(out1)  I(Vdd)
.probe tran  out1=V(out1) Vdd=I(Vdd)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=2.0ns to=10.0 ns
.meas avg_power param = '-avg_curr*1.5'
.end

**********************************************
** This file is HSPICES NETLIS of Fig 2.12c /AXORB **
** Realistic-simulated circuit for Fig. 4                **
**********************************************
* File:Fig. 12c.sp
* Vcc = 1.5V
M1 out    a     Vdd    Vdd  CMOSP L=0.35U W=30U
M2 out    a     Vss    Vss  CMOSN L=0.35U W=10U
M3 out1   b     out    Vdd  CMOSP L=0.35U W=3u
M4 out1   b     a      Vss  CMOSN L=0.35U W=1u
M5 out2   out1   Vdd    Vdd CMOSP L=0.35U W=9U
M6 out2   out1   Vss    Vss CMOSN L=0.35U W=3U
**********input_an,  output_a

M7  a    an    Vdd   Vdd CMOSP L=0.35u W=6u
M8  a    an    Vss   Vss CMOSN L=0.35u W=2u
**********input_bn,  output_b

M9  b    bn    Vdd   Vdd CMOSP L=0.35u W=6u
M10 b    bn    Vss   Vss CMOSN L=0.35u W=2u

*WAVEFORM SETUP
Va  a  0 pulse(0, 1.5 1ns 3.33ns 3.33ns 20ns, 66.66ns)
Vb  b  0 pulse(0, 1.5 1ns 3.33ns 3.33ns 40ns 86.66ns)
Van  an  0 pulse(1.5,0 1ns 3.33ns 3.33ns 20ns, 66.66ns)
Vbn  bn  0 pulse(1.5,0 1ns 3.33ns 3.33ns 40ns 86.66ns)
Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
R out1  Vss  550
R1 out2 Vss  50
```

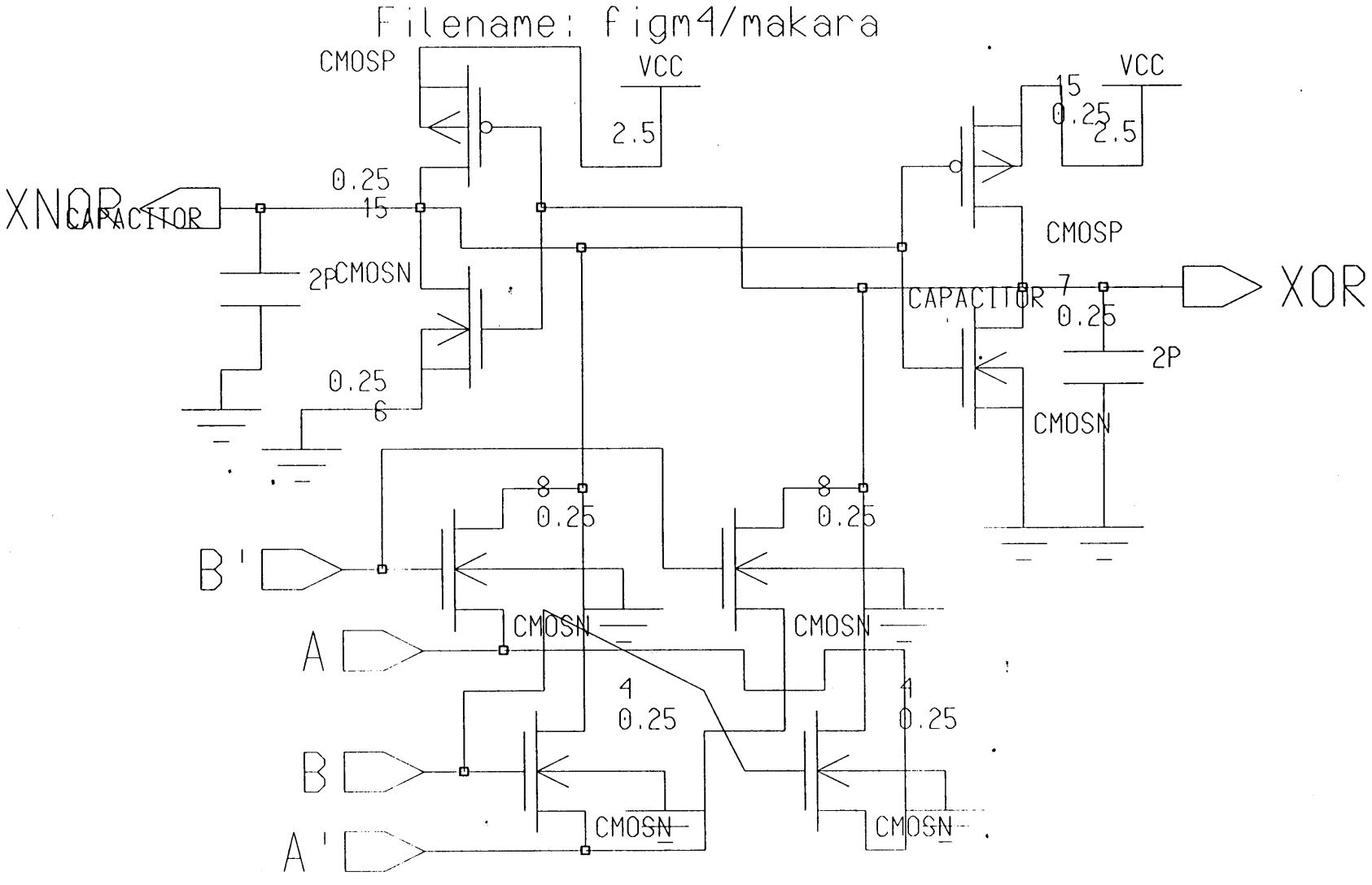
```
.TRAN .02NS 100NS
.PRINT TRAN V(out1)  I(Vdd)
.probe tran  out1=V(out1) Vdd=I(Vdd)
* let's measure average power consumption
.meas tran avg_curr avg I(Vdd) from=2.0ns to=10.0ns
.meas avg_power param = '-avg_curr*1.5'
.end

************************************************
** This file is HSPICES NETLIS of Fig 2.12d /AXORB    **
** Circuit: Fig. 12d Realistic-simulated circuit for Fig. 6    **
************************************************
* File:fig12d.sp,        l=.35u, WP=2.1u
* Vcc = 1.5V
Vdd Vdd 0 DC 1.5V
Vss Vss 0 DC 0V
M1  out1  out   Vdd    Vdd    CMOSP L=0.35U W=15u
M2  out1  out   Vss    Vss    CMOSN L=0.35U W=5u
M3  out   B     y      Vdd    CMOSP L=0.35U W=2.1u
M4  y     A     Vdd    Vdd    CMOSP L=0.35U W=2.1u
M5  out   B     A      Vss    CMOSN L=0.35U W=1.05u
M6  out   A     B      Vss    CMOSN L=0.35U W=1.05u
M7  a     an    Vdd    Vdd CMOSP L=0.35u W=6u
M8  a     an    Vss    Vss CMOSN L=0.35u W=2u
**********input_bn,  utput_b
M9  b     bn    Vdd    Vdd CMOSP L=0.35u W=6u
M10 b     bn    Vss    Vss CMOSN L=0.35u W=2u
C1 out1   Vss   1pF
Va  A   0 pulse(0,1.5  1ns  3.33ns 3.33ns 20ns, 66.66ns)
Vb  B   0 pulse(0,1.5  1ns 3.33ns 3.33ns 40ns, 86.66ns)
Van  an  0 pulse(1.5,0 1ns 3.33ns 3.33ns 20ns, 66.66ns)
Vbn  bn  0 pulse(1.5,0 1ns 3.33ns 3.33ns 40ns 86.66ns)
.TRAN 0.020NS 100NS
.probe tran  out=V(out) out1=V(out1)
.meas tran avg_curr av          g I(Vdd) from=1.0ns to=10.0ns
.meas avg_power param= '-avg_curr*1.5'
.end
********* END OF HSPICES NETLIS ***************
```

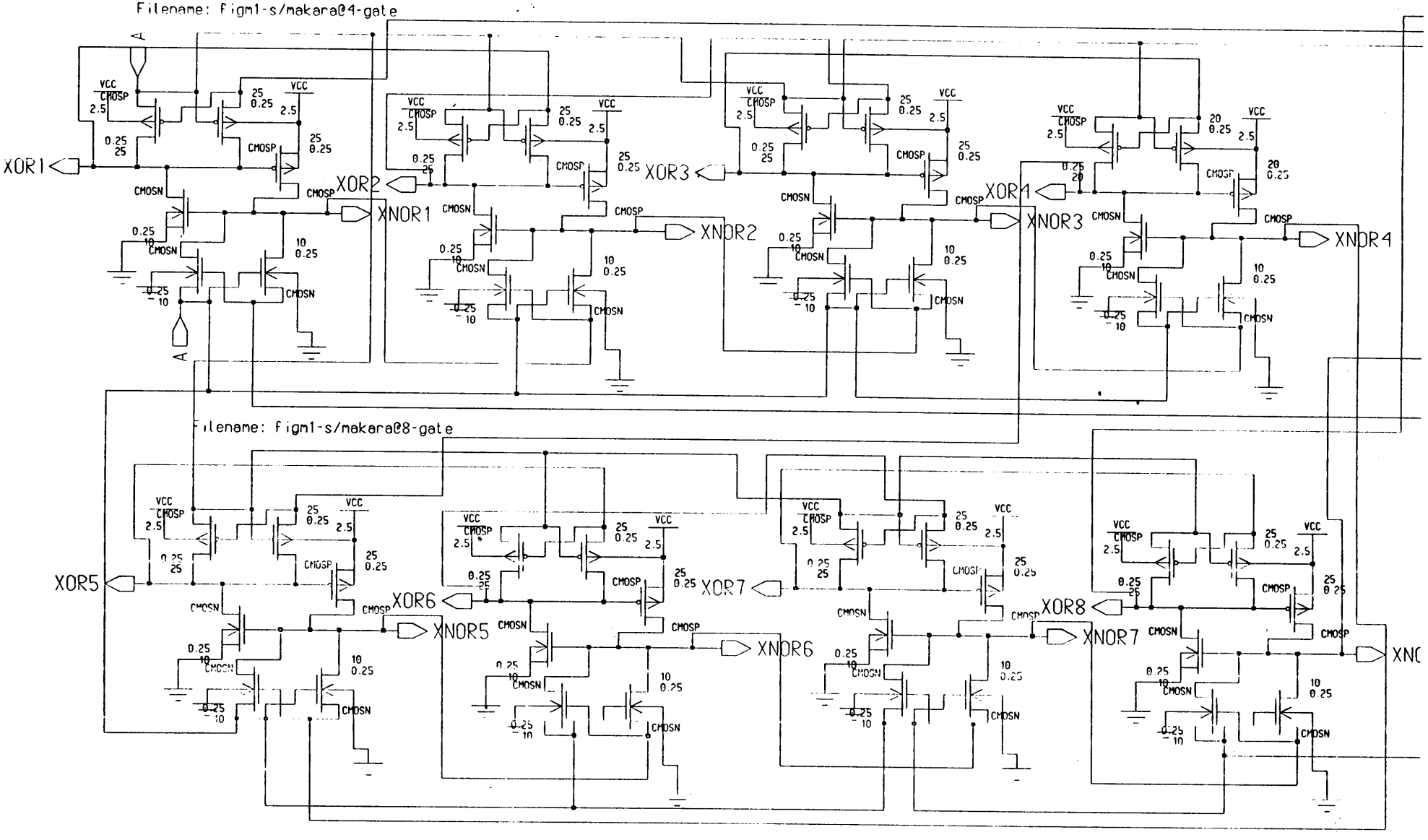
APPENDIX D: The Layout of XOR/XNOR Works on Mentor Graphics, Design Architecture (DA) from Figures 2.M1 to 2.M5, and Schismatic of 128 XOR/XNOR-Gates.

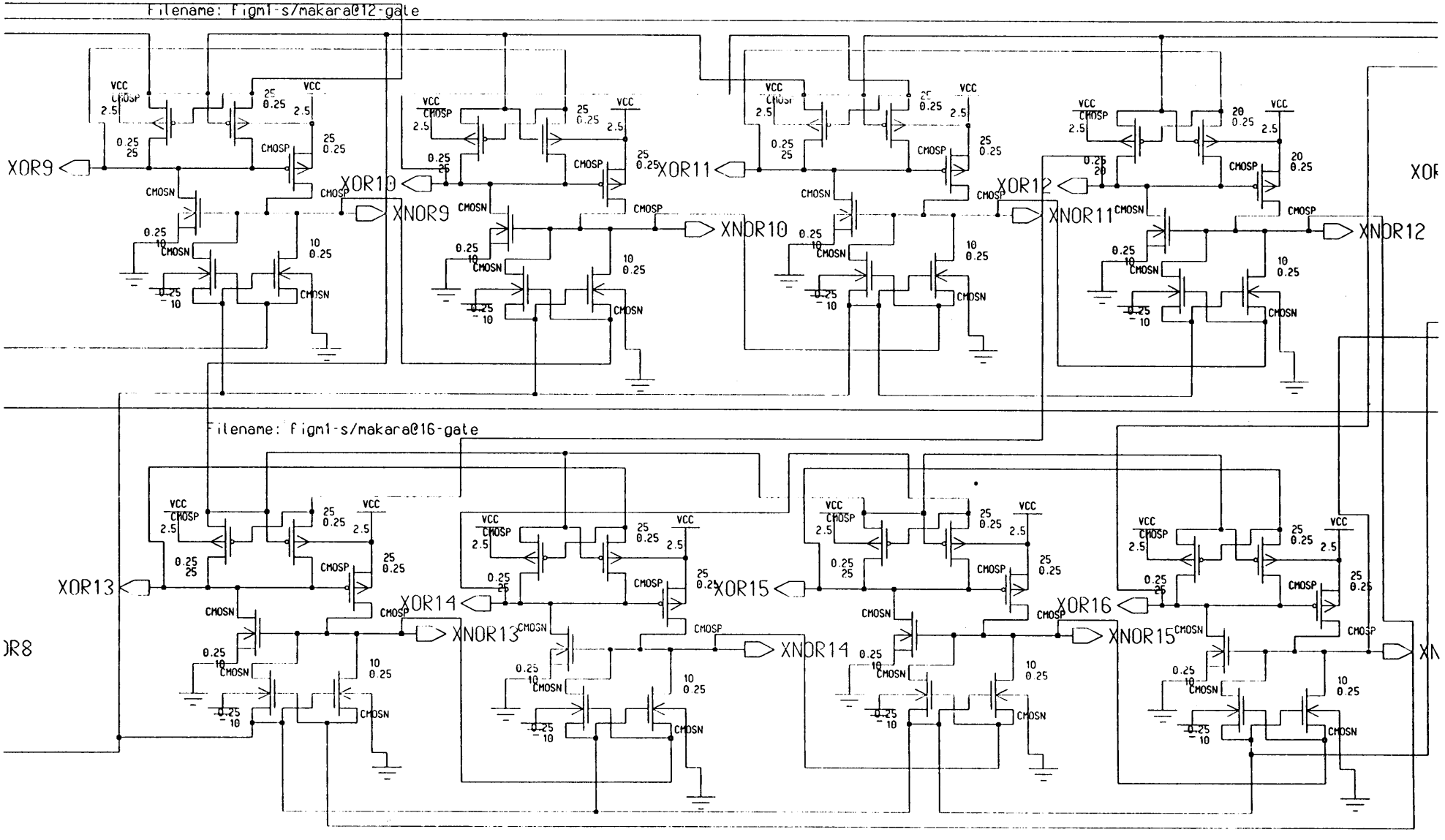

A
B
VCC
CMOSP
2.5
0.25
25
VCC
2.5
Filename: figM1
0.25
25
CMOSP
.25
0.25
AxorB
CAPACITOR
CMOSN
CMOSP
1P
aXNORb
0.25
10
CMOSN
CAPACITOR
10
0.25
1P
0.25
10
CMOSN
A
B

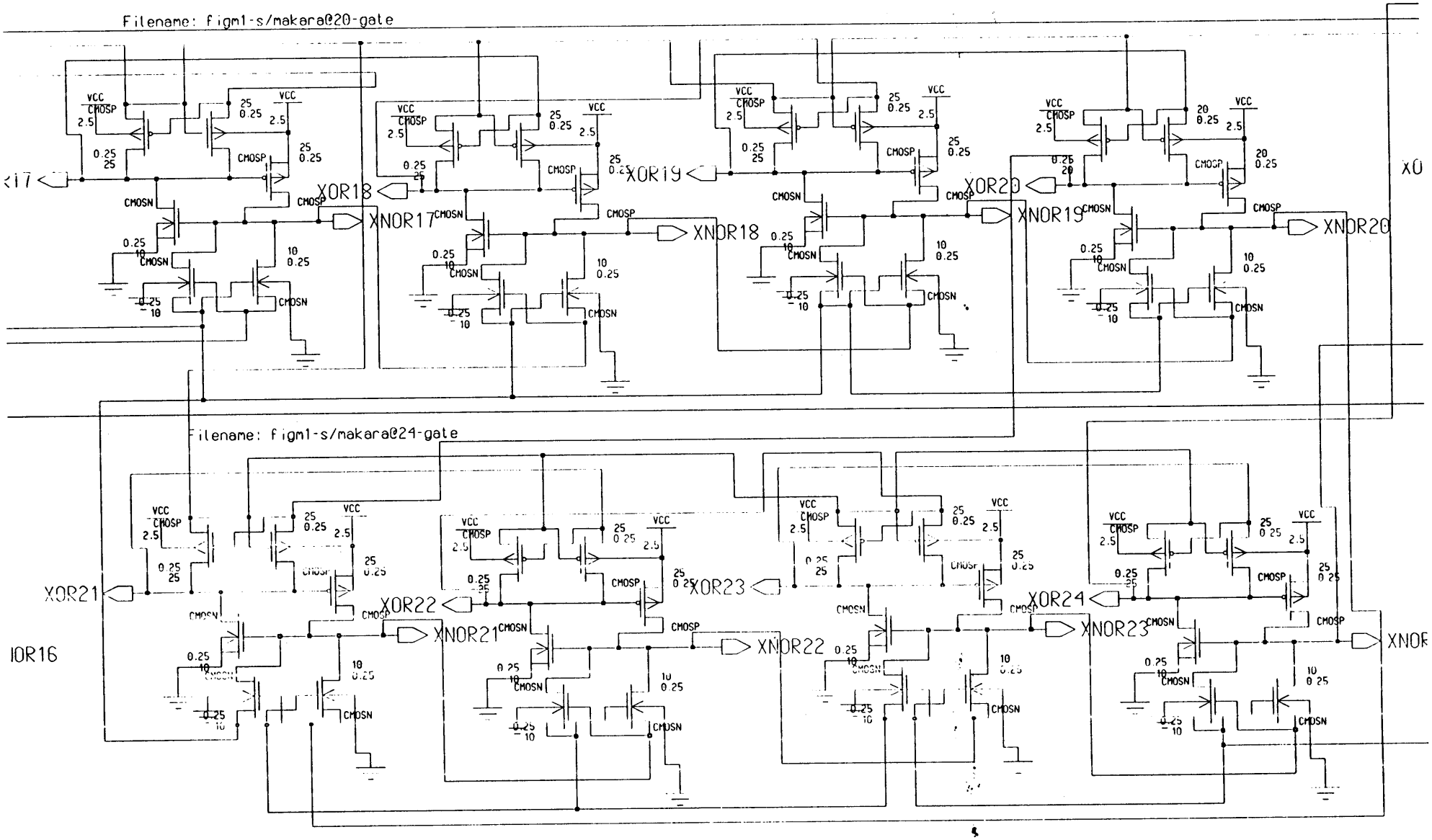

Filename: figm2/makara
VCC
CMOSP
2.5
0.25
2
CAPACITOR
10P
CMOSN
0.25
4
0.25
5
XNOR
VCC
5
0.25
15
2.5
0.25
CMOSP
CMOSP
CAPACITOR
7
0.25
10P
CMOSN
XOR
5
0.25
5
0.25
B'
CMOSN
CMOSN
A
A'
10
0.25
10
0.25
B
CMOSN
CMOSN

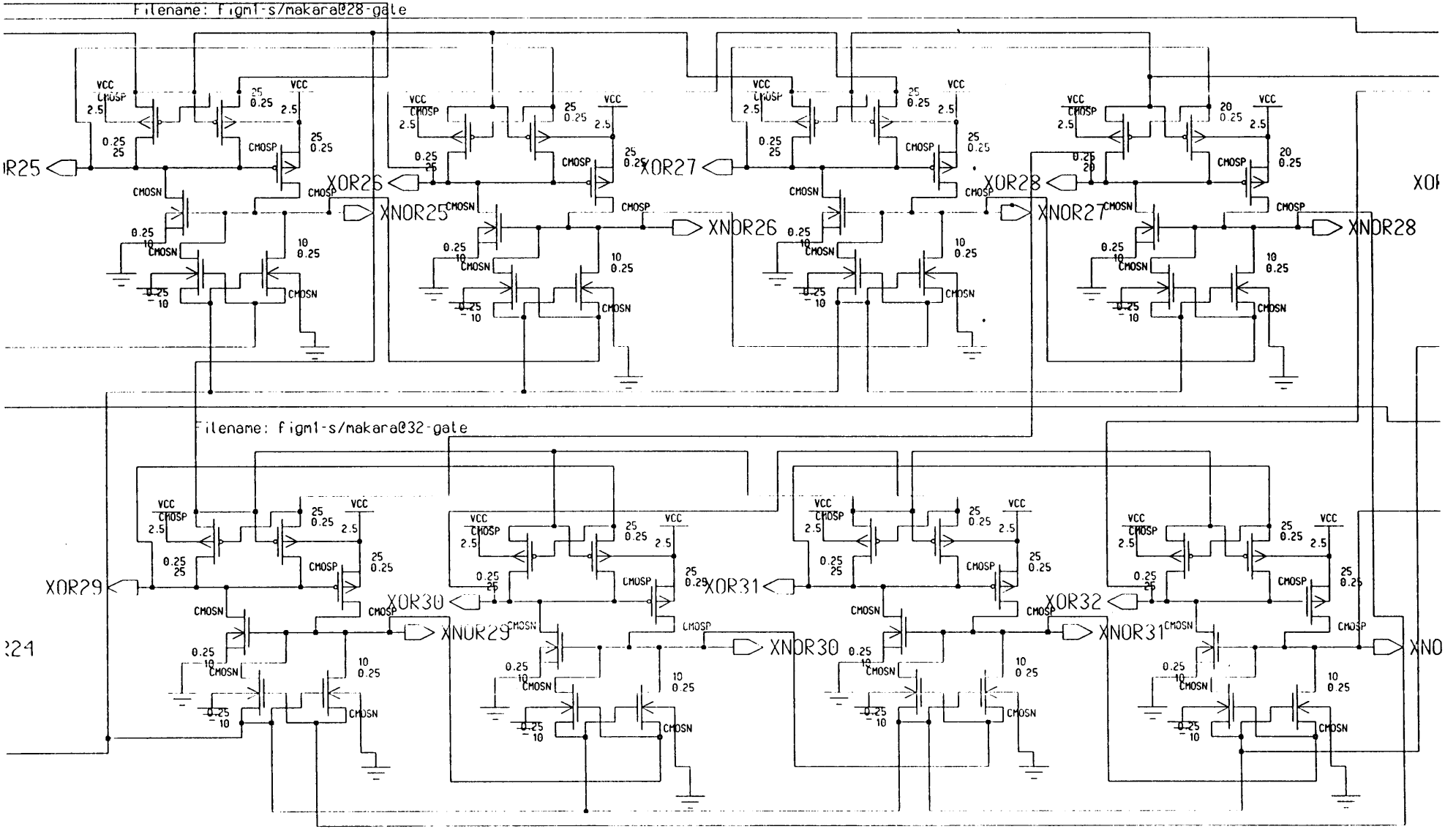

filename: figM3
VCC
CMOSP
2.5
CMOSP
0.25
0.25
XNOR
CAPACITOR
2
5
10P
CMOSN
0.25
4
5
0.25
VCC
15
2.5
0.25
CMOSP
CMOSP
CAPACITOR
7
0.25
XOR
10P
CMOSN
B'
A
B
A'
5
0.25
5
0.25
CMOSN
CMOSN
10
0.25
10
0.25
CMOSN
CMOSN

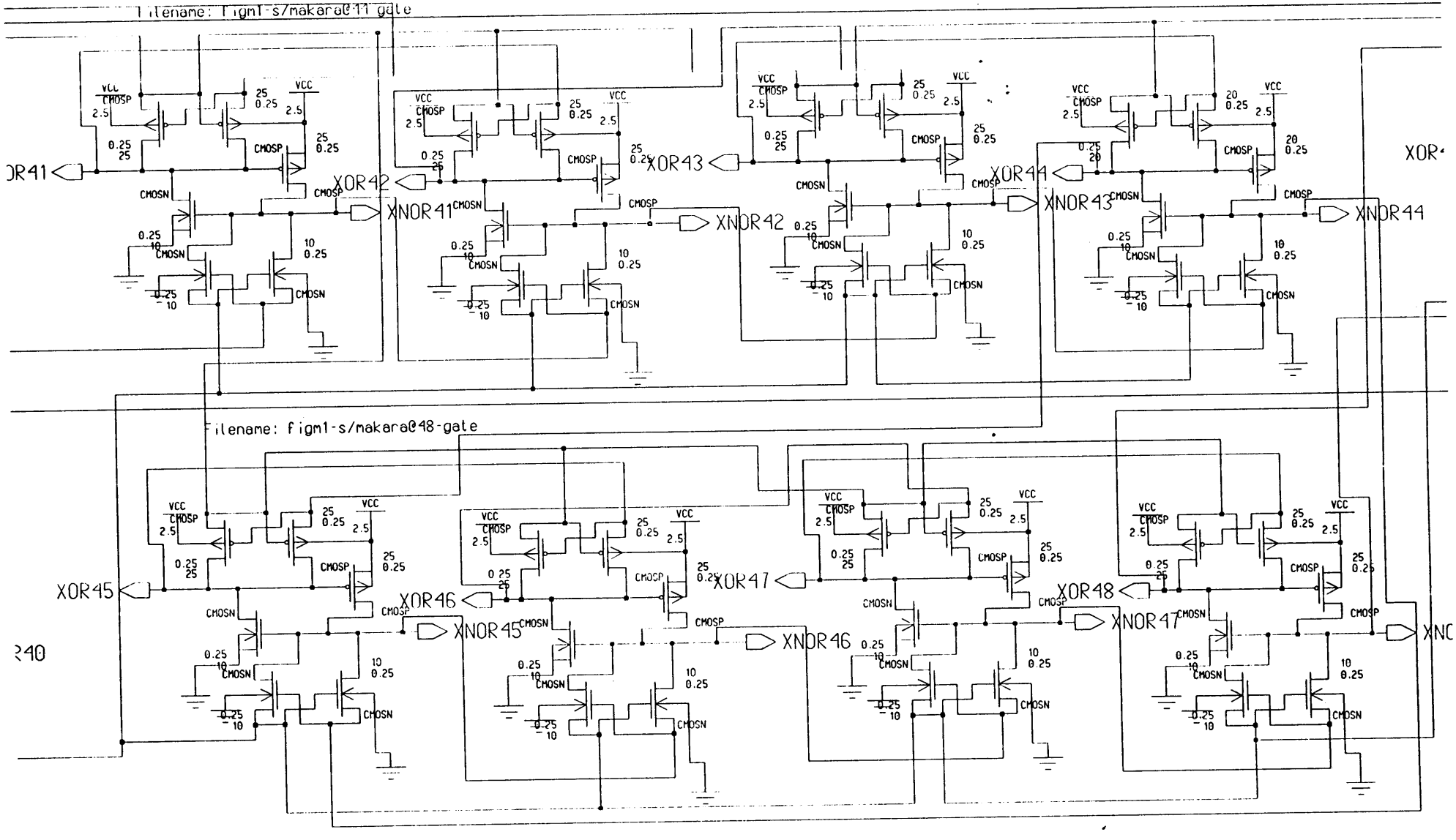

Filename: figm4/makara
CMOSP
VCC
2.5
0.25
15
XNOR
CAPACITOR
2P
CMOSN
0.25
6
15
0.25
VCC
2.5
CMOSP
CAPACITOR
7
0.25
XOR
2P
CMOSN
8
0.25
8
0.25
B'
CMOSN
CMOSN
A
4
0.25
4
0.25
B
CMOSN
CMOSN
A'

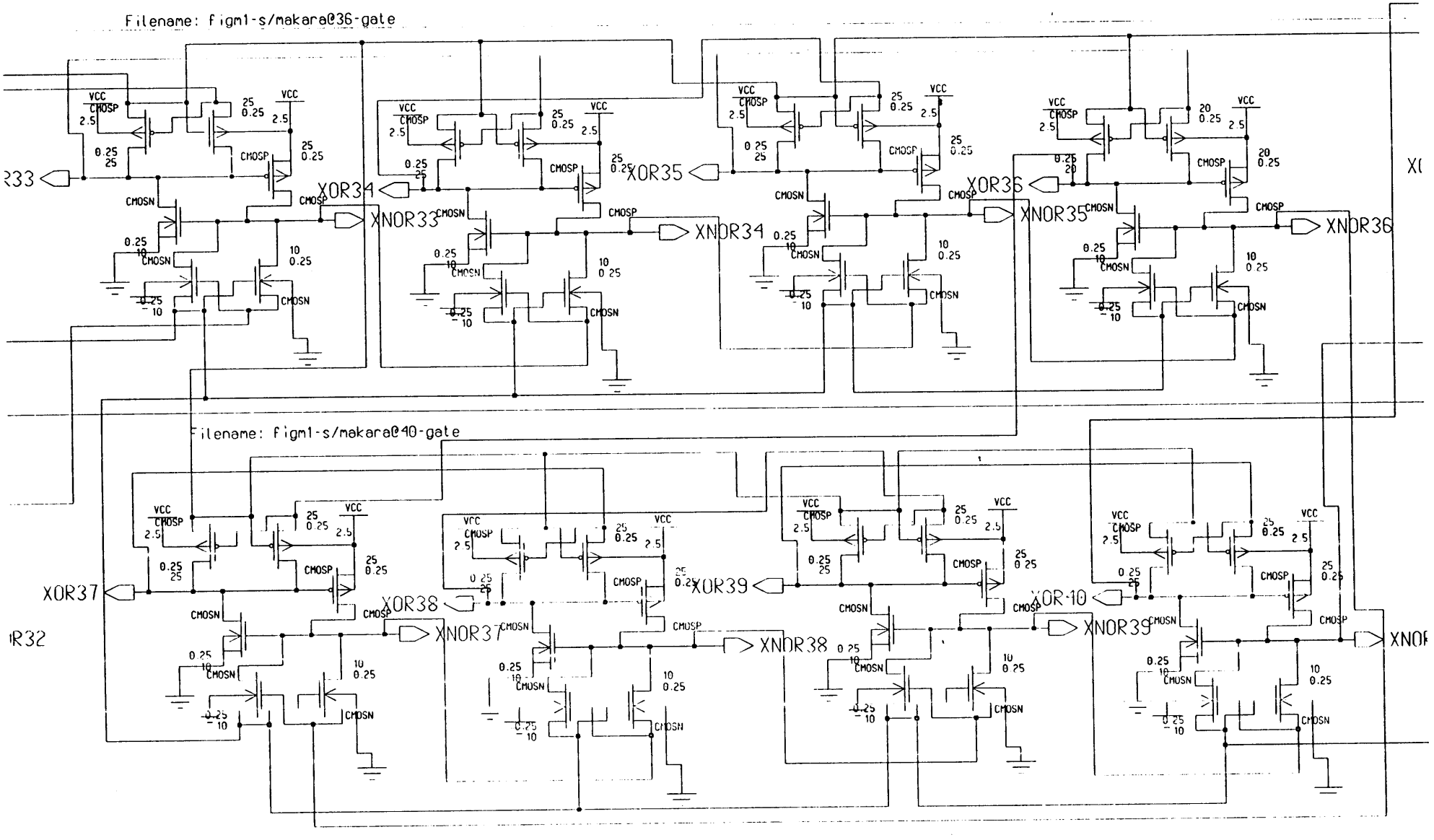

Filename: figm1-s/makara@4-gate
XOR1
XOR2
XOR3
XOR4
XNOR1
XNOR2
XNOR3
XNOR4
Filename: figm1-s/makara@8-gate
XOR5
XOR6
XOR7
XOR8
XNOR5
XNOR6
XNOR7
VCC
CMOSP
CMOSN
A

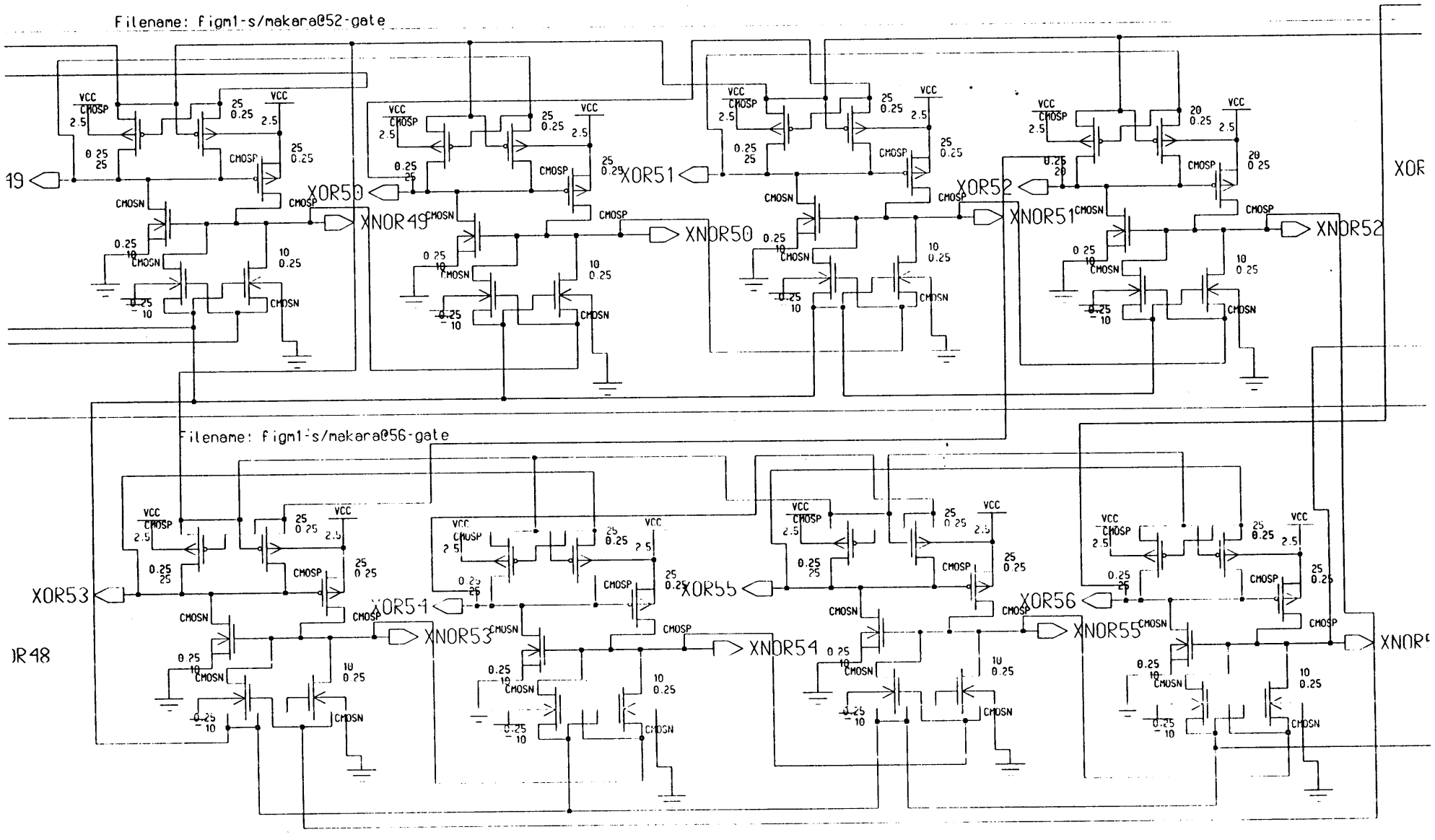

Filename: Fig1-s/makara@12-gate
XOR9
XOR10
XOR11
XOR12
XNOR9
XNOR10
XNOR11
XNOR12
Filename: Fig1-s/makara@16-gate
XOR13
XOR14
XOR15
XOR16
XNOR13
XNOR14
XNOR15
VCC
CMOSP
CMOSN

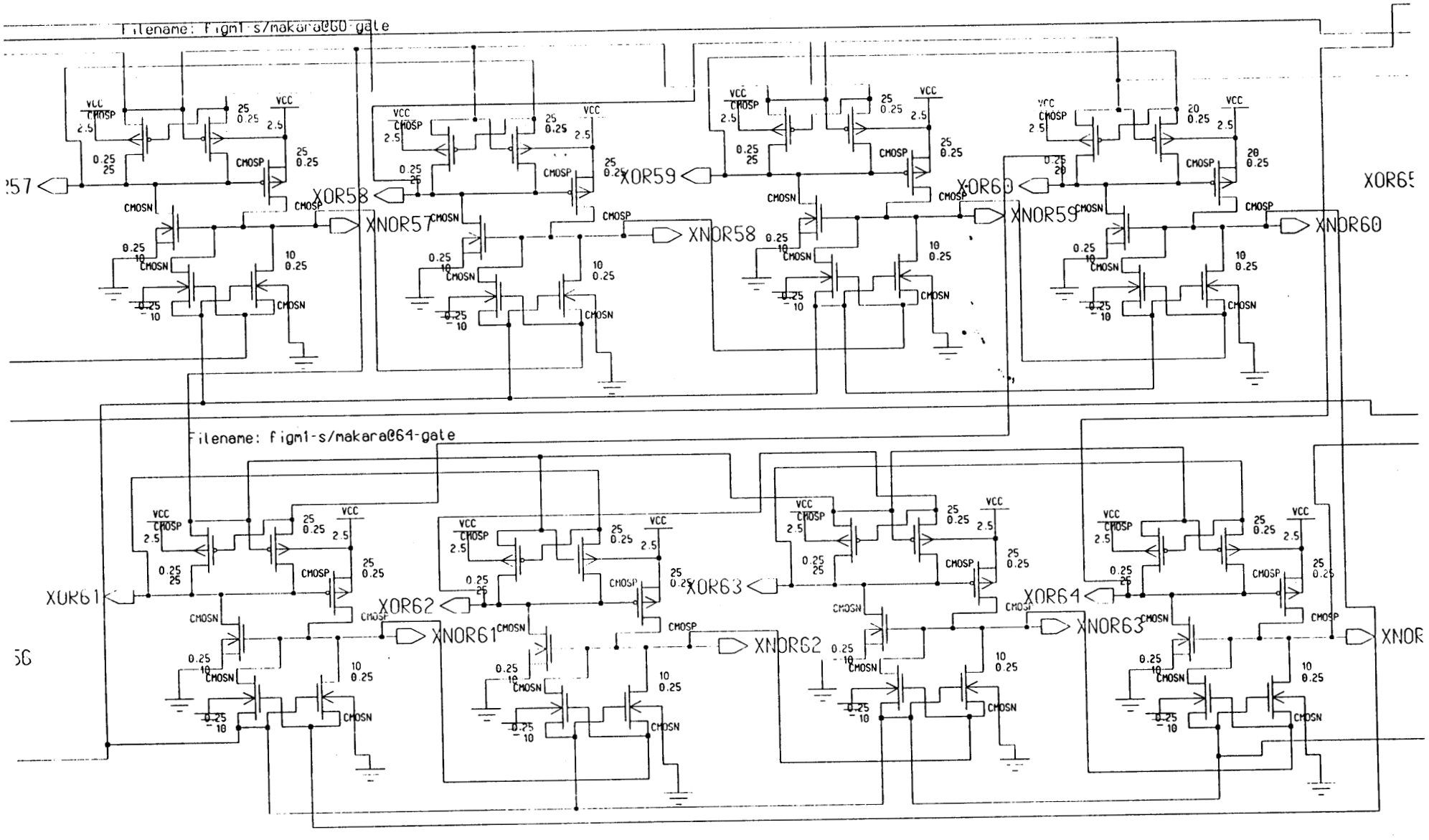

Filename: figm1-s/makara@20-gate
XOR18
XOR19
XOR20
XNOR17
XNOR18
XNOR19
XNOR20
Filename: figm1-s/makara@24-gate
XOR21
XOR22
XOR23
XOR24
XNOR21
XNOR22
XNOR23
VCC
CMOSP
CMOSN

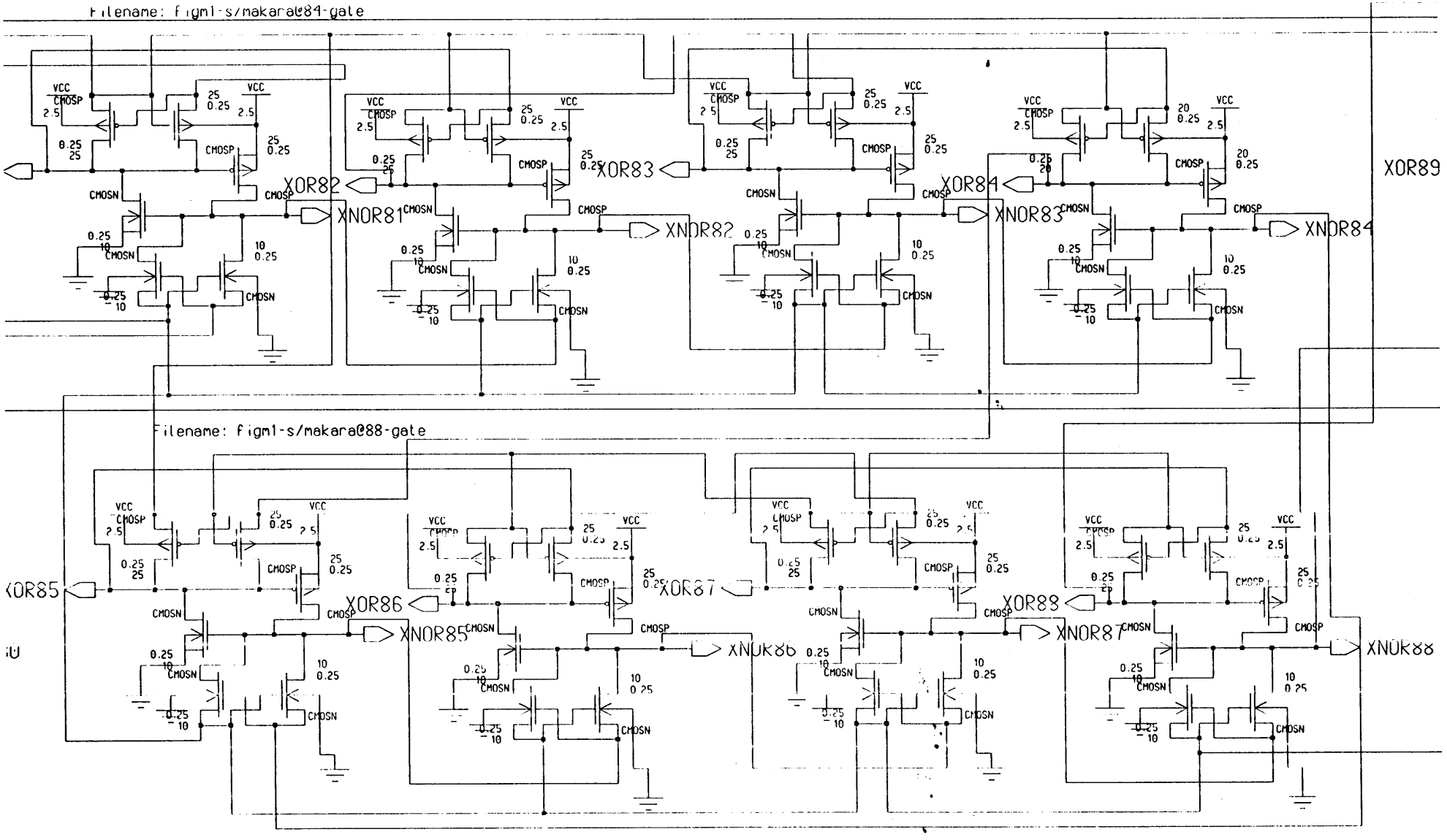

Filename: figm1-s/makara@28-gate
XOR25
XOR26
XOR27
XOR28
XNOR25
XNOR26
XNOR27
XNOR28
Filename: figm1-s/makara@32-gate
XOR29
XOR30
XOR31
XOR32
XNOR29
XNOR30
XNOR31
VCC
CMOSP
CMOSN


Filename: figm1-s/makara@41-gate
XOR41
XOR42
XOR43
XOR44
XNOR41
XNOR42
XNOR43
XNOR44
Filename: figm1-s/makara@48-gate
XOR45
XOR46
XOR47
XOR48
XNOR45
XNOR46
XNOR47
VCC
CMOSP
CMOSN

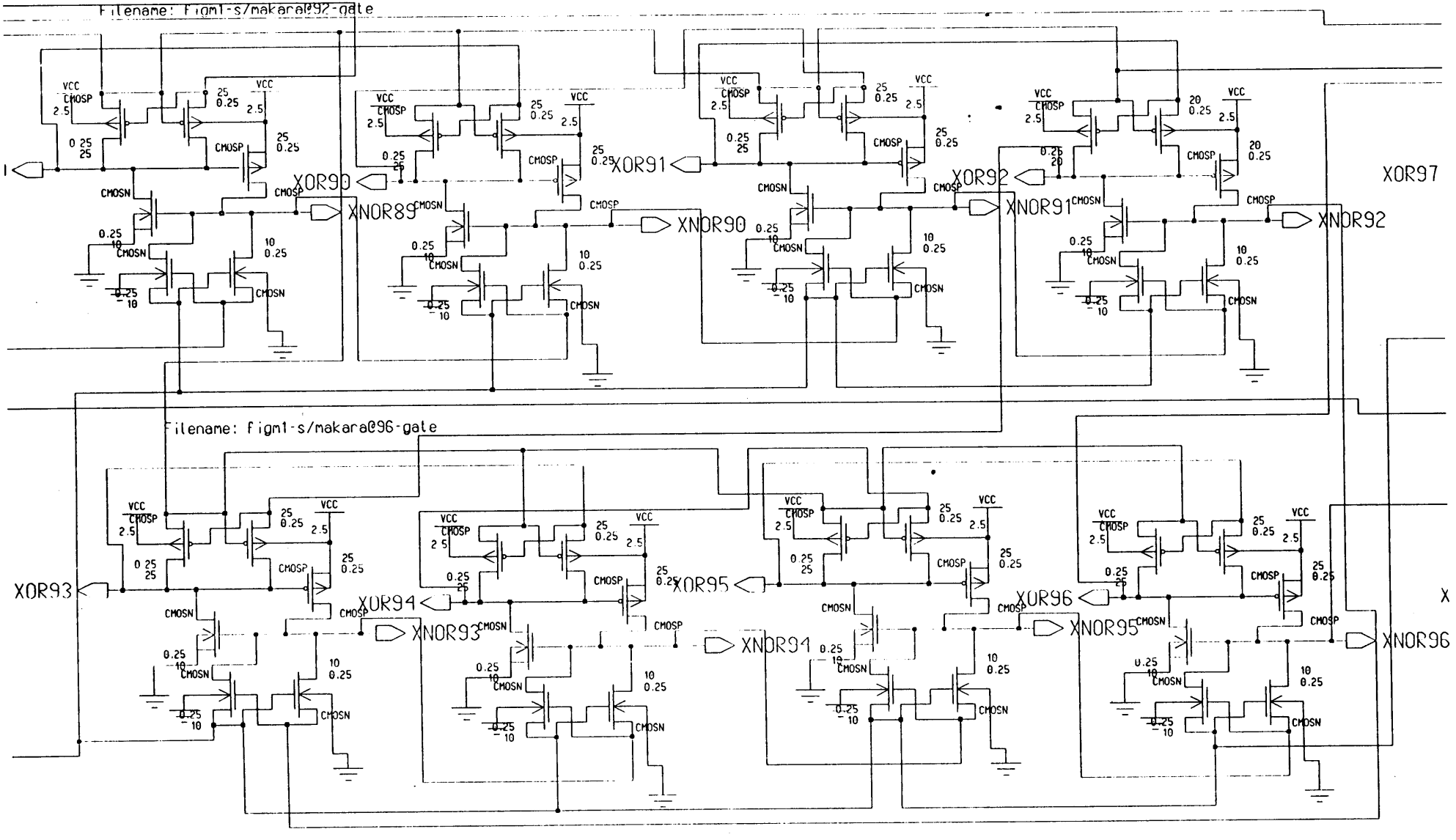

Filename: figm1-s/makara@36-gate
XOR34
XOR35
XOR36
XNOR33
XNOR34
XNOR35
XNOR36
Filename: figm1-s/makara@40-gate
XOR37
XOR38
XOR39
XNOR37
XNOR38
XNOR39
VCC
CMOSP
CMOSN

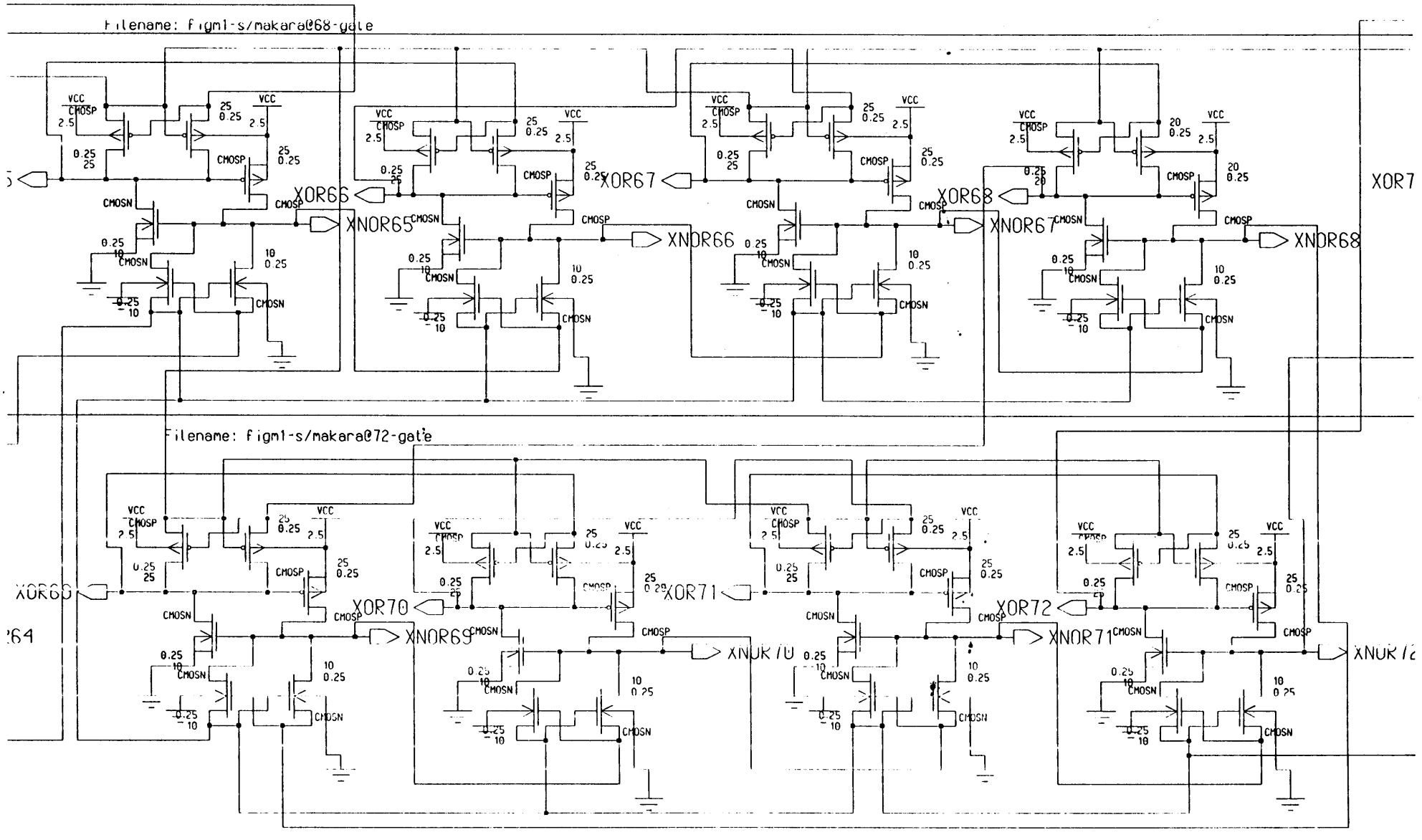

Filename: figm1-s/makara@52-gate
XOR50
XOR51
XOR52
XNOR49
XNOR50
XNOR51
XNOR52
Filename: figm1-s/makara@56-gate
XOR53
XOR54
XOR55
XOR56
XNOR53
XNOR54
XNOR55
VCC
CMOSP
CMOSN
2.5
0.25


Filename: figm1-s/makara@60-gate
XOR58
XOR59
XOR60
XNOR57
XNOR58
XNOR59
XNOR60
Filename: figm1-s/makara@64-gate
XOR62
XOR63
XOR64
XNOR61
XNOR62
XNOR63
VCC
CMOSP
CMOSN

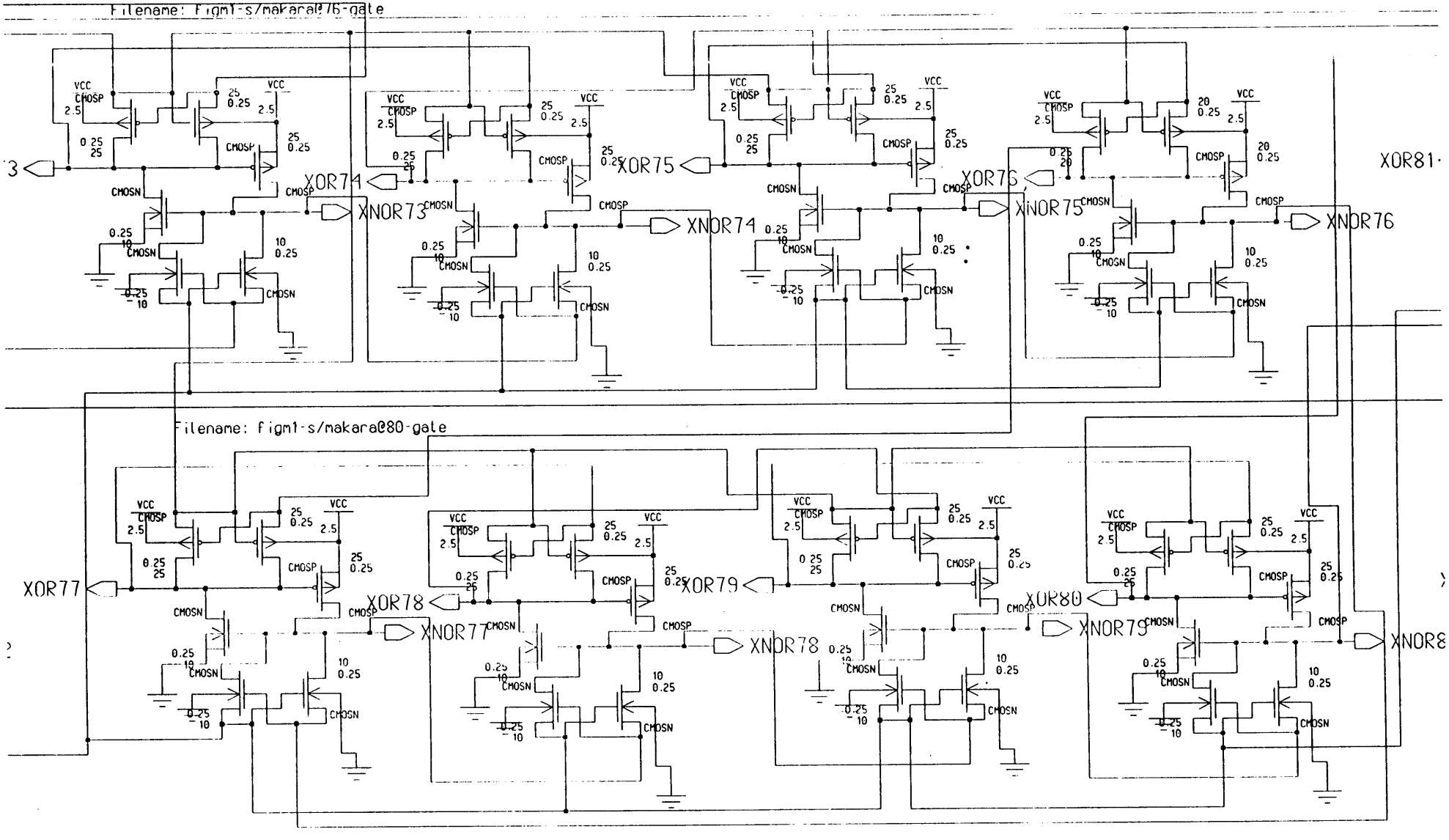

Filename: figm1-s/makara084-gate
XOR82
XOR83
XOR84
XOR89
XNOR81
XNOR82
XNOR83
XNOR84
Filename: figm1-s/makara088-gate
XOR85
XOR86
XOR87
XOR88
XNOR85
XNOR86
XNOR87
XNOR88
VCC
CMOSP
CMOSN

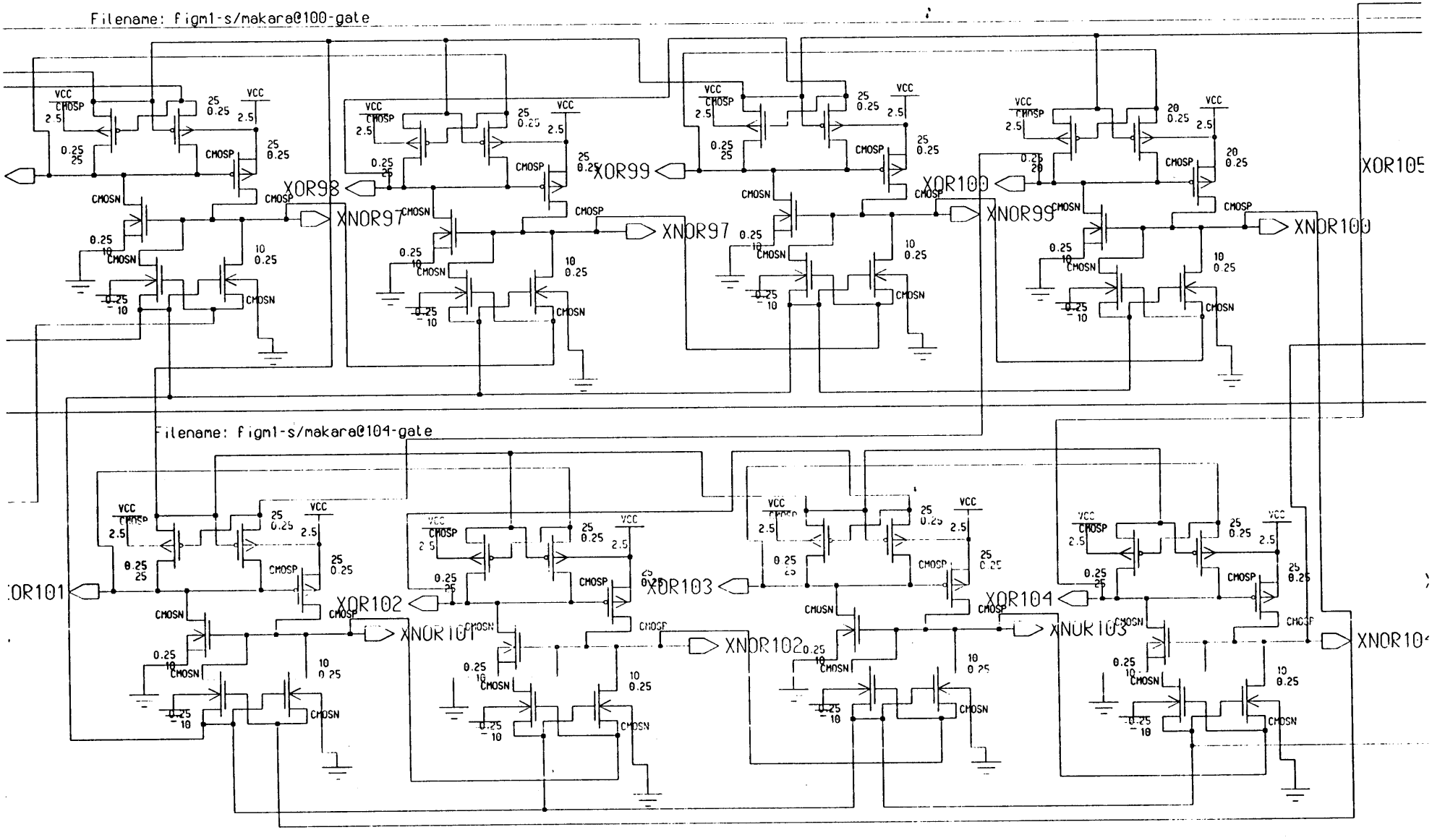
XI

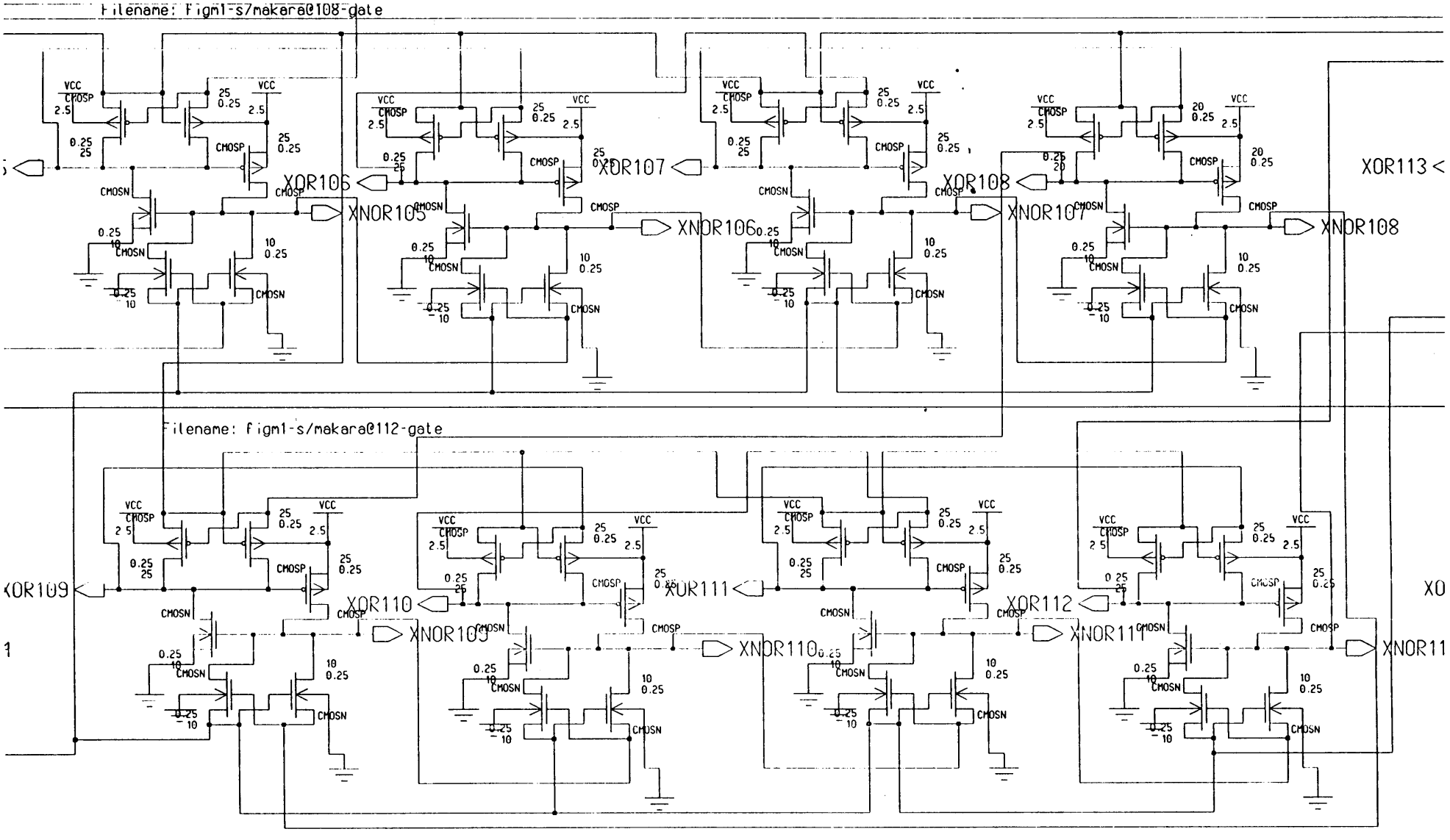

Filename: figm1-s/makara@92-gate
XOR90
XOR91
XOR92
XOR97
XNOR89
XNOR90
XNOR91
XNOR92
Filename: figm1-s/makara@96-gate
XOR93
XOR94
XOR95
XOR96
XNOR93
XNOR94
XNOR95
XNOR96
VCC
CMOSP
CMOSN

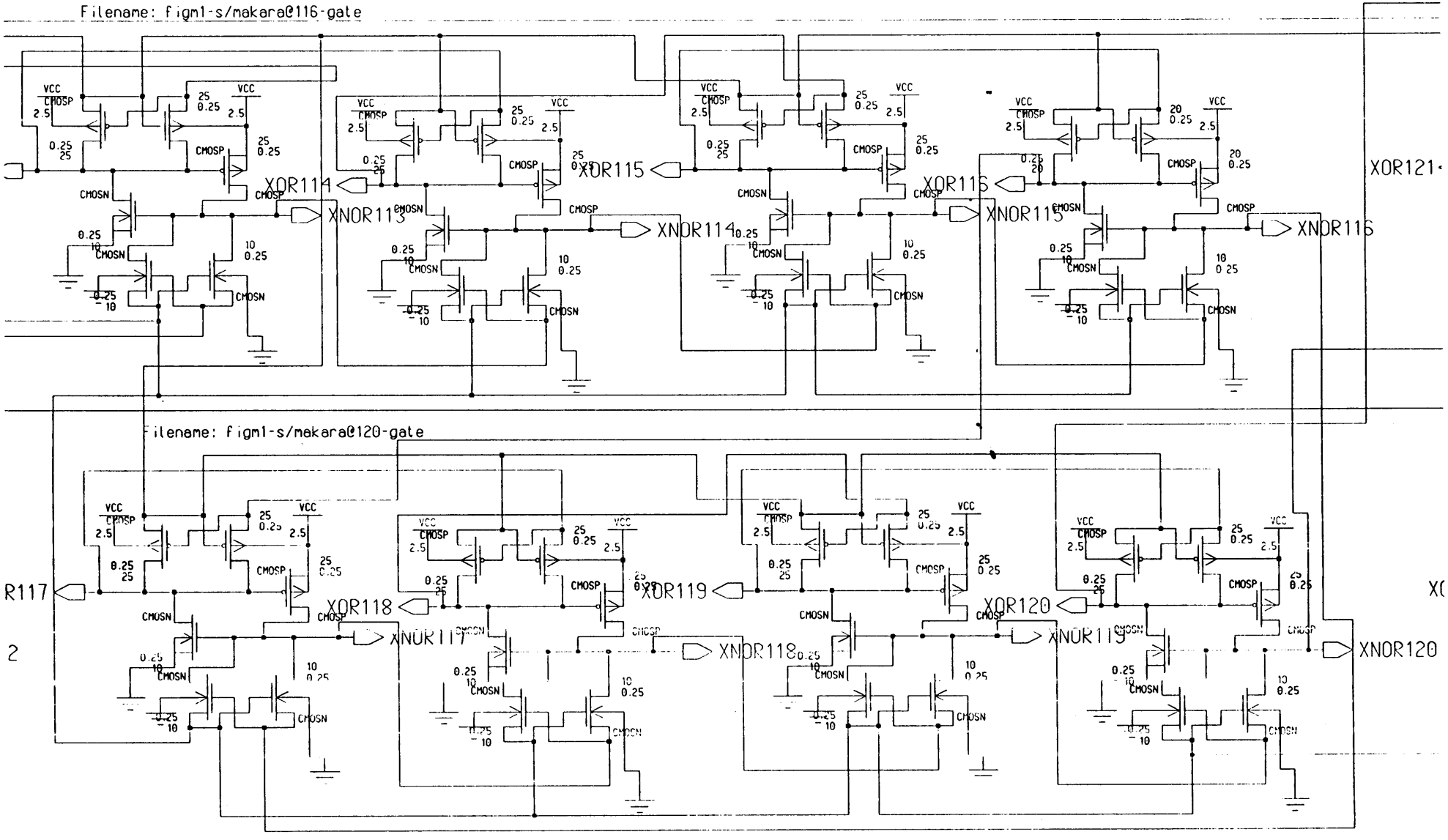

Filename: figm1-s/makara@68-gate
XOR66
XOR67
XOR68
XOR7
XNOR65
XNOR66
XNOR67
XNOR68
Filename: figm1-s/makara@72-gate
XOR70
XOR71
XOR72
XNOR69
XNOR70
XNOR71
VCC
CMOSP
CMOSN

IX


Filename: figm1-s/makara@76-gate
XOR74
XOR75
XOR76
XOR81
XNOR73
XNOR74
XNOR75
XNOR76
Filename: figm1-s/makara@80-gate
XOR77
XOR78
XOR79
XOR80
XNOR77
XNOR78
XNOR79
XNOR8
VCC
CMOSP
CMOSN


Filename: figm1-s/makara@100-gate
XOR98
XOR99
XOR100
XOR105
XNOR97
XNOR97
XNOR99
XNOR100
Filename: figm1-s/makara@104-gate
XOR101
XOR102
XOR103
XOR104
XNOR101
XNOR102
XNOR103
XNOR10
VCC
CMOSP
CMOSN


Filename: Figm1-s/makara@108-gate
XOR106
XOR107
XOR108
XOR113
XNOR105
XNOR106
XNOR107
XNOR108
Filename: Figm1-s/makara@112-gate
XOR109
XOR110
XOR111
XOR112
XNOR109
XNOR110
XNOR11
VCC
CMOSP
CMOSN


Filename: figm1-s/makara@116-gate
XOR114
XOR115
XOR116
XOR121
XNOR113
XNOR114
XNOR115
XNOR116
Filename: figm1-s/makara@120-gate
R117
XOR118
XOR119
XOR120
XNOR117
XNOR118
XNOR119
XNOR120
VCC
CMOSP
CMOSN

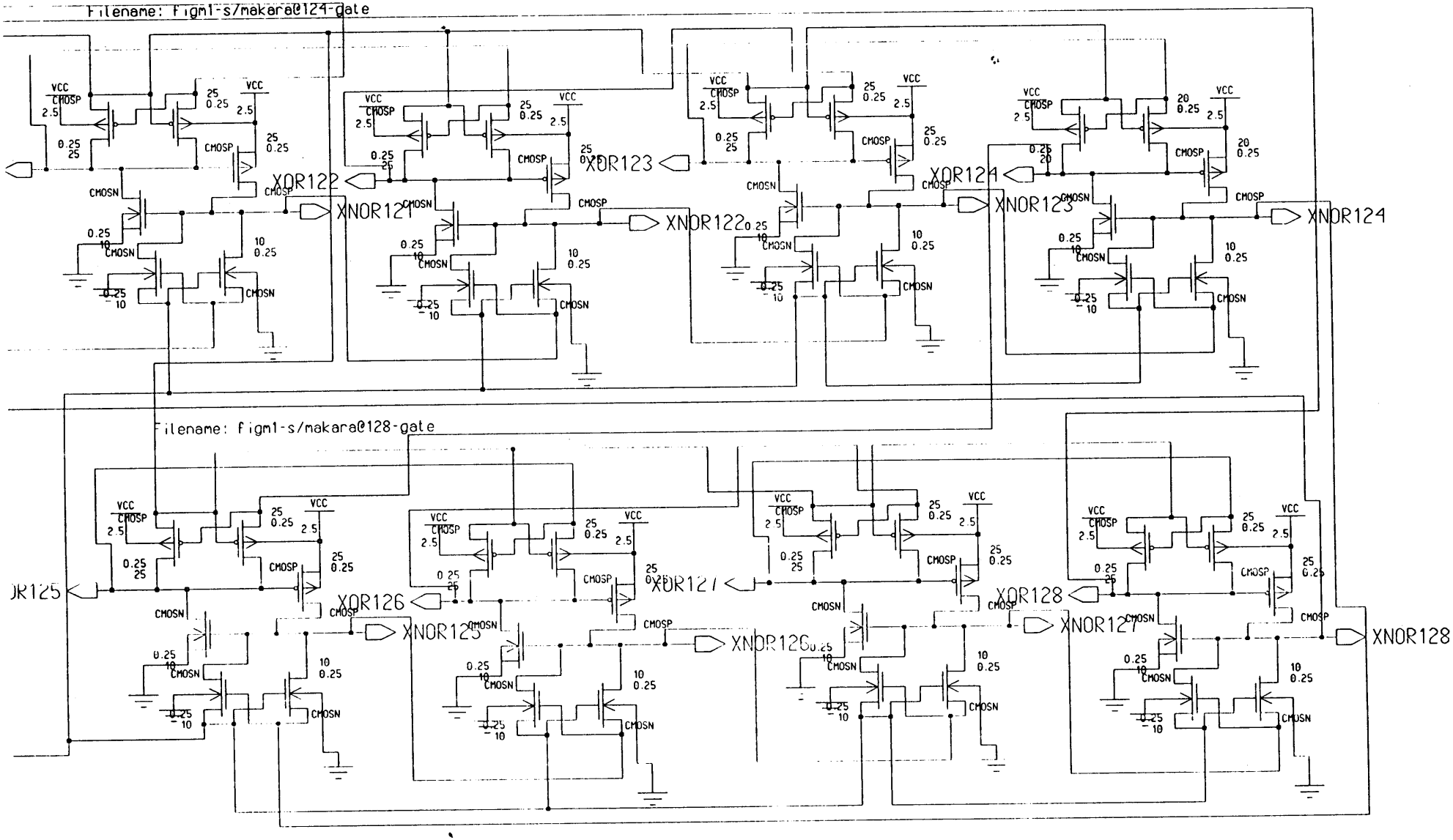

Filename: figm1-s/makara@124-gate
XOR122
XOR123
XOR124
XNOR121
XNOR122
XNOR123
XNOR124
Filename: figm1-s/makara@128-gate
XOR125
XOR126
XOR127
XOR128
XNOR125
XNOR126
XNOR127
XNOR128
VCC
CMOSP
CMOSN

Fig.3(b) Inverter-base XNOR structure

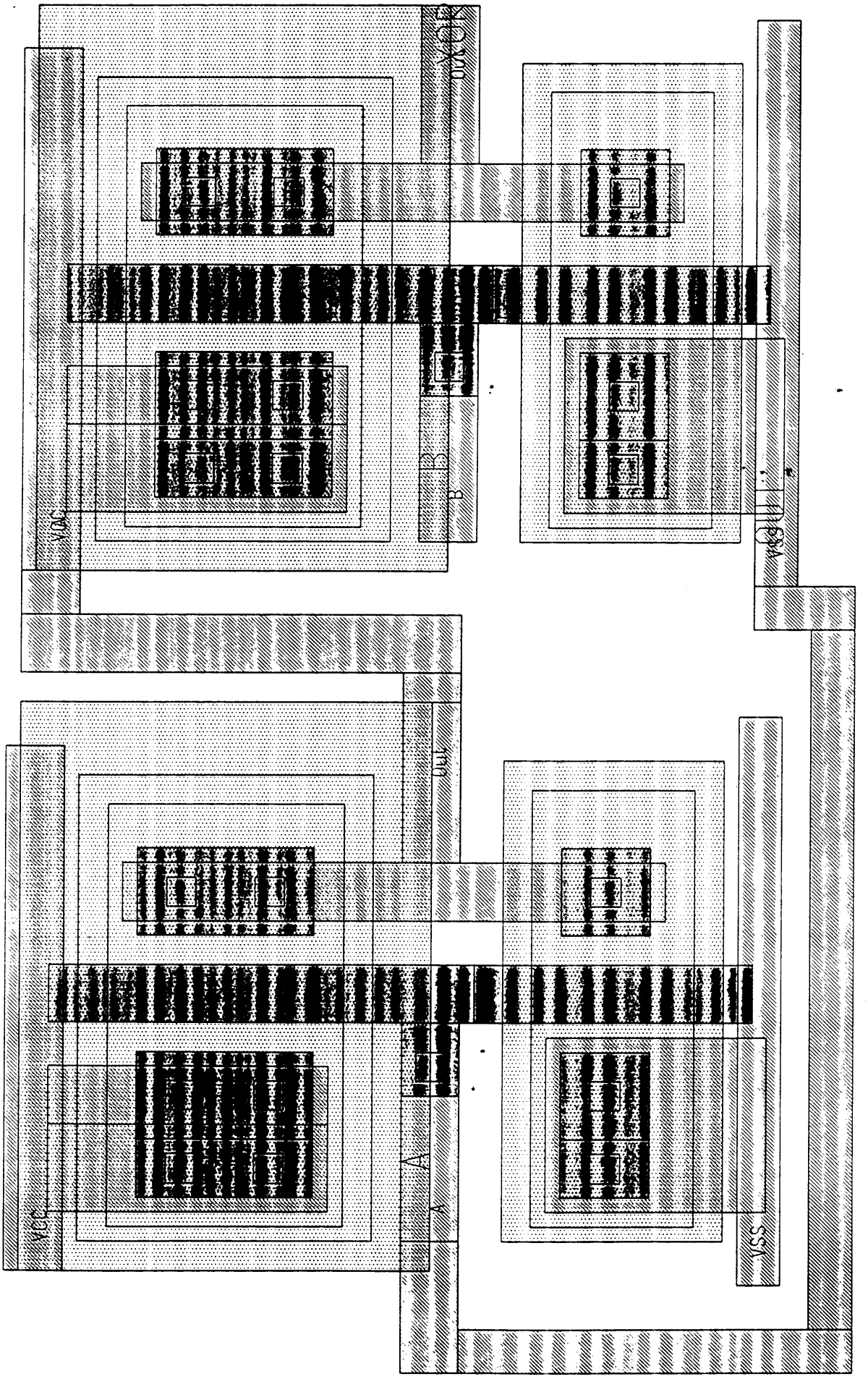


Fig.3 (a) Inverter-base XOR structure

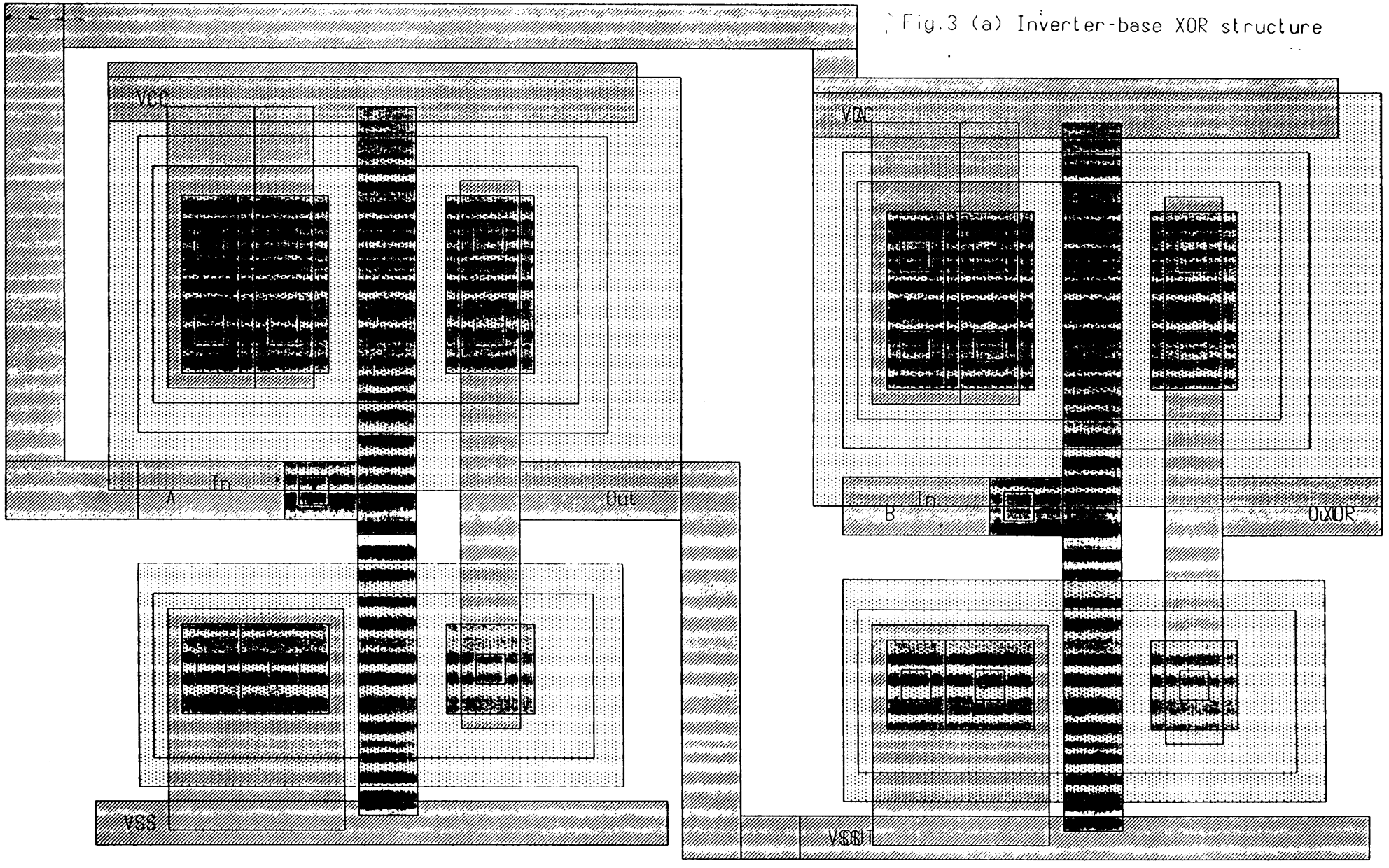


Fig.3(a) Inverter-base XNOR structure driving output

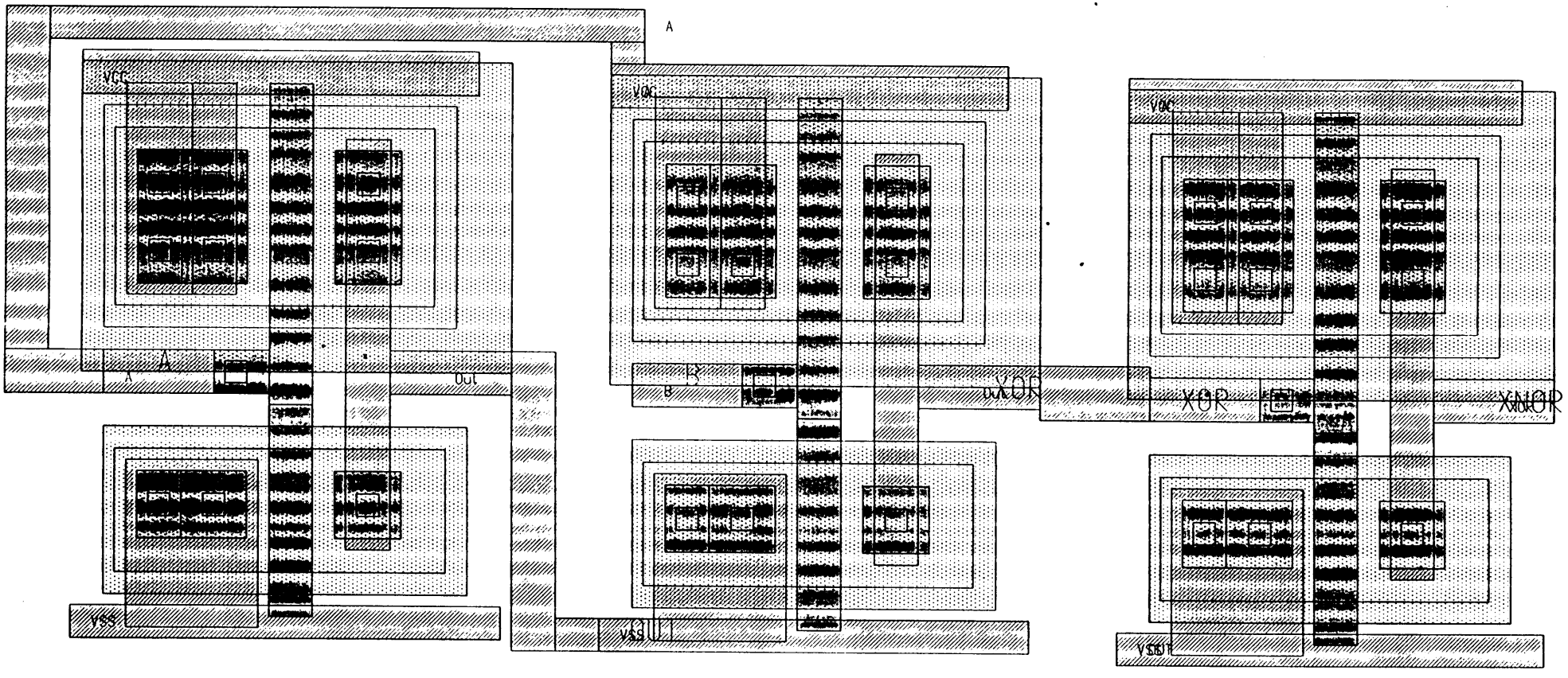


Fig.4(b) Inverter-base XOR structure driving output