Characterization of NMOS and PMOS Transistors on Silicon-on-Insulator Substrates.

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A thesis submitted to the faculty of the

Oregon Graduate Institute of Science and Technology

in partial fulfillment of the requirements for the degree

Master of Science in Electrical Engineering.

August, 1997

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Dedication

I dedicate this work to my wife Jennifer, my son John, and my daughter Avery.

Acknowledgments

I would like to thank my advisor, Raj Solanki, for his patience and consistent encouragement. He, better than anyone, understood the changes I was going through. He was an exceptional teacher and his good humor made this part of my education a positive experience.

I am thankful for both the financial and educational support from Planar Systems. I especially want to thank Larry Arbuthnot, Tin Nguyen and Pat Green. Each of these individuals has provided me with instructional experiences in the area of process engineering that can not be obtained in a classroom.

Finally, I thank my wife, Jennifer. This is the second dissertation she has experienced with me. With two young children, John William and Avery Harlow, she has worried more and slept less than any person I've ever known.

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Abstract

The goal of this investigation has been to improve process-device simulations of reverse breakdown for the high voltage DMOS transistor fabricated on silicon-on-insulator (SOI) substrates. Parametric data collections and Silvaco process-device simulations were designed to characterizeo reverse breakdown voltage (VBR) including characterization of current-dependent walk-out, and examine threshold voltage (Vt) shift in the parasitic edge devices of silicon mesa structures. Through careful attention to methods of data collection, the phenomenon of VBR walk-out was characterized. Although difficult to model, the results of the simulations were optimized to actual DMOS device performance by inclusion of lattice heating (electrothermal model) and demonstrate how changes in the p-n junction depth in the n-drift region of the DMOS device may reduce VBR. The mechanism for VBR walk-out was found to be related, in part, to irreversible changes that facilitated DMOS voltage-regulation of light production in active matrix electroluminescent (AMEL) displays. Based on these simulations, and their comparisons to the measured data, ways to improve device performance are proposed. These devices are used in active matrixhead mounted electroluminscent (AMEL) displays.

Chapter 1
SOI transistors.

1.1 Background.

Silicon-on-insulator (SOI) is silicon dioxide (SiO_2) sandwiched between crystalline silicon. The layer of SiO_2 is usually between 0.2 and 2µm thick placed beneath a variable thickness of silicon. This arrangement is essentially equivalent to epitaxial silicon crystal atop SiO_2 on a silicon wafer. The goal is to create a high quality silicon layer on top of SiO_2 . Two parameters are central to SOI processing: the thickness of the silicon film and the buried oxide (BOX). There are three leading SOI material technologies: SIMOX (Separation by IMplated OXygen), BESOI (Bond and Etched back SOI), and ISE (isolated silicon epitaxy, by seed/zone melting recrystallization) that can produce very thin SOI films (1-5). In order to realize its advantages, SOI processing must satisfy three criteria: (1) the BOX must be formed with adequate dielectric isolation characteristics, (2) the isolated silicon (top) must maintain sufficient mono-crystallinity, and (3) thermally oxidized SiO_2 used to cover mesa-like silicon islands must form a continuum with the BOX (2-4).

ISE processed SOI wafers are formed from a single crystalline silicon wafer with thermally (usually steam) grown oxide on its surface (2). Oxide is removed from the perimeter prior to depositing amorphous silicon. A graphite strip heater is then scanned across the surface (~5mm above the surface) of the amorphous silicon, heating it to near 2300°C. The silicon that was exposed along the wafer's perimeter acts as a seed for epilayer growth of single crystalline silicon on top of SiO_2 (2). BESOI wafers are formed by anneal-bonding two oxidized wafer surface together (4). The top wafer's backside, now facing up, is then etched back to the desired silicon thickness and then polished. A major drawback of this process for SOI fabrication is contamination

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of the bonding SiO_2 surface that introduces defects into the resulting BOX layer (5).

Compared to the SOI technologies listed above , SIMOX is the most mature process. A 0.2-0.4um thick BOX can be processed by internal oxidation after deep implant (>150KeV) of oxygen ions into silicon. High temperature anneal (1200-1400°C) is needed to ensure silicon recrystallization after implant damage (5). Formation of SiO_2 is accompanied by emission of interstistial silicon atoms produced during the oxygen implant. The silicon interstistials migrate and reconstruct the surface, which alleviates the damage caused by incoming oxygen ions. Ideally this should relieve oxidation-related stain, however, migration paths are blocked by the forming SiO_2. Increased defect densities and interface roughness have also been reported at SIMOX BOX formations (1). Although present, BOX defects do not usually create problems for devices fabricated on SOI wafers.

One of the advantages of SOI is that the capacity to electrically isolate transistors by etching silicon back to the underlying BOX layer. This process leaves a silicon "mesa" that is completely isolated from its neighboring mesas. Oxide grown on the silicon mesa, for the purposes of gate oxide formations, also grows down the mesas' side wall until it meets the BOX layer. Silicon oxidation near sharp corners creates stress related defects and interface roughness. If located near an active silicon area these defects can lead to higher local electric fields, higher leakage currents and lower dielectric breakdown (6,7). Oxide defects act as trap sites for charges that have profound influences on the performance of nearby electrical devices. The degree to which these defect sites charge and discharge depends on the voltage applied and the rate of the device operation. In addition, SiO_2 has low heat conductivity and will retain heat generated during device operations. Self-heating of the silicon active regions will increase lattice vibrations and adversely affect carrier mobility (8).

SOI simplifies transistor fabrication because dielectric isolation is located

under a layer of single crystal silicon. This arrangement reduces processing cost associated with fabricating isolation trenches, reduces the overall thermal budget, and allows for higher speed operation and circuit integration (7-9). Improved transistor isolation offered by SOI wafers is especially important in preventing parasitic latch up involving parasitic bipolar devices when arrays of NMOS and PMOS transistors are operated at higher voltages (see figure 1, references 7,8).
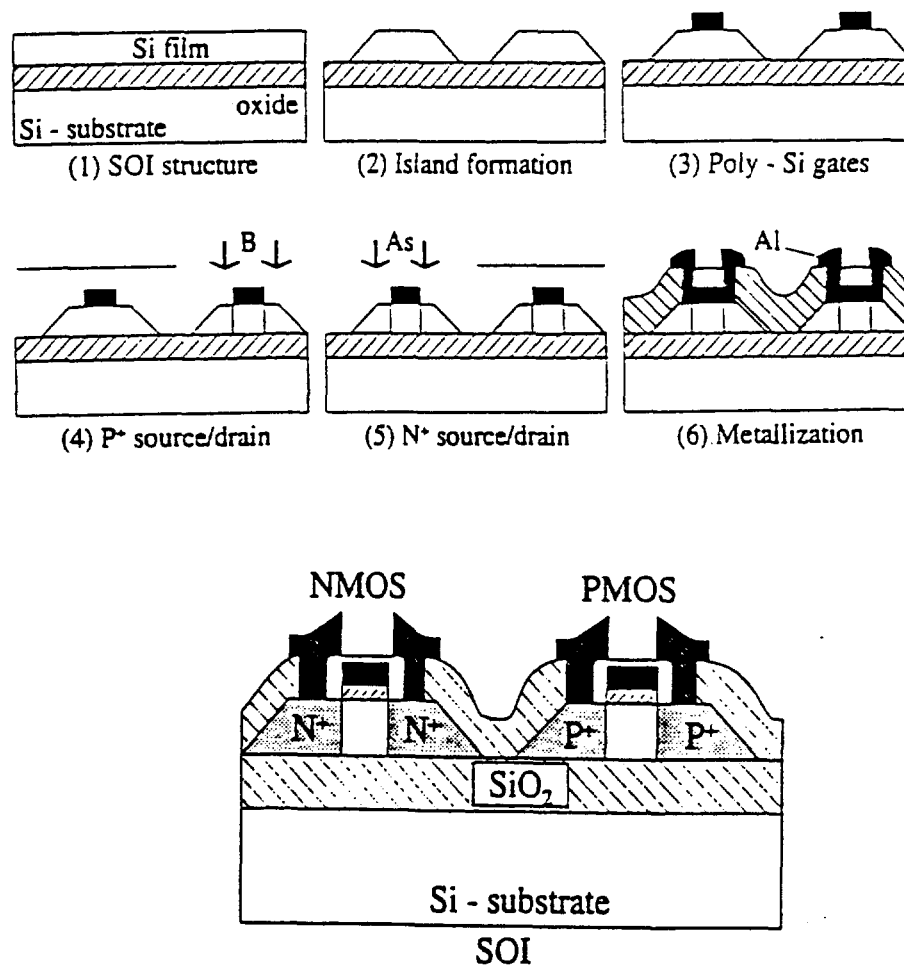
Figure 1: General sequence for processing of NMOS and PMOS transistors on SOI wafers (adapted from Cristolveanu and Li (1995)).

Advantages of SOI device fabrication must be carefully weighted against its disadvantages. The key disadvantage of SOI transistor fabrication is the floating body effect which results from charge accumulation. The body of an SOI device is isolated and is left floating so that its potential under DC conditions is determined by the balance of generation and recombination currents. Generation currents arise from (i) impact ionizations near the drain (high field end) and (ii) leakage at the drain's p-n junction and the gate. This is balanced against recombination with holes which accumulate in the isolated body. For NMOS devices the net result of these dueling currents is a positive body potential which reduces the threshold voltage and increases the drive current. The floating body effect puts a forward bias on the body/source junction and results in a steep subthreshold swing (11). Positive feedback from impact ionization can lead to low drain/source breakdown (12). Floating body effects can be alleviated by fabricating a grounded body tie with the silicon mesa (6).

The goal of the work leading to this thesis has been to identify problems and investigate process techniques to improve the operation of pixel control circuitry in active matrix electroluminescent AMEL displays. The central focus has been on two transistors: a PMOS transistor (Pixel-P) governing access to the hold node, and a high voltage DMOS (Pixel-HV) governing the voltage drop across the electroluminescent (EL) layer placed in series with its drain. Light production by the EL layer is a function of the field across it. When the channel of the DMOS is inverted (conducting) the field is centered within the EL layer, i.e., the entire voltage drop occurs across the EL layer. When the channel is not conducting, a field sufficient to cause the reverse breakdown of the p-n junction of the drain must precede any voltage drop across the EL layer. As such, the electric field (=voltage drop) across the EL stack is reduced and no light is emitted. The principles of AMEL function are discussed elsewhere (17) and are not the focus of this thesis.

Measurement of electric parameters provide the means for rapid,

accurate characterization of the individual devices and components of which circuits are made. It provides information for process control, for engineering new processes and devices, and provides device characteristics required for circuit modeling and design (18). The primary goal of each test effort was to collect information for engineering decisions.

Parametric control measurements (PCM) of circuits provided a final evaluation of the interaction between materials and processing. PCM were designed to determine yield- and/or performance-limiting processes. To be useful, PCM required: 1) precise, sensitive and accurate measurements; 2) detailed and rapid analysis of results; and 3) PCM database tracking. Feedback to wafer lots in process was in terms of the best physical models, however, emphasis was placed on sensitivity to explain unexpected recurring results.

Individual devices were located either on special test chips or in the scribe lines. Routine DC PCM were performed on representative structures (see list below). The primary focus was on Pixel-HV and -P transistors used in the pixel control and 3x10 NMOS(LxW) and 3x10 PMOS transistors used in the select scanner circuitry. Where indicated, special-purpose PCM and analysis were designed and performed. These include stress test, resistance and capacitance measurements. Whenever possible, data analysis and correlation to processes were kept simple.

Listing of parameter values extracted from transistors.

Threshold voltage, V_t (front gate)

Transconductance, Gm

Saturation (drive) current, I_s or I_{sat}

Reverse Breakdown voltage, VBR
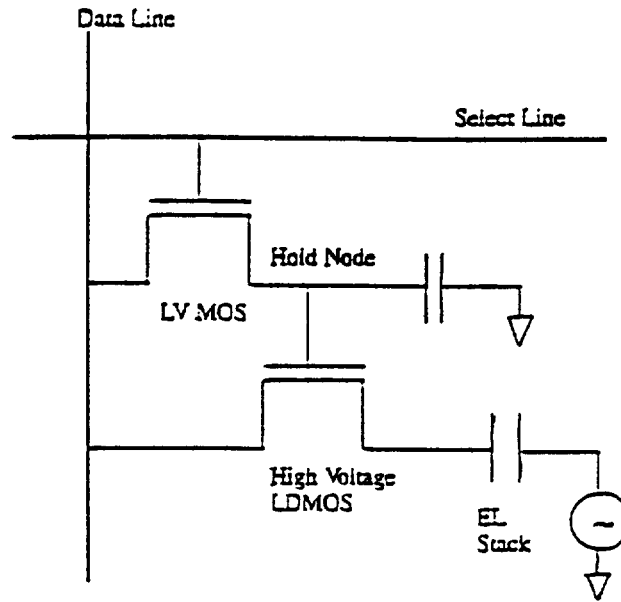
Figure 2. Pixel control circuit design. Low voltage PMOS (LVMOS) refers to Pixel-P in this text and represents the access transistor to the hold-node (capacitor) which controls the high voltage NMOS transistor with a lightly doped drain (LDMOS) called Pixel-HV (S. Ahmed, 1996). The state of Pixel-HV (gate on or off) determines the voltage drop across the electroluminescent (EL) stack.

1.2 Equations describing basic MOSFET parameters.

Valuable parameters governing the behavior of the MOS transistor can be extracted from measuring MOSFET operation in the linear region just past the subthreshold regions. Equations used to determine these MOS parameters are described by Pelloie (see reference 18). Abbreviated terms used below are defined as follows: I_d=drain current; μ=mobility of carrier; C_{ox}=gate oxide capacitor; W=width of channel; L=length of channel; V_g=gate voltage; V_t =threshold voltage; and V_d=drain voltage. In the linear region at small drain voltage the current can be written as (18):

$$I_d = \mu^* C_{ox}(W/L)[(V_g - V_t)V_d]$$

Transconductance (Gm) is expressed as (18):

$$Gm = dI_d/dV_g = C_{ox}{}^*V_d{}^*(W/L)[\mu + (Vg - V_t)d\mu/dV_g]$$

Its maximum value occurs at the threshold voltage:

$$Gmmax = \mu^*(W/L)^*C_{ox}{}^*V_d$$

and represents the maximum slope found at the inflection point of the curve $I_d(V_g)$ which corresponds to the transition point between weak and strong inversion regions (18).

1.3 Equipment.

SOI wafers were mounted on grounded chucks with heating capacity (Micromanipulator inc., model HSM) and probed using a Micromanipulator probe station (Micromanipulator inc., model 7000-LTE, Carson City, Nevada) , with connections to both a HP4156A Precision semiconductor parameter analyzer and HP4275A multifrequency LCR meter (Hewlett-Packard, San Jose, CA).

1.4 Thesis Overview.

This thesis has been organized into three chapters, including this one. Chapter two introduces parametric control measurement (PCM) techniques and discusses experimental PCM results. Later sections of chapter two review the properties of SiO_2 that are important to transistor function. The last couple of sections of chapter 2 show results and discuss inherent problems presented by oxide structures in SOI transistors.

Chapter three opens with an introduction to the function of the p-n junction and reverse breakdown of this junction in the drain region. Other sections deal primarily with VBR walk-out. Walk-out was found in both pixel-P (PMOS) and -HV (high voltage NMOS) that form the pixels' control circuitry. Results of experiments are compared to Silvaco-based process/electrical simulations which attempt to resolve VBR walk-out.

Chapter 2
Parametric control measurements (PCM).

2.1 Parametric test structures.

Test devices processed on SOI wafers were probed and tested for electrical behavior related to processing accuracy and reliability. The names for these devices reflect LxW dimensions and/or unique process applications. Tables 1 through 3 list many device names for the purpose of PCM comparison. The focus of this thesis was centered primarily on the high voltage Pixel-HV and the PMOS Pixel-P.

2.1.1 Results.

Test structures on SIMOX wafers were measured at Oregon Graduate Institute and compared to values provided by the foundry, as shown in Table 1. As indicated the reverse breakdown voltages (VBR) were measured after 5 repeated V_d sweeps. This was necessary because there were progressive shifts in VBR after the first sweep which appeared to stabilize by the 5th measurement. For low voltage NMOS and PMOS transistors the increased breakdown voltage increases with progressive sweeps.

The choice of a common (current) point of V_t characterization was based on extrapolation from the linear portion of the I_D-V_g curves. Threshold voltage (V_t) and transconductance plotted together show a linear curve of I_D vs V_g with tangent extrapolation to the x-axis, and subthreshold swing with maximum point Gmmax ($d(\log(I_d))/dV_g$) establishing a tangent point for linear extrapolation (see Figures 2 and 3).

The change in subthreshold current as V_g approaches V_t from the subthreshold region (dI_D/dV_g) is the transconductance (Gm=μ^*C_{ox}(W/L)$^*V_d$, V_d=0.1V) and measures channel conductance prior to inversion. The subthreshold slope is often expressed as the subthreshold swing S=$d(\log I_d)/dV_g$

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and indicates how fast the device can be turned on as well as the number of interface gate oxide traps (19). By comparing the same test device (same (W/L)), at the same point in the I-V curve, at different loci it was possible to examine processing consistency related to mobility (μ) and oxide capacitance (C_{ox}) which are functions of channel doping/size and oxide thickness, respectively.

Table 1: Transistor values represent V_t and VBR, respectively. All other values were obtained from resistive structures.

Device	Foundry	OGI
Pixel P	-2.2V, 8V	-1.6V, -19V
Pixel HV	1.5V, 80V	1.7V, 67V
NMOS 5x10	1.05V, 6V	1.42, 5V
PMOS 3x10	-1.15V, -13V	-1.36V,-12V

2.1.2 Discussion.

The goal of this study was to establish dependable PCM acceptance criteria for future reference. This study has cataloged the electrical behavior of many of the transistors processed on SOI wafers, four of those relevant to this study are shown in Table 1. Data from the low voltage NMOS transistors suggested that 1 out of 5 devices fabricated would have lower resistance and would not perform as the others.

2.2 Fast states introduced into oxide by electron beam.

Deposition by electron beam evaporation (e-beam) resulted in a general lowering of V_t for both low and high voltage NMOS devices. High voltage NMOS devices and PMOS devices showed less change in V_t after E-beam

processing. Increased I_D values measured at $V_d=5V$ (I_{sat}) can be explained by the relationship $I_D=\mu^*C_{ox}^*W/L^*V_d^*[(V_gs-V_t)-V_d/2]$ (19). Lower V_t values result in higher current for a given gate voltage. Reverse breakdown voltage (VBR) for all high voltage devices dramatically increased ($\geq99V$) after E-beam processing.
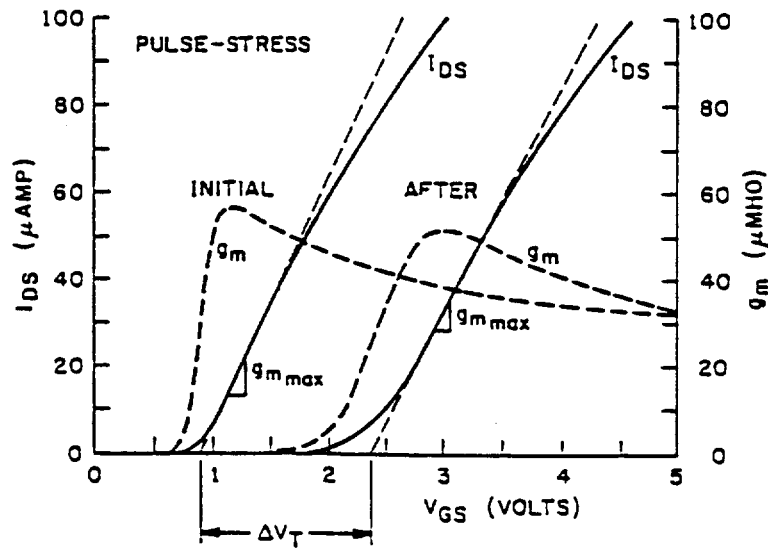
Figure 3: Sensitivity of threshold voltage and transconductance to stress. Threshold voltage (V_t): a linear curve of I_D vs V_gs with tangent extrapolation to the x-axis, and transconductance (Gm, dotted line) show subthreshold swing with maximum point Gmmax ($d(\log(I_d))/dV_g$) establishing a tangent point for linear extrapolation (Adapted from Sabnis (1990)).
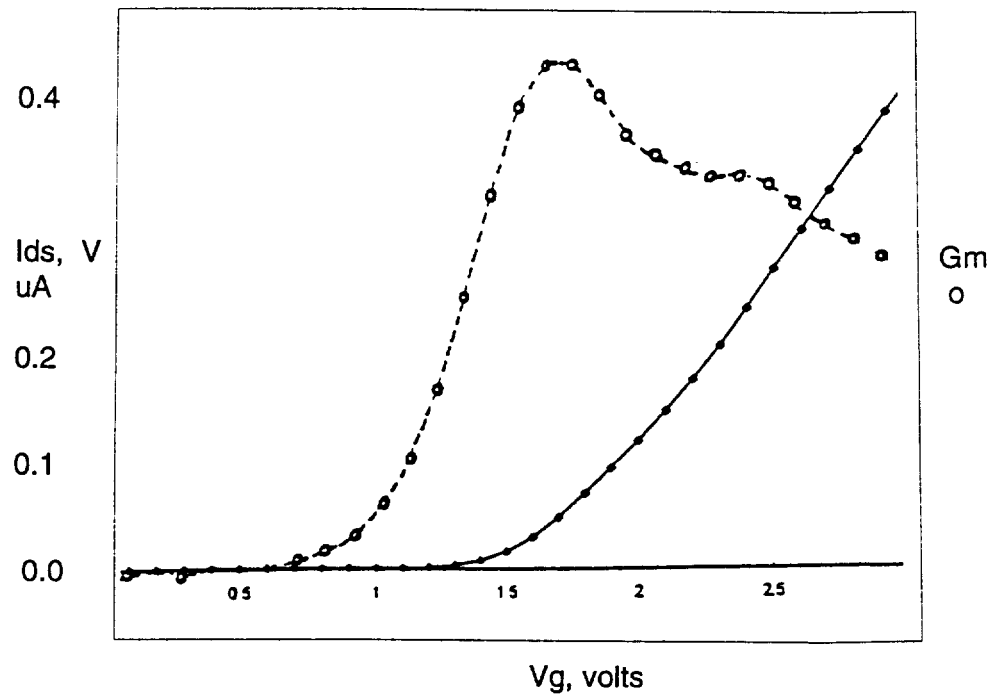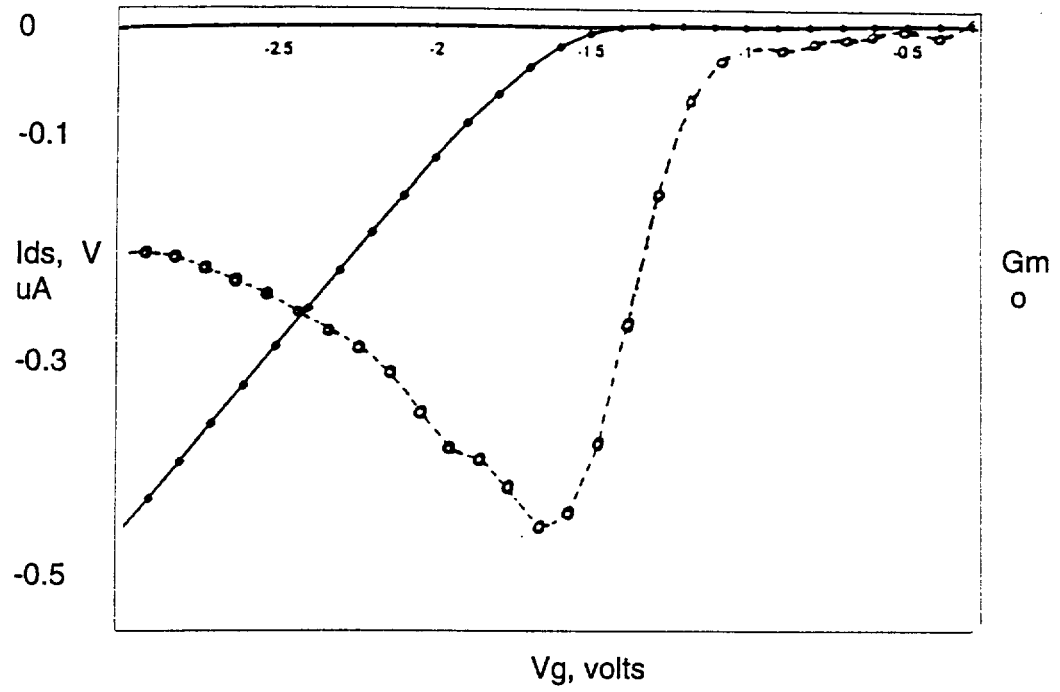
Figure 4: Typical threshold curves. Threshold curves for Pixel-P (top) and Pixel-HV (bottom). See legend of figure 2 for details.

2.2.1 Results.

Table 3 contains the measured values (I_{sat}, V_t & VBR) measured after e-beam deposition processing and again after anneal (-a). Drive current (I_{sat}) values for all devices were comparatively higher after e-beam processing and somewhat lower after the annealing. V_t measurements were consistent with I_{sat} values. Annealing lowered I_{sat} values which alone suggested that V_t had increased. e-beam treatments decreased VBR of low voltage devices but increased VBR of high voltage transistors. Anneal greatly reduced VBR of high voltage (Pixel-HV) devices (see Table 3). VBR shift disappeared after e-beam treatment. After anneals (400 °, 2 hrs) the shift returned to the original values for PMOS devices and the Pixel-HV devices.

2.2.2 Discussion.

E-beam treatments introduced a change in the transistor's electrical behavior. The change was increased threshold voltages and was predominantly irreversible. Conclusion: this form of deposition should not be adopted for any further processing.

Table 2: Saturation current and threshold voltage after E beam treatment. Saturation current (Is) measurements at 5V (=value of both Vds and Vgs) and corresponding threshold voltages (Vt) for e-beam treated (e) and e-beam then followed by anneal treated (a) wafers.

Device	Is-e, μA	Is-a, μA	Vt-e, V	Vt-a, V
nmos2.10	2800	2210	0.7	0.6
nmos3.10	639	560	0.8	0.8
nmos5.10	483	387	0.9	0.6
nmos20.20	202	237	1.1	0.9
Pixel P	-20	-24	-1.7	-1.3
pmos3.10	-297	-401	-1.5	-1.1
pmos5.10	-165	-166	-1.6	-1.0
pmos20.20	-74	-67	-1.4	-1.0
pmos2x10	-2321	-1643	-1.3	-1.0
PAA2S3D25	193	223	1.6	1.5
PAA3S3D10	221	132	1.7	1.5
PAA3S3D25	200	188	1.8	1.5
Pixel HV	35	30	1.0	1.2
Pixel HV2	38	23	0.7	0.9

Table 3: Shifts in reverse breakdown voltage (VBR) after repeated Vds-sweep.

Device	VBR-e, V	ΔV	VBR-a, V	ΔV
n.edgeless	5.2	0.00	5	0.00
nmos3.10	6	0.00	5.9	0.00
nmos5.10	7.4	0.00	7.9	0.00
nmos20.20	14.7	0.00	13	0.00
Pixel P	-14	0.00	-12	open
pmos3.10	-12	0.00	-18	-6.5V
pmos5.10	-13	0.00	-21	-2.9V
pmos20.20	-15	0.00	-19	-5.7V
p.edgeless	-8.5	0.00	-19	open
PAA2S3D25	99	1V	96	2V
PAA3S3D10	99	2V	97	2V
PAA3S3D25	99	1V	98	1V
Pixel HV	100+	limit	30	5V
Pixel HV2	33	0.00	37	6V

open=represent damaged contacts identified visually. Limit of measurement was 100V.

2.3 Oxide properties.

The surface of silicon is covered at all times with a layer of native SiO_2. Thicker layers of SiO_2 are commonly used in isolating active areas of silicon, controlling leakage current of junction devices. Thin layers are used to form gate oxide for field effect devices (20). Experiments with oxidation have shown that oxides which are grown rapidly at high temperatures have a higher defect density than those grown slowly at reduced temperatures ($\approx 900°C$). For these reasons gate oxides are typically grown by 2 step process, initially at low temperature in the presence of HCL (3%) followed by higher temperature (20).

Oxidation of silicon involves a large change in volume, expanding out from the surface of the silicon. Compressive stress has been observed when oxide growth is carried out near temperatures (950°C) at which viscous flow occurs. Further compressive stress results during cool down that is caused by thermal coefficient of expansion mismatch between SiO_2 and silicon. Interfacial compressive stress approaches $4 \times 10^9 dyn/cm^2$ and is sufficient to produce dislocations (21). This stress can cause the underlying silicon to bow out and tends to concentrate near the perimeter (21). Incomplete oxidation at the silicon-SiO_2 interface results in excess silicon interstistials that cause fault formations by nucleating at strain centers. These centers are primarily associated with oxygen precipitates in the silicon and induce stacking faults (21).

Charge states in SiO_2 are associated with the nature of the oxide growth process and with the interaction between the oxide and the silicon surface (20). An important property of thermally grown SiO_2 is its ability to reduce the surface states density of silicon by tying up dangling bonds (21). The silicon surface represents a major discontinuity in the crystal lattice in the form of dangling bonds ($1 \times 10^{15}/cm^2$). The oxide layer reduces these surface states to $10^{11}/cm^2$, which then remain as interface trap sites (fast surface states) and are located in the first 25Å of the silicon surface. The density of these traps ($Nit \approx 1 \times 10^{10}/cm^2$)

is a function of both the process conditions and crystal orientation (19). Traps deep within the silicon bandgap contribute to generation and recombination of carriers at the surface and contribute to leakage current and shorter minority carrier lifetimes (19).

Slow surface states from trapped positive charges (Li^+, K^+ or Na^+) establish a surface potential by pinning the Fermi level to the surface trap level (19). The role of slow surface states is minor in heavily doped silicon, but becomes significant with lighter doped material such as the n-drift region of the DMOS transistor (22). These alkali metals are usually mobile when the SiO_2 is heated and biased. Long term reliability is dramatically affected by the presence of slow surface states and great efforts are made to reduce these.

2.3.1 Oxide characterizations.

The SiO_2-silicon interface region differs radically from the bulk SiO_2 film because of stress and interfacial impurity segregation. Within the interface region, two distinct classes of silicon defects are involved in the transfer of electrons to and from the silicon substrate via thermionic or tunneling processes (23). Within the bulk, neutral defects related to water impurities can capture electrons from the SiO_2 conduction band. These are classified below (according to Feigl (1987)) .

Qotb, bulk oxide trapped charge, distributed within the oxide film, excluding the first 3nm adjacent to the SiO_2-silicon interface. Qotb is negatively charged and is due to either trapped electrons at oxide defects or impurities in the network.

Qoti, oxide trapped charges within the first 3 nm of the SiO_2-silicon interface. This charge is generally positive and is due to trapped holes at defects or impurities.

Qit, interface trap charge, localized at the SiO_2-silicon interface. The density of Qit (Dit) within the gap can be determined experimentally. These traps quickly equilibrate with carriers in the silicon bands and are referred to as

fast surface states.

Hydrogen impurities in SiO_2 occur in large concentrations, the total hydrogen concentration is represented by SiH, SiOH and loosely bound H_2O (23). Within the bulk of the oxide, the H concentration is typically less than 1% of the silicon concentration in SiO_2. Higher concentrations are often observed in the first 5nm of the SiO_2-silicon interface and can approach 5% of the concentration of silicon in SiO_2. Studies by Fiegl showed that the total concentration of H impurity and physical defects (step ledges and strained bonds) were on the order of $1 \times 10^{14}/cm^2$, while Qoti seldom exceeded $1 \times 10^{13}/cm^2$ (23). A simple interpretation was that hydrogen impurities are incorporated at strained bonds within the oxide network, forming SiOH defects in the bulk of the oxide film and SiH defects near the silicon interface (23). The SiOH defects have been associated with Qotb, but there is no supporting evidence to show that H impurities or strained bonds are associated with hole traps related to Qoti.

A mechanism proposed for positive bias stress is tunneling of electrons from the interface traps into the near-interface defects responsible for Qoti (24). This requires defect energy levels within the SiO_2 which are energetically within or close to the silicon bandgap. The reverse tunneling process presumably occurs under negative bias stress.

Positive Qoti produced by direct injection of holes can be neutralized by electron tunneling from the silicon valence band into near-interface traps responsible for Qoti. Once neutralized, the trapped hole charge cannot be regenerated by negative bias stressing, and gate bias variations only affect the time required to neutralization by altering the tunneling barrier for electrons (24).

18

Gate

Qotb

− − − − − −
− − − − − −

Qoti

+ + + + + + + + + + + +

Qit   Oxide

− − − − − − − − − − − − −

Silicon
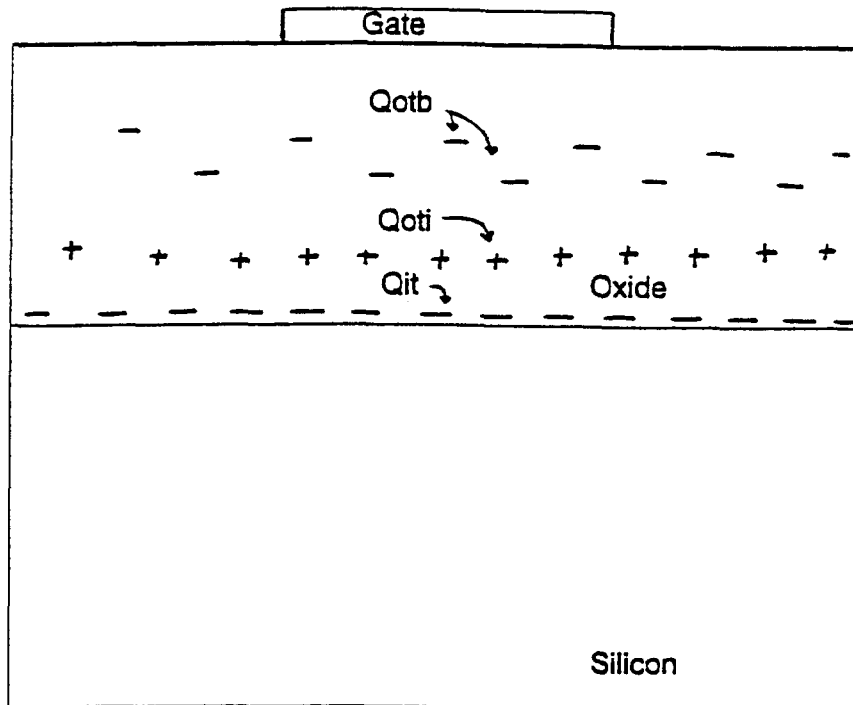
Figure 5: Schematic representation of oxide charges (adapted from Manzini and Modelli (1983), see text for details).

Feigl (23) has proposed a band-to-trap tunneling model that shows significant hysteresis (see Figure 6). In this model (23), oxide traps (ET), filled at zero-bias have an energy level below the silicon valence band edge. Decreasing applied bias raises the oxide band relative to silicon's valence band and electrons tunnel into silicon. Once depleted of electrons, the energy level of the oxide traps relaxes to a slightly higher energy level (Er). A greater positive bias is then required to refill the elevated trap energy levels. As positive bias bends the oxide band downward more electrons tunnel from silicon valence band to oxide traps and reposit into the traps and re-establish ET.
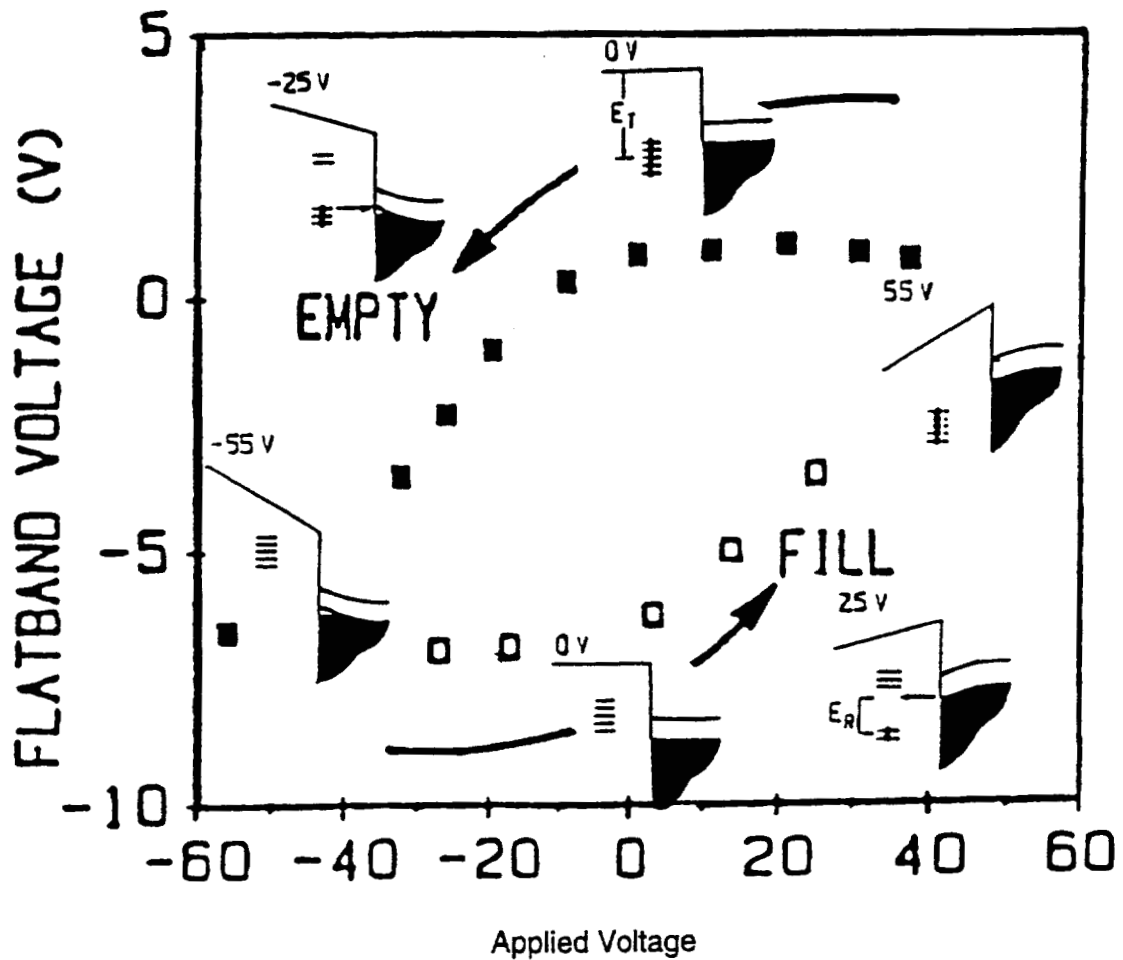
Figure 6: Band to band tunneling (according to Feigl (1987)) of electrons between silicon valence bands and oxide band-gap states (defect traps) located near the interface. Schematic inserts distributed along the FILL and EMPTY curves correspond to the applied voltages (x-axis) and illustrate the concept of band to band tunneling.

This model only describes the energy levels of the defects responsible for Qoti. The near-interface defect energy level must be energetically degenerate with the silicon valence band and displaced in energy from the silicon bandgap (23). This model does not address the atomic structure of these defects. Several investigators have shown that bias-stress induced Qoti defects correlate to oxygen vacancies in SiO_2 (25). Qotb and electron trapping defects are located outside of the region near the interface. Different defects dominate the bulk charge trapping behavior of wet oxide and annealed oxide films. In contrast, ultradry oxide films are essentially free of bulk traps.

Oxides can become contaminated during processing and handling. Sodium ions are the chief contaminant. Special precautions are taken to prevent sodium contamination and to getter it away from active areas containing devices. The effects of ionic contamination include dipole and mobile ion charges in the oxide. These introduce instability in C-V and I-V characteristics (26).

2.3.2 C-V measurements.

Important issues for C-V measurements are related to the geometric dimensions of the gate capacitor and series resistance represented by the underlying silicon and backside contact. The oxide is very thin compared to the substrate. Thus, the point of contact (electrode) will produce a spreading resistance within the bulk. The area from which the spreading originates will be proportional to the area of the electrode (27). In SOI there is a continuous BOX approximately 0.1µm beneath the gate oxide that restricts this spreading and represents a series capacitance. However, this is less of a concern with non-fully depleted SOI devices. Although C-V measurements were not made on these SOI wafers, these types of measurements would provide the information needed to determine whether wafer contaminations at the foundry was responsible for low yields and early failures of the AMEL displays.

2.3.3 Field oxides.

The purpose of field oxides (FOX) is to electrically isolate active regions of the silicon (24). A FOX, based on LOCOS (local isolation of silicon) technique, was used to shield the n-drift region and extend the gate and the depletion layer into the drift region (see figure 7). However, special precautions must be taken to avoid water vapor which can migrate beneath the nitride pad designed to prevent oxidation in the LOCOS process. Water can liberate free ammonia from nitride which diffuses to the interface between the stress-relieving oxide and the silicon. Oxynitride, which appears as a white ribbon, forms at this interface and is resistant to the buffered HF wet etch used to remove the stress-relieving SiO_2 (28). The thin layer of oxynitride which forms prevents subsequent gate-oxide formation (26). Devices with white ribbons formations do not meet the goals of the original device design and therefore reduce device yield.

One solution to this problem is to eliminate all forms of interfacial oxide between the nitride and silicon and thereby remove the conduit for waters diffusion. The process is called SILOS (Sealed Interface Local Oxidation of Silicon) and also helps to eliminate the birds beak encroachment under the passivating nitride layer (26). Another potential solution is to turn the problem into a utility, especially if moisture is difficult to control. Oxynitride films can be used as gate oxide, and are excellent barriers to diffusion of light alkali ions (N^+, K^+,) (29). Nitrogen reduces the concentration of strained Si-O bonds and suppresses generation of interface states in the insulator during electrical stress. This reduces hot electron effects and also reduces pinhole defects in the oxide (29). If gate oxides were of the appropriate thickness of thermally grown oxynitride (150Å, silicon oxidation in the presences of N_2O at 1150°C, 2.5 min RTA) then LOCOS process could be preformed without too much concern for white ribbon artifacts or changes in the shape of silicon-SiO_2 interface (27).
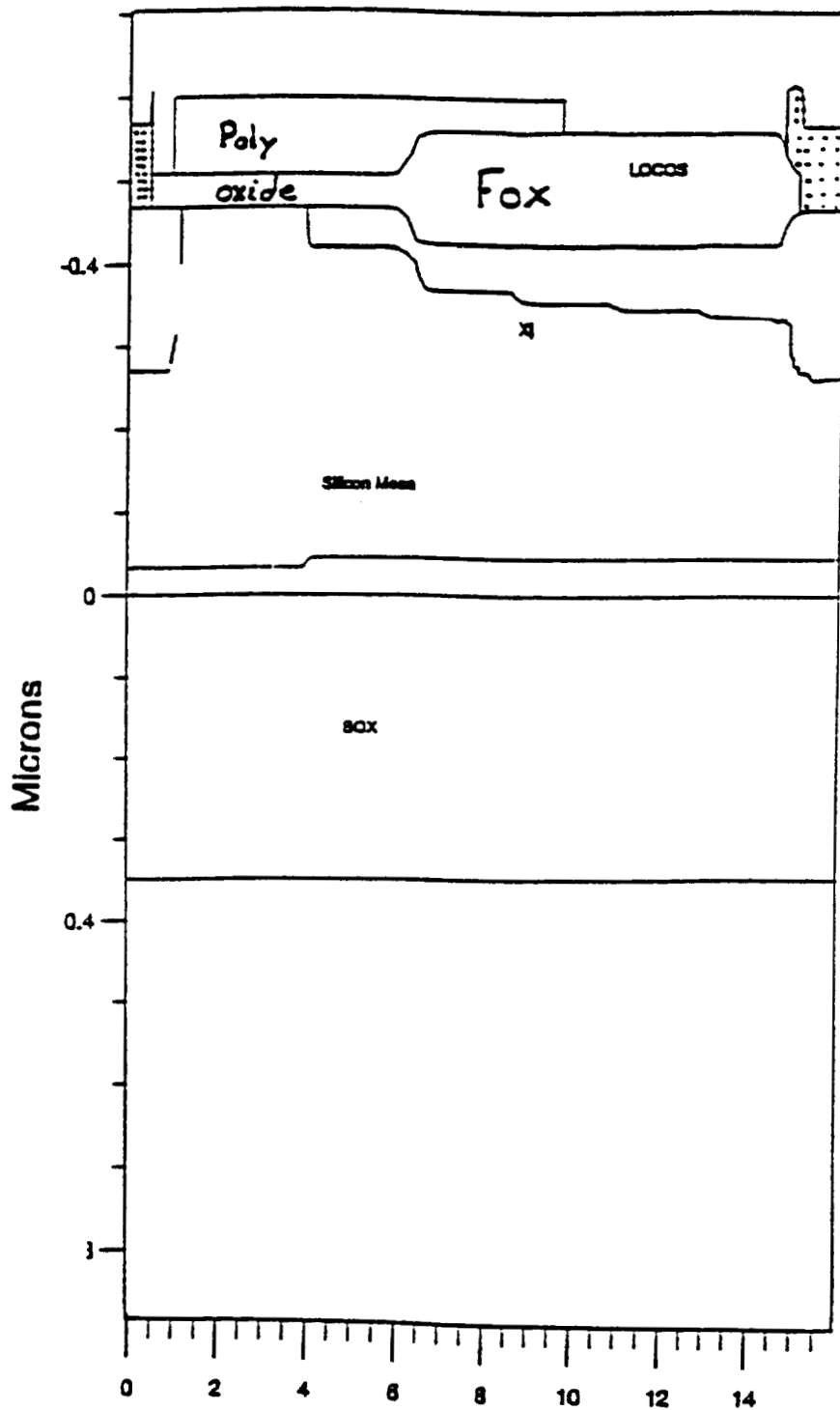
Figure 7: DMOS structures with field oxide shields designed using grown LOCOS oxide. Junction depths (Xj) and gradations of phosphorous for source, drain and n-drift regions are also shown.

2.4 SOI mesa formations.

The mesa technique is an effective way of isolating silicon islands from one another (30,31). It is simple and consists of patterning silicon into sloped islands (or mesas) using a mask step and an etch step (see Figure 1). However, the gate oxide grows both on the top and the edges of the mesas. Gate oxide on the side walls of the silicon mesa act as parasitic edge devices/channels unless special precautions to isolate the side gates are taken. Another problem is non-uniform SiO_2 thickness at the corners of the mesa-BOX intersection (see figure 8) which are typically 30 to 50% thinner than the gate oxide owing to compounded compressive stresses and restricted silicon available for oxide growth (32,33). The thinning is temperature dependent, and is more pronounced if oxidation is preformed below or near the SiO_2 viscous flow temperature at about 965°C (32). Side wall oxidation also sharpens silicon corners reducing both the breakdown voltage of the gate and the threshold voltage (V_t) at the corners of the islands (33).

2.4.1 The edge effect.

Side-gate oxide and undercut related thinning of the gate oxide near the mesa BOX junction can cause low voltage parasitic side channel activity. Lower V_t values result from its inverse relationship with C_{ox}. Two test devices were designed especially for the purpose of addressing this "edge effect". The devices LWL.N.5.1000 and Mel N 1000.5 represent arrays of NMOS devices linked in parallel or in series to simulate either 200 or 2 edges, respectively. Each has the same length (L) and effective width (W), (5Lx1000W) verses [100x(5Lx10W)]. Individual device measurements and their averages are shown in Table 4 for threshold (V_t), transconductance ($Gmmax = \mu^* C_{ox}(W/L)$), and the breakdown voltage of the gate oxide (BVox).

Poly line

Gate Oxide

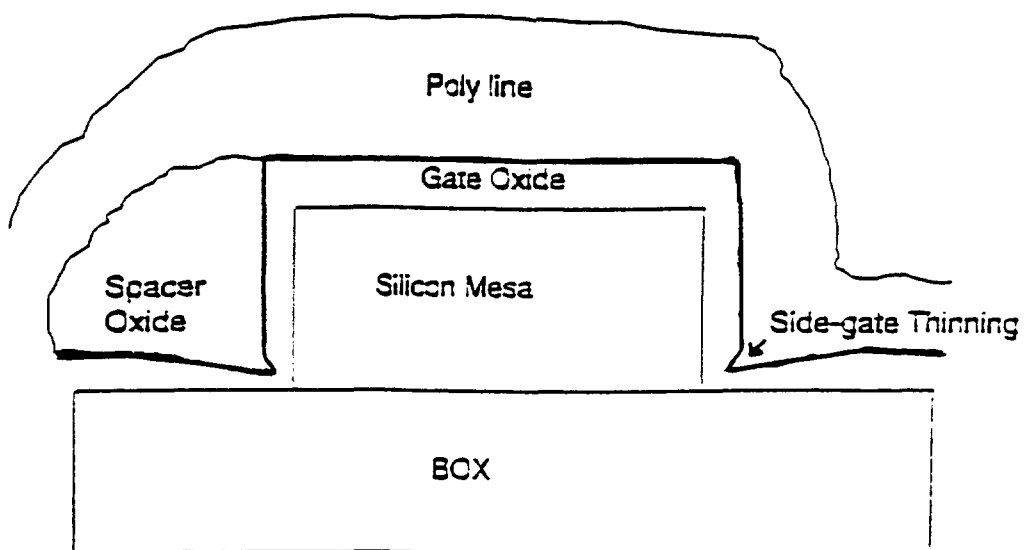Spacer
Oxide

Silicon Mesa

Side-gate Thinning

BOX

Figure 8: Side-view schematic of silicon mesa on buried oxide (BOX). Gate oxide grown on the mesa encompass both the top and sides. **Right half:** Side-gate thinning without spacer oxide; **Left Side:** spacer oxide used to fill in thinned side-gates.

2.4.2 Results.

The NMOS 5x1000 has only 2 edges, compared to the NMOS 100.5x10 which has 200 edges, and has a V_t that was 79mV higher (see Table 4). Maximal transconductance (Gmmax) measurements were higher in the single wide test structure (5x1000) demonstrating a lower channel resistance compared to the 100 thinner devices test structure (100.5x10). Reduced C_{ox} thickness due to mesa undercutting could have also contributed to this difference. However, BVox values between the two test structures was only slightly lower in the 100.5x10 devices reflecting the increased probability of encountering greater gate thinning near the side gate oxide-BOX junction when comparing a greater number of side gates. Figure 9 shows a typical threshold curves for these two test structures. A single V_t value can be extracted from the smooth curve representing the NMOS 5x1000 device. A biphasic I_D-V_g curve can be seen from the NMOS 100.5x10 device indicating that there are two threshold voltages, early turn on by side gates, separated by a subthreshold kink from the higher V_t of the top gate.

2.4.3 Discussion.

Silicon mesa side gate oxides contribute to lower threshold voltages and are sites of increased resistance (=lower Gm). Application of voltages near the subthreshold kink region can contribute to device leakage currents. Defects at the side-gate mesa-BOX junction may contribute to a slightly lower oxide breakdown voltage.

2.5 Spacer Oxide.

Chemical vapor deposition (CVD) of SiO_2 is frequently used to deposit oxide over areas needing isolation (35). CVD spacers oxides were expected to reduce the effects of gate constriction near the base of the mesa-BOX junction (see left side of figure 8). However, the spacer oxides did not correct the problem. Instead the deposited oxide spacer replaced problems caused by thin

oxides at the side-gate-BOX interface with problems related to oxide charge accumulations.

Table 4: Individual and average device parameters are compared to determine the influence of silicon mesa edges. Four sites were randomly chosen for the 5x1000 NMOS test structure and were compared to 3 sites containing the 100* 5x10 test structure. Threshold voltages are measured in millivolts, Gmmax are expressed in $(C/V^{2*}sec)x10^9$, BVox in volts.

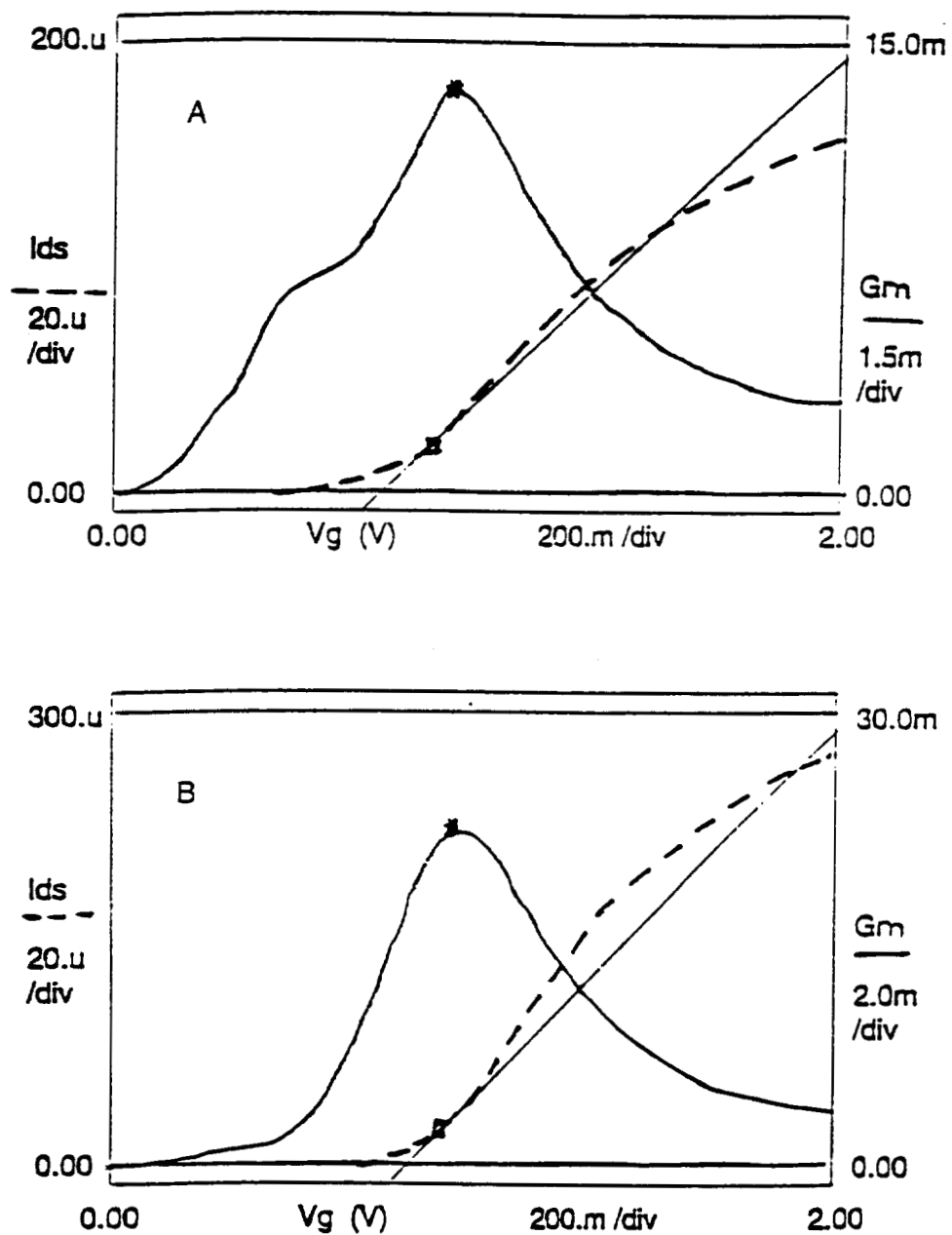| Number of	V_t, mV	Gmmax	BVox
2 gates #1	780	54.5	12.0
2 gates #2	778	53.1	11.5
2 gates #3	779	52.4	11.2
2 gates #4	779	49.6	12.2
Average of 2	**779**	**52.5**	**11.9**
200 gates #1	697	20.0	10.0
200 gates #2	696	21.1	10.5
200 gates #3	705	19.4	10.8
Average of 200	**700**	**20.0**	**10.5**

27

Figure 9: Threshold voltage determinations by extrapolation at maximal transconductance (Gm) points are plotted for (A) NMOS 5x1000 and (B) NMOS 100.5x10 test structures.

2.5.1 Spacer oxide charging and discharging.

Subthreshold currents measured from NMOS transistors (used in the peripheral select-scanner circuitry) demonstrated biphasic transconductance curves as a function of V_g under low V_d (0.1V, see figure 9). The change in the curve was represented as a "kink" in the current and indicates that one threshold voltage (V_t) has been succeeded by another, i.e., 2 V_t values. The first V_t (lower) is believed to be the result of side-gate oxide functioning as a gate capacitor for side channel formation within the silicon island.

2.5.2 Results.

2.5.2.1 Threshold voltage (V_t).

Measurements were made in the dark and V_t curves were generated by sweeping the gate voltage from 0 to -3V and collecting $\log(I_d)$. The first baseline V_t measurement showed 2 potential V_t subsections, the lower maxima representing the side channel V_t. Heat treatment (400°C for 2 hrs) caused a parallel shift to the right resulting in higher V_t values (figure 10). The first attempts to stress the spacer oxide were through reverse breakdown voltage (VBR) sweeping the drain voltage ($V_g=0$; $V_d=0{\rightarrow}16V$; I_D compliance set to 2μA) for 2 hours (filled diamonds, figure 11). This caused a slight parallel shift to the left by the entire curve, i.e., it was not selective for the lower or upper portions of the curve. This shift was easily restored after 2 hours of heat treatment (anneal) at 400°C.

A second approach was to stress the spacer oxide involved ramping V_d ($0{\rightarrow}10V$) while holding $V_g=1.85V$, 0.02V below the previously measured baseline V_t value (V_t-stress (X), figure 10). Such treatment selectively shifted the lower V_t section to the left and caused the upper V_t curve to flatten slightly. This shift was also completely reversed after 2 hours of anneal (400°C). Normal operation ($V_d=0{\rightarrow}5$, $V_g=5V$) overnight did not charge side gate oxide. Spacer oxide stress-charging was selective for the side channel oxide as compared to light induced carrier formations induced by intense light.
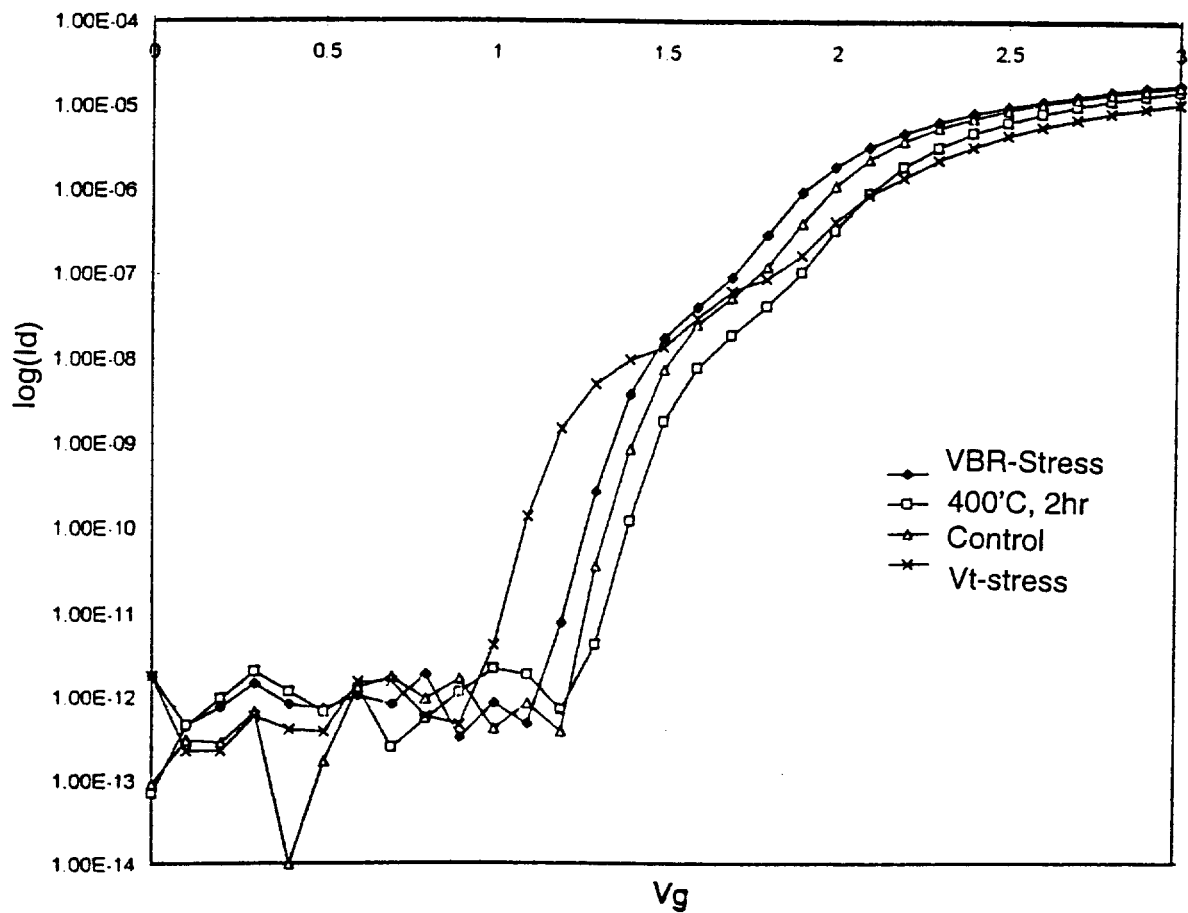
Figure 10: Threshold measurements before and after stress affects and before and after heat anneal (see legend and text for details related to stress conditions). For each measurement, drain voltage was held constant at 0.1V and the gate voltage was increased as indicated.
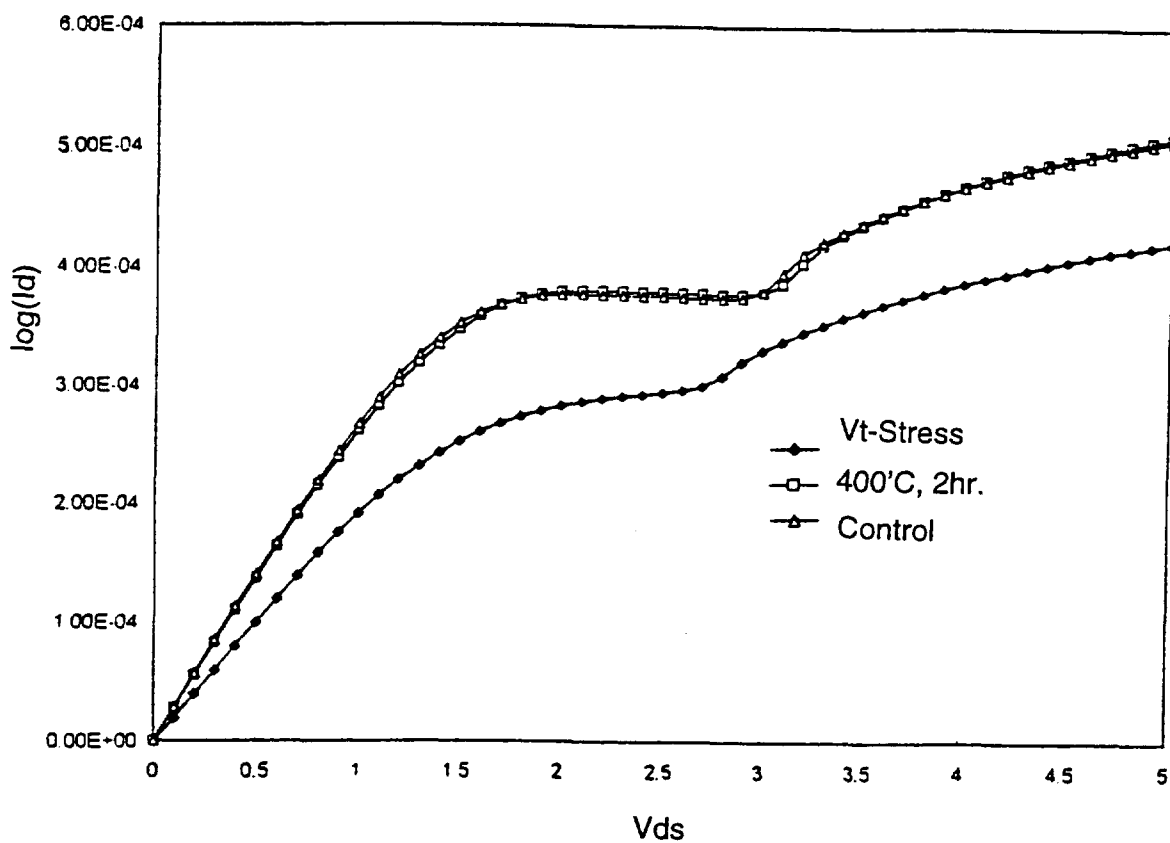
Figure 11: Saturation currents (I_{sat}) associated with the indicated stress treatments (see legend and text for details related to stress). In each case, the drain voltage was increased as shown and the gate voltage held constant at 5V.

2.5.2.2 Saturation current (I_{sat}).

The result of a lower V_t value was expected to translated into greater differences in I_{sat} according to $I_{sat}=\mu^*C_{ox}/2^*(W/L)(V_g-V_t)^2$. However, side-oxide stress-induced lower V_t shifts correlated to depressed I_{sat} (drive). In addition, the significant "Kink" near 3V was closer to 2.75V (see V_t-stress, closed diamonds, figure 11). Stress effects on I_{sat} were annealed by heating for 2 hours at 400°C.

2.5.3 Discussion.

First indications were that the left shift in the V_t-stress curve (i.e., left-shifted bottom portion of the subthreshold curve) would translate to an early transistor turn-on with greater drive current (I_{sat}). However, the saturation data was consistent with a functionally higher V_t, as evidence by a lower I_{sat} measurement. The data indicate that fast states were trapping hot carriers and in doing so facilitated side-channel inversion associated with the lower V_t curve. When the side-oxide becomes highly charged the impact ionizations near the drain were enhanced (early Vkink). The lower portion of the threshold curve shown in figure 11 showed a definite slope change. The upper portion of the V_t curve flattened significantly and is directly responsible for the reduce drive current after Vt-stress (see figures 3 and 12). Charging of the side-oxide increased both the transistors' main V_t as well as subthreshold leakage current.

2.6 Hot carrier effects.

Carriers can enter the oxide by tunneling at the silicon/SiO_2 interface. For direct tunneling, the oxide has to be very thin (<100A). Under high fields carriers can attain sufficient energies (="hot") and can inject into the oxide (26). The barrier height to injection is approximately 3eV for electrons and closerer to 4eV for holes. During saturation mode operation ($V_g<V_d$) of transistors the high electric field that develops near the drain facilitates the injection of holes into the oxide (26). The damage to the silicon-SiO_2 interface depends on 3 factors:

generation of carriers, hot carrier injection, and trapping of hot carriers (36). Characterization of damage is by V_t curve shifts (ΔV_t) and by single-point maxima change (ΔGmmax; see figure 3). A change in slope gradient (subthreshold swing) suggests the possibility of hole injection.

Two patterns of stress-induced aging are: (1) decreased slope (transconductance change) while operating in the reverse mode (using source as the drain) indicates the presence of interface states near the drain end, (2) a left shift in the V_t while operating in normal mode (source to drain) represents a channel shortening effect due to the accumulation of positive charges near the oxide-Silicon interface (21). Trapped holes are believed to capture electrons (or negative ions) and are termed fast states. The slope of a ΔV_g vs log(I_d) curve defines the density of interface states Dit=$(C_{ox}/q)^*(d\Delta V_g/d\phi_s$; see figure 3). Dit cause Gm to degrade because they must be filled before a channel can turn on (see figure 6), thus increases in in V_t for NMOS transistors is observed (26).

MOSFET hot carrier aging, accelerated voltage stress causing drift in V_t and Gm, is the main criteria for circuit failure analysis. When identified, trapped holes, neutralized by electrons or negative ions, can be annihilated by annealing out the wafer. High temperatures (>200°C) in the presence of hydrogen accelerate the annealing process. One approach towards preventing (reducing) hot carrier effects is by careful attention to gate oxide growth such as the use of halogenic oxidation or by using ultra thin oxynitride. Another approach is to reduce the electric field near the drain by fabricating a graded lightly doped (LDD) n-drift drain region (see figure 7).

2.7 Breakdown.

Silicon oxide usually breaks down and begins to leak current when the electric field across the exceeds 10MV/cm (21). A difficulty in defining oxide breakdown is that thinner oxides can pass larger currents (Fowler-Nordheim tunneling where current is proportional to the field squared) without breaking down. Breakdown most often occurs in regions of defect or impurity

accumulation and increases with defect density. However, the complexity of defect dominated breakdown mechanism is related to defects that are randomly distributed and each defect has its own threshold of failure (37). Intrinsic oxide breakdown is believed to occur by impact ionization. Defects are sites of current leakage which increase with time, temperature, and electric field. Self-healing has been observed after some forms of breakdown but cannot be explained (26).

Breakdown can be measured by applying voltage across an oxide while measuring leakage current, BVox is recorded when leakage current reaches 1μA. Another approach is to calculate the charge at breakdown (Q_{bv}). In this case a fixed current is forced through the oxide and the voltage is measured (26). Time to BVox (t_{bv}) is where the voltage across the oxide suddenly decreases. The charge at that time is calculated by $Q_{bv}=I^*t_{bv}$.

The mechanism of oxide breakdown is thought to be due to positive charge buildup near the injecting (cathode) interface (21). For oxides thicker than 12nm, the source of the positive charge is believed to be impact ionizations deep within the oxide. Positive charges associated with the tunneling current drift back towards the cathode and get trapped near the interface. These trapped positive charges lower the energy band and facilitate further electron injection, and a runaway process (21). Higher currents result in I^2R heating sufficient to melt SiO_2. However, high leakage current causes circuit malfunction prior to catastrophic breakdown (21,34,37).

A similar mechanism has been suggested for thinner oxides (<10nm). However, the source of positive charges is hot holes created at the anode side (23,25). The hot holes are thought to be the product of electron tunneling, and transfer of kinetic energy to valence band electrons. Hot holes are then injected back into the oxide by the electric field and once trapped near the oxide-cathode interface, again leading to thermal runaway (39).

Three distinct types (A, B, & C) of oxide failure have been characterized from voltage ramp test (21). Each type respectively corresponds to an

increasing electric field strength (<2, 2-8, & >8; MV/cm) required to show BVox. There are ongoing studies to establish a correlation between the type of defect (defect signature) mediating the BVox (21,40). Type A is where BVox<2MV/cm and is the sign of a major defect that are usually tested out during burn in. Type B represents a range of BVox between gross oxide defects and good oxide, leakage occurs early and will pose a long-term reliability problem. Type C (>8MV/cm) are considered to be intrinsically good oxides (21,34).

2.8 Hold node oxides.

Interlayer dielectric (ILD) plays an important role in separating multilevel interconnects. These are deposited oxides usually 1µm thick (34). Deposition of ILD must be economical; produce films low in pinhole, particle density, and tensile stress, and finally have low permitivity to reduce capacitive coupling (38). In AMEL application, ILD-oxides also served as hold capacitors (see figure 2). If leaky, data "hold" function by ILD can be severely compromised. Leaky hold capacitors may yield "0s" rather than "1s" during select scanning.

2.8.1 Results.

BVox values for intermetal (P, see table 5)) capacitor test structures in the test scribe lines for P1-P2 ILD and P2-P3 ILD demonstrated dielectric strengths of 0.55-1.1 and 3.45-4.15 MV/cm, respectively (see Table 5 below). Capacitance measurements made from different wafers showed lower than expected breakdown values for ILD capacitors. Although BVox values were low the pattern of current rise for P2-P3 ILD was sharp and indicated low defect density. In contrast, a gradual pattern of current increase was observed for P1-P2 BVox. Visual inspection of P1-P2 capacitor structures during BVox testing revealed that the P1-P2 oxide itself was not breaking down and instead allowed current to increase and overheat (I^2R) poly line resistance causing destruction of the junction between the probe pad and the line to the capacitor structure.

2.8.2 Discussion.

There are alternative explanations for the lower than expected BVox values. If ILD structures were actually thinner than reported, and the structural integrity was high, then BVox values would approach the ideal 9MV/cm level. Why drain-line contacts burnt-out for P1-P2 ILD capacitive test structures but not for the P2-P3 test structures remains to be determined. SIMOX (versus ISE) wafers showed slightly lower BVox for the P2-P3 test capacitors but were not significantly different. The implication of these results is that ILD capacitor structures (hold node) may be the source of current leakage and can adversely affect storage of data turning select/scanning operation.

Table 5: ILD breakdown (BV) measurements: V_d required to induce current leak and calculated dielectric strength.

Lot/Wafer# : type	BV, P1-P2*	MV/cm*	BV, P2-	MV/cm
14989-1 18, ISE	10	0.5	72	3.6
15114-1 06, Simox	11	0.55	70	3.5
15197-1 16, ISE	22	1.1	81	4.05
15410-1 03, Simox	11	0.55	74	3.7
15410-1 24, ISE	11	0.55	75	3.75

Calculated dielectric strengths = BVox/thickness (MV/cm). The thickness, by design, for both ILDs was 2000Å. *BVox for P1-P2 was the result of $P=I^2R$ polyline (resistor) burnout.

Chapter 3
Reverse drain breakdown, and Walk-out.

3.1 The p-n junction of the drain: reverse breakdown.

The reverse breakdown voltage (VBR) of the barrier to current flow within the p-n junction of the drain/channel depends on the curvature of the p-n junction and the dopant concentrations (19). High fields bend the valence and conduction bands such that electrons are pulled free of their covalent bonds and tunnel through the energy barrier leaving a hole behind. This form of VBR becomes more likely as dopant concentrations increase because the width of the depletion region decreases and the energy bands in the depletion region are bent more steeply.

Tunneling is only significant in highly doped material in which the fields are high and the depletion region is narrow (19). As the dopant concentration decreases the width of the space charge region increases and the probability of tunneling decreases. Avalanche breakdown occurs by field-induced electron acceleration. Low doping profiles favor avalanche breakdown involving impact ionizations because the mean free path of the accelerated electron has sufficient space (length) to gain enough energy ($=3/2Eg$) to break covalent bonds (40). These two mechanisms can be distinguished according to temperature sensitivity. As temperature increases the tunneling breakdown occurs at a lower voltages because of increased electron flux across the energy gap from the valance band of the p-type material to the conduction band of the n-type material. Avalanche breakdown voltage increases with temperature because of temperature-induced lattice scatter reduces impact ionizations (19).

The breakdown voltage of the drain can be increased by engineering the RESURF (REduced SURface Field) diode structure into the design of the high voltages devices (41,42). This principle has been incorporated into high voltage Pixel-HV transistor by engineering a lightly doped drain (LDD) called the n-drift region with partial overlap by the gate electrode (41,42). Low doping is critical

to field spreading. If the doping is too high a narrow depletion zone at the surface causes low voltage breakdown (tunneling breakdown). However, if doping is too low the drift region depletes very fast and the breakdown occurs at the drift region-drain interface, resistance increases and impact ionizations become localized near the p-n-drift interface and resulti in low voltage breakdown (36,41,42). Oxide structures can affect the spread of the impact ionizations along the n-drift region. Both the field and buried oxide layers help to spread the impact ionizations over the length of the n-drift region and improve the reverse breakdown voltage.

3.2 Reverse breakdown voltage in SOI transistors:

There are two important mechanisms of p-n junction breakdown in SOI MOSFET transistors: avalanche breakdown and punch-through (19,40). During punch-through breakdown reverse bias on p-n junction at the drain creates a depletion region which merges with the depletion region developing at the source. However, punch-through breakdown is only observed in short channel devices ($\leq 1 \mu m$). Avalanche breakdown is dependent on the field in the depletion region and thermally generated minority carriers drifting down the potential hill to give rise to breakdown current. The drift velocity is proportional to the field strength. When the drain-source voltage exceeds a critical value, the maxim field at the drain-channel junction can exceed the breakdown field of Silicon ($\mathscr{E}br$) which is between 0.2 and 0.8 MV/cm (19,40).

Once the field exeeds $\mathscr{E}br$ the carriers will be accelerated to velocities capable of causing impact ionizations. For an NMOS transistor, electrons generated in the depletion region will reach high velocities. Impact collisions with the lattice then generate electron-hole pairs, electrons promoted into the conduction band leaving holes in the valence band. Three carriers are now present and are accelerated in the field. This process cascades, holes entering the depletion region edge are multiplied by the avalanche until they approach the p-bulk where the field falls off (40).

If the accelerated ("hot") carriers enter and become trapped in the oxide they will create a space charge which can affect junction behavior. The reverse breakdown voltage changes by an amount that depends on the extent of avalanche and carrier trapping. Typically, devices recover over a period of days, however, the rate of recovery depends on the quality of the surface oxide and especially on its water content. This problem, called junction walkout cannot be eliminated but can be reduced by careful processing. Long, low temperature bake-outs (2-3 days) can help remove extra water (39,43).

3.2.1 Results.

3.2.1.1 Pixel P test structures demonstrate VBR Walk-out.

VBR is a measure of p-n junction doping and is influenced by field oxide and buried oxide insulations. It is easy to measure and can provide information on processing uniformity and device performance. Measurements from different wafer lots undergoing the same process showed 10V differences. PMOS transistors fabricated on SIMOX wafers demonstrated
lower VBR than ISE wafers, however, within each group there was 4 to 5V variation (see Table 6). Each VBR value recorded was obtained after the third consecutive V_d sweep. This walk-out behavior was independent of current compliance limitation. That is, walk-out did not show correlation to magnitudes of current carried by the transistor (see figure 12).

3.2.1.2 Discussion.

VBR is a characteristic of channel-drain p-n diode function. Pixel P (PMOS) shows a definite left shift in VBR values following the first V_d sweep. Final measured VBR values ranged from -13V up to -32V, but were most often between -13 and -18V. I_{sat} values measured at -5V V_d with -5V on the gate were often slightly higher after VBR measurements indicating that extra current could be produced in a Pixel P channel that had been in repeated heavy use.

Self heating may scatter hole-motions in the channel so that higher (more negative) V_d sweeps are required to achieve VBR. An alternative explanation is that repeated V_d sweeps result in the accumulation of electrons near the source and that these then recombine with (scavenge) injected holes thereby requiring higher applied voltage for subsequent VBR.

Table 6: VBR values measured from different Pixel P (PMOS) transistors and SOI wafers.

Lot/Wafer# : type	VBR, final	ΔVBR	Compliance
14989-1 18 ISE	-24.00	5V	-1mA
14989-1 15 ISE	-22.00	7V	-1mA
15114-1 16 Simox	-14.00	4V	-100μA
15410-1 03 ISE	-20.00	4.5V	-10μA
15041-1 24 Simox	-17.00	2.5V	- 10μA

3.3 High voltage transistors exhibit VBR Walk-out.

The HV_PAA-structures were designed with an extension of the n-drift region as a circle around the drain. This n-drift ring was reported to have higher VBR than Pixel HV-transistors not containing ringed drains. This was tested using a SIMOX wafer so that a greater range of walk-out could be observed after repeated V_d sweeping.
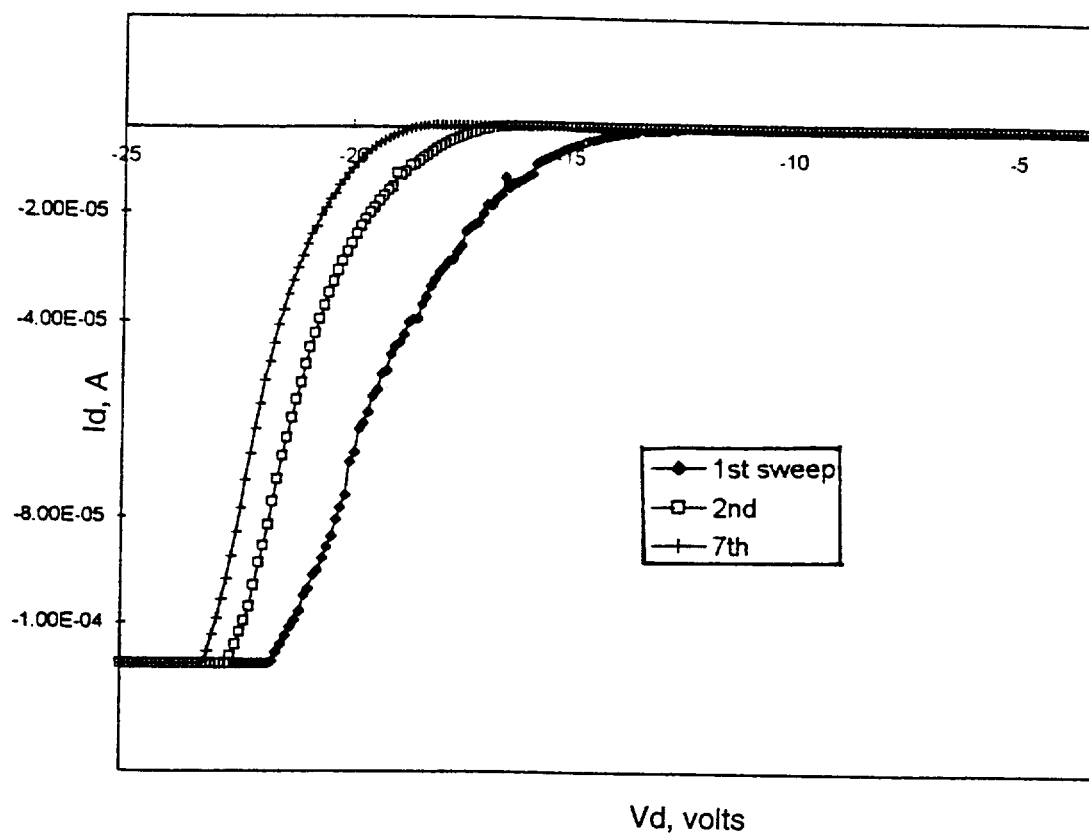
Figure 12: Characteristic Walk-out curve shift for Pixel P (PMOS) transistor fabricated on a SIMOX SOI wafer. Breakdown voltage was taken at the point where currents reached -100nA. Complience was expanded to 0.1mA.

3.3.1 Results.

Compared to Pixel-HV test structures the HV_PAA-structures showed similar family of curves and V_t. However, its initial VBR values were higher: 62 compared to 48V for Pixel-HV. Another difference was that Pixel HV_PAA test structures showed a low current tolerance (compliance near 2uA). Sweeping V_d under 2uA compliance reduced the VBR shift. Pixel-HV structures withstood 50uA or more current without gate oxide/polyline burnout. The one common characteristic shared by the two transistor variants was VBR walk-out.

Pixel-HV (DMOS) transistors showed current-dependent VBR walk-out (Figure 13). Voltage between the source and drain was swept using stepped increments of compliance ranging between 2 and 60uA. VBR shifted by 5V at 2μA compliance to 10V at 60μA setting. A second test was performed using stepped compliance of 1→10→30→60μA while sweeping V_d. VBR shifts were between 3 and 5V initially, then started to crowd together. Each increased compliance re-set this shift pattern. These results show that VBR walk-out was current dependent and suggest that the mechanism is linked to some form of current-dependent trapping of interface charge (see figure 13).

3.4 Currents present during DMOS walk-out.

VBR walk-out showed current-dependent right-shifted VBR after repeated V_d sweeps that has been documented using both SIMOX and ISE wafers. The goal of this study was to determine the degree of VBR walk-out present under normal AMEL operating (dc) currents, and whether there is any "untapped" VBR walk-out potential that can be utilized to increase operating voltages for increased luminosity. Understanding the mechanism for the VBR walk-out is important and could be utilized to improve DMOS performance.

3.4.1 Results.

Probing Pixel-HV and sweeping V_d under 2uA compliance, the operating current presently used by AMEL displays, demonstrated partial (≈10V) VBR
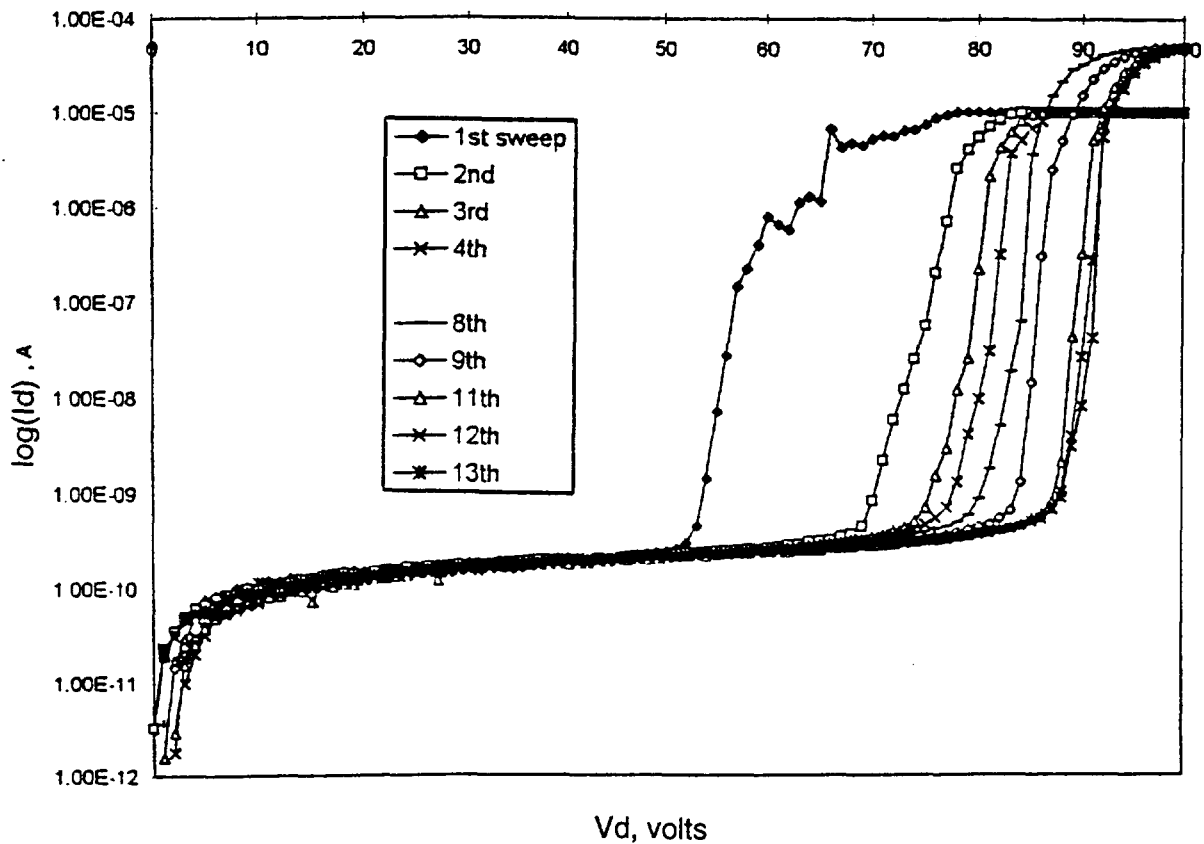
Figure 13: Characteristic VBR walk-out for Pixel-HV. Voltage from the drain to the source was swept from 0 to 100V. The 1st-four V_d sweeps (see legend) were performed at 10μA complience limits. The curves for the 5th through the 7Th sweeps were very close and thus were removed for clarity. The compliance limit was raised to 80μA for the 8th sweep and accentuated the rate of VBR walk-out. VBR approached 92V within 10 min., after which smaller shifts were observed and testing was terminated.

walk-out. Expanding current compliance to 10uA produced further walk-out (≈5V). Another 10V walk-out was obtained from Pixel-HV devices by sweeping V_d with a 50uA limiting compliance. Damage to the SIMOX wafer appeared at voltages near 80V. Current-dependent accumulation of charges in buried oxide surface states was tested and found <u>not</u> to be the mechanism for VBR walk-out. This was established by comparing walk-out using ISE wafers to that seen using the SIMOX wafers, SIMOX BOX structures were expected to have higher implant-related Nit levels. Identical VBR patterns were reproduced, showing a gradient of VBR shifting as current compliance was increased from 0.5uA to 80uA.

3.5 Duration and Rate of VBR change.

Time-dependent VBR walk-out was studied by probing Pixel-HV while rapidly sweeping V_d under 2uA compliance, the operating current used by AMEL displays.

3.5.1 Results.

SIMOX wafers typically demonstrate initial VBR near 55V which increased by 10-15V after the initial VBR sweep. Subsequent V_d sweeping produced less and less change but continued to walk-out. After 30 minutes of repeating V_d sweep the increment of change became perceptually constant at a calculated linear rate of 1.7V/hr. The longest continuous testing was for 26.5 hrs. In this long-term test VBR was initially observed at 52V and shifted to 62V after 45 min, thereafter the walk-out proceeded by progressively smaller steps until testing was terminated. After 26.5 hrs. VBR was 96V, representing a total ΔVBR of 44V. When retested 5 days later the first V_d sweep demonstrated a VBR of 93V indicating little or no loss of walk-out potential.

In a separate test, VBR walk-out was run for 30 min and resulted in a shift from 57V to 76V. When the same device was retested 3 days later, the VBR shifted from 71V to 79V (3 sweeps). Retested again 5 days later

produced similar results (74→79V). Each test demonstrated a small 4-5V shift after initial VBR near 74V. This result showed that intermediate walk-out (74V), without prolonged burn-in leaves Pixel-HV with a submaximal VBR by continuing to show small walk-out.

3.5.2 Discussion.

SIMOX wafers had VBR values near 55V and rapidly developed (walked-out) a higher VBR potential. VBR walk-out did not dramatically alter transistor function related to saturation current (I_{sat}), leakage current and threshold voltage (V_t). Thus, VBR walk-out developed independently of other functional parameters. Results above show that DMOS VBR walk-out was current dependent and demonstrated signs of current-related accumulation. Although charge trapping in BOX oxides was ruled out, it is possible that charges were trapped in the field oxide. Once understood this parameter will certainly offer greater potential in DMOS transistor design and AMEL performance.

3.6 VBR walkout.

3.6.1 Simulated DMOS processing and electric behavior.

Simulations provided critical information for understanding the interaction between materials, processing and electrical performance. DMOS VBR on SOI was simulated and compared using both isothermal and non-isothermal energy balance models contained in Silvaco simulation software package (interactive Athena, Atlas, Spicses, Blaze and Giga programming). Dominant temperature effects, evoked by the lattice temperature model, were on energy gap and band parameters, carrier mobility, and impact ionization rates. According to this model, carrier mobility decreased with increased temperature or impurity concentration (19,44).

The figure sets associated with the simulations are sequential graphical representations of the process-simulated DMOS transistor's electrical behavior

according to the encoded models. They are shown as a collection in section 3.6.6. The differences in the model (solutions) are discussed in the text.

3.6.2 Process parameters for simulated DMOS.

Process parameters used in the DMOS simulation were adjusted to match the actual Pixel-HV design used to fabricate the working device. The buried oxide layer was 0.4μm thick, the silicon mesa was 0.35μm thick, the spacer oxide was ≥200nm thick, and the gate oxide was 40nm. Two processes for field shield oxide (FOX=0.25μm) were compared, deposition of oxynitride and LOCOS. LOCOS represents the actual process used to fabricate the FOX in the Pixel-HV device.

The n-drift region measuring between 8 to 12μm from channel-edge to drain-edge was formed by implanting (25 and 50 KeV) low doses (1×10^{12} atoms) of phosphorous. Final phosphorous densities in the n-drift region, 2μm steps from the channel to drain were: 3×10^{16} to 4×10^{17} atoms/cm^3. Resulting VBR values ranged from 20V up to 52V. Many features (e.g., FOX thickness, doping and channel length) are know to influence the VBR of the DMOS. This study focused on how changes in the n-drift p-n junctional depth (Xj) caused impact ionization potential to spread along the n-drift region and how this translated to VBR.

3.6.3 Energy Balance Simulation of a DMOS device.

DMOS structures have been simulated using Medici software which calculate VBR at the point where ionization intergrals reached unity (17). However, rectangular coordinates were used to define each area and the influence of the LOCOS FOX structure was not considered. The purpose of the Silvaco simulation was to simulate the effects of process-related influences on VBR. In particular, the shape of the n-drift region, and influence of LOCOS field shield oxide were investigated with regard to distribution of the impact ionization rates.

Simulations solved for drift-diffusion through application of energy balance model which incorporates Poisson's equation and energy flux equations. Solutions were obtained for both electrons and holes. Transport parameters for mobility and impact ionization coefficient did not account for lattice heating unless specifically included in the model.

3.6.3.1 Results.

Encroachment of silicon consumption during LOCOS oxide growth was responsible for a semi-abrupt curvature in the oxide continuum between the gate and FOX. Gate overlap of drain (GOLD) by the polysilicon gate was designed to bridge the inverted channel region into the n-drift region.

Figure 14 shows that pre-VBR voltage increases caused potential lines to cluster at abrupt changes in the p-n junction interface (Xj) of the n-drift region. Potential crowding was observed under regions of abrupt change in deposited FOX (Figure 14). Figure 15 demonstrates an initial build up of impact generation rate under the GOLD (44) and deposited FOX regions. Sequential figures (Figure 15) show how impact ionizations accumulate at the p-n Xj step in the mid-n-drift region. Increased p-n curvature (bending) in the n-drift region created site of impact ionization and eliminated design advantages (higher VBR) of the n-drift region (Figure 18A).

Improved VBR ($\approx$20V) was obtained by reducing Xj in the n-drift region. The leading edge of the n-drift region reduced the ionizing impacts reaching the deep Xj of the drain (Figure 16). Impact ionization spread between the leading edge of the n-drift region and the drain. The separation of this spread reduced the impact ionization rate at both locations and prolonged avalanche breakdown leading to VBR (Figure 18B).

Growth of the FOX created a LOCOS bird's beak (see Figure 7) and an abrupt step formation in the p-n Xj. Spreading was observed after this step (see Figure 17), the primary site of impact was focused at the p-n Xj step just beneath the FOX edge. Like the step formed by implant (compare Figures

15 & 17), the LOCOS-induced Xj step caused impact ionizations to accumulate and lead to lower VBR (Figure 19A).

Increasing phosphorus implant gradients along the n-drift region helped to reduce the LOCOS geometric influence on p-n junction. Decreasing implant gradients resulted in low VBR (data not shown). Misalignment and increased overlap of the n^+ source implant by the gate did not alter normal I_d-V_d function at fixed gate voltages and ultimately showed a relatively high VBR. However, low current leakage was detected as drain voltage approached VBR (Figure 19B). The leak was probably the result of a graded p-n junction and was removed by careful attention to gate alignment of the n^+ source implant.

3.6.4 Electrothermal simulation of VBR Walk-out.

Application of the lattice heating solutions to the silicon mesa region had a significant affect on the results of DMOS electrical simulations. Solutions that did **not** incorporate lattice heating (top, Figure 20) demonstrated leading edge n-drift impact ionizations. When modelled with lattice heating (bottom , Figure 20) impact ionizations were reduced. This change correlated to a reduction in the number of electrons at higher electron temperature suggesting that accelerated electrons were losing their energy through lattice scattering (compare top sequence and bottom set of Figure 21).

Simulations on DMOS structures that incorporated the lattice heating model demonstrated greater spreading of the initial impact ionization across the birds beak p-n Xj (Figure 22). This de-localized the initial build-up of impact ionizations and allowed them to spread to the n^+ drain. The result was less crowding of the impact ionization rate along the p-n junction curvatures and improved VBR. Figure 23 shows VBR after simulating DMOS devices with deposited oxynitride FOX films along with lightly graded n-drift regions while using the lattice heating model.

3.6.5 Discussion.

Incorporation of lattice heating gave solutions showing improved VBR values but does not explain the mechanism for VBR walk-out (changes up to 40V) observed while measuring the Pixel-HV devices. Kim et. al demonstrate that increased lattice scattering due to self-heating reduced impact ionizations near the drain (45). In standard NMOS SOI transistors holes generated by the impact ionizations cannot find their way to lower fields in bulk silicon, and become trapped in potential wells setup between the source and drain. Potential wells filled with holes can increase recombination near the source and reduce electron currents at a given voltage. Increased recombination between electrons injected and accumulating holes near the source has the potential to contribute VBR walk-out. Higher voltages would be needed to proviide the free electrons for acceleration leading to impact ionizations and avalanche breakdown (VBR).

The increase of the body potential increases I_D at a kink voltage as the threshold voltage (V_t) decreases (45-47). Accumulations of trapped avalanche holes under high drain bias could raise the potential of the silicon mesa and decrease the V_t (46,47). Under these conditions the majority of the channel current is composed of electrons injected to balance the pre-existing hole current (45), hence control is lost and the device cannot be turned off by reverse gate sweep.

3.6.6 Simulation figure sets; Figures 14→23.

This section contains the figure sets associated with the simulations discussed in section 3.3. In some cases they are sequential graphical extracts of the process-simulated DMOS transistor's electrical behavior. Figures containing multiple boxes were generated using the Tonyplot graphics program (Silvaco) and can be read from left to right, where each box to the right represents the results of the simulation at higher voltage.
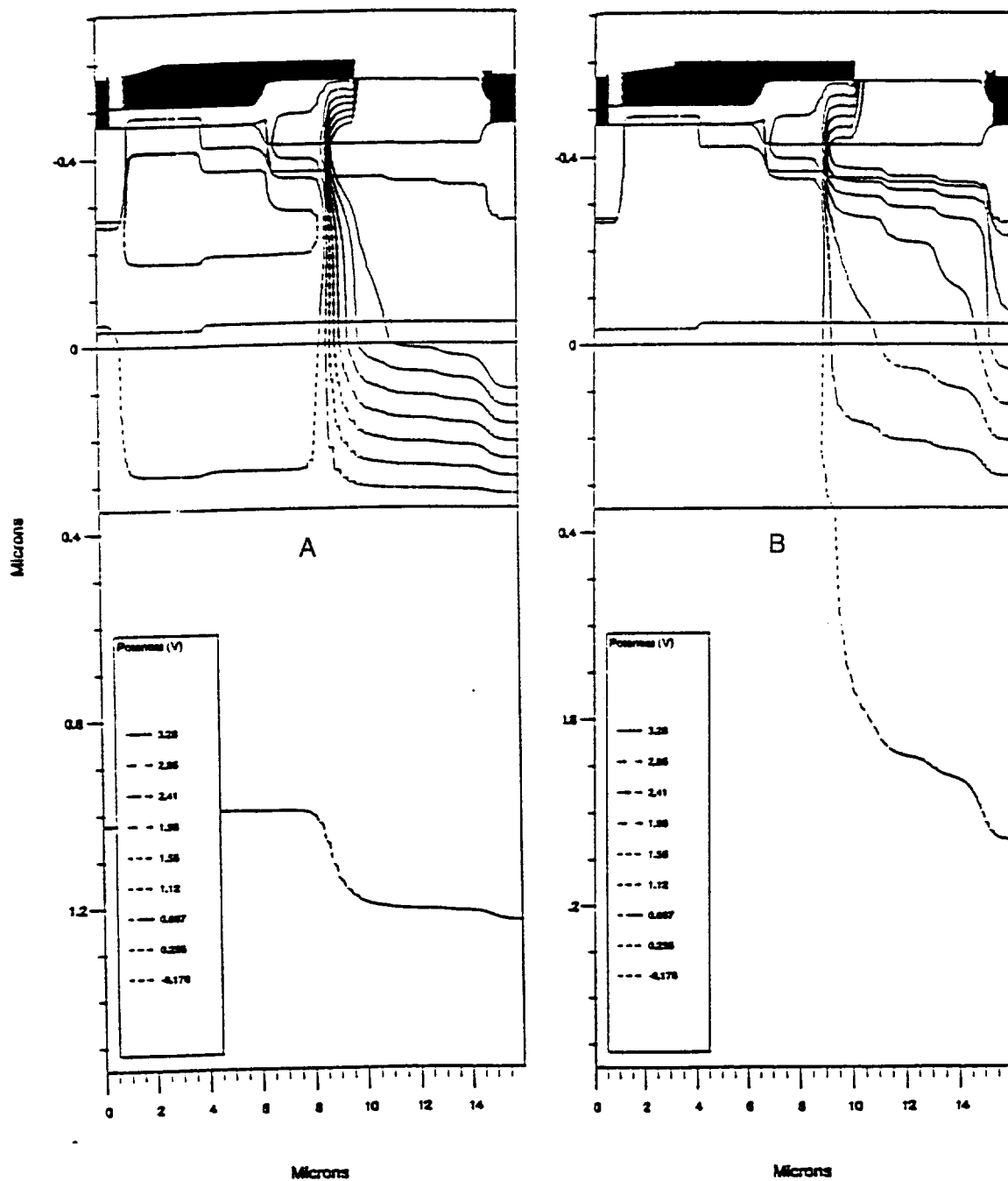
Figure 14: Developing potentials during DMOS simulation. Solutions were based on energy balance alone (A), or lattice heating (B).
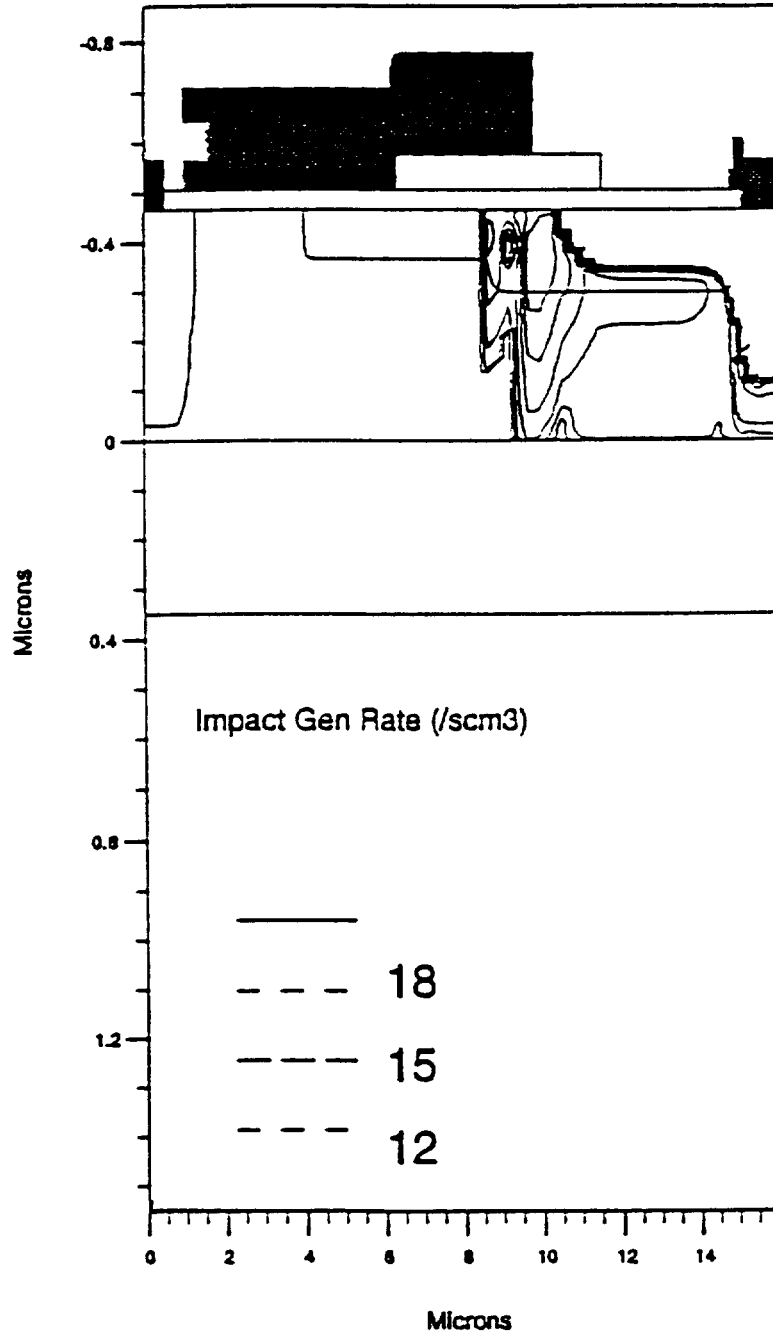
Figure 15: Simulated impact ionization rate <u>with</u> Xj step. Build-up of impact ionization rate. Notice the abrupt change of the p-n junction near the gates overlap of the FOX.
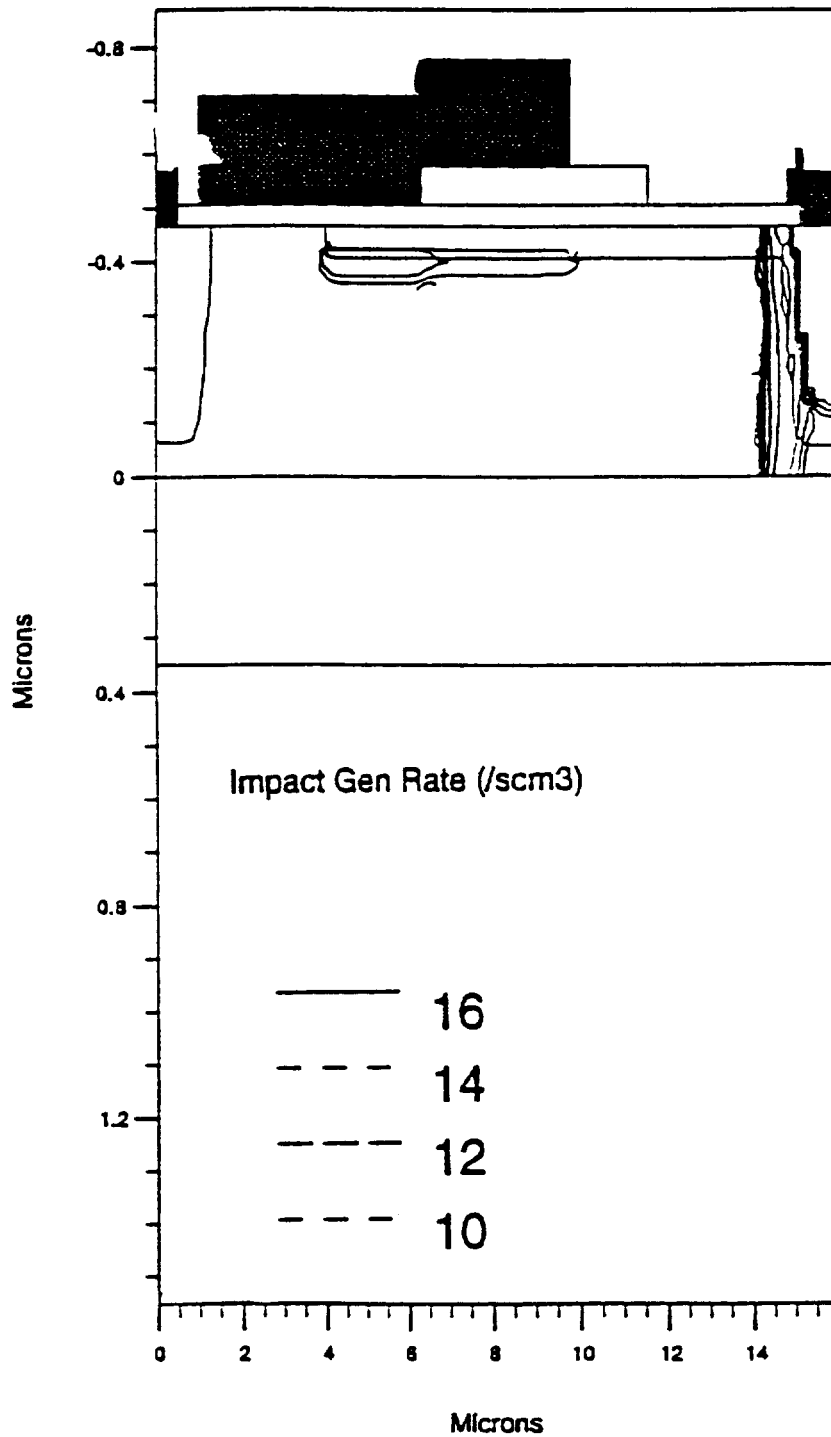
Impact Gen Rate (/scm3)

——— 16

— — — 14

— — — 12

— — — 10

Microns

Microns

Figure 16: Simulated impact ionization rate <u>without</u> Xj step. Build-up of impact ionization rate. Lack of the abrupt change in the p-n junction permits greater impact ionization spreading.
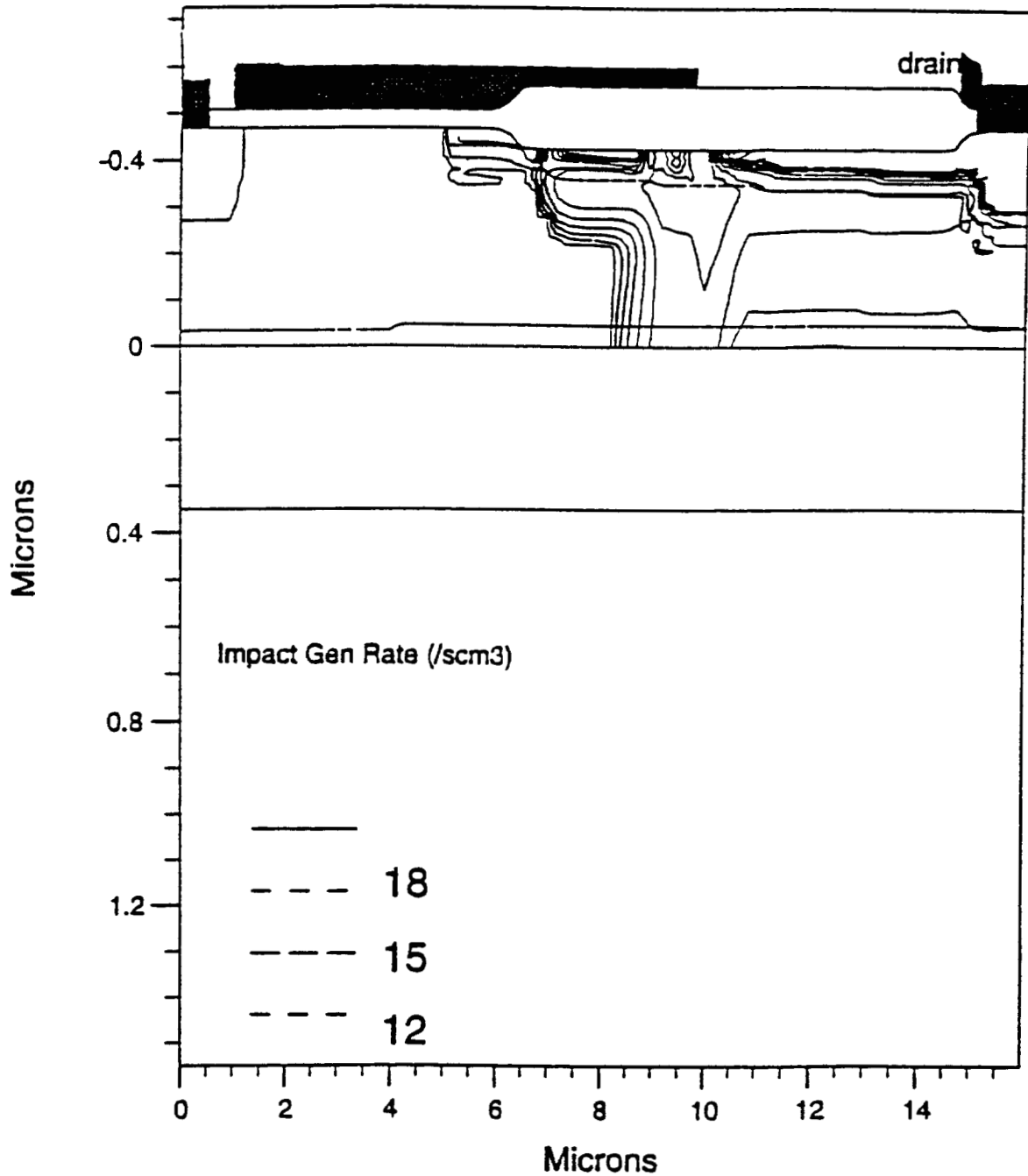
Figure 17: Effect of LOCOS on simulated impact ionization rate. Build-up of impact ionization rate and the effects of the LOCOS structure on p-n junction curvature. The abrupt change in the p-n junction near the birds beak creates a site for impact ionization to build up.
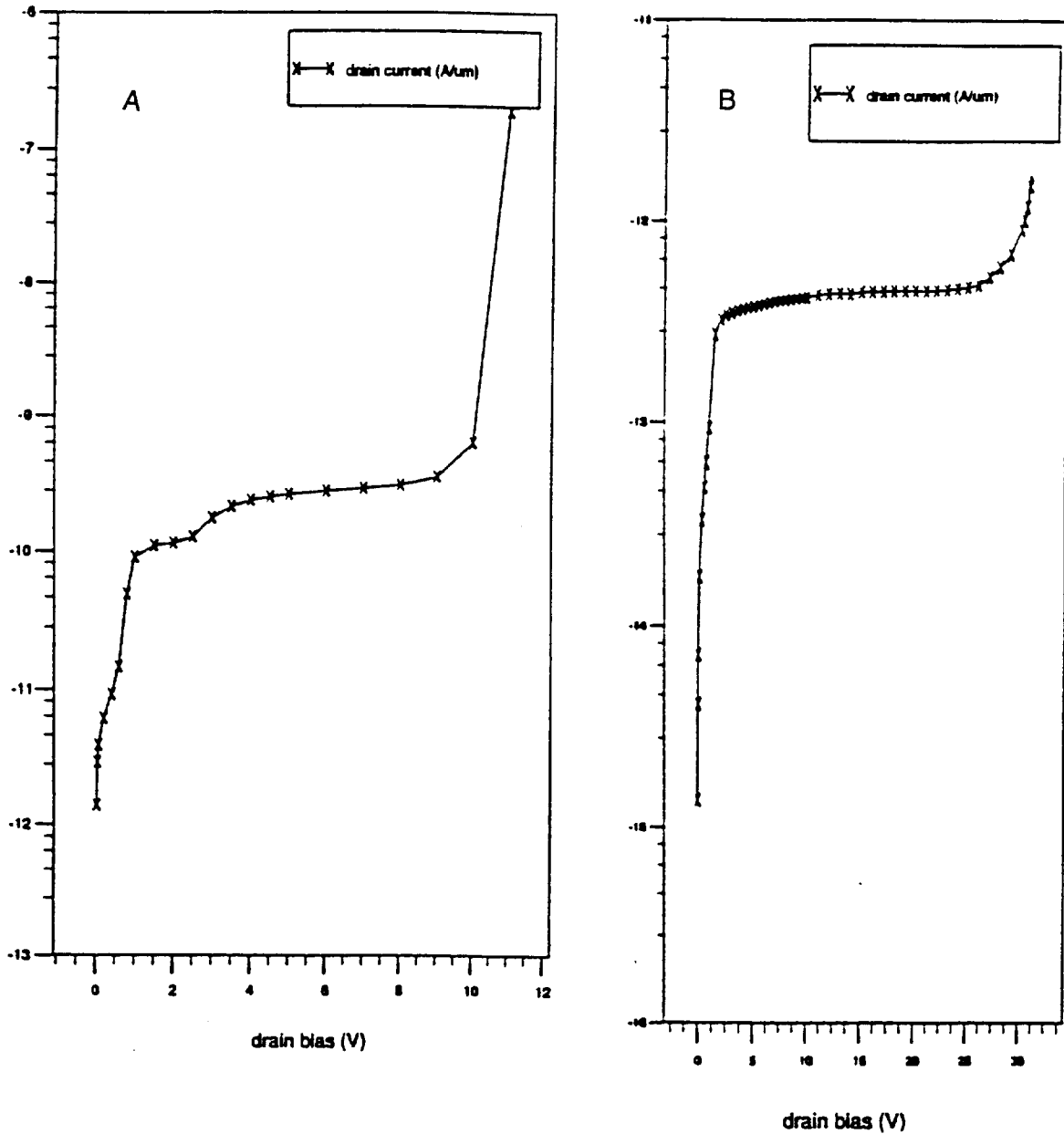
Figure 18: Reverse breakdown voltage (VBR) IV-curves. **(A)** VBR for the simulation data shown in figure 15. **(B)** VBR for the simulation data shown in figure 1*6.*
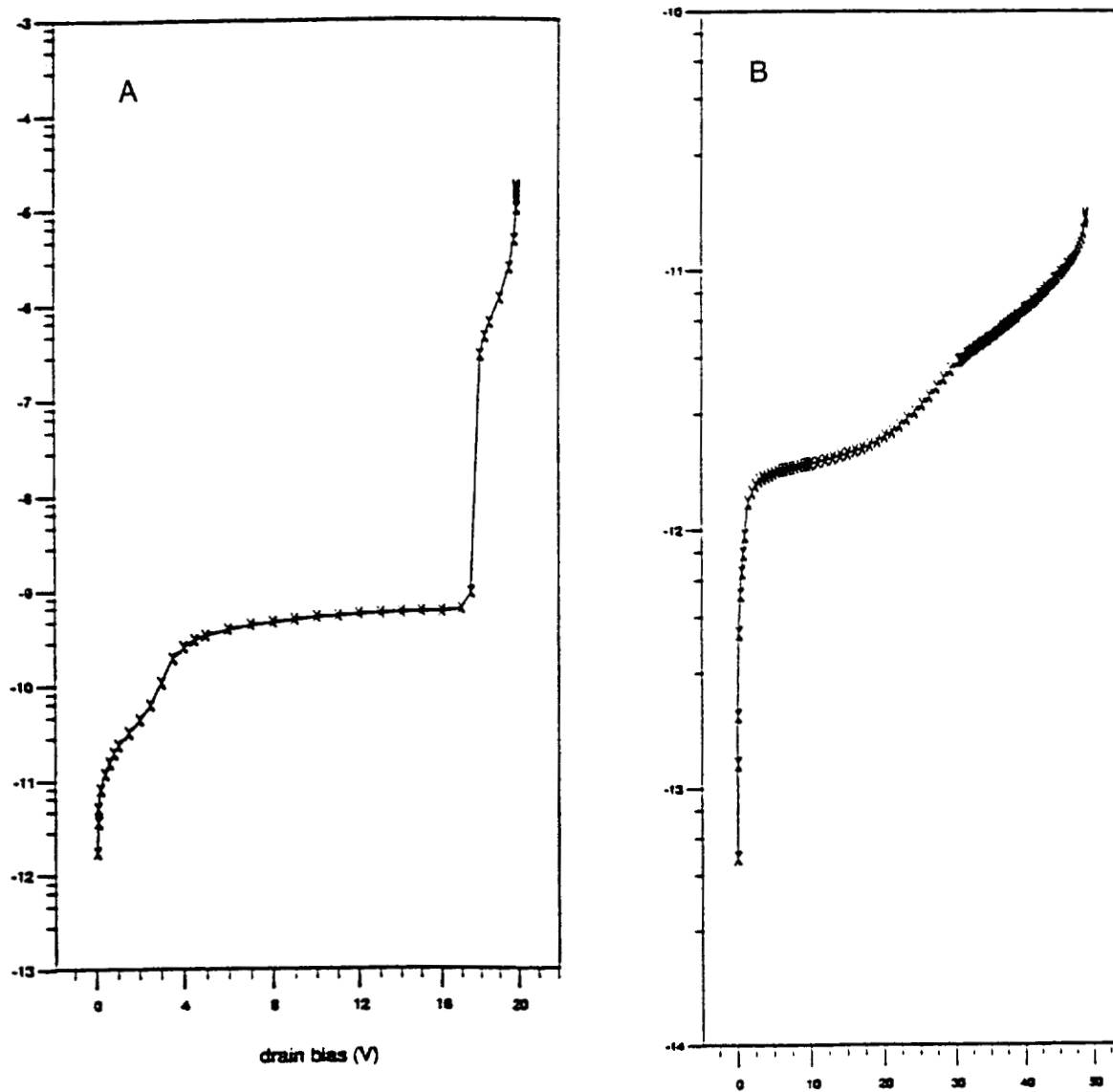
Figure 19: Reverse breakdown voltage (VBR) IV-curves. **(A)** VBR for the simulation data shown in figure 17. **(B)** VBR for the same device with significant overlap (~0.2μm) between the gate and the source implant/diffusion.
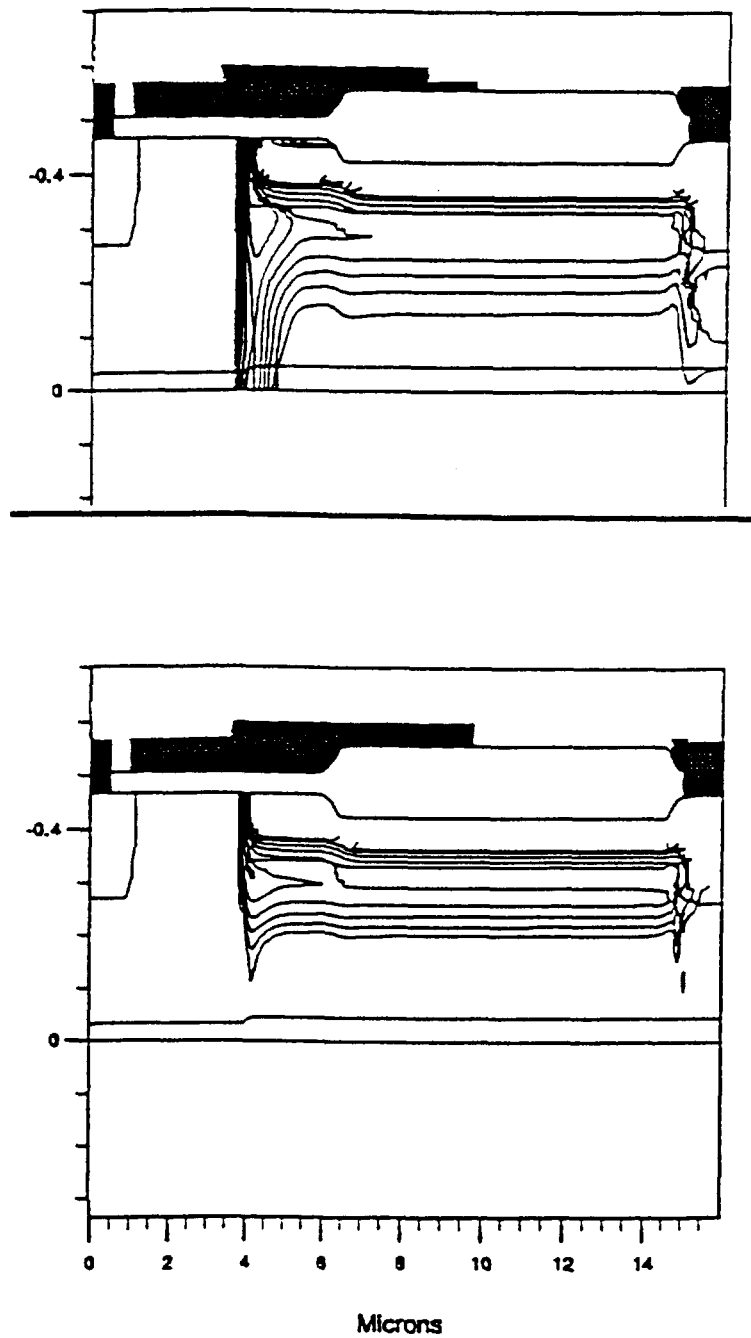
Figure 20: Modelled VBR with and without lattice heating. **TOP:** Early build-up of impact ionization rate under a LOCOS structure solved by the standard energy balance model (48). **Bottom:** Early build-up of impact ionization rate under a LOCOS structure solved by including lattice heating in the standard energy balance model (48).
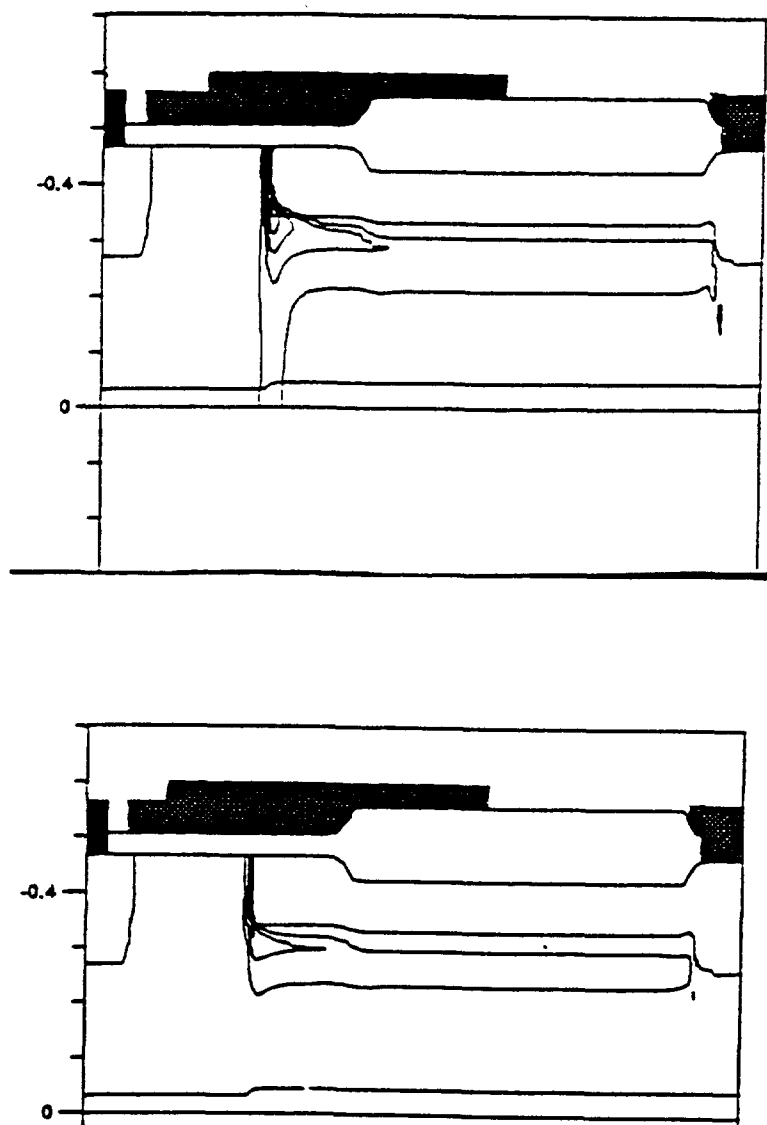
Figure 21: Modelled electron temperature with and without lattice heating. Same simulations as shown in figure 20. **TOP:** Early build-up of electron temperature under a LOCOS structure solved by the standard energy balance model (48). **Bottom:** Build-up of electron temperature under a LOCOS structure solved by including lattice heating in the standard energy balance model (48).
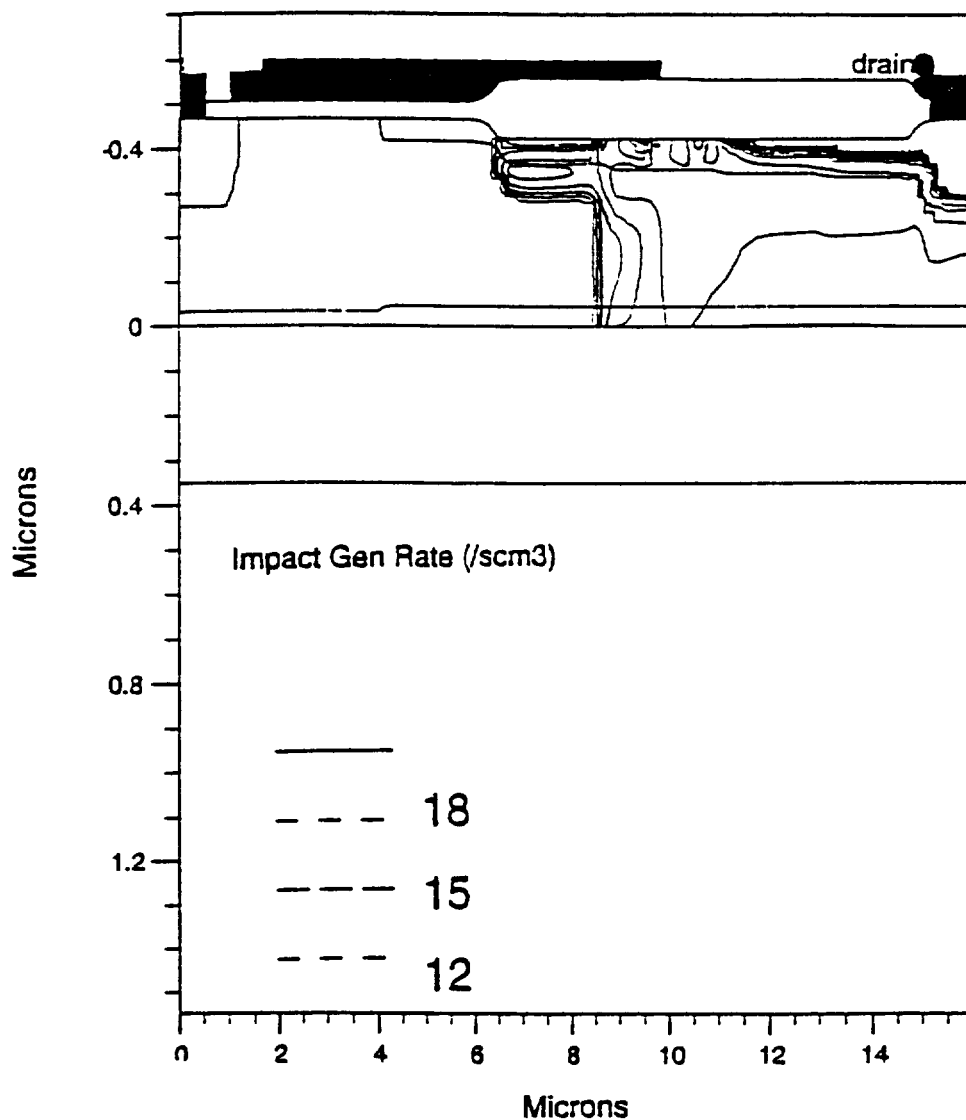
Figure 22: Walk-out caused by lattice heating. Similar to the simulation presented in figure 17, except that lattice heating was included in the models. Build-up of impact ionization rate and the effects of the LOCOS structure on p-n junction curvature. Lattice heating permitted greater spread on the impact ionization.

Figure 23: Improved VBR caused by lattice heating. Greater VBR cab be realized by incorporating lattice heating models, lightly graded n-drift regions and deeper drain Xj.

3.7 Conclusion.

The focus of this thesis has been examination of the influence of side-wall and LOCOS oxides on SOI transistor function and the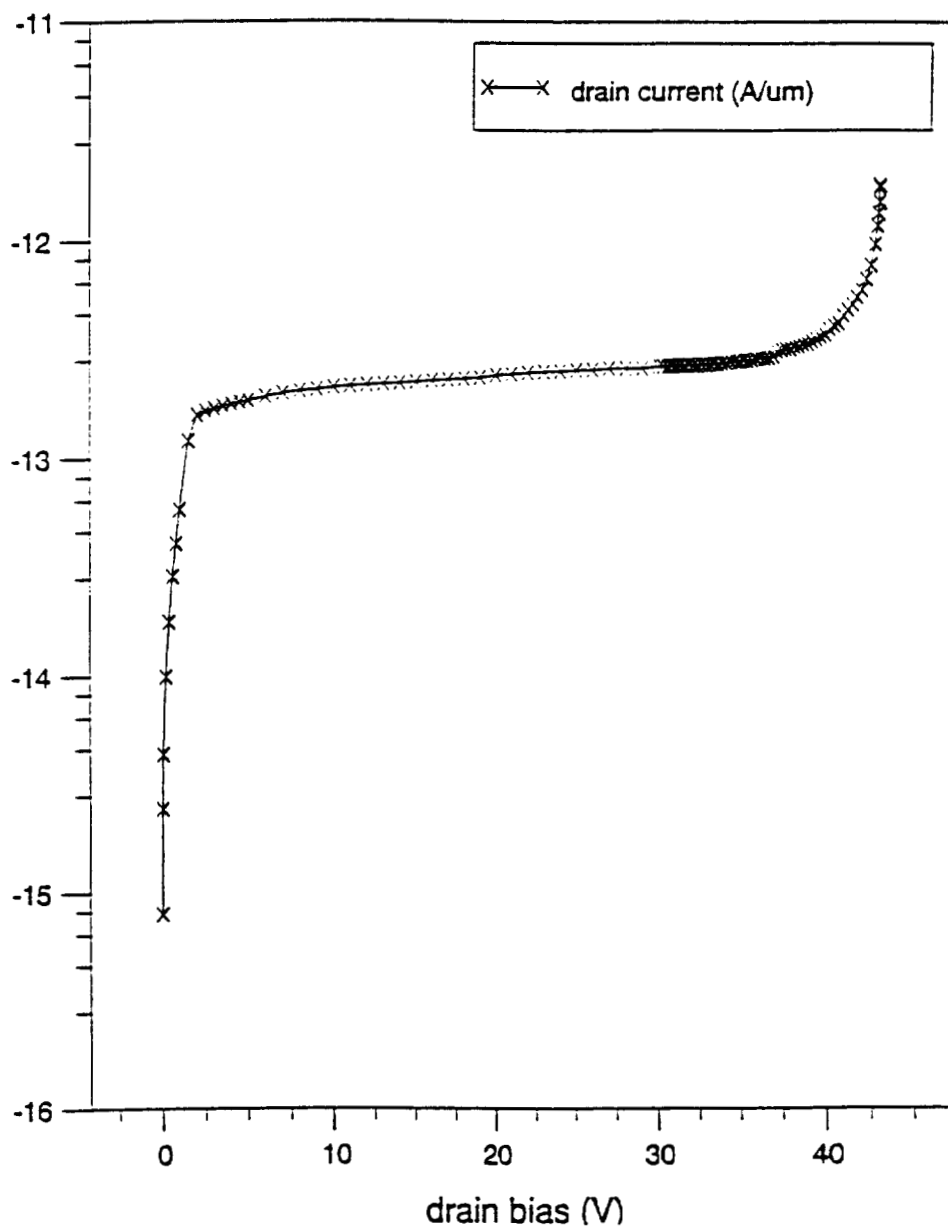 VBR of the high voltage transistor Pixel-HV. Silicon oxide completely surrounds the silicon mesa in which the transistor has been fabricated. This isolation provides superior electrically isolation but has disadvantages as well. Oxide isolation allows heat and charge to accumulate in the silicon. Build up of heat and charge directly affect scattering of carriers and lead to the floating body effect, respectively. Side (mesa-edge) channel function is parasitic to the normal operation of SOI NMOS and PMOS transistors. The advantage of using SOI substrate (electrical isolation) for the purpose of operating high density arrays of transistors containing high voltage DMOS transistors must be balanced against the parasitic devices inherent in the oxide capsule.

The purpose of the n-drift region of the DMOS transistor is to reduce impact ionizations and thus increase VBR. Spread of impact ionizations along the n-drift region was key to increased VBR and was affected by changes in the p-n Xj depth. The simulation data show that deposited FOX layers provides a level horizontal under-structures that translate into n-drift Xj levels better suited to spreading impact ionizations. Other optimizing features were: (i) deeper source/drain implants to allow for distant vertical spread of impact ionizations; (ii) thicker FOX and BOX structures to reduce abrupt vertical field changes and back channel formations, respectively; and (iii) body tied sources with minimum gate overlap to reduce charge accumulations and high leakage currents, respectively.

The low thermal conductivity of silicon oxide insulates the SOI channel region and prevents heat dissipation. Self-heating resulting in lattice scatter reduces mobility of accelerated carriers, requiring higher field strength (voltage) to achieve impact ionization leading to avalanche breakdown. Inclusions of lattice heating was required to obtain a close match between VBR simulations and experimental VBR data. While improving simulated VBR, lattice heating did

not explain the mechanism for VBR walk-out. The simulations did however show that site-localized spreading (verses delocalized spreading) greatly improved VBR.

3.8 Future Direction: This study has defined the untapped potential to be utilized to produce greater VBR and thus greater on/off contrast for light production from the AMEL displays. This potential may be as simple as increasing operating currents above 2uA (=maximum current under normal operation, Imax=C*dV/dt*ω*2π*cosω). The current, and thus VBR, could be increased by increasing the operating frequency. Full utilization will require a better understanding of the mechanism.

The mechanism involves an irreversible change that is likely to be associated with trapped charges in the FOX. Future device simulation should be attempted after creating discrete "pockets" of stress-induced traps in the FOX. The stress sites would originate from geometries conducive for the accumulations of electric fields and impact ionizations (these have been demonstrated in this study). It may be that these centers of impact ionizations are sites of increased FOX traps. As the FOX traps accumulated, the center of the electric field responsible for the impact ionizations shifted. During the shift, field energy could be insufficient at any of the sites to support the required ionizing impacts for VBR. Thus resulting in VBR walk-out.

The greatest improvements in optimizing DMOS VBR were obtained through simulating process-related geometric influences on the spread of impact ionizations. As process issues, they can be changed and will have dramatic influence of the performance of the actual device (Pixel-HV). Future work on the DMOS transistor should also focus on how other modalities contribute to the mechanism of VBR walk-out.

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Vita

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He will live long and prosper with his wife Jennifer and two children, John and Avery.