AC/DC CHARACTERIZATION OF NMOS AND PMOS DEGRADATION UNDER AC/DC STRESS

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A thesis submitted to the faculty
of the Oregon Graduate Center
in partial fulfillment of the
requirements for the degree
Master of Science
in
Electrical Engineering

May 1989

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ACKNOWLEDGEMENTS

I wish to express my gratitude to my advisor Professor Dae Mann Kim for his encouragement, direction and communication of his love of physics and learning.

I am very grateful to Intel Corporation for allowing me the use of their facilities and the material which made this thesis possible. I am particularly indebted to Mohsen Alavi for directing my work at Intel and to the people in the reliability physics lab (Joan Davis, Tim LaBeck, Yung Huei Lee, Stan Maston, Stan Miller and John Thomas). Without their support and assistance much of this work could not have been done.

I also wish to thank the members of the thesis committee, Dr. John Blakemore, Dr. Ron Burghard, and Dr. Mohsen Alavi for their helpful suggestions and comments.

Finally, I thank God for His faithfulness and goodness in giving me the opportunity to learn and attend OGC.

To my Aunt, who has encouraged and demonstrated the pursuit of excellence.

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ABSTRACT

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Hot carrier induced NMOS and PMOS degradation is experimentally examined. AC and DC measurement of n- and p-channel device parameter shifts are compared following DC stress. In both types of devices, there was no appreciable difference in AC and DC measurements of device degradation. The data indicate that hot carrier induced interface states are shallow and fast with lifetimes less than 20 ns. The effects of AC and DC stress on NMOS and PMOS are studied in terms of DC characterization. In PMOS, AC drain stress is generally quasi-static. On the other hand, AC gate stress produced enhanced device degradation corresponding to the worst case DC stress. In NMOS, the effect of AC stress is apparent and drastic. Here, the threshold value of the oxide electric field, Eot is operative. Below Eot AC drain stress is again found to be quasti-static. However, AC gate stress is shown to give rise to enhanced parameter shift compared to the corresponding DC stress. This dynamic stress could lead to device failure for an oxide electric field greater than Eot. Above Eot drain pulsing also results in pronounced device degradation again leading to device failure. The observed AC stress effects

are consistent with the two carrier model.

CHAPTER 1

INTRODUCTION

As silicon fabrication technology has advanced, the feature size of MOSFETs have been continuously reduced to enhance packing density and device speed in VLSI circuits. Accompanied with this scaling down of device features, however, are many undesirable side effects that can pose serious limitations on reliability. The major concern has been with the increasingly large electric fields that result from the decreasing channel length. Hot carriers resulting from these high electric fields can severely degrade device characteristics. Hence, the stability of short channel MOSFETs is a growing area of concern in VLSI. It has thus become imperative to clarify hot carrier phenomena.

Hot carrier induced degradation of device characteristics under DC bias stress has been well researched. Device degradation has been attributed to carriers being accelerated in the high field region near the drain. This in turn gives rise to hot carrier generation via impact ionization. These hot carriers break or strain interfacial bonds, generating interface

states or are injected into the interface/oxide region, giving rise to interface and/or oxide trapped charge.

More recently, device stability under pulsed or AC biasing is being extensively studied, since AC stress simulates the device operating conditions in actual circuit applications. However, the mechanism for dynamic degradation under AC stress has not been fully clarified thus far. It is not clear to date whether or not the same kind of mechanisms for device degradation may be operative under both AC and DC biases. Also it is not clear whether or not DC and AC measurement of parameter shift arising from a common DC stress are the same. There is growing evidence that additional dynamic mechanisms may enter into AC bias induced hot carrier effects.

Present AC hot carrier treatment is primarily based on empirical modeling and computer simulation rather than upon experimental data. This simulation work makes two important assumptions. First, that the observed degradation of device electrical parameters under DC measurement is the same as that under AC measurement, and second, that AC hot carrier stress behaves similarly to DC stress for a small increment of time (quasi-static assumption). The purpose of this thesis is to test experimentally these two assumptions.

For this purpose, the DC and AC behavior of NMOS and PMOS devices was examined under DC and AC stress. However, there were some experimental limitations that need to be pointed out. AC measurement data was restricted by the 20 ns circuit resolution. Also the frequency of AC stress was limited by circuit parasitics to 10 MHz.

The major thrust of this thesis is directed toward the characterization and comparison of, (i) DC and AC measurement of device parameters following DC stress, and (ii) DC and AC stress in terms of parameter shifts measured under DC bias conditions. This thesis is divided into six chapters. Chapter 2 presents a survey of the background literature in these areas. The description of experiments performed during the course of this study is given in chapter 3. In chapter 4, the results obtained are presented and discussed. Chapter 5 presents the qualitative interpretation of the data, and in chapter 6 the highlights of the work are summarized, together with a few concluding remarks.

CHAPTER 2

BACKGROUND LITERATURE

Hot carrier induced degradation of device characteristics under DC conditions has been well characterized and researched. A survey of published literature shows that the hot carrier problem has been extensively studied for both n- and p-channel MOSFETs. The primary source of device degradation is generally believed to be the same for both n- and p-channel cases, namely high electric fields and the resulting impact ionization [1]. However, the manifestation of this damage is markedly different in these two types of devices.

2.1 NMOS

Hot carrier effects in n-channel transistors were studied by Hu et al. in 1985 [2]. They presented a physical model which relates the large channel electric field to the shifts in pertinent device parameters. The model was based on this high electric field causing (i) impact ionization giving rise to substrate current, (ii) hot electron emission producing gate current, and (iii) interface damage resulting in interface state generation.

Hu et al. pointed out that NMOS degradation shows up primarily in

three device parameters, a shift in threshold voltage, Vt, subthreshold swing, S and transconductance, Gm. The authors proposed that n-channel hot electron induced degradation is mainly caused by the generation of interface states rather than by electron trapping in the oxide. Furthermore, these interface states reduce local carrier density and mobility and are generated by hot electrons rather than by hot holes. Additionally, data were presented to support a linear correlation between Vt, S and Gm via the total number of generated interface states [2].

Much work has been focused on correlating n-channel MOSFET degradation to interface state generation and oxide trapping. In 1988 Robin et al. presented a hot electron oxide trapping model to explain NMOS degradation [3]. They use the bond-stretching model of the Si-SiO2 interface of Sakurai and Sugano [4]. Specifically, weak and stretched bonds with varying angles introduce a continuum of shallow and deep level traps. Robin et al. point out that although improved oxidation technology has reduced trap concentration, shallow trap levels persist in the oxide bulk and deep trap levels near the interface because of its higher density of strained and dangling bonds.

In 1987 Chen et al. studied electron trap generation during high oxide field stressing [5]. They proposed that neutral electron traps could

be generated by the energy released during the recombination of free electrons and trapped holes, and that this is the mechanism of electron trap generation during high field oxide stressing. Chen et al. explain this recombination induced trap generation in a manner as may occur in the two carrier model.

The two carrier model was proposed by S. K. Lai in 1981. This model pointed out a key mechanism responsible for generating the interface and/or oxide trap states. The model is based on the (i) injection and subsequent trapping of holes in the oxide, and (ii) the capture of injected electrons by trapped holes [6]. It is important to note, as pointed out by Lai, that this is not the usual recombination process that occurs in silicon. When a hole enters a strained bond, and reaches a lower energy state by deforming it further, it is trapped by the strained bond. Electron trapping by holes could then be described as electron capture by Coulombic attractive charge centers. When trapped holes capture electrons, deformed bonds cannot be restored to their original states. In this manner, neutral traps would be formed both in the oxide bulk and at the interface.

In 1987 Tsuchiya performed experiments to distinguish the effect of the electron trapping in the gate oxide from that of interface trap generation [7]. He concluded that transconductance degradation was caused by

both trapped electrons and generated interface traps. However, the effect of interface traps becomes increasingly important and that of trapped electrons less important, as degradation increased.

In 1986 the oxide trapping properties were examined by Nissan-Cohen et al. with charge injection stress experiments [8]. They presented a dynamic oxide trapping model based on two competing processes: (i) the continuous trapping of a portion of the injected electrons in localized oxide states, and (ii) the detrapping of the electrons from occupied traps. Their data showed that the rate of trap generation increased exponentially with the oxide electric field, and that only a small fraction of the newly generated traps are occupied. Hence, measured oxide charge buildup does not accurately reflect the actual increase in generated traps.

Instabilities in n-channel transistors have been reported to be markedly increased at stress bias conditions that cause peak substrate current [9,10]. It has also been suggested that both hot holes and hot electrons generated by impact ionization, together with high energy electrons in the channel, play an important role in device degradation [10-12].

In addition to the interface state generation [2,13,14], increased source/drain series resistance [14-16], decreased effective mobility [2,14,15], velocity saturation [16-18] and charge trapping localized near the drain

[7,19,20] have also been considered as possible mechanisms for device degradation. These phenomena are all collectively responsible for the observed decrease in Gm, decrease in Idsat, increase in Vt and increase in S [2,13, 15,19,21].

In 1988 Trocino et al. related some of these hot carrier effects in the n-channel to the stress bias [22]. They proposed that the degradation observed with a positive gate oxide electric field stress, i.e. ($Vg > Vd$) is a result of localized electron trapping in the oxide near the drain. On the other hand, the damage resulting from a negative electric field stress, i.e. ($Vg < Vd$) is primarily from interface trap generation localized near the drain.

2.2 PMOS

Recently, hot carrier induced degradation in p-channel devices has been a growing area of concern as well. Hot carrier effects in p-channel devices differ considerably from those in n-channel devices.

Instabilities in p-channel transistors have also been reported to be considerably enhanced at stress bias conditions causing peak substrate current as in the n-channel case [9,23]. However, more recent work indicate that the enhanced damage in p-channel transistors is more closely

correlated to peak gate current [10,24,25]. Hot electrons induced by impact ionization have been suggested to be primarily responsible for device damage [25]. Again this is in contrast to the n-channel case where both hot electrons and hot holes are believed to cause degradation [12,26]. Differences in the polarity of the effective gate field, i.e. a positive or negative field, account for how the hot carriers are injected into the gate oxide and reach the gate terminal near the drain region. In the p-channel device operating in the saturation region, ($Vg > Vd$) hot electrons are pulled into the oxide, some will be trapped and others will traverse the oxide to constitute the gate current. Holes are swept from the channel to the drain terminal. Simultaneously hot electrons are also pulled towards the substrate to constitute substrate current. Again this is in contrast with the n-channel operating in the saturation region, where the polarity of the bias is switched. Thus, for the n-channel case, holes contribute to both gate and substrate currents. Most of the electrons are swept from the channel to the drain terminal while some are believed to be trapped in the interface [19,25,26,27].

The different physical processes involved in n- and p-channel devices give rise to contrasting damage effects. Specifically, the directions of device parameter shifts in the n- and p-channel, are often opposite to each other. For the case of the p-channel device, this damage is exhibited in an

increased Idsat, an increased Gm, a decreased | Vt | and an increased S [10,25,28,29]. These shifts in device parameters are explained in the literature as follows. Impact ionization induced hot electrons are accelerated by the positive gate field into the gate oxide near the drain. Consequently, electrons are trapped near the oxide interface, inverting the surface to p-type, and resulting in an extension of the p+ drain region. This in effect reduces the effective channel length [14,19,25]. Koyanagi et al. caution that the decrease in punchthrough voltage which results from trapped electrons creating a shortened channel, may place a fundamental limitation on device scaling [25].

Hot carrier effects have been examined in n- and p-channel devices when the measurement was done with the source and drain terminals interchanged from that of the applied stress [30-32]. In 1983 Lombardi et al. measured electrical parameters before and after stress using the same (forward) and opposite (reverse) polarity, to that of the applied stress. Data showed an enhanced degradation for parameters measured in the reverse mode. They explained this finding in terms of the potential energy barrier lowering caused by the trapped charge. That is, electrons trapped closer to the injecting terminal (i.e. the terminal used as the source) would be more effective in reducing the surface potential than electrons trapped near the terminal used as the drain [33]. More measurable

degradation in the reverse mode can also be accounted for with the decreased screening of the trapped charge that occurs with the smaller source junction depletion region [32].

2.3 AC STRESS

The study of AC hot carrier induced degradation is important since the device operates in a dynamic AC environment in actual circuit applications.

Until recently, most AC hot carrier treatment was primarily based on empirical modeling and computer simulation rather than experimental data. Quasi-static models were used, based upon the assumption that AC hot carrier stress behaves similarly to DC stress for small time increments. Kuo et al. voiced a concern about the applicability of a quasi-static model and the use of DC stressing data for AC stressing lifetime predictions [34]. To support their concern, they cited the work of Weber et al., showing that enhanced degradation occurs as a result of fast high to low gate transients in the presence of a high drain bias [11]. They proposed that this was due to the simultaneous presence of a very high channel field and a large capacitive drain current, which produced an additional component of substrate current during the falling edge of the gate pulse. This

capacitative current cannot be incorporated into the quasi-static substrate current model. Interesting experimental evidence was also reported by Bellens et al. in 1988 [35]. They observed that the switching off of the transistor causes substrate current which keeps flowing during the gate switch off period, another condition not covered in the quasi-static model.

While hot carrier induced damage under DC stress has been well characterized, no unanimous agreement exists on the mechanism for AC degradation. However, there appears to be some consensus, namely, that dynamic degradation may involve an additional mechanism arising from the periodic switching of field conditions [35-37].

In 1988 Cham et al. reported that the degradation of electrical characteristics of AC stressed n-channel MOSFETs is not in general commensurate with the DC results [38]. Specifically, AC drain stress is equivalent to DC stress by the active duty cycle. However, AC gate stress produced much more damage than the duty cycle factor would have indicated. The authors proposed that it was the gate voltage swing from high to low value under constant high drain bias that caused the most severe damage.

In 1988 Ong et al. reported a similar conclusion for p-channel MOSFETs when the gate pulse turn-off transient was short, concurrent with a

high drain voltage [37]. Aoki et al. evaluated hot carrier effects under pulsed stress in CMOS inverters in 1987 [39]. Their data suggested that (i) trap and/or interface state generation was dominant rather than trap filling, and (ii) trap generation was enhanced by pulsed stress.

Various studies on the effects of AC stress on device performance have made use of the two carrier model of S. K. Lai [6] to explain AC degradation phenomena.

In 1988 Weber studied AC stressing using separate pulses applied to the drain and gate [40]. He proposed a qualitative model of AC hot carrier degradation which emphasized the important part that holes had in the final formation of interface states. His model incorporated the two carrier model of S. K. Lai [6], i.e. postulating that injected electrons could be captured by injected trapped holes, resulting in the formation of interface states. Furthermore, Weber proposed that with increasing damage, the number of hole traps increased and the hole energy barrier decreased, so that the hole injection efficiency was further increased.

In 1987 Choi et al. reported the effects of AC gate and drain voltage transients on hot carrier induced NMOS degradation [41]. They concluded that, while AC drain stress voltage transients had little effect on the degradation rate, AC gate voltage transients increased the degradation

rate. They further suggested that this finding could be attributed to enhanced surface state generation as may occur in the two carrier model [6]. Doyle et al. reported dynamic NMOS stress data and suggested that both types of charge species were needed in the oxide for enhanced surface state generation [36], again in support of the two carrier model [6].

In 1984 Hofmann et al. carried out n-channel AC stress hot carrier experiments [42]. They also proposed a degradation mechanism in accord with the two carrier model [6], and correlated the observed enhanced degradation under pulsed stress to the presence of fast hole traps close to the interface. For the static case, these traps were postulated to be positively charged, causing the effective carrier injection to be screened by the field near the drain. However, in the pulsed case, these traps emptied in the time between pulses such that there was a certain time elapse before they were filled again. Consequently, under these conditions there was a period of increased effective carrier injection, causing increased degradation.

Igura and Takeda reported on the hot carrier effect from dynamic stressing using different n- and p-channel device structures [43]. They postulated that the initial electric field distribution at the instant of every AC pulse would differ from that of the DC stress, depending upon the

amount of electron detrapping, i.e. the trap lifetimes. Data showed that for certain n-channel device structures, the field could become larger, causing more damage than the active duty cycle would have indicated. The majority of p-channel data showed that AC degradation was qualitatively the same as that under DC stress.

2.4 CHARGE PUMPING

Hot carrier-assisted interface state generation has been shown to be one of the primary consequences for DC and AC stress in both n- and p-channel devices [14]. It has been pointed out that the charge pumping technique can provide an improved evaluation of the damaged interface. Specifically, the technique can monitor interface state generation free of the various masking effects due to trapped charge [14,44]. Hence, a survey of literature on charge pumping is due.

The charge pumping experiment was first initiated by Brugler and Jespers in 1969 [45]. The experiment consists of applying a pulse train to the gate and a small reverse bias to the source and drain, while the DC substrate current is recorded. Since mobile channel carriers are swept to the source and drain, the substrate current consists of the carriers that are detrapped from the surface states. Thus, the substrate or charge

pumping current can provide useful surface state information.

In 1976 A. Elliot used charge pumping currents to measure surface state densities [46]. He used this technique as a means of separating the contributions made by fast surface states and fixed oxide charges to threshold voltage shift. He noted the importance of surface state time constants. For example, he pointed out that while most measurements were carried out under steady state conditions, devices in actual circuit applications might be operating at speeds faster than the response time of some of the surface states. Consequently, transistors could have some high frequency characteristics that differed from those under steady state conditions.

In 1984 Groeseneken et al. carried out charge pumping measurements to determine the Si-SiO2 interface state density on MOS transistors [47]. They presented a model for charge pumping current, based on the emission of electrons and holes to the conduction and valence bands respectively, under both equilibrium and non-equilibrium conditions. The model also analyzed the surface band bending under transient gate biasing and the concomitant trapping and detrapping of electrons and holes.

In 1987 Tseng modified the standard charge pumping technique used for interface state density measurements [48]. His work was motivated by

the fact that interface states can act as either traps or recombination centers depending on the characteristics of the applied gate waveform. By tailoring the gate voltage pulses in time and analyzing the surface band bending with respect to the Fermi level, he was able to separate the states which behaved as traps from those which acted as recombination centers.

In 1986 Heremans et al. used the charge pumping technique in examining NMOS degradation [49]. They concluded that the two carrier model [6] is indeed valid for fast interface states. More recently, they pointed out that device parameter shifts partially reveal the physical damage at the interface, and that a more precise evaluation of interface degradation can only be made using charge pumping data in conjunction with parameter shift data [14].

Thus, much work has been done to contribute toward a better understanding of the hot carrier phenomenon and its effect upon device degradation. Yet the complexity of the problem leaves many areas open to further investigation and some questions still unanswered.

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CHAPTER 3

DESCRIPTION OF EXPERIMENT

3.1 Experiment

The experimental objectives were to test the two premises upon which previous AC simulation work had been based: 1) AC and DC parameter measurement equivalence, and 2) AC and DC stress equivalence for small time increments (quasi-static assumption).

Single n- and p-channel MOSFETs were fabricated at Intel and packaged for examination. Although the single transistor configuration may not occur in actual circuit applications, it is important to understand the physics of stress, based on the single transistor operation. Stress was applied to devices under both AC and DC conditions. Device stress, as used in this experiment, is the simultaneous application of an increased source-drain voltage and a worst case gate voltage in the saturation region. The worst case gate voltage was the gate bias at which the maximum substrate current for n-channel and the maximum gate current for p-channel devices are induced. It is under these high electric field conditions that carriers in the channel become 'hot', i.e. gain enough energy before an

energy stripping collision to cause device degradation.

3.2 AC vs. DC Measurement

Data was collected using 20 packaged p-channel and 10 n-channel one micron technology MOSFETs. The same testing sequence, DC measurement, AC measurement and charge pumping, was followed before and after DC stress. The electrical parameters of the transistor under test were measured under low noise DC conditions according to the scheme shown in Fig. 1.

The application of DC stress biases and measurement of electrical parameters were performed by the use of an Intel Vax-controlled computer program in conjunction with a HP 4145 semiconductor parameter analyzer and a HP 10658A test box. This DC characterization consisted of measuring quantities such as drain saturation current, Idsat, threshold voltage, Vt, transconductance, Gm and subthreshold swing, S.

The value of Idsat was also measured under low and high frequency low distortion AC conditions following the setup described in Fig. 2. A packaged transistor was enclosed in a Faraday shielded box, while a HP 8116A pulse generator pulsed the gate and a HP 6622A DC power supply biased the drain. The source was connected to a 50 ohm Tektronix Digital

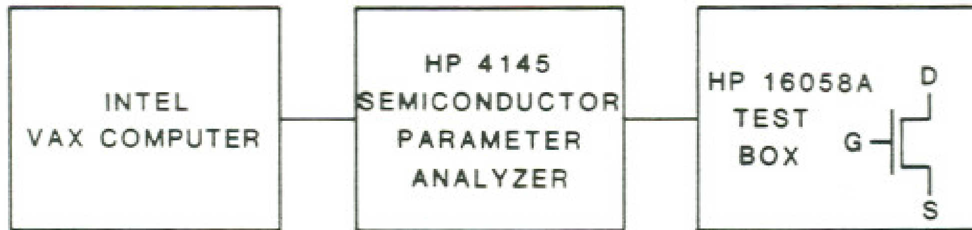

Figure 1: **Block diagram for DC characterization and DC stressing.**

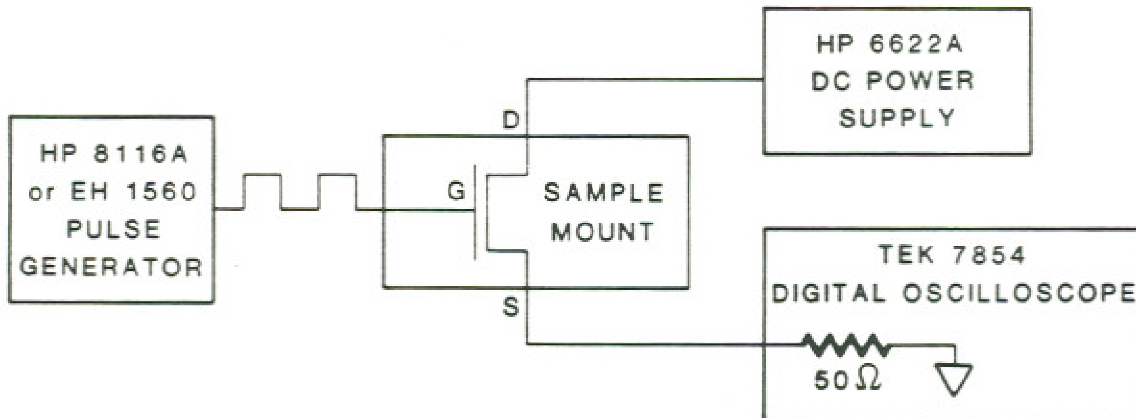

Figure 2: Block diagram for AC characterization.

oscilloscope termination. Comparisons of AC and DC measurement were carried out based on AC and DC Idsat values. The parameter of Idsat was selected primarily because of its direct measurability under AC conditions. Idsat values were computed by recording transistor output voltages divided by the 50 ohm oscilloscope termination. This output resistance value was small enough to insure that saturation drain current would be measured and that the resistor voltage drop would be a negligible percentage of the bias voltage.

Additionally, charge pumping experiments were carried out both before and after DC stress. The experiment involves the application of a train of voltage pulses to the gate, while a small DC reverse bias is applied to both the source and drain and the DC substrate current is recorded. As shown in Fig. 3, this was performed by means of an Intel 301 PC-controlled computer program, a HP 8116A pulse generator, a HP 16055A test box and a HP 4140B picoammeter. As the gate is pulsed, the channel is cycled between inversion and accumulation, causing a repetitious charging and discharging of the Si-SiO2 interface states. Under this condition, the trapped minority carriers recombine with substrate majority carriers during accumulation, and result in recombination current, i.e. charge pumping current, Icp [1].

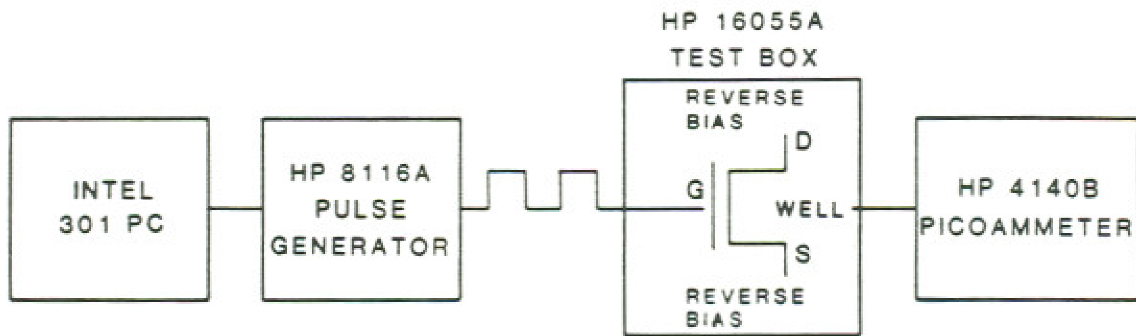

Figure 3: Block diagram for charge pumping.

This experiment is based upon the following assumptions. First, that mobile minority carriers induced in the channel drift back to the source and drain, and do not contribute to the charge pumping current. Second, that channel inversion time is sufficiently long for carriers to be trapped at the interface. Third, that pulse switching time is long enough to allow mobile inversion minority carriers to drift back to the source and drain. Additionally, the application of square gate pulses with fixed rise and fall times, made possible the assumption that there was a constant amount of emitted charge per cycle, and consequently, the same recombining charge, Qss per cycle [1-4].

$$\mathrm{Icp} = \frac{\mathrm{Qss}}{\mathrm{second}} \tag{1}$$

$$\mathrm{Icp} = \mathrm{Qss} \cdot \mathrm{frequency} \tag{2}$$

The increase in charge pumping current, if any, can be considered to be a monitor of interface trap density. The measurements can thus be used to evaluate hot carrier degradation in terms of interface damage and/or interface state generation [1].

3.3 AC vs. DC Stress

Data was collected from 30 p-channel and 20 n-channel submicron technology devices from the same run using the scheme shown in Fig. 4. DC electrical parameter measurements were made on devices before and after high frequency low distortion AC stress. AC stress time was assumed to correspond to the pulse active duty cycle time.

Comparisons were made for three groups of bias conditions, differing in whether the applied voltage was AC or DC. These included (a) DC drain with DC gate bias, (b) AC drain with DC gate bias and (c) AC gate with DC drain bias. The transistors which were compared were from the same process run and device structure. An additional precaution was made by selecting devices with essentially the same substrate current for each of the above three stress conditions. The substrate current was measured at fixed bias conditions before any applied stress. These measurement conditions consisted of a fixed drain voltage under worst case bias conditions, i.e. Vd=7.0V and Vg =2.0V for n-channel and Vd=-5.5V and Vg=-1.0V for p-channel devices. This method of categorization compensated for any discrepancies in effective channel length and bias that might be present. In this way, any differences in transistor degradation could be attributed to differences in the three stress cases, (a),(b) and (c).

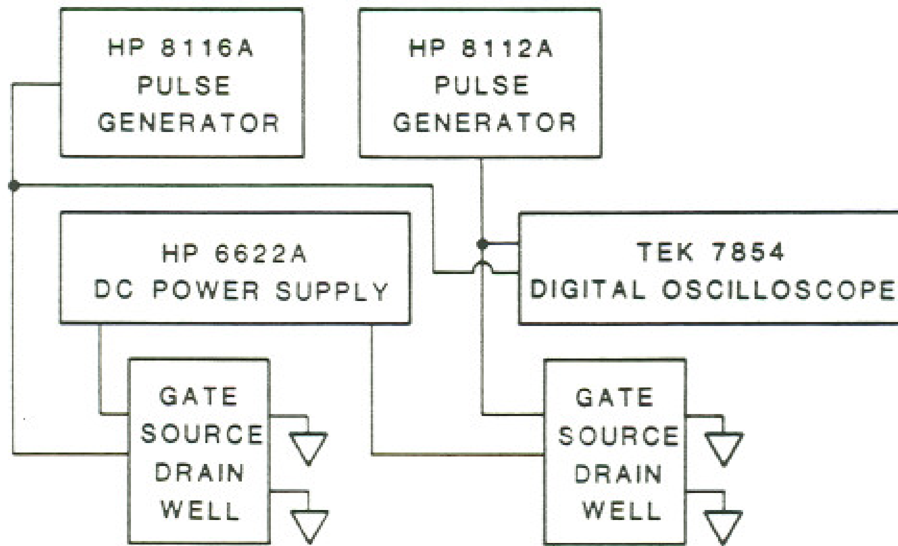

Figure 4: Block diagram for AC stressing.

The details of the test conditions have been relegated to the appendix.

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CHAPTER 4

RESULTS

This chapter summarizes the experimental results obtained during the course of this thesis. As mentioned in the previous chapter, the experiments were designed (i) to compare AC and DC measurements of MOSFET parameters before and after DC stress and, (ii) to compare AC and DC stress in terms of DC measurements of MOSFET parameters before and after stress.

A brief look at MOSFET operation is needed at this point for a clearer presentation of these results. The MOSFET is a three terminal device, in which source-drain current is controlled by the gate voltage. Since the gate terminal is insulated from the channel by a high impedance dielectric material, it draws virtually no current. Hence, by changing the gate bias, the conducting channel between the source and drain turns off and on [1]. Three types of charge states are induced under the gate as a result of the change in gate bias. These include (i) the 'accumulation' of majority carriers, (ii) the 'depletion' of majority carriers, and (iii) the induction of minority carriers. The device turns on when the gate voltage exceeds the threshold voltage, Vt the minimum gate voltage required to

invert the surface and induce the conducting channel.

It is important to define threshold voltage measurement, since it can be measured in different ways. Threshold voltage as defined in this experiment, was the gate voltage at which 10 μA of drain current were measured for a fixed aspect ratio under a fixed drain voltage of $\pm$ 0.1V. The aspect ratio was 50 for the n-channel devices and 60 for the p-channel devices.

When a gate voltage, Vg larger than Vt is applied, the drain bias, Vd produces a a resistor-type operation. In this triode region, the drain current, Id depends on both the gate and drain voltages, the oxide capacitance (Cox), mobility (μ) and channel length (L) as [2]:

$$\mathrm{Id} = \mathrm{K} \cdot \left[(\mathrm{Vg} - \mathrm{Vt}) \cdot \mathrm{Vd} - \frac{\mathrm{Vd}^2}{2} \right] \tag{3.1}$$

$$\mathrm{K} = \frac{\mu \cdot \mathrm{Cox}}{\mathrm{L}} \tag{3.2}$$

As Vd is increased, the channel pinches off and the voltage across the channel remains fixed. In this saturation region, the drain current is controlled by the gate voltage and becomes almost independent of the drain voltage [2]:

$$\mathrm{Idsat} = \frac{\mathrm{K}}{2} \cdot (\mathrm{Vg} - \mathrm{Vt})^2 \tag{4}$$

The transconductance is defined as $Gm = \Delta Id/\Delta Vg$,Vd = constant and is an important parameter affecting the small signal amplification. It is given in the linear and saturation regions respectively as [1],

$$Gm = K \cdot Vd \tag{5.1}$$

$$Gm = K \cdot (Vg - Vt) \tag{5.2}$$

For gate voltages less than Vt, no channel is formed, so that there is only a very low subthreshold drain current. The subthreshold swing, S is a measure of the MOSFET's turn-off characteristic. Specifically, the subthreshold swing is the gate voltage swing needed to reduce the subthreshold drain current by one decade [3]:

$$S = \frac{\Delta Vg}{\Delta Log_{10}(Id)} \tag{6}$$

4.1 DC Measurement

Figure 5 summarizes the typical characteristics of a n-channel transistor, i.e. Id as a function of drain voltage (A), Id, Vt and peak Gm as a function of gate voltage (B) and S as a function of stress time (C). The parameters under study, Idsat, Gm, Vt and S were measured under DC conditions before and after DC stress. Notice that Idsat and Gm are the most sensitive monitors of stress induced degradation. The effect of DC

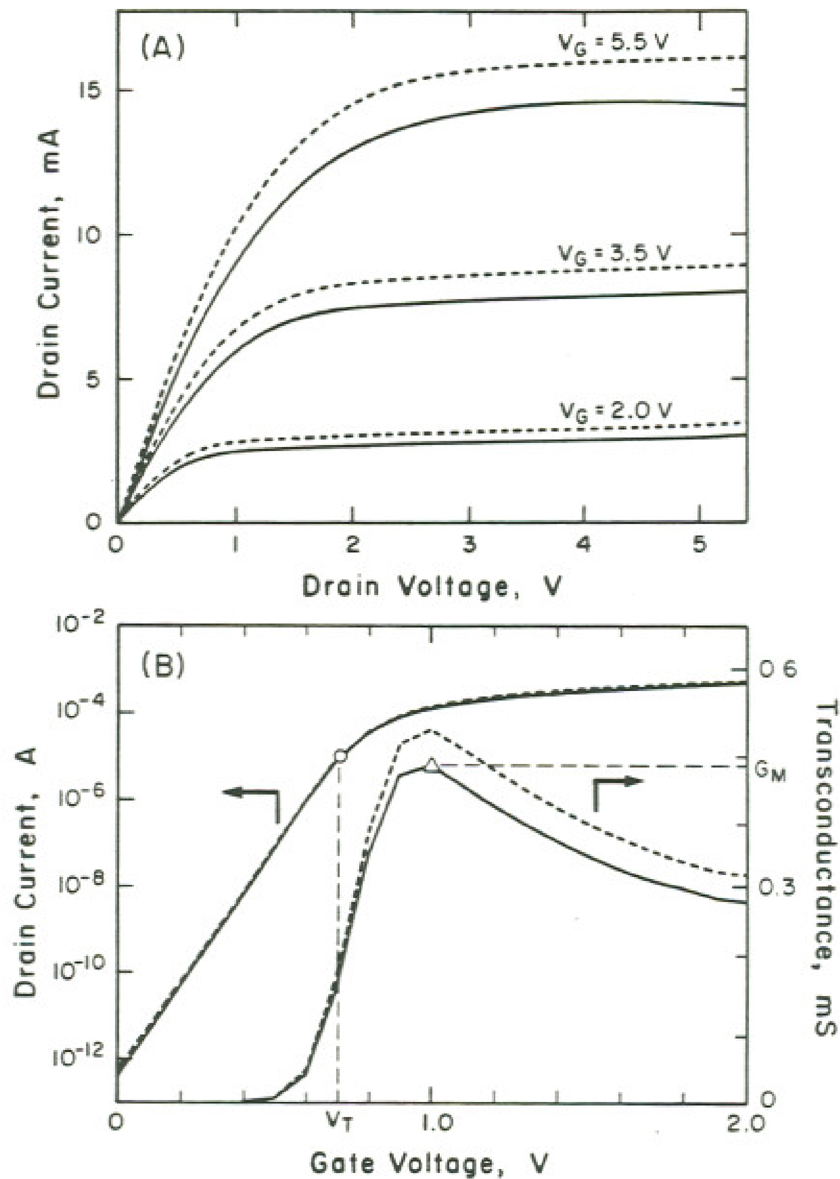
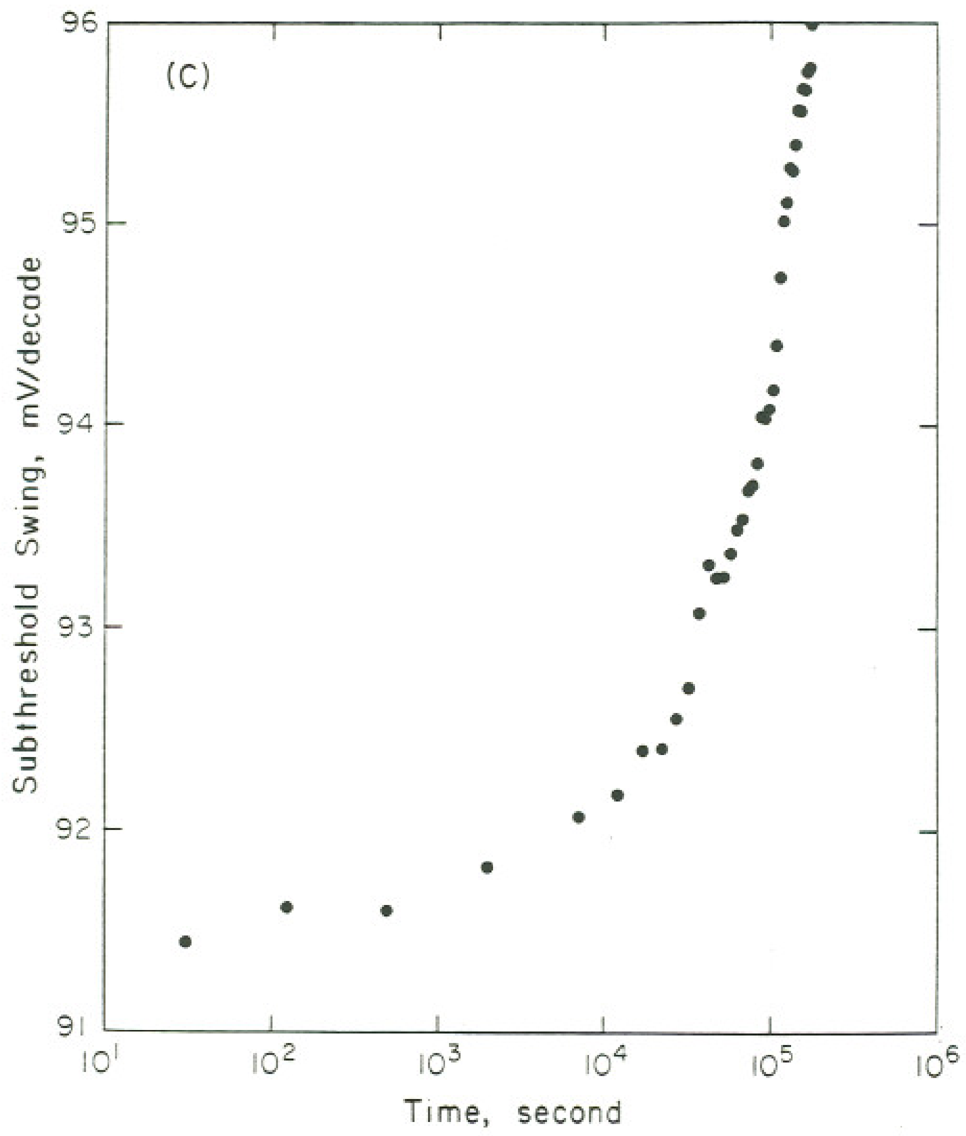


Figure 5: N-channel transistor I-V curves (A), subthreshold characteristics and transconductance (B), before (---) and after (—) DC stress, and subthreshold swing vs. stress time (C). Stress conditions for (A) and (B) were Vd=7.0V, Vg=2.5V for 3 days. Stress conditions for (C) were Vd=7.0V, Vg=2.5V. Measurements were made with the source/drain terminals interchanged from that of the applied stress (reverse).


(C)
Subthreshold Swing, mV/decade
96
95
94
93
92
91
10^1
10^2
10^3
10^4
10^5
10^6
Time, second

stress for the n-channel is manifested in:

i) a decrease in Idsat, i.e. by 11%

ii) a decrease in Gm, i.e. by 10%

iii) an increase in Vt, i.e. by 1%

iv) an increase in S, i.e. by 5%

These measured values of stress induced shifts are consistent with those reported in literature [4-7]. From these data one can conclude that (i) a degradation in mobility, (ii) an increase in series resistance, (iii) reduced surface mobile charge density via interface state generation or (iv) the combination thereof have occurred following DC stress. Note that the rise in S as a function of stress time is distinctly bimodal.

Figure 6 shows the corresponding p-channel data measured under DC conditions before and after DC stress. It is interesting to note that for the case of p-channel, most of the direction of stress induced parameter shift is in marked contrast with the n-channel case. Again Idsat and Gm are the most sensitive monitors of degradation. The effect of DC stress is manifested in:

i) an increase in Idsat, i.e. by 30%

ii) an increase in Gm, i.e. by 14%

iii) a decrease in | Vt |, i.e. by 10%

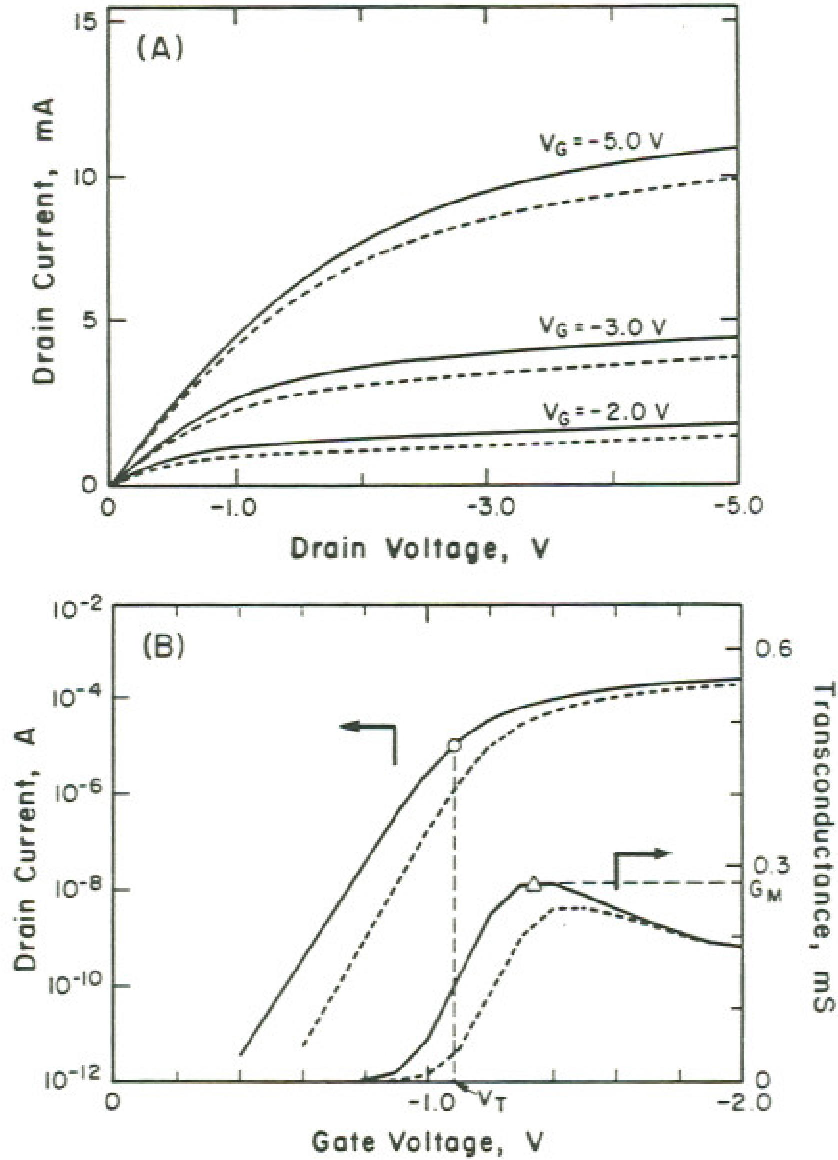
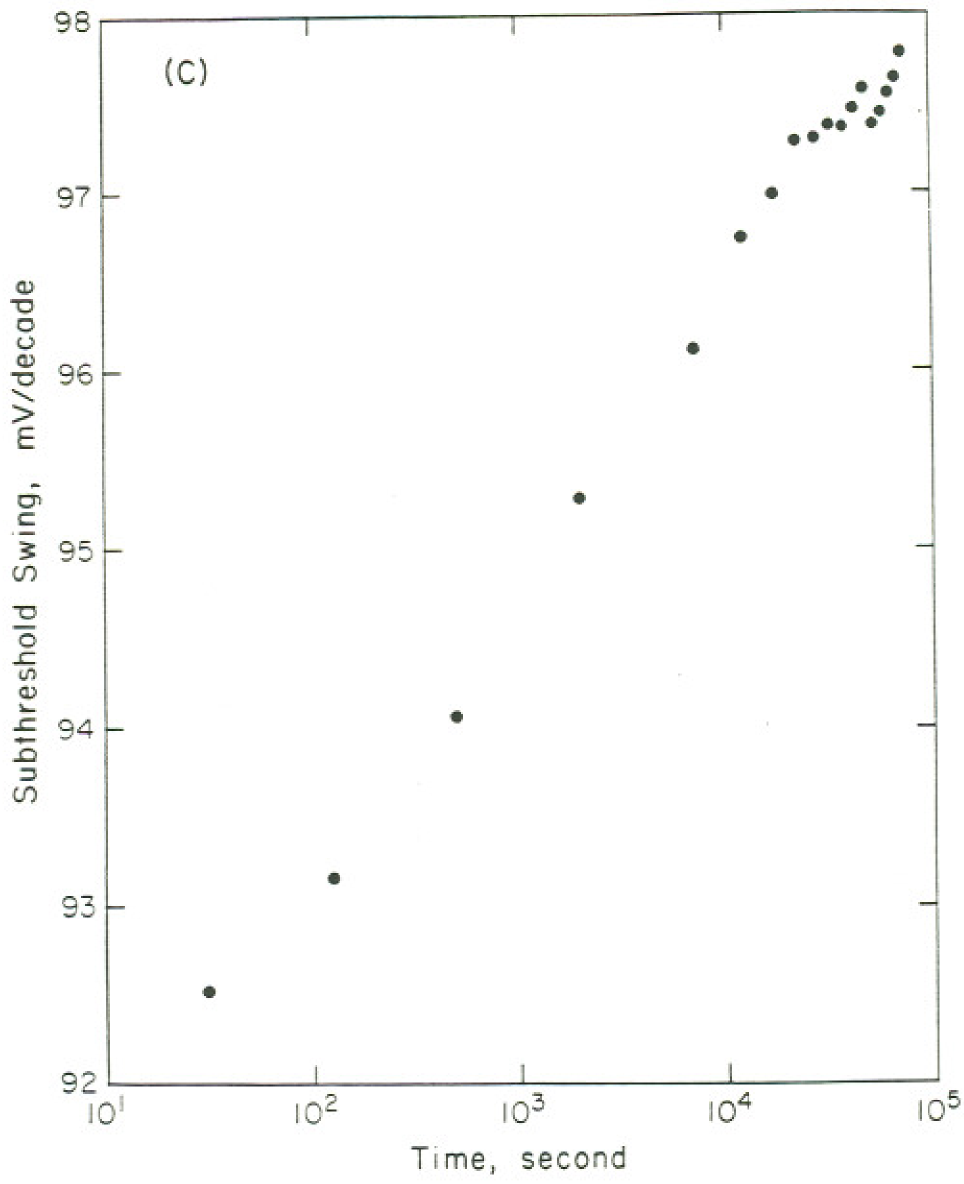


Figure 6: P-channel transistor I-V curves (A), subthreshold characteristics and transconductance (B), before (---) and after (—) DC stress, and subthreshold swing vs. stress time (C). Stress conditions for (A) and (B) were Vd=-8.0V, Vg=-1.7V for 6 hrs. Stress conditions for (C) were Vd=-9.0V, Vg=-1.7V.


(C)
Subthreshold Swing, mV/decade
98
97
96
95
94
93
92
10^1
10^2
10^3
10^4
10^5
Time, second

iv) an increase in S, i.e. by 11%

These measured parameter shifts again are consistent with the values reported in the literature [7-10]. A striking feature of p-channel degradation is the apparent channel shortening, as may be seen from Eqs. (3.1)-(5.2). Note that S as a function of stress time is unimodal in contrast with the n-channel case.

The degree of change in device characteristics measured under DC conditions is quite sensitive to the polarity of measurement with respect to the applied stress. Figure 7 presents a n-channel example of this effect. Parameters were measured with the same source/drain configuration as that of the applied stress (forward), and with the source and drain terminals interchanged (reverse). As observed in this figure, Idsat as measured in the reverse direction, decreased by 19%, while Idsat as measured in the forward direction decreased by about 3%.

This larger parameter shift measured with the source and drain terminals interchanged has been noted in literature [11]. As mentioned in chapter 2, this can be qualitatively understood as follows. A trapped charge affects the device performance more directly when it is not hidden by the depletion region, and is close to the injecting terminal where the potential energy barrier lowering is more significant [12,13].

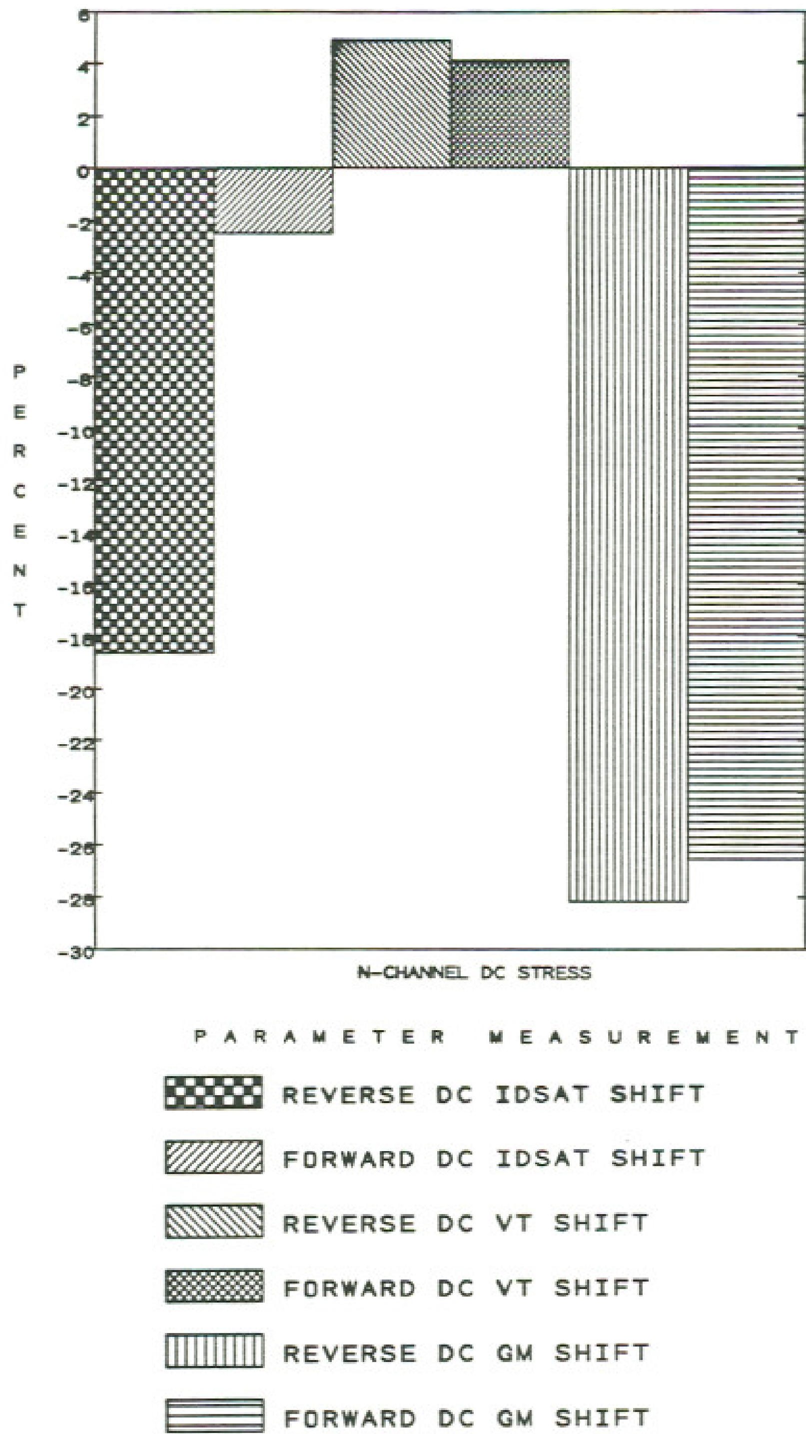


Figure 7: Forward and reverse measurement of n-channel parameter shifts after DC stress. Stress conditions were Vd=7.0V, Vg=2.5V for 2 days.

4.2 AC Measurement

Figures 8 and 9 present the AC data, measured from the same devices whose DC data have been discussed in Figs. 5 and 6. Figures 8 (A),(B),(C) and (D) display the n-channel pre- and post-stress AC voltage waveforms measured at a frequency of 10 kHz. Each oscilloscope trace exhibits the input voltage waveform (upper signal) and the output voltage waveform (lower signal). Figures 8 (A) and (B) show the rising edge of both the input and output waveforms before and after DC stress. Figures 8 (C) and (D) show the corresponding falling edge. Circuit parasitics restricted measurement resolution to 20 ns, i.e. the time to reach steady state following overshoot. Note that the effect of stress manifests itself in the difference in the steady state output voltages, as can be clearly observed from these figures. Parasitic induced waveform overshoot and ringing is essentially the same before and after DC stress. Specifically, this n-channel device showed a 11% decrease in steady state output voltage. This explicitly indicates that Idsat is decreased by 11%, in agreement with the DC data discussed earlier. Impact ionization induced breakdown limited the upper range of stress voltages to 7.5V. Hence, stress voltages were applied for longer periods of time and measurements were taken with the source and drain terminals interchanged in order to enhance stress induced

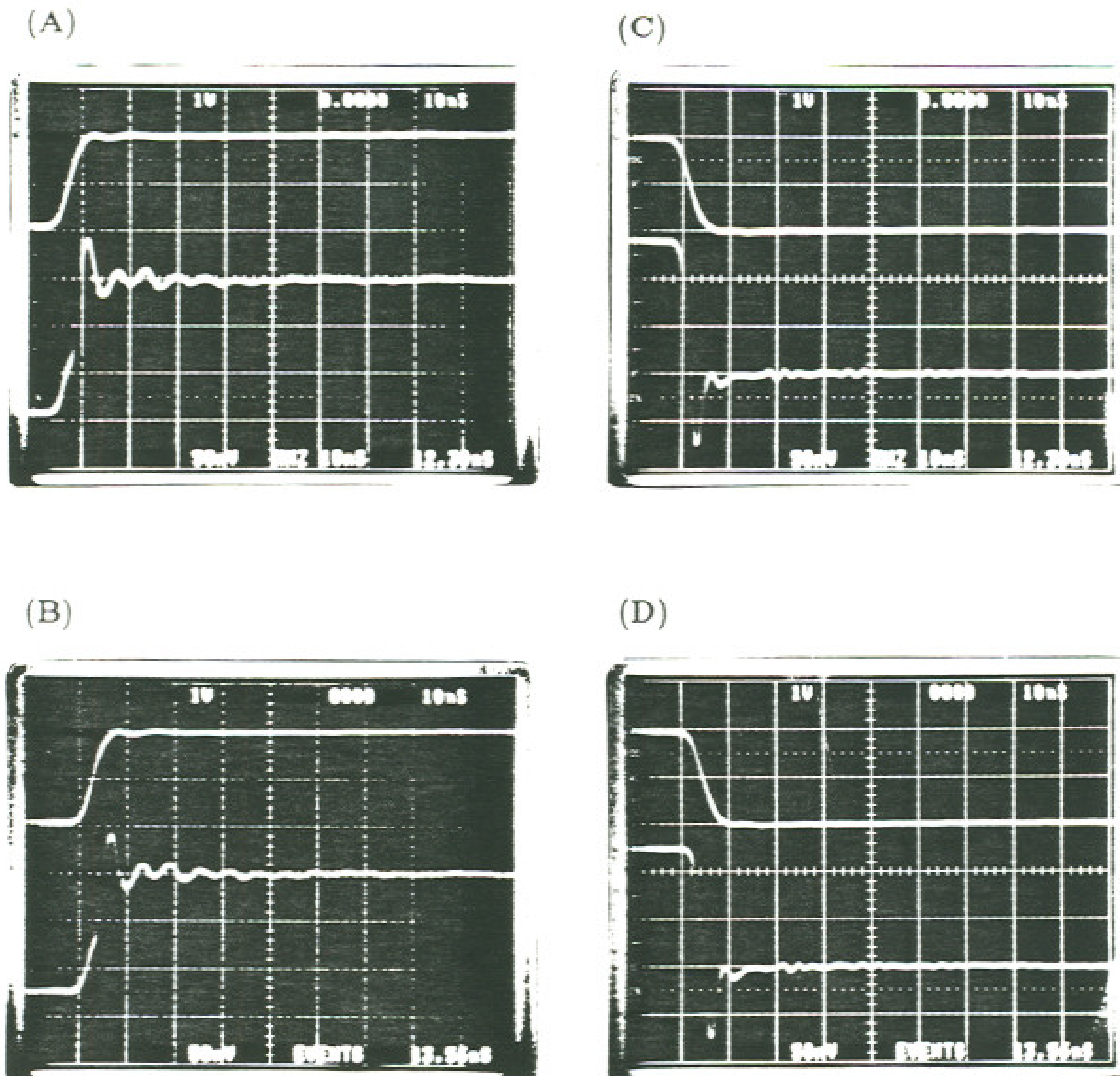


Figure 8: N-channel gate input and load output waveforms: (A),(B) the rising edge before and after DC stress, (C),(D) the respective falling edge. Stress conditions were Vd=7.0V, Vg=2.5V for 3 days. Measurements were made in the reverse direction with 50% duty cycle pulses at a frequency of 1 MHz.

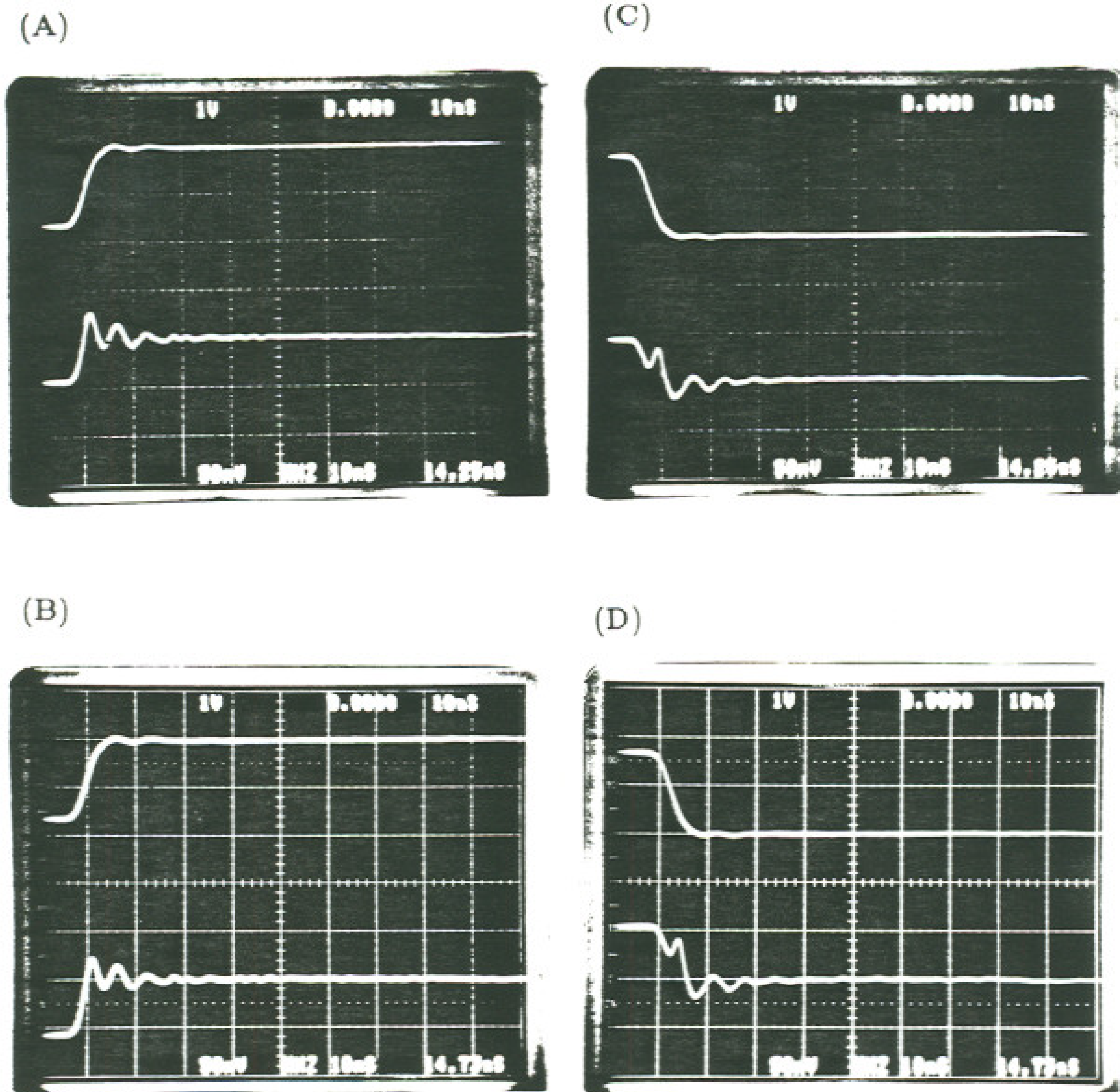


Figure 9: P-channel gate input and load output waveforms; (A),(B) the rising edge before and after DC stress, (C),(D) the respective falling edge. Stress conditions were Vd=-8.0V, Vg=-1.7V for 6 hrs. Measurements were made with 50% duty cycle pulses at a frequency of 1 MHz.

damage for examination (appendix).

Figure 9 presents the corresponding data obtained from a p-channel device using a frequency of 1 MHz. Again, the effect of stress is exhibited in the difference in the steady state output voltages. Note that the 31% output voltage level increase is in agreement with the corresponding DC data of Fig. 6. The p-channel devices were not restricted in stress voltage levels. Hence the higher bias conditions used (Vd=-8.0V, Vg=-1.7V) resulted in greater Idsat shifts.

The comparison between AC and DC measurements was further carried out by systematically varying the stress conditions, i.e. by changing the drain voltages for a fixed gate voltage. As can be observed from Figs. 10 and 11, the AC and DC measured shifts in n- and p-channel Idsat values, are in good agreement for all the drain voltages used.

The shifts in AC Idsat values in n- and p-channel devices are now plotted in Figs. 12 and 13 respectively as a function of frequency, ranging from 100 Hz to 3 MHz. Note that the 11% decrease in n-channel Idsat and 27% increase in p-channel Idsat remain approximately independent of frequency. The slight downward trend in Idsat values with increasing frequencies is due to the low pass nature of the parasitic capacitances in the circuit. This frequency independence of the parameter shift again indicates

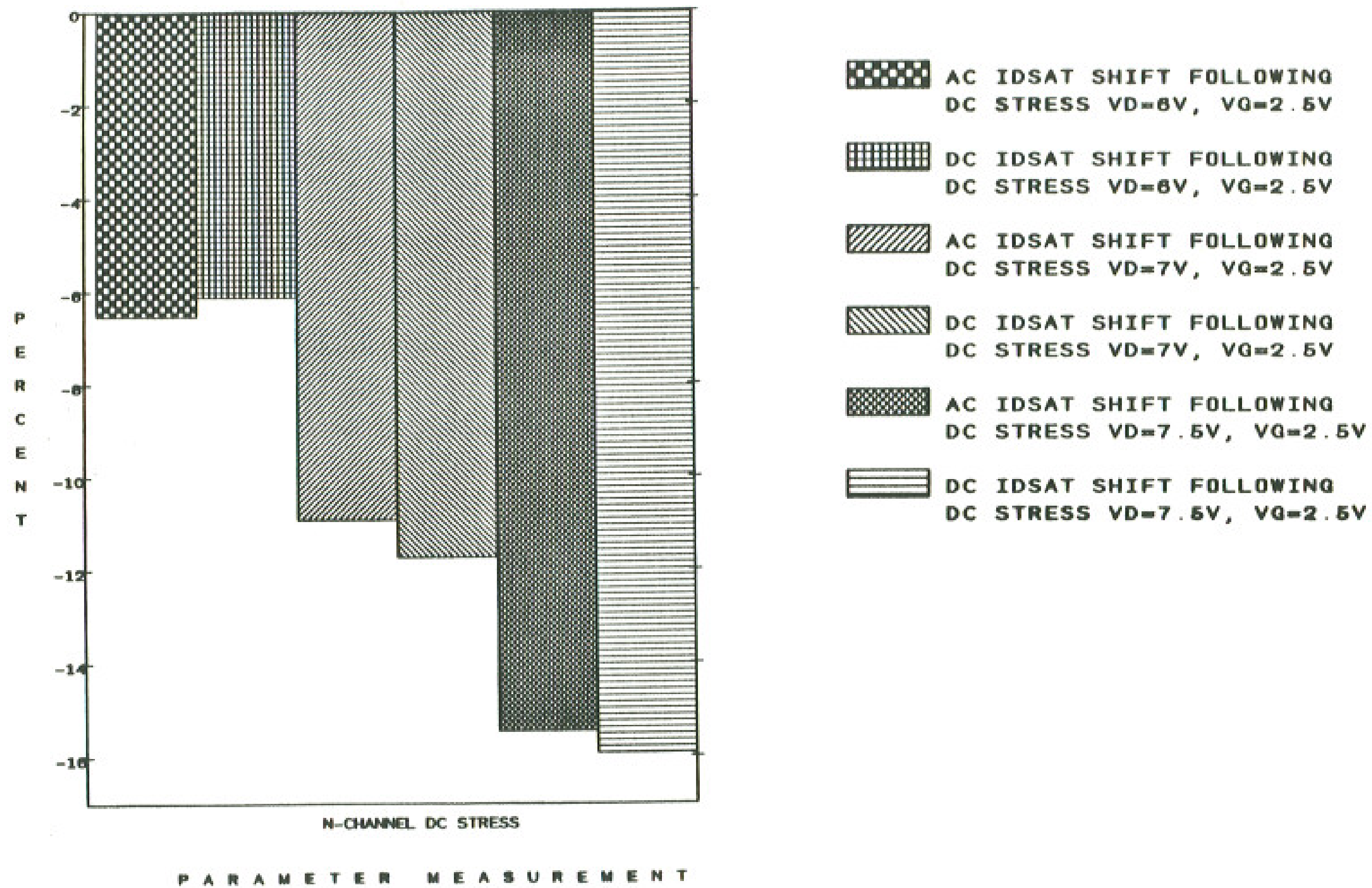


Figure 10: N-channel AC and DC Idsat shifts for different DC stress conditions. Measurements were made in the reverse direction with 50% duty cycle pulses at a frequency of 100 Hz.

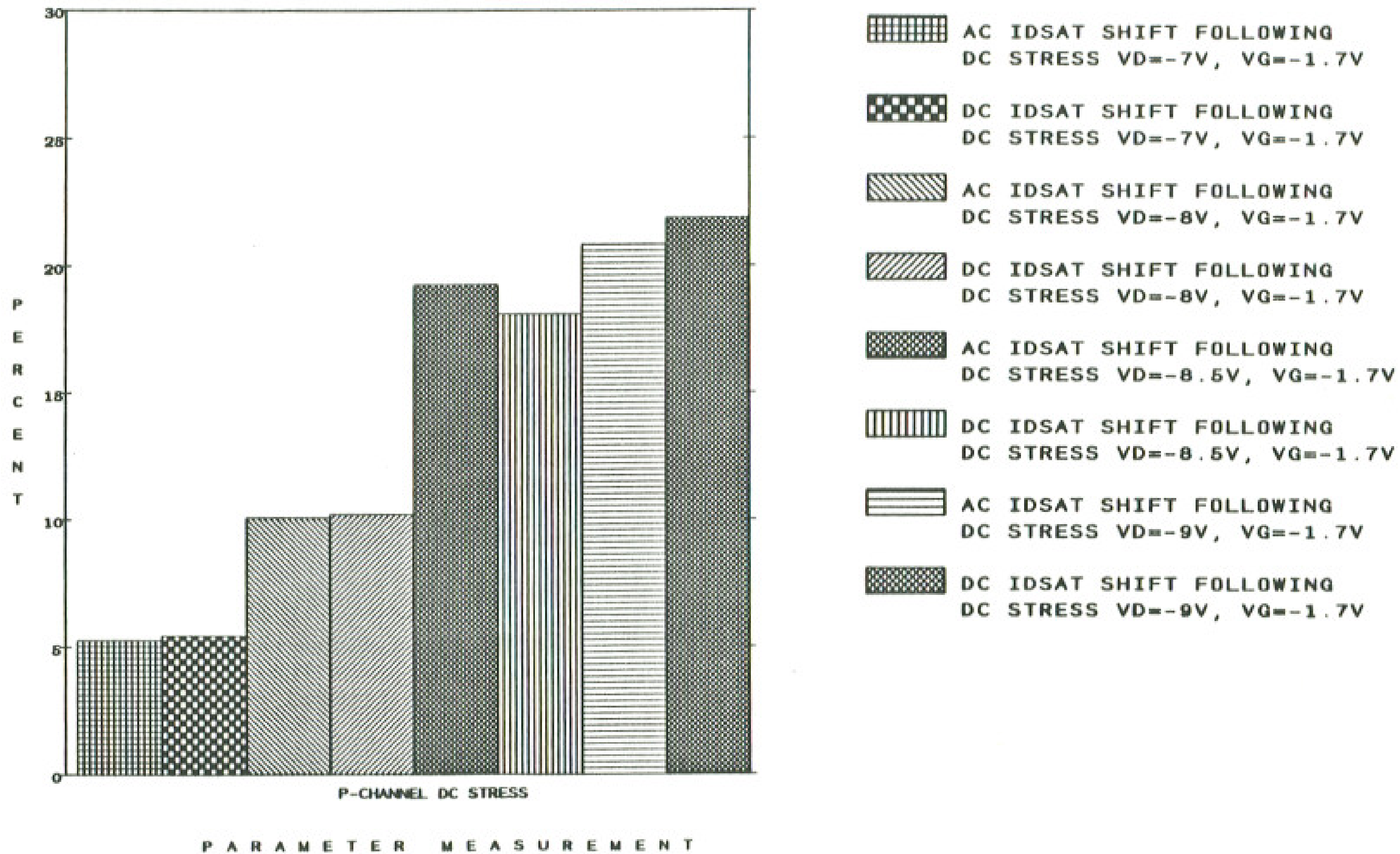


Figure 11: P-channel AC and DC Idsat shifts for different DC stress conditions. Measurements were made with 50% duty cycle pulses at a frequency of 100 Hz.

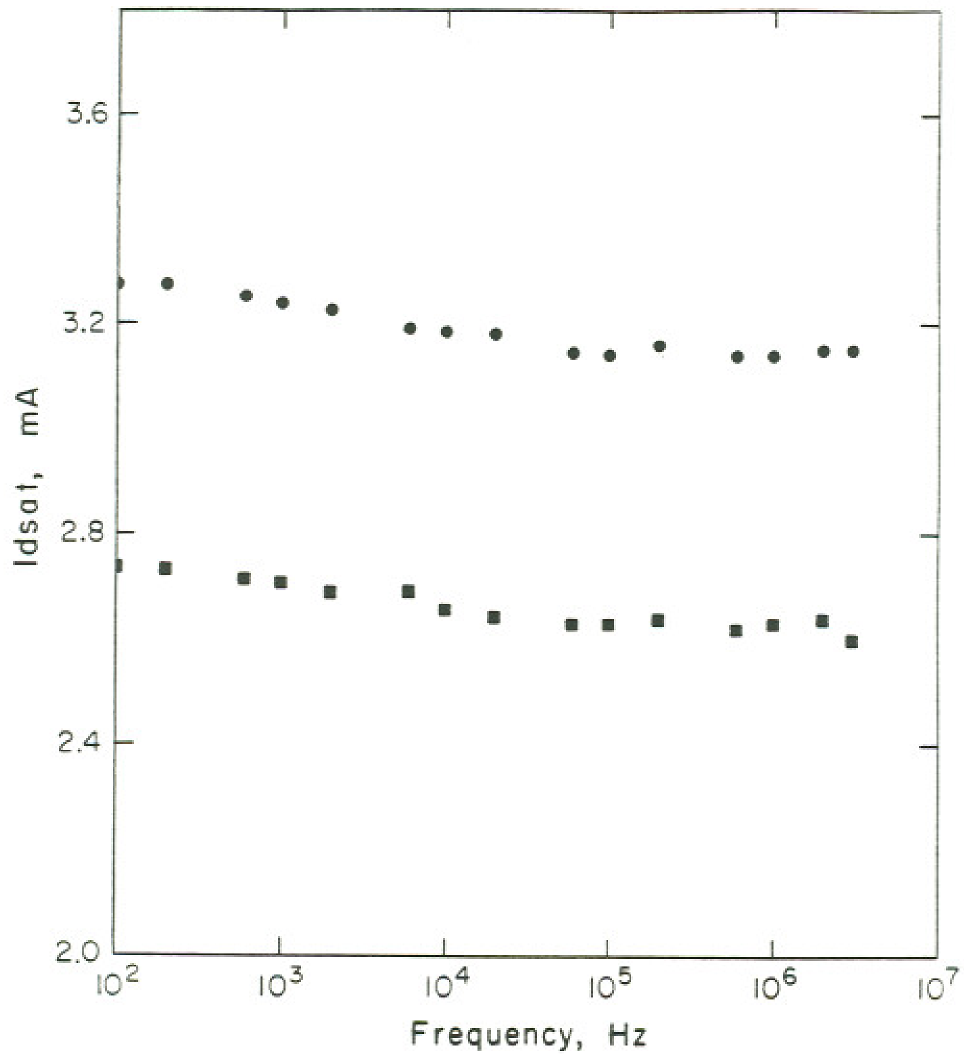


Figure 12: N-channel Idsat vs. frequency before (●) and after (■) DC stress. Stress conditions were Vd=7.5V, Vg=2.0V for 8 days. Measurements were made in the reverse direction with 50% duty cycle pulses.

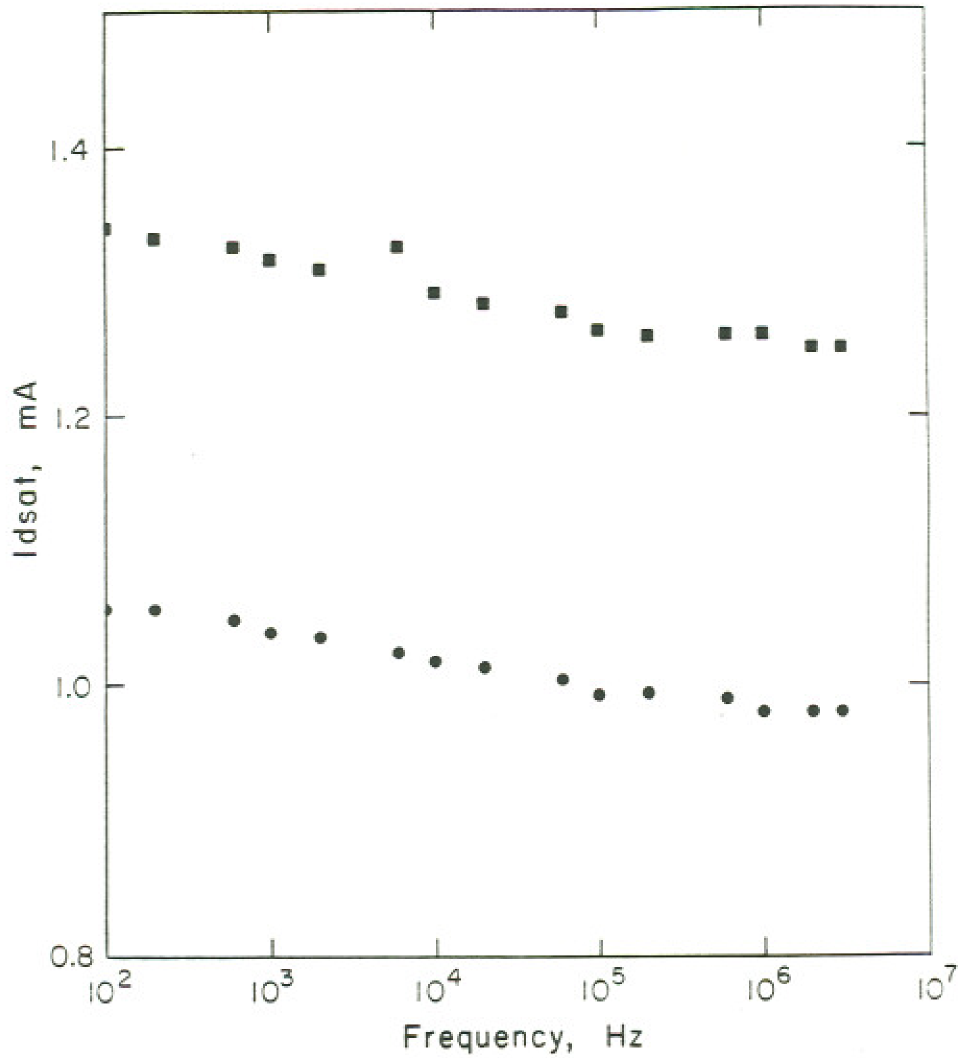


Figure 13: P-channel Idsat vs. frequency before (●) and after (■) DC stress. Stress conditions were Vd=-9.0V, Vg=-1.7V for 21 hrs.

that the characteristic time for charge trapping and/or detrapping as affects device performance is short ($<$ 300 ns). Again the higher stress voltages used with p-channel devices resulted in larger Idsat shifts.

The measurement of Idsat shifts was repeated for different gate voltage base-levels. The surface band bending and concomitant degree of carrier accumulation, trapping or detrapping for a fixed inversion, can be varied by using different gate pulse base-levels. Furthermore, the measurement was carried out at high and low frequencies. In this way, accumulative charge build-up, if any, from incomplete trap emptying in the time between gate pulses, could be observed. Figures 14 and 15 show that changing the base-levels of of the gate voltage do not significantly alter Idsat shifts for either the n- or p-channel transistors. From this one may infer that the stress induced trap level is shallow and that the trap lifetime is shorter than 20 ns. Additionally, the charge trapping or detrapping from deep levels, if any, does not play a significant role in changing Idsat levels.

It is interesting to point out that the parasitic effects associated with AC measurement depend sensitively on the gate base-level used. As can be observed from Figs. 16 and 17, the Idsat shift remains more or less constant at approximately 16% and 30% for n- and p-channel devices respec-

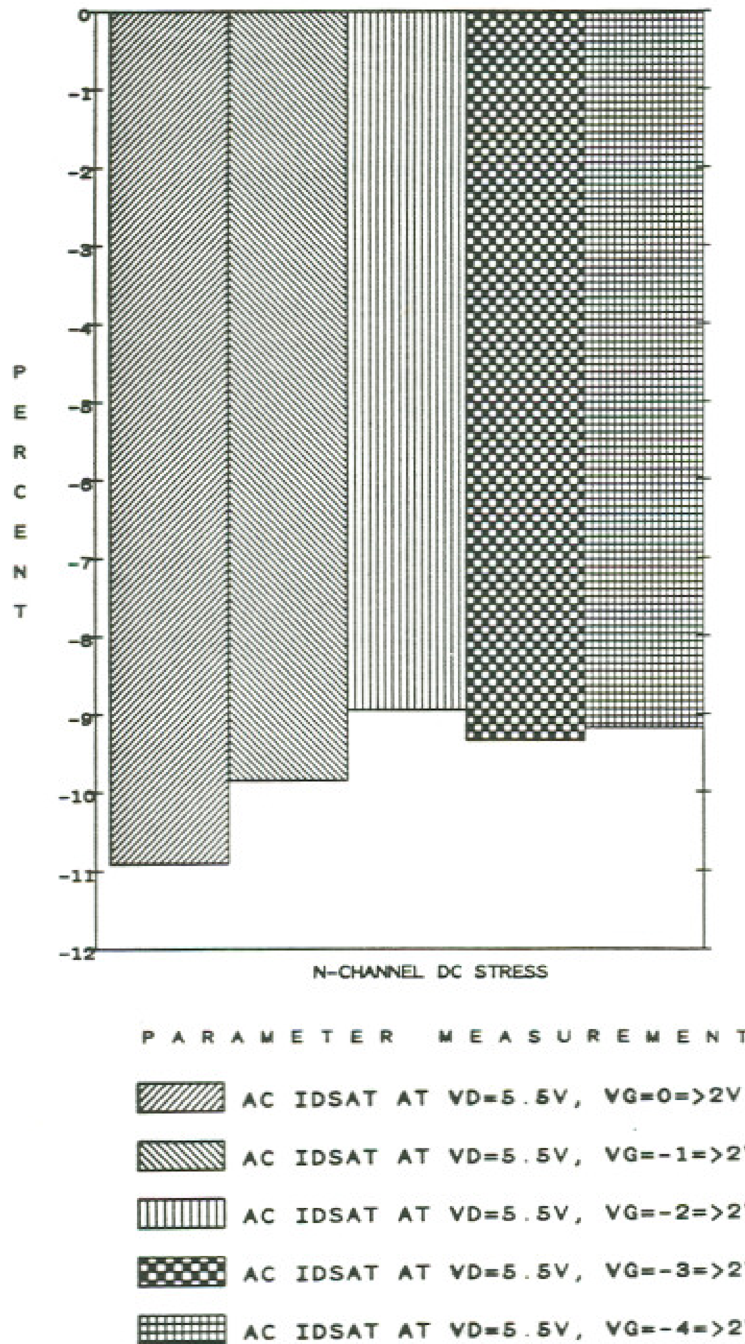


Figure 14: AC measurement of n-channel Idsat shifts for different gate base-levels after DC stress. Stress conditions were Vd=7.5V, Vg=2.5V for 3 days. Measurements were made in the reverse direction with 50% duty cycle pulses at a frequency of 100 Hz.

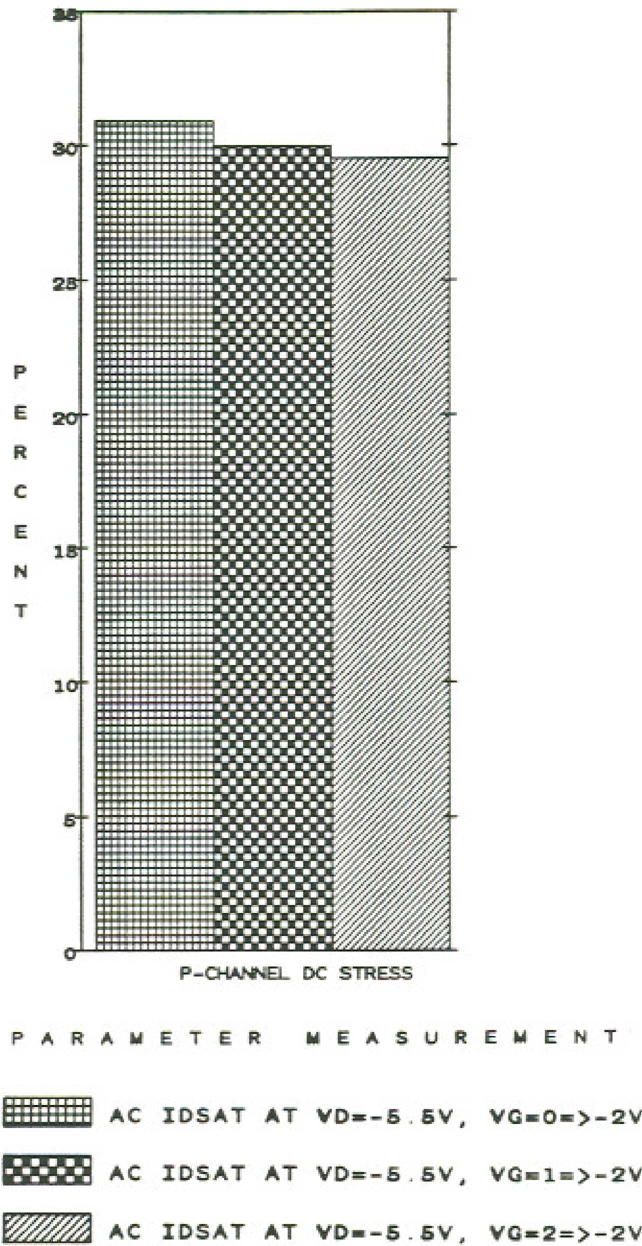


Figure 15: AC measurement of p-channel Idsat shifts for different gate base-levels after DC stress. Stress conditions were Vd=-10.0V, Vg=-1.7V for 16 hrs. Measurements were made with 50% duty cycle pulses at a frequency of 100 Hz.

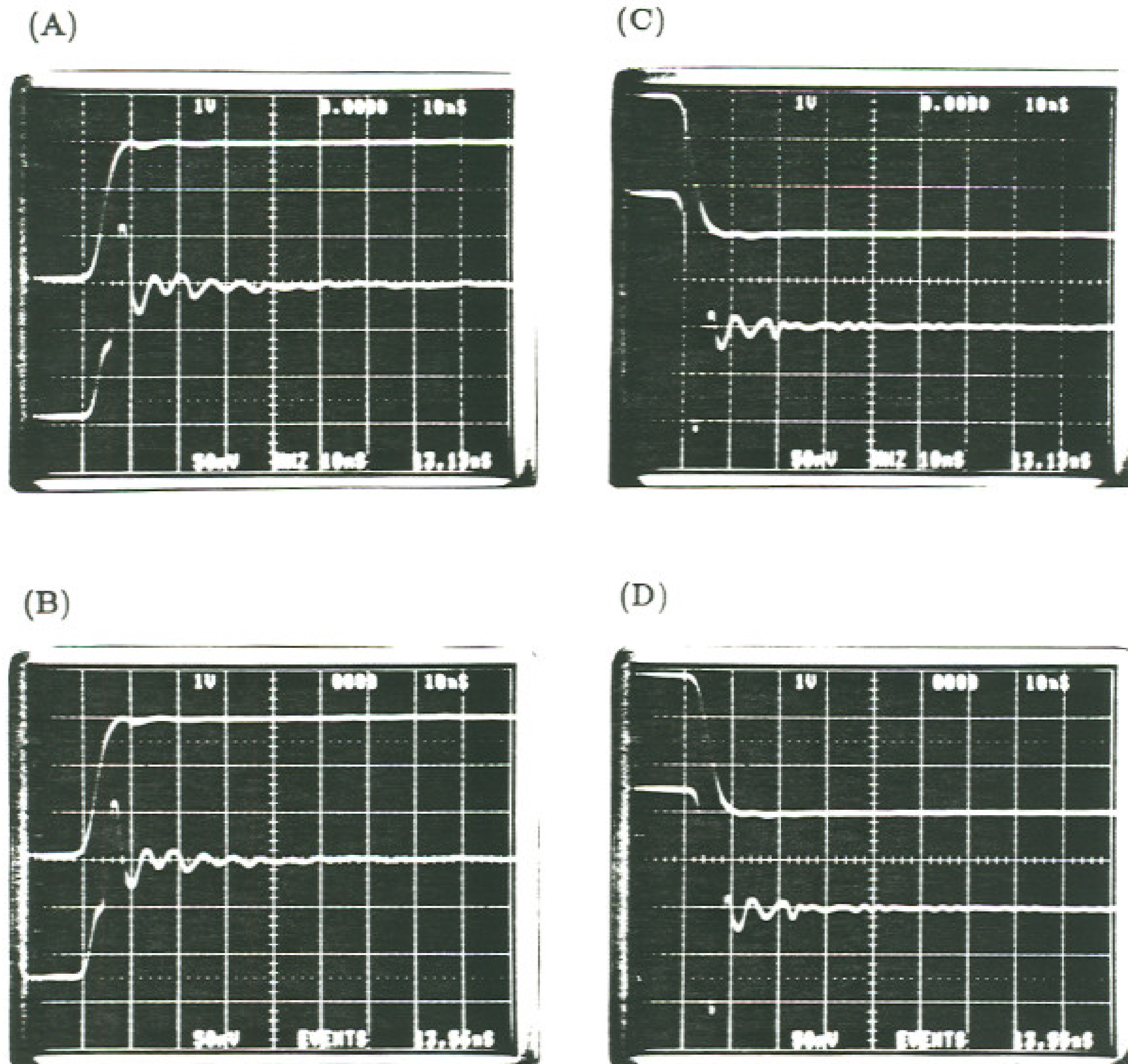
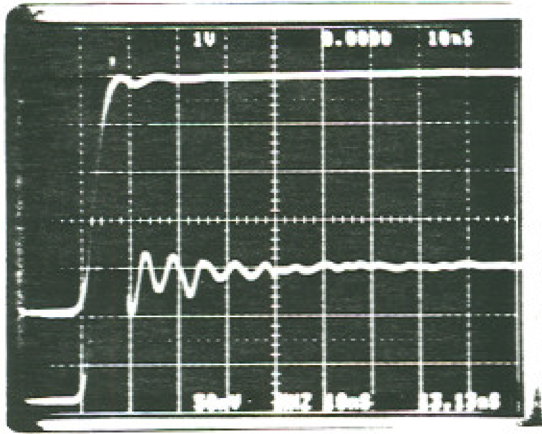
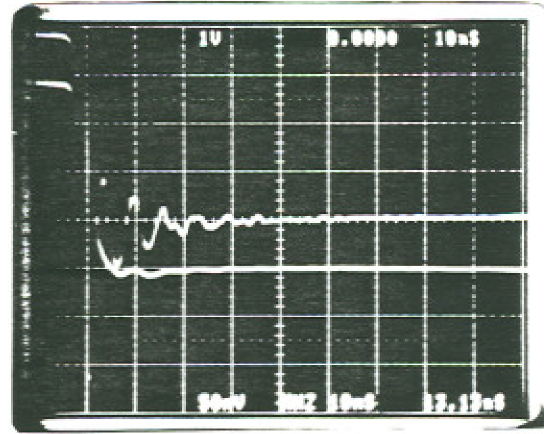


Figure 16: N-channel gate input and load output waveforms; (A),(B) the rising edge measured before and after DC stress with a gate base-level, Vg=-1=>+2V, (C),(D) the respective falling edge, (E),(F) the rising edge measured with a gate base-level, Vg=-3=>+2V, (G),(H) the respective falling edge. Stress conditions were Vd=7.0V, Vg=2.5V for 3 days. Measurements were made in the reverse direction with 50% duty cycle pulses at a frequency of 10 kHz.

(E)



(G)



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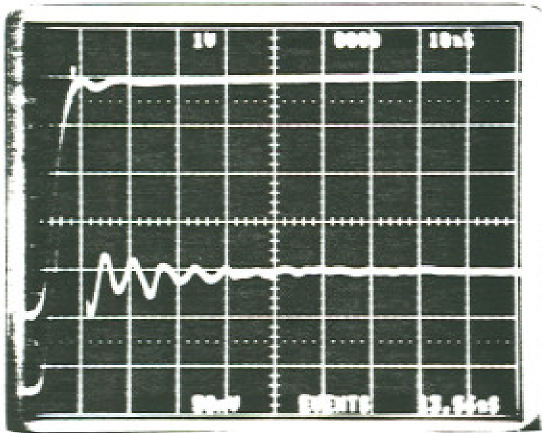

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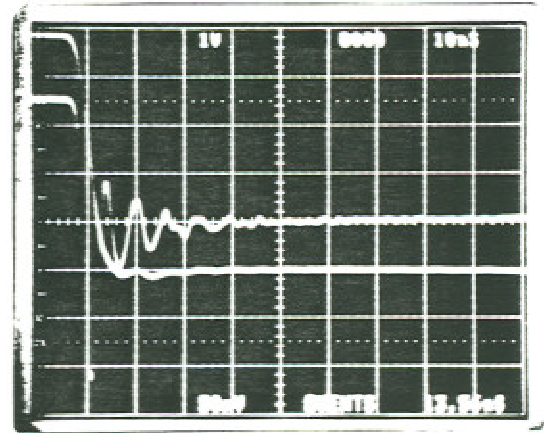


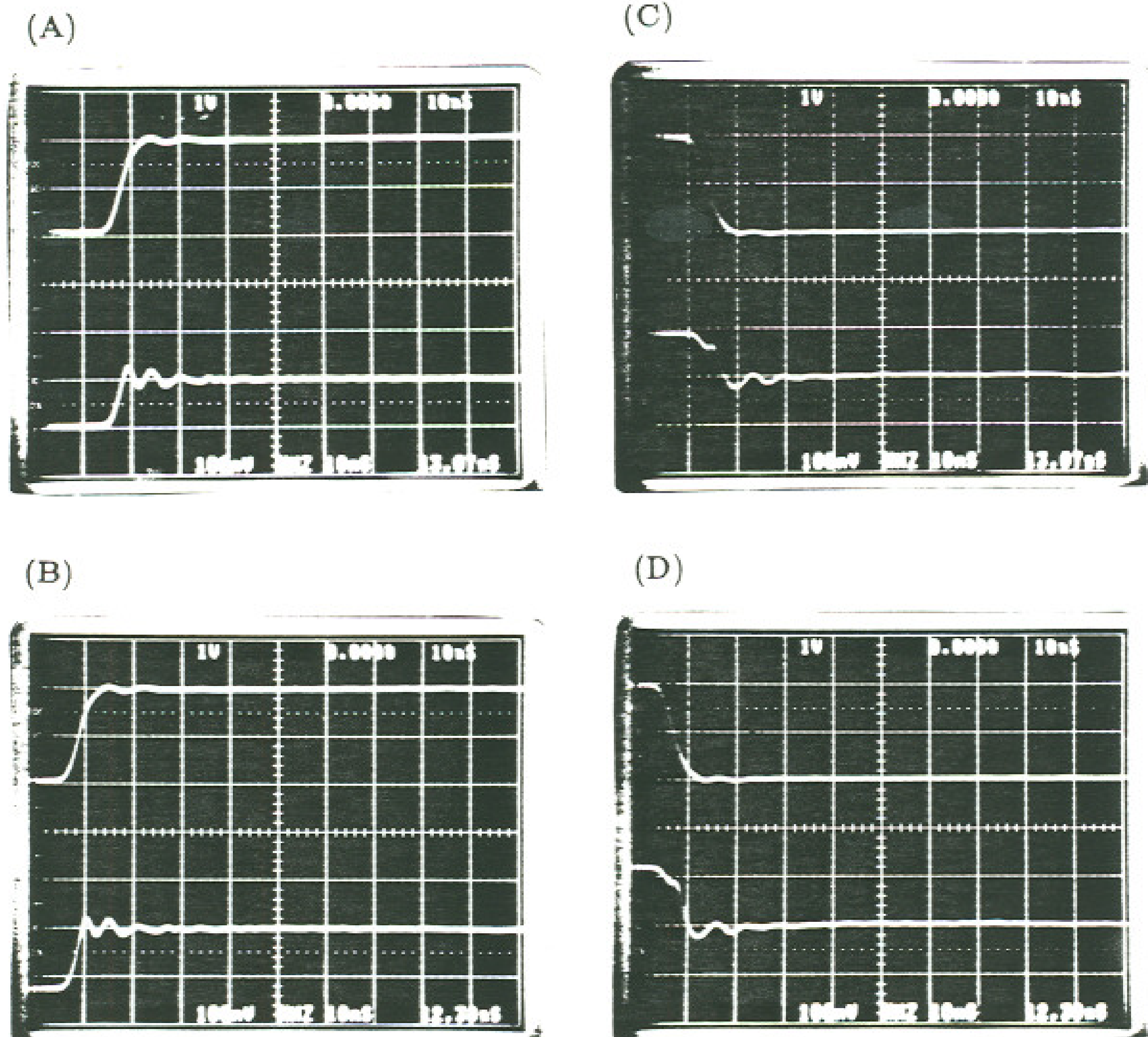
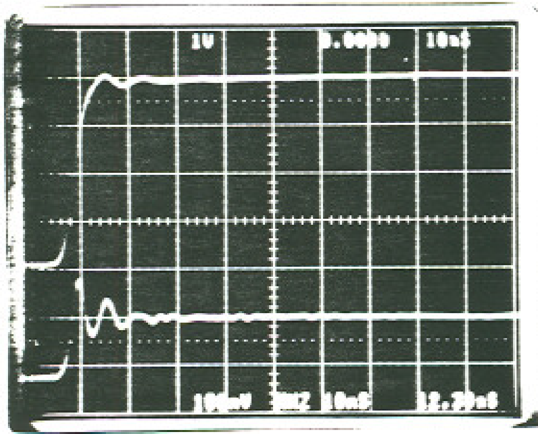
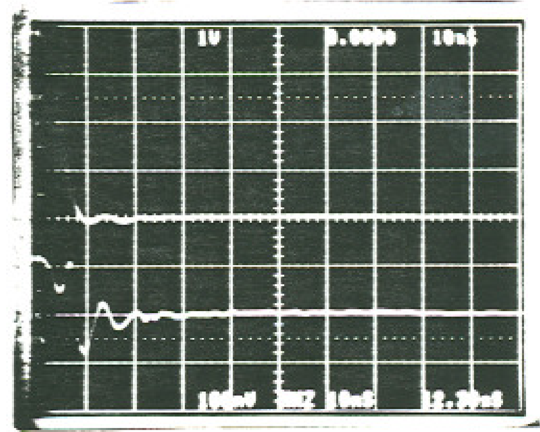


Figure 17: P-channel gate input and load output waveforms; (A),(B) the rising edge measured before and after DC stress with a gate base-level, Vg=0=>-2V, (C),(D) the respective falling edge, (E),(F) the rising edge measured with a gate base-level, Vg=+2=>-2V, (G),(H) the respective falling edge. Stress conditions were Vd=-10.0V, Vg=-1.7V for 16 hrs. Measurements were made with 50% duty cycle pulses at a frequency of 10 kHz.

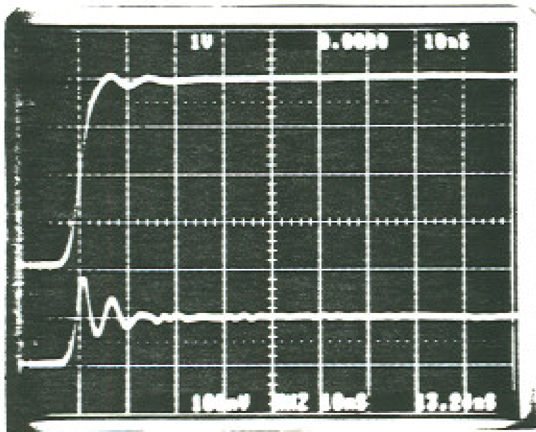
(E)



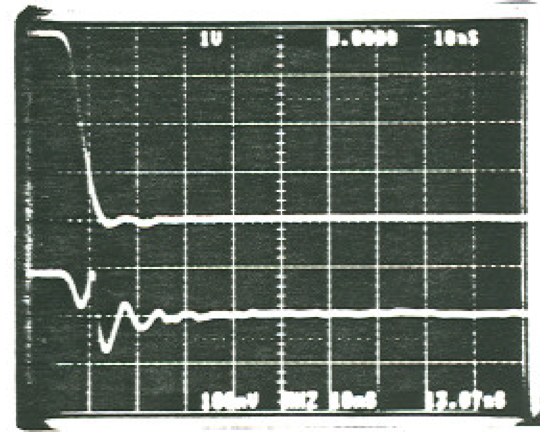
(G)



(F)



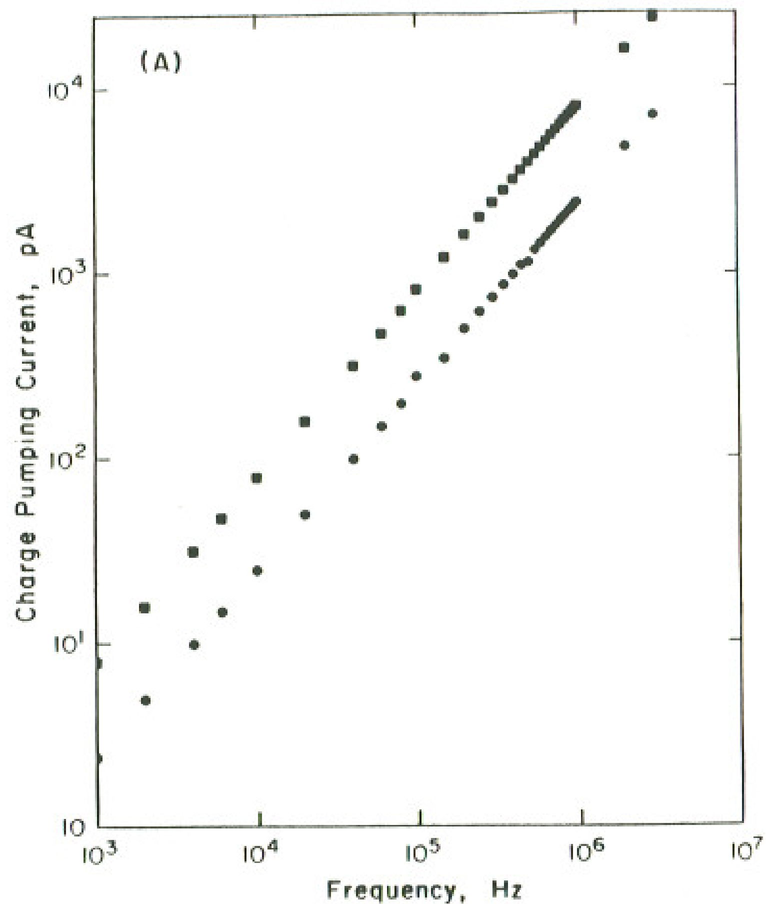
(H)



tively. However, waveform overshoot and ringing are more pronounced with increasing base-level magnitude.

4.3 Charge Pumping Measurement

Charge pumping measurements were made before and after DC stress for n- and p-channel devices. Figures 18 and 19 show that charge pumping current increases following stress, in agreement with reported results [14,15]. Figure 18 presents the n-channel pre- and (higher) post-stress charge pumping current, (A) and corresponding difference,(B) as functions of frequency. Figure 19 shows the same data measured from the p-channel case. Note that charge pumping current is significantly increased after stress in both cases. This is experimental evidence that hot carriers damage the interface and generate interface states. The degree of damage is primarily determined by the bias voltages: Vg by controlling the carrier injection rate into the high field region, and Vd by dictating the channel electric field near the drain. Notice also that charge pumping current is proportional to frequency. This can be expected from equations (1) and (2), and from published findings [16,17].



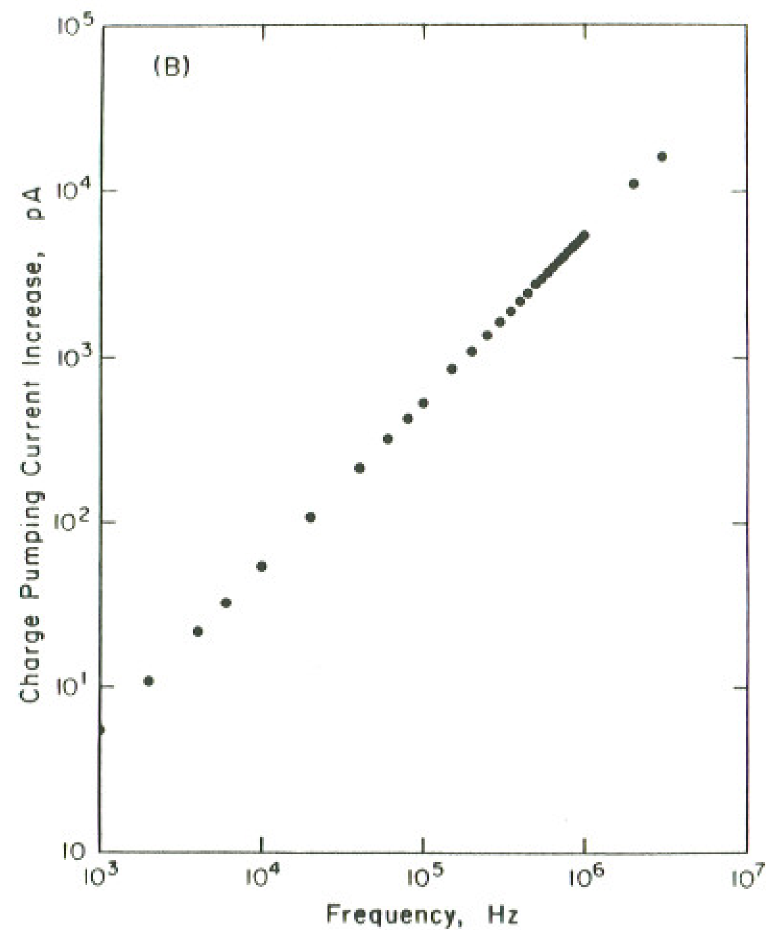
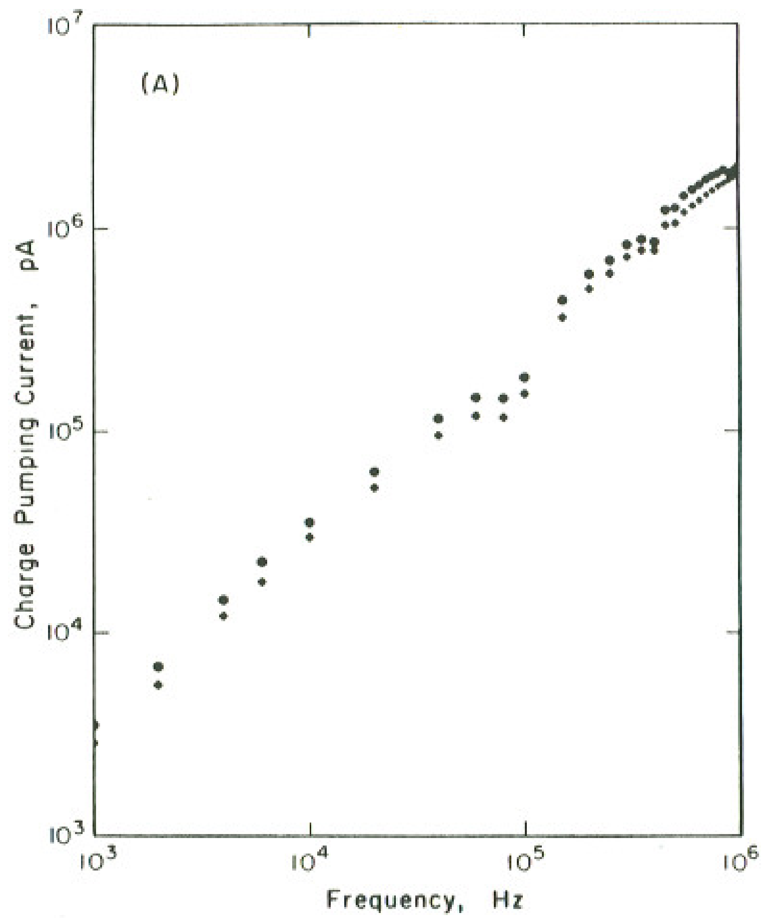


Figure 18: (A) N-channel charge pumping current vs. frequency before (●) and after (◆) DC stress, (B) the corresponding change in charge pumping current vs. frequency. Stress conditions were Vd=7.5V, Vg=2.5V for 2 days.



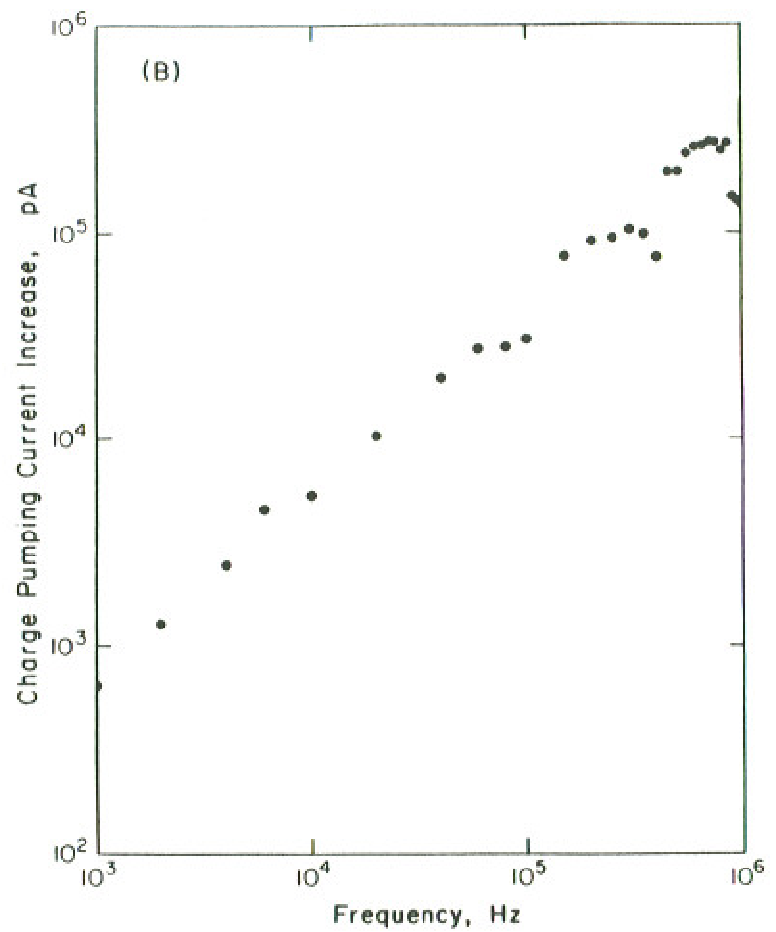


Figure 19: (A) P-channel charge pumping current vs. frequency before (◆) and after (●) DC stress, (B) the corresponding change in charge pumping current vs. frequency. Stress conditions were Vd=-10V, Vg=-1.7V for 21 hrs.

4.4 AC vs. DC Stress

The focus of this section is to present the data collected in testing the assumption that AC and DC stresses are equivalent for small time increments. As mentioned in the previous section, AC and DC data under DC stress were found to be the same. Here, the effects of AC and DC stresses are compared in terms of DC parameter measurement.

Devices with the same initial substrate current were evaluated in terms of the following stress conditions: (a) DC drain with DC gate bias, (b) AC drain with DC gate bias and (c) AC gate with DC drain bias. The shifts in Gm and Idsat were examined for n- and p-channel devices.

4.4.1 PMOS

As discussed in the previous chapter, instabilities in p-channel parameters can be significantly enhanced at stress bias conditions that cause peak gate current to flow [18,19]. Figure 20 displays both substrate and gate currents as functions of gate voltage for different Vd's. Note that the peak gate current for a fixed drain voltage (Vd=-8.0V), occurs when Vg≈ -1.0V. Devices were tested for the three cases, (a),(b) and (c) near the worst case condition, namely at Vd=-8.0V, Vg=-1.0V and Vd=-8.0V, Vg=-2.0V.

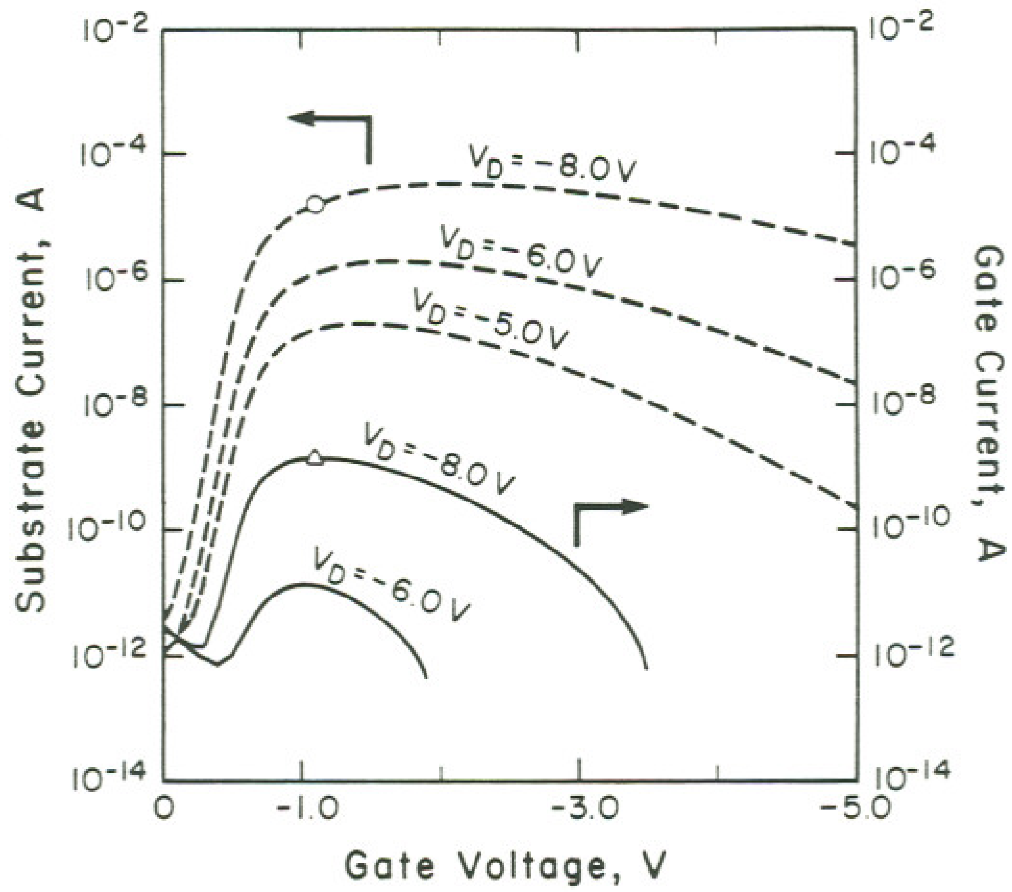


Figure 20: P-channel substrate (---) and gate (—) current vs. gate voltage for different drain voltages.

Figure 21 shows typical stress gate current as a function of DC stress time from case (a). Note that it starts at a maximum and monotonically decreases as time increases. This can be qualitatively understood as increased hot electron trapping reducing the channel field near the drain end [20,21].

The resulting Idsat shifts measured for the three cases, (a), (b) and (c) near the maximum gate current are plotted as a function of stress time in Fig. 22 (Vd=-8.0V, Vg=-1.0V) and Fig. 23 (Vd=-8.0V, Vg=-2.0V). AC stress time was compared with DC stress time in terms of the active duty cycle pulse 'on time'. Notice that there does not exist a significant difference among these three cases. This implies that near the worst case gate bias, AC gate or AC drain stress result in degradation comparable to the DC case in terms of the active duty cycle. Note also (i) the non-saturating behavior of the Idsat shifts as a function of stress time, and (ii) that the peak gate current (Vg=-1.0V), is consistently associated with higher Idsat shifts.

When these three stress cases are compared at a gate bias much higher in magnitude than the worst case, i.e. Vg=-5V, there is a distinct difference in the parameter shifts. As observed in Fig. 24, cases (a) and (b) do not show much shift at all (within the 1% limit of the system

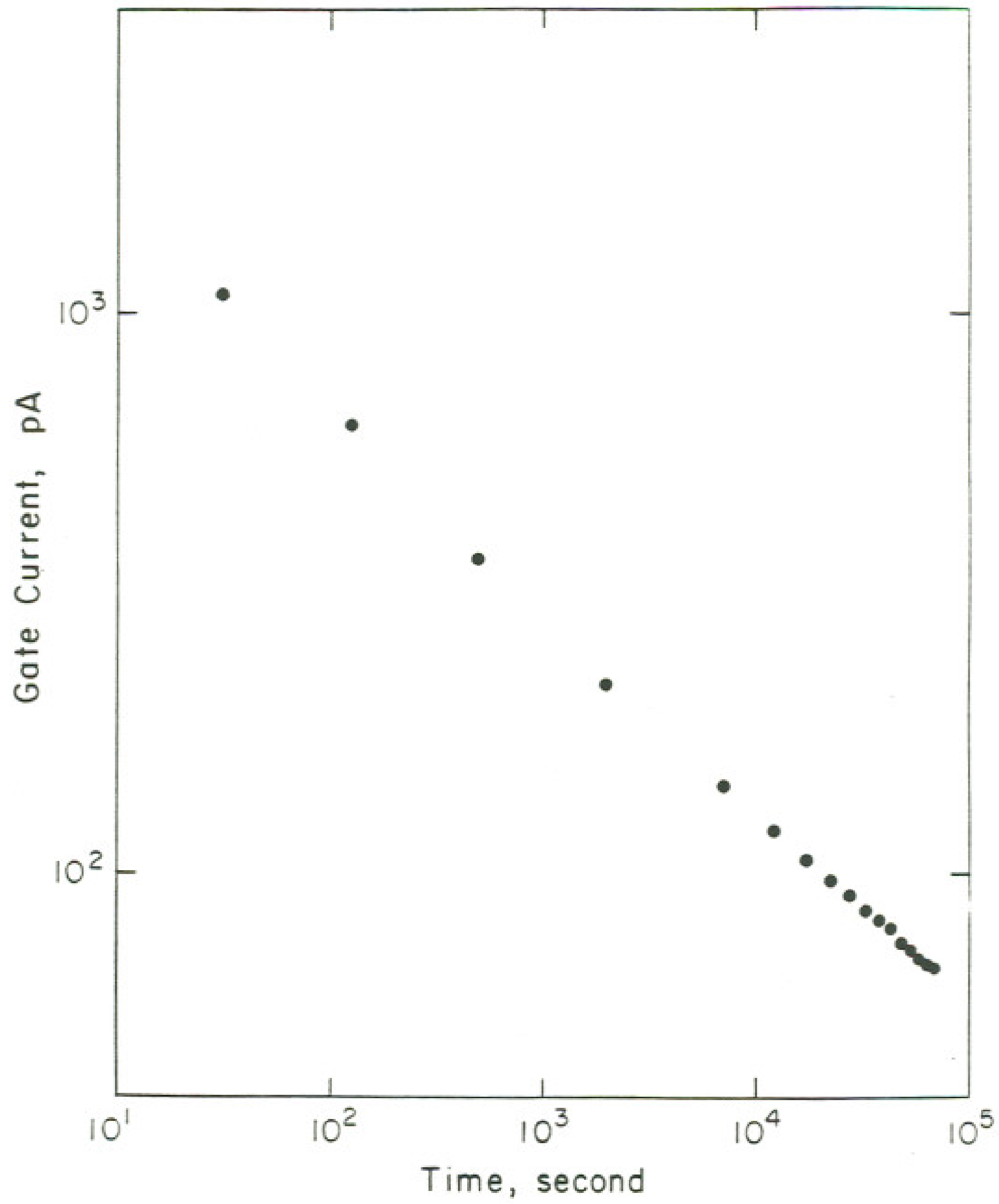


Figure 21: P-channel gate current vs. DC stress time. Stress conditions were Vd=-8.0V, Vg=-1.0V.

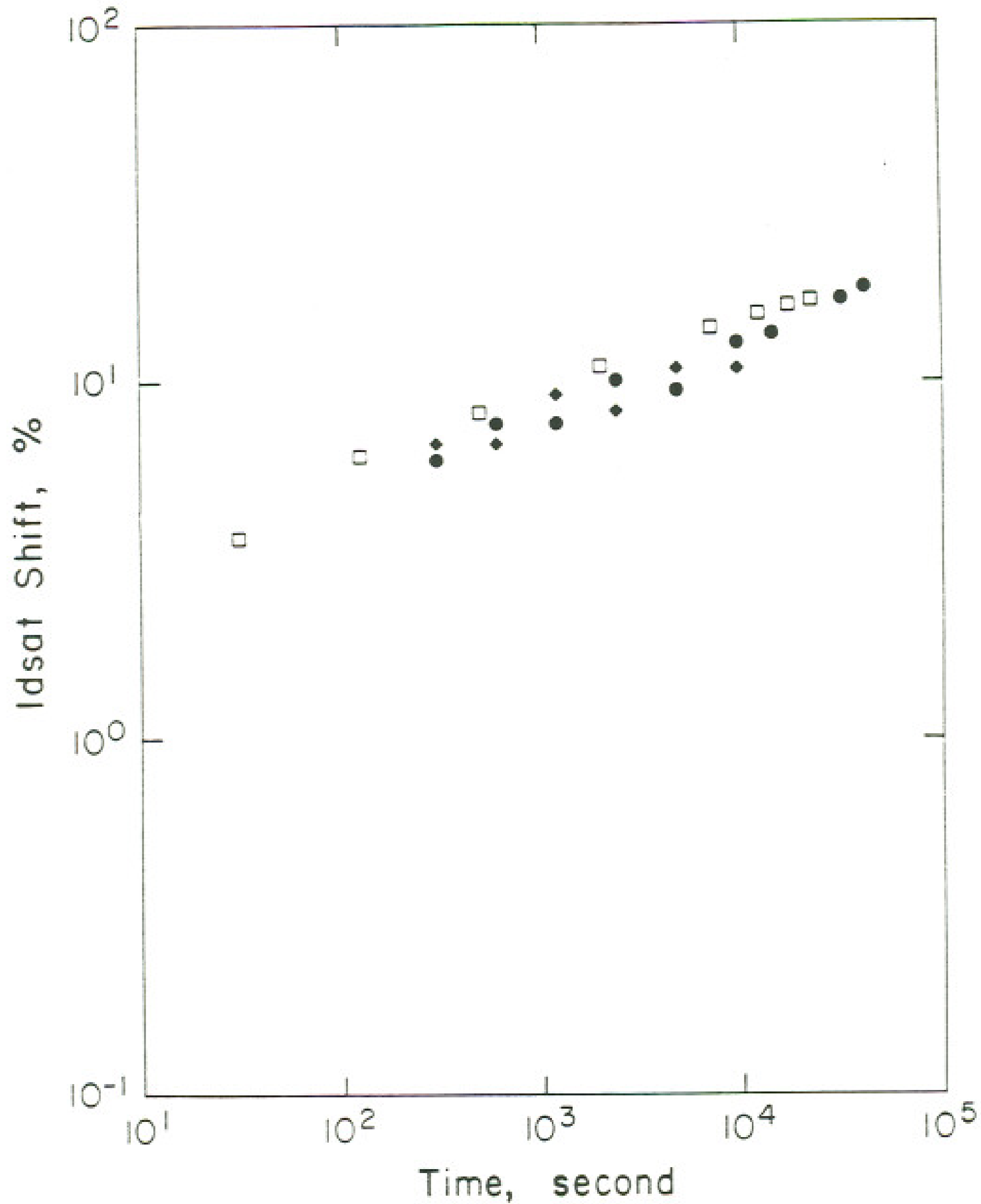


Figure 22: P-channel Idsat shifts vs. effective stress time: filled diamonds (◆) represent an AC stress with Vd=-8.0V drain pulse, Vg=-1.0V DC gate bias, filled circles (●) represent an AC stress with Vg=-1.0V gate pulse, Vd=-8.0V DC drain bias and open squares (□) represent a DC stress with Vd=-8.0V, Vg=-1.0V. Stress was applied with 50% duty cycle pulses at a frequency of 10 MHz.

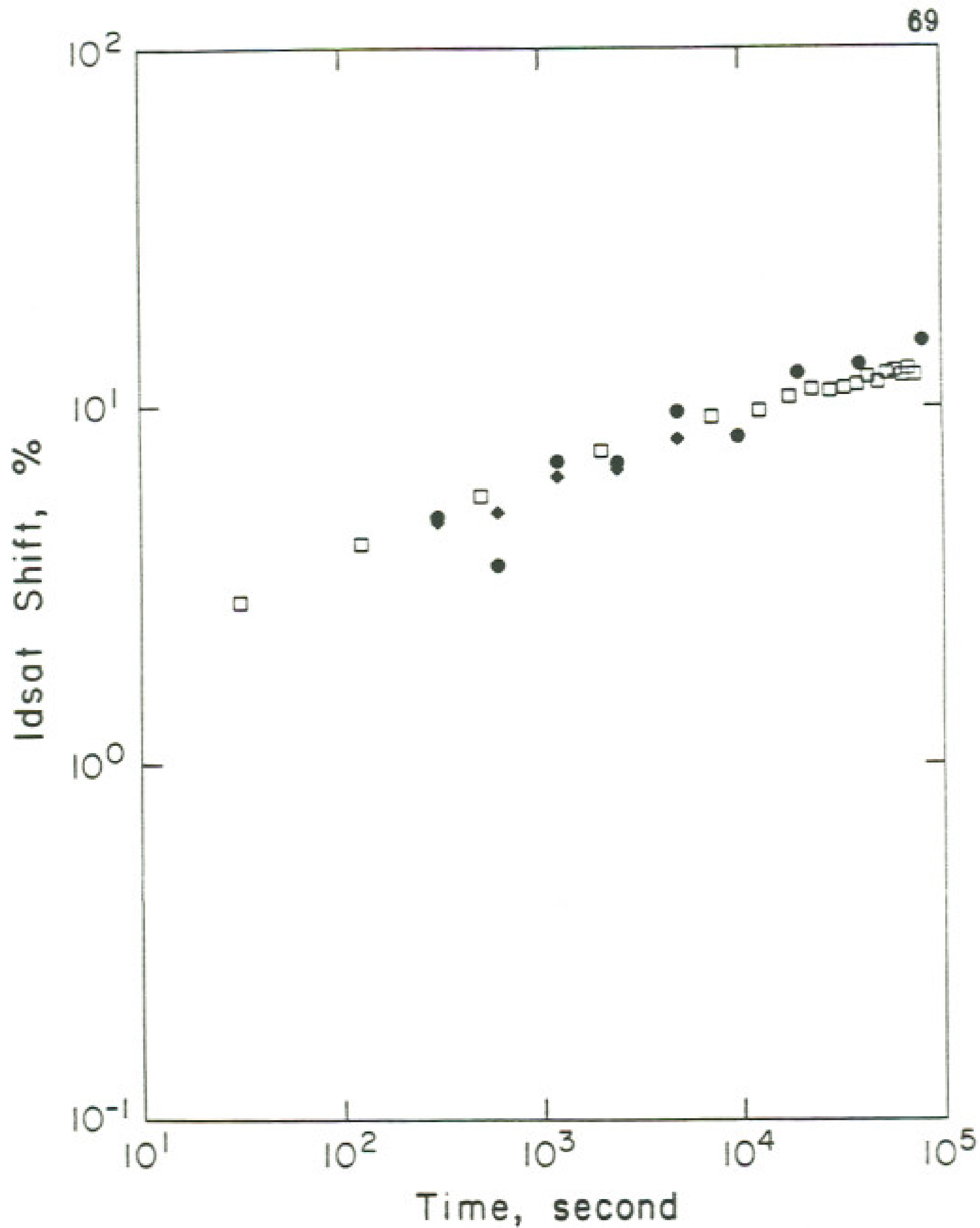


Figure 23: P-channel Idsat shifts vs. effective stress time: filled diamonds (◆) represent an AC stress with Vd=-8.0V drain pulse, Vg=-2.0V DC gate bias, filled circles (●) represent an AC stress with Vg=-2.0V gate pulse, Vd=-8.0V DC drain bias and open squares (□) represent a DC stress with Vd=-8.0V, Vg=-2.0V. Stress was applied with 50% duty cycle pulses at a frequency of 10 MHz.

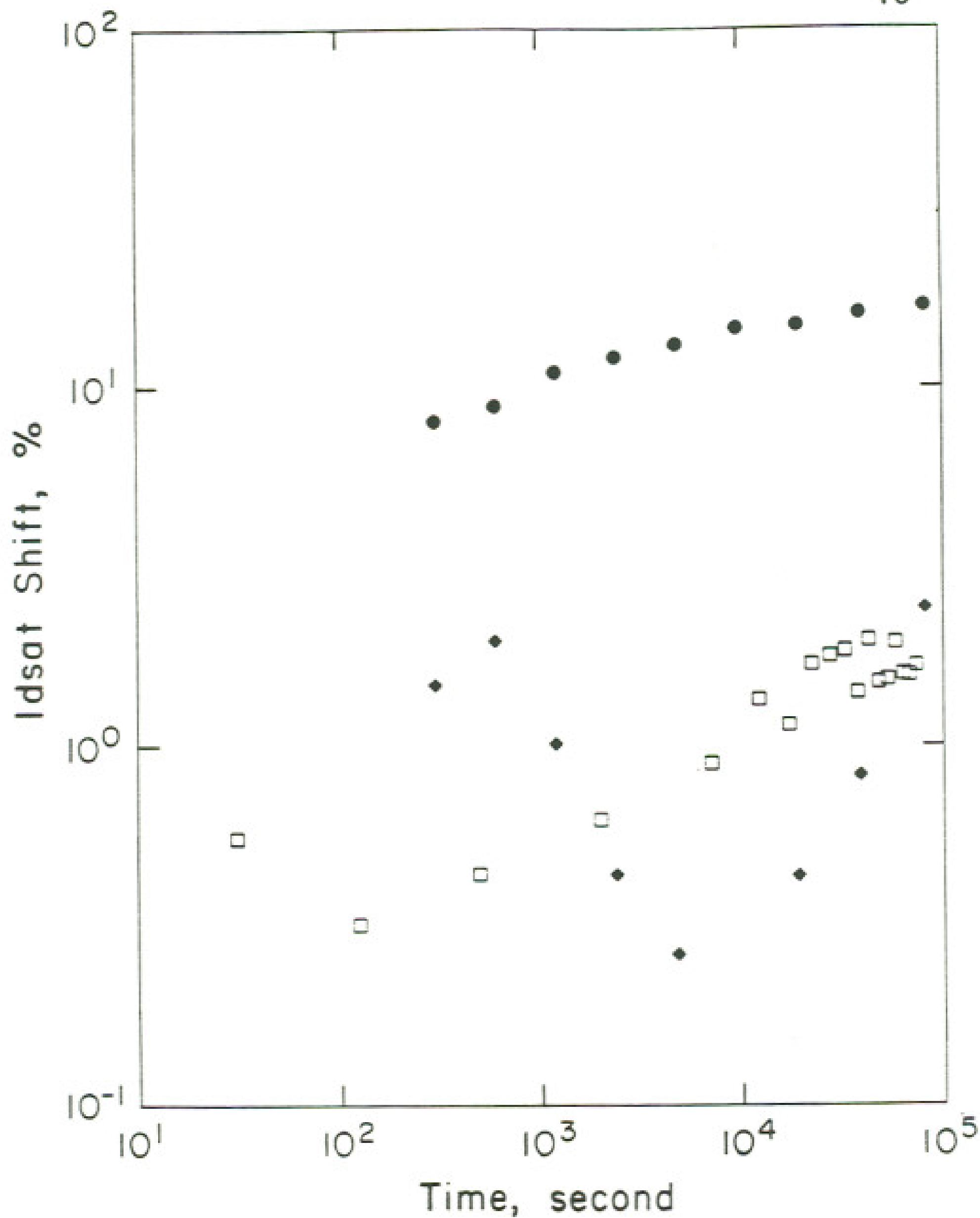


Figure 24: P-channel Idsat shifts vs. effective stress time: filled diamonds (◆) represent an AC stress with Vd=-8.0V drain pulse, Vg=-5.0V DC gate bias, filled circles (●) represent an AC stress with Vg=-5.0V gate pulse, Vd=-8.0V DC drain bias and open squares (□) represent a DC stress with Vd=-8.0V, Vg=-5.0V. Stress was applied with 50% duty cycle pulses at a frequency of 10 MHz.

resolution). This is in marked contrast with the results of Figs. 22 and 23 where Idsat shifts as much as 10% were observed for (a) and (b). However, unlike (a) and (b), case (c) shows the same non-saturating 10% Idsat shift as in Figs. 22 and 23. To the best of our knowledge, the striking difference observed in case (c) from those of (a) and (b) is reported here for the first time.

Since the AC gate stress resulted in more pronounced Idsat shift, the p-channel degradation behavior was further examined using different gate pulsing conditions. Figure 25 presents the shift in Idsat as a function of stress time for several different gate pulse amplitudes at a fixed off-bias, i.e. Vg=0V. As can be seen from this figure, Idsat shift is essentially the same for all the gate pulse amplitudes used. As mentioned earlier, the maximum degradation in p-channel devices occurs at a gate bias, Vgm causing maximum gate current. Hence, as long as the gate pulse amplitude crosses Vgm, the parameter shift is essentially the same.

Next, the gate voltage amplitude was varied by changing the pulse base-level for a fixed on-bias, i.e. Vg=-1.0V. Figure 26 presents the corresponding Idsat shifts as a function of stress time for different gate pulse base-levels. Again the effect of gate base-level on device degradation is not significant.

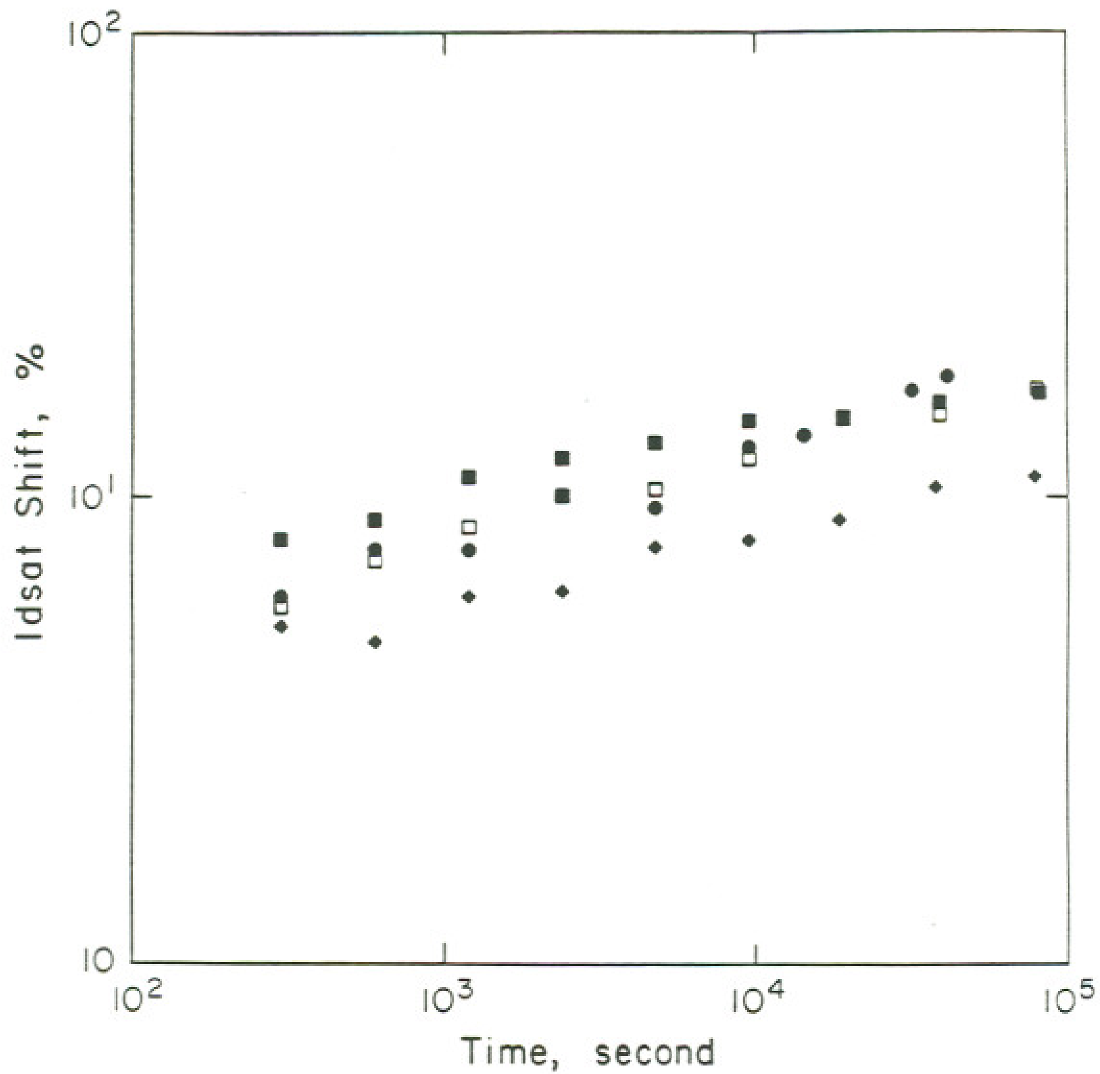


Figure 25: P-channel Idsat shifts vs. effective stress time for different gate pulse amplitudes at a common voltage high, (Vg=0V) and a common DC drain bias, Vd=-8.0V : filled circles (●) represent an AC stress with a Vg=-1=>0V gate pulse, open squares (□) with a Vg=-2=>0V gate pulse, filled diamonds (◆) with a Vg=-4=>0V gate pulse and filled squares (■) with a Vg=-5=>0V gate pulse. Stress was applied with 50% duty cycle gate pulses at a frequency of 10 MHz.

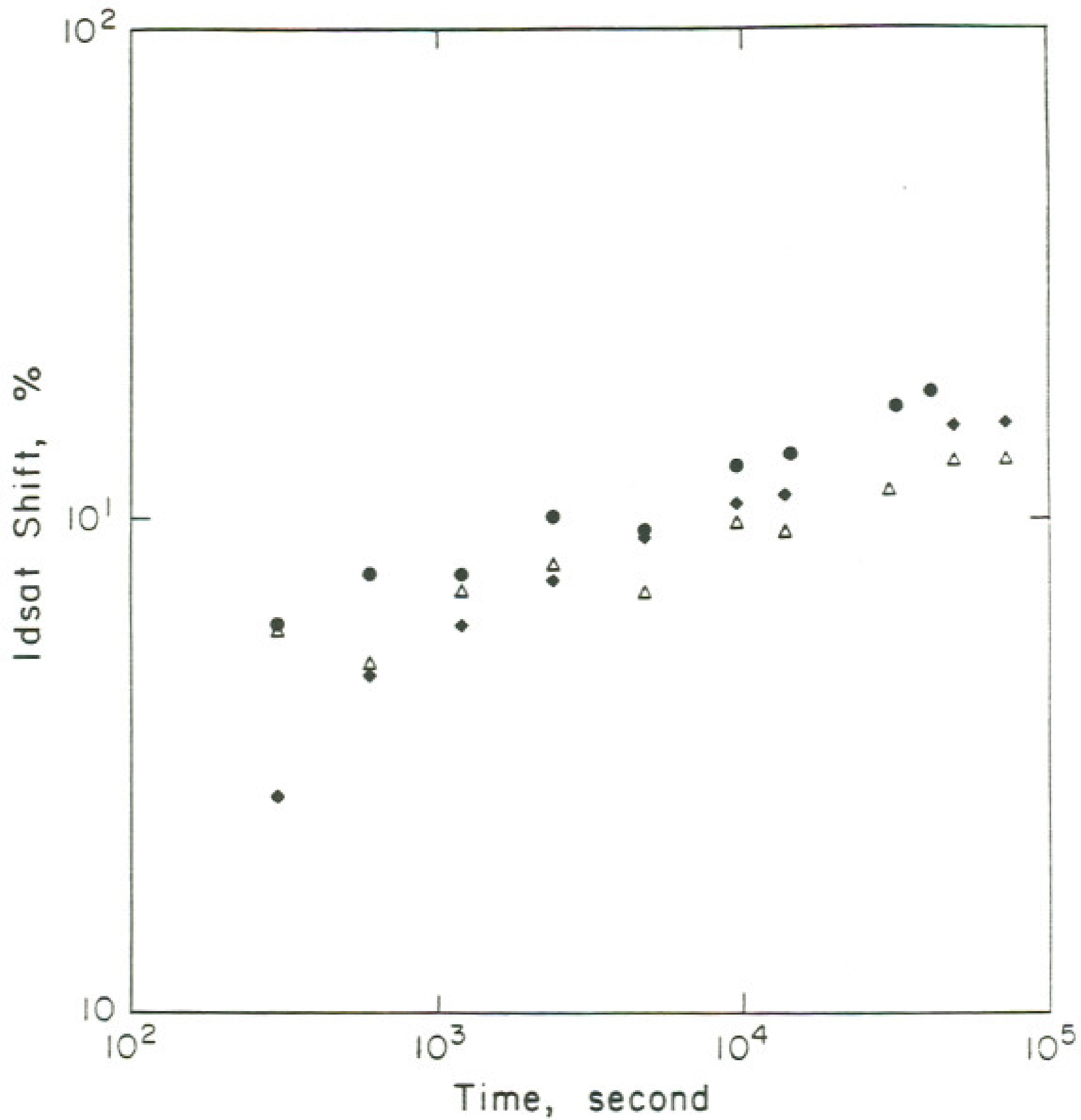


Figure 26: P-channel Idsat shifts for different gate pulse base-levels at a common voltage low, (Vg=-1.0V) and a common DC drain bias, Vd=-8.0V : filled circles (●) represent an AC stress with a Vg=0=>-1V gate pulse, filled diamonds (◆) with a Vg=+1=>-1V gate pulse and open triangles (△) with a Vg=+2=>-1V gate pulse. Stress was applied with 50% duty cycle gate pulses at a frequency of 10 MHz.

4.4.2 NMOS

The performance of n-channel transistors was likewise examined under the three stress conditions, (a),(b) and (c). The instabilities in n-channel transistors are sharply peaked at stress bias causing the maximum substrate current [19,20].

Figure 27 shows both substrate and gate currents as functions of gate voltage for different Vds. The peak substrate current for a fixed drain voltage (Vd=7.5V) is shown to occur when Vg $\approx$ 2.0V. Figure 28 presents the substrate current as a function of DC stress time from case (a). Again the substrate current monotonically decreases as stress time increases.

Figure 29 is the n-channel counterpart of the p-channel data presented in Fig. 22. The gate voltage was chosen near the worst case bias, i.e. near Vg=2.0V. The same observed Gm shift for cases (a) and (b) suggests that AC drain stress results in degradation identical to the DC case in terms of the active duty cycle. The gate pulsing stress, case (c) however, gives rise to considerably larger Gm shift for all the examined stress times. This is in marked contrast with the p-channel case (Fig. 22). The work of Cham et al using gate and drain pulse stress on submicron NMOS devices is in agreement with this data [22].

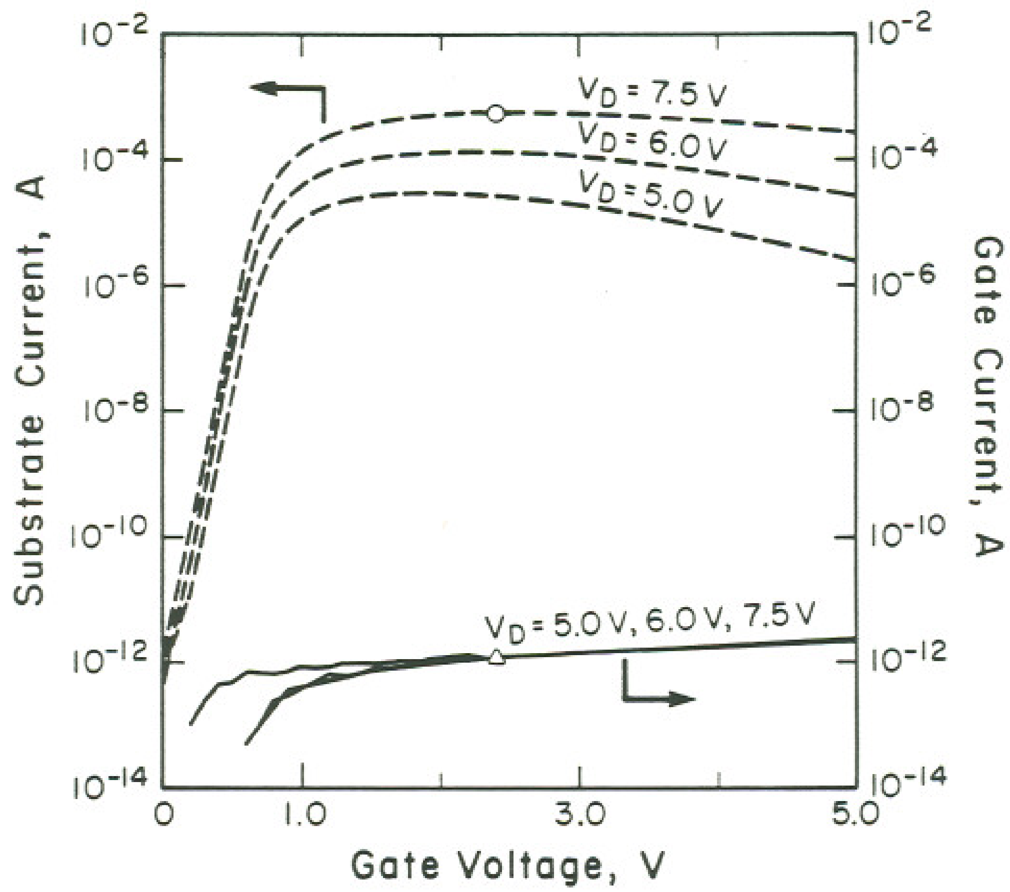


Figure 27: N-channel substrate (---) and gate (—) current vs. gate voltage for different drain voltages.

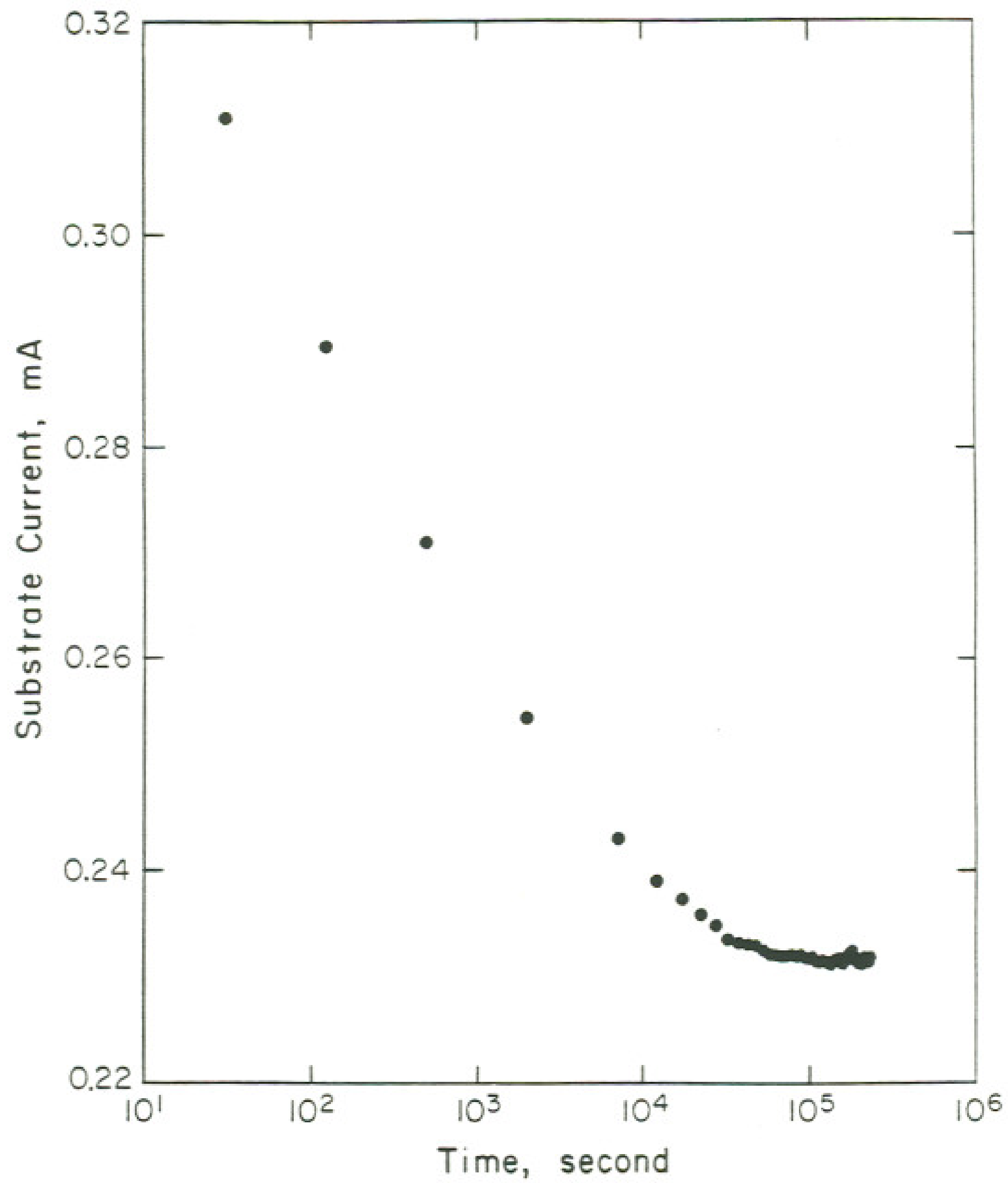


Figure 28: N-channel substrate current vs. DC stress time. Stress conditions were Vd=7.5V, Vg= 2.0V.

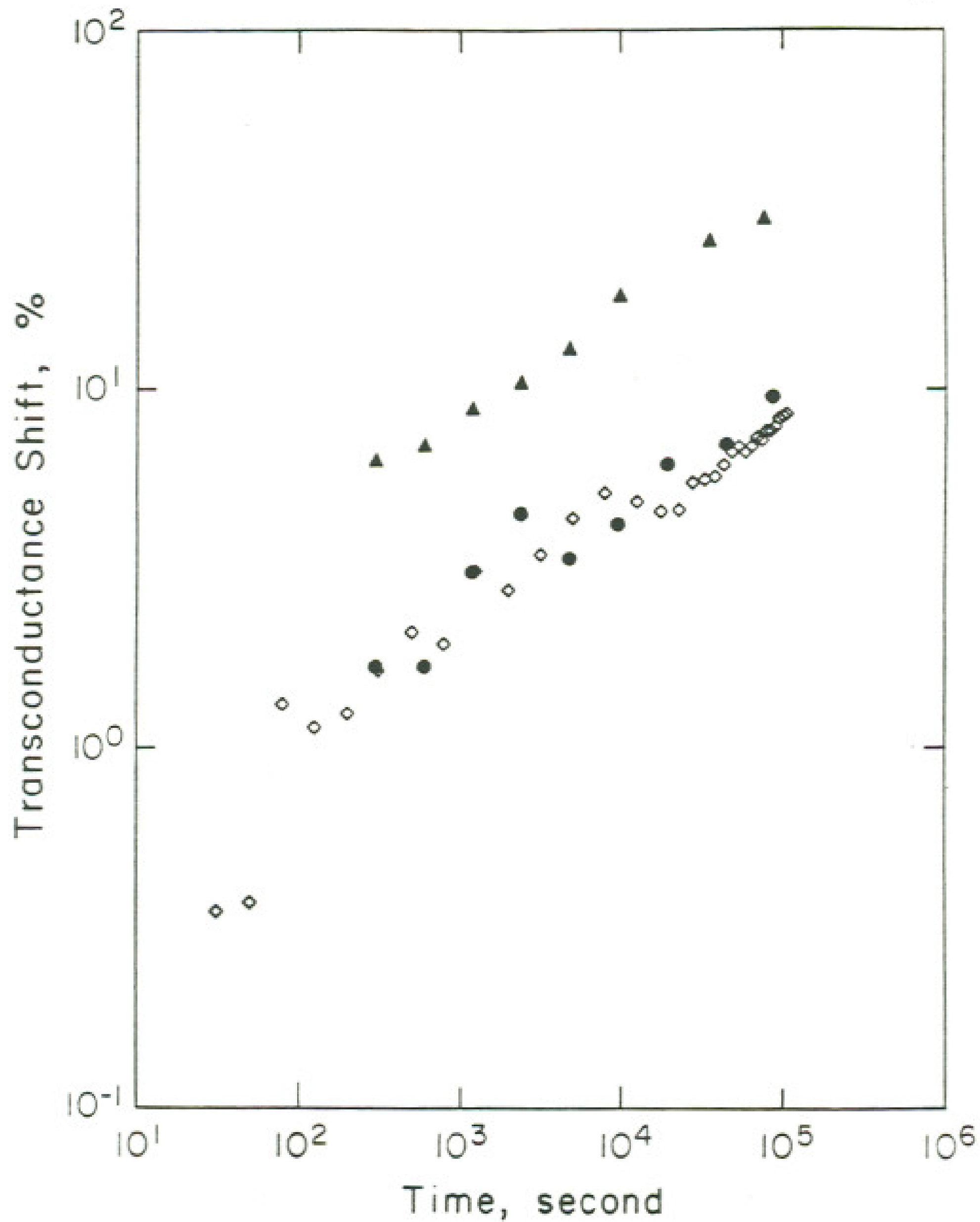


Figure 29: N-channel Gm shifts vs. effective stress time: filled circles (●) represent an AC stress with Vd=7.5V drain pulse, Vg=2.0V DC gate bias, filled triangles (▲) represent an AC stress with Vg=2.0V gate pulse, Vd=7.5V DC drain bias and open diamonds (◇) represent a DC stress with Vd=7.5V, Vg=2.0V. Stress was applied with 50% duty cycle pulses at a frequency of 10 MHz.

Next, attempts were made to compare these cases at a bias much higher than worst case, i.e. Vg=5V. Figure 30 presents the Gm shift for case (a) only. In contrast to the p-channel case, the parameter shift is almost the same as that in Fig. 29. The data for cases (b) and (c) could not be obtained because of repeated device failure via gate burn-out. Devices failed for both case (b) (Vd=7.5V AC, Vg=5.0V DC) and case (c) (Vg=5.0V AC, Vd=7.5V DC).

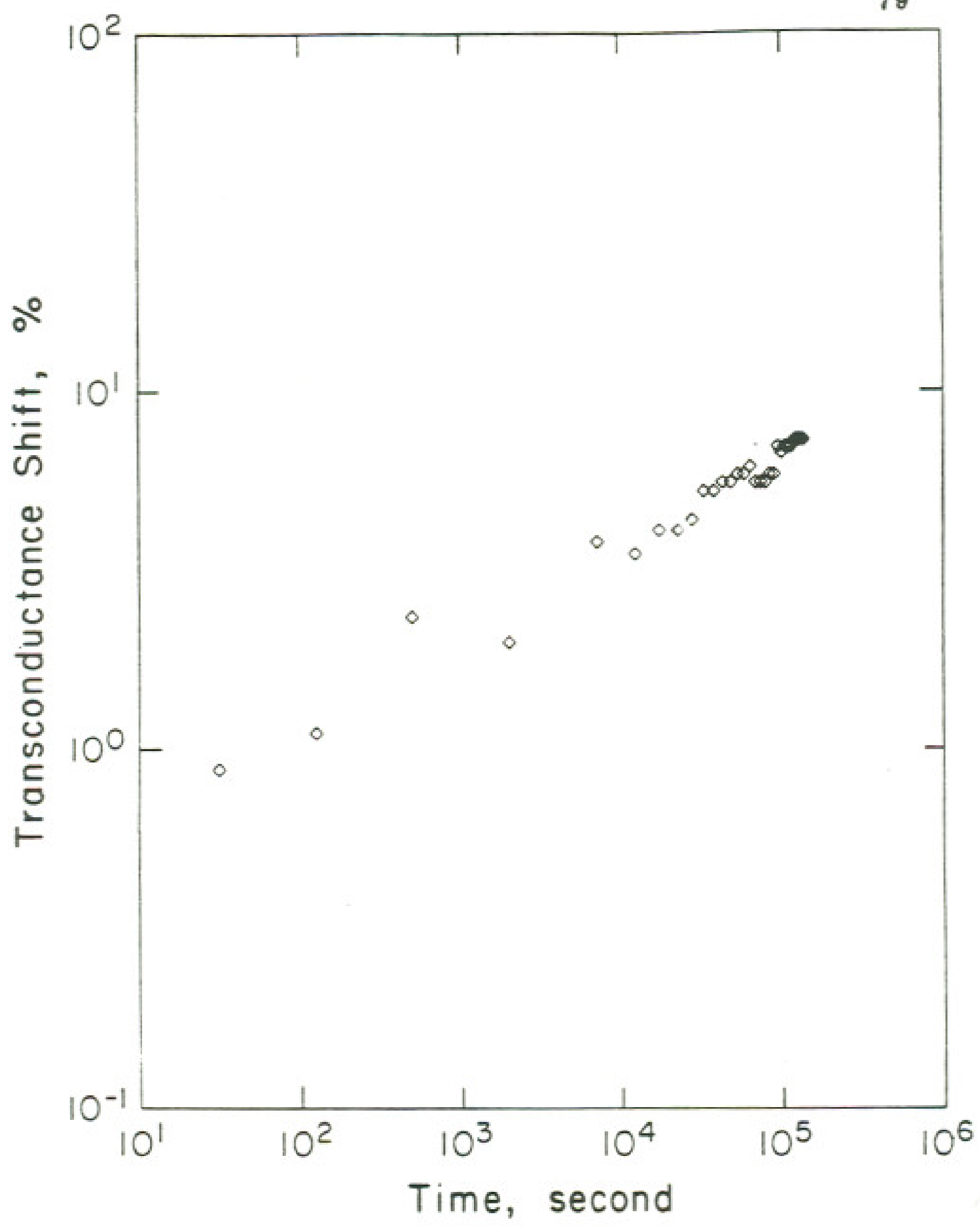


Figure 30: N-channel Gm shift vs. effective stress time: open diamonds (◇) represent a DC stress with Vd=7.5V, Vg=5.0V.

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CHAPTER 5

INTERPRETATION AND DISCUSSION

In this section the physical processes associated with stress induced degradation will be highlighted. First a general discussion of the physics behind the hot carrier phenomenon will be briefly summarized. Following this, the specific hot carrier effects as applied to the data presented in this thesis will be discussed.

5.1 General Discussion

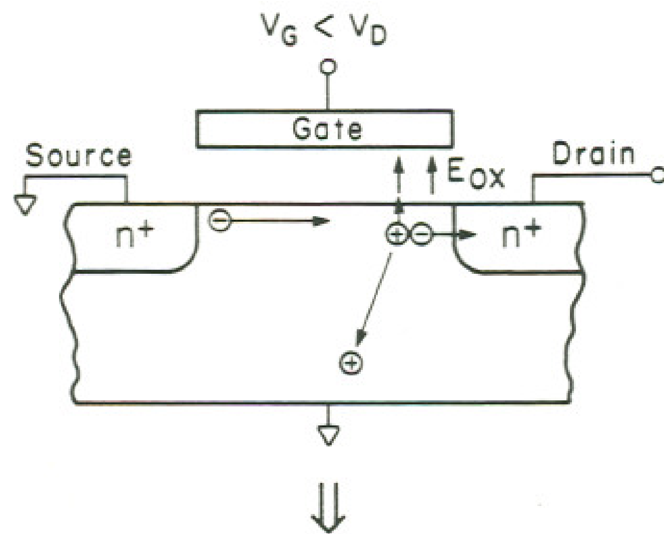
As mentioned in the introduction, there is a general consensus that the driving force behind all hot carrier effects is the large electric field induced at the drain end of short channel devices. In the presence of a high field, a carrier can gain enough kinetic energy that upon collision with an atom, it can break lattice bonds and create an electron-hole pair. This is illustrated schematically for the case of the n-channel device in Fig. 31.

The stress enhanced substrate current is a direct consequence of hot carrier effects. The substrate current can be phenomenologically expressed as,

$$\mathrm{Isub} \propto \mathrm{Id} \cdot \exp(-\mathrm{Qi}/q\lambda \mathrm{Em}) \qquad (7)$$

N-Channel Hot Carrier Effects

Hot Carrier Injection and Impact Ionization



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Resulting Device Degradation

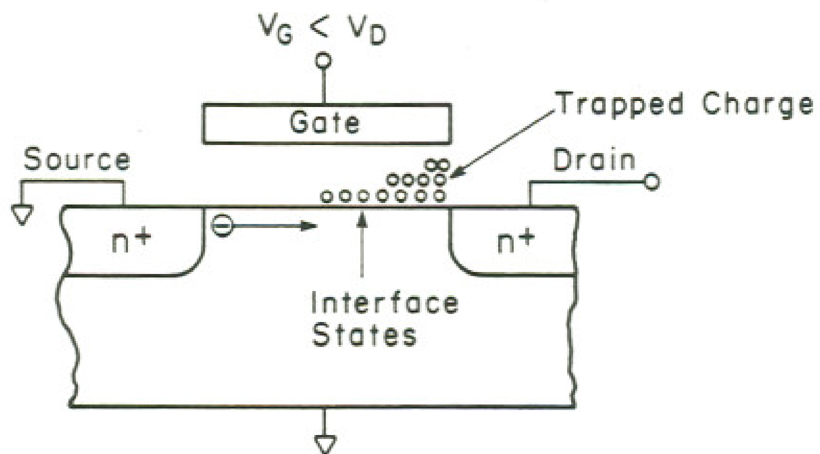


Figure 31: N-channel hot carrier induced degradation model.

where Id is the drain current, Qi the minimum energy for impact ionization, q the electronic charge, λ the carrier mean free path and Em the maximum channel electric field [1-4]. The substrate current is determined by two factors, first Id, a measure of the number of carriers injected into the high field region, and second, the exponential term representing the probability that the hot carrier gains sufficient energy to give rise to impact ionization. As the electric field, Em is increased, Isub exponentially grows.

The failure mechanism in devices involves two steps: (i) a high field giving rise to hot carriers, and (ii) the injection and/or trapping of these hot carriers in the oxide/interface region. An important consequence of this is the formation of interface states or traps. Interface trap generation therefore can be empirically modeled as,

$$\Delta \mathrm{Nit} \propto \left[\frac{t \cdot \mathrm{Id}}{\mathrm{W}} \cdot \exp(-\mathrm{Qit}/q\lambda \mathrm{Em})\right]^{n} \tag{8}$$

where ΔNit is the generated interface trap density, t the stress time, W the channel width, Qit the critical energy required to create an interface trap and n an empirical fitting parameter [1,4].

Interface state generation also is comprised of two factors; the total number of carriers spilling into the high field region during the stress time

t, t·Id/W and the probability to create an interface trap.

Charge pumping current, Icp is a monitor of interface state generation. The current can be correlated to Nit as,

$$Icp \propto q \cdot f \cdot A \cdot Nit \cdot \Delta E \tag{9}$$

where f is the pulse frequency, A the effective gate area and ΔE the interface state energy range [4-7]. Charge pumping current can, in essence, be interpretated as being due to the carriers which are detrapped from the interface states via the gate bias. Thus an increase in interface state density due to stress will be accordingly reflected in an increase in charge pumping current [8].

The physical damages introduced by hot carriers are not only reflected in interface trap generation, but also in shifts in such device electrical parameters as Gm, Vt, Idsat and S. The stress induced parameter shift in the normalized subthreshold swing, S/So is related to the shift in the normalized interface state generation, Nit/Nito as,

$$\frac{\Delta S}{So} \propto \frac{\Delta Nit}{Nito} \cdot \frac{Csso}{Cox + Cd + Csso} \tag{10}$$

where So is the initial subthreshold swing, Nito the initial interface state density, Csso the initial surface state capacitance. Cox the gate oxide capacitance and Cd the depletion region capacitance [9].

5.2 DC Stress and DC Characterization

The data presented in this thesis are now discussed. Charge pumping current measurements before and after stress (Figs. 18 and 19) show that indeed interface states are generated as a result of stress for both n- and p-channel devices. For both the cases, Nit is approximately proportional to stress time for all frequencies used for measurement, i.e. the empirical factor in Eq. (8) is approximately one.

For PMOS, both substrate and gate current exhibit pronounced peak as a function of gate voltage (Fig. 20). This trend can be understood with the use of Eq. (7) in conjunction with the electric field distribution in the channel. For a fixed Vd in the leakage region of device operation, most of the drain voltage is dropped across the reverse-biased p-n junction region at the drain end. The field is therefore highly localized and Em at the drain end is large. This field configuration remains more or less the same throughout the subthreshold region.

With the onset of channel formation, Em is still high since the device is saturated. With increasing Vg, the device enters into the linear region, and Em will be rapidly reduced. In the leakage and subthreshold regions, Em will remain essentially flat and the impact ionization rate is constant. At fixed Vd, the drain current exponentially increases with increasing Vg

in the subthreshold region. Thus, the resulting electron flux into the high field region gives rise to the rapid increase in substrate current.

For Vg > Vt, Id increases according to the power law Vg (linear region) or Vg^2 (saturation region). Simultaneously, Em decreases slightly for the reasons discussed in [10]. The effect of the slight decrease in Em is exponentially amplified (Eq. (7)). Hence, the decrease in probability for impact ionization outweighs the increase in Id, and Isub should fall with increasing Vg. Therefore, Isub will be peaked at an appropriate Vg value. One can understand the substrate current data obtained from the NMOS (Fig. 27) in the same manner.

The behavior of Ig (Fig. 20) can also be understood in a similar manner. Here Isub can be viewed as a source for generating Ig. The same electron, if pulled toward the substrate, constitutes Isub. For the later process, however, the electron can further induce impact ionization, making more carriers available for Isub and Ig. This point was further examined experimentally by measuring Ig and Isub simultaneously. Figure 32 presents Ig vs. Isub plots for several PMOS gate voltages. Clearly, Ig is seen to follow the square law with respect to Isub, viz.

$$Ig = C \cdot Isub^{2} \qquad (11)$$

Here, the proportionality constant, C is found to be independent of

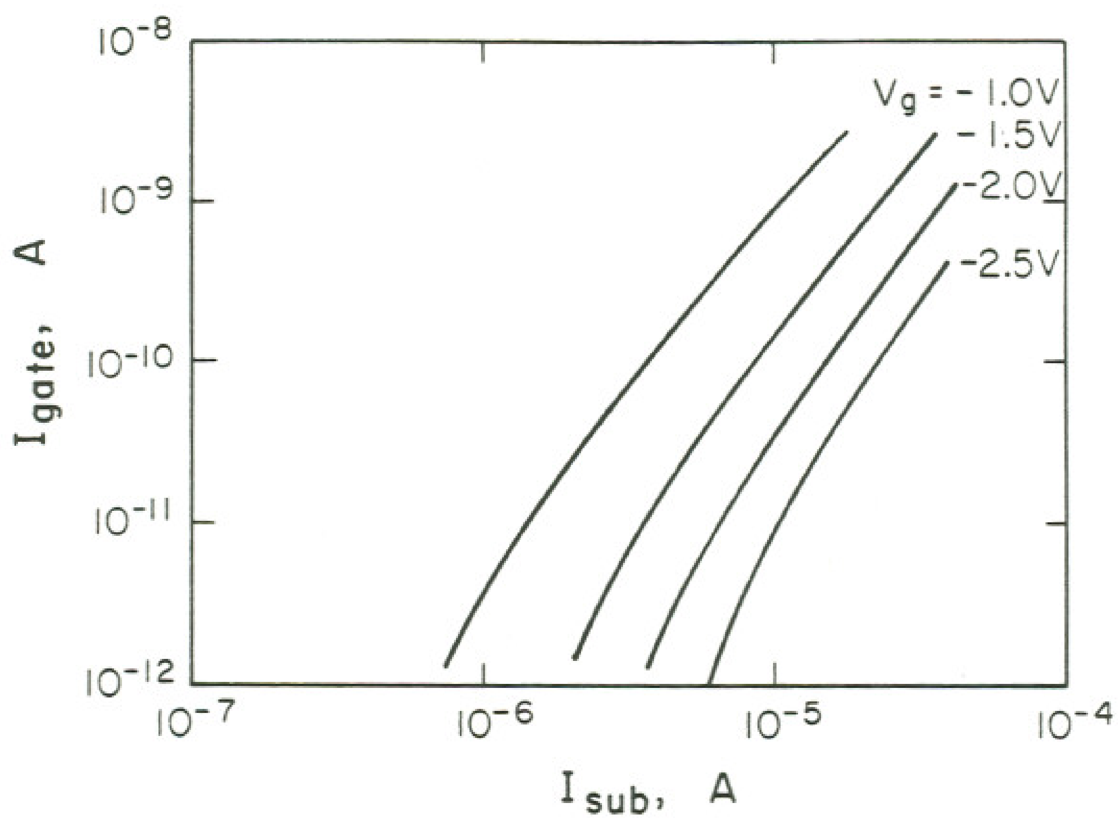


Figure 32: P-channel gate current vs. substrate current for different gate biases with Vd varied from -5.0V to -8.0V.

temperature, but is weakly dependent on Vg. The data presented in Figs. 20 and 32 are consistent with each other. According to Eqs. (7) and (11), Ig is more sensitively dependent on Em than Isub. That is, the peak of Ig should be shifted to the left of the Vg axis from the corresponding Isub-peaks, which is in agreement with the data.

Next, the device parameter shift measured under DC conditions following stress is discussed. For the NMOS, Idsat and Gm decrease due to stress. The Vt-shift is insignificant because Vt is measured with a small Vd bias. The decrease in Idsat and Gm is an indication that the effective channel mobility has decreased, series resistance has increased or the combination thereof. Figure 33 shows that the extracted series resistance does indeed increase with stress time with both DC and AC stress time. The observed transconductance, Gm(obs) depends on the series resistance at the source (Rs) according to

$$\mathrm{Gm(obs)} = \frac{\mathrm{Gm}}{1 + \mathrm{Rs} \cdot \mathrm{Gm}} \tag{12}$$

where Gm is the true transconductance [11]. The monotonic increase in S as a function of stress time is consistent with the monotonic increase in Nit with stress time (Eq. (8)).

Next consider the change in parameter shift as measured in forward

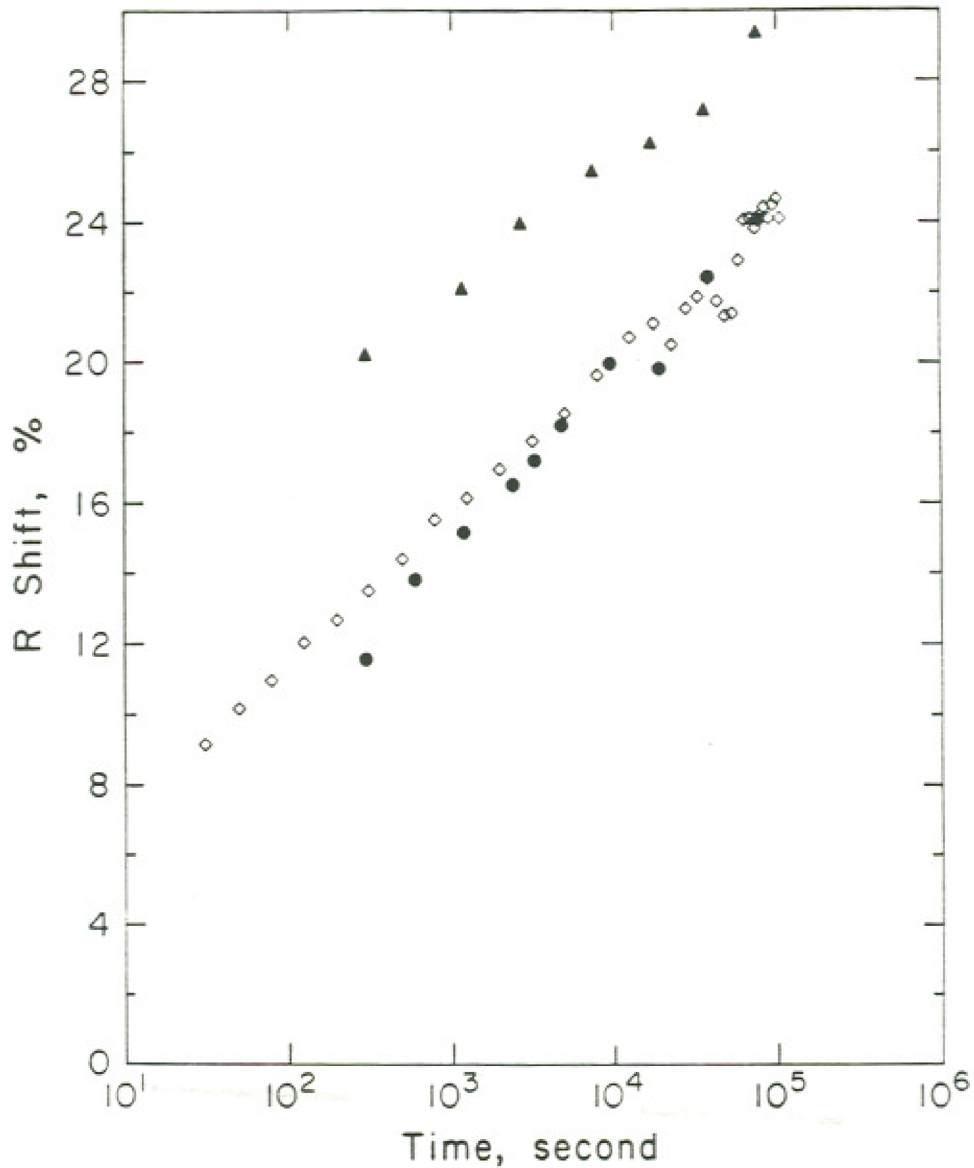


Figure 33: N-channel series resistance vs. effective stress time: filled circles (●) represent an AC stress with Vd=7.5V drain pulse, Vg=2.0V DC gate bias, filled triangles (▲) represent an AC stress with Vg=2.0V gate pulse, Vd=7.5V DC drain bias and open diamonds (◇) represent a DC stress with Vd=7.5V, Vg=2.0V. Stress was applied with 50% duty cycle pulses at a frequency of 10 MHz.

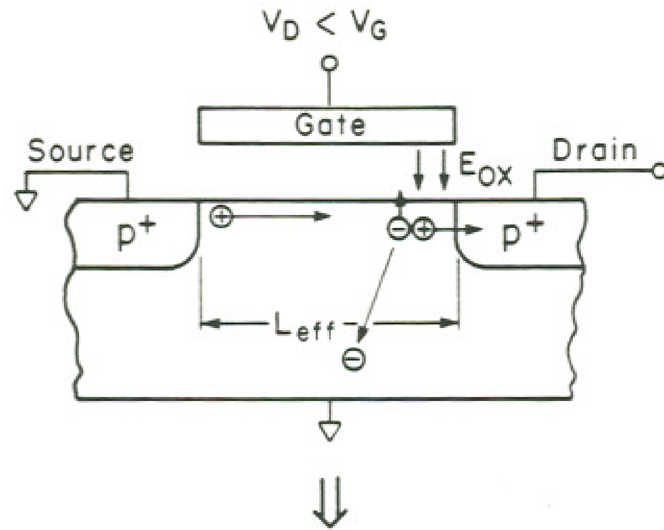
and reverse directions. The shift in Idsat is much more pronounced when measured in the reverse direction (Fig. 7). This is expected since interface state generation and the electrons trapped therein adversely affect device performance much more directly when located near the injection terminal [12,13]. The dependence of Vt and Gm shift on source/drain polarity is not appreciable. This is due to the fact these parameters were measured in the linear I-V region, where the channel extends all the way from the source to the drain.

For the case of PMOS, Idsat and Gm increase while the magnitude of Vt decreases. The decrease in the magnitude of Vt is an indication that surface damage has been created and a positive charge sheet has resulted. It is reasonable to attribute the increase in Idsat and Gm to the appreciable channel shortening operative in the stressed p-channel device. As mentioned earlier, hot electrons are accelerated by the positive gate field ($Vg > Vd$) into the gate oxide near the drain. Those electrons being trapped at the interface invert the surface to p-type, resulting in an extension of the p+ drain region and a reduction in the effective channel length (Fig. 34) [14].

To further examine this stress-induced channel shortening, the channel length was extracted with the use of the Yu method as a function of

P-Channel Hot Carrier Effects

Hot Carrier Injection and Impact Ionization



⇓

Resulting Device Degradation

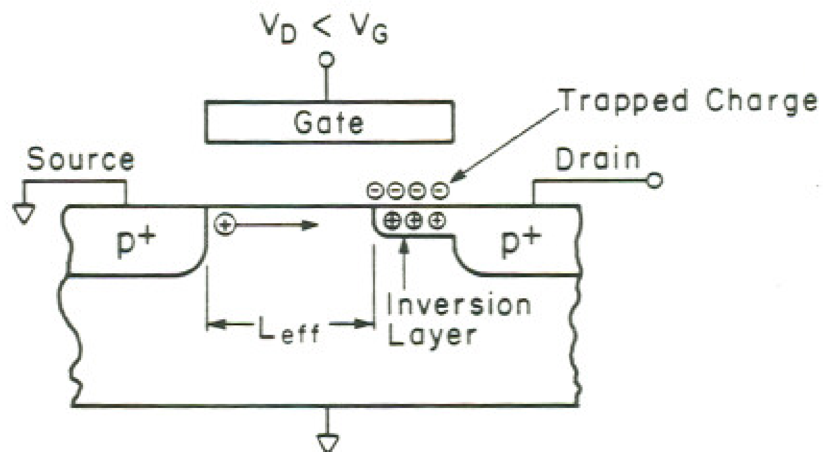


Figure 34: P-channel hot carrier induced degradation model.

stress time and is presented in Fig. 35. The effective channel length is indeed shown to decrease under both DC and AC stress time. This channel shortening is sufficient to offset possible mobility degradation and increased series resistance effects. The monotonic increase in S as a function of stress time is again consistent with the monotonic increase in Nit with stress time (Eq. (8)).

The rise in subthreshold swing as a function of stress time is distinctly bimodal for NMOS (Fig. 5). This is an interesting contrast with the p-channel case (Fig. 6). The main difference between n- and p-channel device fabrication was the presence and absence of a LDD structure. Thus, one may assume that for the n-channel device, interface state generation could begin in the lightly doped region near the drain. With increasing stress time, the high field region may extend to the drain end of the channel. The generated interface states could then increase the subthreshold swing in the usual manner.

5.3 DC Stress and AC Characterization

For fixed DC gate voltages, AC and DC measurement is shown to give rise to the same amount of parameter shift in both n- and p-channel devices (Figs. 10 and 11). From this one can conclude that the charac-

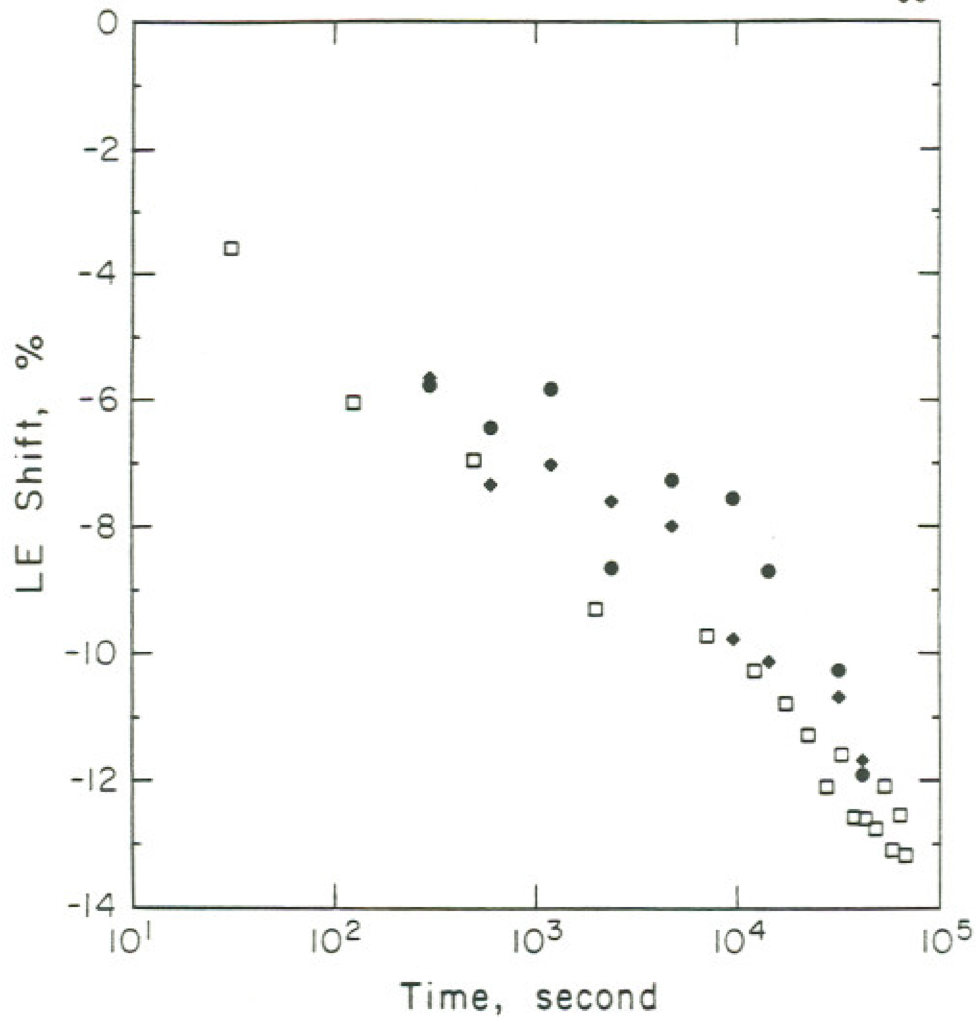


Figure 35: P-channel effective channel length vs. effective stress time: filled diamonds (◆) represent an AC stress with Vd=-8.0V drain pulse, Vg=-1.0V DC gate bias, filled circles (●) represent an AC stress with Vg=-1.0V gate pulse, Vd=-8.0V DC drain bias and open squares (□) represent a DC stress with Vd=-8.0V, Vg=-1.0V. Stress was applied with 50% duty cycle pulses at a frequency of 10 MHz.

teristic time for trapping and detrapping is indeed short (< 20 ns). Note also that with increasing magnitude of drain voltage, the degree of parameter shift also increases in both n- and p-channel devices. This again constitutes experimental evidence that the channel field further increases after pinch-off.

Both n- and p-channel devices exhibit parameter shifts that are essentially independent of gate base-level (Figs. 14 and 15). This provides an additional evidence for shallow interface state generation. Shallow defect sites are normally characterized by fast trapping/detrapping times and this is consistent with the frequency independence of parameter shift up to 3 MHz (Figs. 12 and 13).

5.4 DC and AC Stress

Here AC and DC stresses are compared. For PMOS, the parameter shifts accurately reflect the gate current vs. gate voltage curve (Figs. 22-24). More importantly, near the gate bias, Vgm of peak gate current there is no significant difference existing between the AC and DC stress effects. However, away from Vgm, there is an appreciable difference existing between gate AC and DC stress.

These p-channel data can be interpreted as follows. In the saturated

region of device operation, the electric field lines in the oxide originate from the gate and terminate in the channel. The hot electrons generated via impact ionization therefore should gain energy and be pulled toward the oxide interface, while energetic holes are rapidly drawn through the drain terminal. Hence, interface state generation is mainly done by hot electrons. The fact that the parameter shift is more or less the same for cases (a), (b) and (c), at Vgm implies that the amount of electrons capable of damaging the interface/oxide region is the same. More importantly, there does not appear to be an additional damage effect arising from dynamic stress either in terms of drain pulsing or gate pulsing at Vgm (Figs. 22 and 23).

Substrate current was measured for cases (a), (b) and (c). As can be observed from Fig. 36, the substrate currents are about the same for all cases. Since the number of impact ionization induced electron-hole pairs can be assumed to be approximately the same for these three cases, the same substrate currents imply the same gate currents. Since the gate current is a sensitive monitor of device damage, this Isub data is consistent with the parameter shift data shown in Fig. 22.

However, the situation changes when the gate voltage is appreciably away from the Vgm value. In this case, the amount of electrons capable

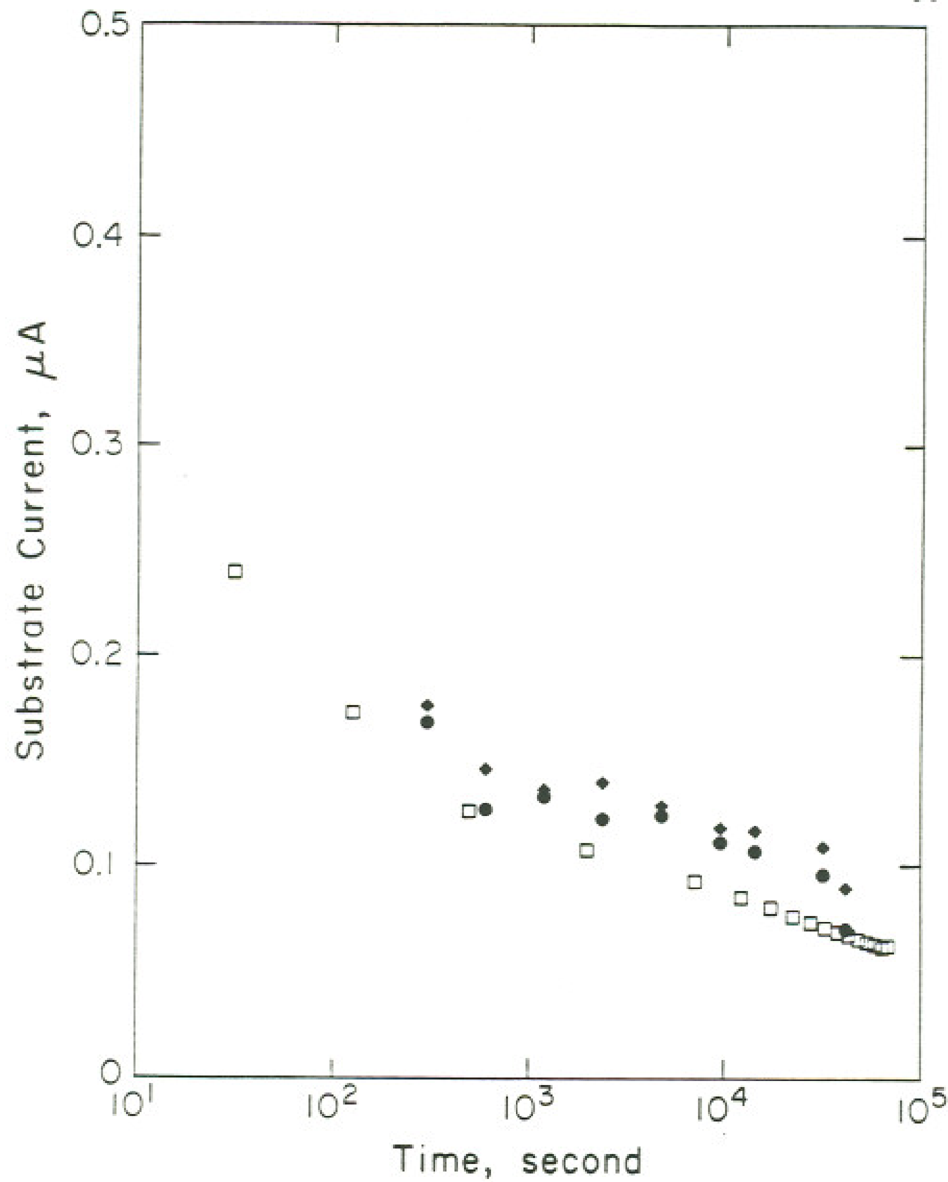


Figure 36: P-channel substrate current vs. effective stress time: filled diamonds (◆) represent an AC stress with Vd=-8.0V drain pulse, Vg=-1.0V DC gate bias, filled circles (●) represent an AC stress with Vg=-1.0V gate pulse, Vd=-8.0V DC drain bias and open squares (□) represent a DC stress with Vd=-8.0V, Vg=-1.0V. Stress was applied with 50% duty cycle pulses at a frequency of 10 MHz.

of damaging the interface is smaller for cases (a) and (b), as detailed in the discussion for Isub. Therefore, the degree of parameter shift should be much less than the case of maximum gate current. This is indeed born out by experimental data (Fig. 24). However, for the case (c), the gate voltage swings from high to low. In the process, Vgm is crossed, and the number of electrons capable of damaging the interface is the same as in Figs. 22 and 23. The degree of parameter shift should then be essentially the same as in Figs. 22 and 23 and is indeed supported by experimental data. The effect of this Vg swing is reported here for the first time.

Consider next n-channel devices. Here, the effect of AC stress is drastically different from that in p-channel devices. Specifically, even for a gate voltage of peak substrate current, Vgm, the degree of parameter shift for cases (a),(b) and (c) is rather different (Fig. 29). This is in direct contrast with the p-channel case (Fig. 22). Note that for cases (a) and (b), the parameter shifts are more or less the same. From this one can conclude that there is no dynamic effect associated with pulsing the drain voltage. Furthermore, one can also surmise that the role of the drain bias whether or not it is pulsed, is to provide the high field region near the drain, thereby enabling the carriers to gain sufficient energy for interface/oxide damage.

However, the fact that gate pulsing results in significantly larger parameter shift for all stress time considered constitutes direct evidence that dynamic stress is indeed operative. What then are the physical mechanisms responsible for this enhanced stress effect? To date there is no comprehensive theory for this.

When the NMOS is saturated, hot electrons tend to be swept toward the drain terminal. Simultaneously hot holes can either be pulled toward the gate electrode or pushed away to the grounded substrate. The larger parameter shift observed for case (c) indicates that more holes are pulled toward the gate electrode. A question can thus be raised, why is the probability of holes being pulled toward the gate higher in case (c)?

A possible answer to this question can perhaps be sought from a consideration of the oxide electric field under gate bias conditions. Near the drain end of the channel where Vd=7.5V, Vg=2.0V, for case (a), the oxide electric field emanates from the Si-SiO2 interface and terminates at the gate electrode. Its magnitude is approximately given by $Eox = |(Vg-Vd)/tox| \approx 3.7$ MV/cm. In case (b), Vd is pulsed between 0 and 7.5V, while Vg is fixed at 2.0V. Thus, during the OFF cycle (Vd=0V), the field polarity flips from case (a), with the magnitude, $Eox \approx 1.3$ MV/cm. During the ON cycle, the field polarity and magnitude are the

same as in case (a). Since hole injection into the oxide is the major cause of degradation, the device damage is done during the ON cycle of the drain pulsing. The degree of damage therefore, should be the same for (a) and (b) for a given effective stress time, and this is born out by experimental data.

For case (c), Vg was pulsed between 0 and 2.0V, while Vd was fixed at 7.5V. During the ON cycle, the polarity and magnitude of the oxide field are the same as in case (a). During the OFF cycle however, the field magnitude is increased from 3.7 MV/cm to 5.0 MV/cm. This leads to some interesting consequences. As Em is increased, the rate of impact ionization enhances. Concomitantly the trapped holes near the interface are released, thereby descreening the electric field [15]. As a result, more hot holes are injected into the gate dielectric. For a given initial number of available holes, this will reduce the substrate current. Further, more holes being injected into the gate oxide will induce more damage and hence more parameter shift. This picture is consistent with data presented in Fig. 29.

In an attempt to further examine the AC gate stress effect, the magnitude of gate voltage was increased from 2.0 to 5.0V for both DC and AC biases. The three cases (a), (b) and (c) were investigated under this

condition. Figure 30 presents the stress induced parameter shift for case (a). Note that the measured parameter shift is slightly smaller than the corresponding values from Fig. 29 for all the observed stress times. This tendency can again be understood in terms of the oxide field configuration. In this case, the magnitude of the oxide field is approximately 1.7 MV/cm, and is seen to be smaller than the corresponding value in Fig. 29.

It is important to point out that the data for cases (b) and (c) could not be obtained due to repeated device failure. This failure could be largely attributed to excessive gate current (i.e. $>$ 100 nA). This suggests that here dynamic stress is indeed operative and its effect can be drastic. This repeated device failure can perhaps be understood in terms of the oxide electric field configuration under a pulsed gate bias.

Consider case (c). During the ON cycle (Vg=5.0V) with Vd fixed at 7.5V, Eox is approximately 1.7 MV/cm, a value considerably lower than case (c) in Fig. 29. On the other hand, during the OFF cycle (Vg=0V), Eox is about 5.0 MV/cm, which is the same as that in Fig. 29. Thus, the main difference in this case is the magnitude of the oxide field swing under the gate pulsing from high to low. Specifically, for the same gate voltage fall time (10 ns), the electric field grows from 1.7 MV/cm to 5.0

MV/cm, i.e. a 60% larger growth rate. This enhanced oxide field swing could lead to: (a) more holes being pulled from the channel, thereby inducing more interface state generation, (b) mobile holes in the oxide acquiring energy from the field therein to further damage the interface and/or oxide and (c) the trapped holes near the interface being released, thereby descreening the electric field. The combined effect of these processes causes more hot holes to be injected into the gate dielectric. Further, this in turn lowers the barrier for the electrons to tunnel through from the gate electrode with the trapped holes providing the final electron tunneling states. The excessive gate current that was observed and concomitant device burn out could be due to this additional conduction channel for the gate current.

It is pointed out that device failure was also observed for case (b), in which the gate voltage was fixed at Vg=5.0V and the drain voltage was pulsed between 0 and 7.5V. Thus, during the ON cycle (Vd=7.5V), hot holes in the channel are pulled into the gate oxide and trapped near the interface. As a result, during the OFF cycle (Vd=0V), the potential barrier for electrons to tunnel through the gate is considerably lowered. This in turn could trigger the device burn out as in case (c) discussed above. In conclusion, in both cases of device failure, the dynamic stress appears to be initiated by holes being injected into the oxide. This is consistent

with the the two carrier model [16].

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CHAPTER 6

CONCLUSIONS

The highlights of the results are summarized as follows:

(i) The observed shifts in device electrical parameters due to DC stress are shown to be the same under DC and AC measurement for both n- and p-channel devices.

(ii) DC and AC measurement shows that the stress induced interface states are shallow with lifetimes less than 20 ns for both NMOS and PMOS.

(iii) For PMOS, the AC drain stress is essentially quasi-static. However, AC gate stress gives rise to device parameter shift corresponding to the worst case DC stress at all gate voltage swings.

(iv) For NMOS, the effect of AC stress is more complex. For a magnitude of the oxide electric field less than a value Eot, the AC drain stress is again quasi-static as in the PMOS case. However, the AC gate stress results in significantly increased parameter shift. The effect of this dynamic stress is shown to be drastically enhanced, leading possibly to device failure when the magnitude of the oxide field is greater than Eot. Under this condition of large oxide electric field swing, the AC drain stress also introduces a striking dynamic stress effect which can lead to

device failure.

(v) In conclusion, pronounced device degradation is shown to occur under the bias conditions such that first, high energy holes are pulled into the gate oxide, and second, an oxide electric field is large enough to induce electron tunneling from the gate. These factors are in good agreement with the two carrier model.

APPENDIX

TEST CONDITION

AC vs. DC Measurement

- N-Channel

  DC MEASURE

  in forward and reverse directions

  following 20 min packaged part cooling time

  Peak Gm, Vt and S at Vd=0.1V

  Idsat at Vd=5.0V,5.5V Vg=2.5V

  AC MEASURE

  50% duty cycle square pulse 100 Hz => 3 MHz

  10 ns rise/fall times, 20 ns settling time

  following 20 min packaged part cooling time

  Idsat at Vd=5.0,5.5V Vg=2.5,4.0V

  Vg=-4=>2V

  Vg=-3=>2V

  Vg=-2=>2V

  Vg=-1=>2V

  Vg= 0=>2V

DC STRESS

Vd=6.0,7.0,7.5V, Vg=2.0, 2.5V

for approximately 2 days

- P-Channel

  DC MEASURE

  in the forward direction

  following 20 min packaged part cooling time

  Peak Gm, Vt and S at Vd=-0.1V

  Idsat at Vd=-5.0,-5.5V Vg=-1.7,-5.0V

  AC MEASURE

  50% duty cycle square pulse 100 Hz => 3 MHz

  10 ns rise/fall times, 20 ns settling time

  following 20 min packaged part cooling time

  Idsat at Vd=-5.0,-5.5, Vg=-1.7,-4.0,-5.0V

  Vg=4=>-2V

  Vg=3=>-2V

  Vg=2=>-2V

  Vg=1=>-2V

  Vg=0=>-2V

DC STRESS

Vd=-7.0,-8.0,-8.5,-9.0,-10.0V   Vg=-1.7V

for approximately 20 hrs.

- Charge Pumping Measurement

  Procedure

  1. A pulse train is applied to the gate.

  2. A small reverse-bias is applied to the source and drain.

  3. The DC substrate charge pumping current is recorded.

AC vs. DC Stress

- N-Channel

  DC STRESS

  Vd=7.0,7.5V   Vg=2.0V

  Peak Gm measured following 20 min cooling time

  AC DRAIN STRESS

  Vd=7.0,7.5V at 10 MHz

  50% duty cycle square pulse

  10 ns rise/fall times, 20 ns settling time

  DC GATE Vg=2.0V

  for approximately 40 hrs. (20 hrs. active duty cycle)

  Peak Gm measured following 20 min cooling time

AC GATE STRESS

Vg=2.0V at 1 MHz and 10 MHz

50% duty cycle square pulse

10 ns rise/fall times, 20 ns settling time

DC DRAIN Vd=7.0,7.5V

approximately 40 hrs. (20 hrs. active duty cycle)

Peak Gm measured following 20 min cooling time

- P-Channel

  DC STRESS

  Vd=-8.0V, Vg=-1.0,-2.0,-5.0V

  for approximately 20 hrs.

  Idsat measured following 20 min cooling time

  AC DRAIN STRESS

  Vd=-8.0V at 10 MHz

  50% duty cycle square pulse

  10 ns rise/fall times, 20 ns settling time

  DC GATE Vg=-1.0,-2.0,-5.0V

  for approximately 40 hrs. (20 hrs. active duty cycle)

  Idsat measured following 20 min cooling time

  AC GATE STRESS

  Vg=-1.0,-2.0,-3.0,-4.0,-5.0V at 10 MHz

Vg=+2=>-1V,+1=>-1V at 10 MHz

10 ns rise/fall times, 20 ns settling time

DC DRAIN Vd=-8.0V

for approximately 40 hrs. (20 hrs. active duty cycle)

Idsat measured following 20 min cooling time

VITA

The author was born in San Mateo, California. She later moved to Portland, Oregon where she graduated from Woodrow Wilson High School. She received a B.S. in Nursing from Oregon Health Sciences University in 1970. She continued to work as a perinatal nurse while going to school on a part-time basis. She earned a B.S. in Mathematics with honors from Portland State University in 1982 and a B.S.E.E. with honors from University of Portland in 1984. She is a member of Eta Kappa Nu, an electrical engineering honorary and is listed in the 1984 Who's Who Among Students in American Universities and Colleges.

In 1984 she joined Intel Corporation where she worked as a process and device engineer. In 1985 she entered Oregon Graduate Center where she spent the first year in the Department of Materials Science and Engineering and the following two years in the Department of Applied Physics and Electrical Engineering. She rejoined Intel Corporation to work in research and development and reliability for three summers while a graduate student.

The author is currently employed at Intel Corporation as a reliability engineer.